INTEGRATED CIRCUITS ENGINEERING
AND
INTEGRATED CIRCUITS MANUFACTURING

CATALOG

REVISED EDITION JULY, 1977

TEKTRONIX, INC.

INTEGRATED CIRCUITS ENGINEERING

AND

INTEGRATED CIRCUITS MANUFACTURING

Revised Edition

June, 1977

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I. GENERAL CIRCUITS

IN Production
by CER

MO36E | 155-0022-00 155-0022-01 | CHANNEL SWITCH

Description:

This IC selects one or mixes two input analog signals in response to a digital input. In its simple application, it is a double-pole double-throw selector of one of two balance input signals. Its more sophisticated role is in providing signal steering in dual-trace vertical and horizontal amplifiers.

It is designed for two balanced input signals of 25 mV/division per side into 50 ohms per side (0.5 mA/division). The 50 Ω terminations to ground are external to the package. A current gain of one is intended. The gain setting resistors are external to the package. Total dynamic range is ± 15 divisions (± 7.5 mA).

The switch output is at a + 5 V DC level. It is a current output into a resistance of 50 Ω per side. Side-to-side diodes are included inside the IC for limiting the differential voltage swing of the output. The risetime of the switch is less than 1 ns.

A logic-one controls the selection of CH1 - CH2, OFF and ADD. The CH1 - CH2 input permits high speed switching between the two inputs suitable for "CHOPPED" or "ALTERNATE" operation at frequencies up up to 1 MHz or greater. Logic levels are -0.5 V CH1 and +0.0 CH2 into a high impedance. The OFF input inhibits both inputs from reaching the output. Logic levels and input impedance are the same as the CH1 - CH2 selections with the OFF level being +1.0 V. The ADD input requires a + 5 volts input to sum the two input sigals at the output terminals. The OFF mode supercedes the other two inputs while the ADD mode requires the other two inputs to be negative.

The common-mode current output of the signal channel is maintained and constant for the various modes.

M036E (continued)

Characteristics:

Low Frequency Current Gain	60 Minimum
Low Frequency α	0.94 Minimum
Output Impedance	100 KΩ Nominal
Output Current Swing	± 7.5 mA Maximum
Input Capacitance Each Side	2.3 pF Nominal
Output Capacitance Each Side	5.2 pF Nominal
Switching Time	20 ns Maximum
Signal Risetime: $Rs = 100$ $R_e = 82$ $R_L < 50$	1.0 ns Maximum
Differential DC Offset Between Modes	20 mV Maximum
Gain Difference Between Modes: $A_I = 1$ Output Current Swing	0.5% Maximum < ± 2.5 mA
Low Frequency Opposite Channel Isolation	750:1 Minimum F < 10 kc
100 MHz Opposite Channel Isolation	100:1 Nominal

Other characteristics are described in the listing of the terminals.

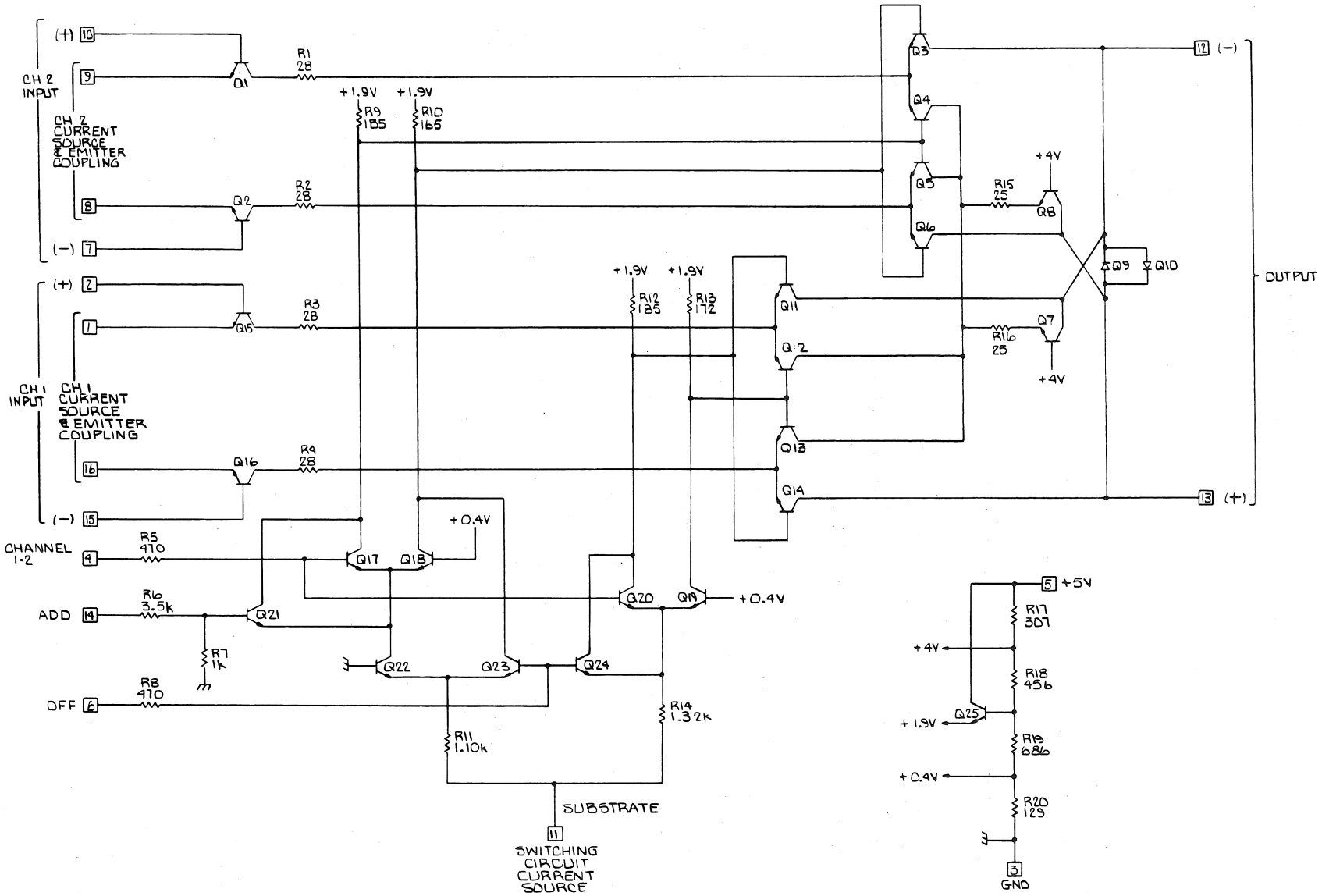
Package: 16 DIP

Designer: Gene Andrews

ICE Contact: Einar Traa

Instrument Usage:

7603K (3)	7603H (3)	7603G (3)	7603N11S (2)
R7603 (3)	1430 (2)	147 (2)	148 (2)
7313 (3)	7603 (3)	7613 (3)	5A38 (1)
4503 (1)	335K (2)	1461 (1)	1441 (1)
7704A (5)	7912 (1)	5403 (2)	7903 (1)
7403 (2)	7D12 (1)	7844 (2)	5441 (2)
7D11 (1)	5440 (2)	7504 (4)	7514 (4)
R7704 (3)	P7001 (2)	7704A (5)	5433 (2)
7623A (3)	149 (2)	5443 (2)	7A18 (2)
7904 (1)	7633 (3)	A7704 (5)	7012 (1)



ENGR	Einar Troa	10-24-74	PROCESS	50/450 Ω/□
DWN BY	Pam Cherrie	10-23-74	PACKAGE	16 PIN DIP
CHK BY	[illegible]	11-7-74	DIE SIZE	40 mil × 50 mil
TYPE	MONOLITHIC	CHANNEL SWITCH		M036E
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0022-00		

IN Production
by CER

M047 155-0031-01 QUAD TIMING UNIT

Description:

Generates four separate and independent timing intervals.

Input Required: RTL, current limiting required.

Output Available: During the timing interval, the output is at 5 V through 5 kΩ. During the off period, the output will sink 5 mA below 0.4 V.

RC Required: Resistor should supply no more than 750 μA. Allow 5 μA for the operation of the IC. For narrow input pulses (less than 0.5 ms per μF of capacitance), the timing ramp will occur from 1 V to 3.6 V. Wider input pulses will change the ramp to 0 V to 3.6 V.

Operation: The circuit is a pulse stretcher in operation. The output will remain positive for a time set by the width of the input pulse plus a timing interval set by an RC.

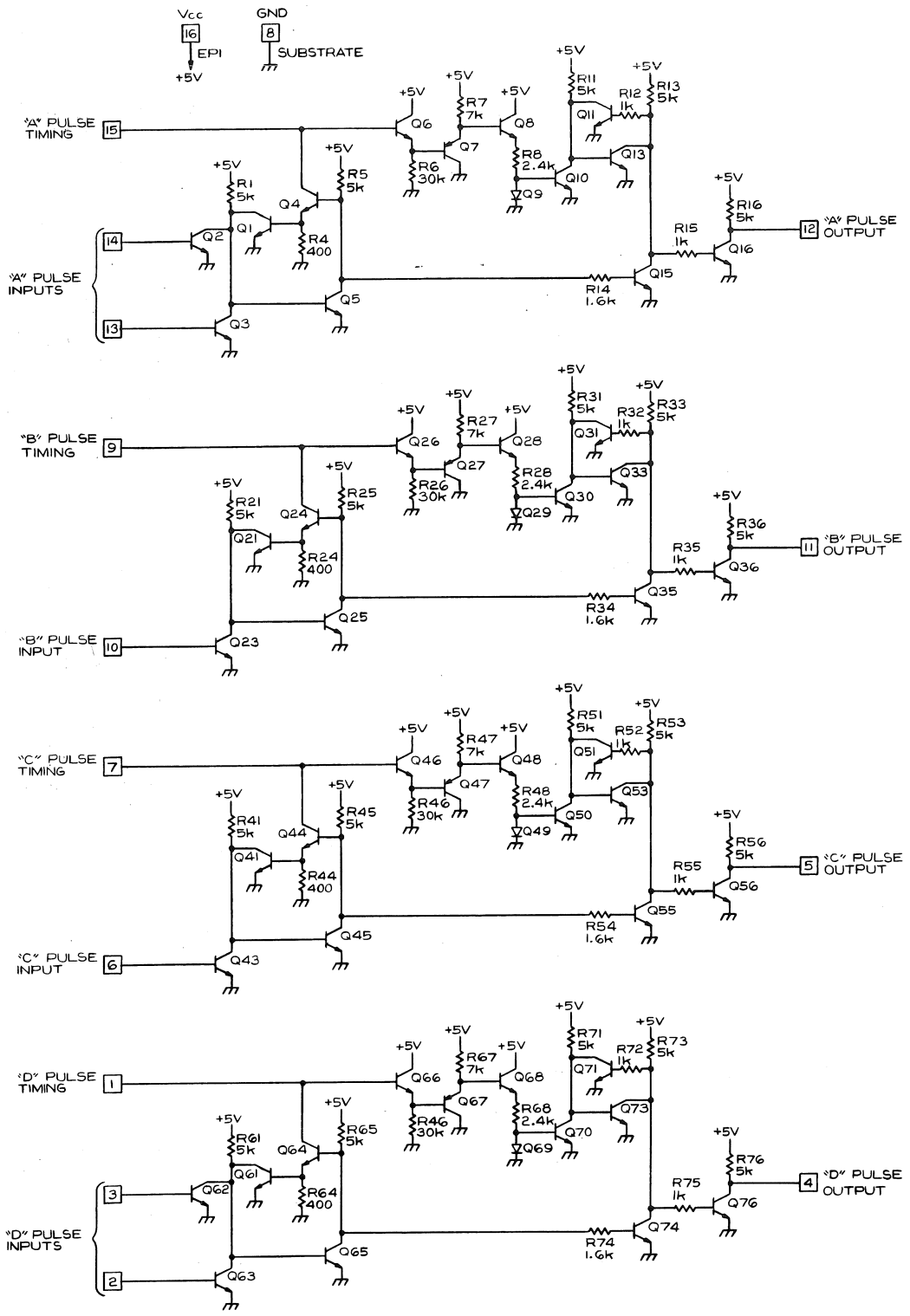
Power Supply: V_{CC} + 5 V

Package: 16 DIP

Designer: Mike Nash

ICE Contact: Mike Metcalf

Instrument Usage: None



ENGR	M. H. Mustard	12-10-76	PROCESS	200 Ω/□
DWN BY	J. Langley	4-19-76	PACKAGE	16 PIN DIP
CHK BY	David Van Cleve	3-22-77	DIE SIZE	50 mil X 50 mil
TYPE	MONOLITHIC	QUAD TIMING UNIT		M047
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0031-01		

IN Production
by CER

M050B 155-0047-00 DUAL OUTPUT AMPLIFIER

Description:

Two variable gain amplifiers on a single chip. The input is a single-ended voltage and the output a differential current. Intended to be used as mini-scope output amplifiers.

Characteristics:

Gain (Current Output	Adjustable From 0.5 to 5 mA/Volt
Bandwidth.	Determined by Load and Source Impedances
Input Impedance.	20 k - A
DC Balance	Adjustable Internally Over Entire Dynamic Range

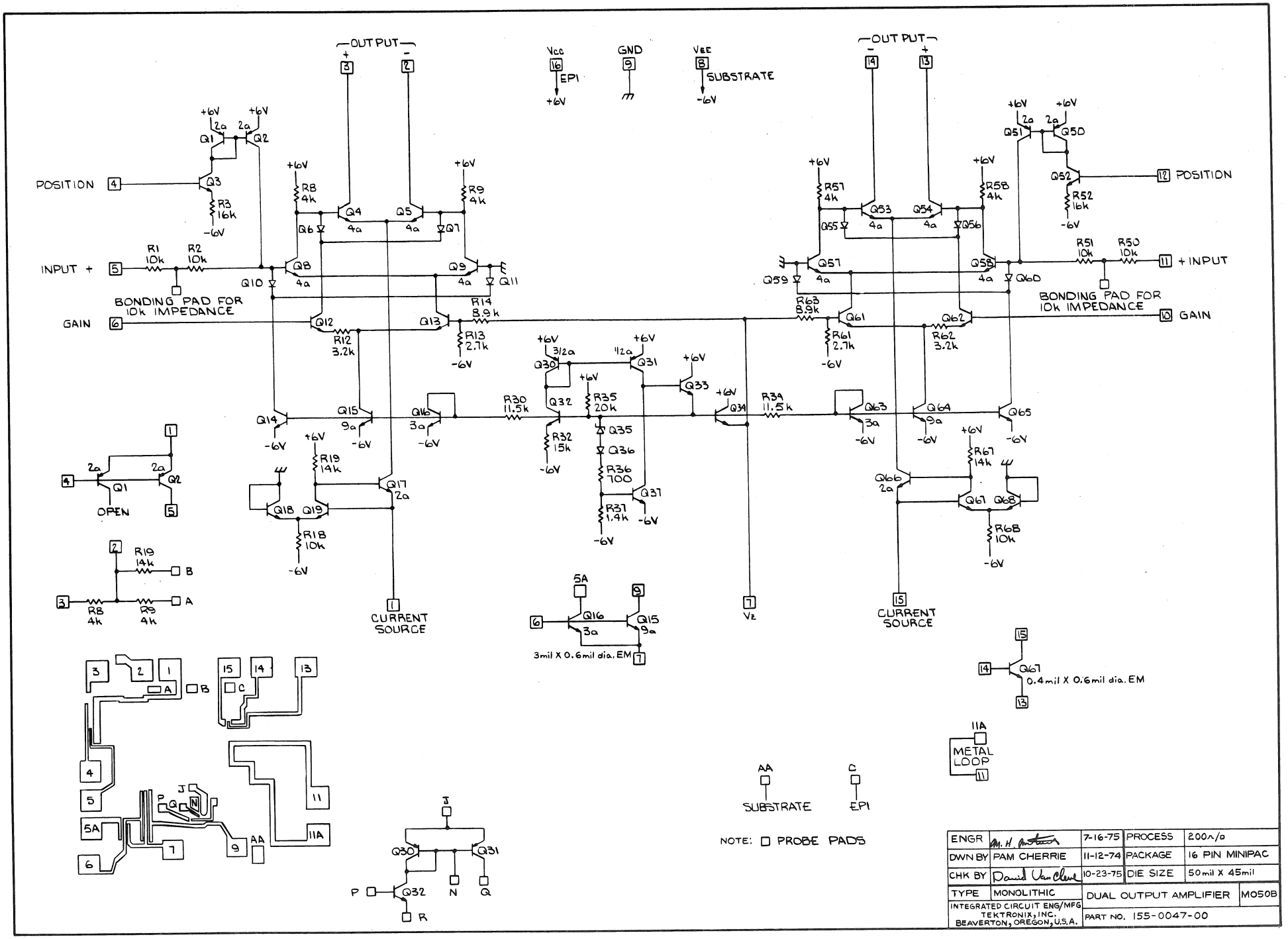
Power Supply: V_{CC} + 6V
V_{EE} - 6V

Package: 16 DIP

Designer: David Allen

ICE Contact: Mike Metcalf

Instrument Usage: 211 (1)
212 (1)
214 (1)


OUT PUT
Vcc
GND
VEE
EPI
SUBSTRATE
POSITION
INPUT +
GAIN
BONDING PAD FOR 10k IMPEDANCE
+ INPUT
OPEN
CURRENT SOURCE
Vz
3mil X 0.6mil dia. EM
0.4mil X 0.6mil dia. EM
METAL LOOP
SUBSTRATE
EPI
NOTE: PROBE PADS
ENGR
DWN BY PAM CHERRIE 11-12-74
CHK BY 10-23-75
7-16-75
PROCESS 200Ω/□
PACKAGE 16 PIN MINIPAC
DIE SIZE 50mil X 45mil
TYPE MONOLITHIC
DUAL OUTPUT AMPLIFIER
M050B
INTEGRATED CIRCUIT ENG/MFG
TEKTRONIX, INC.
BEAVERTON, OREGON, U.S.A.
PART NO. 155-0047-00

IN Production
by CER

M061 155-0034-00 DUAL DIODE

Description:

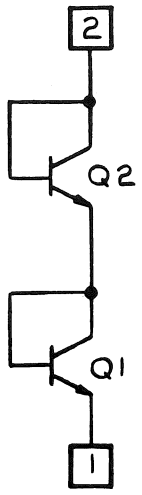
Diode Pair - matched for V_{BE} and specific thermal tracking with temperature.

NOTE: Foot of "T" stamped on side of case is the cathode.

Package: Micro T

ICE Contact: Carlos Madina

Instrument Usage: 010-0227-00 (1)



ENGR	C. MADINA	9-25-75	PROCESS	200 Ω/□
DWN BY	J. Langley	2-12-75	PACKAGE	MICRO T
CHK BY	David Van Cleve	10-23-75	DIE SIZE	60 mil X 50 mil
TYPE	MONOLITHIC	DUAL DIODE		M061
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0034-00		

IN Production

By CER

M071E 203-0071-00 CHANNEL SWITCH

Description:

Has two push-pull inputs. 50 ohm terminating resistors are external to the package. Has one push-pull output. Output impedance - 50 Ω per side. Operating modes: CH1/CH2, ADD or OFF. Provides remote selection of the vertical signal for the 7904.

IC Process: SHF II, Nichrome resistors, two-layer metal.

Input: 25 mV/Division per side, maximum signal limits: ! 30 division, usable signal limits: ! 15 division, maximum common mode signal: ! 0.5 volt, input impedance: 50 Ω ! 1%.

Risetime: Approximately 500 psec, 25 Ω source, 50 Ω load.

Gain: 2X Current or voltage gain (with a 50 Ω load). Insertion gain: 2X (50 Ω).

Output: DC lead + 6 volts, current: 80 mA, maximum current swing: ! 20 mA into 50 Ω load, impedance: 50 Ω, capacitance: Approximately 4.5 pf.

Substrate: 12 mA at -3.7 volts.

Power Supply: > 900 mW.

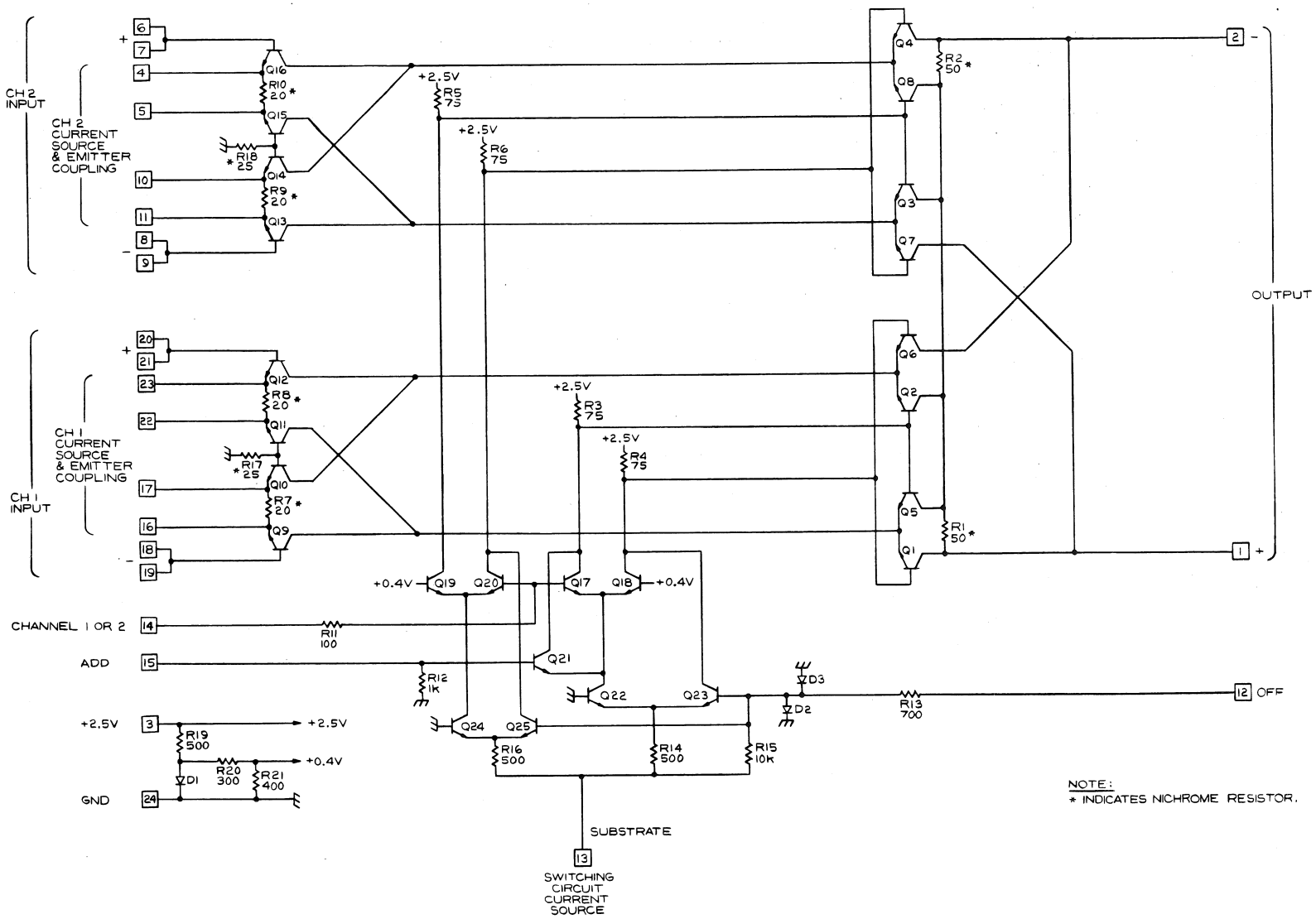
Package: 24 Pin package, short bonding wires, 100 Ω p.p. transmission line, 900 mW power dissipation.

Designer: Hans Springer

ICE Contact: George Wilson

Instrument Usage:

155-0060-00		155-0060-01	
7903	(1)	7903	(1)
7904	(1)	7904	(2)
7912	(1)		



ENGR	Dick Wang	6-30-75	PROCESS	SHF II
DWN BY	J. Langley	6-17-75	PACKAGE	24 PIN
CHK BY	C. WESTON	10-9-75	DIE SIZE	60mil X 65mil
TYPE	MONOLITHIC	CHANNEL SWITCH		M071E
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 2[illegible]-0071-90		

IN Production
By CER

M091B 155-0067-02 POWER SUPPLY REGULATOR

Description:

Designed to control DC to DC inverter supplies, it provides the necessary circuitry to do all regulation and protection of the inverter system.

Inputs are provided to: a) sense and control secondary voltage faults (detected by a bidirectional; ground-referenced node, Pin 2), b) sense and limit maximum inverter current (Pin 13), c) sense line voltage (Pin 3), present (Pin 3), and d) sense inverter current phase (Pins 10 and 11).

Outputs (Pins 8 and 9) control the inverter base drive circuitry.

The circuit provides its own positive supplies; a negative supply of -2 to -3 volts must be provided externally.

Power Supply: V_{CC}: requires a current source, internally regulated at 7.5 V.
V_{EE}: -2 V.

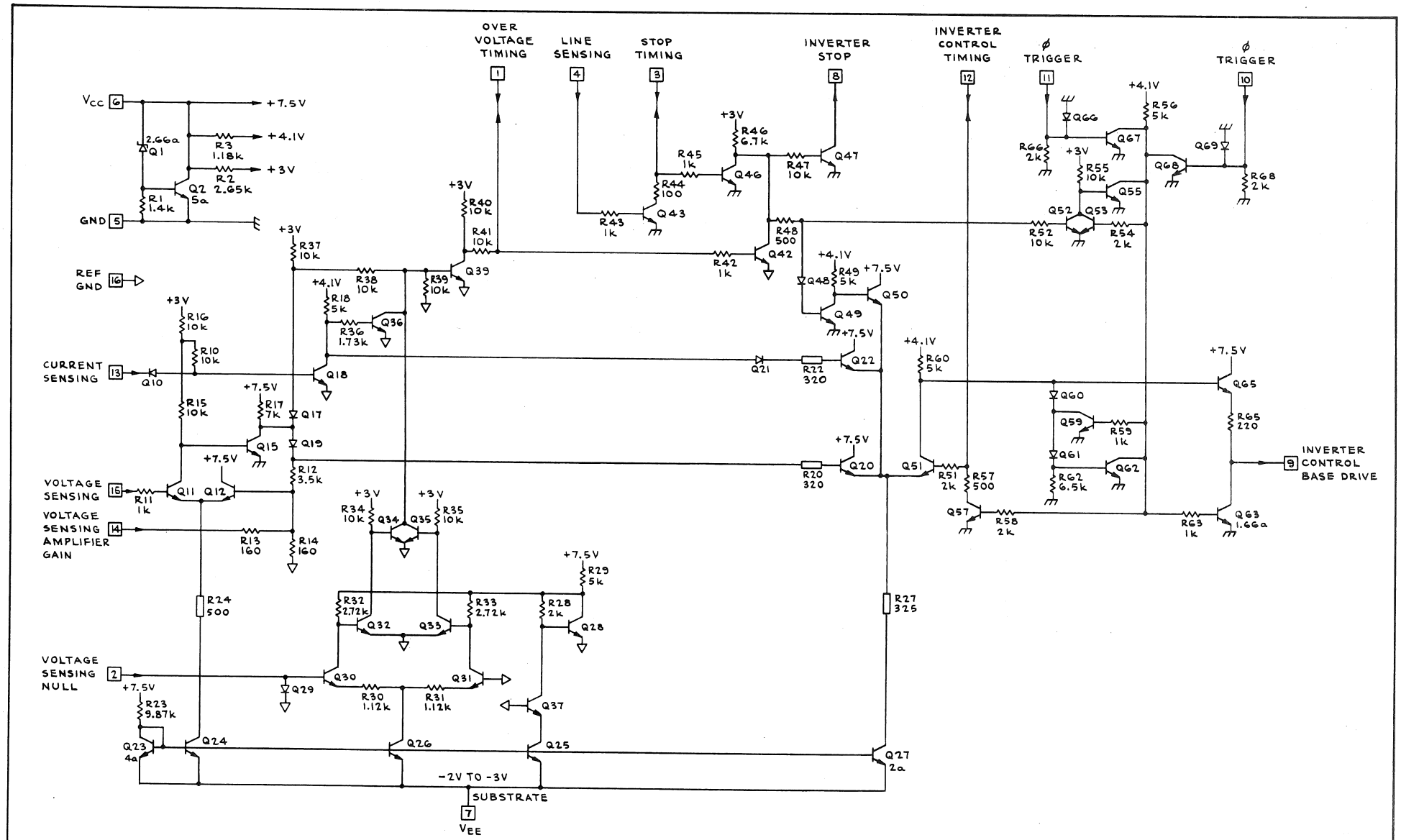
Package: 16 DIP

Designers: Joe Burger/Gene Andrews

ICE Contact: Mike Metcalf

Instrument Usage:

155-0067-01	155-0067-02			
P001	485	(1)	7844	(1)
	7904	(1)	7903	(1)
	7704A	(1)	7912	(1)
	4851	(1)	P7001	(1)
	4852	(1)	434	(1)
	A7704	(1)	7704A	(1)



NOTES:

1. —▭— INDICATES CROSS UNDER RESISTOR.

ENGR	M.H. Roberts	3-25-75	PROCESS	200Ω/□
DWN BY	Ron Hankins	3-7-75	PACKAGE	16 PIN DIP
CHK BY	C WESTON	9-24-75	DIE SIZE	55 x 55 mils
TYPE	MONOLITHIC	POWER SUPPLY REGULATOR		M091B
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0067-02		

IN Production
By CER

M095A 155-0091-00 CHANNEL SWITCH

Description:

Consists of one Ft-Doubler cascode stage per channel, with parallel outputs. The channel switching is done by switching the dual common base transistors in these cascode stages. The circuit also has provisions for trigger pick-offs from each channel.

The input is 20 mV/DIV into built-in 50 ohm terminations, at a DC level of -5 V. The output is 1 mA/DIV into reverse terminated 50 ohm line (ie., 20 ohm x 1 mA = 25 mV/DIV at ground DC level).

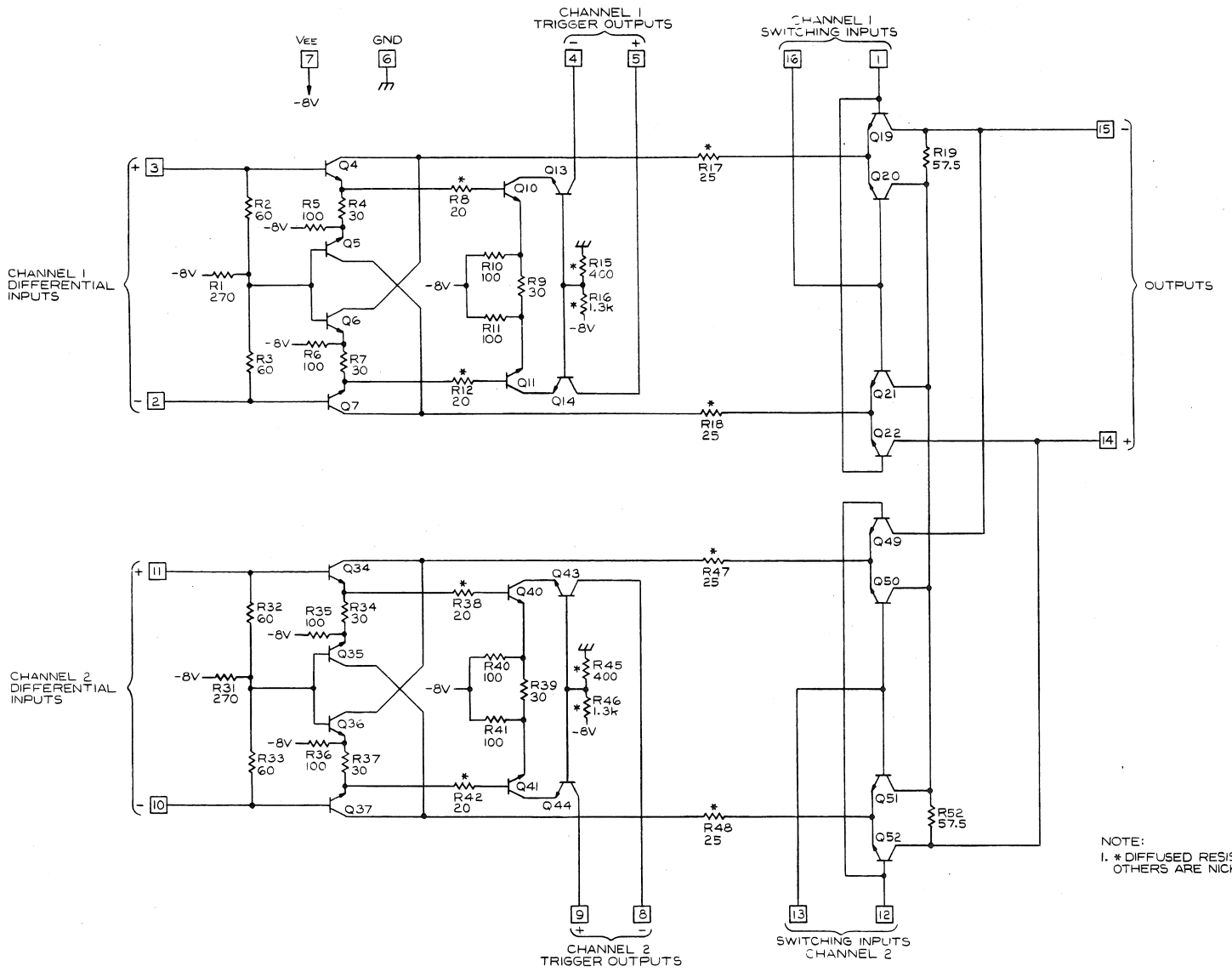
Power supplies are -8 V and ground dissipation is 1 watt.

Package: 16 lead large pattern TO-8 w/brazed Moly Shim

Designer: Einar Traa/Jim Woo

ICE Contact: Einar Traa

Instrument Usage: 475 (1)



NOTE:
1. * DIFFUSED RESISTORS, OTHERS ARE NICHROME.

ENGR	Jim Moo	3-5-76	PROCESS	SHF II
DWN BY	J. Langley	2-3-76	PACKAGE	16 PIN TO-8 LG.
CHK BY	Linda Bazyl	3-10-76	DIE SIZE	60mil X 60mil
TYPE	MONOLITHIC	CHANNEL SWITCH		M095A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0091-00		

IN Production

M101A 155-0106-00 NORMALIZING CIRCUIT

Description:

The M101A is a programmable function generator constructed as an integrated circuit. It produces an output voltage or current which is a programmable function of an input voltage or current at 19 evenly spaced values of the input voltage or current. For values of the input signal between 19 points, the output is a linear interpolation between the output values at the nearest points. The programming of each point is independent of all other points, and the output at any point can be established by the ratio of two resistors.

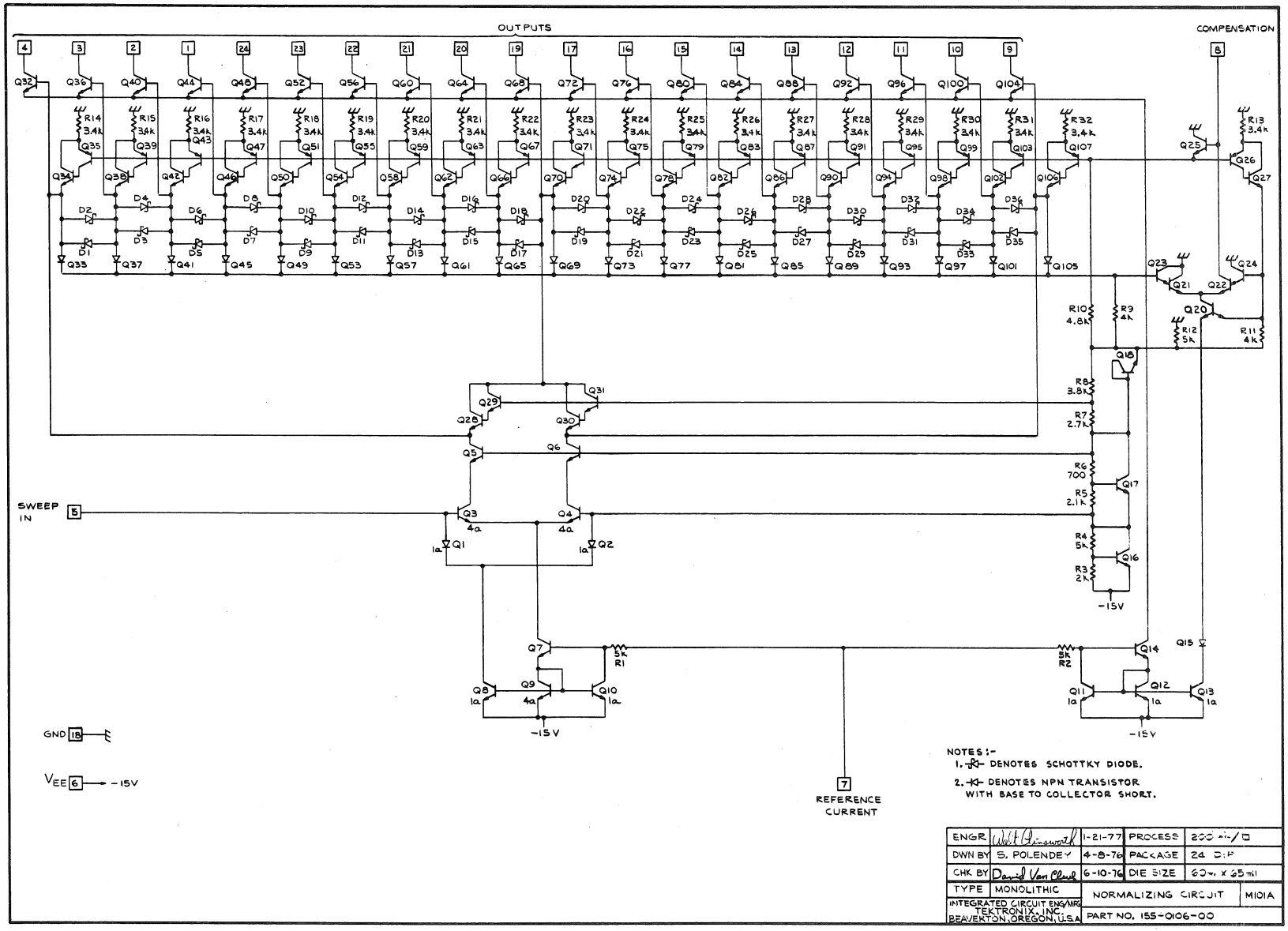
Power Supply: V_{CC} 0
V_{EE} -15 V.

Package: 24 DIP

Designer: John Pace

ICE Contact: Walt Ainsworth

Instrument Usage: J20 (2)


OUTPUTS
COMPENSATION
SWEEP IN
GND
VEE
-15V
REFERENCE CURRENT
NOTES:-
1. DENOTES SCHOTTKY DIODE.
2. DENOTES NPN TRANSISTOR WITH BASE TO COLLECTOR SHORT.
ENGR
DWN BY S. POLENDEY 4-8-76
CHK BY 6-10-76
PROCESS
PACKAGE 24 D.I.P.
DIE SIZE
TYPE MONOLITHIC
NORMALIZING CIRCUIT
M101A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.
PART NO. 155-0106-00

IN Production

M115A 155-0118-00 7L5 VERTICAL CONTROL

Description:

The M115 is a MOS IC designed to allow the user to select a reference level within the dynamic range of most instruments. The selection may be made through a knob command, or it may be remotely programmed. Scale factor selection is also included.

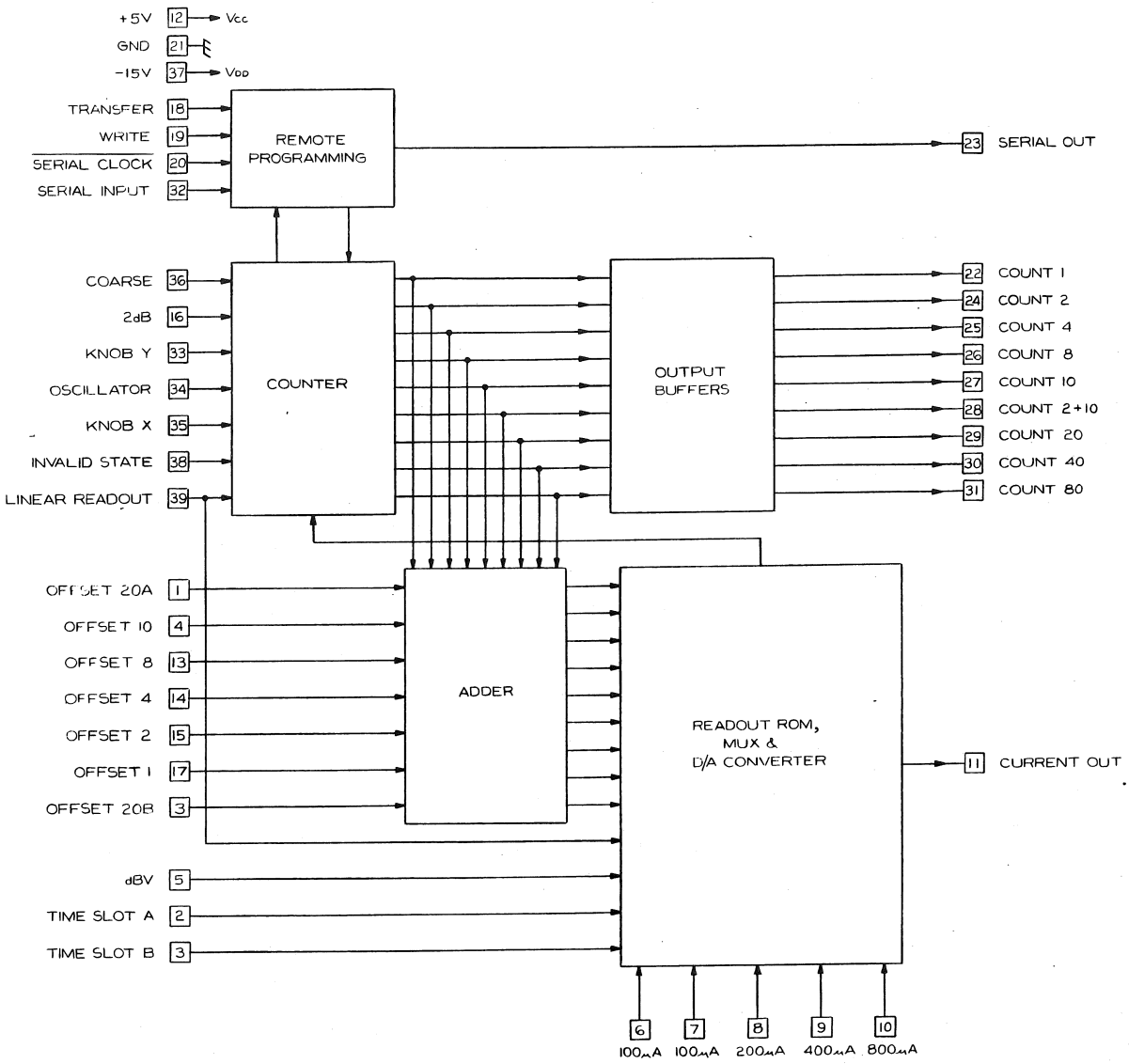
The IC accepts offset constant inputs which may be used to control the upper limit of the instruments dynamic range. An invalid state input allows the user to also truncate the lower limit of operation if desired.

The M115 counter states are direct outputs which may be used to control external circuitry such as amplifiers and attenuators.

The circuit is designed to accept TTL inputs. The outputs (other than readout) will interface directly to LPTTL or CMOS circuits.

The M115 provides for logarithmic (dB) or linear readout. It is designed to interface directly with the 7000 series CRT readout system and/or with a BCD-to-seven segment display decoder/driver.

Power Supply:	V_{DD} = -15V V_{CC} = +5.0V
Package:	40 PIN Leadless
Designer:	Dave Allstott
ICE Contact:	Randy Young
Instrument Usage:	7L5



ENGR	da Finke	2-10-76	PROCESS	P-MOS
DWN BY	J. Langley	2-6-76	PACKAGE	40 PIN LEADLESS
CHK BY	F Winsky	4-21-76	DIE SIZE	151mil X 173mil
TYPE	MONOLITHIC	7L5 VERTICAL CONTROL BLOCK DIAGRAM		M115A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0118-00		

IN Production

M180 155-0157-00 DIGITAL STORAGE VERTICAL CONTROL

Description:

The M180 and M181 acquire a low speed, low repetition rate waveform, store the waveform in a digital form, and then redisplay the waveform at a higher rate. Also, the waveform may be digitally processed to provide several types of displays. The waveform is segmented into 1024 horizontal locations. An eight bit vertical value is computed for each horizontal location and stored in an external RAM. The memory can be split into two smaller memories of 512 locations. One waveform can be retained for comparison with a waveform acquired later.

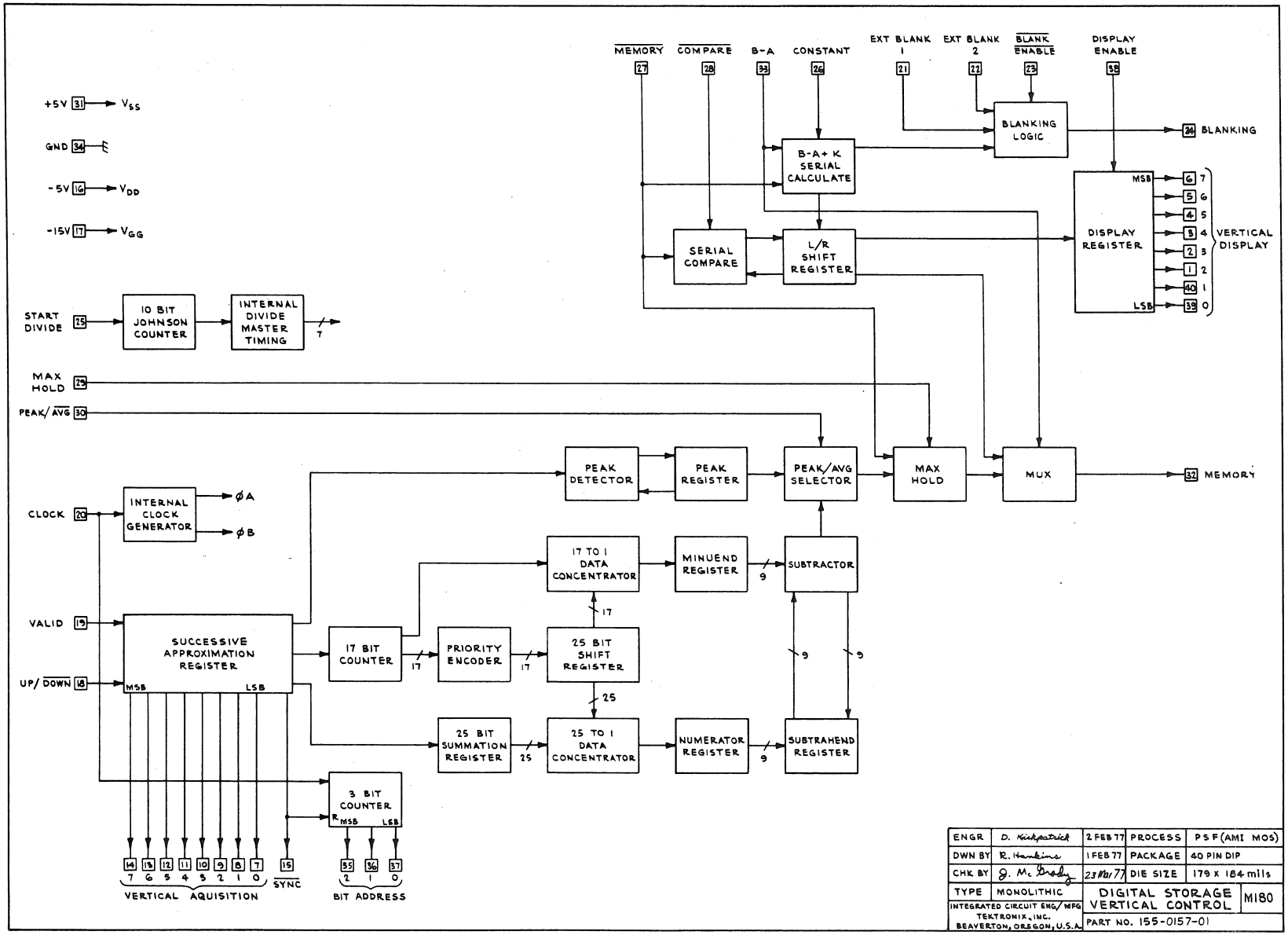
The M180 constantly digitizes a waveform using the successive approximation technique. All vertical values are summed for a single horizontal location. The number of vertical values is counted. These two numbers are divided giving an average value. Also, the largest vertical value is retained. The process begins anew at each horizontal location. The largest value or the average value is then selected and stored. The selected value can be compared with the current memory content and the larger of the two stored.

The M181 determines the horizontal position using a ten bit tracking ADC. A programmable logic array in the M181 controls the display. The user can display either half of the memory, both halves interlaced, or the algebraic difference between the two halves. The M181 controls the addressing of memory. Provisions exist for external circuitry to read and modify the memory.

Either circuit by itself is useless, but the two together form a complete digital package. The memory and the analog portion of the A/D and D/A converters are external.

M180 (continued)

Power Supply:	+5/50ma, -5/50ma, -15/10μa
Package:	40 pin Dual in line
Designer:	Don Kirkpatrick
ICE Contact:	Randy Young
Instrument Usage:	7L5, 7L13, 7L18, 49X



ENGR	D. Kirkpatrick	2 FEB 77	PROCESS	PSF (AMI MOS)
DWN BY	R. Hawkins	1 FEB 77	PACKAGE	40 PIN DIP
CHK BY	G. McGrady	23 Mar 77	DIE SIZE	179 x 184 mils
TYPE	MONOLITHIC	DIGITAL STORAGE VERTICAL CONTROL		M180
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0157-01		

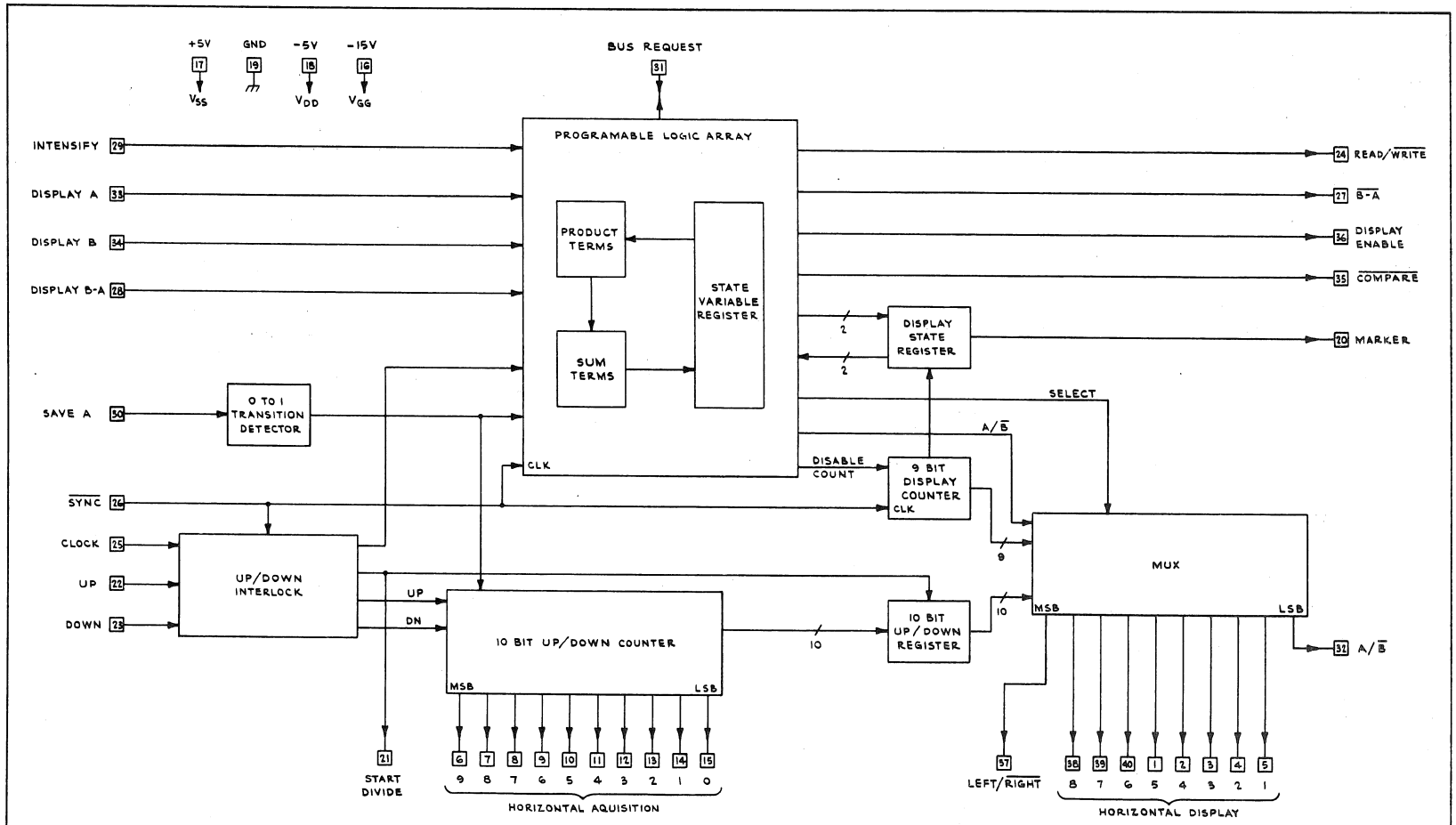
IN Production

M181	155-0158-00 155-0158-01	DIGITAL STORAGE HORIZONTAL CONTROL

Description:

This circuit must be used with the M180. See the M180 for a complete description.

Power Supply:	+5/40ma, -5/40ma, -15/10μa
Package:	40 pin Dual in line
Designer:	Don Kirkpatrick
ICE Contact:	Randy Young
Instrument Usage:	7L5, 7L13, 7L18, 49X



ENGR	D. Kirkpatrick	7 FEB 77	PROCESS	PSF (AMI MOS)
DWN	R. Hankins	4 FEB 77	PACKAGE	40 PIN DIP
CHK	J. McBroom	22 Mar. 77	DIE SIZE	130 X 151 mils
TYPE	MONOLITHIC	DIGITAL STORAGE HORIZONTAL CONTROL		M181
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0158-01		

II. OPERATIONAL AMPLIFIERS

IN Production
by CER

M053B | 155-0035-00 155-0116-00 | QUAD OPERATIONAL AMPLIFIER

Description:

Four operational amplifiers on a chip with the following specifications:

Maxium Power Dissipation	500 mW at 25°C Derate 5 mW/°C to 125°C
Power Supplies	± 5 to ± 15 V
Open Loop Gain	≥ 1500
Gain Bandwidth	≥ 80 MHz
Input Offset	≤ 5 mV
Output Swing	- 0.7 w.r.t. Input Level To + V_{CC} - 1.5V
Maximum Output Current.	20 mA, Limited By Package Dissipation

The amplifier is stable in all modes without external compensation if C_L ± 10 pF.

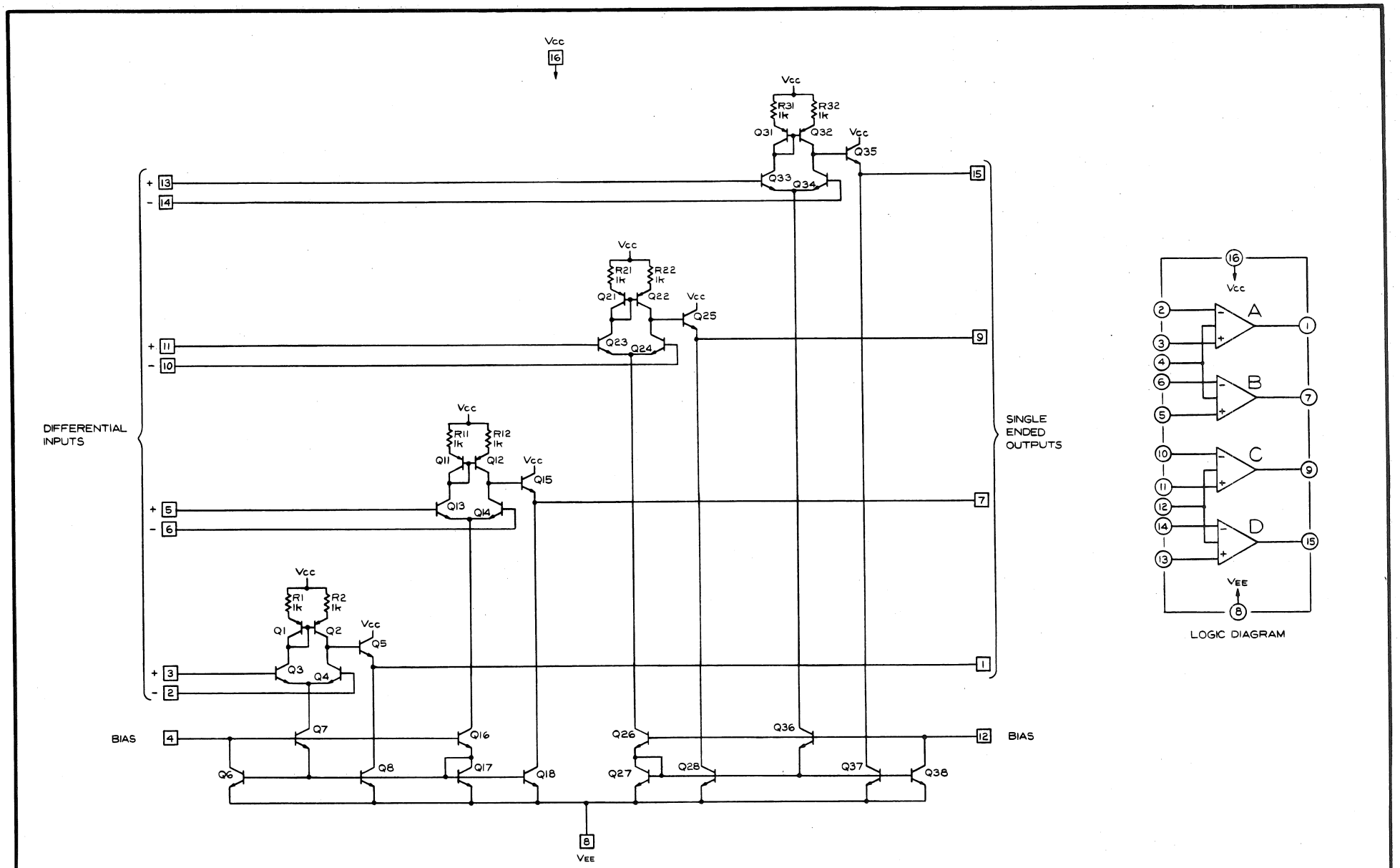
Package: 16 DIP Plastic (-0035)
16 DIP Ceramic (-0116)

Designer: Mike Metcalf

ICE Contact: Mike Metcalf

Instrument Usage:

3110 (1)	7L5 (2)
4010 (1)	7L12 (3)
4011 (4)	7L13 (3)
4012 (2)	7S12 (2)
4013 (2)	7T11 (2)
4602 (1)	S6 (1)
613 (2)	P7001 (1)
653 (1)	1461 (2)



ENGR	M. H. Arthur	6-30-75	PROCESS	200 A/a
DWN BY	J. Langley	6-18-75	PACKAGE	16 PIN DIP
CHK BY	C. WESTON	10-9-75	DIE SIZE	40mil X 40mil
TYPE	MONOLITHIC	QUAD OPERATIONAL AMPLIFIER		M053B
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0035-00/155-0116-00		

IN Production
by CER

M053B 155-0057-00 2 OP AMPS - 2 CURRENT SOURCES

Description:

This is a variation of the Quad-Op-Amp chip (M053) hooked up in such a fashion that Amplifiers "A" and "B" are operative as amplifiers, while "C" and "D" pin-outs are arranged in such a fashion as to become a constant current source rather than operating as amplifiers. The magnitude of constant current available is approximately 4 times the bias current as measured at Pin 11 when the output is taken from Pins 8, 9, 10, 12, 13, and 14 all connected together.

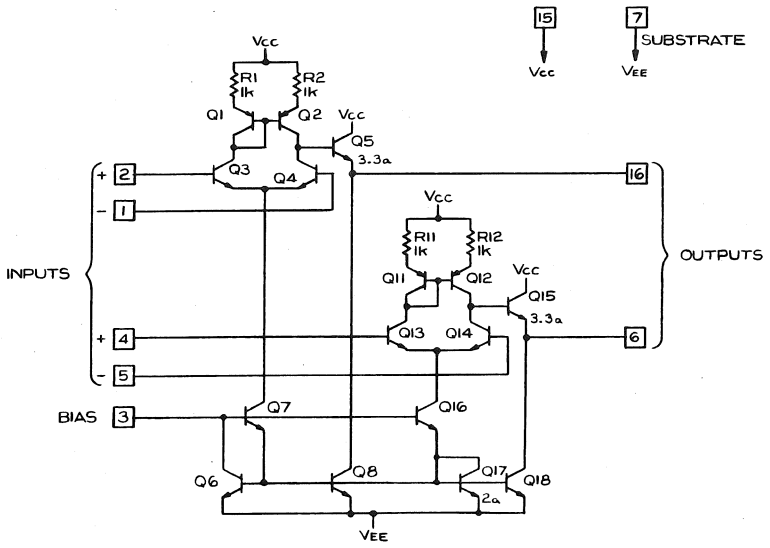
Power Supply: V_{CC} + 5 to + 15
V_{EE} - 5 to - 15

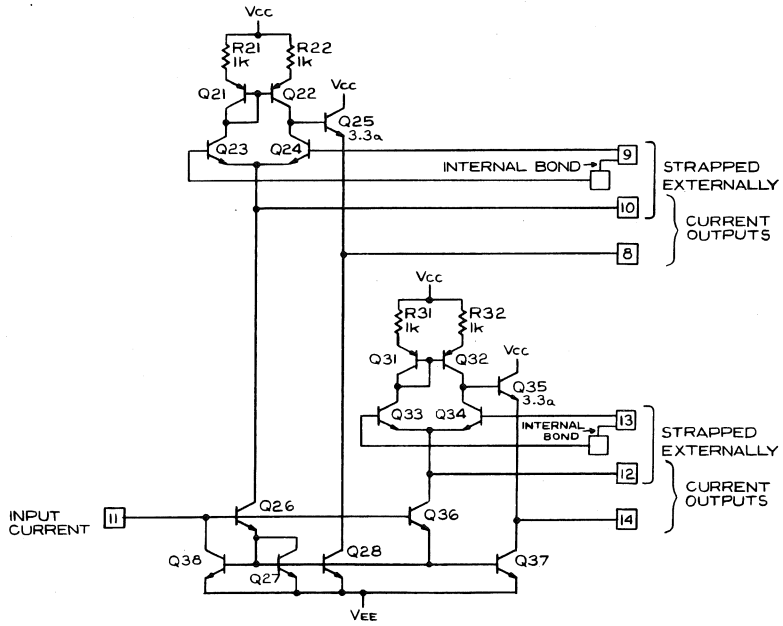
Package: 16 Minipac

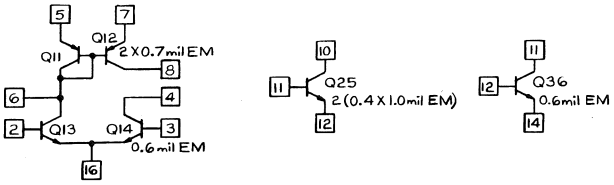
Designer: Dave Allen

ICE Contact: Mike Metcalf

Instrument Usage: 211950C (1)







TEST ROW

ENGR	M. H. Newton	6-10-76	PROCESS	200Ω/□
DWN BY	J. Langley	4-5-76	PACKAGE	16 PIN MINIPAC
CHK BY	Linda Boyer	7-13-76	DIE SIZE	40mil X 40mil
TYPE	MONOLITHIC	2 OP AMPS/ 2 CURRENT SOURCES		M053B
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0057-00		

IN Production
by CER

M105 155-0083-00 DUAL OP AMPS & CHANNEL SWITCH

Description:

A variation of the "Quad-Op-Amp" (M053) with internal "Pin-Out" such that the two of the Op Amps that have separate Outputs share a common Reference current source determining their current operating level while the other two Op Amps share a common Output but are connected so as to have separate Reference current sources so they can be operated on an either-or basis. This Unit was originally designed as a dual Input Amplifier and Channel Switch.

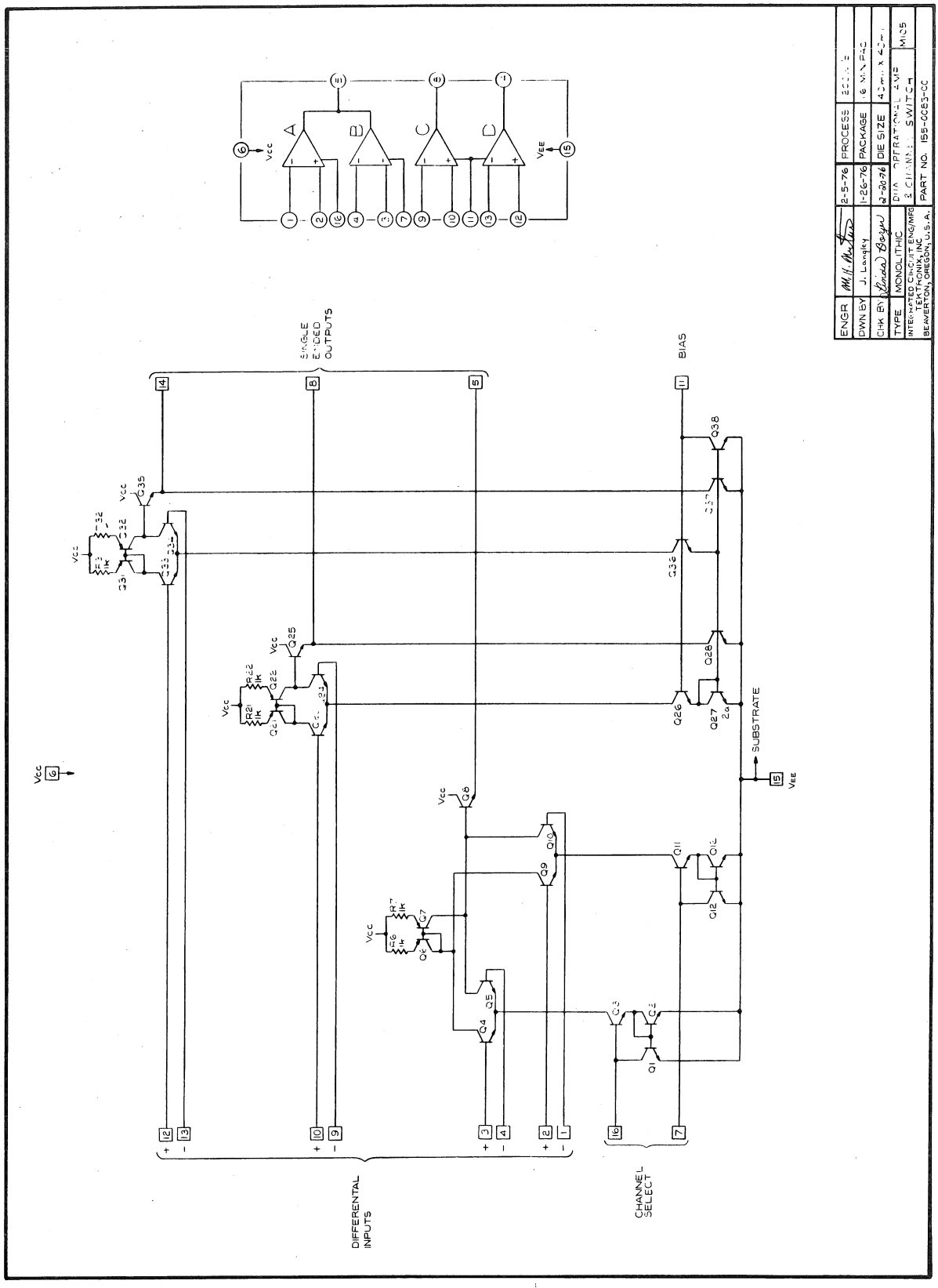
Power Supply: V_{CC} + 5 to + 15
V_{EE} - 5 to - 15

Package: 16 Minipac

Designer: Dave Allen

ICE Contact: Mike Metcalf

Instrument Usage: 212 (1)
214 (1)


ENGR
DWN BY J. Langley
CHK BY
TYPE MONOLITHIC
INTEGRATED CIRCUIT ENG/MFG
TEKTRONIX, INC
BEAVERTON, OREGON, U.S.A.
2-5-76
1-26-76
2-20-76
PROCESS
PACKAGE
DIE SIZE
PART NO. 155-0083-00
SINGLE ENDED OUTPUTS
BIAS
SUBSTRATE
DIFFERENTIAL INPUTS
CHANNEL SELECT
Vcc
VEE

III. MAINFRAME LOGIC

IN Production
by CER

M001 155-0009-00 HORIZONTAL LOCKOUT LOGIC

Description:

The horizontal lockout logic receives inputs from the horizontal chop and alt. binary, A sweep delay control, A sweep gate, B sweep holdoff and B sweep gate. Logic is performed on these signals to provide lockout for A sweep or B sweep and alternating signals for the horizontal chop and alt. binary.

Power Supply: V_{CC} + 5

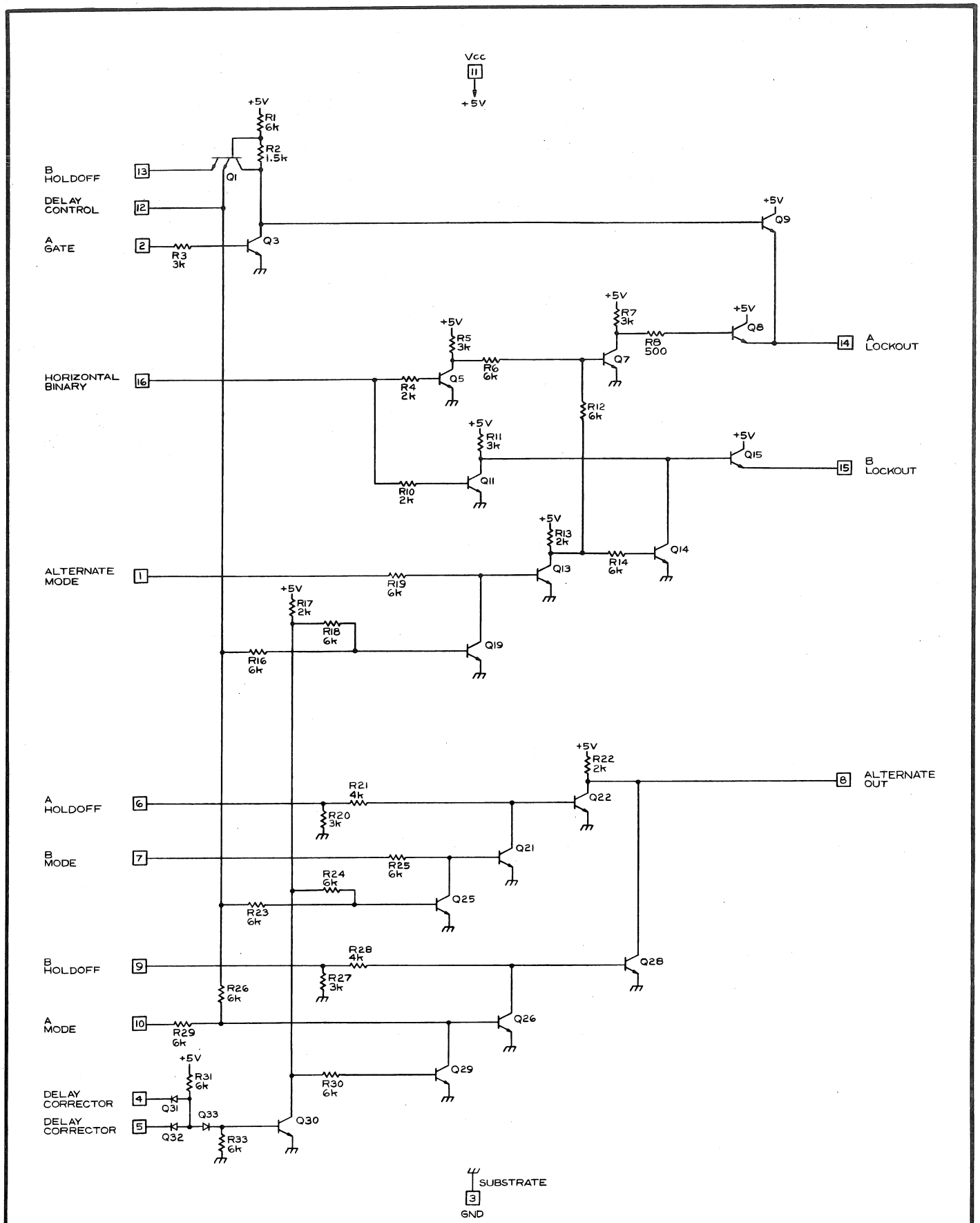
Package: 16 DIP

Designer: Les Larson

ICE Contact: Mike Metcalf

Instrument Usage:

7704A (1)
A7704 (1)
R7704 (1)
7844 (1)
7504 (1)
7514 (1)
7904 (1)



ENGR	M.H. Pettus	8-22-75	PROCESS	200Ω/□
DWN BY	J. Langley	8-19-75	PACKAGE	16 PIN DIP
CHK BY	David Van Cleve	10-23-75	DIE SIZE	45 mil X 45 mil
TYPE	MONOLITHIC	HORIZONTAL LOCKOUT LOGIC		M001
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0009-00		

IN Production
by CER

M004 155-0010-00 CHOP DIVIDER AND BLANKING (TYPE 3)

Description:

The chop divider receives a clock signal from the chop decoder and blanking circuit and counts it down by two for the vertical switch, and by four for the plug-in chop. It also provides a horizontal chop blanking pulse if the horizontal mode switch is CHOP.

Power Supply: V_{CC} + 5

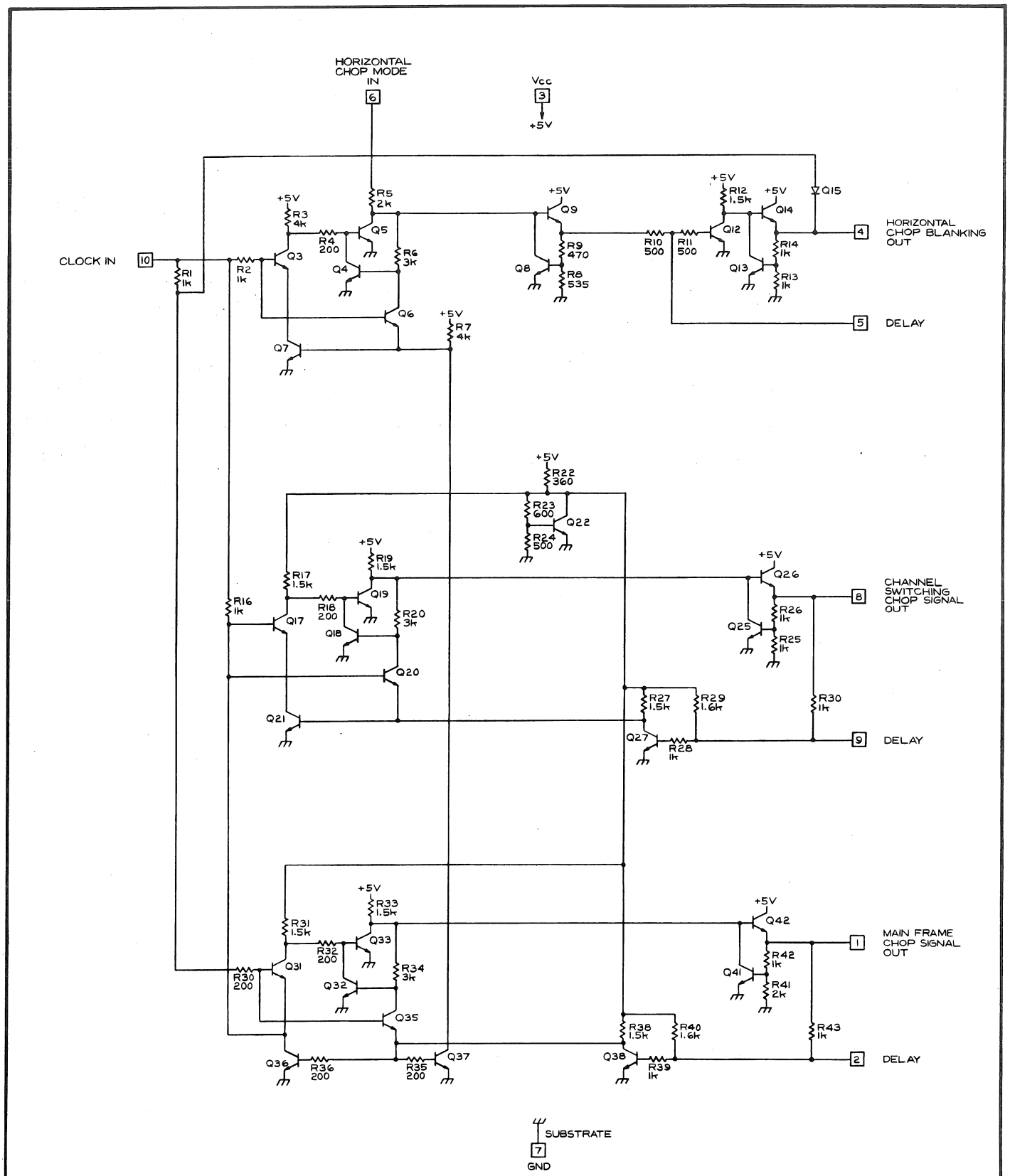
Package: 10 Lead TO-5

Designer: Les Larson

ICE Contact: Mike Metcalf

Instrument Usage:

7704A (1)
A7704 (1)
R7704 (1)
7504 (1)
7514 (1)
7904 (1)



ENGR	M. H. Merton	9-9-75	PROCESS	200Ω/□
DWN BY	J. Langley	9-2-75	PACKAGE	10 LEAD TO-5
CHK BY	David Van Oleck	10-23-75	DIE SIZE	45mil X 40mil
TYPE	MONOLITHIC	CHOP DIVIDER & BLANKING (TYPE 3)		M004
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0010-00		

IN Production
by CER

M012 155-0011-00 CLOCK AND CHOP BLANKING

Description:

This IC generates the 2 MHz chop clock signal for triggering the chop counter (M004) as well as the chop blanking waveform. The blanking waveform can be delayed in time and varied in width over a certain range to accommodate different delay lines. It also has fine logical inputs which are the plug-in and mainframe modes that are used to decide if chop blanking should be used at a certain time.

Power Supply: + 5

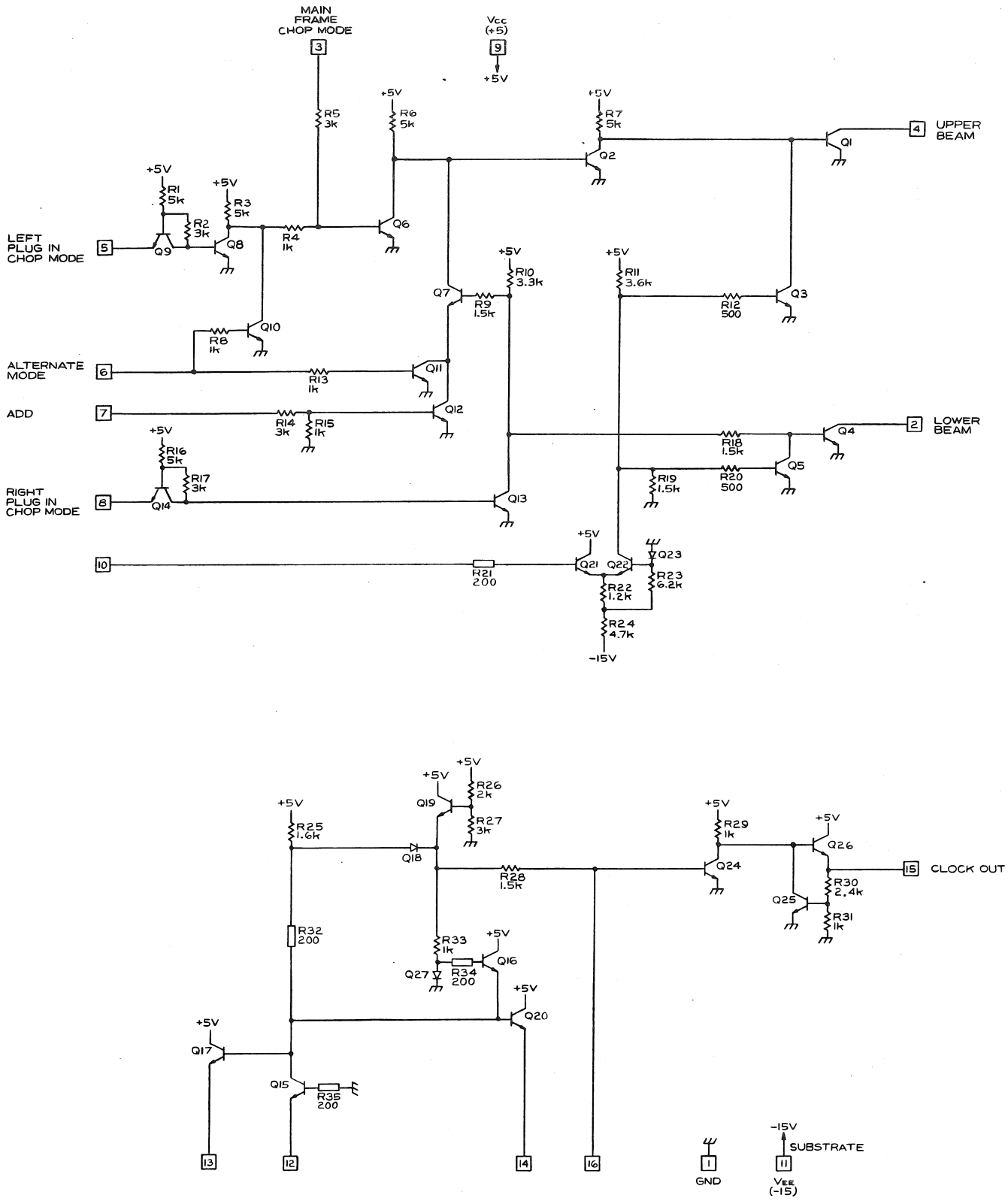
Package: 16 DIP

Designer: Les Larson

ICE Contact: Mike Metalf

Instrument Usage

7704A	(1)	7603	(1)
A7704	(1)	7603G	(1)
R7704	(1)	7603H	(1)
7403	(1)	7603K	(1)
7504	(1)	7613	(1)
7514	(1)	7633	(1)
7904	(1)	485	(1)
7844	(1)	4851	(1)
7313	(1)	4852	(1)
R7603	(1)	7903	(1)
7603N11	(1)	7912	(1)



NOTE:
1. ⊣⊢ INDICATES CROSS UNDER RESISTOR.

ENGR	M. H. [illegible]	9-9-75	PROCESS	200Ω/□
DWN BY	J. Langley	9-8-75	PACKAGE	16 PIN DIP
CHK BY	David Van Ela	10-23-75	DIE SIZE	40mil X 50mil
TYPE	MONOLITHIC	CLOCK & CHOP BLANKING		M012
INTERGATED CIRCUITS ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0011-00		

IN Production
by CER

M015 155-0012-00 Z AXIS LOGIC

Description:

This IC is a signal conditioner for the main Z axis amplifier. It is under control of the horizontal switch drive, A gate, B gate, delay control, A intensity control and B intensity control. With these signals, it properly selects, at one output, either A intensity, B intensity or A intensified by B for delaying modes.

Additional functions are chop blanking for vertical and horizontal, external and plug-in Z axis input, and fast limiting of the composite signal. The signals are further limited at slow sweep speeds to prevent burning of the CRT.

Power Supply: V_{CC} + 5

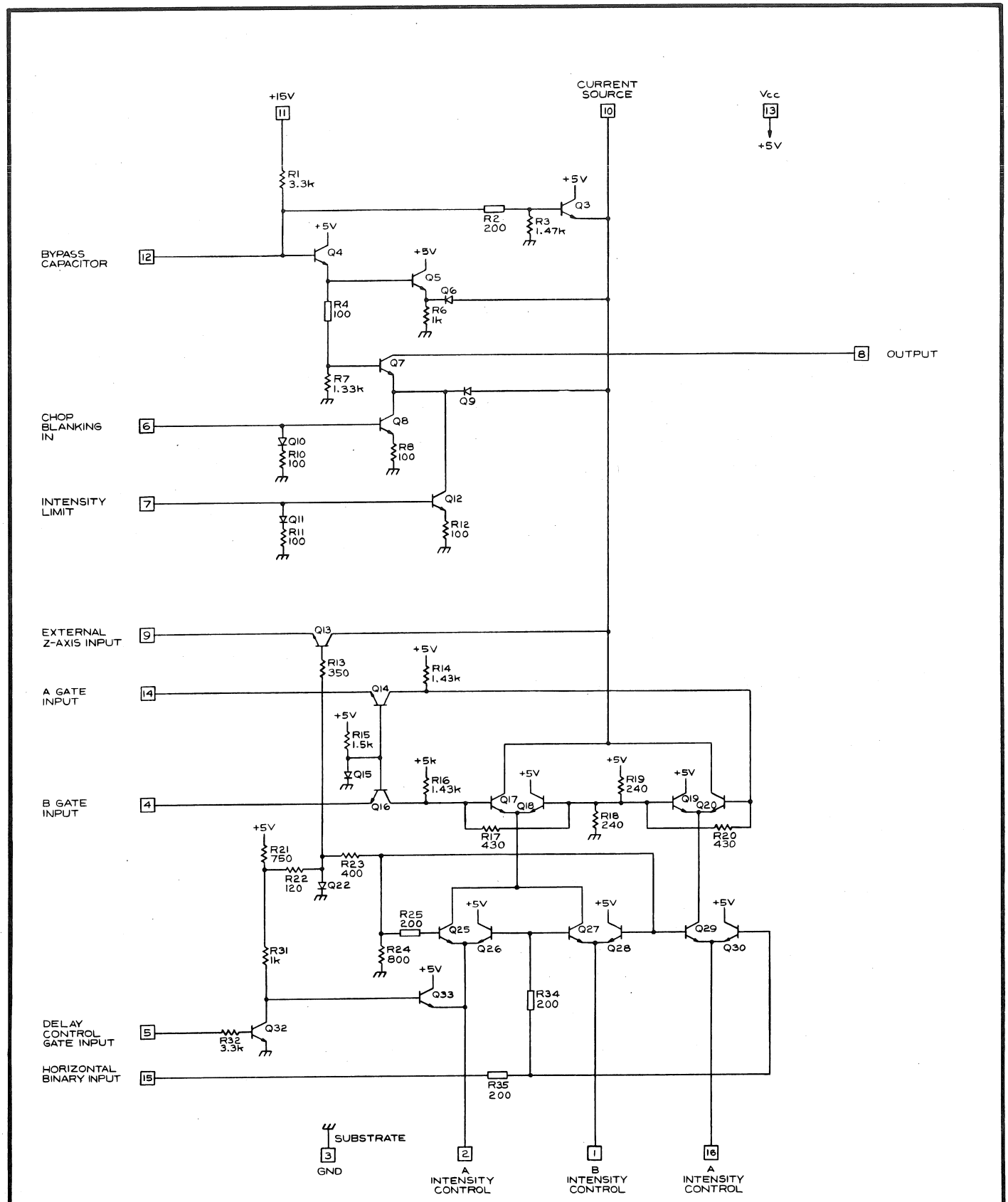
Package: 16 DIP

Designer: Les Larson

ICE Contact: George Wilson

Instrument Usage:

485	(2)	7504	(1)
4851	(2)	7514	(1)
4852	(2)	7844	(2)
7704	(1)	7903	(1)
A7704	(1)	7904	(1)
R7704	(1)	7912	(1)
7704A	(1)		



NOTE:
1. —▭— INDICATES CROSS UNDER RESISTOR.

ENGR	G.L.	9-26-75	PROCESS	200 Ω/□
DWN BY	J. Langley	9-11-75	PACKAGE	16 PIN DIP
CHK BY	David Van Cleve	10-23-75	DIE SIZE	45mil X 50mil
TYPE	MONOLITHIC		Z-AXIS LOGIC	M015
INTERGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.			PART NO. 155-0012-00	

IN Production
by CER

M022	155-0013-00 155-0013-01	HORIZONTAL CHOP & ALT. BINARY (TYPE 2)

Description:

This circuit receives horizontal mode switch information, alternating signals, and chopping signals (.5 MHz), and produces an output to the horizontal switch as to which sweep should be received. This same output is used in the horizontal lockout logic and in both vertical alt. binaries.

Power Supply: V_{CC} + 5

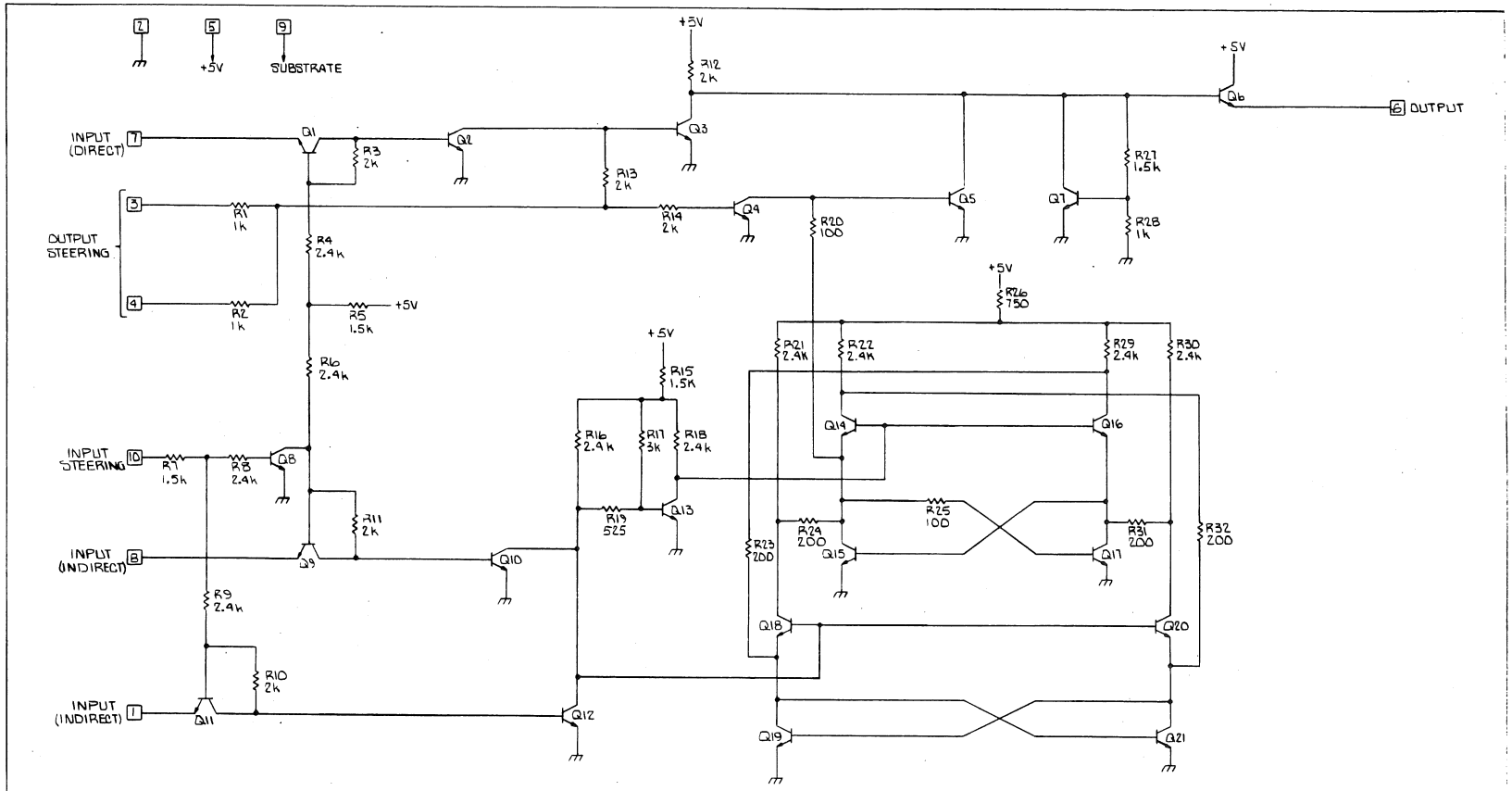
Package: 10 lead TO-5

Desginer: Les Larson

ICE Contact: George Wilson

Instrument Usage:

7704A	(2)
A7704	(2)
R7704	(2)
7504	(2)
7514	(2)
7904	(2)



ENGR	M. H. Whitten	11-11-74	PROCESS	200Ω/□
DWN BY	Ron Greene	11-9-74	PACKAGE	10 PIN TO-5
CHK BY	Jim McNally	11-25-74	DIE SIZE	45 mil × 50 mil
TYPE	MONOLITHIC	HORIZONTAL CHOP & ALT. BINARY		M022
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0013-00		

IV. KNOB READOUT SYSTEM

IN Production
by CER

M019D 155-0014-01 ANALOG TO DECIMAL CONVERTER

Description:

The M019 converts differential analog input voltage to one of ten output indications, with a transition spacing of 500 mV ± 2% and a transition zone of less than 5 mV. The outputs may be wired as current steering, in which case one of the circuit terminals accepts the current input, or in the form of saturated transistors. Ratings of the output circuits are presently 15V and 25 mA.

Power Supply: V_{CC} + 15

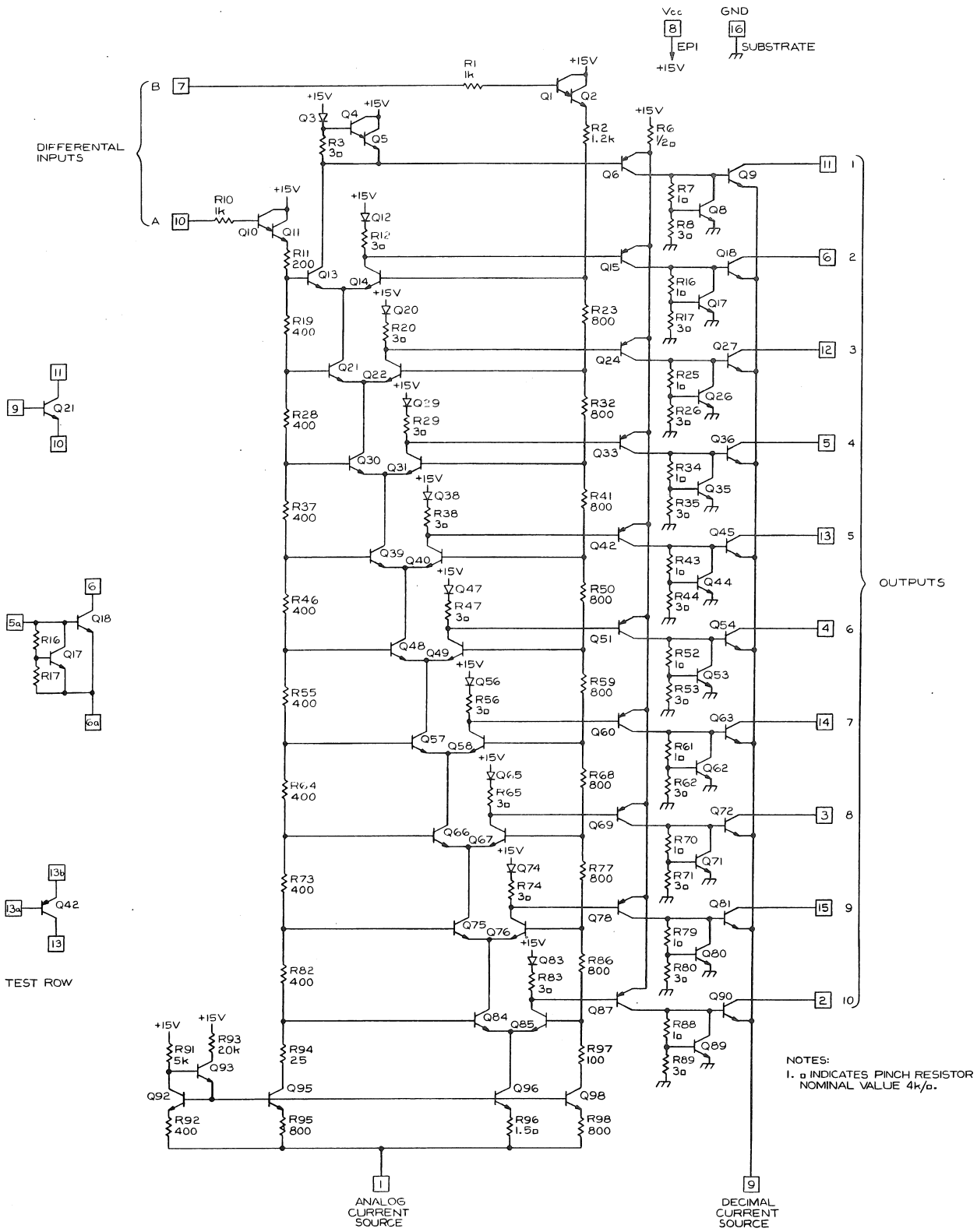
Package: 16 DIP

Designer: Barrie Gilbert

ICE Contact: Mike Metcalf

Instrument Usage:

7704A	(2)	7514	(2)
A7704	(2)	7904	(2)
R7704	(2)	7313	(2)
P7001950C	(2)	7613	(2)
P7001953Q	(2)	7633	(2)
5403	(2)	7603	(2)
5441	(2)	7603G	(2)
5443	(2)	7603H	(2)
7844	(2)	7603K	(2)
7903	(2)	7J20	(2)
7912	(2)	5440	(2)
7504	(2)	P7001	(2)



NOTES:
1. o INDICATES PINCH RESISTOR NOMINAL VALUE 4k/o.

ENGR	M.H. McKinnon	3-4-76	PROCESS	200Ω/o
DWN BY	J. Langley	2-12-76	PACKAGE	16 PIN DIP
CHK BY	Linda Boyer	3-10-76	DIE SIZE	50mil X 55mil
TYPE	MONOLITHIC	ANALOG TO DECIMAL CONVERTER		M019D
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0014-01		

IN Production
by CER

M020F 155-0015-01 DATA SWITCH

Description:

A current-steering switching circuit designed specifically for the know-readout system.

Accepts nine inputs at currents in the range 0 - 1 mA and selects one under the control of a BCD code. The output is from an NPN collector. The inputs are virtual grounds within ± 100 mV of ground potential for input range of ± 1 mA.

Power Supply: V_{CC} + 5V

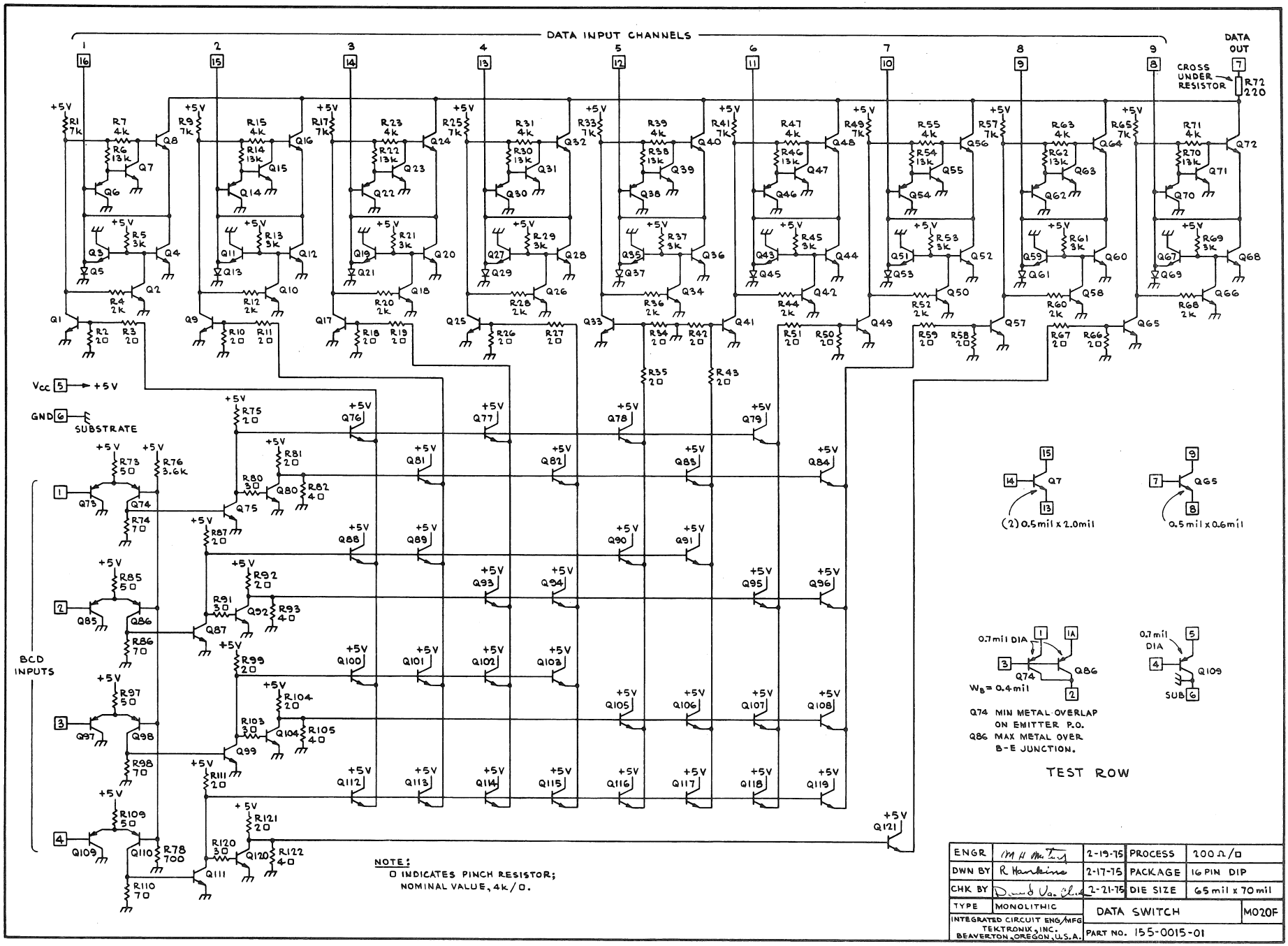
Package: 16 DIP

Designer: Barrie Gilbert

ICE Contact: Mike Metcalf

Instrument Usage:

7704A	(2)	7904	(2)
A7704	(2)	7504	(2)
R7704	(2)	7514	(2)
5403	(2)	7313	(2)
5440	(2)	7613	(2)
5441	(2)	7633	(2)
5443	(2)	7603	(2)
7844	(2)	7603G	(2)
7912	(2)	7603H	(2)
7903	(2)	7603K	(2)
P7001	(2)		



ENGR	M H Mutty	2-19-75	PROCESS	200 Ω/□
DWN BY	R Hawkins	2-17-75	PACKAGE	16 PIN DIP
CHK BY	David Van Glad	2-21-75	DIE SIZE	65 mil x 70 mil
TYPE	MONOLITHIC	DATA SWITCH		M020F
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0015-01		

IN Production
by CER

M025 155-0017-00 DECADE COUNTER

Description:

General.

The M025 is a decade counter having power-handling output capabilities, and all ten outputs brought out to pins. It features an auxiliary count output pin, a reset input and versatile operating modes. Count input rates up to 5 MHz are acceptable.

Power Supply: V_{CC} + 5 V

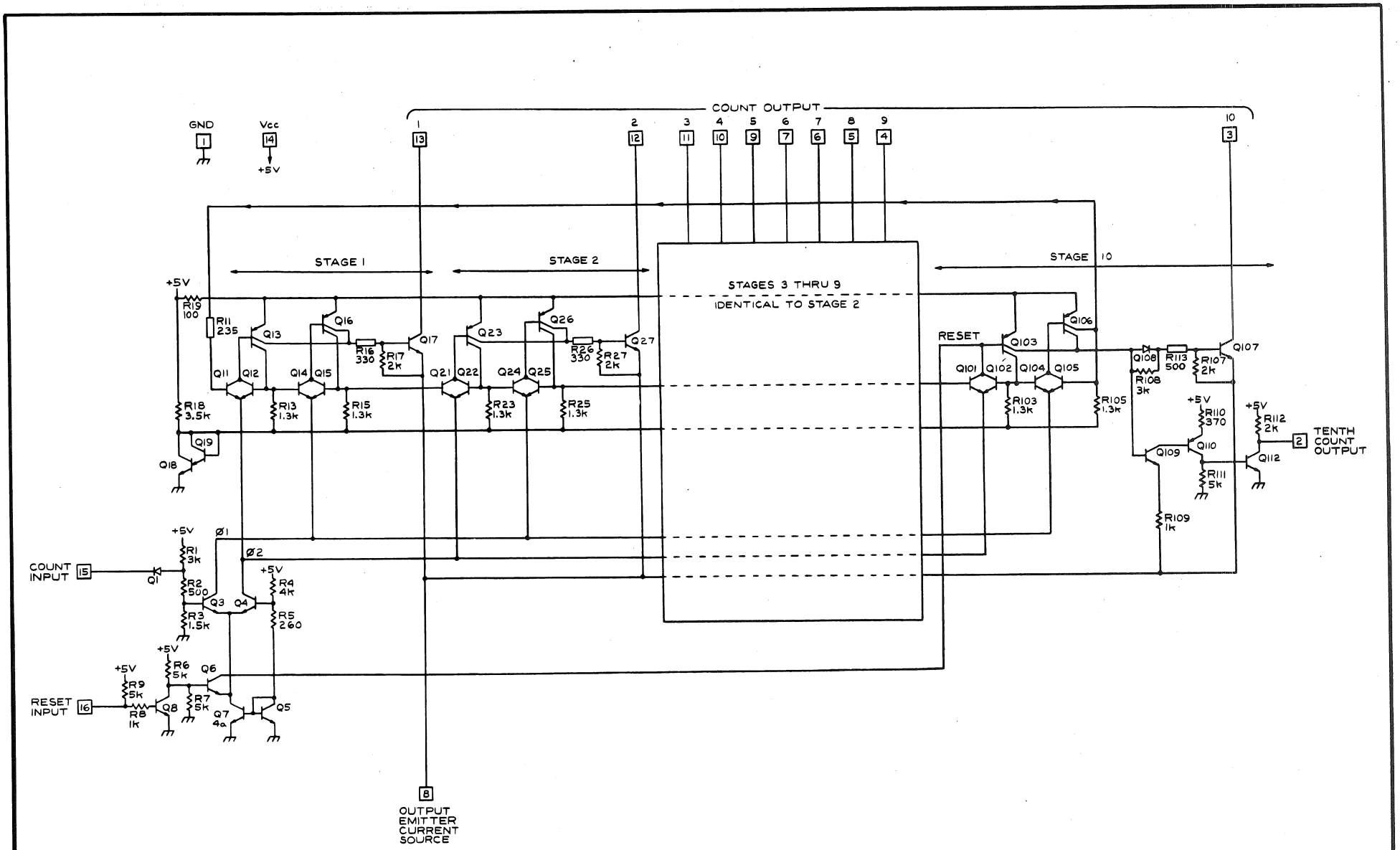
Package: 16 DIP

Designer: Barrie Gilbert

ICE Contact: Mike Metcalf

Instrument Usage:

7704A	(1)	7514	(1)
A7704	(1)	7904	(1)
R7704	(1)	7903	(1)
5403	(1)	7313	(1)
5440	(1)	7613	(1)
5441	(1)	7633	(1)
5443	(1)	7603	(1)
7844	(1)	7603G	(1)
7912	(1)	7603H	(1)
7504	(1)	7603K	(1)
P7001	(2)		



ENGR	M. H. Pettus	3-19-75	PROCESS	200 n/o
DWN BY	J. Langley	3-17-75	PACKAGE	16 PIN DIP
CHK BY	David Van Cleve	10-23-75	DIE SIZE	60 X 65 mil
TYPE	MONOLITHIC	DECADE COUNTER		M025D
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0017-00		

IN Production
by CER

M026 155-0018-00 ZERO LOGIC

Description:

General.

The M026 is a special-purpose circuit for use in the new-generation knob-readout system. It comprises an input logic section, four memory cells, an output logic section and a binary-to-ternary conversion stage.

Power Supply: V_{CC} + 5 V

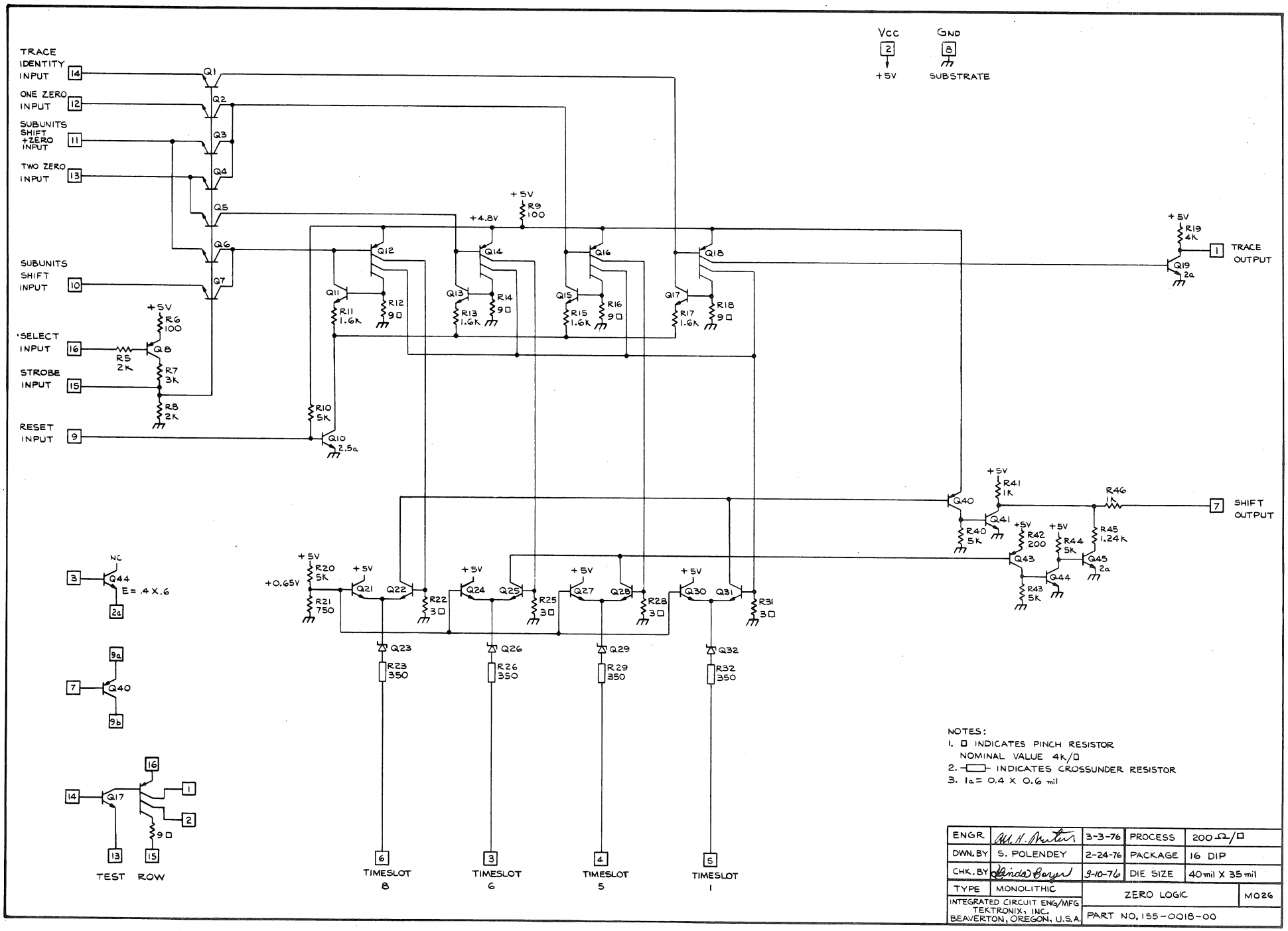
Package: 16 DIP

Designer: Les Larson

ICE Contact: Mike Metcalf

Instrument Usage:

7704A	(1)	7514	(1)
A7704	(1)	7904	(1)
R7704	(1)	7903	(1)
5403	(1)	7313	(1)
5440	(1)	7613	(1)
5441	(1)	7633	(1)
5443	(1)	7603	(1)
7844	(1)	7603G	(1)
7912	(1)	7603H	(1)
7504	(1)	7603K	(1)
P7001	(2)		


TRACE IDENTITY INPUT
ONE ZERO INPUT
SUBUNITS SHIFT +ZERO INPUT
TWO ZERO INPUT
SUBUNITS SHIFT INPUT
SELECT INPUT
STROBE INPUT
RESET INPUT
Vcc
GND
+5V
SUBSTRATE
TRACE OUTPUT
SHIFT OUTPUT
+4.8V
+0.65V
NC
E = .4 X .6
TEST
ROW
TIMESLOT 8
TIMESLOT 6
TIMESLOT 5
TIMESLOT 1
NOTES:
1. □ INDICATES PINCH RESISTOR NOMINAL VALUE 4k/□
2. INDICATES CROSSUNDER RESISTOR
3. 1a = 0.4 X 0.6 mil
ENGR 3-3-76 PROCESS 200Ω/□
DWN. BY S. POLENDEY 2-24-76 PACKAGE 16 DIP
CHK. BY 9-10-76 DIE SIZE 40 mil X 35 mil
TYPE MONOLITHIC
ZERO LOGIC
M026
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.
PART NO. 155-0018-00

IN Production
by CER

M027 155-0019-00 DECIMAL POINT & SPACING

Description:

The M027 is used to produce a positioning signal (10 level staircase) for the new generation readout system, and also to position the decimal point. Consists of a decade counter, digital-to-analog converter, input logic.

Power Supply: V_{CC} + 5V

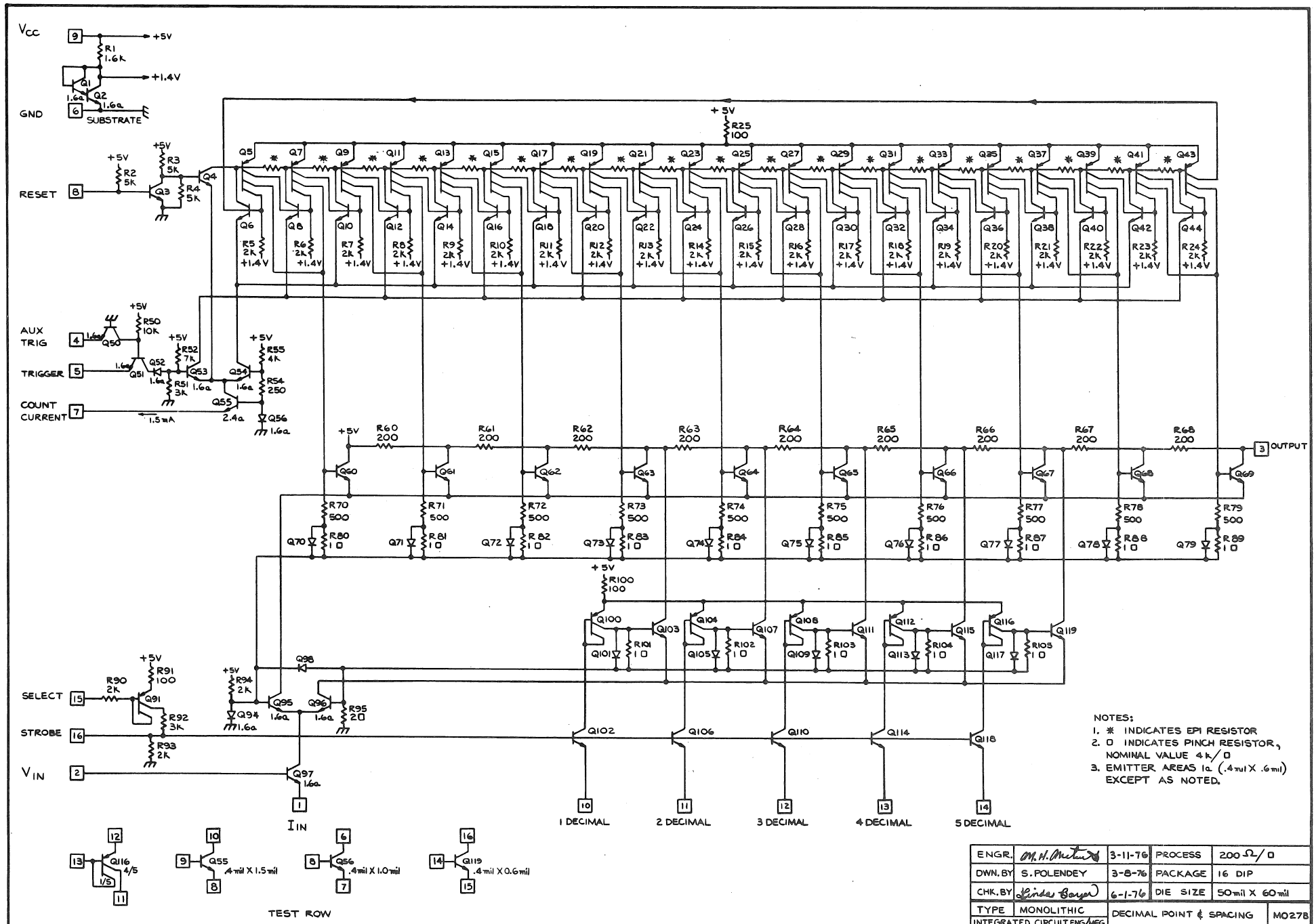
Package: 16 DIP

Designer: Les Larson

ICE Contact: Mike Metcalf

Instrument Usage:

7704A	(1)	7904	(1)
A7704	(1)	7903	(1)
R7704	(1)	7313	(1)
5403	(1)	7613	(1)
5441	(1)	7633	(1)
5443	(1)	7603	(1)
7844	(1)	7603G	(1)
7912	(1)	7603H	(1)
7504	(1)	7603K	(1)
7514	(1)	5440	(1)
P7001	(2)		


VCC
GND
SUBSTRATE
RESET
AUX TRIG
TRIGGER
COUNT CURRENT
SELECT
STROBE
VIN
IIN
OUTPUT
1 DECIMAL
2 DECIMAL
3 DECIMAL
4 DECIMAL
5 DECIMAL
TEST ROW
.4 mil X 1.5 mil
.4 mil X 1.0 mil
.4 mil X 0.6 mil
NOTES:
1. * INDICATES EPI RESISTOR
2. O INDICATES PINCH RESISTOR, NOMINAL VALUE 4k/□
3. EMITTER AREAS 1a (.4 mil X .6 mil) EXCEPT AS NOTED.
ENGR. M.H. Mitchell 3-11-76 PROCESS 200 Ω/□
DWN. BY S. POLENDEY 3-8-76 PACKAGE 16 DIP
CHK. BY Linda Bayer 6-1-76 DIE SIZE 50 mil X 60 mil
TYPE MONOLITHIC
DECIMAL POINT & SPACING
M027B
INTEGRATED CIRCUIT ENG/MFG
TEKTRONIX, INC.
BEAVERTON, OREGON, U.S.A.
PART NO. 155-0019-00

IN Production
by CER

M028 155-0020-00 OUTPUT ASSEMBLER

Description:

Produces a display format signal (X- and Y- waveforms) from binary and analog input signals. Part of new generation readout system.

Power Supply: V_{CC} + 5 and + 15 V

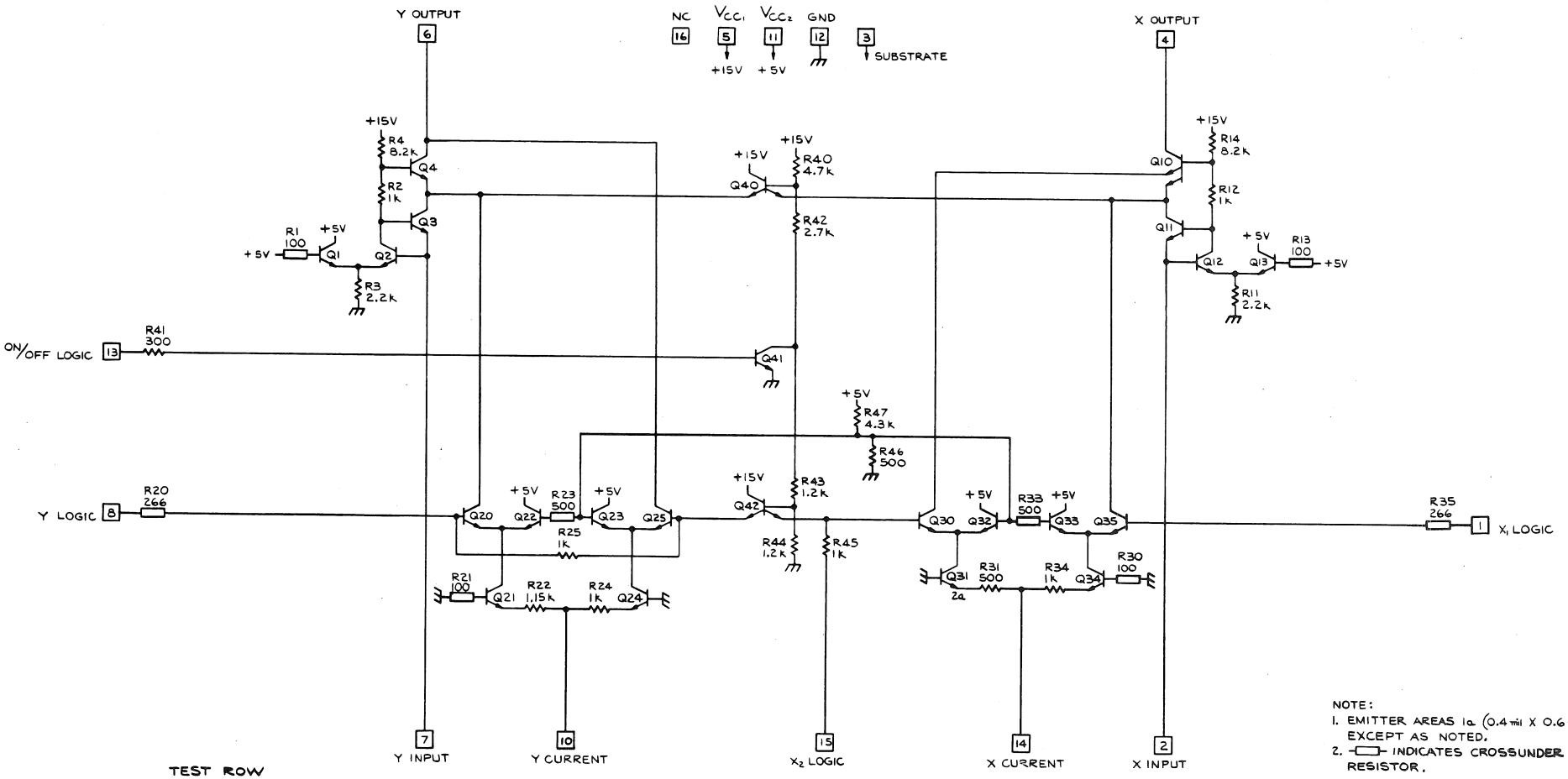
Package: 16 DIP

Designer: Les Larson

ICE Contact: Mike Metcalf

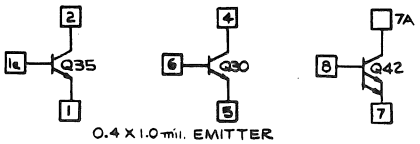
Instrument Usage:

7704A	(1)	7904	(1)
A7704	(1)	7903	(1)
R7704	(1)	7313	(1)
5403	(1)	7613	(1)
5441	(1)	7633	(1)
5443	(1)	7603	(1)
7844	(1)	7603G	(1)
7912	(1)	7603H	(1)
7504	(1)	7603K	(1)
7514	(1)	5440	(1)
P7001	(2)		



NOTE:
1. EMITTER AREAS 1a (0.4 mil X 0.6 mil) EXCEPT AS NOTED.
2. —▭— INDICATES CROSSUNDER RESISTOR.

TEST ROW



ENGR	M.H. Nelson	6-10-76	PROCESS	200 Ω/□
DWN BY	S. POLENDEY	2-17-76	PACKAGE	16 PIN DIP
CHK BY	Linda Bayer	7-12-76	DIE SIZE	40 mil X 45 mil
TYPE	MONOLITHIC INTEGRATED CIRCUIT	OUTPUT ASSEMBLER		M028A
ENG/MFG	TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.	PART NO. 155-0020-00		

IN Production
by CER

M029C 155-0021-01 TIMING GENERATOR

Description:

Generates a timing clock, a shaped negative pulse for the M025, a scanning ramp for the M024, and X-Y on-off and intensity controls for the Z axis.

Power Supply: V_{CC} + 5V
V_{EE} - 15 V

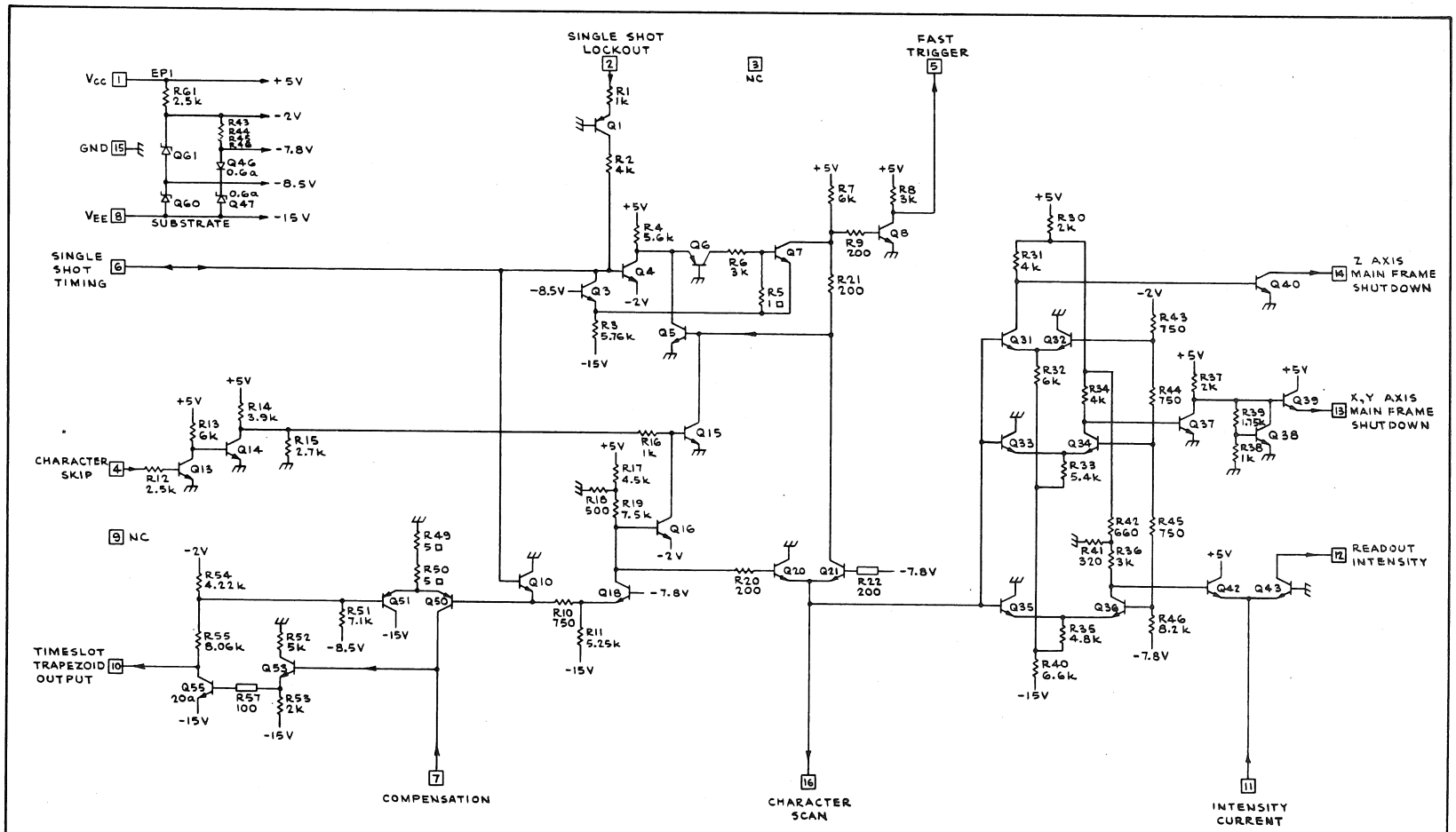
Package: 16 DIP

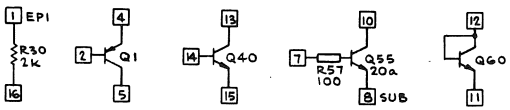
Designer: Les Larson

ICE Contact: Mike Metcalf

Instrument Usage:

7704A	(1)	7904	(1)
A7704	(1)	7903	(1)
R7704	(1)	7313	(1)
5403	(1)	7613	(1)
5441	(1)	7633	(1)
5443	(1)	7603	(1)
7844	(1)	7603G	(1)
7912	(1)	7603H	(1)
7504	(1)	7603K	(1)
7514	(1)	5440	(1)
P7001	(2)		





TEST ROW

NOTES:

1. □ INDCATES PINCH RESISTOR, NOMINAL VALUE 4k/□.
2. -▭- INDICATES CROSSUNDER RESISTOR.
3. 1a = 13 X 25 μ.

ENGR	M. H. Mertens	6-20-77	PROCESS	200 Ω/□
DWN BY	Ron Hamkins	6-17-77	PACKAGE	16 PIN DIP
CHK BY	David VonCleve	6-20-77	DIE SIZE	48 x 57 mils
TYPE	MONOLITHIC		TIMING GENERATOR	M029C
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.			PART NO. 155-0021-00	

REVISIONS

ENGINEERING	DATE	DRAWN BY	DATE	PRODUCTION	DATE
M. Mertens	6-20-77	R. Hamkins	6-17-77	David VonCleve	6-20-77

IN Production

M112AA 155-0117-00 KNOB READOUT COUNTER

Description:

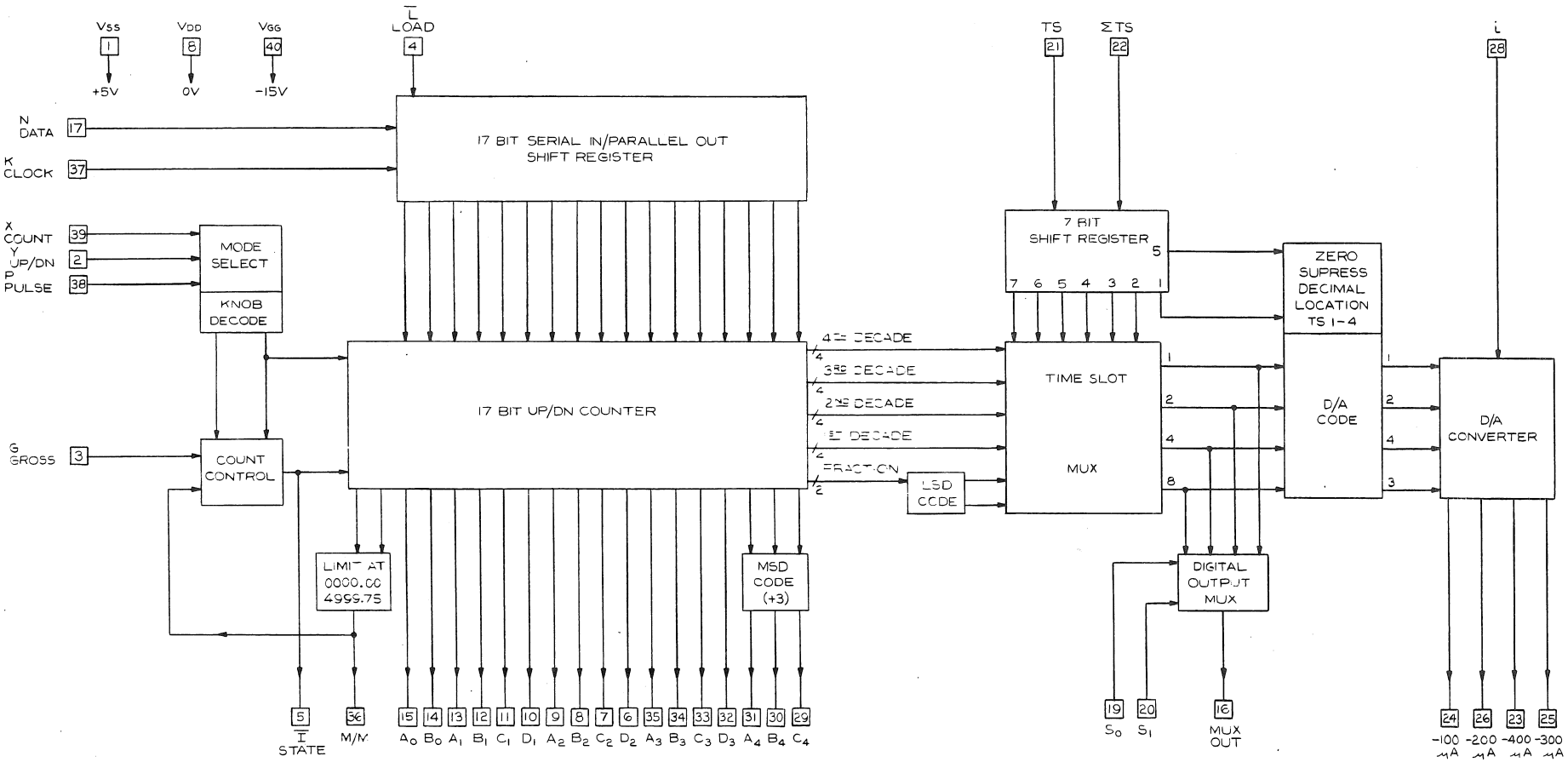
The M112 is a 17 bit up/down counter used for knob readout of the frequency control in the 7L5 spectrum analyzer. Up down counting can be performed using either an overlapping two-phase clock input whose phase overlap controls count direction or a single-phase clock input and an up/down control line. The counter can be preset to a known state using a serial input shift register which loads the counter. Both BCD (parallel) outputs and a multiplexed analog current output compatible with 7000 Series displays are provided. The counter counts from 0 to 4999.75 by 0.25 increments. In the gross count mode the counter increments by 10 until it is within 10 counts of the end limits. It then reverts to the fine count mode.

Power Supply: $V_{DD} = -15$
$V_{SS} = +5$

Package: 40 PIN DIP; leadless

Designer: Bob Nordstrom

ICE Contact: Warren Finke



ENGR		1-21-76	PROCESS	P MOS
DWN BY	J. Langley	1-20-76	PACKAGE	40 PIN DIP; LEADLESS
CHK BY	Linda Bazer	2-25-76	DIE SIZE	147mil X 160mil
TYPE	MONOLITHIC	KNOB READOUT COUNTER BLOCK DIAGRAM		M112AA
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0117-00		

IN Production

M119 155-0110-00 LEGEND GENERATOR

Description:

This is identical to the M92 with a different metal mask to change the time slot coding. See Truth Table.

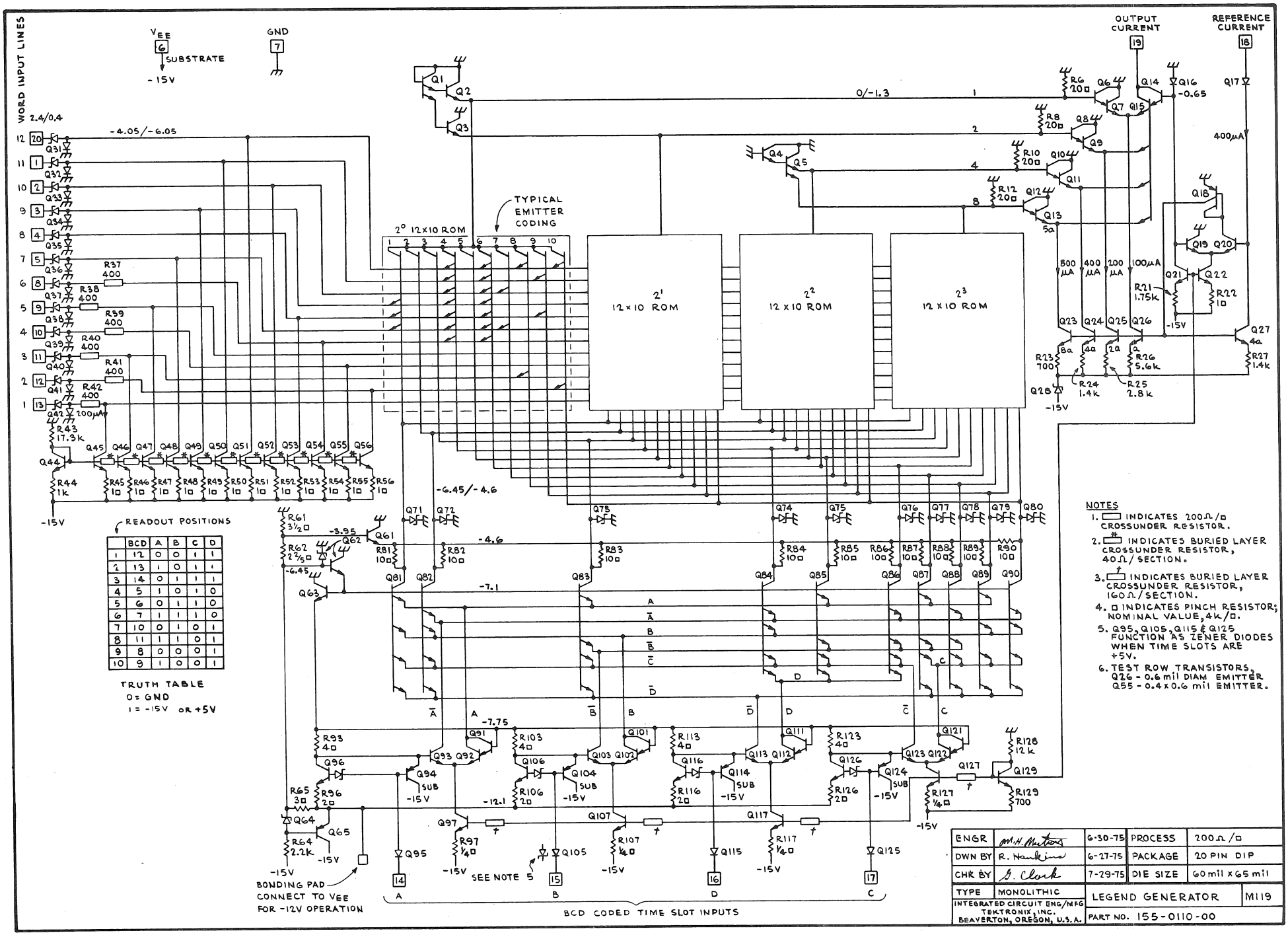
Power Supply: V_{CC} 0 V
V_{EE} -15 V.

Package: 20 DIP

Designers: Roger McCoy/Mike Metcalf

ICE Contact: Mike Metcalf

Instrument Usage: 7L5 (R_1)


WORD INPUT LINES
VEE
SUBSTRATE
-15V
GND
OUTPUT CURRENT
REFERENCE CURRENT
TYPICAL EMITTER CODING
2° 12x10 ROM
2¹ 12 x 10 ROM
2² 12 x 10 ROM
2³ 12 x 10 ROM
READOUT POSITIONS
TRUTH TABLE
0 = GND
1 = -15V OR +5V
BONDING PAD CONNECT TO VEE FOR -12V OPERATION
SEE NOTE 5
BCD CODED TIME SLOT INPUTS
NOTES
1. INDICATES 200Ω/□ CROSSUNDER RESISTOR.
2. INDICATES BURIED LAYER CROSSUNDER RESISTOR, 40Ω/SECTION.
3. INDICATES BURIED LAYER CROSSUNDER RESISTOR, 160Ω/SECTION.
4. □ INDICATES PINCH RESISTOR; NOMINAL VALUE, 4k/□.
5. Q95, Q105, Q115 & Q125 FUNCTION AS ZENER DIODES WHEN TIME SLOTS ARE +5V.
6. TEST ROW TRANSISTORS, Q26 - 0.6 mil DIAM EMITTER Q55 - 0.4 x 0.6 mil EMITTER.
ENGR
DWN BY R. Hankins 6-27-75
CHK BY 7-29-75
TYPE MONOLITHIC
PROCESS 200Ω/□
PACKAGE 20 PIN DIP
DIE SIZE 60 mil x 65 mil
LEGEND GENERATOR M119
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.
PART NO. 155-0110-00

ROM PROGRAMMING

TIME SLOT

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1														2		
2										1						
3												1				
4												4				
5										4						
6						1	4	5	2	2	2	2	2		6	
7						1	4	5		2	1	2	1		6	
8						1	4	5	1	2		2	1		6	
9						1	4	5	2	2	2	2	1			
10						1	4	5		2	1	2				
11						1	4	5	1	2		2				
12						1	4	5		1		1				

155-0110-00

M119

NOTE: The number in the square is in terms of tenths of mA of output current.

Crossed out area is not used.

IN Production

By CER

M150A 155-0171-00 4-DECADE COUNTER AND MEMORY

Description:

The circuit is comprised of four cascaded decade counters, each with a buffer memory, each of which can drive the decimal to analog converter. Thus it can count up to 9999, store the count at anytime and convert it to an output form suitable for interfacing with the New-Generation Knob-Readout system. Output pulses are also provided at the output of the 2nd, 3rd, and 4th decades. A zero-not output is provided for leading zero's blanking.

Power Supply: V_{CC} + 5 V.

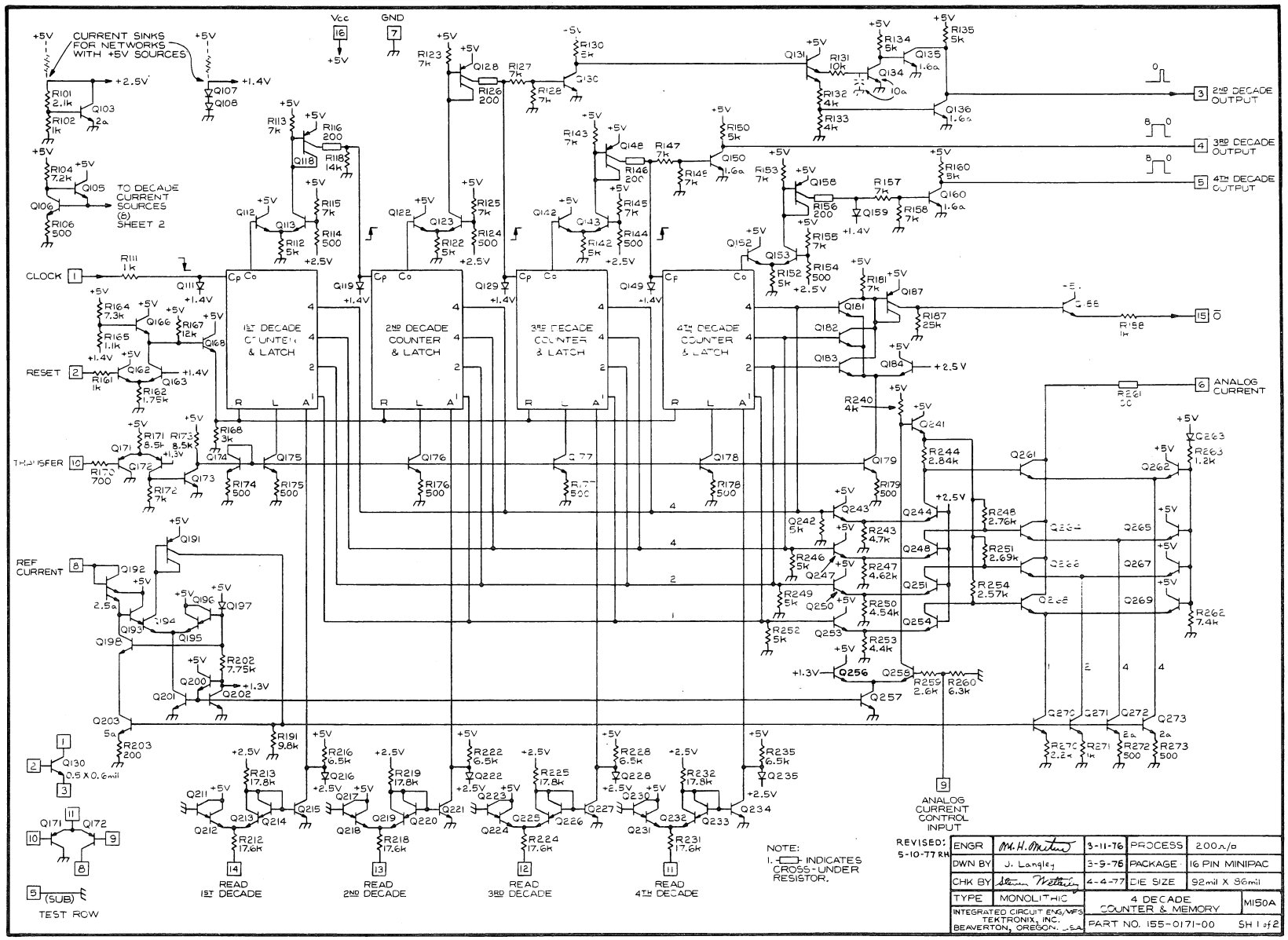
Package: 16 Minipac

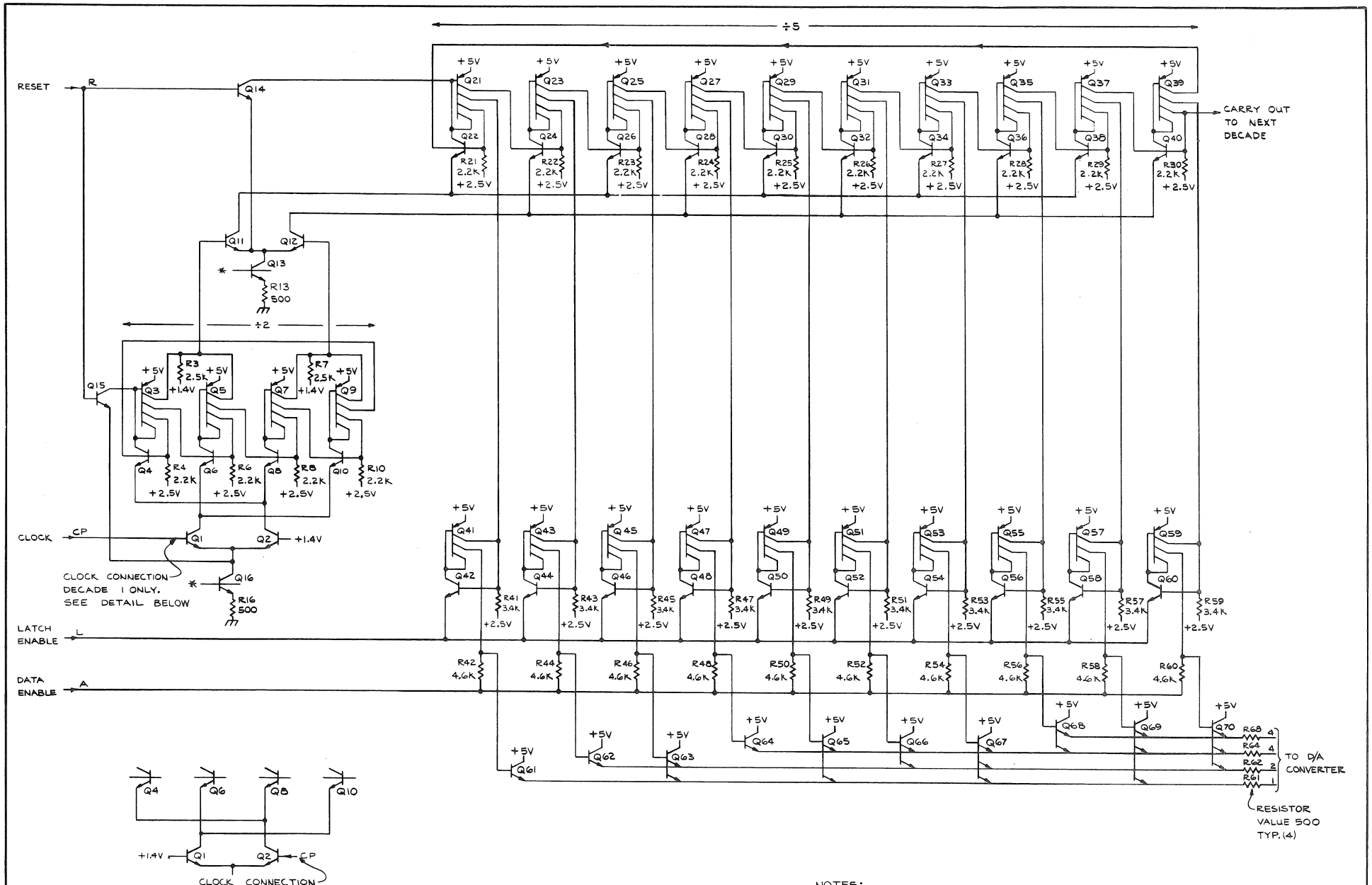
Designer: Mike Metcalf

ICE Contact: Mike Metcalf

Instrument Usage:

7J20 (1)
7D12 (1)
7D15 (2)
7B85 (1)
7D01 (1)


CURRENT SINKS FOR NETWORKS WITH +5V SOURCES
TO DECADE CURRENT SOURCES (B) SHEET 2
Vcc
GND
CLOCK
RESET
TRANSFER
REF CURRENT
1ST DECADE COUNTER & LATCH
2ND DECADE COUNTER & LATCH
3RD DECADE COUNTER & LATCH
4TH DECADE COUNTER & LATCH
2ND DECADE OUTPUT
3RD DECADE OUTPUT
4TH DECADE OUTPUT
ANALOG CURRENT
ANALOG CURRENT CONTROL INPUT
READ 1ST DECADE
READ 2ND DECADE
READ 3RD DECADE
READ 4TH DECADE
TEST ROW
NOTE: 1. INDICATES CROSS-UNDER RESISTOR.
REVISED: 5-10-77 RH
ENGR M. H. Mattes 3-11-76 PROCESS 200A/a
DWN BY J. Langley 3-9-76 PACKAGE 16 PIN MINIPAC
CHK BY 4-4-77 DIE SIZE 92mil X 86mil
TYPE MONOLITHIC 4 DECADE COUNTER & MEMORY M150A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.
PART NO. 155-0171-00 SH 1 of 2



NOTES:
1. * FOR CURRENT SOURCE CONTROL SEE SHEET 1.

ENGR	M. H. Metten	3-11-76	PROCESS	200 Ω/□
DWN BY	S. POLENDEY	2-12-76	PACKAGE	16 PIN MINIPAC
CHK BY	Steve Metterly	4-4-77	DIE SIZE	92 mil X 86 mil
TYPE	MONOLITHIC	4 DECADE COUNTER AND MEMORY		M150A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON - OREGON, USA		PART NO. 155-0171-00		SH 2 OF 2

IN Production
by CER

M160	155-0023-00	CHARACTER GENERATOR
M161	155-0024-00	
M162	155-0025-00	
M163	155-0026-00	
M164	155-0027-00	

Description:

To generate the X- and Y- waveforms corresponding to ten different alphanumeric symbols, under control of an external scanning voltage. There are four different sets of symbols, designated by the suffixes -N (numbers), -L (letters), -S (symbols) and-P (prefixes).

Power Supply: V_{CC} + 5V
V_{EE} - 15V

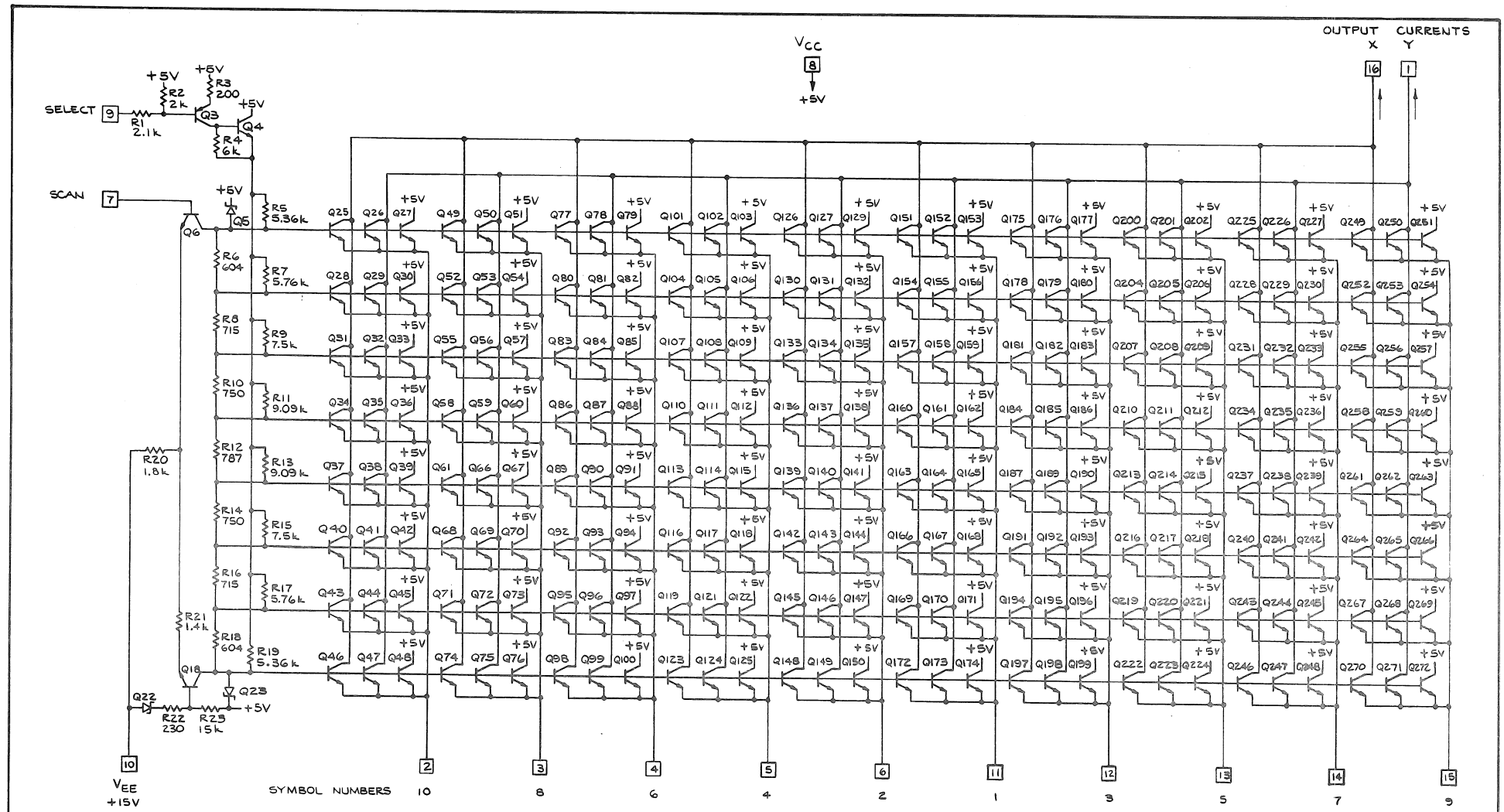
Package: 16 DIP

Designer: Barrie Gilbert

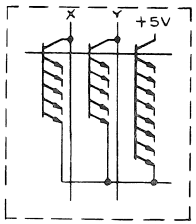
ICE Contact: Mike Metcalf

Instrument Usage:

5403	(1)	7603K	(1)
5440	(1)	7514	(1)
5441	(1)	7704A	(1)
5443	(1)	A7704	(1)
7313	(1)	R7704	(1)
7613	(1)	7844	(1)
7633	(1)	7903	(1)
7603	(1)	7904	(1)
7603G	(1)	7912	(1)
7603H	(1)	7504	(1)
P7001	(2)		



Q25 THRU Q272



TYPICAL EMITTER CONFIGURATION (80)

SEE TABLE FOR NUMBER OF CONNECTED EMITTERS

155-0023-00 M160
155-0024-00 M161
155-0025-00 M162
155-0026-00 M163
155-0027-00 M164

ENGR	M. H. Smeltzer	6-18-76	PROCESS	200Ω/□
DWN BY	S. POLENDEY	6-9-76	PACKAGE	16 PIN DIP
CHK BY	Linda Boyer	7-8-76	DIE SIZE	71 mil x 75 mil
TYPE	MONOLITIC	CHARACTER GENERATOR		M16X
INTEGATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-002X-00		

IN Production

M165	155-0086-00	LEGEND GENERATOR
M166	155-0087-00	
M167	155-0088-00	
M169	155-0104-00	
M170	155-0105-00	
M171	155-0135-00	

Description:

12 x 10 x 4 read only memory coupled to a 4-bit D to A converter with internal precision current sources requiring a single precision external reference. This output is directly compatible with KRO row and column data lines. The ten "memory positions" are scanned by a 4-bit B.C.D. coded input which may be 0 to -15 V time slot data or T^2 levels or any combination thereof. The 12 "word" lines are T^2 compatible only and NEG true. Several "word lines" may be true at one time as long as memory locations (time slots) are not shared.

Intended applications are for encoding of CRT read-out directly with electrically alterable information. Other variations are possible, such as it may be used to multiplex and encode three, 4-bit words.

Programming is accomplished by inexpensive preohmic and emitter mask changes.

Power Supply: V_{CC} 0 V
V_{EE} -15 V.

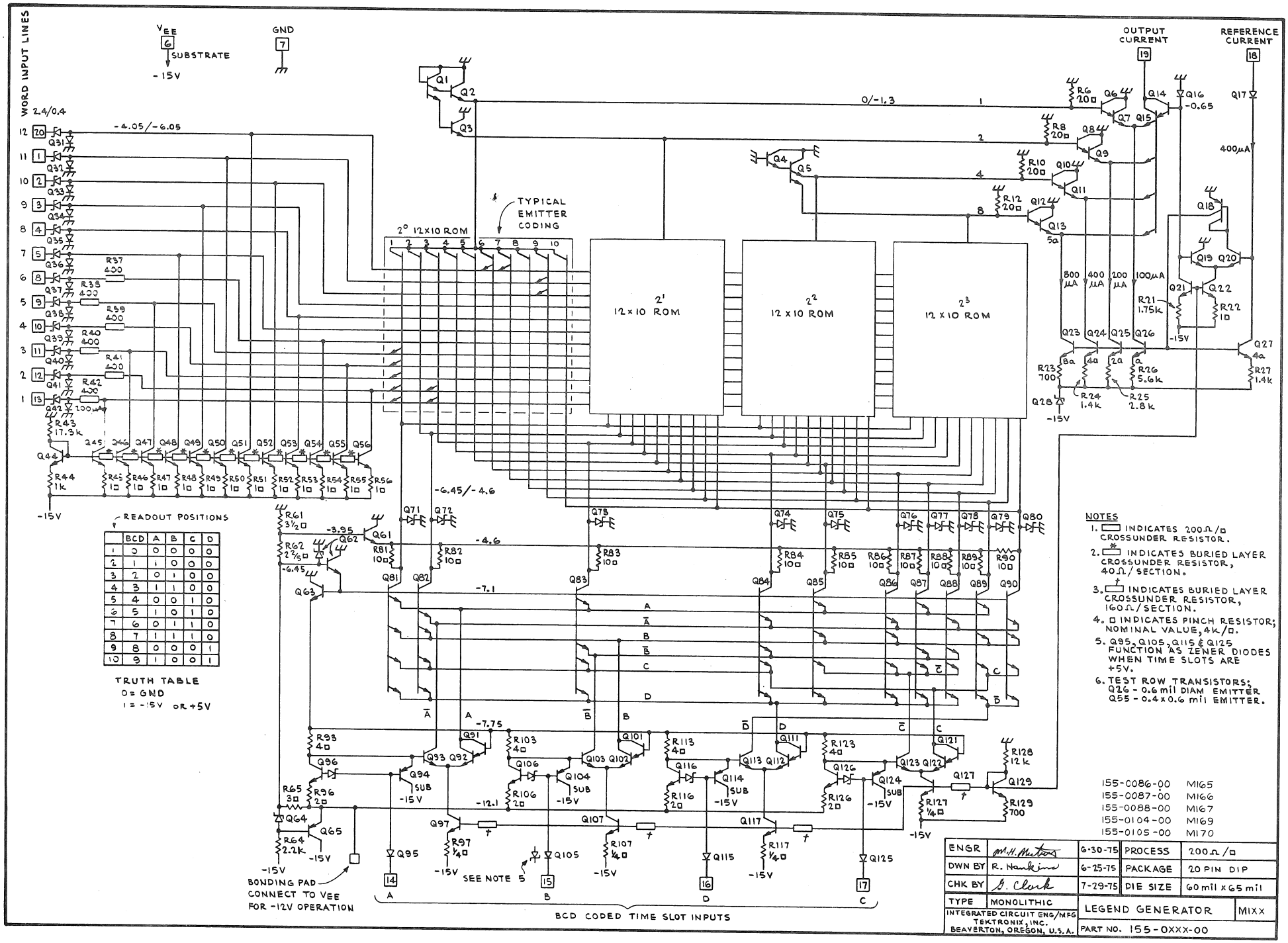
Package: 20 DIP

Designers: Roger McCoy/Mike Metcalf

ICE Contact: Mike Metcalf

Instrument Usage:

155-0086-00 - 7D15 ("R") (1)	155-0104-00 - 7J20 ("C3") (1)
155-0087-00 - 7D15 ("C1")(1)	155-0105-00 - 7J20 ("A") (1)
155-0088-00 - 7D15 ("C2")(1)	155-0104-00 - 7J20 ("C3A")(1)
155-0088-00 - 7L13 ("C2")(1)	155-0105-00 - 7J20 ("R3") (1)


WORD INPUT LINES
VEE
SUBSTRATE
-15V
GND
OUTPUT CURRENT
REFERENCE CURRENT
TYPICAL EMITTER CODING
2° 12x10 ROM
2¹ 12 x 10 ROM
2² 12 x 10 ROM
2³ 12 x 10 ROM
READOUT POSITIONS
TRUTH TABLE
0 = GND
1 = -15V OR +5V
BONDING PAD CONNECT TO VEE FOR -12V OPERATION
SEE NOTE 5
BCD CODED TIME SLOT INPUTS
NOTES
1. INDICATES 200Ω/□ CROSSUNDER RESISTOR.
2. INDICATES BURIED LAYER CROSSUNDER RESISTOR, 40Ω/SECTION.
3. INDICATES BURIED LAYER CROSSUNDER RESISTOR, 160Ω/SECTION.
4. □ INDICATES PINCH RESISTOR; NOMINAL VALUE, 4k/□.
5. Q95, Q105, Q115 & Q125 FUNCTION AS ZENER DIODES WHEN TIME SLOTS ARE +5V.
6. TEST ROW TRANSISTORS: Q26 - 0.6 mil DIAM EMITTER Q55 - 0.4x0.6 mil EMITTER.
155-0086-00 M165
155-0087-00 M166
155-0088-00 M167
155-0104-00 M169
155-0105-00 M170
ENGR M.H. Mutton 6-30-75 PROCESS 200Ω/□
DWN BY R. Hawkins 6-25-75 PACKAGE 20 PIN DIP
CHK BY G. Clark 7-29-75 DIE SIZE 60 mil x 65 mil
TYPE MONOLITHIC
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.
LEGEND GENERATOR MIXX
PART NO. 155-0XXX-00

ROM PROGRAMMING

TIME SLOT

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	3	4	5	10												
2	3	4	5	10												
3	3	4		10												
4	3	4		10												
5	3	4		10												
6		4		10												
7																
8																
9																
10									3	4						
11									3							
12			4	4	4	5	3	4								

155-0086-00

M165

NOTE: The number in the square is in terms of tenths of mA of output current.

Crossed out area is not used.

ROM PROGRAMMING

TIME SLOT

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	7	5	4		2											
2	6	5	4		2											
3	3	1			2											
4	2	1			2											
5	1	1			2											
6		1			2											
7						1	1	1								
8						1	1									
9						1										
10									1	1						
11									5							
12			10	2	10	2	9	1								

155-0087-00

M166

NOTE: The number in the square is in terms of tenths of mA of output current.

Crossed out area is not used.

ROM PROGRAMMING

TIME SLOT

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1		8														
2		4														
3		2														
4		1														
5					7											
6					6											
7					5											
8			8													
9			4													
10			2													
11			1													
12									10							

155-0088-00

M167

NOTE: The number in the square is in terms of tenths of mA of output current.

Crossed out area is not used.

ROM PROGRAMMING

TIME SLOT

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1							3		1	5						
2					3		1	5	1	1						
3					2		1	3	1	1						
4							5		1	9						
5							3		1	5						
6							2		1							
7					2		1		1							
8							6		1							
9							3		1							
10							2		1							
11			5	5												
12			4	4												

155-0104-00

M169

NOTE: The number in the square is in terms of tenths of mA of output current.

Crossed out area is not used.

ROM PROGRAMMING

TIME SLOT

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1			9	9		9										
2				9												
3				9												
4			9	9		9										
5			9	9		9										
6			9													
7																
8			9													
9			9													
10			9													
11									2	2						
12									4	4						

155-0105-00

M170

NOTE: The number in the square is in terms of tenths of mA of output current.

Crossed out area is not used.

TIME SLOT

WORD	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1				1	1	1	1									
2				2	2	2	2									
3				4	4	4	4									
4				8	8	8	8									
5	1															
6	2															
7								1								
8								2								
9		6														
10		1														
11			10													
12	10															

155-0135-00

M171

NOTE:

The number in the square is in terms of tenths of mills of current.

Crossed out area is not used.

V. READOUT SYSTEM

V.1,2,3,4,5.

IN Production
by CER

Readout System

M033B	155-0004-01
M034C	155-0005-00
M035B	155-0006-01
M038C	155-0007-01
M039C	155-0008-01

Description:

The 576 readout system is comprised of four fiberoptic readout modules. Three of these modules are each driven by a M038 and M039. The fourth module displays the ration of vertical current/div. to base step/div. This beta/div. readout is driven by M033, M034 and M035. The IC's are programmed from switch closures or external inputs and perform the required logic functions to drive the lamps in the readout.

Power Supply: V_{CC} + 5 V

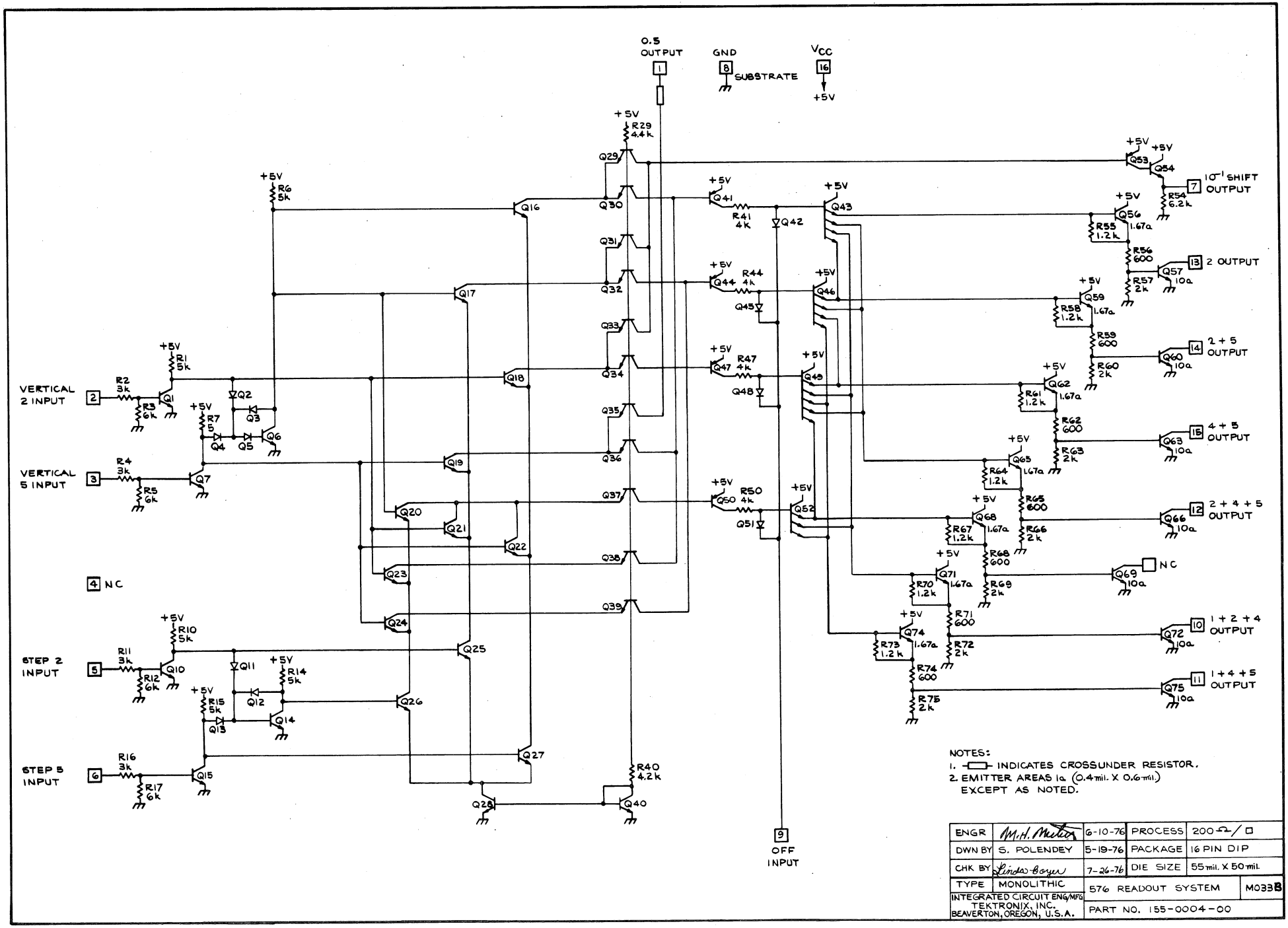
Package: All in 16 DIP

Designer: Mike Metcalf

ICE Contact: Mike Metcalf

Instrument Usage:

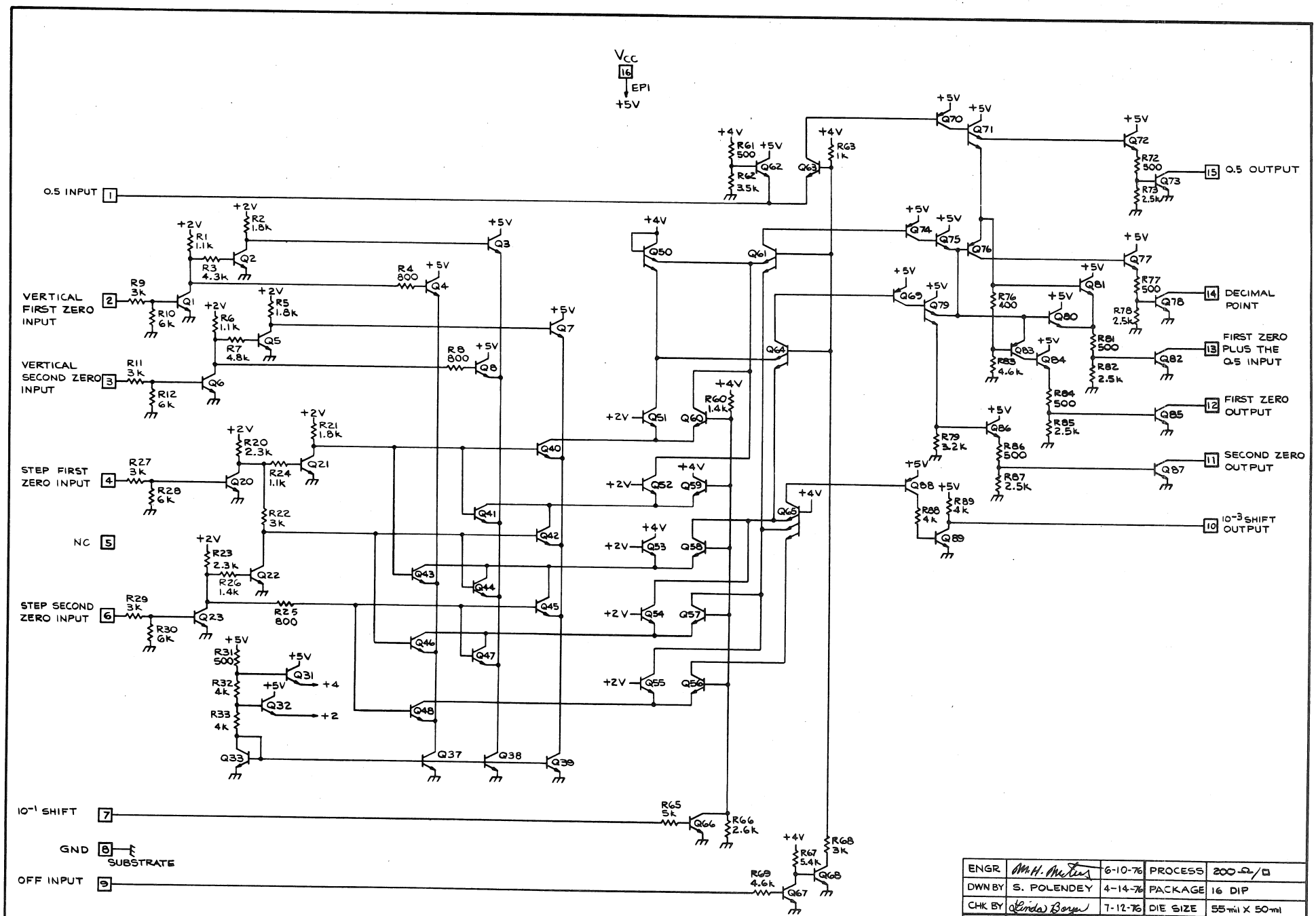
155-0004-01	576 (1)
155-0005-00	576 (1)
155-0006-01	576 (1)
155-0007-01	576 (3)
155-0008-01	576 (3)



NOTES:
1. -▭- INDICATES CROSSUNDER RESISTOR.
2. EMITTER AREAS 1a (0.4 mil. X 0.6 mil.) EXCEPT AS NOTED.

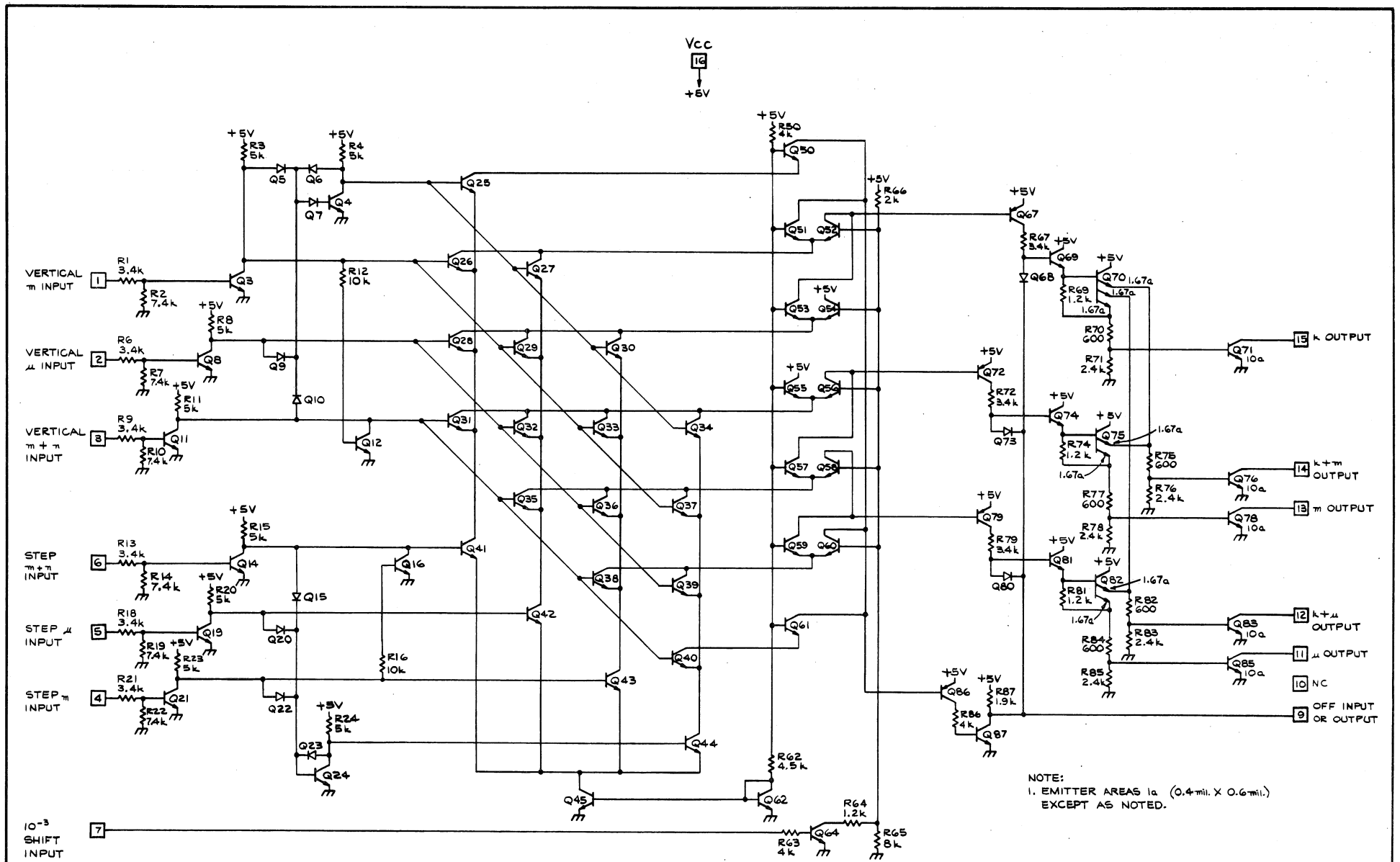
ENGR	M.H. Melton	6-10-76	PROCESS	200 Ω/□
DWN BY	S. POLENDEY	5-19-76	PACKAGE	16 PIN DIP
CHK BY	Linda Boyer	7-26-76	DIE SIZE	55 mil. X 50 mil.
TYPE	MONOLITHIC	576 READOUT SYSTEM		M033B
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0004-00		

V. 1.



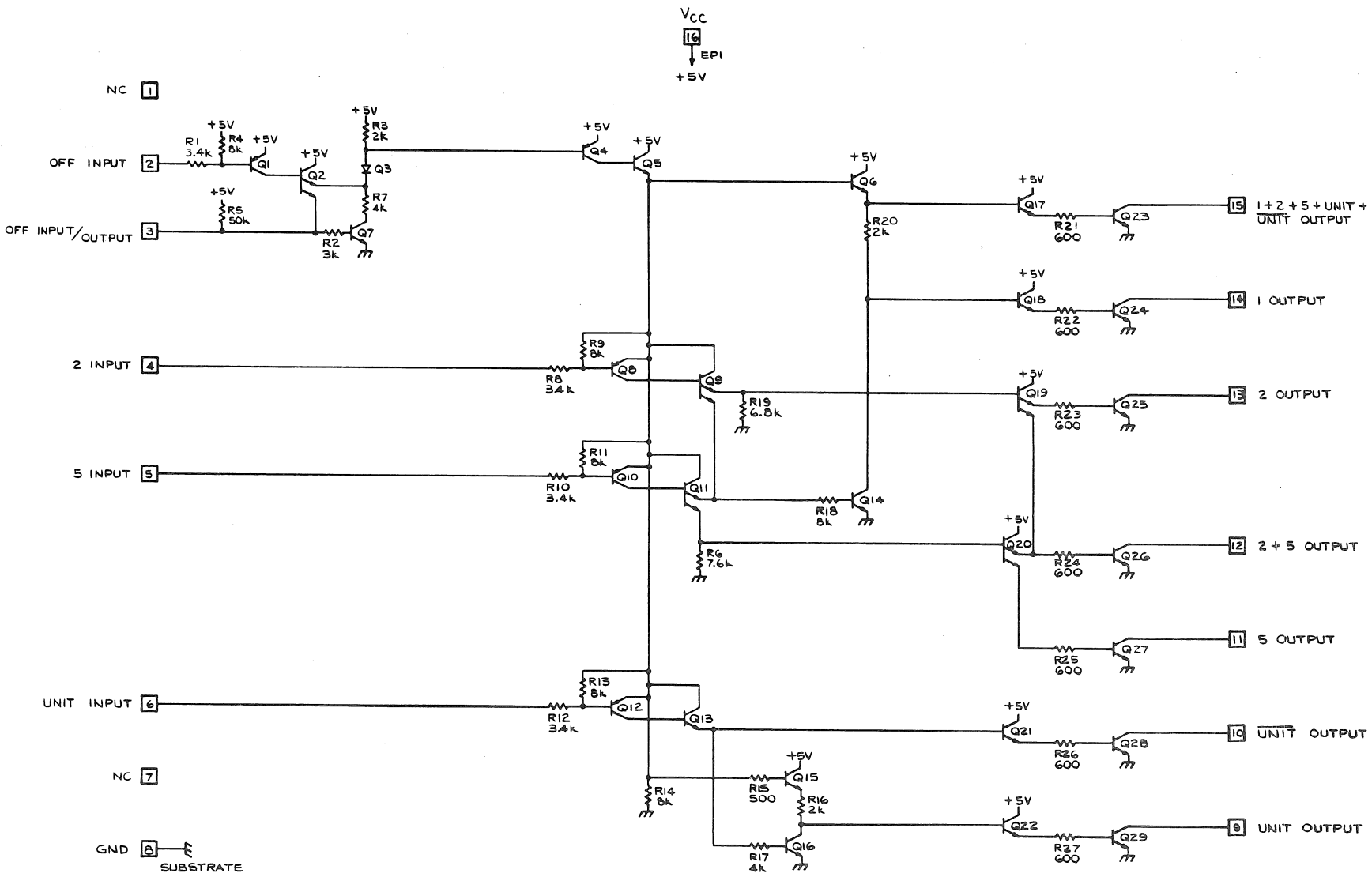
ENGR	M.H. Metzes	6-10-76	PROCESS	200 Ω/□
DWN BY	S. POLENDEY	4-14-76	PACKAGE	16 DIP
CHK BY	Linda Boyer	7-12-76	DIE SIZE	55 mil X 50 mil
TYPE	MONOLITHIC	576 READOUT SYSTEM		M034C
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0005-00		

V. 2.



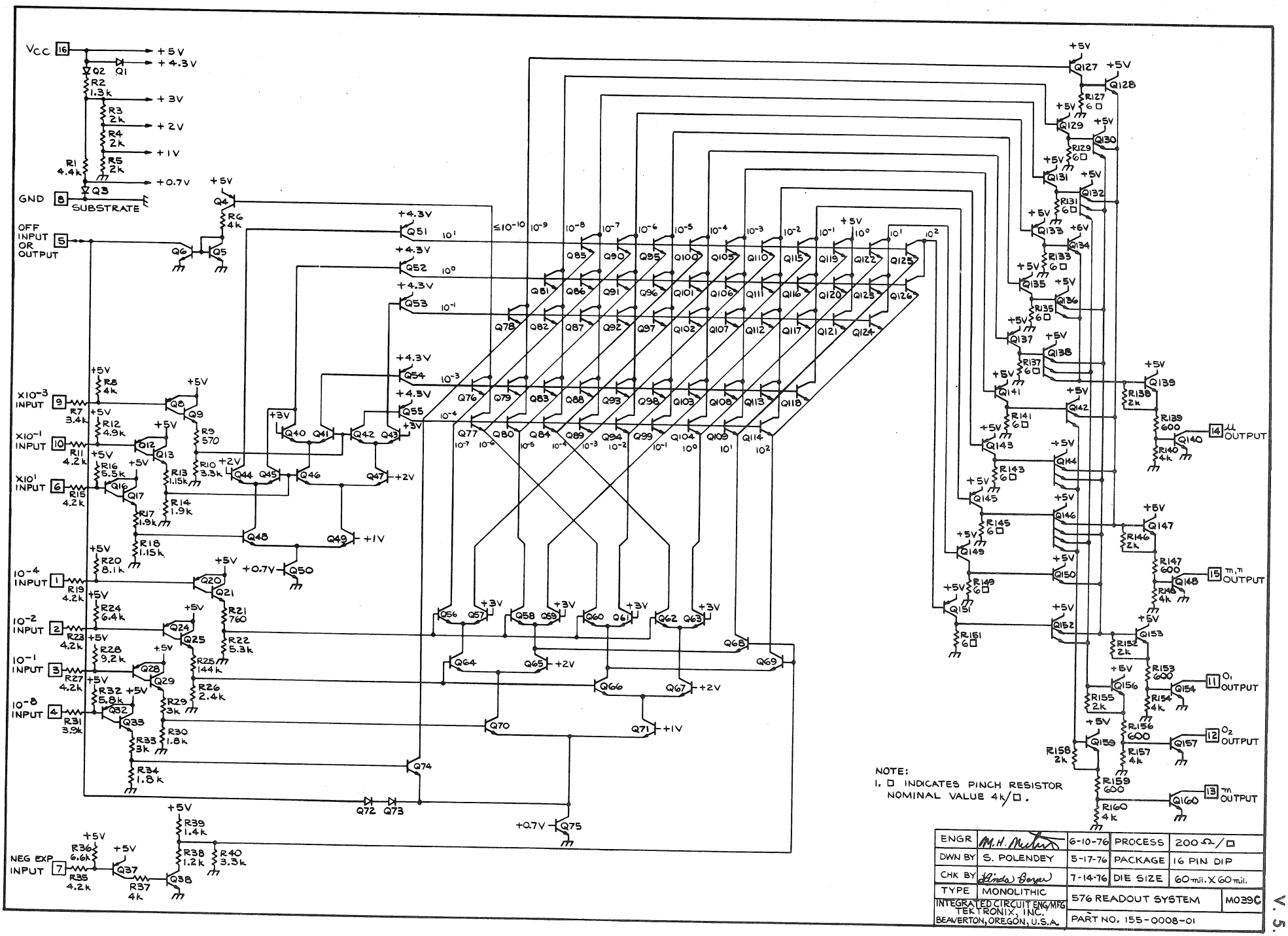
NOTE:
1. EMITTER AREAS 1a (0.4 mil. X 0.6 mil.) EXCEPT AS NOTED.

ENGR	M.H. Mitra	6-10-76	PROCESS	200 Ω/□
DWN BY	S. POLENDEY	5-25-76	PACKAGE	16 PIN DIP
CHK BY	Linda Bayer	7-15-76	DIE SIZE	55 mil. X 50 mil.
TYPE	MONOLITHIC	576 READOUT SYSTEM		M035B
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON U.S.A.		PART NO. 155-0006-01		



ENGR	M. H. Mitchell	6-10-76	PROCESS	200 Ω/□
DWN BY	S. POLENDEY	5-5-76	PACKAGE	16 PIN DIP
CHK BY	Linda Boyer	7-13-76	DIE SIZE	50 mil X 50 mil.
TYPE	MONOLITHIC	576 READOUT SYSTEM		M038C
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, USA		PART NO. 155-0007-00		

V.4.


Vcc 16
+5V
+4.3V
+3V
+2V
+1V
+0.7V
GND 8
SUBSTRATE
OFF INPUT OR OUTPUT 5
X10⁻³ INPUT 9
X10⁻¹ INPUT 10
X10¹ INPUT 6
10⁻⁴ INPUT 1
10⁻² INPUT 2
10⁻¹ INPUT 3
10⁻⁸ INPUT 4
NEG EXP INPUT 7
14 μ OUTPUT
15 m,n OUTPUT
11 O₁ OUTPUT
12 O₂ OUTPUT
13 m OUTPUT
NOTE:
1. □ INDICATES PINCH RESISTOR NOMINAL VALUE 4k/□.
ENGR M.H. Mutter 6-10-76 PROCESS 200Ω/□
DWN BY S. POLENDEY 5-17-76 PACKAGE 16 PIN DIP
CHK BY Linda Berger 7-14-76 DIE SIZE 60 mil. X 60 mil.
TYPE MONOLITHIC
576 READOUT SYSTEM M039C
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.
PART NO. 155-0008-01

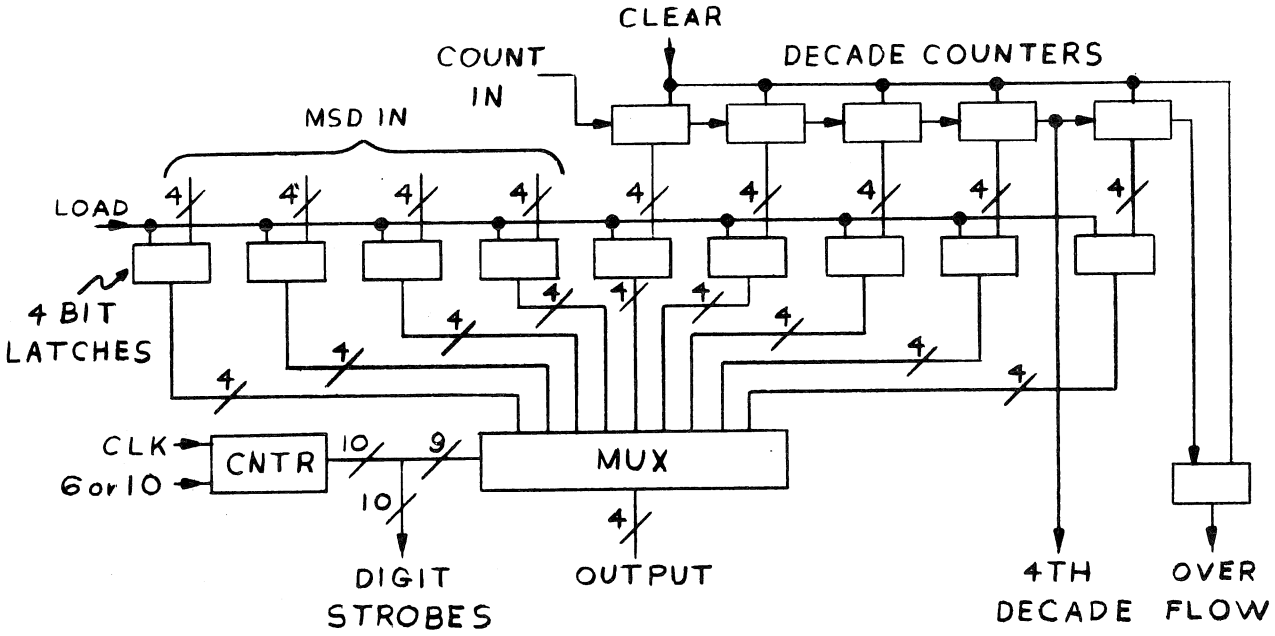
V. 5.

IN Production

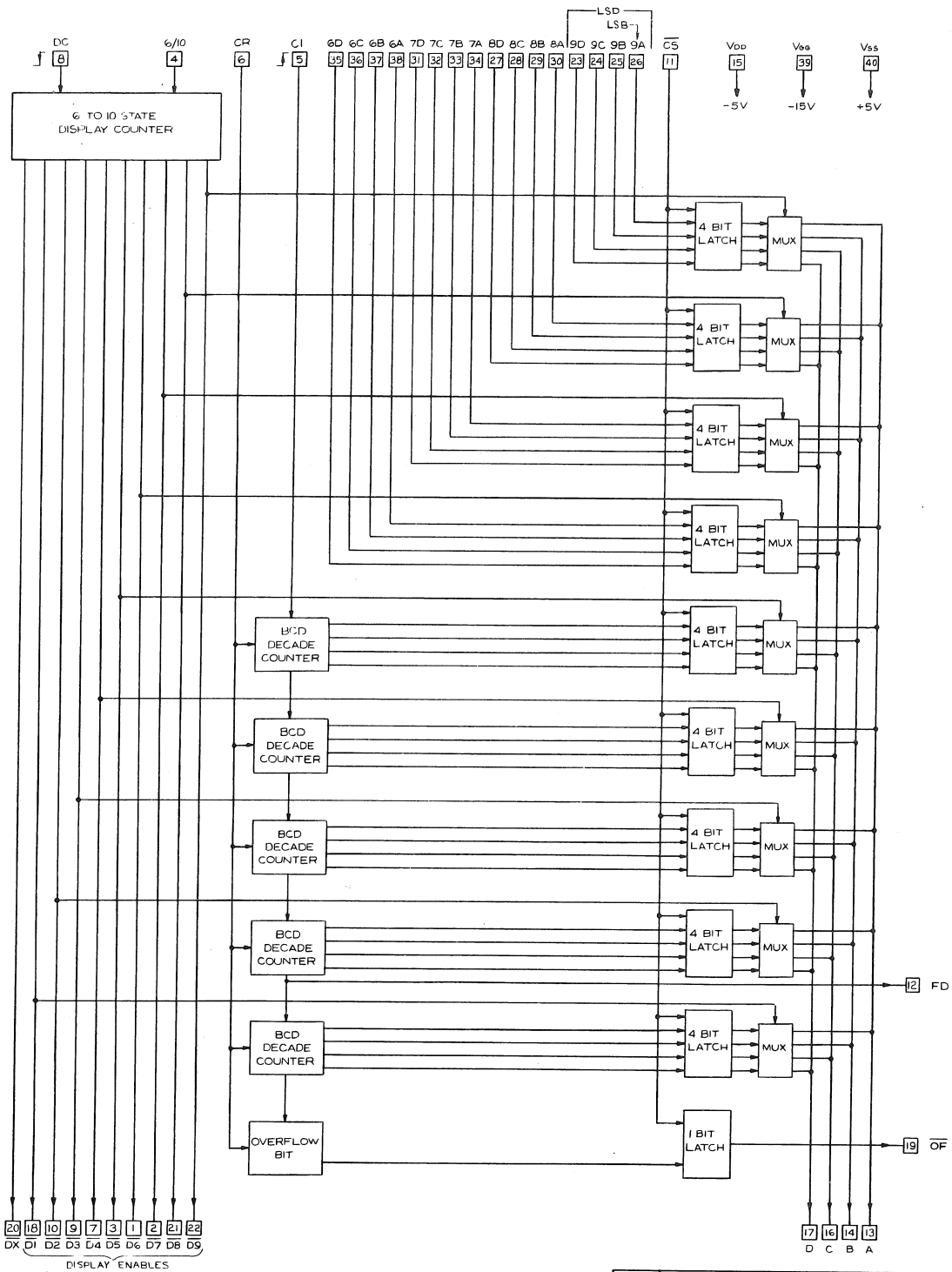
M123A 155-0119-00 5 DIGIT BCD COUNTER

Description:

The M123 is a five digit BCD counter with the outputs buffered and multiplexed. The maximum input count frequency is 5 MHz and an overflow latch is provided to detect over range counts. The chip also contains latches for four higher order digits which can be loaded from external counter stages. All nine digits are multiplex out serially. Digit strobes are provided in order to easily interface to LED readouts. The output multiplexer can be set to strobe out only the five least significant digits. An extra strobe is provided as a time slot for decimal points or units. The output of the fourth decade is also brought out.



Power Supply:	+5, -5, -15
Package:	40 PIN DIP
Designer:	Dave Allstot
ICE Contact:	Randy Young
Instrument Usage:	DC508



ENGR	J M CONNELL	1-16-76	PROCESS	MOS
DWN BY	J. Langley	1-9-76	PACKAGE	40 PIN DIP
CHK BY	Linda Boyer	2-25-76	DIE SIZE	124 mil X 129 mil
TYPE	MONOLITHIC	5 DIGIT BCD COUNTER BLOCK DIAGRAM		M123
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC BEAVERTON, OREGON, U.S.A.		PART NO. 155-0119-00		

IN Engineering

M127C 155-0114-00 SEVEN SEGMENT CHARACTER GENERATOR

Description:

This circuit takes information inputed in BCD form (negative logic), decodes it, and generates the necessary outputs to display a seven segment character on a CRT screen. Inputs have TTL voltage thresholds. The X and Y position outputs are currents as is the Z-axis output. A character segment is generated by first positioning the segment origin with X and Y currents and then ramping either the X or Y current to create the segment. The next segment is created by repositioning the origin and again ramping either X or Y, and so on. A sign input is provided allowing a choice of plus, minus or no sign to be displayed. Outputs are provided to indicate when the M127 is generating a character and to indicate when a decimal point is being made.

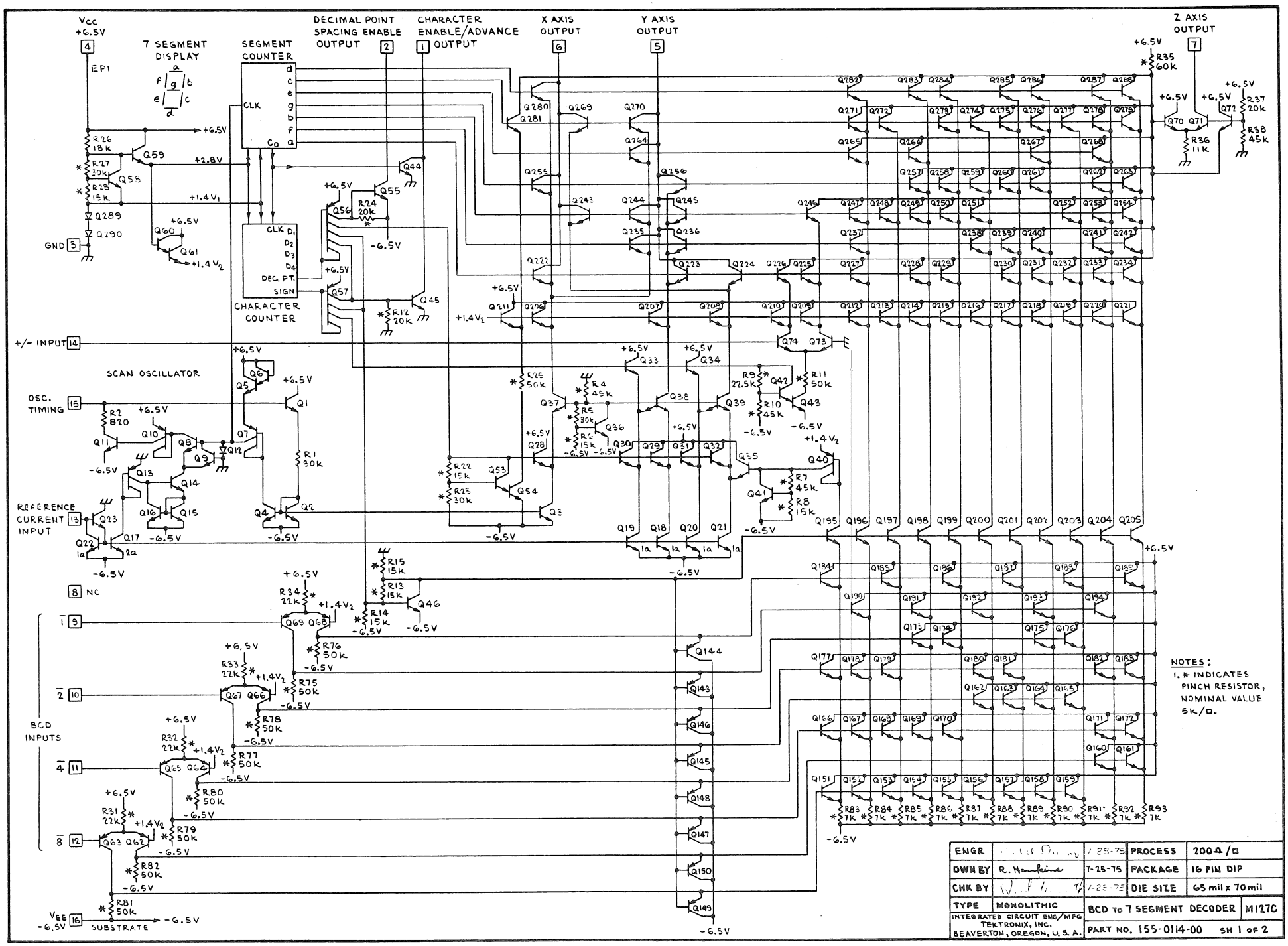
Power Supply: V_{CC} + 6.5 V
V_{EE} - 6.5 V.

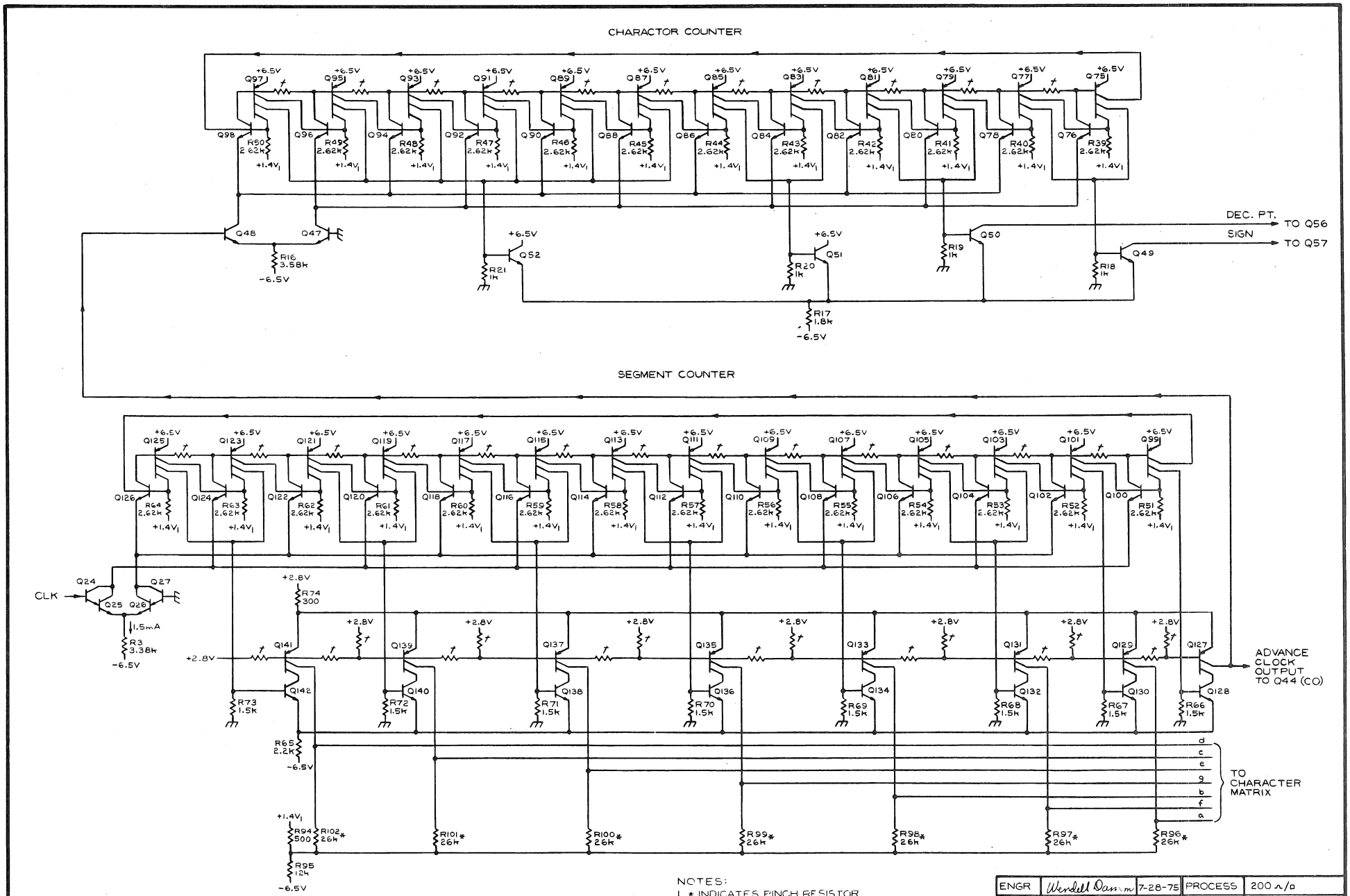
Package: 16 DIP

Designer: Wendell Damm

ICE Contact: Walt Ainsworth

Instrument Usage: 213 (1)


Vcc +6.5V
DECIMAL POINT SPACING ENABLE OUTPUT
CHARACTER ENABLE/ADVANCE OUTPUT
X AXIS OUTPUT
Y AXIS OUTPUT
Z AXIS OUTPUT
7 SEGMENT DISPLAY
SEGMENT COUNTER
CHARACTER COUNTER
SCAN OSCILLATOR
+/- INPUT
OSC. TIMING
REFERENCE CURRENT INPUT
NC
BCD INPUTS
GND
VEE -6.5V
SUBSTRATE
NOTES:
1. * INDICATES PINCH RESISTOR, NOMINAL VALUE 5K/□.
ENGR
DWN BY R. Hawkins T-25-75
CHK BY
PROCESS 200Ω/□
PACKAGE 16 PIN DIP
DIE SIZE 65 mil x 70 mil
TYPE MONOLITHIC
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.
BCD to 7 SEGMENT DECODER
M127C
PART NO. 155-0114-00 SH 1 OF 2



NOTES:
1. * INDICATES PINCH RESISTOR NOMINAL VALUE 5kΩ/□.
2. ⊤ INDICATES EPI RESISTOR.

ENGR	Wendell Dansm	7-28-75	PROCESS	200 Ω/□
DWN BY	J. Langley	7-14-75	PACKAGE	16 PIN DIP
CHK BY	Walt Ausmith	7-28-75	DIE SIZE	65 mil X 70 mil
TYPE	MONOLITHIC	BCD TO 7-SEGMENT DECODER		M127
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0114-00		SH 2 OF 2

V. 7.

VI. HORIZONTAL SYSTEMS

IN Production
by CER

M018G 155-0028-00, -01
155-0042-02, -03

MILLER INTEGRATOR & DELAY PICKOFF

Description:

Circuit Performance: (0°C to + 70°C)

A. All Input Gating

(Pins 1 and 5) as follows:

0 . . . . . < 0.4 V

1 . . . . . > 0.8 V (0.5 mA to 5 mA), current limit required.

B. Integrator Out (Pin 3)

1. Maximum slewing rate 1 volt/100 ns. This is premised on an Integrating I of 1 mA and a timing of C of 100 pF.
2. Maximum loading: ≤ 2 mA in addition to the Integrating I.
3. Timing C: 100 pF to 10 μF (connected between Pins 8 and 9).
4. Integrating I: + 1 μA to + 1 mA (out of Pin 9).
5. Quiescent level (Pin 1 . . . logic 0)
   a. Integrating I: 1 μA to 0.2 mA, Level ± 50 mV
   b. Integrating I: > 0.2 mA to 1 mA, Level ± 75 mV
6. Z Out: ≤ 50 ohms.

C. Summing Pt (Pin 9)

Error I ≤ 1 nA at 25°C, reducible to ≤ 0.5 nA at 25°C using Thermalloy 2211B Heat radiator.

D. Delayed Gate Out (Pin 4)

1. Waveform: Ground referenced + 3.5 V step. I limited to 3 mA with + 10 V supply and 5 mA with + 15V supply.
2. Risetime: ≤ 50 ns with falltime 2 k paralleled by 10 pF.
3. Jitter: When used as a delaying gate ≤ 40 k:1.
4. Hysterysis: ie. the Integrator out excursion necessary to switch Gate on (+ 3.5V) then off (0 V) ± 10 mV.

M018G (continued)

Package: 10 Lead TO-5

Designer: Joe Burger

ICE Contact: Mike Metcalf

Instrument Usage:

155-0028-00

1480 (2)
1481 (2)
1482 (2)
1485 (2)
26G1 (2)
26G2 (1)
26G3 (1)
7L12 (1)
7L13 (1)
5S14 (1)
7S14 (1)

155-0042-02

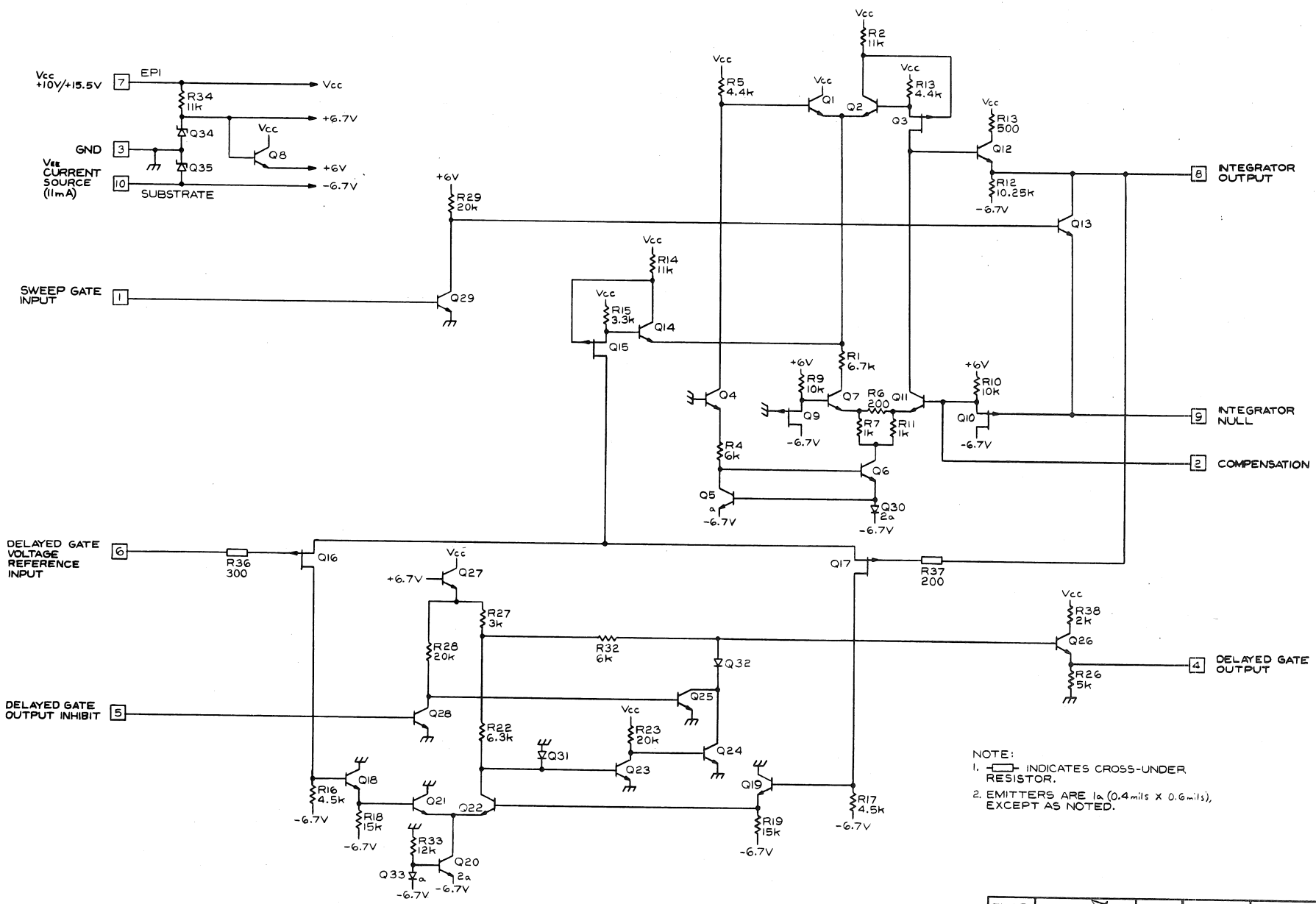
1401A (1)
5S14N (1)
7L12 (1)
7L13 (1)
7S14 (1)

155-0028-01

434 (1)
432 (1)

155-0042-03

7B53
314K (2)
5B10N (1)
5B12N (2)
5B40 (1)
5B42 (2)
5B42G (2)
55B31 (1)
5B53 (2)
RG501 (1)
5B10 (1)
5B12 (2)
5B53A (2)



ENGR	M. H. Mulvey	6-10-76	PROCESS	200 Ω/□ P-	
DWN BY	J. Langley	4-1-76	PACKAGE	10 LEAD TO-5	
CHK BY	Linda Bayer	7-13-76	DIE SIZE	50 mil X 50 mil	
TYPE	MONOLITHIC	MILLER INTEGRATOR & DELAY PICKOFF			M018G
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0028-00			

VI. 1.

IN Production
by CER

M042E 155-0056-00 SWEEP CONTROL

Description:

This single package control system is intended for use in conjunction with the M018 Miller Integrator and Delay Pickoff. Its primary application is for the H series of instruments, and it should be generally useful in other low-to-medium-speed applications. Logic inputs: RTL current limiting required.

Functions

Trigger slope selection and pulse forming.
Sawtooth start/stop.
Holdoff and single-sweep lockout.
Bright baseline generation.

Characteristics

Sweep (with M018):	Amplitude	0 to + 10 V starts at gnd.
	Max. output rate. . . .	10 V/μs
Triggering:	Min. Input (<10 MHz). .	0.2 mA p-p
	Max. usable frequency .	40 MHz
	Triggering delay. . . .	50 ns

The maximum usable frequency may be increased by connecting external T.D. trigger processing.

Power Supply: V_{CC} + 5 V.

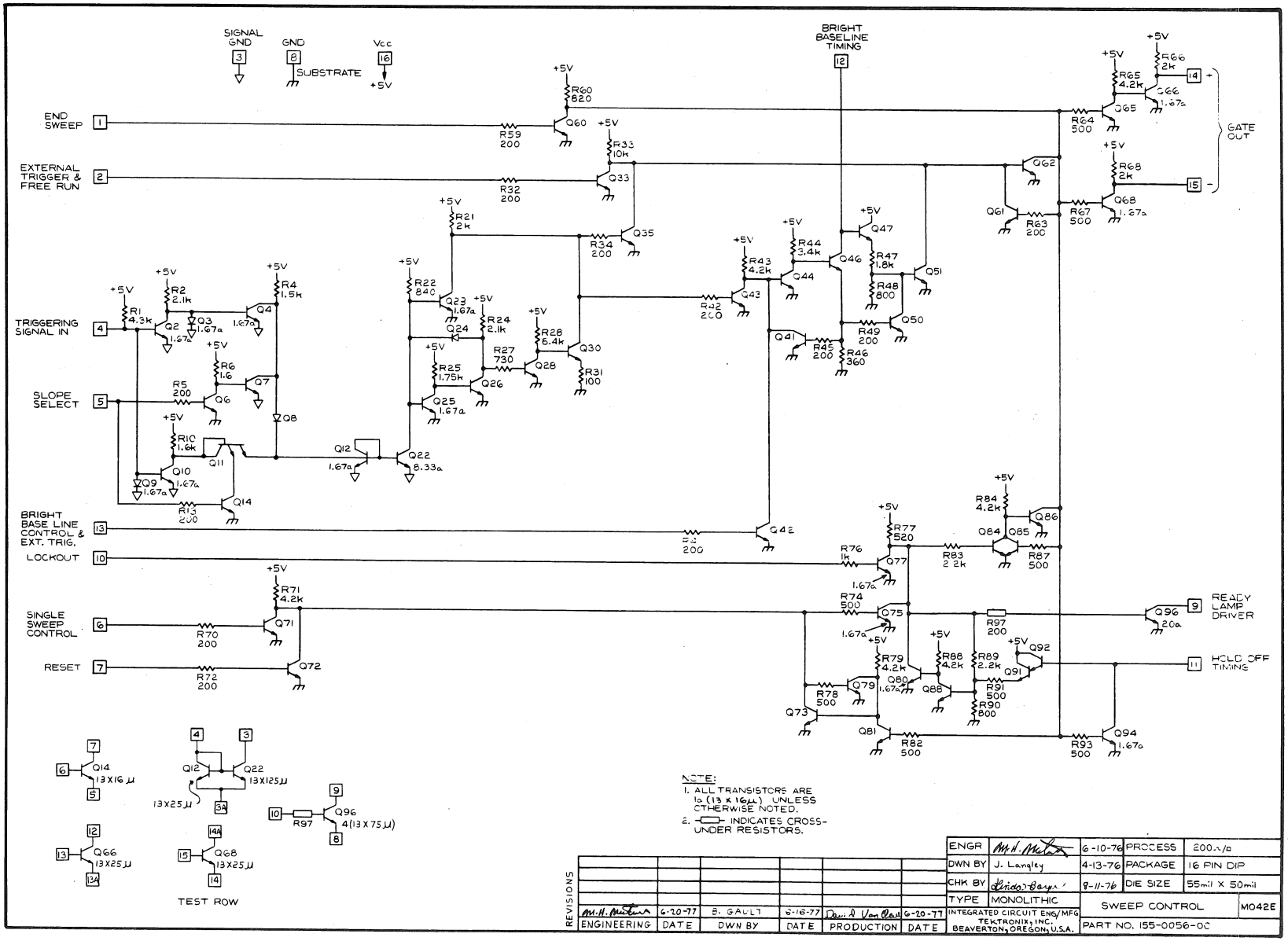
Package: 16 DIP

Designer: Val Garuts

ICE Contact: Mike Metcalf

Instrument Usage:

26G1 (1)	5B10N (1)	7L12 (1)
26G2 (1)	5B12N (2)	7L13 (1)
26G3 (1)	5S14N (1)	7S14 (1)
314K (1)	7L5 (1)	RG501 (1)
4701 (1)		


SIGNAL GND
GND
SUBSTRATE
Vcc
+5V
BRIGHT BASELINE TIMING
END SWEEP
EXTERNAL TRIGGER & FREE RUN
TRIGGERING SIGNAL IN
SLOPE SELECT
BRIGHT BASE LINE CONTROL & EXT. TRIG.
LOCKOUT
SINGLE SWEEP CONTROL
RESET
GATE OUT
READY LAMP DRIVER
HOLD OFF TIMING
TEST ROW
NOTE:
1. ALL TRANSISTORS ARE 1a (13 X 16μ) UNLESS OTHERWISE NOTED.
2. INDICATES CROSS-UNDER RESISTORS.
ENGR 6-10-76 PROCESS 200Ω/□
DWN BY J. Langley 4-13-76 PACKAGE 16 PIN DIP
CHK BY 8-11-76 DIE SIZE 55mil X 50mil
TYPE MONOLITHIC
SWEEP CONTROL M042E
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.
PART NO. 155-0056-00
REVISIONS
ENGINEERING 6-20-77 DATE
B. GALLI DWN BY 6-16-77 DATE
PRODUCTION 6-20-77 DATE

IN Production
by CER

M052F | 155-0048-00, 155-0048-01, 155-0055-00 | TRIGGER & SWEEP

Description:

This IC includes all functions for trigger and sweep.

TRIGGER:

Input: FET input, 50 mV to 1 V pp.

Level: Single control for level and plus or minus slope.

Frequency: DC to 5 MHz.

SWEEP:

Ramp Output: Negative slope from + 2 V to -2 V, ext. adj. ± 0.5 V.

Maximum dV/dT: 1 V/μsec.

Timing Resistor Voltage: + 2.5 V ± 0.5 V. (+2v+3v)

Holdoff: Ext. C, internal 0.25 mA timing I.

Auto Free-Run: External RC

Unblank Output: + 2 V during sweep.

Power Supply: ± 5 to ± 10 V at 8 mA

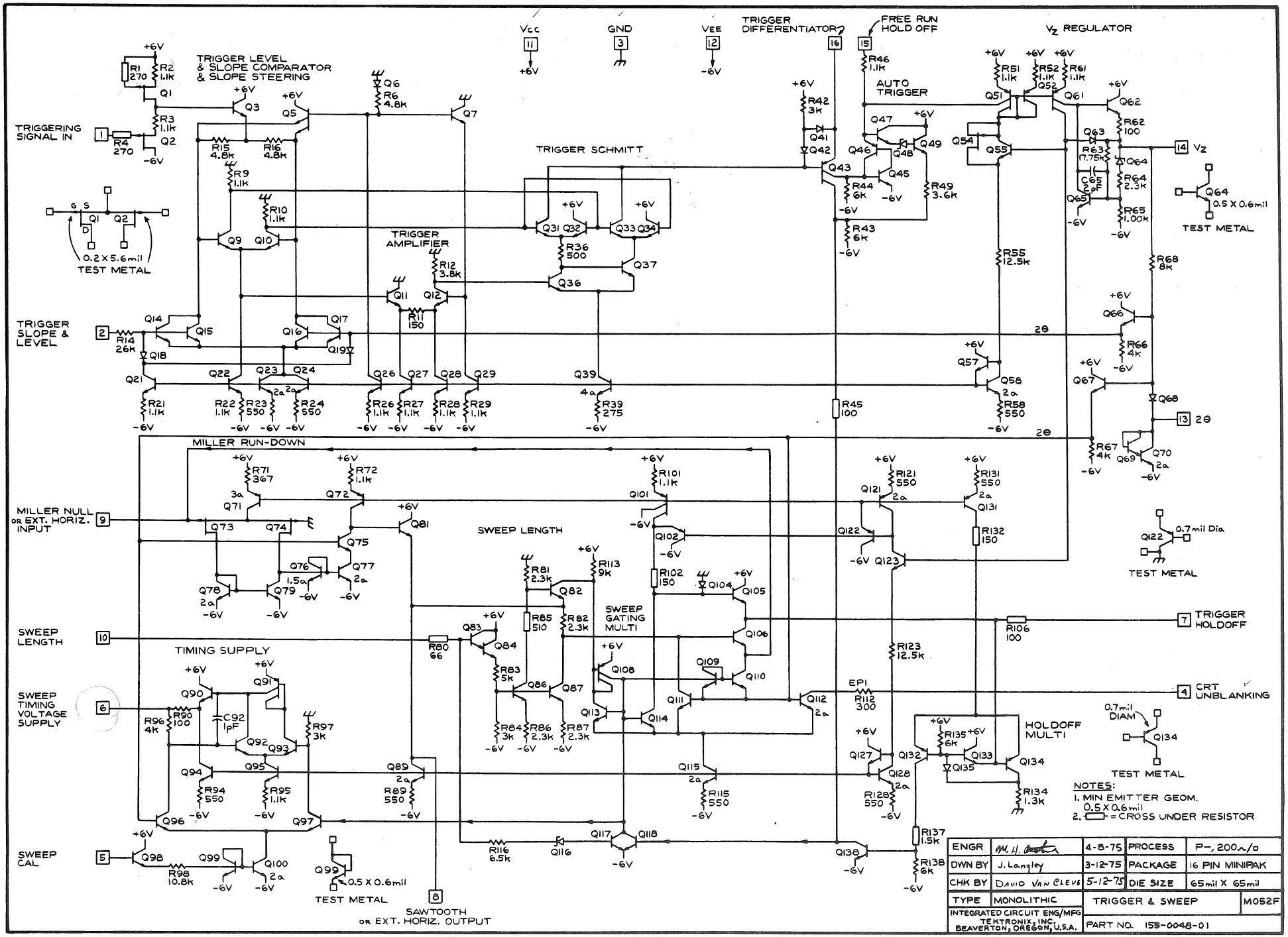
Package: 155-0048-01, 16 Minipac
155-0055-00, 16 DIP

Designer: Dave Allen

ICE Contact: {Mike Metcalf} 5586
Eng. Dave Vancleve
Ken Harris 5613

Instrument Usage:

211 (1)	5B12N (1)	SC501 (1)
212 (1)	5B13N (1)	5L4N (1)
213 (1)	603950H (1)	605950H (1)
214 (1)	604950H (1)	5B13NH (1)


Vcc
GND
VEE
TRIGGER DIFFERENTIATOR
FREE RUN HOLD OFF
Vz REGULATOR
TRIGGER LEVEL & SLOPE COMPARATOR & SLOPE STEERING
TRIGGERING SIGNAL IN
TRIGGER SCHMITT
AUTO TRIGGER
TRIGGER AMPLIFIER
TRIGGER SLOPE & LEVEL
TEST METAL
MILLER RUN-DOWN
MILLER NULL OR EXT. HORIZ. INPUT
SWEEP LENGTH
SWEEP GATING MULTI
TIMING SUPPLY
SWEEP TIMING VOLTAGE SUPPLY
SWEEP CAL
SAWTOOTH OR EXT. HORIZ. OUTPUT
TRIGGER HOLDOFF
CRT UNBLANKING
HOLDOFF MULTI
NOTES:
1. MIN EMITTER GEOM. 0.5 X 0.6 mil
2. = CROSS UNDER RESISTOR
ENGR
DWN BY J. Langley 3-12-75
CHK BY DAVID VAN CLEVE 5-12-75
4-8-75
PROCESS P-, 200Ω/□
PACKAGE 16 PIN MINIPAK
DIE SIZE 65 mil X 65 mil
TYPE MONOLITHIC
TRIGGER & SWEEP
M052F
INTEGRATED CIRCUIT ENG/MFG
TEKTRONIX, INC.
BEAVERTON, OREGON, U.S.A.
PART NO. 155-0048-01

IN Production

M079G 155-0049-01 SWEEP CONTROL

Description:

Sweep Control IC contains bright baseline auto circuit, single sweep circuit, and holdoff circuit with terminals for S.S. Reset Ready light, triggered light, auto timing, H.O. timing, and two pins for new gen. logic, ie. lock-out, and main frame delay mode control.

Power Supply: V_{CC} + 5 V
V_{EE} - 5 V.

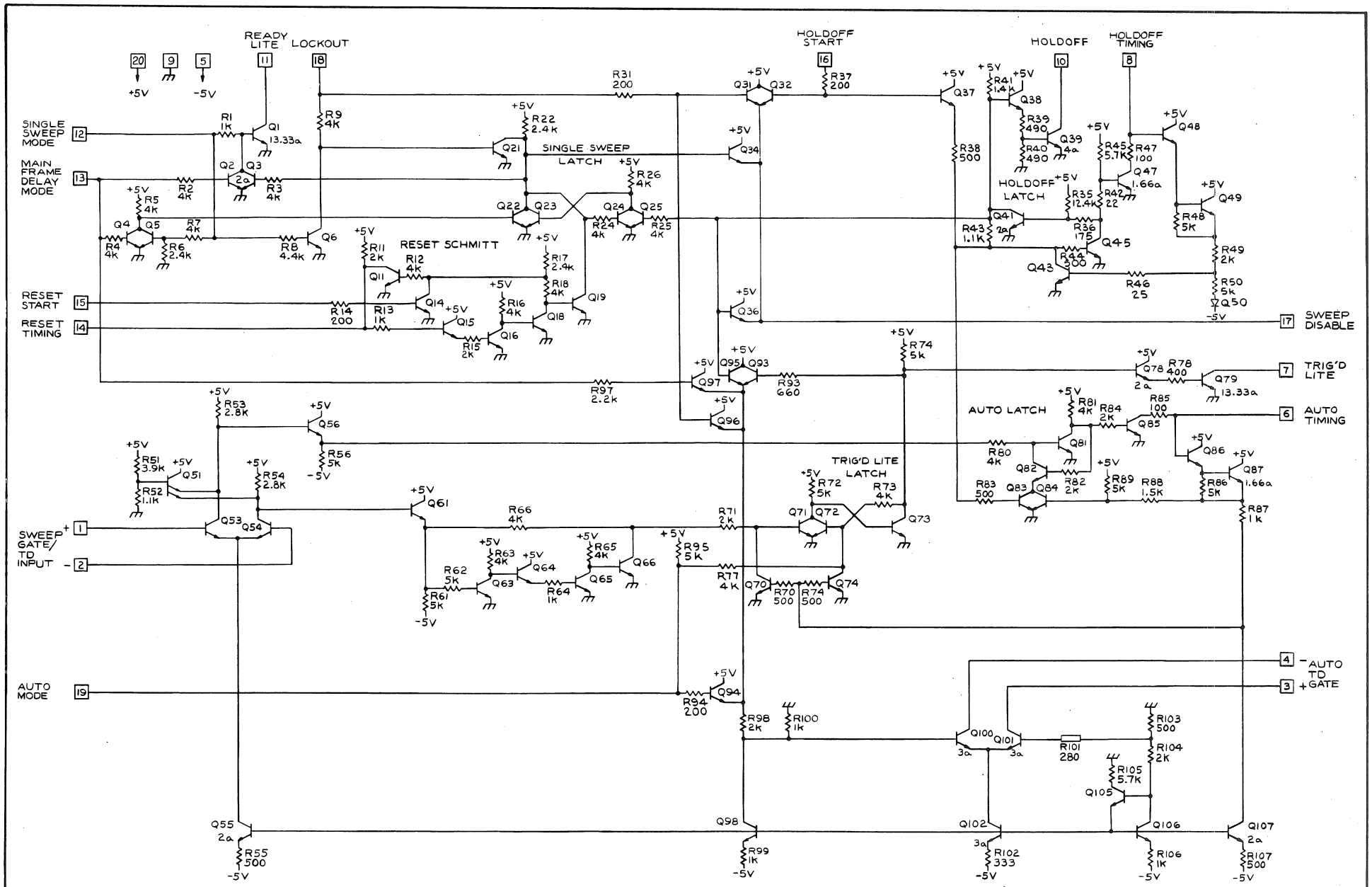
Package: 20 DIP

Designer: Bill DeVey

ICE Contact: Mike Metcalf

Instrument Usage:

7B92 (1)	485 (1)	7B53 (1)
335K (1)	5B31 (1)	4851 (2)
464 (1)	5B40 (1)	4852 (1)
465 (1)	5B42 (1)	SC502 (1)
466 (1)	5B42G (1)	Some 475 Mods (2)
475 (2)	5B44 (2)	7B50A (1)
7B80 (1)	7B85 (1)	



NOTE:
1. CROSS UNDER RESISTOR.
2. ALL EMITTER AREAS ARE 1a, (0.5 mil X 0.6 mil) UNLESS OTHERWISE INDICATED.

ENGR	M. H. Mathews	19 NOV 76	PROCESS	200 Ω/□
DWN BY	J. Langley	3 NOV 76	PACKAGE	20 PIN DIP
CHK BY	C. WESTON	19 JAN 77	DIE SIZE	60 mil X 60 mil
TYPE	MONOLITHIC	SWEEP CONTROL		M079G
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0049-02		

IN Production
by CER

M120B 155-0109-00 TRIGGER CIRCUIT

Description:

This circuit is intended for use in instruments in the medium to high frequency range. It employs SHF II processing, ECL circuitry, requires one power supply (plus five volts), dissipates about 500 mW, and is packaged in a 16 DIP. The circuit should be driven differentially. Hysteresis at low frequencies is 40 mV and increases bu a factor of 3 at 400 MHz. DC trigger input levels are at about 3.8 volts. A slope select control is included. Input signal conditioning (ie. preamplificattion and source selection) is done external to the IC. Another IC, the M121, has been designed to accomplish this. Other inputs are hold-off and end-sweep (tied together in typical application). A free run input is also provided. Gate out is at an ECL level.

Power Supply: V_{CC} + 5.0 V.

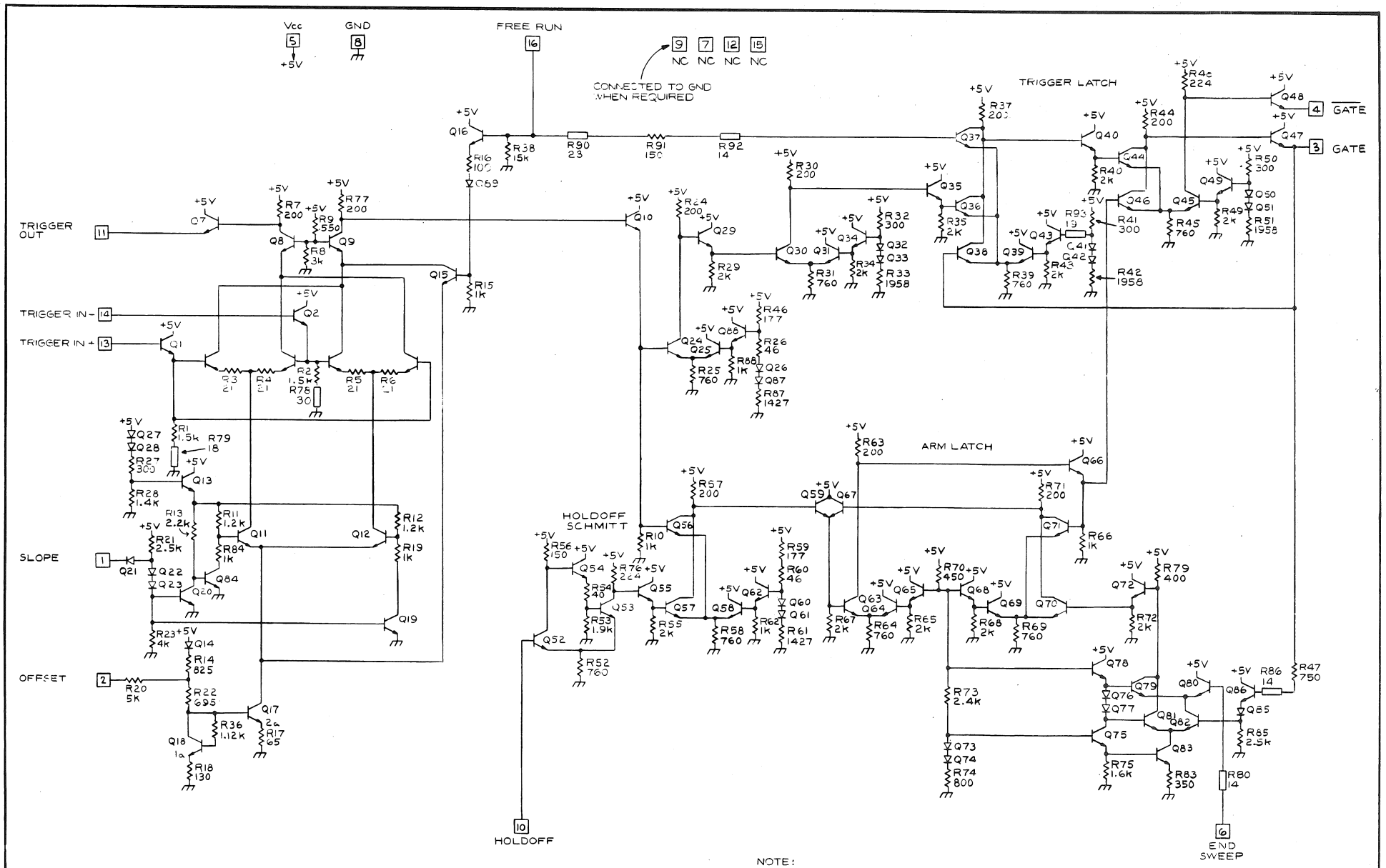
Package: 16 DIP (Kovar-Copper-Kovar)

Designer: Gary Vance

ICE Contact: Walt Ainsworth

Instrument Usage:

5B31	(1)	7B81P	
5B40	(1)	7B80	(1)
5B44	(2)	7B85	(1)
SC502	(1)	7B50A	(1)
5S14N	(1)	7S14	(1)



ENGR	Walt Ausmus	9-26-75	PROCESS	SH II
DWN BY	J. Langley	1-17-75	PACKAGE	16 PIN DIP
CHK BY	C. WESTON	7-30-76	DIE SIZE	65 mil x 65 mil
TYPE	MONOLITHIC	TRIGGER		M120B
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0109-01		

IN Production
by CER

M121C 155-0126-00 TRIGGER AMPLIFIER, SOURCE SELECT, AND PEAK-TO-PEAK AUTO

Description:

The M121 is designed to be used with the M120 ECL trigger IC in medium to high frequency instruments. It employs SHF II processing and requires two power supplies; +5 volts and a current source (25 mA out of the IC source compliance must range at least from -4.5 V to -5.5 V). Power dissipation is 425 mV, and the package is a 20 pin DIP. Provision is made for trigger source switching (5 inputs), high frequency rejection, trigger view, and P-P auto operation with addition of external components A level control is also provided. Input signal range is centered around ground, with input sensitivity of 4 - 5 mV when used with the M120. Maximum amplifier gain is 9, and bandwidth is 600 MHz. A selected version of the M121 having all the above features except for the peak-to-peak aut mode is available.

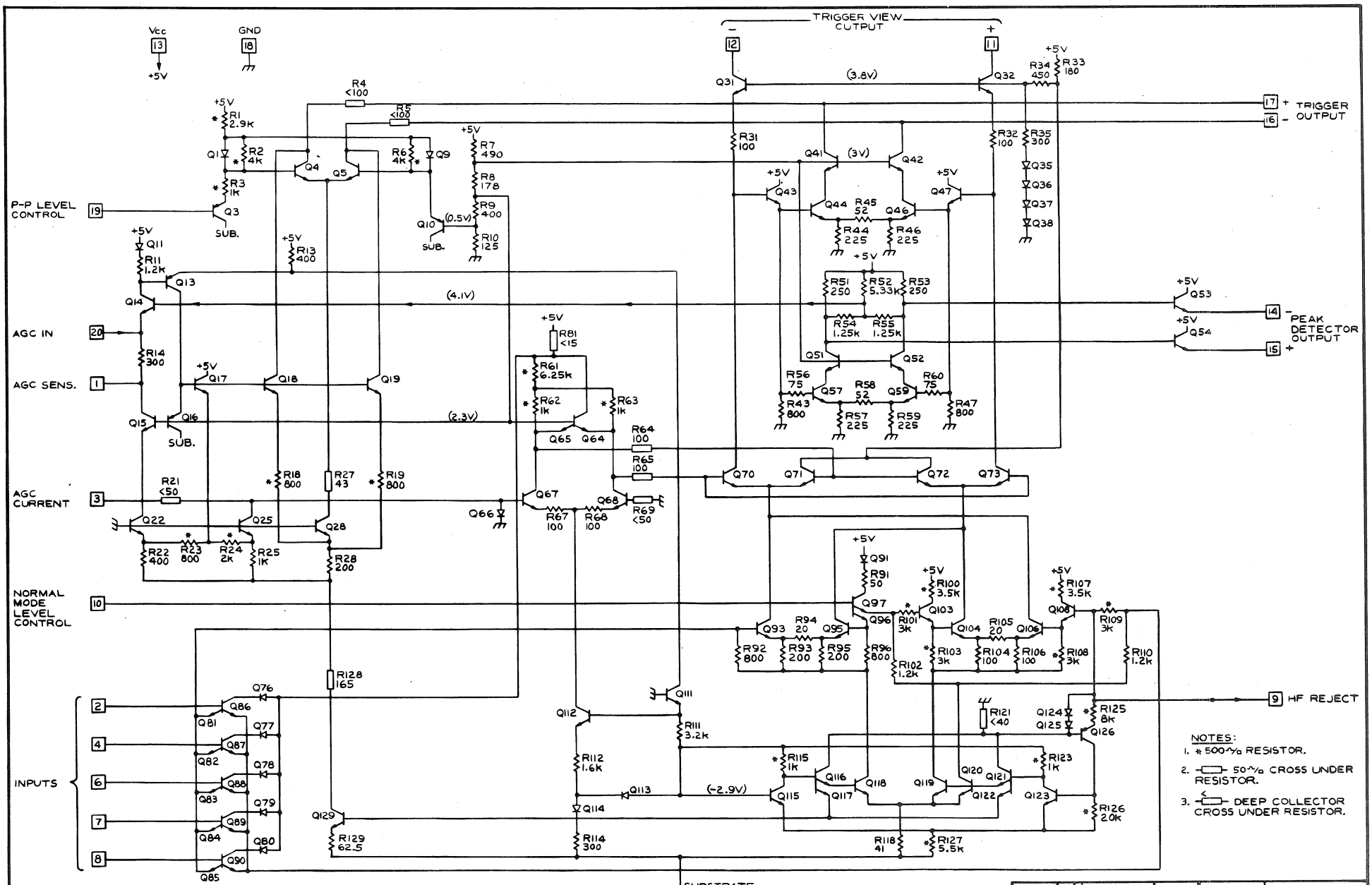
Power Supply: V_{CC} + 5.0 V
I_{EE} - 25 mA

Package: 20 pin DIP (Kovar-Copper-Kovar)

Designer: Art Metz

ICE Contact: Walt Ainsworth

Instrument Usage: 7B81P 7B85
7B80 7B50A



NOTES:
1. * 500 ~/o RESISTOR.
2. -[ ]- 50 ~/o CROSS UNDER RESISTOR.
3. <[ ]- DEEP COLLECTOR CROSS UNDER RESISTOR.

ENGR		5-20-75	PROCESS	SH II
DWN BY	J. Langley	2-5-75	PACKAGE	20 PIN DIP
CHK BY		7-22-75	DIE SIZE	65mil X 65mil
TYPE	MONOLITHIC	TRIGGER AMPLIFER		M121C
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0126-00		

IN Engineering

M122B 155-0150-00 FAST TRIGGER CIRCUIT

Description:

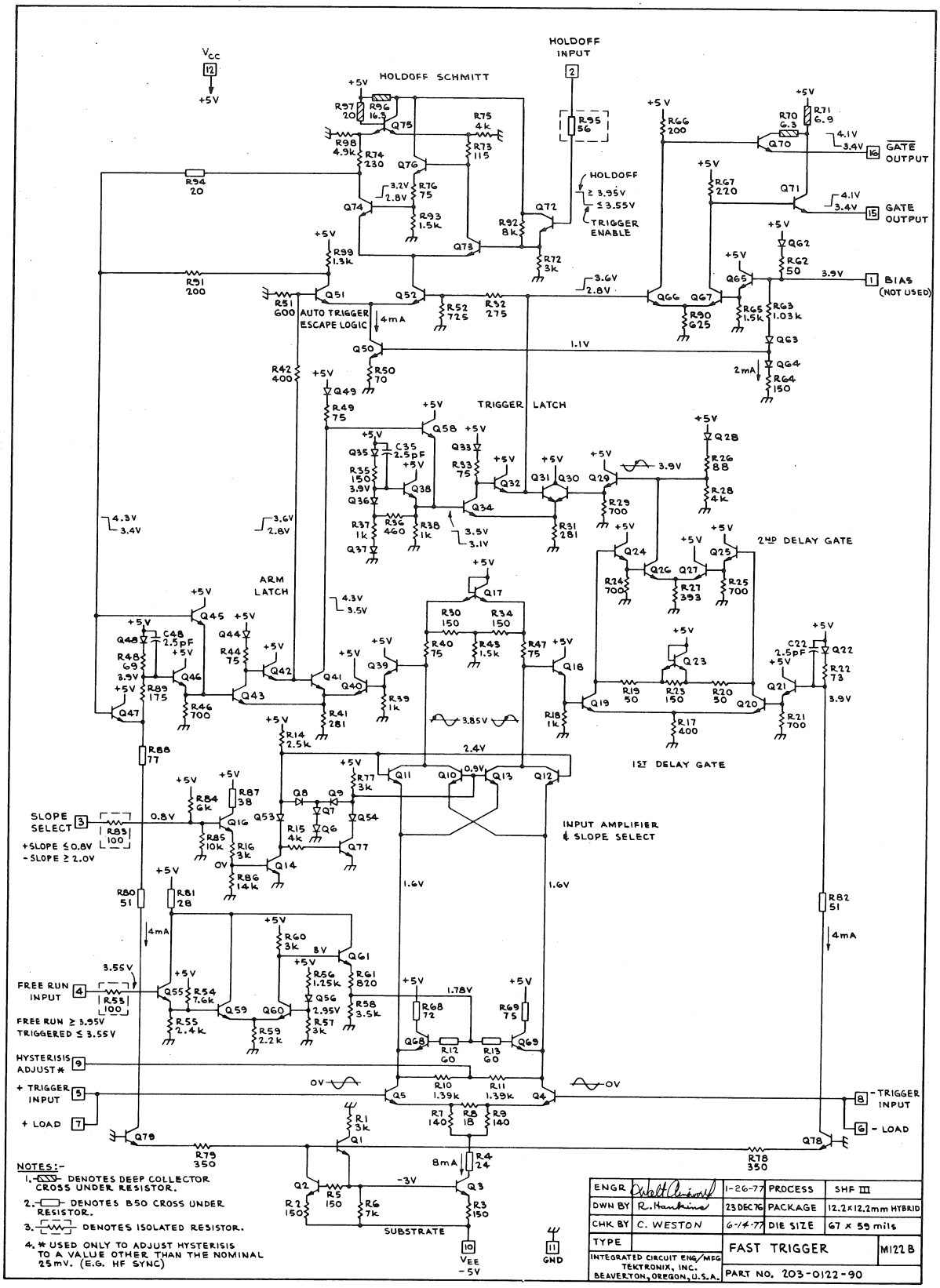
This circuit is intended for use in high frequency instruments. It employs SHF III processing, ECL/E^2L circuitry, requires two power supplies (plus and minus five volts), dissipates about 600 mW, and is packaged in a 1.25 cm x 1.25 cm hybrid substrate (H473). The circuit should be driven differentially. Input T-coiling is accomplished a combination of the M122 IC and the hybrid, the 50 Ω load resistors are not included in the hybrid. Hysteresis at low frequencies is 25 mV and increases by a factor of 2 to 3 at 1.2 GHz. DC trigger input levels are at zero volts. A slope select control is included. Input signal conditioning (ie. preamplification and source selection) is done external to the IC< Another IC, the M136, has been designed to accomplish this. Other inputs are hold-off and free-run (if that mode is to be used). Gate out is at an ECL level.

Power Supply: V_{CC} + 5.0 V
V_{EE} - 5.0 V.

Package: 1.25 cm x 1.25 cm Hybrid (H473)

Designer: Art Metz/Walt Ainsworth

ICE Contact: Walt Ainsworth


HOLDOFF INPUT
HOLDOFF SCHMITT
AUTO TRIGGER ESCAPE LOGIC
TRIGGER LATCH
ARM LATCH
2ND DELAY GATE
1ST DELAY GATE
INPUT AMPLIFIER & SLOPE SELECT
GATE OUTPUT
BIAS (NOT USED)
SLOPE SELECT
+SLOPE ≤ 0.8V
-SLOPE ≥ 2.0V
FREE RUN INPUT
FREE RUN ≥ 3.95V
TRIGGERED ≤ 3.55V
HYSTERISIS ADJUST *
+ TRIGGER INPUT
+ LOAD
- TRIGGER INPUT
- LOAD
HOLDOFF
≥ 3.95V
≤ 3.55V
TRIGGER ENABLE
SUBSTRATE
VEE -5V
GND
NOTES:-
1. DENOTES DEEP COLLECTOR CROSS UNDER RESISTOR.
2. DENOTES B50 CROSS UNDER RESISTOR.
3. DENOTES ISOLATED RESISTOR.
4. * USED ONLY TO ADJUST HYSTERISIS TO A VALUE OTHER THAN THE NOMINAL 25mV. (E.G. HF SYNC)
ENGR
DWN BY R. Hawkins
CHK BY C. WESTON
TYPE
1-26-77
23 DEC 76
6-14-77
PROCESS SHF III
PACKAGE 12.2x12.2mm HYBRID
DIE SIZE 67 x 59 mils
FAST TRIGGER
M122B
INTEGRATED CIRCUIT ENG/MFG
TEKTRONIX, INC.
BEAVERTON, OREGON, U.S.A.
PART NO. 203-0122-90

IN Production
By CER

M131A 155-0121-00 TRIGGER SUB-SYSTEM

Description:

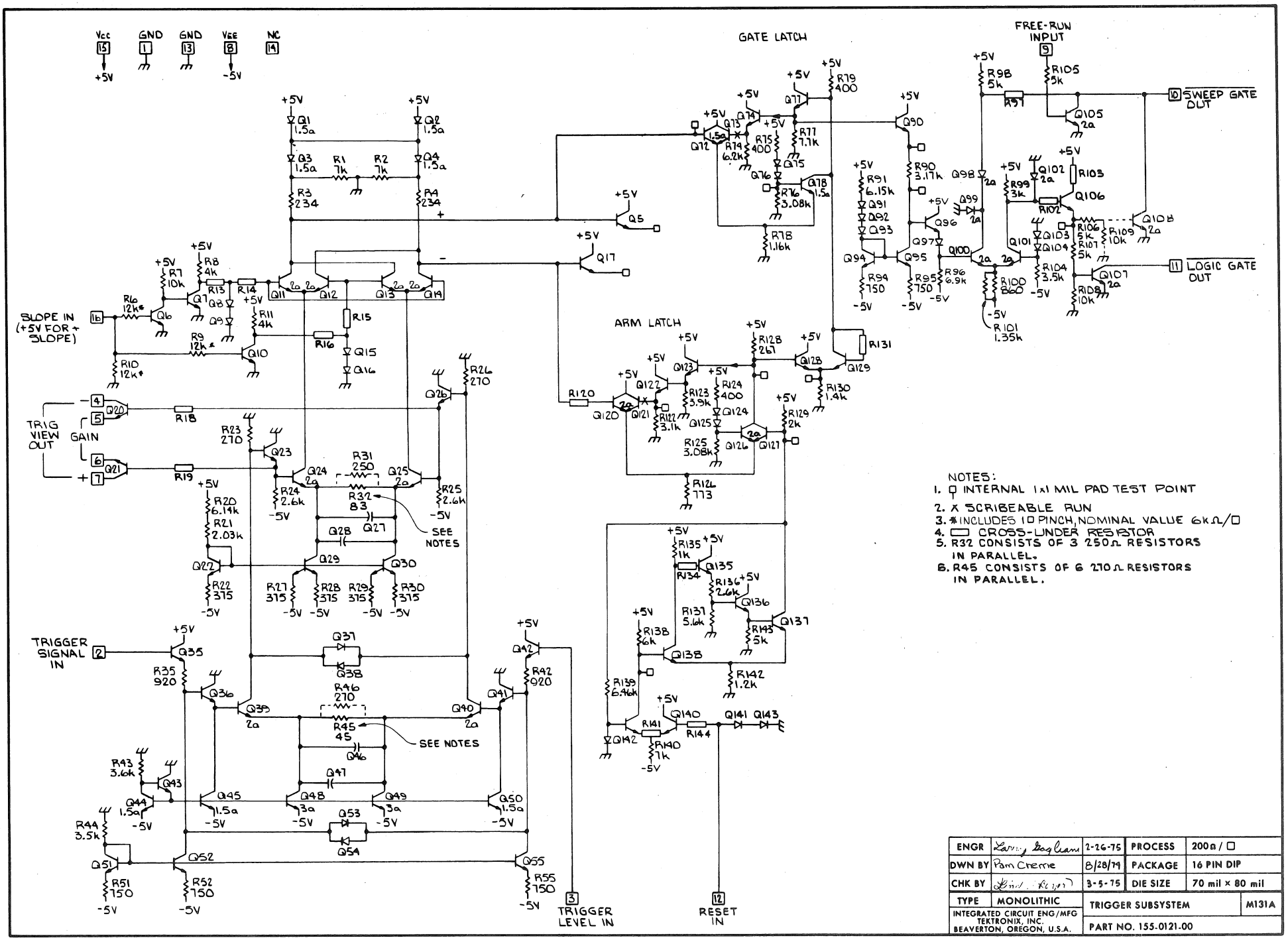
This trigger circuit is intended for use up to 50 MHz. It contains a triggering circuit, a trigger signal preamp, and a trigger view amplifier. The trigger signal input and level input are designed for ! 0.5 V signals referenced to ground. The M131A is designed to interface with the M132A sweep control and M133A sweep and delay pickoff ICs to form a complete horizontal system. Operating voltages for the M131A are ! 5V at a power dissipation of approximately 310 mW.

Package: 16 Pin DIP

Designer: Larry Gagliani

ICE Contact: Walt Ainsworth

Instrument Usage: 455 (2)


Vcc 15 +5V
GND 1
GND 13
VEE 8 -5V
NC 14
GATE LATCH
FREE-RUN INPUT 9
10 SWEEP GATE OUT
11 LOGIC GATE OUT
SLOPE IN (+5V FOR + SLOPE) 16
TRIG VIEW OUT
GAIN
ARM LATCH
TRIGGER SIGNAL IN 2
3 TRIGGER LEVEL IN
12 RESET IN
SEE NOTES
NOTES:
1. ⊡ INTERNAL 1x1 MIL PAD TEST POINT
2. X SCRIBEABLE RUN
3. * INCLUDES 1 □ PINCH, NOMINAL VALUE 6kΩ/□
4. ▭ CROSS-UNDER RESISTOR
5. R32 CONSISTS OF 3 250Ω RESISTORS IN PARALLEL.
6. R45 CONSISTS OF 6 270Ω RESISTORS IN PARALLEL.
ENGR
DWN BY Pam Crerie 8/28/74
CHK BY 3-5-75
TYPE MONOLITHIC
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.
2-26-75
PROCESS 200Ω / □
PACKAGE 16 PIN DIP
DIE SIZE 70 mil × 80 mil
TRIGGER SUBSYSTEM
M131A
PART NO. 155-0121-00

IN Production
by CER

M132A 155-0122-00 SWEEP CONTROL

Description:

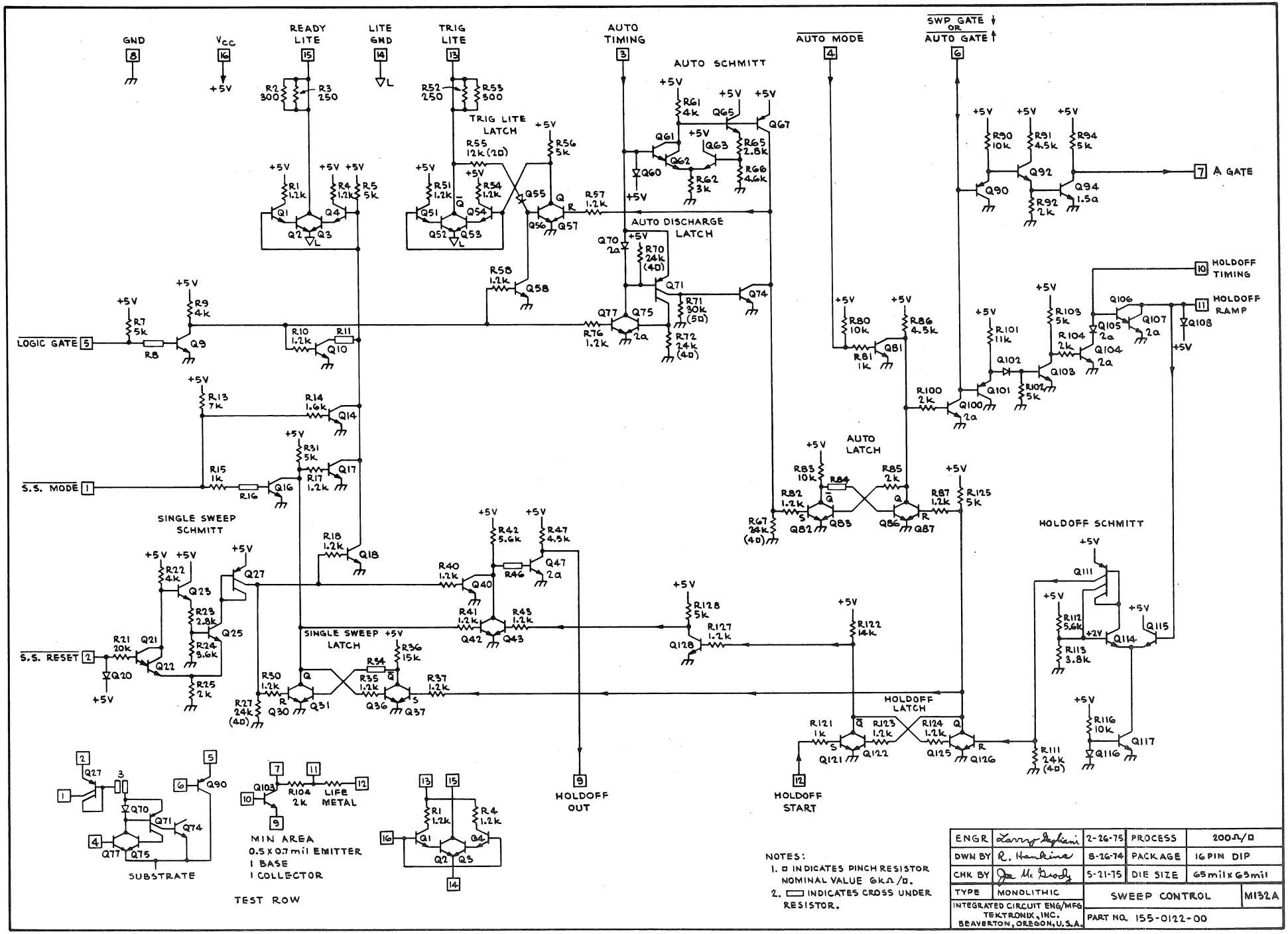
This sweep control circuit contains the hold-off timing Miller, single sweep lockout circuit, triggered and single sweep ready light lamp drivers, single sweep reset debounce circuit, auto timing circuit and an A Gate output. The M132A is designed to operate with the M133A sweep and delay pickoff and the M131A trigger. The M132A operates from + 5 V at a power dissipation of approximately 125 mW.

Package: 16 pin DIP

Designer: Larry Gagliani

ICE Contact: Mike Metcalf

Instrument Usage: 455 (1)


GND
Vcc
READY LITE
LITE GND
TRIG LITE
AUTO TIMING
AUTO MODE
SWP GATE
OR
AUTO GATE
AUTO SCHMITT
TRIG LITE LATCH
AUTO DISCHARGE LATCH
A GATE
HOLDOFF TIMING
HOLDOFF RAMP
LOGIC GATE
S.S. MODE
SINGLE SWEEP SCHMITT
AUTO LATCH
HOLDOFF SCHMITT
S.S. RESET
SINGLE SWEEP LATCH
HOLDOFF LATCH
HOLDOFF OUT
HOLDOFF START
SUBSTRATE
MIN AREA
0.5 x 0.7 mil EMITTER
1 BASE
1 COLLECTOR
TEST ROW
R104 2k
LIFE METAL
NOTES:
1. ▫ INDICATES PINCH RESISTOR NOMINAL VALUE 6kΩ/▫.
2. ▭ INDICATES CROSS UNDER RESISTOR.
ENGR
DWN BY
CHK BY
TYPE
MONOLITHIC
INTEGRATED CIRCUIT ENG/MFG
TEKTRONIX, INC.
BEAVERTON, OREGON, U.S.A.
2-26-75
8-26-74
5-21-75
PROCESS
200Ω/▫
PACKAGE
16 PIN DIP
DIE SIZE
65mil x 65mil
SWEEP CONTROL
M132A
PART NO. 155-0122-00

IN Production

by CER

M133A 155-0123-00 SWEEP & PICKOFF

Description:

The 155-0123-00 contains a control circuit and current source for an external Miller, sweep end circuit, sweep switch, Z axis control, and a delay pickoff.

It is used with the 155-0122-00 sweep control IC, and the 155-0124-00 horizontal pre-amp IC.

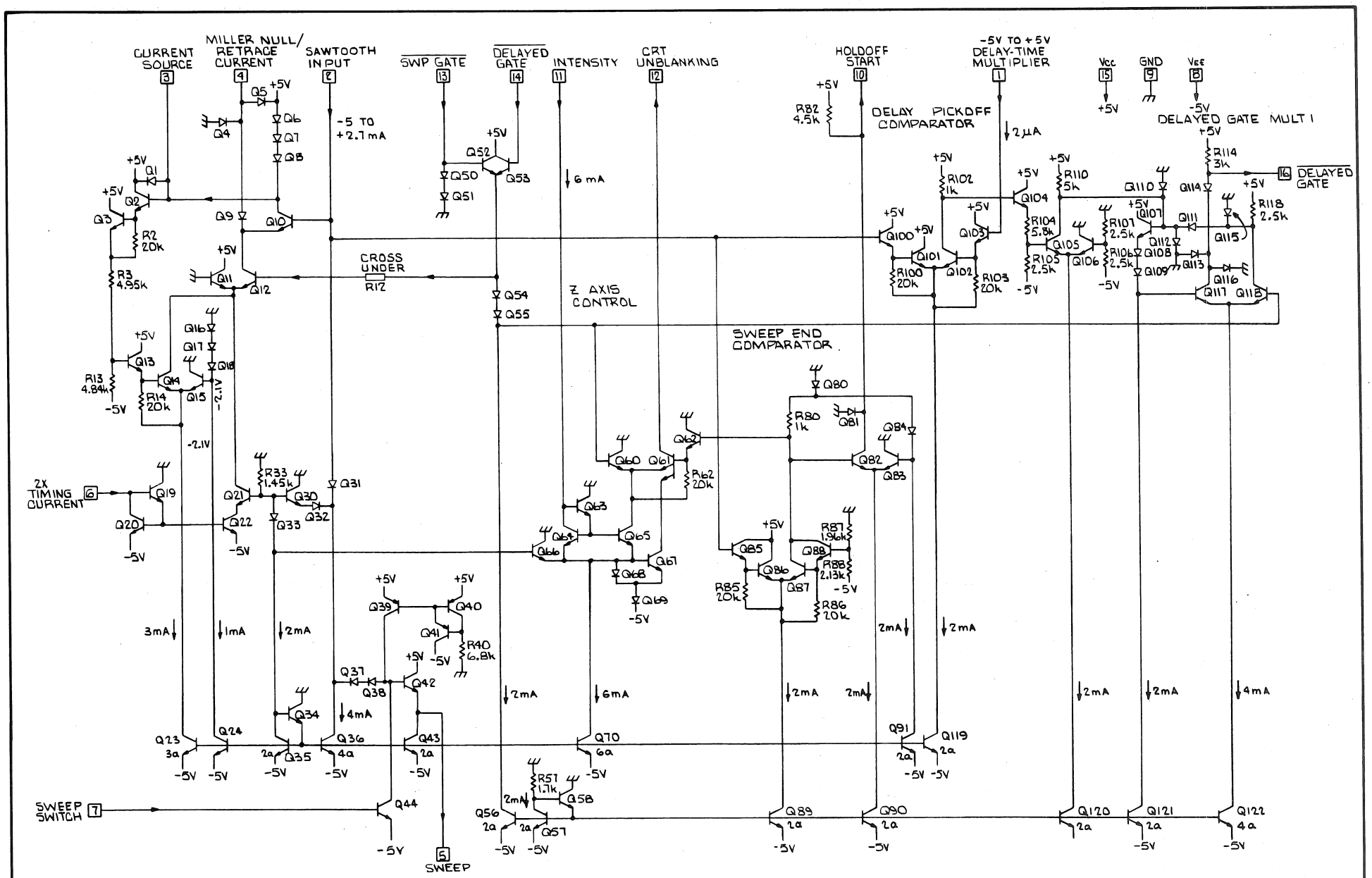
Power Supply: ± 5 volts, 330 mW.

Package: 16 pin

Designer: Jim Godwin/Mike Metcalf

ICE Contact: Mike Metcalf

Instrument Usage: 455 (1)



ENGR	Jim Sohwin	4-28-75	PROCESS	200Ω / □
DWN BY	Pam Cherne	9-10-74	PACKAGE	16 PIN DIP
CHK BY	Jack Brock	5-20-75	DIE SIZE	60 mil × 60 mil
TYPE	MONOLITHIC	SWEEP & PICKOFF		M133A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0123-00		

IN Engineering

M136 155-0160-00 TRIGGER SOURCE SELECTOR AND AMPLIFIER

Description:

The M136 provides for selection of one of three trigger sources. There are two high frequency channels and one low frequency channel. Channel selection is accomplished by switching a current source (resistor to -15V) to the appropriate select pin. Input voltages are at zero volts. External load resistors are required. When the load resistors are 50 ohms, gain and bandwidth are nominally six and 1500 MHz respectively.

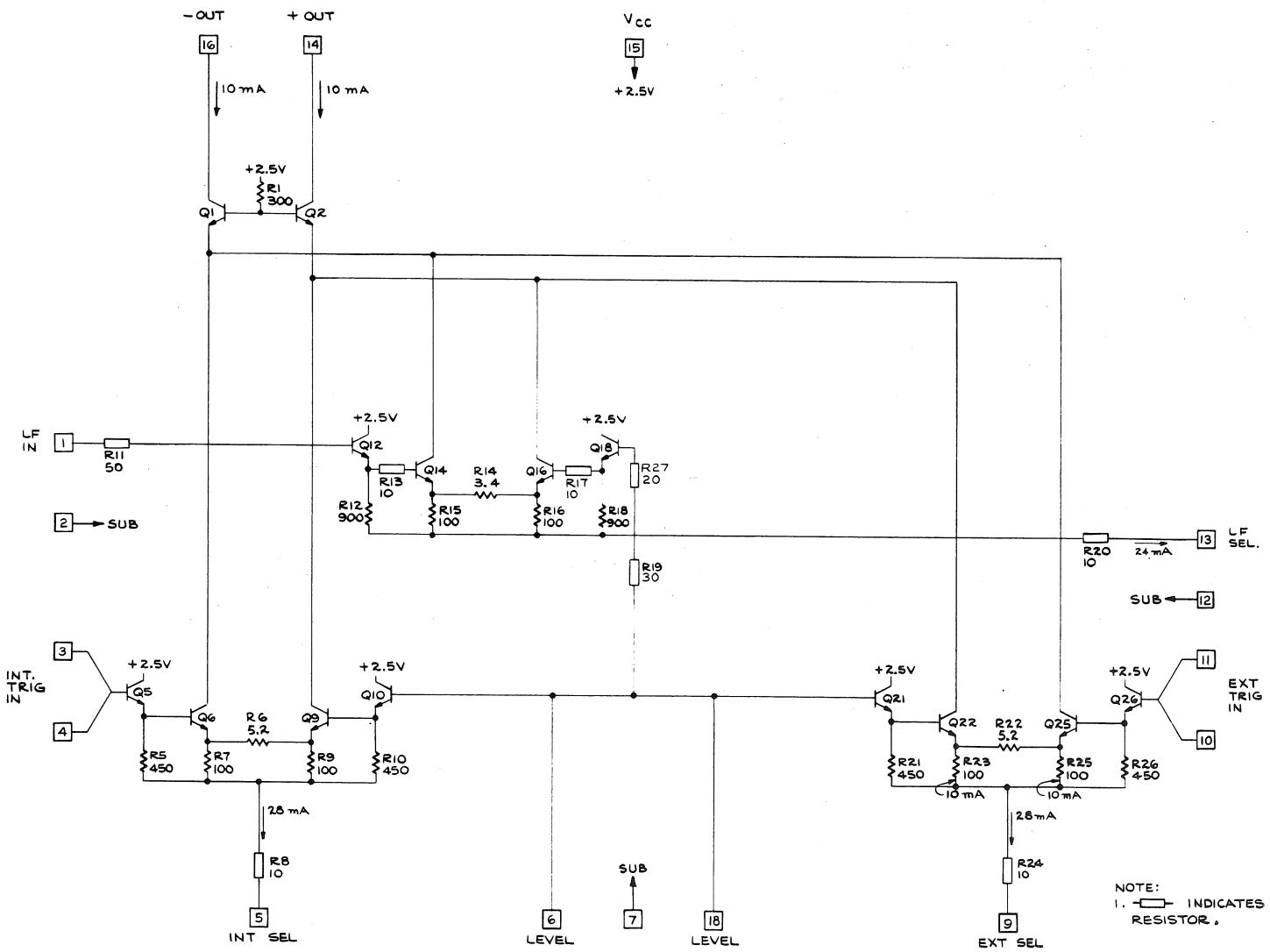
Power Supply: +2.5V, resistor from -15V to source select (one of three).

Package: 16 PIN MINIPAC

Designer: Art Metz

ICE Contact: Walt Ainsworth

Instrument Usage: 7B10/7B15, 067-0821-00



NOTE:
1. —▭— INDICATES CROSSUNDER RESISTOR.

ENGR	Walt Ainsworth	12-9-76	PROCESS	SHF III
DWN BY	S. POLENDEY	9-9-76	PACKAGE	16 PIN MINIPAC
CHK BY	C. WESTON	3-17-77	DIE SIZE	48mil. X 48mil.
TYPE	MONOLITHIC	TRIGGER AMPLIFIER & CHANNEL SWITCH		M136C
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0160-00		

IN Production

M138 155-0124-00 HORIZONTAL PREAMPLFIIER

Description:

Used in the 455 portable oscilloscope with a maximum sweep rate of 5 ns/div. It is fabricated with the standard 200 Ω/sq process.

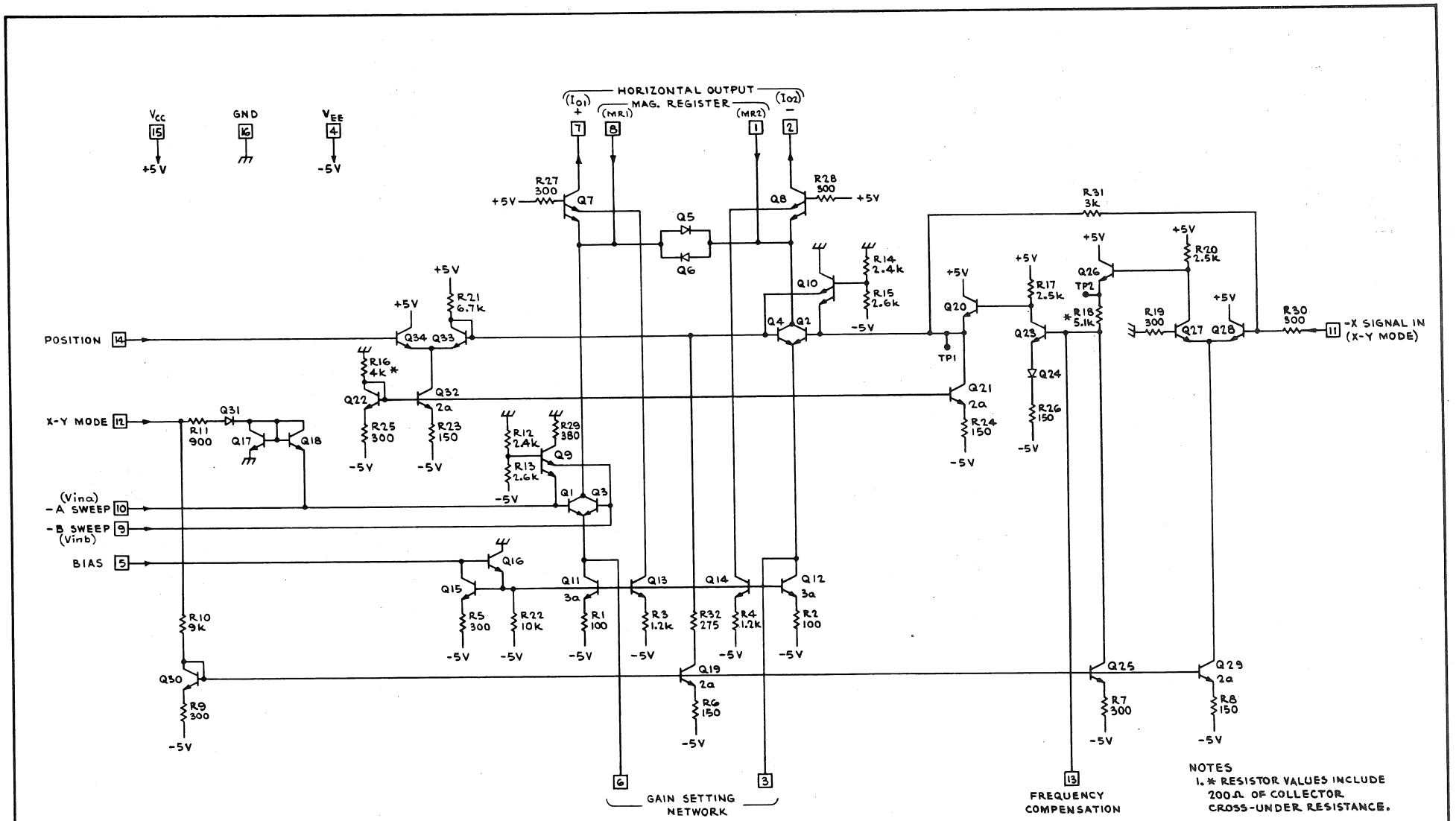
A and B sweep input range is + 2.0 V to - 2.4 V with channel switching accomplished by pulling 2 mA out of the unused input(s). In X-Y operation (selected by pulling mode control to + 5 V), the X signal sees a 5 MHz preamplifier with gain 10 and input range of about ! 200 mV. Output is a differential current from common base transistors with a sensitivity of 0.2 mA/div/side. Gain is adjusted and switched externally by selecting emitter resistors for the input differential pair. The M138 has provisions for mag registration and horizontal position inputs. Bias current level is set with an external resistor. Nominal operation is ! 5.0 V supplies with power dissipation of 185 mW (215 mW in X-Y mode).

Package: 16 Pin DIP

Designer Bob Nordstrom

ICE Contact: Bob Nordstrom

Instrument Usage: 455 (1)



NOTES
1. * RESISTOR VALUES INCLUDE 200Ω OF COLLECTOR CROSS-UNDER RESISTANCE.

ENGR	R. Nobetson	9-19-74	PROCESS	200Ω/□
DWN BY	R. Hankins	9-16-74	PACKAGE	16 PIN DIP
CHK BY	Jas M. Brady	11-12-74	DIE SIZE	55 mil x 55 mil
TYPE	MONOLITHIC	HORIZONTAL PREAMPLIFIER		M138
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0124-00		

IN Engineering

M157

LOW POWER HORIZONTAL OUTPUT AMPLIFIER

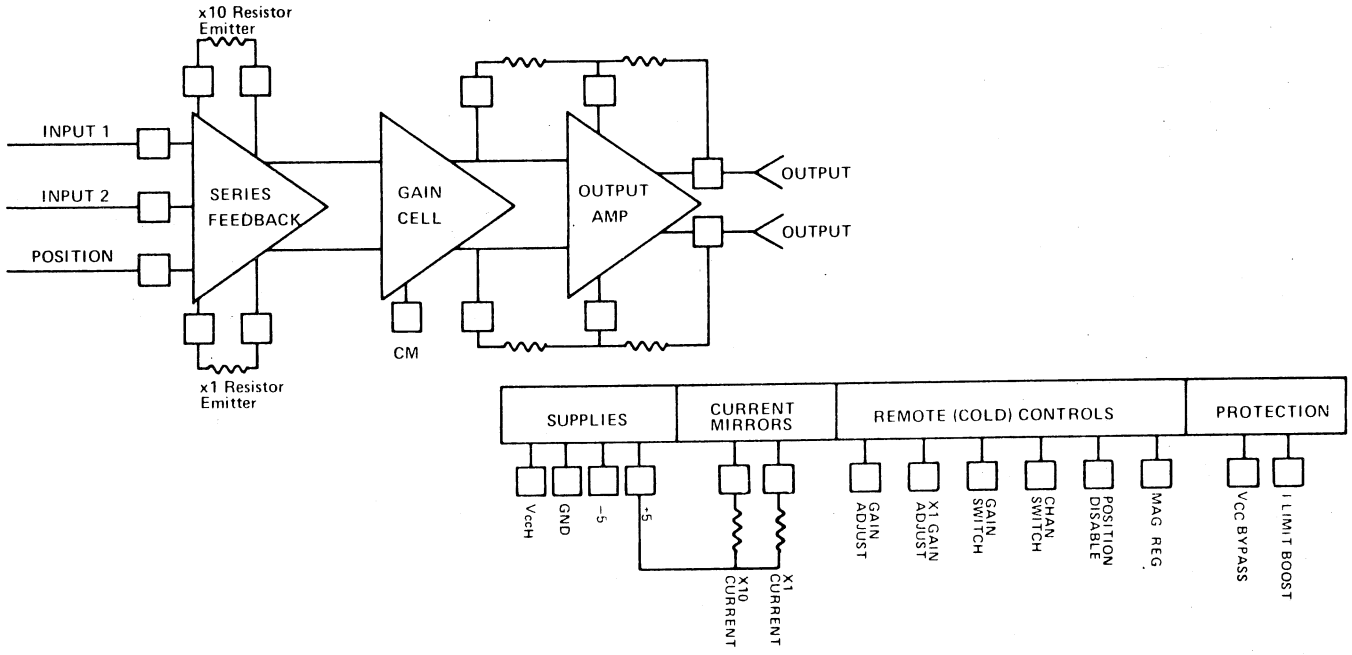
Description:

Low Power Horizontal Output Amplifier, class AB, up to 20 nsec/div sweep rate, up to 90 volts swing per side (± 90 volts differential). Remote switching and control (ground closure or DC voltage) of the following functions:

1) Channel switching
2) Gain switching X10 X1
3) Gain adjust X1
4) Gain adjust
5) Position control disable

Short circuit protection, output limiting (anti-saturation), and average output level regulation are all on chip.

M 157 (Horizontal)



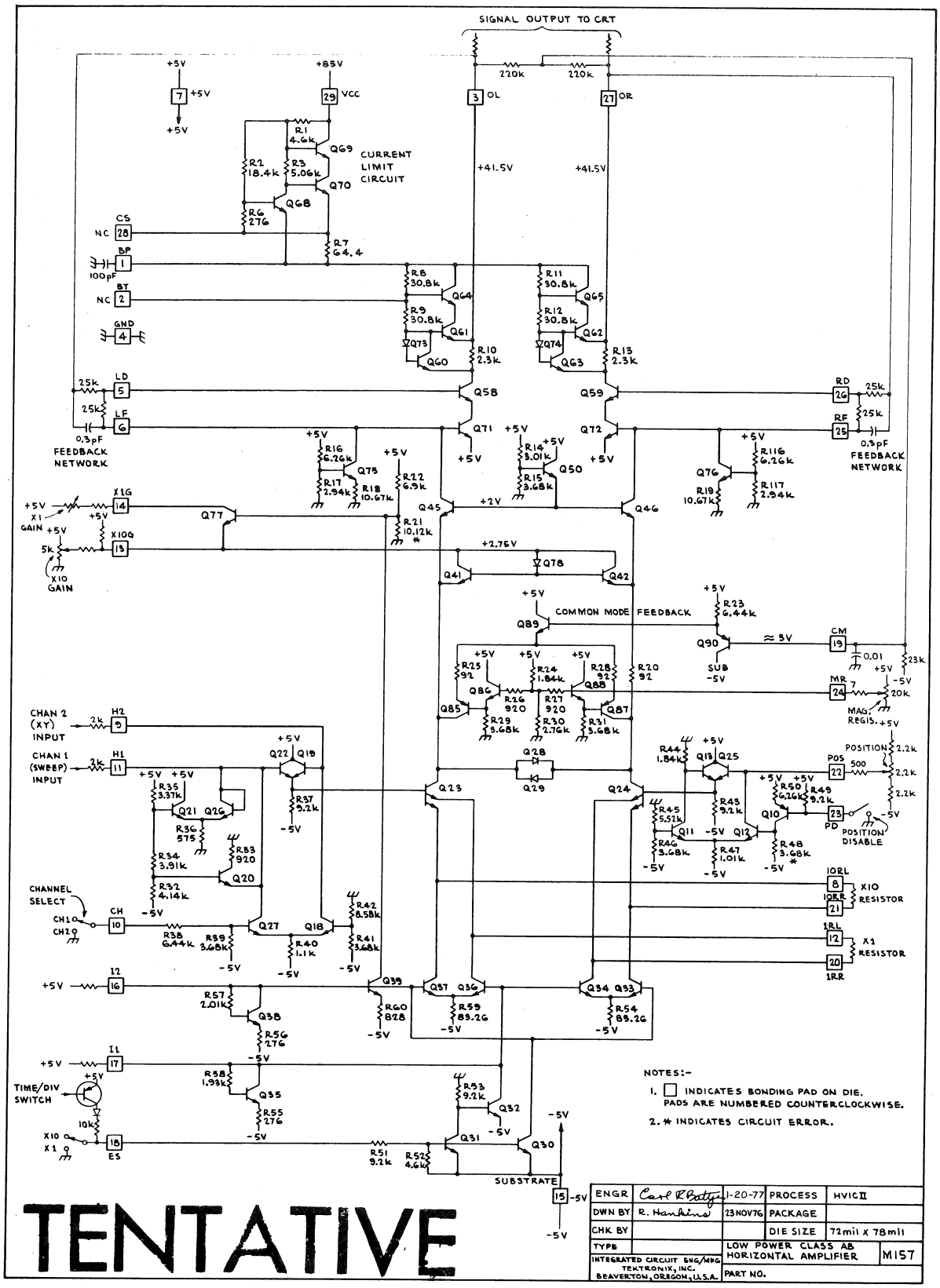
Power Supply: ±5 and V_{CC} up to 110 volts

Package: 28 lead ceramic or hybrid

Designer: Carl Battjes

ICE Contact: Carl Battjes

Instrument Usage: Pending


SIGNAL OUTPUT TO CRT
CURRENT LIMIT CIRCUIT
FEEDBACK NETWORK
COMMON MODE FEEDBACK
CHAN 2 (XY) INPUT
CHAN 1 (SWEEP) INPUT
CHANNEL SELECT
TIME/DIV SWITCH
X1 GAIN
X10 GAIN
POSITION
POSITION DISABLE
MAG. REGIS.
X10 RESISTOR
X1 RESISTOR
SUBSTRATE
NOTES:-
1. ☐ INDICATES BONDING PAD ON DIE. PADS ARE NUMBERED COUNTERCLOCKWISE.
2. * INDICATES CIRCUIT ERROR.
TENTATIVE
ENGR
DWN BY
CHK BY
TYPE
PROCESS
PACKAGE
DIE SIZE
HVICII
72mil X 78mil
LOW POWER CLASS AB HORIZONTAL AMPLIFIER
M157
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.
PART NO.

IN Production
by CER

M159 155-0151-00 TRIGGER GENERATOR

Description:

This IC is intended for use in scopes with up to 100 mHz bandwidth. It employs SHF II processing with ECL circuitry, and requires +5V and -5V power supplies with a power disspation of 310 mW. The package is 20 PIN DIP. Low frequency sensitivity is typically 7.5 mV to 25 MHz and increases by a factor of 3 at 100 MHz. DC trigger input levels are around 0 volts. Features include slope selection, hysteresis adjustment, trigger-level centering, free-run input, trigger-view outputs centered around ground, and an operational amplifier with typical open-loop gain of 500. The gate and gate complement signals are at ECL levels. A Schmitt trigger circuit accepts reset signals with slow transistions.

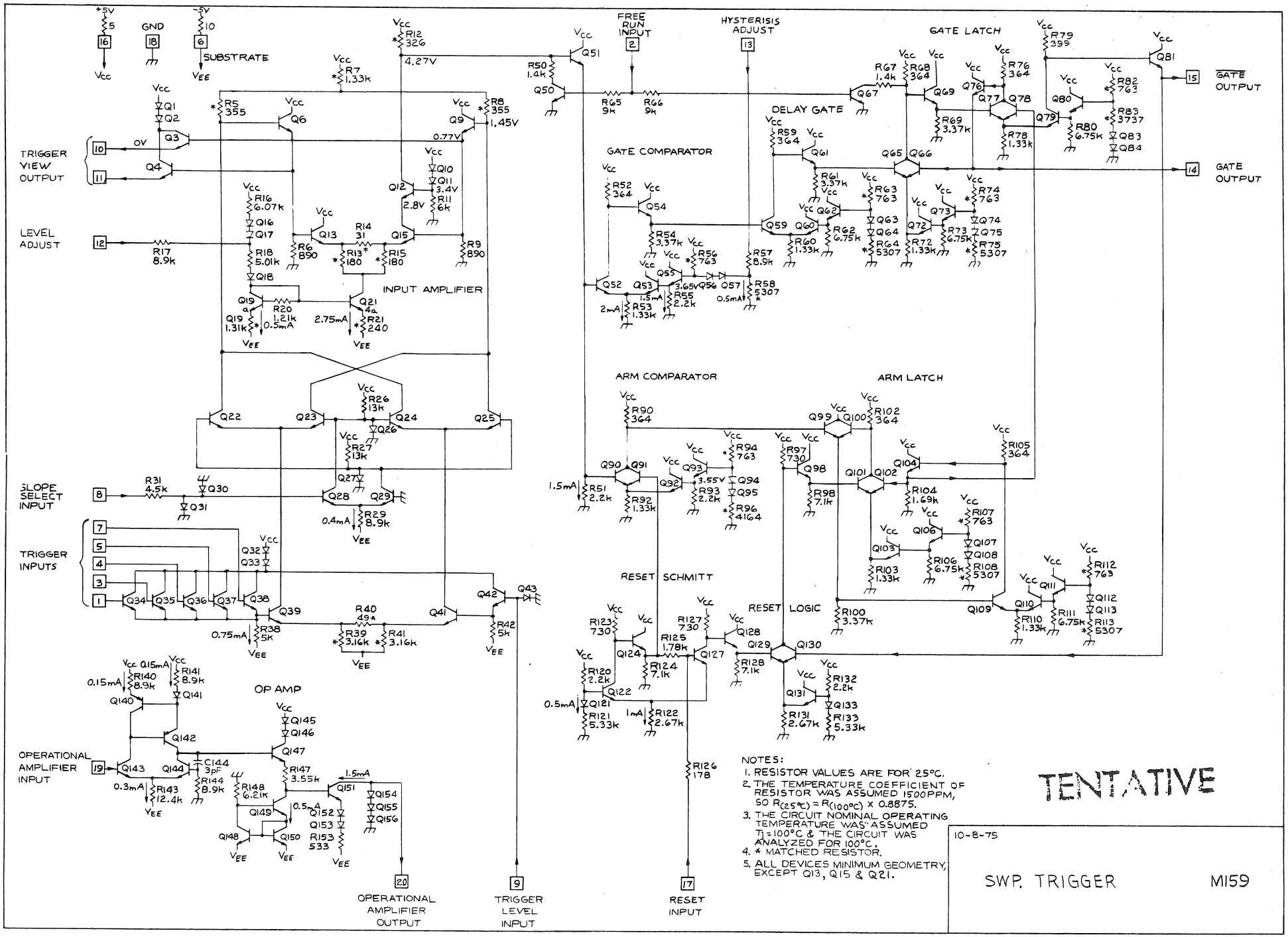
Power Supply: V_{CC} +5V
V_{EE} -5V

Package: 20 PIN DIP (Kovar-cuper-Kovar)

Designer: Gerald McMorrow

ICE Contact: Dick Hung

Instrument Usage: 465M



NOTES:
1. RESISTOR VALUES ARE FOR 25°C.
2. THE TEMPERATURE COEFFICIENT OF RESISTOR WAS ASSUMED 1500PPM, SO $R_{(25°C)} = R_{(100°C)} \times 0.8875$.
3. THE CIRCUIT NOMINAL OPERATING TEMPERATURE WAS ASSUMED $T_j = 100°C$ & THE CIRCUIT WAS ANALYZED FOR 100°C.
4. * MATCHED RESISTOR.
5. ALL DEVICES MINIMUM GEOMETRY, EXCEPT Q13, Q15 & Q21.

TENTATIVE

10-8-75

SWP. TRIGGER M159

IN Engineering

M174 TRIGGER AND SWEEP

Description:

The M174 was designed to be used in low frequency instruments. The circuit employs standard 200 ohm per square processing. Trigger input sensitivity (Hysteresis) at DC is 20 mV. Stable triggering beyond 25 MHz is attainable. The sweep (a Miller Integrator) is a 3 volt positive going ramp centered about zero volts. Auto trigger (bright baseline) timing, hold-off timing, and single sweep circuitry are included.

Power Supply: V_{CC} + 5.0V
V_{EE} - 5.0V

Package: 20 pin DIP (Kovar-Copper-Kovar)

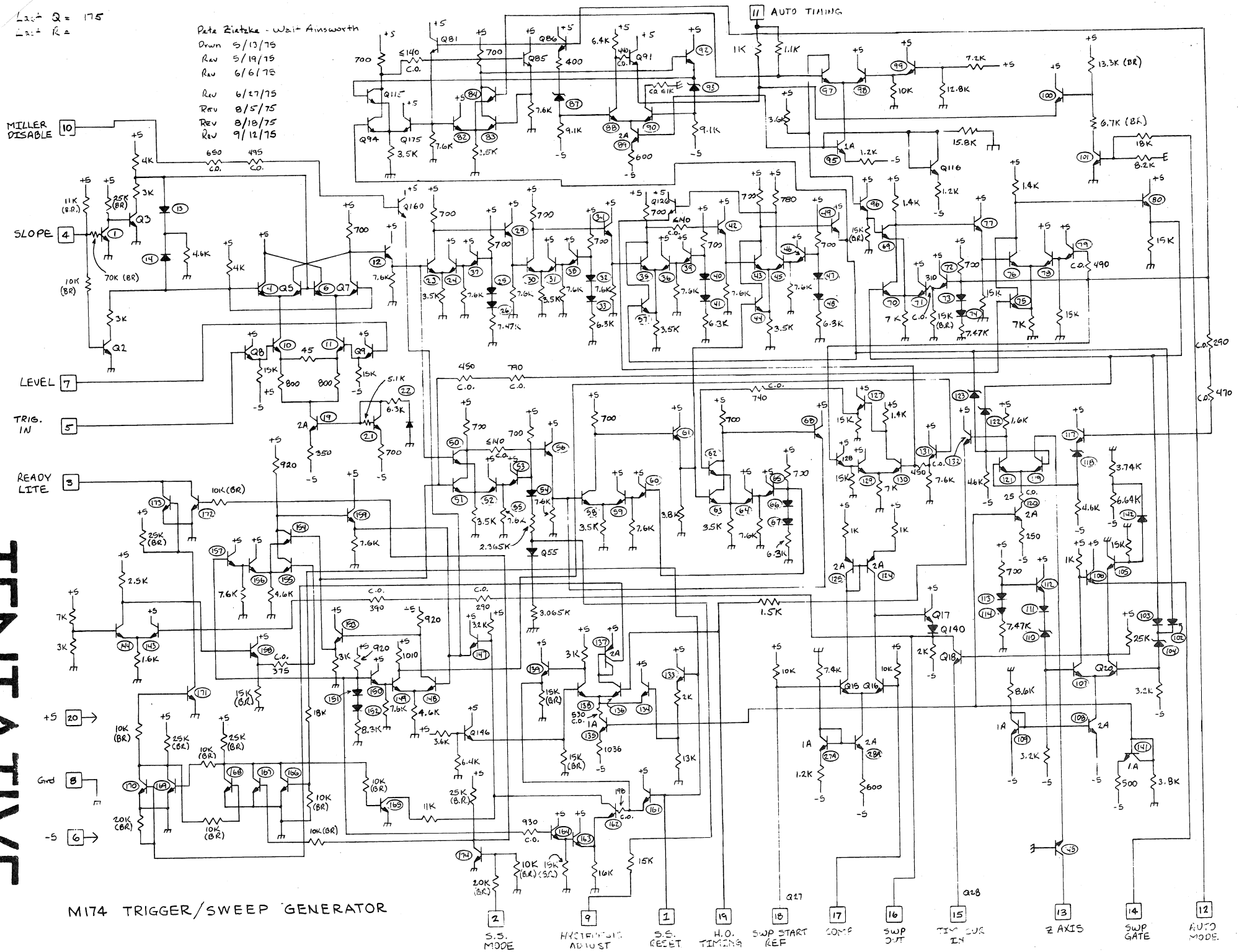
Designer: Pete Zietzke/Walt Ainsworth

ICE Contact: Walt Ainsworth

Instrument Usage: None

Last Q = 175
Last R =

Pete Zietzke - Walt Ainsworth
Drwn 5/13/75
Rev 5/19/75
Rev 6/6/75
Rev 6/27/75
Rev 8/5/75
Rev 8/18/75
Rev 9/12/75



TENTATIVE

M174 TRIGGER/SWEEP GENERATOR

VI. 15.

VII. A/D AND D/A CIRCUITS

In Production
by CER

MO45D | 155-0038-01
155-0038-02 | D/A CONVERTER

Description:

The MO45 is a 5-bit precision current source digital to analog converter. The current ratios are set by external resistors. The range of the MSB is 5 mA to 30 mA. Two packages may be used together for a 10-bit D/A with ± 1/2 LSB accuracy.

The output is designed to sum into OV a negative reference current.

Power Supply: V_{CC} + 5V
V_{EE} -5 to -15V

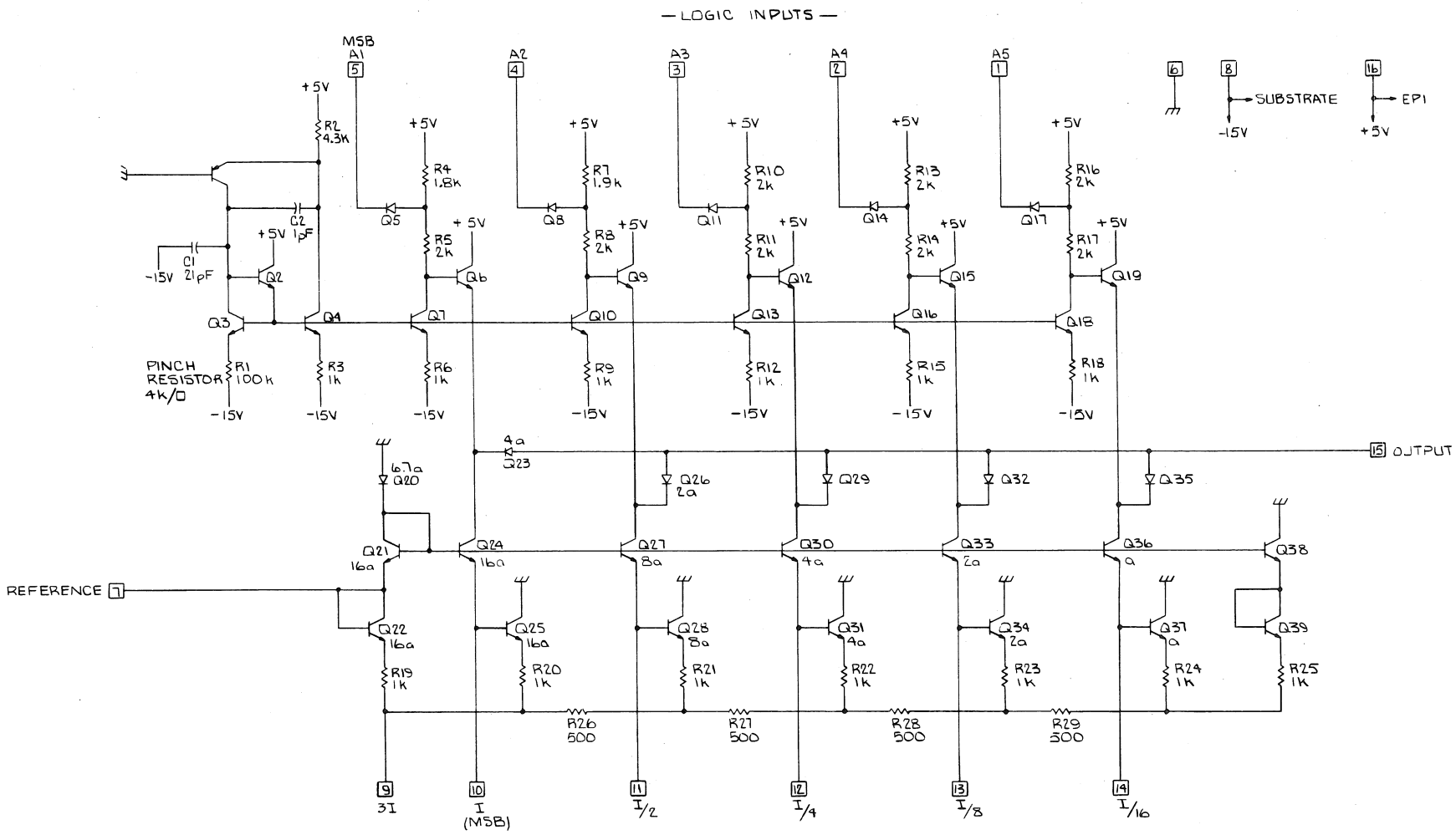
Package: 16 DIP

Designer: Mike Metcalf

ICE Contact: Mike Metcalf

Instrument Usage:

7D13	(1)	P7001950C	(2)
7D14	(1)	P7701953Q	(2)
7M13	(4)	P7001	(2)
7S12	(1)	S6	(1)
1461	(2)		



ENGR	M H Whitaker	11-13-74	PROCESS	200Ω/□
DWN BY	Pam Cherrie	11-1-74	PACKAGE	16 PIN DIP
CHK BY	Jim McCrady	11-25-74	DIE SIZE	50 mil × 50 mil
TYPE	MONOLITHIC	D-A CONVERTER		MO45D
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX,INC. BEAVERTON,OREGON,U.S.A.		PART NO. 155-0038-01/02		

IN Engineering

M155A 203-0155-90 4-BIT FLASH A/D CONVERTER

Description:

The M155A is a 17 level digitizer (4-bits plus over-range), and is designed specifically for use in parallel-serial A/D converter systems. It consists of 16 comparator cells, digital encoding circuitry, and output drivers as shown in the block diagram of Fig. 1. A summary of important characteristics may be found in Fig. 2 and a complete schematic in Fig. 3.

The comparators have a common input Vin and separate, monotonically increasing, reference voltages which may be derived from an external resistor string (hybrid H508). A strobe command forces each comparator (simultaneously) to make a binary decision. Further changes in input are locked out so that the circuit functions as a digital sample-and-hold. This is done by steering a current source from the input differential pair to a cross-coupled latching pair.

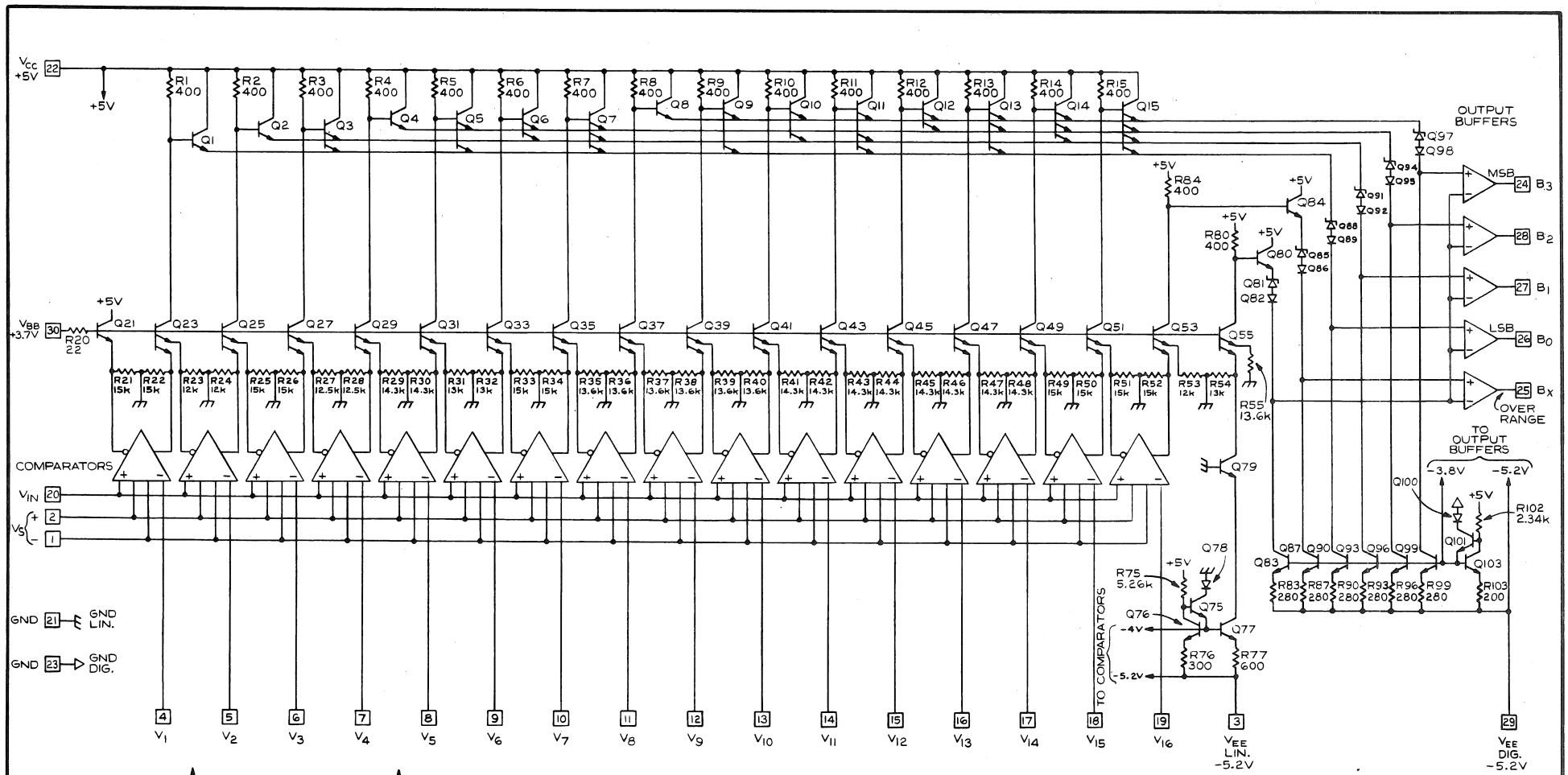
Sixteen common base transistors encode the comparator output to a one-of-sixteen code which is translated to binary by 16 multiple-emitter common collector transistors. The digital data is then level shifted to the output drivers and is valid at the output within 5 ns of strobing.

The inclusion of the sixteenth comparator (over-range) makes it possible to directly combine 2 M155A's for a 5-bit parallel A/D converter.

Differential Non-Linearity:	± 0.2% (good for 8-bits)
Input Range:	± 1.5V or 0 to 3V
Power Supplies:	+ 5.0, - 5.2

M155A (continued)

Power Dissipation:	850 mW
Output:	ECL (binary)
Maximum Clock Rate:	80 MHz
Input Bandwidth:	5 MHz
Package:	H508 hybrid in TEKFORM 35000 (square metal can)
Process:	SHF 2, double-layer metal
Designer:	Bob Nordstrom
ICE Contact:	Bob Nordstrom



ENGR	R. Norton	12-9-76	PROCESS	SHF II
DWN BY	J. Langley	10-27-76	PACKAGE	HYBRID
CHK BY	Jan Forsberg	3-7-77	DIE SIZE	75mil X 132mil
TYPE	MONOLITHIC	4-BIT FLASH A/D CONVERTER		M155A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 203-0155-90		

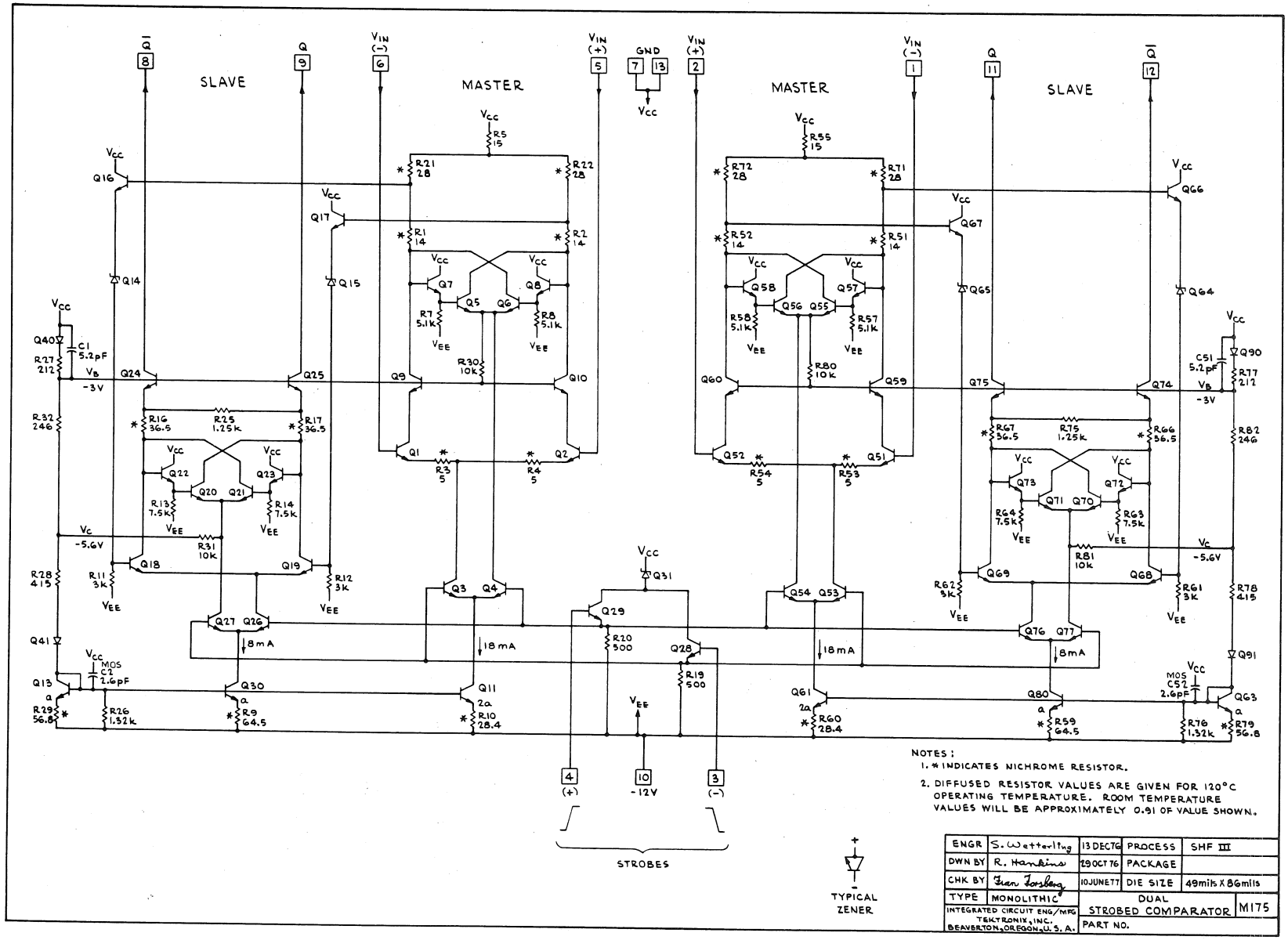
IN Engineering

M175 155-0170-00 DUAL STROBED COMPARATOR

Description:

Each M175 integrated circuit contains two complete strobed voltage comparators. A strobed comparator is different from the more familiar continous-duty comparator in that comparison decisions are made only on the strobe edge. This is a high performance component for clock-driven A/D converters, logic analyzer inputs and digital test systems.

Internally each comparator is arranged in a master-slave configuration which holds the output data valid for a complete clock cycle. (See Block Diagram). Output is a fixed current steered through either collector of a pair of common base NPN transistors. The output current will give sufficient voltage at the remote end of properly terminated transmission lines to accurately drive ECL or TTL differential line receivers. Strobe inputs are level shifted and attenuated differential ECL signals. Only a few hundred millivolts of strobe input are needed to operate the comparators. Though full ECL swings can be used, this unnecessarily brings large signal transients onto the die. For the strobe low input, the Master stage functions as a wide-band differential cascode amplifier. The Slave stage now performs as an amplifier in transmitting the decision state of the Master to the outputs. On return to strobe low input, the Slave stage latches and holds these outputs until the next time that the strobe input goes high. Intended voltage supplies are 0.0v and -12.0v. Intended voltage inputs are -6.38v $\pm$ 0.125v. Voltage supply and input levels can be shifted together as needed for other applications. In doing so, the user must take care that the strobe inputs and current outputs will function correctly. Wider input voltage swings are allowed within the positive



NOTES:

1. * INDICATES NICHROME RESISTOR.
2. DIFFUSED RESISTOR VALUES ARE GIVEN FOR 120°C OPERATING TEMPERATURE. ROOM TEMPERATURE VALUES WILL BE APPROXIMATELY 0.91 OF VALUE SHOWN.

ENGR	S. Wetterling	13 DEC 76	PROCESS	SHF III
DWN BY	R. Hankins	29 OCT 76	PACKAGE	
CHK BY	Fran Forsberg	10 JUNE 77	DIE SIZE	49 mils X 86 mils
TYPE	MONOLITHIC	DUAL STROBED COMPARATOR		M175
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO.		

M175

Description (continued)

limit of the cascode bias voltage and the negative limit of the current source and switch. Signal distortion and slew rate limiting will occur as usual for a small signal amplifier driven outside its linear region.

Comparison Decision Time	less than 500 ps
Strobe Maximum Repetition Rate (Period)	200 mHz (5 ns)
Input Bandwidth (as an amplifier)	greater than 800 mHz
Input Resolution plus Offset	±5 mV or less
Input Range	±125 mV around -6.38 volts
Output	8 mA through either of two common-base buffer transistors.
Power	12-volt supply 1.2 watts

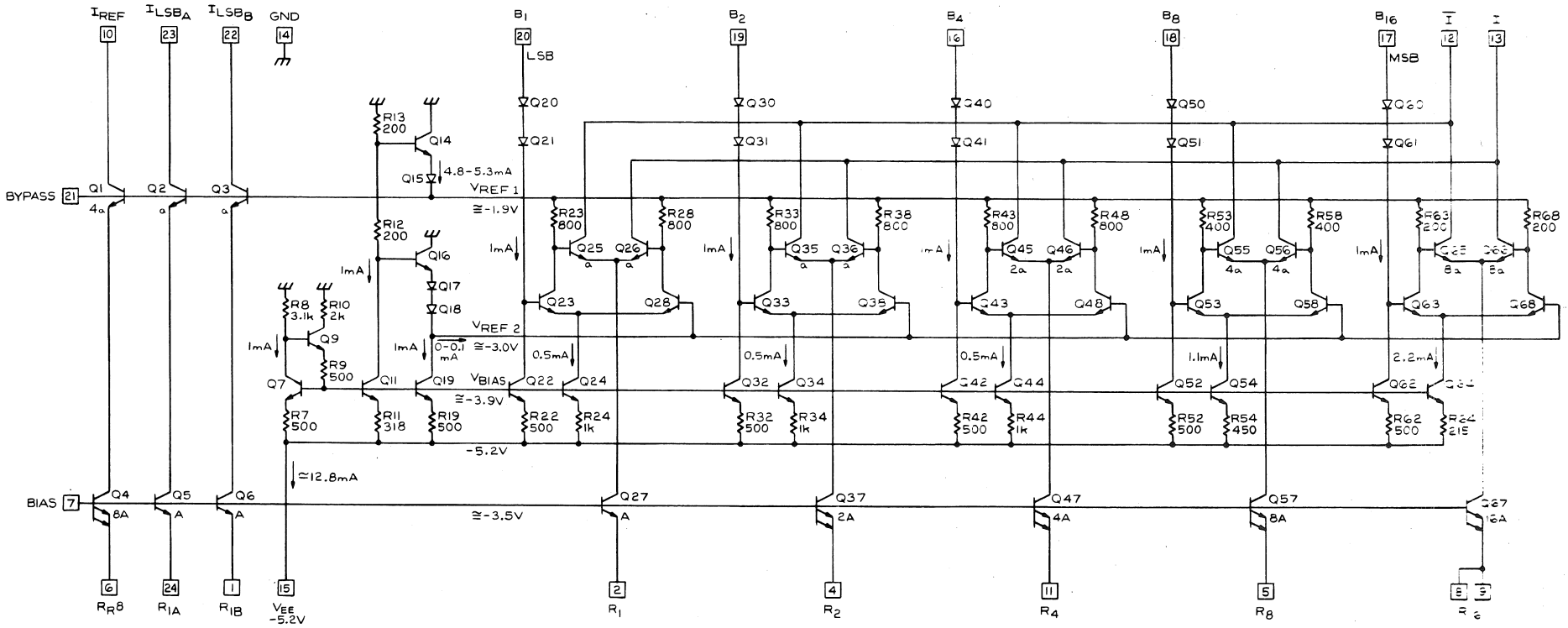
Power Supply: 0, -12v, 100 mA

Package: Subpart for Hybrid

Designer: Steve Wetterling

ICE Contact: Steve Wetterling

Instrument Usage: 7612D



ENGR	A. Taylor R. Nolte	12-9-76	PROCESS	SHF II
DWN BY	J. Langley	11-1-76	PACKAGE	HYBRID
CHK BY	Jan Forsberg	3-4-77	DIE SIZE	83mil X 45mil
TYPE	MONOLITHIC	5-BIT D/A CONVERTER		M177A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 203-[illegible]		

IN Engineering

M177A 203-0177-90 5-BIT ECL D/A CONVERTOR

Description:

M177A is a 5-bit DAC designed for use with the M155A in parallel-serial A/D convertor systems. Five precision binarily-scaled current sources are independently switched to either I or $\overline{I}$ according to the ECL digital input word. I and $\overline{I}$ are supplementary current outputs with a voltage compliance of -1.6v to +3.1v. Switching is done by an emitter-coupled pair driven differentially by an amplifier which converts the single-ended input to a level-shifted differential drive. Two unswitched LSB current sources are provided for a particular application. Settling time to 8-bits with a 240 ohm, 10 pF load is 15 ns.

A reference current equal to 1/2 I (MSB) is set up with an external resistor, voltage reference, and op-amp. I (MSB) is designed to be 12.8 mA. Binarily-weighted emitter resistors are required and are provided by hybrids H710 and H552. Maximum accuracy is achieved by functionally trimming these resistors, dropping several volts across them, and operating the outputs into a fixed voltage.

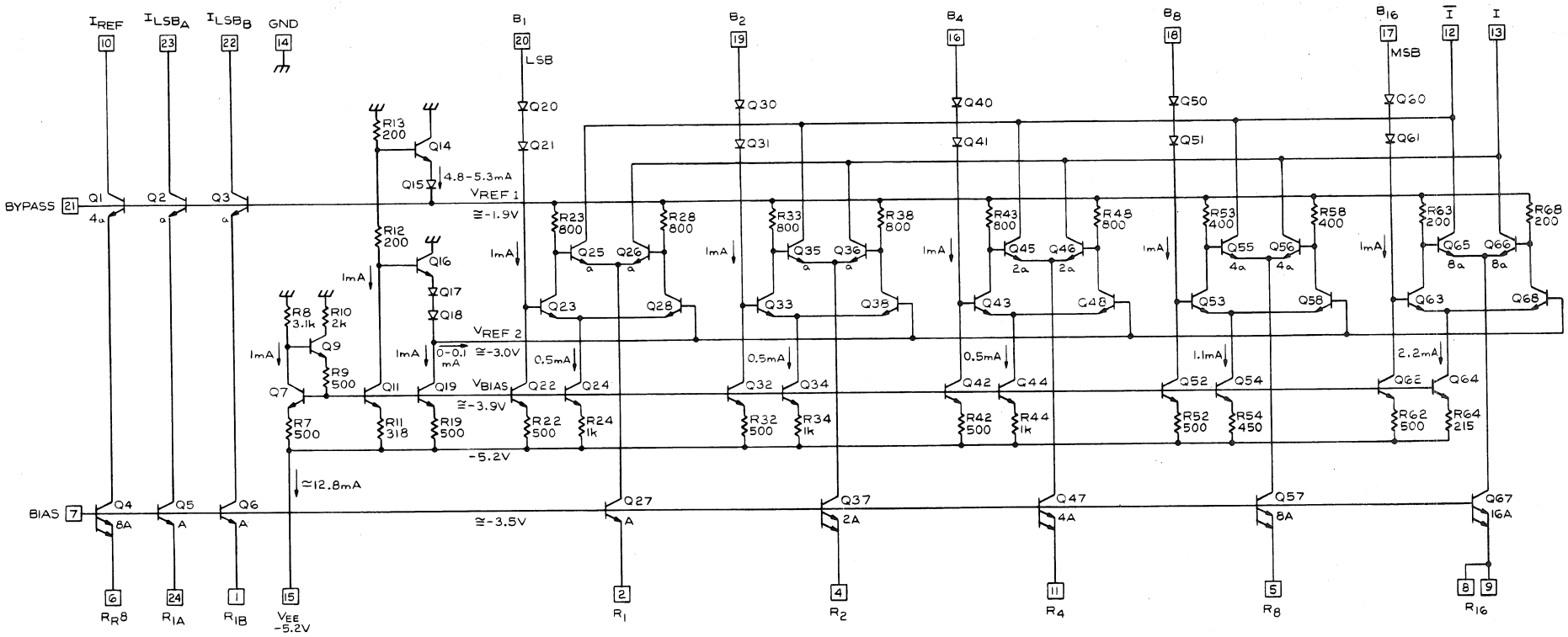
M177A is operated between GND and -5.2v with typical power dissipation of 240 mW depending on usage. It is packaged as the H710 in a 16-pin TO-8 can.

Power Supply: -5.2V

Package: Hybrid

Designer: Stew Taylor/Bob Nordstrom

ICE Contact: Stew Taylor/Bob Nordstrom



ENGR	J. Saylor R. Nagle	12-9-76	PROCESS	SHF II
DWN BY	J. Langley	11-1-76	PACKAGE	HYBRID
CHK BY	Jan Forsberg	3-4-77	DIE SIZE	83mil X 45mil
TYPE	MONOLITHIC	5-BIT D/A CONVERTER		M177A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 203-0177-90		

VIII. VERTICAL AMPLIFIERS

IN Production

M055C 155-0032-00 INPUT AMPLIFIER
155-0032-01

Description:

This circuit is a single channel amplifier designed for the dual channel 7A12.

Pins 1, 2, 15 and 16 are connected to external current sources to provide gain changes.

This package may also be connected differentially using pins 3 and 14.

Current at pin 10 controls the ratio of the current from pin 6 to pins 8 and 9 for output position.

Current at pin 12 controls pin 5 currents to provide gain changes and inverting.

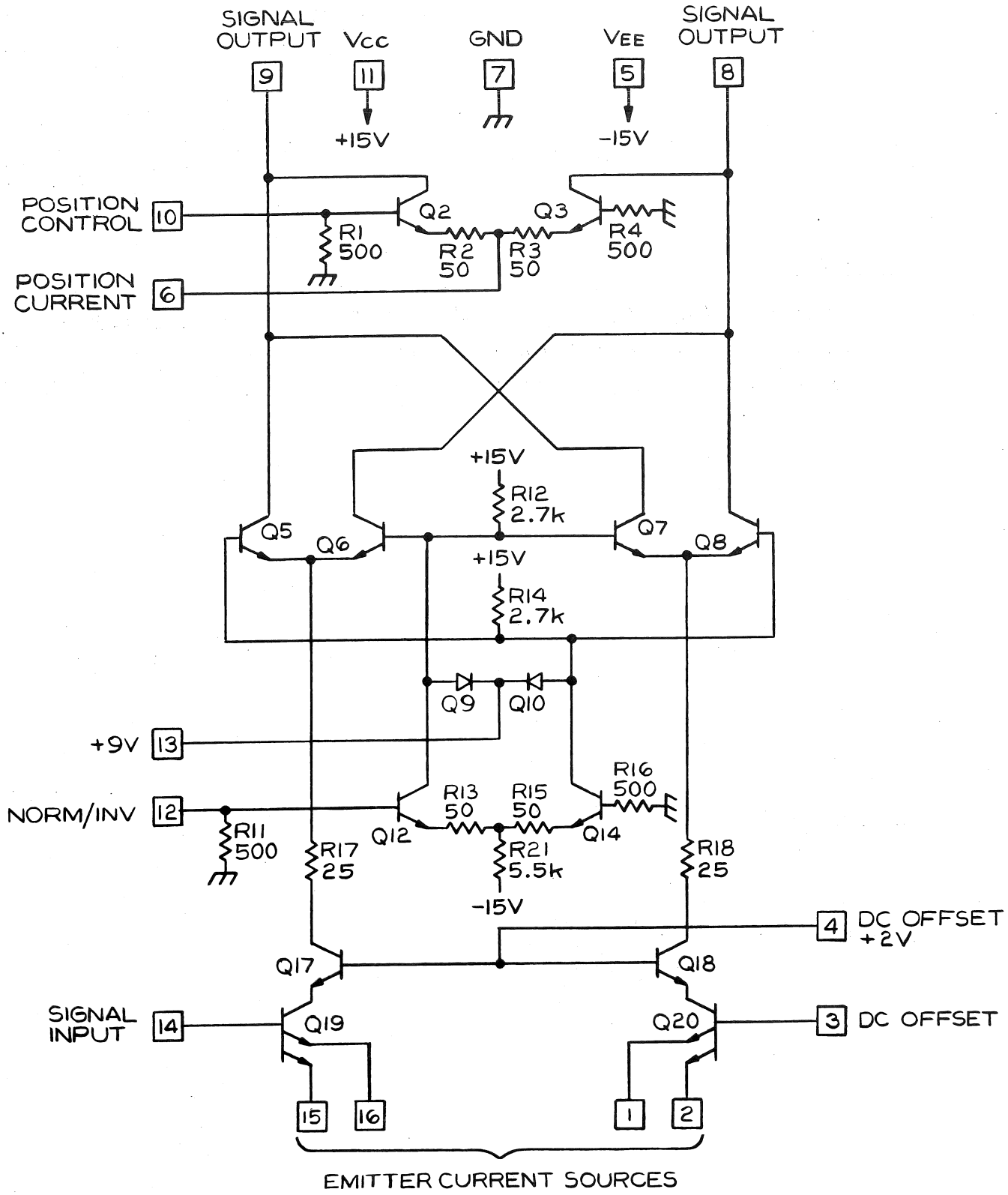
Package: 16 DIP

Designer: Roy Hayes

ICE Contact: Einar Traa

Instrument Usage:

1478 (1)	671 (2)
465 (2)	1460 (2)
475 (2)	670 (2)
464 (2)	466 (2)
1440 (2)	Some 475 Mods (4)
335K (1)	



ENGR	Evan Tree	7-1-76	PROCESS	50-450
DWN BY	J. Langley	6-29-76	PACKAGE	16 PIN DIP
CHK BY	Linda Boyer	7-13-76	DIE SIZE	60mil X 40mil
TYPE	MONOLITHIC	INPUT AMPLIFIER		M055C
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0032-00		

IN Production
by CER

M065 155-0050-01 423 VERTICAL PREAMPLIFIER

Description:

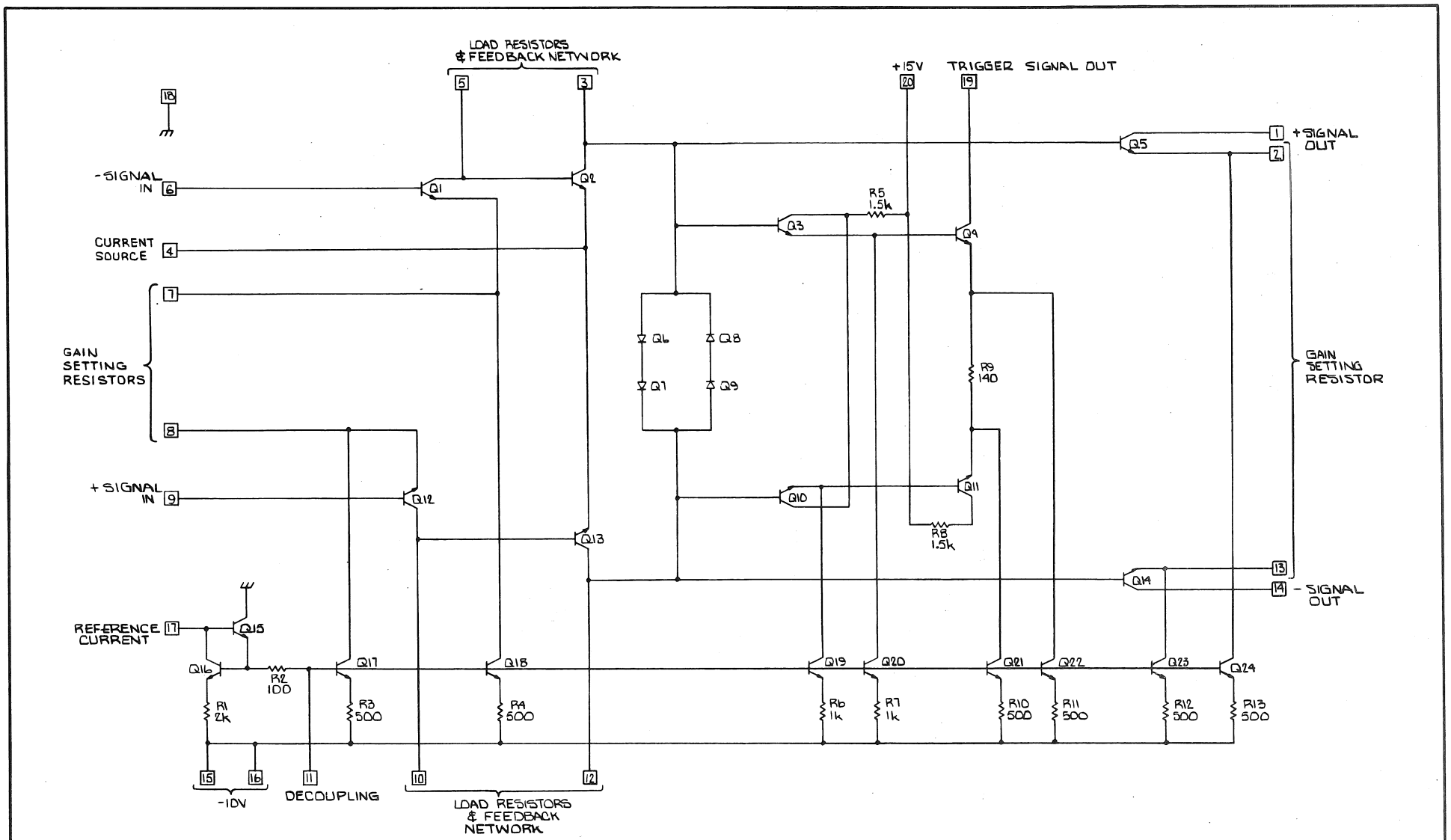
Pre-amp for the 432 and 434 Portable scopes, this circuit has provisions for gain-switching and gain adjustment. In addition, basic sensitivity is set by an external resistor.

Package: 20 DIP

Designer: Bert Tentkate

ICE Contact: Einar Traa

Instrument Usage: 314K (2)
432 (2)
434 (2)



ENGR	Ehen Tiao	9-30-75	PROCESS	200 Ω/□
DWN BY	PAM CHERRIE	11-12-74	PACKAGE	20 PIN DIP
CHK BY	David VanCleave	2-10-76	DIE SIZE	45mil X 35mil
TYPE	MONOLITHIC	VERTICAL PREAMP		M065
INTERGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0050-01		

IN Production
by CER

M077A 155-0059-00 GAIN TRIM AMP

Description:

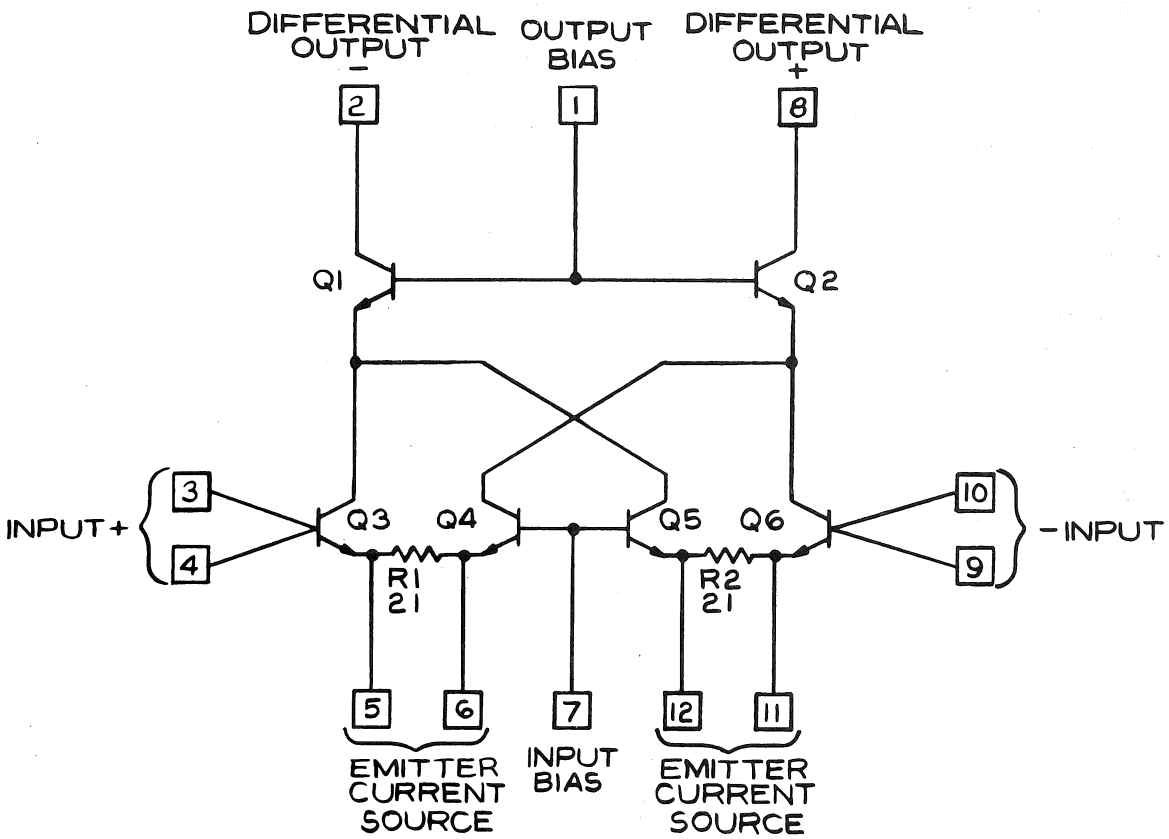
f_T Doubler with Nichrome Emitter resistors, Emitter peaking with MOS capacitors, grounded Base output transistors connected similar to a multiplier for gain trim.

Package: 12 lead Small pattern TO-8

Designer: Thor Hallen

ICE Contact: George Wilson

Instrument Usage:
7904 (1)
7844 (2)
7903 (1)
7912 (1)



NOTE:

1. SUBSTRATE WIRE BONDED TO CASE.

ENGR	[illegible]	7-1-76	PROCESS	SHF II
DWN BY	J. Langley	6-30-76	PACKAGE	12 LEAD SMALL PATTERN TO-8
CHK BY	[illegible]	7-14-76	DIE SIZE	45mil X 40mil
TYPE	MONOLITHIC	GAIN TRIM AMPLIFIER		M077A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0059-00		

IN Production
by CER

M080C 203-0080-00 HF OUTPUT AMP

Description:

The M080 is fabricated by the SHF Process, and has two MOS capacitors across the Nichrome resisters. It is capable of delivering 200 mA to the output.

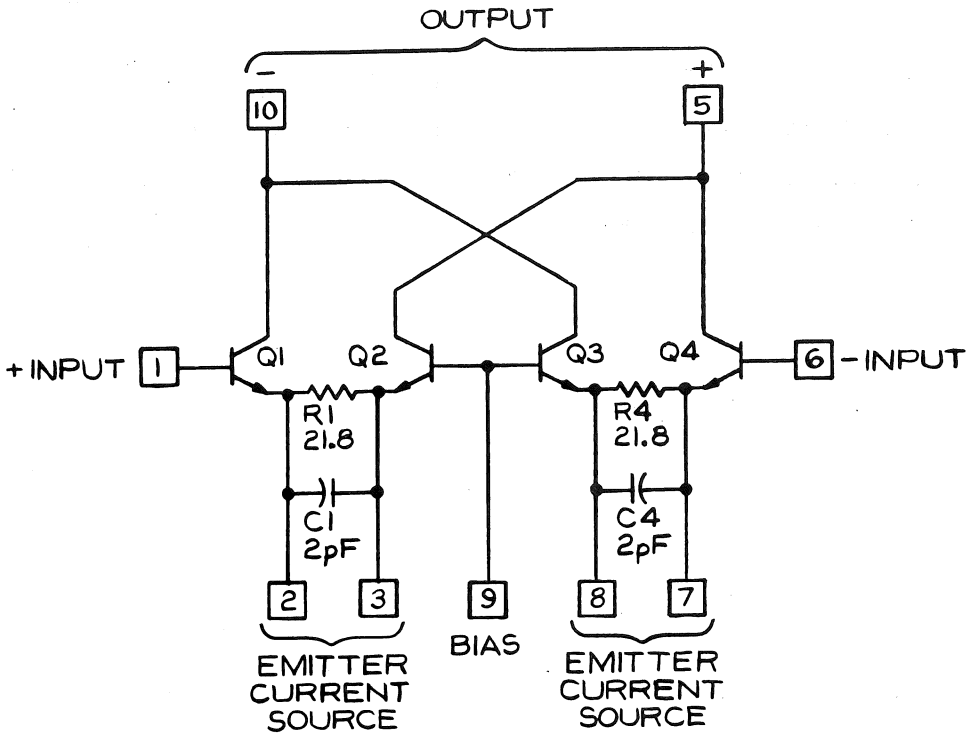
Package: See H074, H074A

Designer: Thor Hallen

ICE Contact: George Wilson

Instrument Usage:

485 (1)	7844 (2)	7912 (1)
4851 (1)	7903 (1)	
4852 (1)	7904 (1)	



ENGR	E. Trae	7-8-76	PROCESS	SHF II
DWN BY	J. Langley	7-6-76	PACKAGE	12 LEAD LARGE PATTERN TO-8
CHK BY	Linda Boyer	7-14-76	DIE SIZE	30mil X 40mil
TYPE	MONOLITHIC	HF OUTPUT AMPLIFIER		M080C
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 203-0080-90		

IN Production

By CER

M083 155-0061-00 f_T DOUBLER AMPLIFIER

Description:

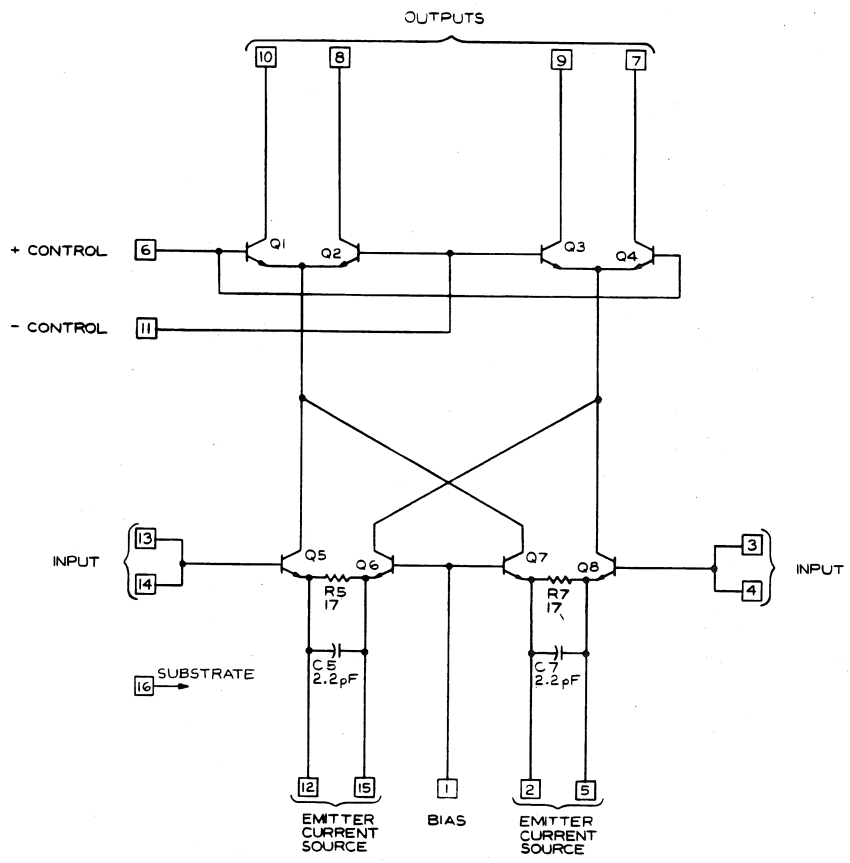
f_T doubler amplifier designed for the 7904 channel switch and built with the SHF Process. Equal size output transistors allow it to be used for variable and invert operations. Output transistors are designed for linear operation to 75 mA.

Package: 16 DIP

Designer: Hans Springer

ICE Contact: George Wilson

Instrument Usage: 7B92A (6)



ENGR		10-28-75	PROCESS	SH II
DWN BY	J. Langley	10-22-75	PACKAGE	16 DIP
CHK BY	C. WESTON	10-28-75	DIE SIZE	50mil X 45mil
TYPE	MONOLITHIC	f_T DOUBLER AMPLIFIER		M083
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0061-00		

IN Production

By CER

M084E	155-0078-00	155-0078-06	485 VERTICAL AMPLIFIER
	155-0078-01	155-0078-07	
	155-0078-02	155-0078-10	
	155-0078-03	155-0078-11	
	155-0078-04	155-0078-12	
	155-0078-05	155-0078-13	

Description:

A differential amplifier designed for the 485 Vertical. The cascode outputs can provide gain adjust or invert functions by using the proper control voltage. All transistors have been designed to carry a maximum of 90 mA while maintaining their f_T.

Package: 16 lead Minipac

Designer: John Addis

ICE Contact: George Wilson

M084E (continued)

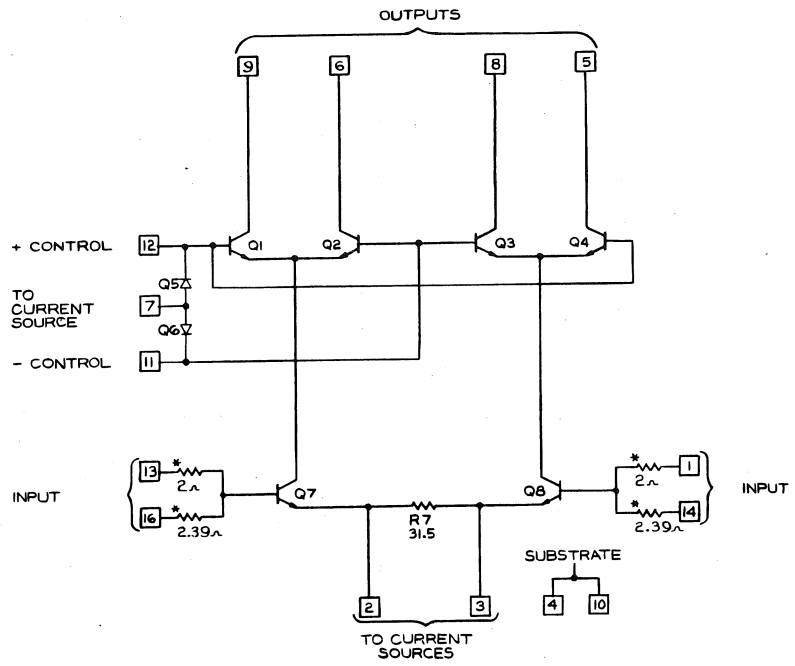
Instrument Usage:

155-0078-00		155-0078-01		155-0078-02		155-0078-03	
475G	(3)	485	(5)	485	(8)	485	(10)
475H	(3)	4851	(5)	4851	(7)	4851	(6)
475K	(3)	4852	(5)	4852	(7)	4852	(6)
485	(2)	7A16	(1)			7844	(2)
4851	(2)	7A24	(4)			7A16	(3)
4852	(2)	7A26	(4)			7A24	(3)
7A24	(1)	7A16A	(1)			7A26	(3)
7A26	(1)					7903	(3)
7A26H						7904	(6)
						475G	(3)
						475H	(3)
						485K	(2)
						475	(1)
						7A26H	(3)

067-0587-01 (1)

155-0078-04	155-0078-05		155-0078-06	155-0078-07	
None	475	(1)	PG 502 (1)	475	(2)
	7912	(1)			

155-0078-10		155-0078-11	155-0078-12	155-0078-13	
485	(2)	485 (5)	AM 503 (1)	7A26	(4)
7A26	(4)			7834	(4)
PG 508	(1)			7A26G	(4)
7A26G	(4)			7A26K	(4)
7A26K	(4)				



NOTE:
1. RESISTORS MARKED WITH * ARE METAL RUNS.

ENGR		10-10-75	PROCESS	SHII
DWN BY	J. Langley	10-9-75	PACKAGE	16 PIN MINIPAC
CHK BY	C. WESTON	10-27-75	DIE SIZE	50 mil X 42 mil
TYPE	MONOLITHIC	485 VERTICAL AMPLIFIER		M084E
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0078-00		

IN Production
by CER

M089A 203-0089-00 VERTICAL OUTPUT AMPLIFIER

Description:

The circuit consists of three cascode stages. The first stage serves as high frequency compensation and termination for the delay line. The second stage will do gain peaking at high frequencies to compensate for the R-C roll-off at the CRT, in addition to low-frequency gain. The last stage has a fixed gain, and has terminals brought out for thermal distortion compensation, and also for external long-tails. The common base devices of the last cascode remain discrete in order to have enough breakdown voltage for a CRT. Bandwidth of the IC into a low impedance load is 600 MHz.

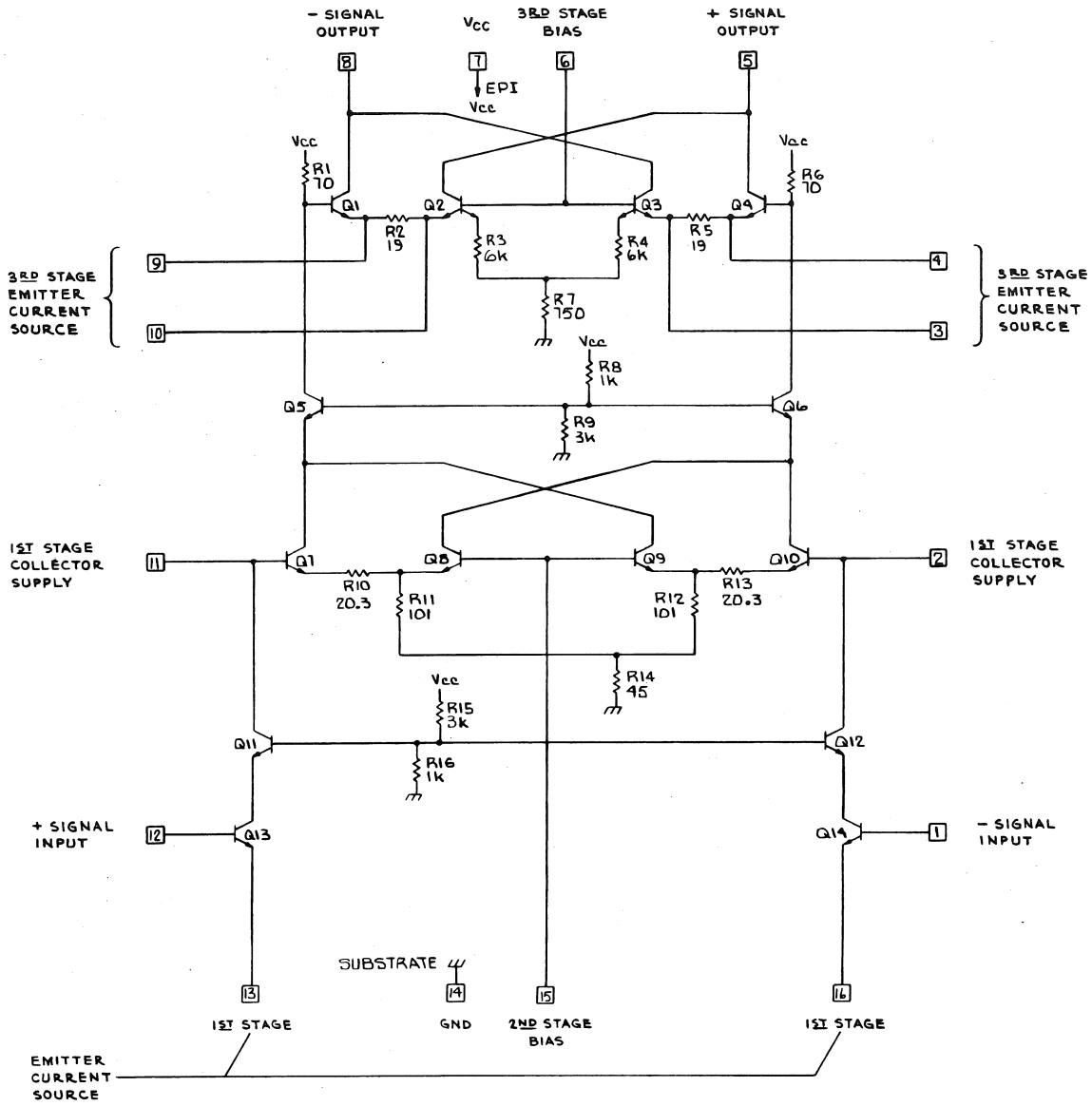
Package: See H106, H125

Designer: Jim Cavoretto - Einar Traa

ICE Contact: Einar Traa

Instrument Usage:

465G (1)
465H (1)
465K (1)
7704A (1)
D7704G (1)
D7704H (1)
335K (1)
464 (1)
466 (1)



ENGR	Chan Tree	10-15-74	PROCESS	SH II
DWN BY	Pam Cherrie	8-8-74	PACKAGE	WAFER FORM
CHK BY	[illegible]	11-1-74	DIE SIZE	50mil x 55mil
TYPE	MONOLITHIC	VERTICAL OUTPUT AMPLIFIER		M089A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A		PART NO. 203-0089-90		

IN Production
by CER

M102A 203-0102-00 VERTICAL OUTPUT AMPLIFIER

Description:

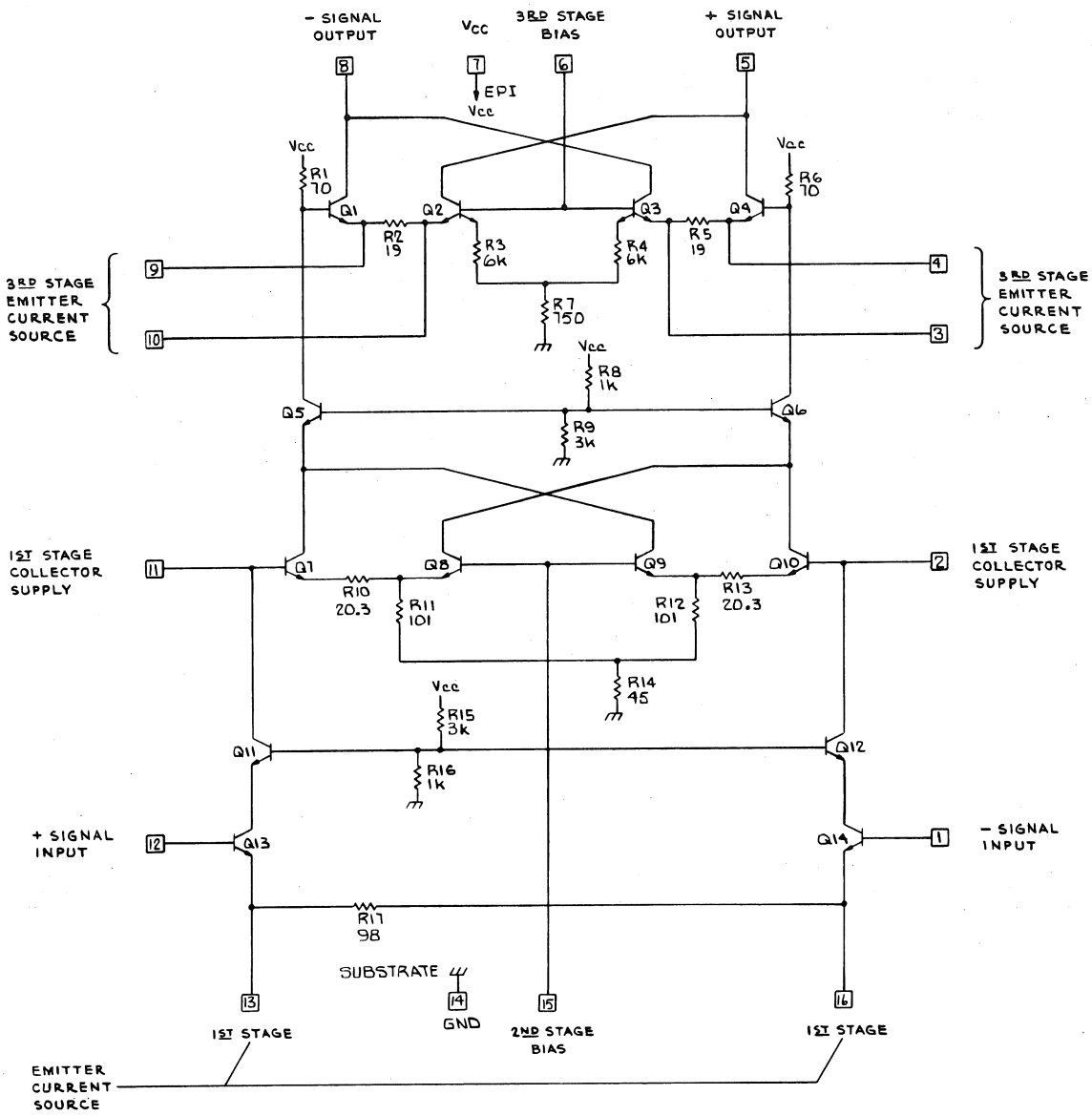
Similar to M089, except for a 98Ω Nichrome resistor added between the Input Emitters as an integral part of the chip.

Package: See H126

Designer: Einar Traa

ICE Contact: Einar Traa

Instrument Usage: 475 (1)



ENGR	Sean Trace	10-28-74	PROCESS	SH II
DWN BY	Pam Cherrie	8-8-74	PACKAGE	WAFER FORM
CHK BY	DK Nikel	11-1-74	DIE SIZE	50 mil x 55 mil
TYPE	MONOLITHIC	VERTICAL OUTPUT AMPLIFIER		M107A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A		PART NO. 203-0102-90		

IN Engineering

M116

VERTICAL AND HORIZONTAL OUTPUT AMPLIFIERS ON ONE CHIP

Description:

Two push pull amplifiers on one chip with plus or minus 60 volt swing (120 volts differentially) available from one, and normally less swing (plus or minus 36 volts) from the other. Low in power consumption.

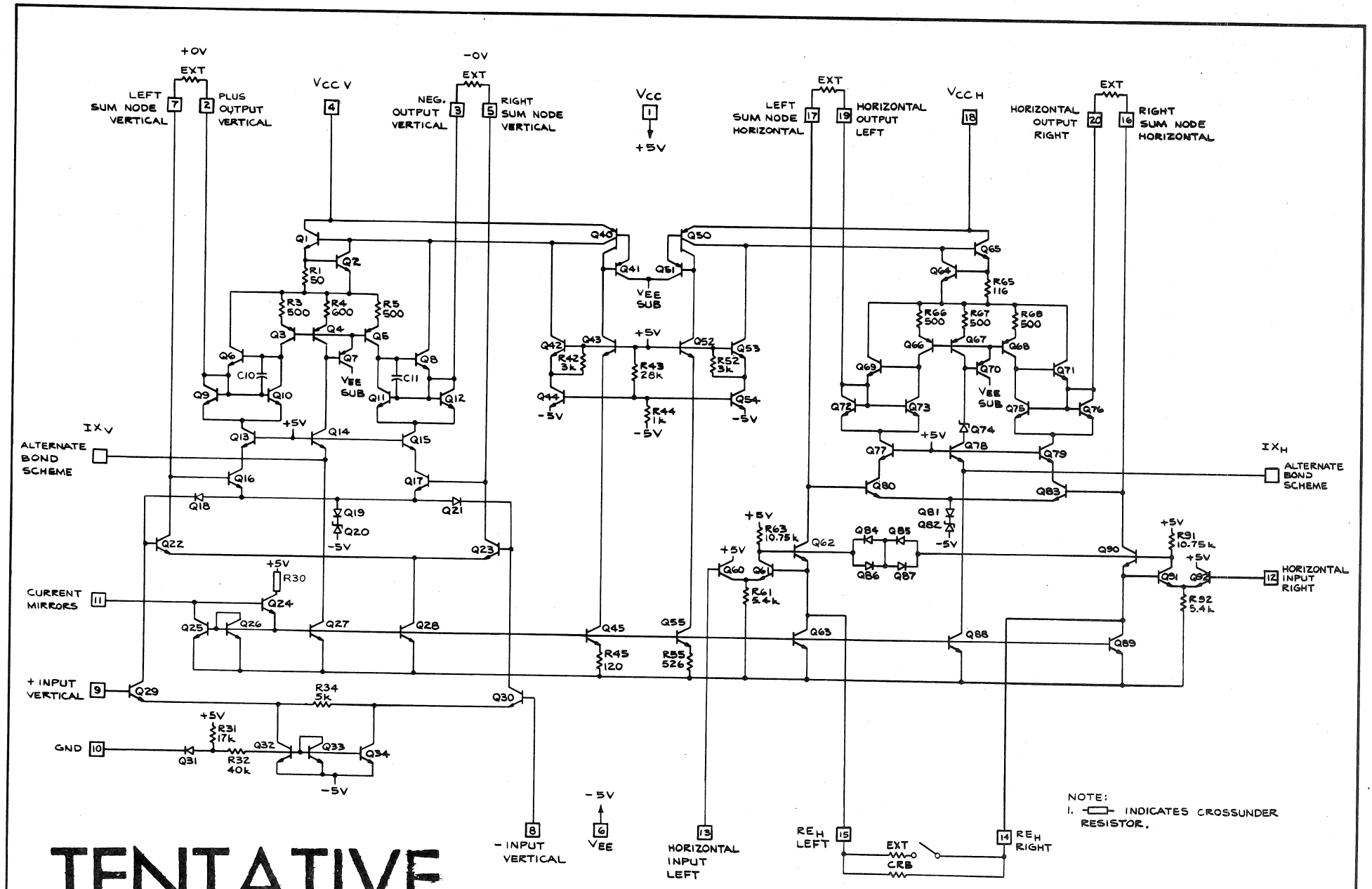
The device features a built-in regulator dependent on the device voltage breakdown, automatically lowering internal supply voltages (+71-91 volts) to a value which will not allow breakdown in the amplifier devices. This circuitry also includes a thermal shutdown capability for the output amplifiers if the chip temperature exceeds 200°C.

Package: 20 pin DIP, second alternative - 24 pin ceramic package.

Designer: Carl Battjes

ICE Contact: Carl Battjes

Instrument Usage: None



TENTATIVE

ENGR	Carl R Battjes	1-20-77	PROCESS	HVIC II
DWN BY	S POLENDEY	8-9-76	PACKAGE	20 PIN DIP
CHK BY			DIE SIZE	65 mil. X 65 mil.
TYPE	MONOLITHIC	VERTICAL & HORIZONTAL OUTPUT AMPLIFIERS		M116
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON U.S.A		PART NO.		

IN Production

M126 203-0126-90 f_T DOUBLER AMPLIFIER

Description:

This circuit is an altered version of the M083. The M083 NiCr emitter resistors have been removed; otherwise it is the same.

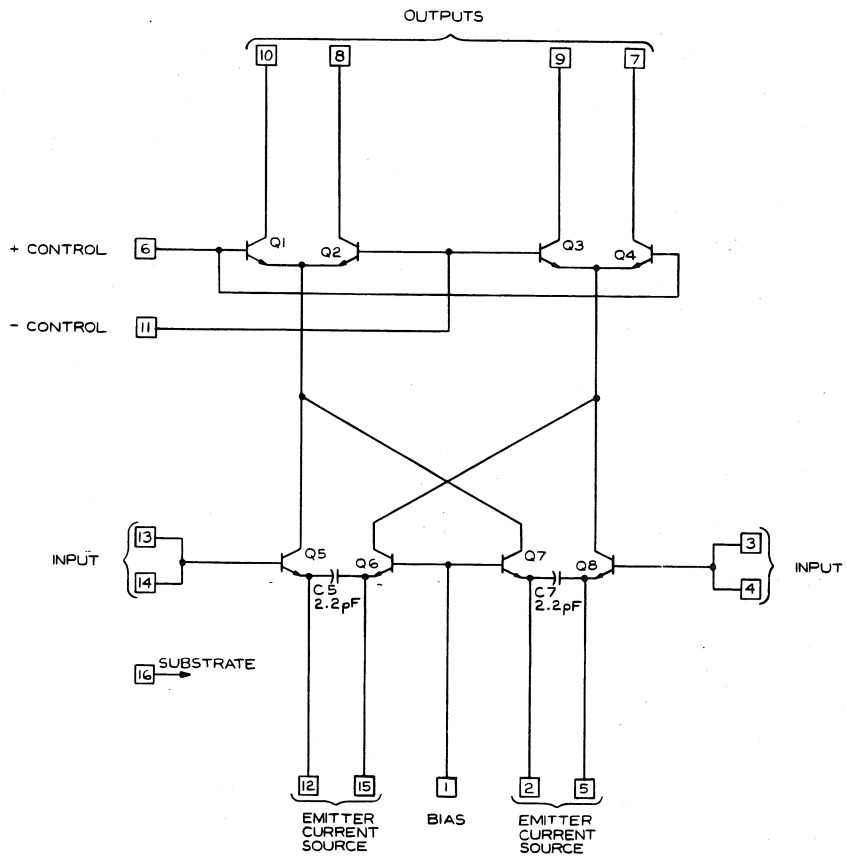
Package: TO-8 with small stud

Designer: Hans Springer

ICE Contact: George Wilson

Instrument Usage: 7844 MODS (2), (4), (8)
7903 (2)
7904 (6)

7903 (2)
7904 (6)



ENGR		10-28-75	PROCESS	SH II
DWN BY	J. Langley	10-22-75	PACKAGE	TO-8 w. STUD
CHK BY	C. WESTON	10-28-75	DIE SIZE	50mil X 45mil
TYPE	MONOLITHIC	f_T DOUBLER AMPLIFIER		M126
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 203-0126-90		

IN Production
by CER

M130 203-0130-00 VERTICAL AMPLIFIER

Description:

M130 is a pre-amplifier for the 455 portable oscilloscope. Each chip contains one channel with gain switch, gain calibration, positioning, trigger pick-off and channel switch. Two chips are combined on a ceramic substrate with heatsink and printed resistors to form H332.

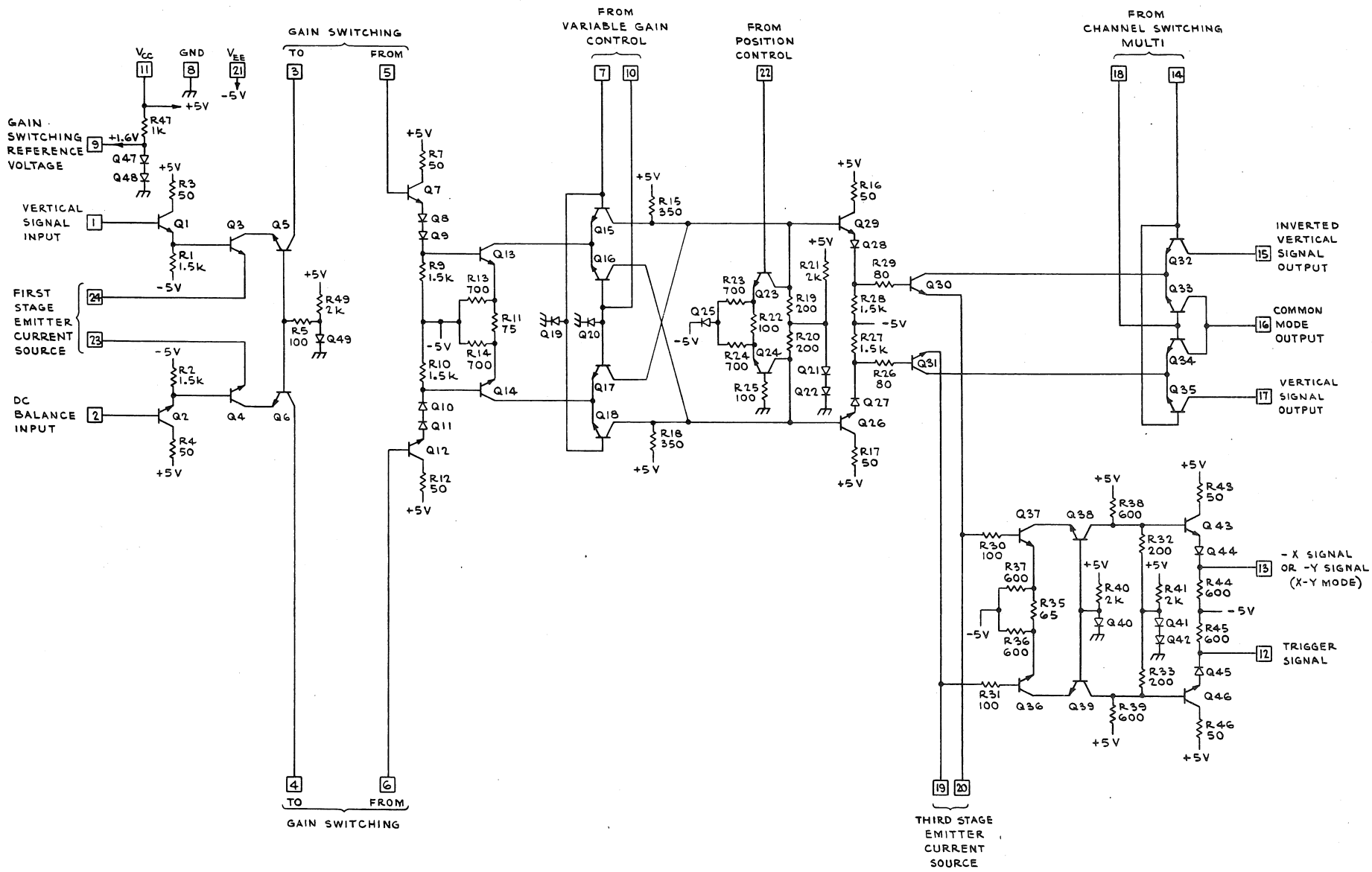
Power Supply: ± 5 volts and ground.

Package: H332

Designer: Jim Woo

ICE Contact: Einar Traa

Instrument Usage: 455 (2)



ENGR	Ehan Trae	1-24-75	PROCESS	SHF II
DWN BY	R. Hankins	12-18-74	PACKAGE	H332
CHK BY	M. Ellson	6-18-75	DIE SIZE	65 mil x 65 mil
TYPE	MONOLITHIC	VERTICAL AMPLIFIER		M130
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 203-0130-00		

IN Engineering

M134

X1 AMPLIFIER

Description:

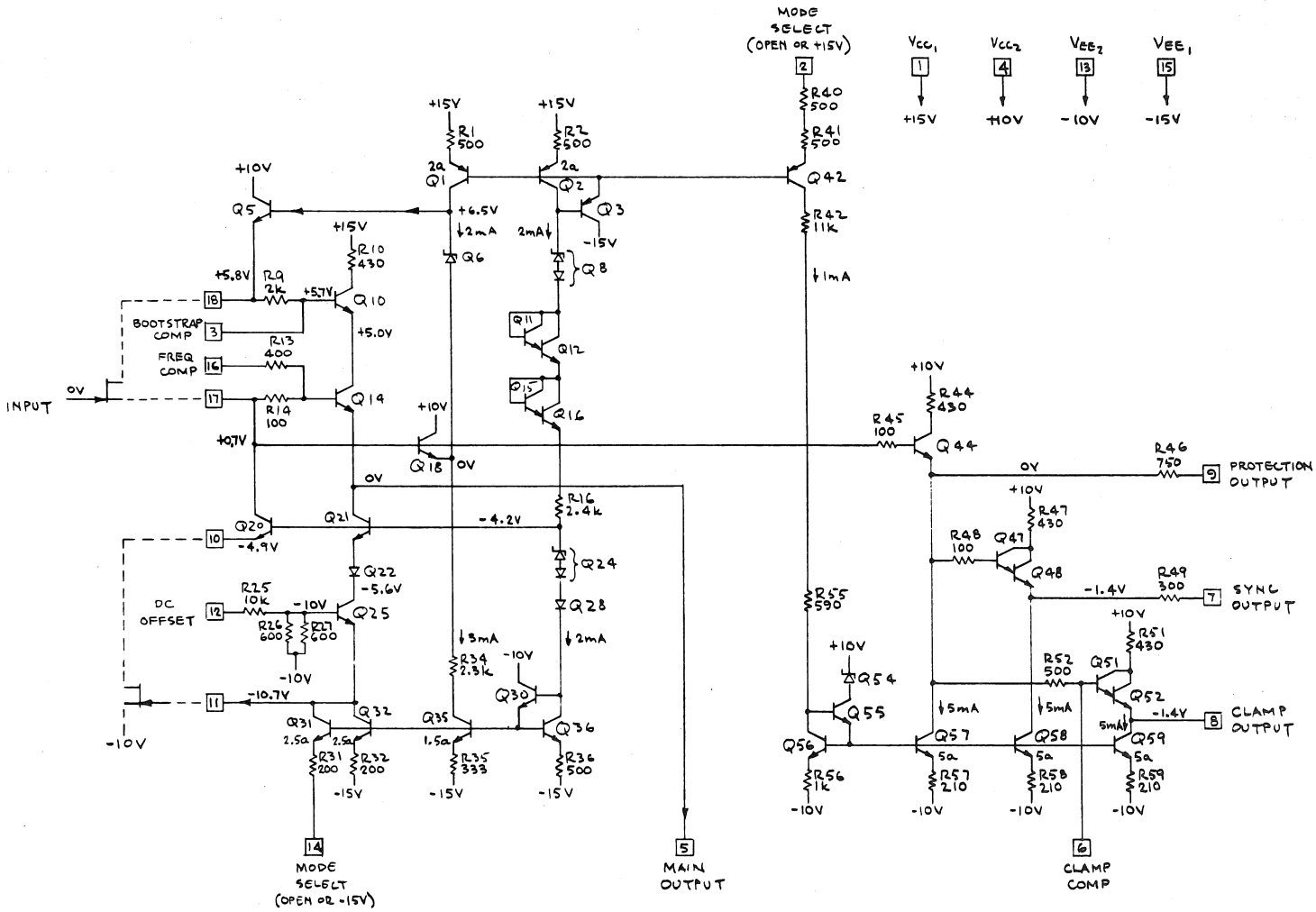
This circuit, in conjunction with a dual matched FET pair, is intended for use as an accurate unity gain buffer amplifier. The low-impedance main output can be externally adjusted to zero output offset voltage. Three independent auxiliary outputs are provided; they may be disabled and their power saved if desired.

Power Supply: ± 15 V

Package: Hybrid H328

Designer: Ken Schlotzhauer

ICE Contact: Ken Schlotzhauer



TENTATIVE

REVISIONS					
ENGR					45 X 55 mil
DR BY RH	9-17-74				
INITIALS	DATE				REMARKS

TITLE X1 AMPLIFIER M134

TEK TRONIX, INC., BEAVERTON, OREGON, U.S.A. DRAWING NO.

CHAS. BRUNING CO.

IN Engineering

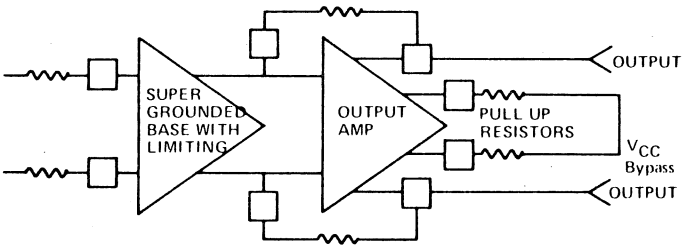
M156

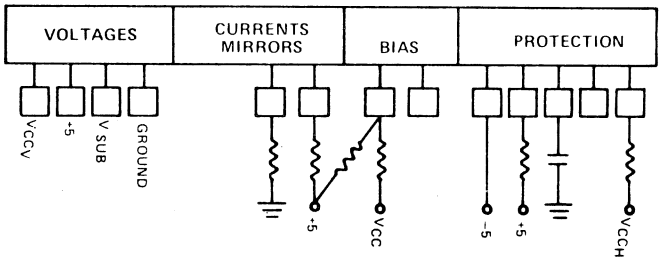
LOW POWER VERTICAL OUTPUT AMPLIFIER

Description:

Low Power Vertical Output Amplifier, class AB, up to 50 MHz bandwidth, up to 45 volts swing per side (±45 volt differential). Short circuit protection, thermal shutdown, output limiting and input circuit for delay line termination are on-chip.

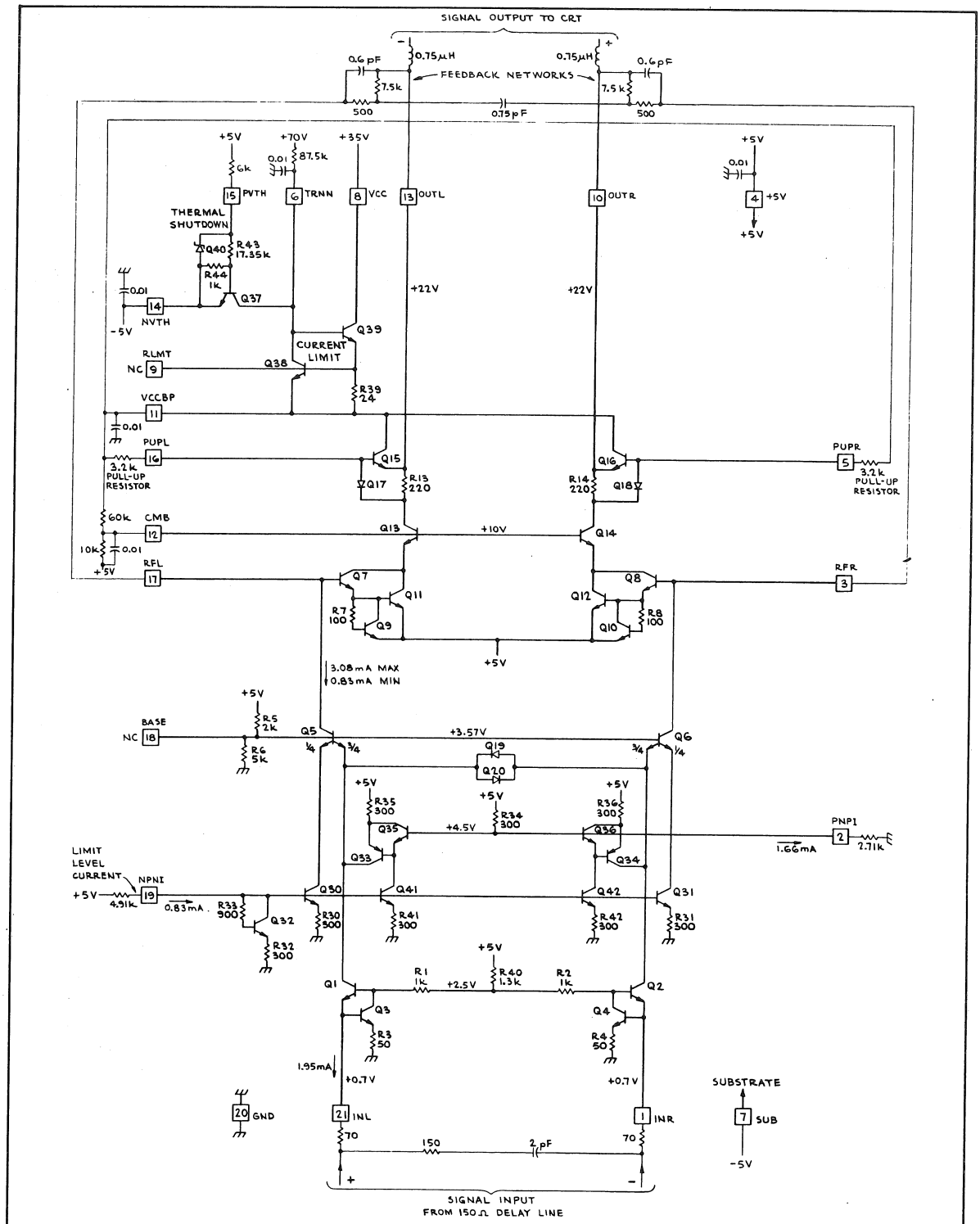
M 156 (Vertical)





Power Supply:	± 5 and V_{CC} up to 65
Package:	20, 24 lead ceramic or hybrid
Designer:	Carl Battjes
ICE Contact:	Carl Battjes
Instrument Usage:	Pending

TENTATIVE



NOTES:

1. ☐ INDICATES BONDING PAD ON DIE. PADS ARE NUMBERED COUNTERCLOCKWISE.
2. AMPLIFIER BANDWIDTH - 40 MHz. SYSTEM BANDWIDTH - 25 MHz.

ENGR	Carl R Betts	1-20-77	PROCESS	HVIC II
DWN BY	R. Hankins	19 NOV 76	PACKAGE	
CHK BY			DIE SIZE	55 mil X 67 mil
TYPE		LOW POWER CLASS AB VERTICAL AMPLIFIER		M156
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO.		

IN Engineering

M176 232-VERTICAL PREAMP

Description:

The M176 is a dual channel vertical preamp with channel switch, channel switch logic and sweep-switch flip-flop/chop oscillator. The chip includes positioning and trigger pick off for both channels. It does not include input stage, gain switching and delay line driver.

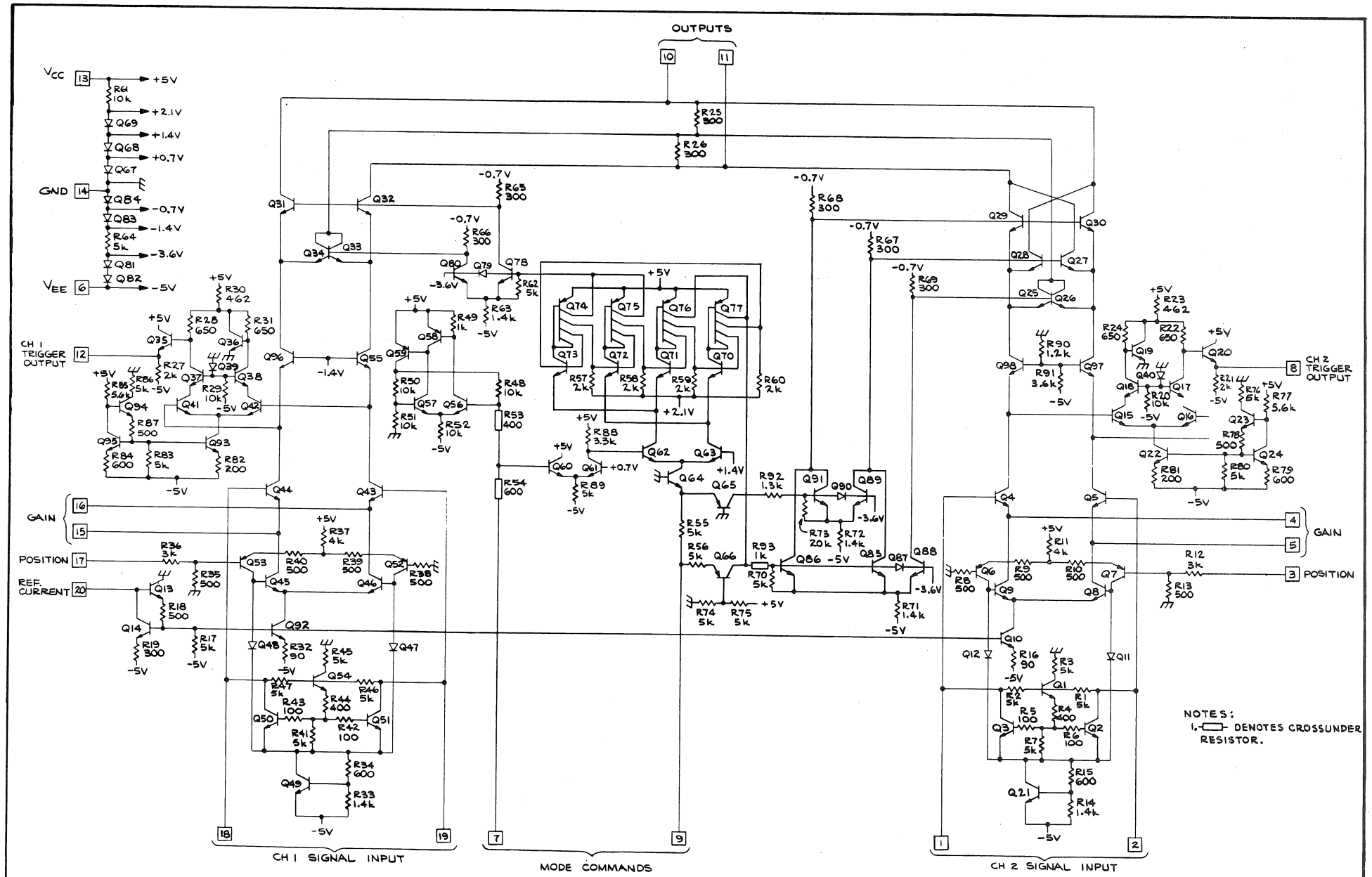
Power Supply: +5v, 0, -5v

Package: 20 PIN DIL

Designer: E. Traa

ICE Contact: E. Traa

Instrument Usage: None



TENTATIVE

ENGR	Eric Traa	1-19-77	PROCESS	200Ω/□
DWN BY	S. POLENDEY	9-17-76	PACKAGE	20 PIN DIP
CHK BY			DIE SIZE	70 mil. X 96 mil.
TYPE MONOLITHIC		232 VERTICAL PREAMP		M176
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON U.S.A.		PART NO.		

IN Engineering

M183 155- PROGRAMMABLE VERTICAL PREAMP

Description:

The M183 is a monolithic integrated circuit consisting of two cascode amplifiers and one f_T doubler amplifier stages which provide single-end or differential input and differential output.

The first stage consist of ÷1, ÷5 and ÷12.5 active gain switching into double-terminated constant resistance network. All gain switchings are done by remote controlling the base dc bias and common-mode voltage of the common-base transistors, and stacking the appropriate sections of the constant resistance network. Similarly, the second stage consists of ÷1, ÷2 and ÷4 gain switchings.

The third stage provides additional gain and may be used for signal inversion and variable gain control.

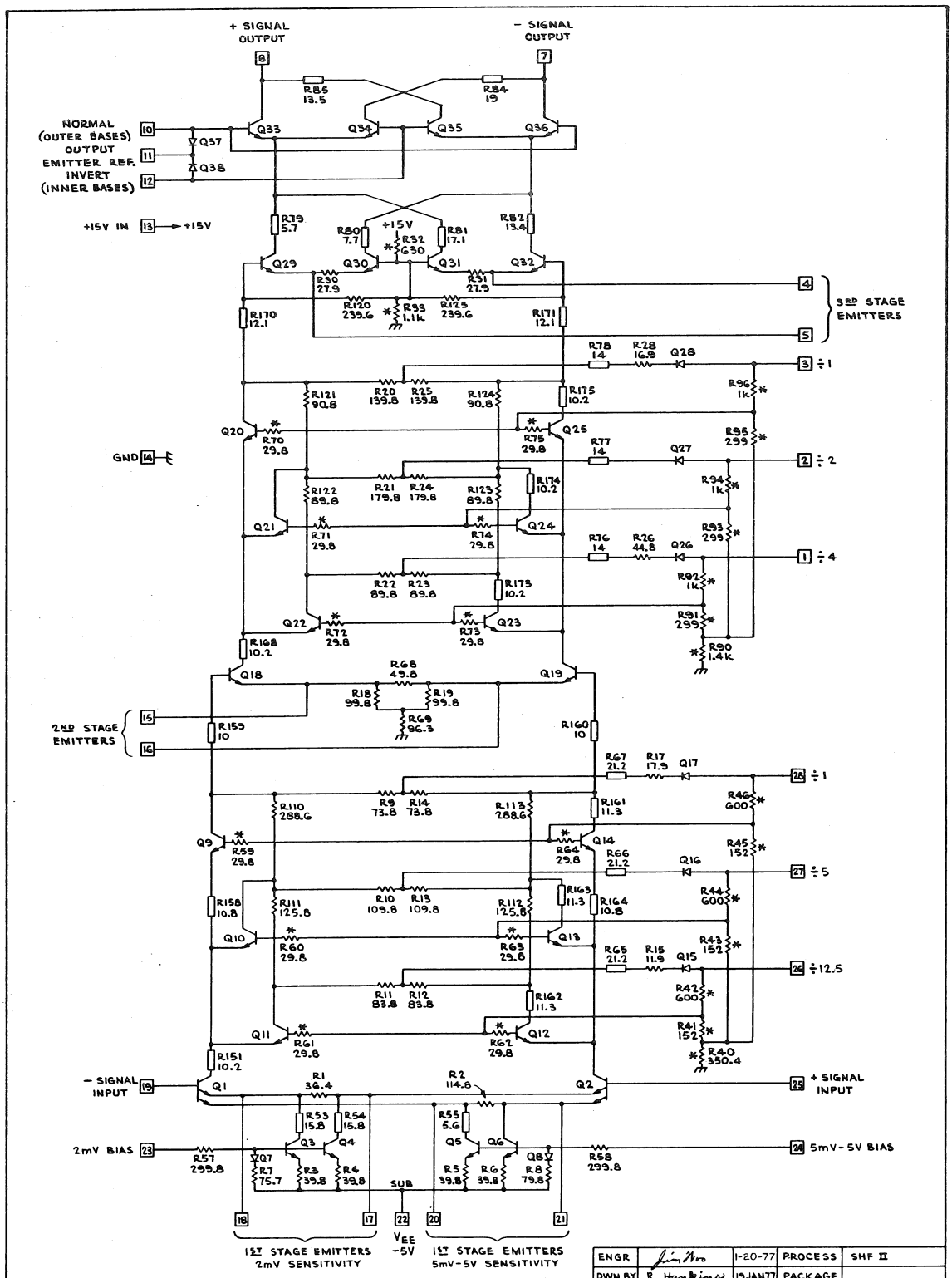
Power Supply: -5v, +15v

Package: 24 Pins

Designer: Jim Woo

ICE Contact: Jim Woo

Instrument Usage: Future 400 Series Scopes (2/instrument)



NOTES:

1. -▭- DENOTES DEEP COLLECTOR CROSS UNDER RESISTOR.
2. * DENOTES 50Ω D BASE DIFFUSED RESISTOR.
3. ALL OTHER RESISTORS ARE NiCr.

ENGR	Jim Moo	1-20-77	PROCESS	SHF II
DWN BY	R. Hawkins	19JAN77	PACKAGE	
CHK BY	C. WESTON	6-20-77	DIE SIZE	70X90 mils
TYPE		PROGRAMMABLE VERTICAL AMPLIFIER		M183B
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO.		

IX. TV AND CRT CONTROL CIRCUITS

IN Production
by CER

M068 155-0051-00 423 Z-AXIS AND HV REGULATOR

Description:

This IC comprises two separate circuits, a H.V. regulator amplifier and the Z axis amplifier.

The H.V. regulator is a high gain non-inverting amplifier using a triple darlington input for low bias current. A reference supply, also using a triple darlington, establishes a differential input voltage.

The Z axis amplifier is used in a feed-back mode with external circuitry. The current into the summing node is determined by three current inputs at -5 V. This current is switched through hot carrier diodes by the unblanking current input.

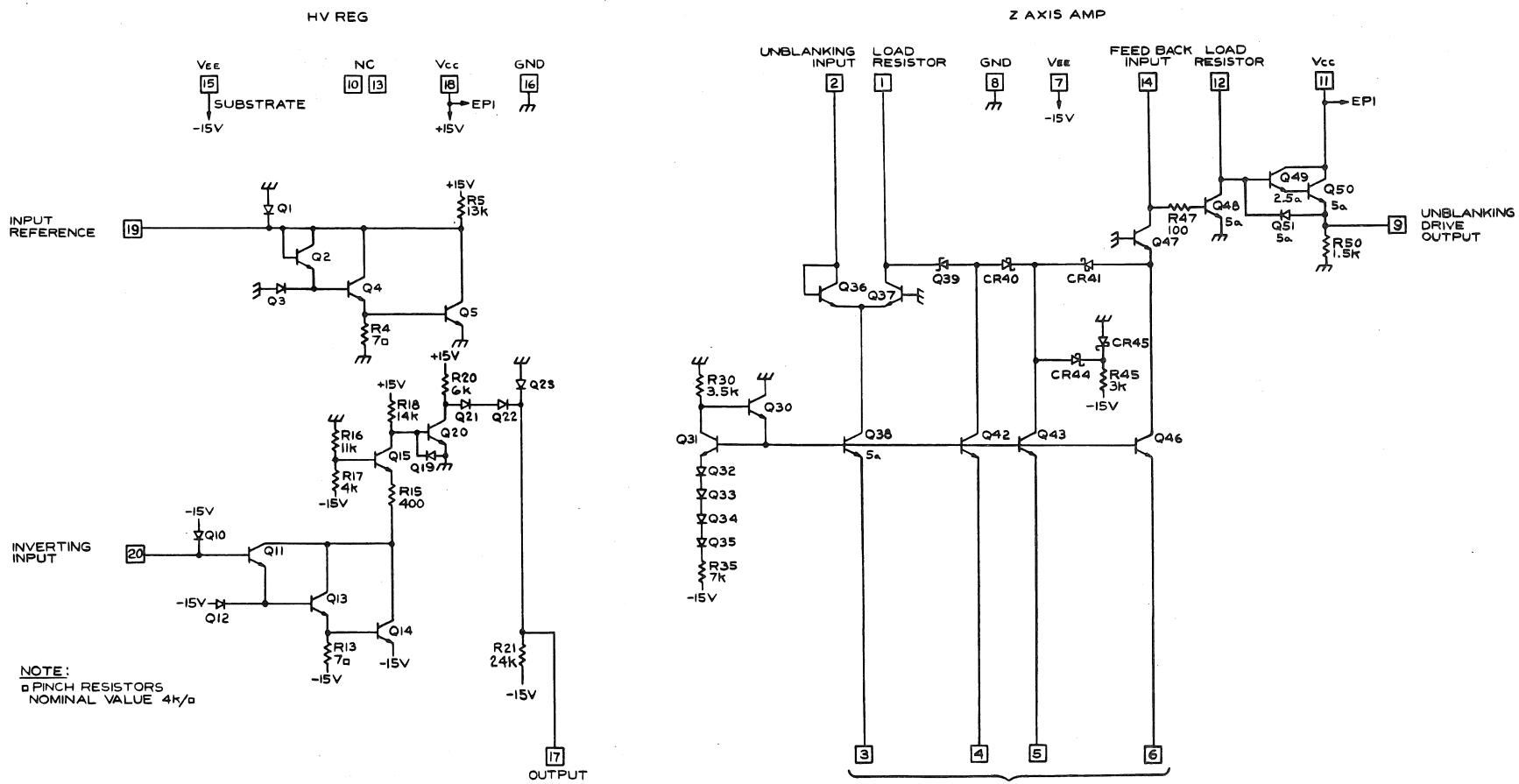
Power Supply: V_{CC} + 15V
V_{EE} - 15V

Package: 20 DIP

Designer: Frank Churchill

ICE Contact: Mike Metcalf

Instrument Usage: 432 (1)
434 (1)



ENGR	M. H. Antent	4-4-75	PROCESS	STD In-cm w/Schottky
DWN BY	J. Langley	3-4-75	PACKAGE	20 PIN DIP
CHK BY	Dee McGrady	6-20-75	DIE SIZE	45 mil X 45 mil
TYPE	MONOLITHIC	Z AXIS & HV REGULATOR		M068
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0051-00		

IN Production
by CER

M124A 155-0144-00 SYNC STRIPPER

Description:

This circuit provides a means of precisely determining the time of occurrence of the 50% points of the horizontal sync pulses accompanying a wide variety of different composite video systems. Several auxilliary outputs are available to aid in system control. The circuit is built using the standard 200Ω/square process.

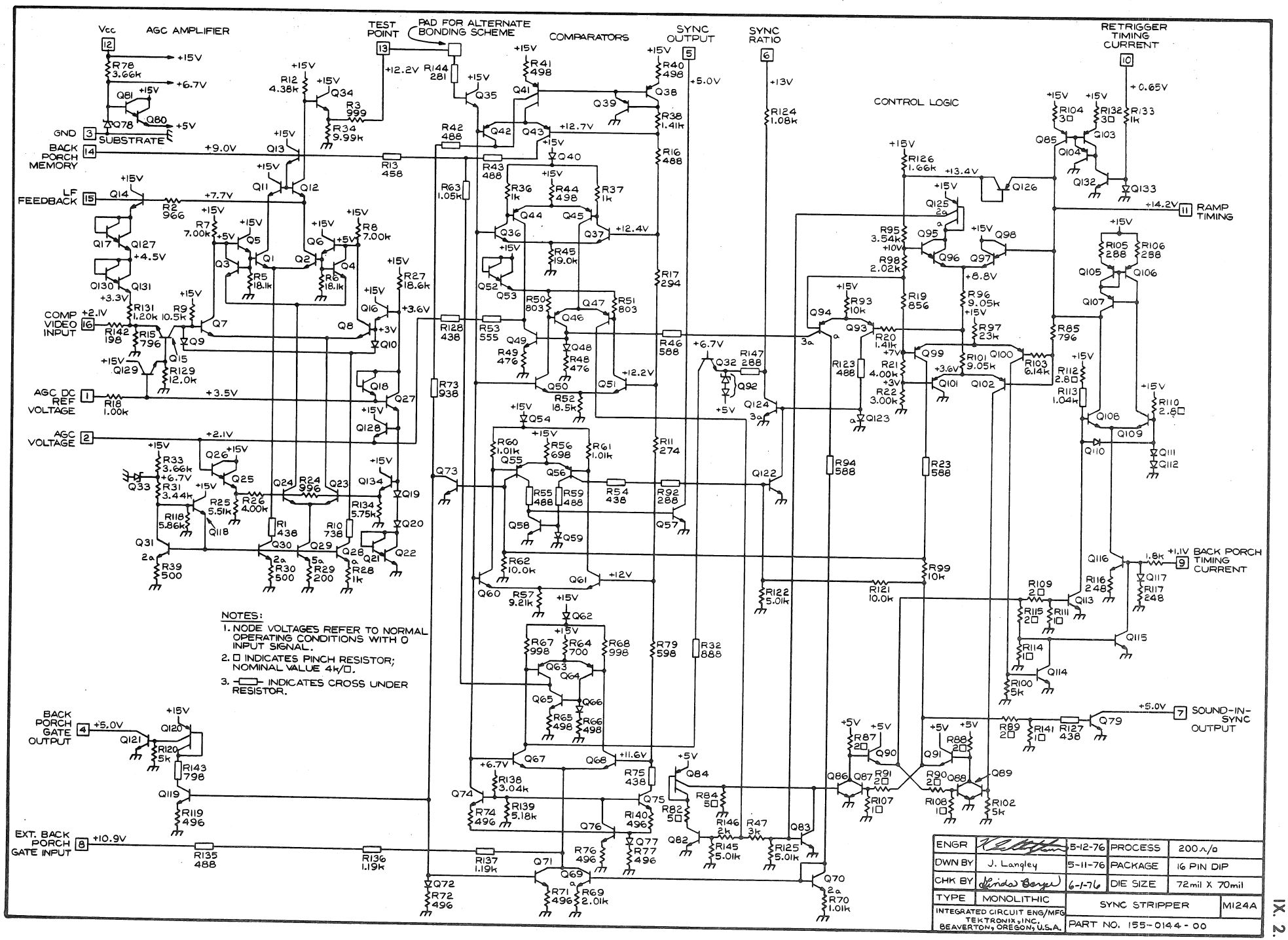
Power Supply: +15

Package: 16 PIN DIP

Designer: Steve Roth, Ken Schlotzhauer

ICE Contact: Ken Schlotzhauer

Instrument Usage: 1410, 1470


AGC AMPLIFIER
TEST POINT
PAD FOR ALTERNATE BONDING SCHEME
COMPARATORS
SYNC OUTPUT
SYNC RATIO
RETRIGGER TIMING CURRENT
CONTROL LOGIC
Vcc
GND
SUBSTRATE
BACK PORCH MEMORY
LF FEEDBACK
COMP VIDEO INPUT
AGC DC REF VOLTAGE
AGC VOLTAGE
BACK PORCH GATE OUTPUT
EXT. BACK PORCH GATE INPUT
RAMP TIMING
BACK PORCH TIMING CURRENT
SOUND-IN-SYNC OUTPUT
NOTES:
1. NODE VOLTAGES REFER TO NORMAL OPERATING CONDITIONS WITH 0 INPUT SIGNAL.
2. □ INDICATES PINCH RESISTOR; NOMINAL VALUE 4k/□.
3. —▭— INDICATES CROSS UNDER RESISTOR.
ENGR 5-12-76 PROCESS 200 n/p
DWN BY J. Langley 5-11-76 PACKAGE 16 PIN DIP
CHK BY 6-1-76 DIE SIZE 72mil X 70mil
TYPE MONOLITHIC
SYNC STRIPPER M124A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.
PART NO. 155-0144-00

IN Production
by CER

M151A 155-0145-00 PULSE OUTPUT AMPLIFIER

Description:

This circuit provides a controlled risetime output pulse occurring between ground and a programmable negative level, given a TTL input pulse. Two such amplifiers are provided per package, and the standard 200 Ω/square process is used.

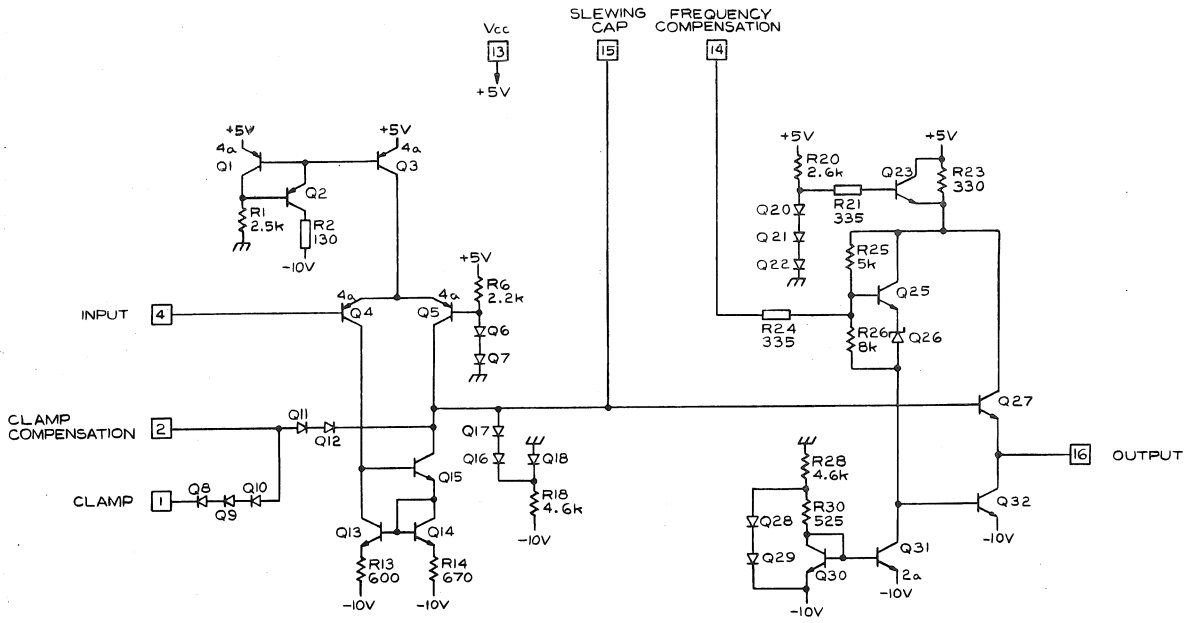
Power Supply: +5 to -10

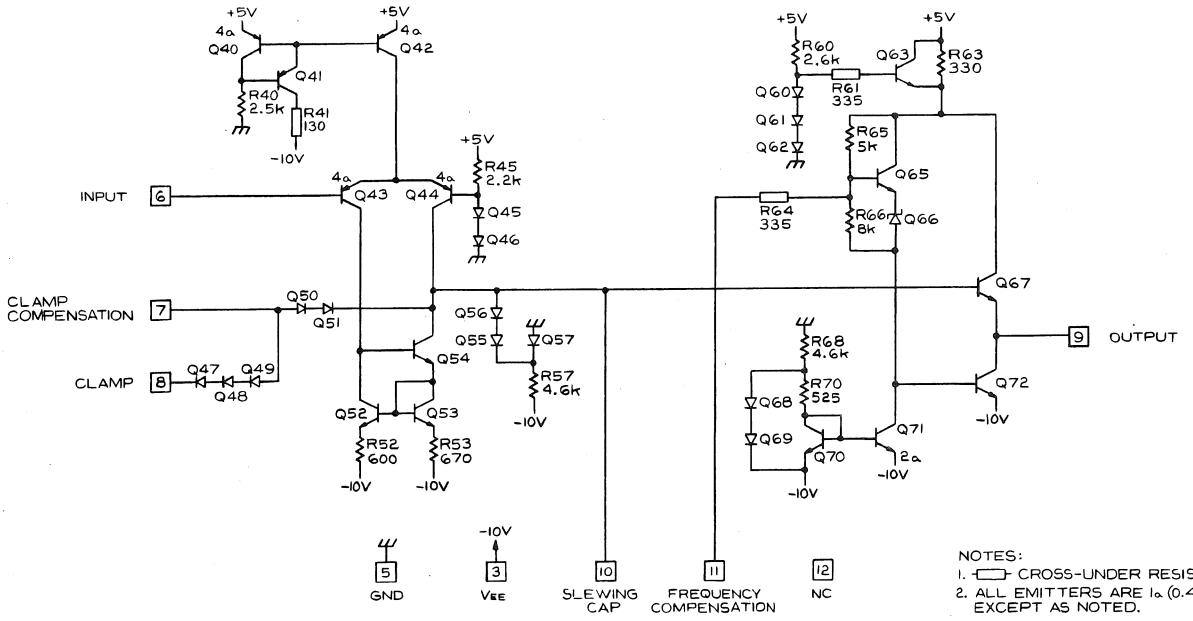
Package: 16 PIN DIP

Designers: Howard Landsman, Ken Schlotzhauer

ICE Contact: Ken Schlotzhauer

Instrument Usage: 1410, 1470





NOTES:
1. CROSS-UNDER RESISTORS.
2. ALL EMITTERS ARE 1a (0.4mil X 0.6mil) EXCEPT AS NOTED.

ENGR		12-29-75	PROCESS	200n/o
DWN BY	J. Langley	12-17-75	PACKAGE	16 PIN DIP
CHK BY	Linda Berger	1-15-76	DIE SIZE	51mil X 70mil
TYPE	MONOLITHIC	PULSE OUTPUT AMPLIFIER		M151A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0145-00		

IN Production

M152 155-0152-00 CRT GEOMETRY CORRECTION

Description:

The M152 is designed to appropriately predistort x and y signals before they are applied to the electromagnetic deflection coils of a CRT, in such a way as to eliminate "pincushion" distortion. It also provides a signal to correct for spot de-focusing that occurs away from the screen's center. The circuit may be used in CRTs of various deflection angles (up to 90°) by adjusting the values of two external resistors.

Mathematically, the following signals are available as outputs:

$$|x|,\ |y|,\ \sqrt{1 + (K_1X)^2 + (K_2Y)^2},$$

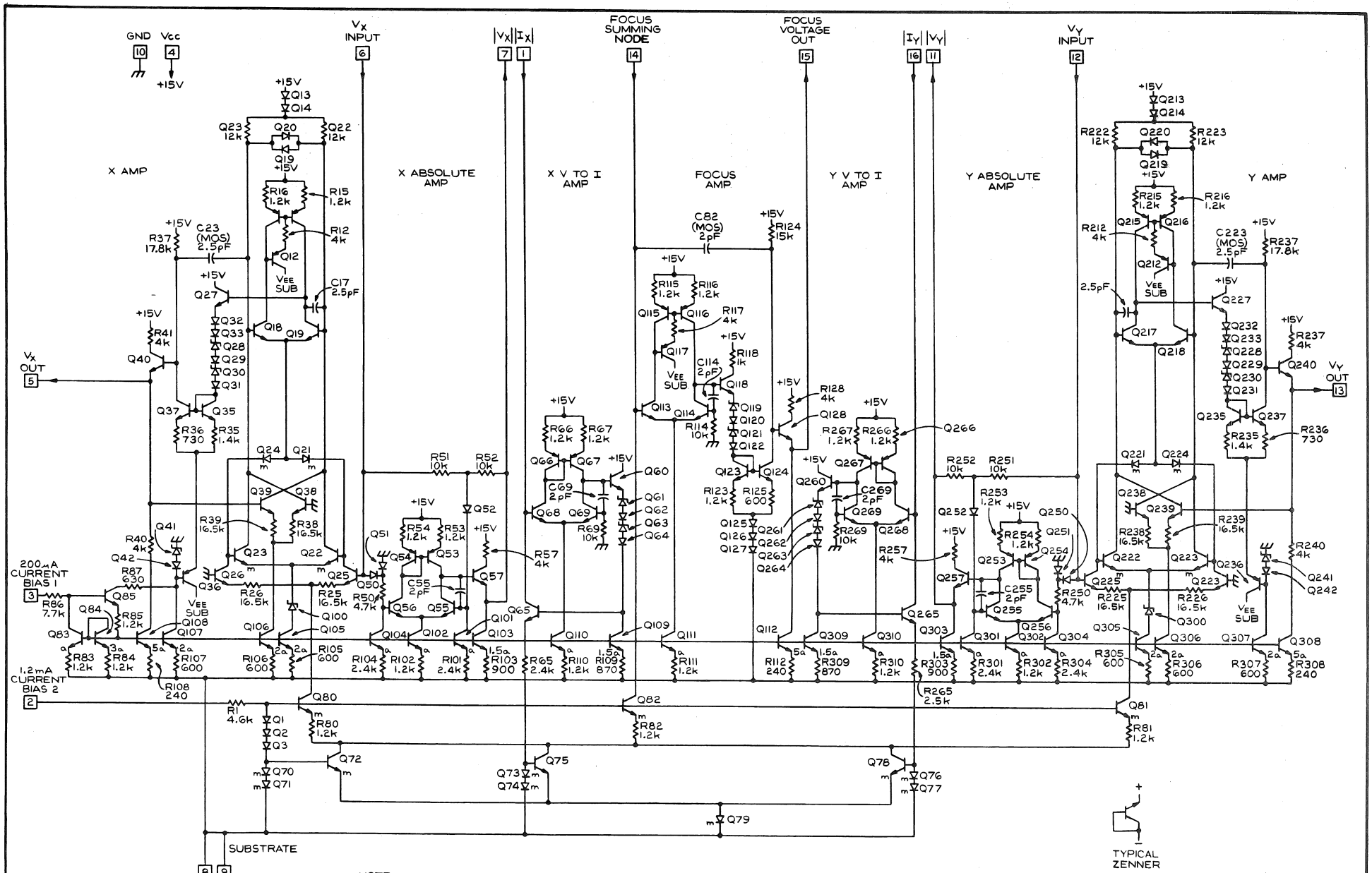
$$K_3 - \sqrt{1 + (K_1X)^2 + (K_2Y)^2},$$

$$\frac{X}{\sqrt{1 + (K_1X)^2 + (K_2Y)^2}},$$

$$\frac{Y}{\sqrt{1 + (K_1X)^2 + (K_2Y)^2}}$$

where K_1, K_2 and K_3 are adjustable externally.

Power Supply: +15, -12 (-15 optional)
Package: 16 PIN DIP, plastic
Designer: Binoy Rosario/Harvey Golladay
ICE Contact: Binoy Rosario
Instrument Usage: 4006



NOTE:
1. "m" INDICATES LARGE AREA EMITTER FOR IMPROVED MATCHING.
2. ALL EMITTER AREAS ARE 1a, (0.5mil X 0.6mil) UNLESS OTHERWISE INDICATED.

ENGR	B. Rosario	1-14-77	PROCESS	200Ω/□
DWN BY	J. Langley	10-14-76	PACKAGE	16 PIN DIP
CHK BY	S. Fiorro	3-4-77	DIE SIZE	72 mil X 93 mil
TYPE	MONOLITHIC	CRT GEOMETRY CORRECTION		M152
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0152-00		

IN Production

M154 155-0154-00 DISPLAY MULTIPLEXER

Description:

The M154 transmits one of three sets of inputs (hardcopy alphanumeric-mode or vector-mode) in accordance with the appropriate two-bit instruction on lines A and B. Each input set has X and Y channels.

A counter sequences through 8 offset positions each time a "page" (erase) signal is received. These offsets are added to the X and Y inputs to uniformly exercise the phosphor on all parts of the screen.

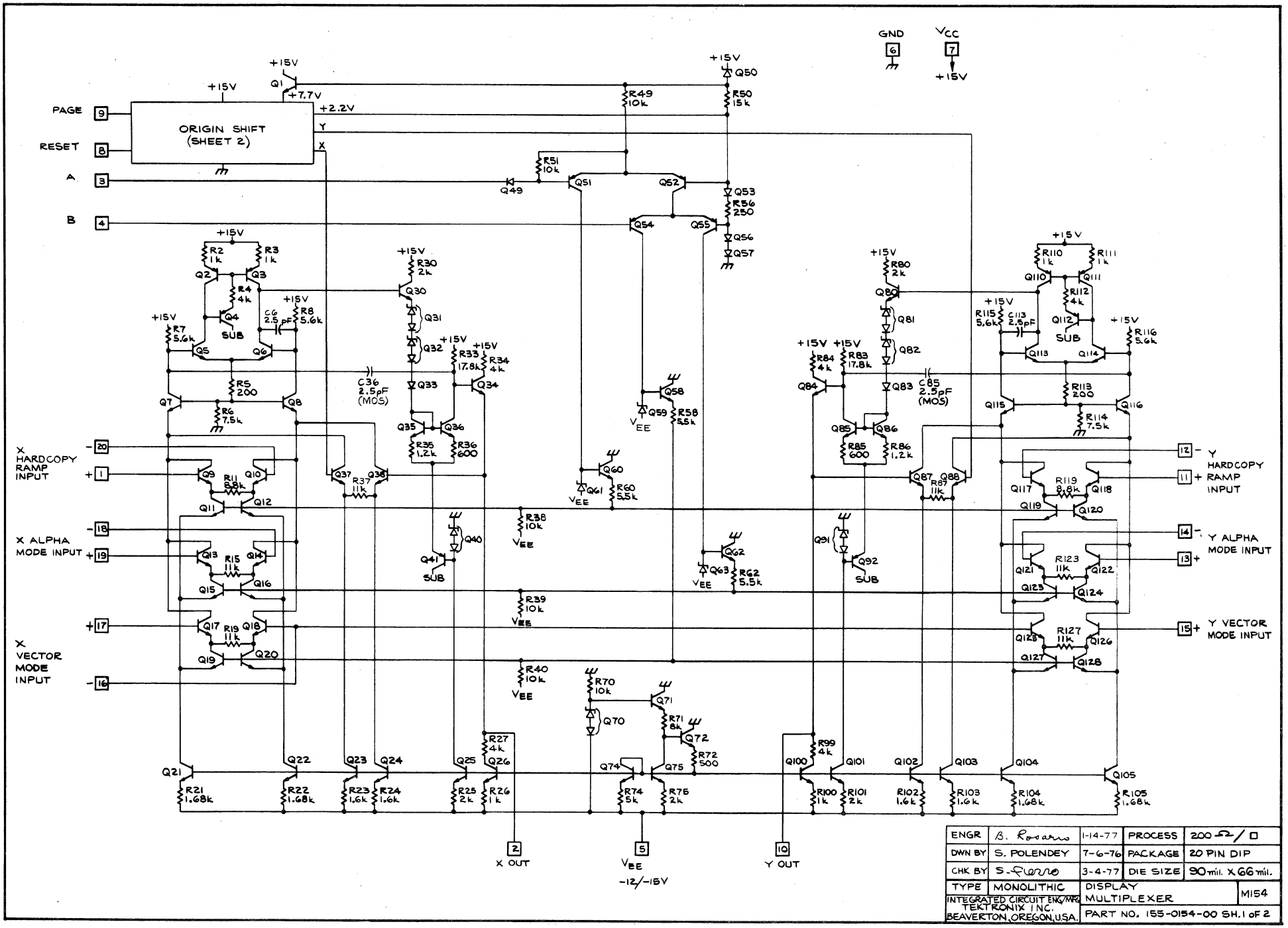
Power Supply: +15, -12 (-15 optional)

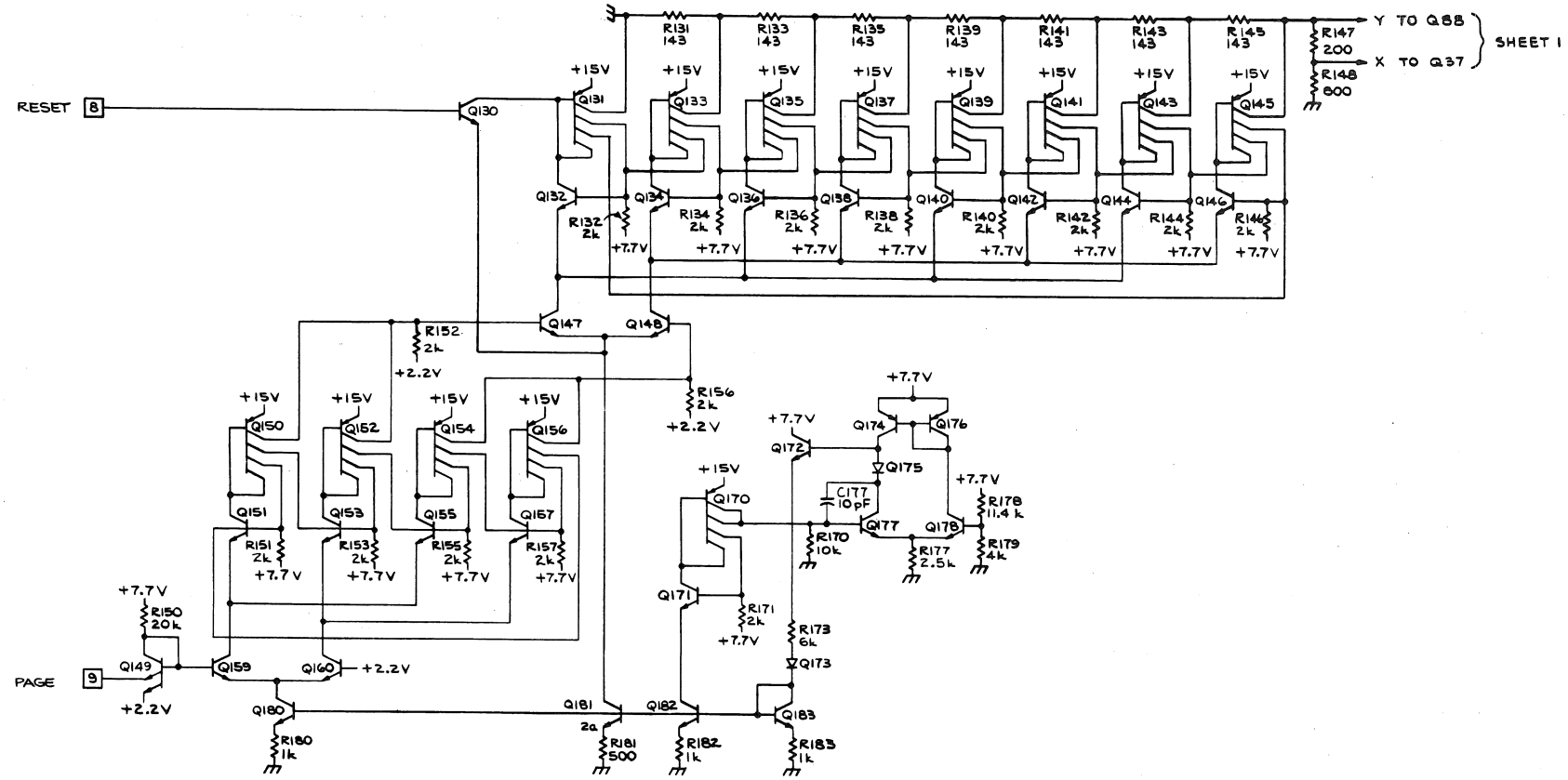
Package: 20 PIN DIP, plastic

Designer: Harvey Golladay

ICE Contact: Binoy Rosario

Instrument Usage: 4006


ORIGIN SHIFT (SHEET 2)
PAGE
RESET
A
B
GND
VCC
+15V
+7.7V
+2.2V
X
Y
X HARDCOPY RAMP INPUT
X ALPHA MODE INPUT
X VECTOR MODE INPUT
Y HARDCOPY RAMP INPUT
Y ALPHA MODE INPUT
Y VECTOR MODE INPUT
X OUT
Y OUT
VEE
-12/-15V
SUB
C36 2.5pF (MOS)
C85 2.5pF (MOS)
ENGR B. Rosario 1-14-77 PROCESS 200 Ω/□
DWN BY S. POLENDEY 7-6-76 PACKAGE 20 PIN DIP
CHK BY S. Rosario 3-4-77 DIE SIZE 90 mil. X 66 mil.
TYPE MONOLITHIC DISPLAY MULTIPLEXER M154
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX INC. BEAVERTON, OREGON, U.S.A.
PART NO. 155-0154-00 SH. 1 of 2



ENGR	B. Rosario	1-14-77	PROCESS	200 Ω/□
DWN BY	S. POLENDEY	7-6-76	PACKAGE	20 PIN DIP
CHK BY	S. Fiorio	3-4-77	DIE SIZE	90 mil. X 66 mil.
TYPE	MONOLITIC	DISPLAY MULTIPLEXER		M154
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0154-00		SH. 2 of 2

IN Production

M172 155-0153-00 VECTOR GENERATOR

Description:

The M172 is a Constant Velocity Vector Generator. The inputs are two step functions in the range ± 5 V, the initial and final values of which represent the initial and final co-ordinates (X1, Y1) and (X2, Y2) of the vector to be drawn on a display.

The outputs are two constant velocity ramps with the same initial and final values as the inputs and a ramp time ΔT which is proportional to the vector length, $\sqrt{(X2 + Y2)^2 + (Y1 - Y2)^2}$. The ramp time is also controlled by the values of two matched external capacitors to obtain writing rates up to 20 Volts/milisec.

An end-of-vector signal is available to control external logic.

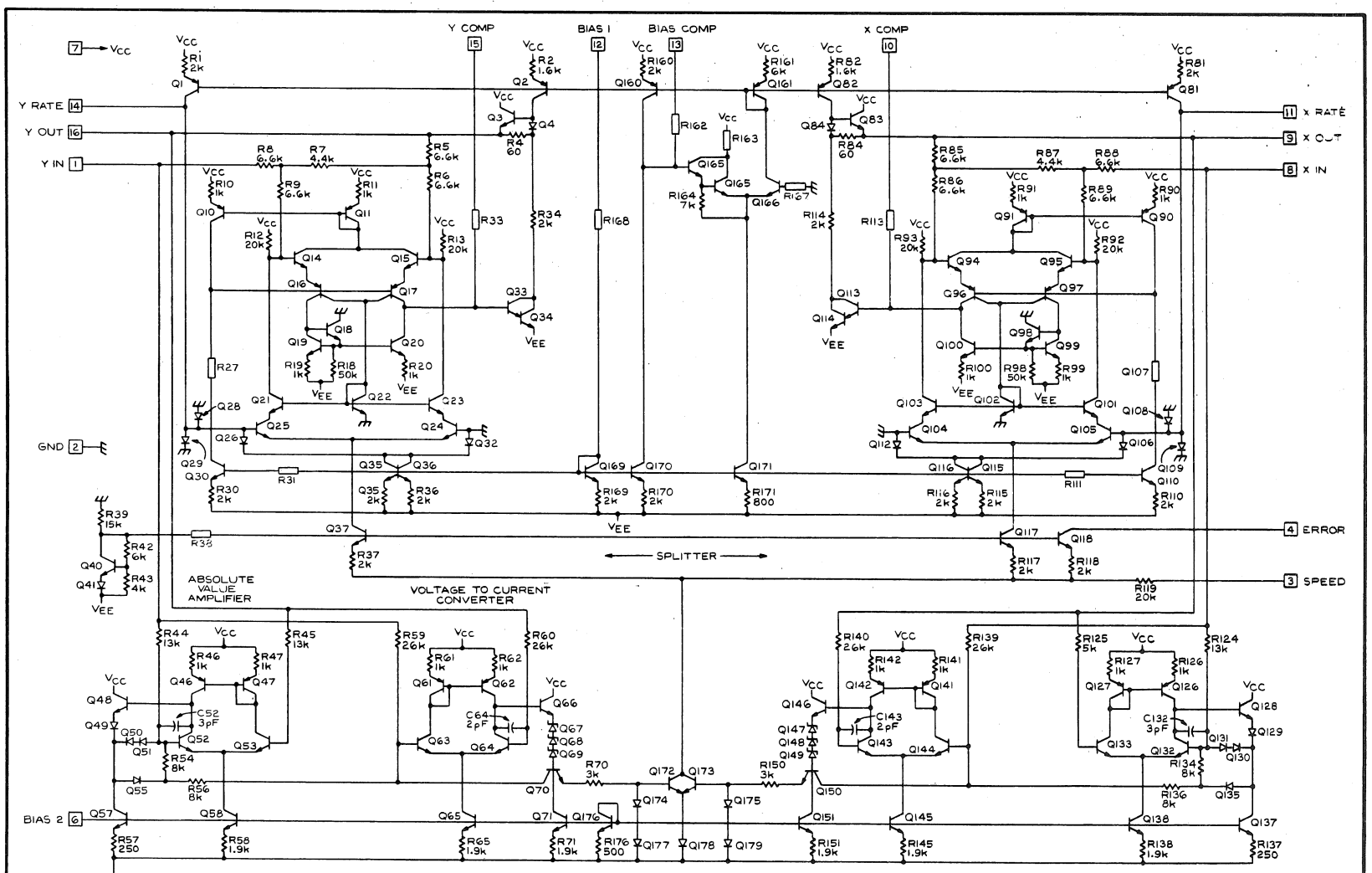
Power Supply: +15V - 15V (negative supply can be -12 to -15V)

Package: 16 pin plastic dip with Kovar clad copper leadframe

Designer: Binoy Rosario

ICE Contact: Binoy Rosario

Instrument Usage: GMA 101A Option 32



NOTE:
1. ⊟ INDICATES CROSSUNDER RESISTOR NOMINAL VALUE 500Ω TO 1500Ω
2. Q172 & Q173 CONSIST OF 3 PARALLEL TRANSISTORS EACH.

ENGR	B. A. Rosario	4-22-77	PROCESS	200Ω/□
DWN BY	J. Langley	3-17-77	PACKAGE	16 PIN DIP
CHK BY	S. Fierro	6-10-77	DIE SIZE	72 X 91 mils
TYPE	MONOLITHIC	VECTOR GENERATOR		M172B
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0153-00		

X. PROBE CONTROL CIRCUITS

IN Production
by CER

M048B 155-0033-00 PROBE POWER SUPPLY

Description:

Provides +7 and -10 volts from ± 12 to ± 15 volts input voltages with an output impedance of less than 10 Ω and temperature coefficient of less than two millivolts per °C. The supplies can deliver upwards from 100 mW, depending on heatsinking and ambient temperature requirements.

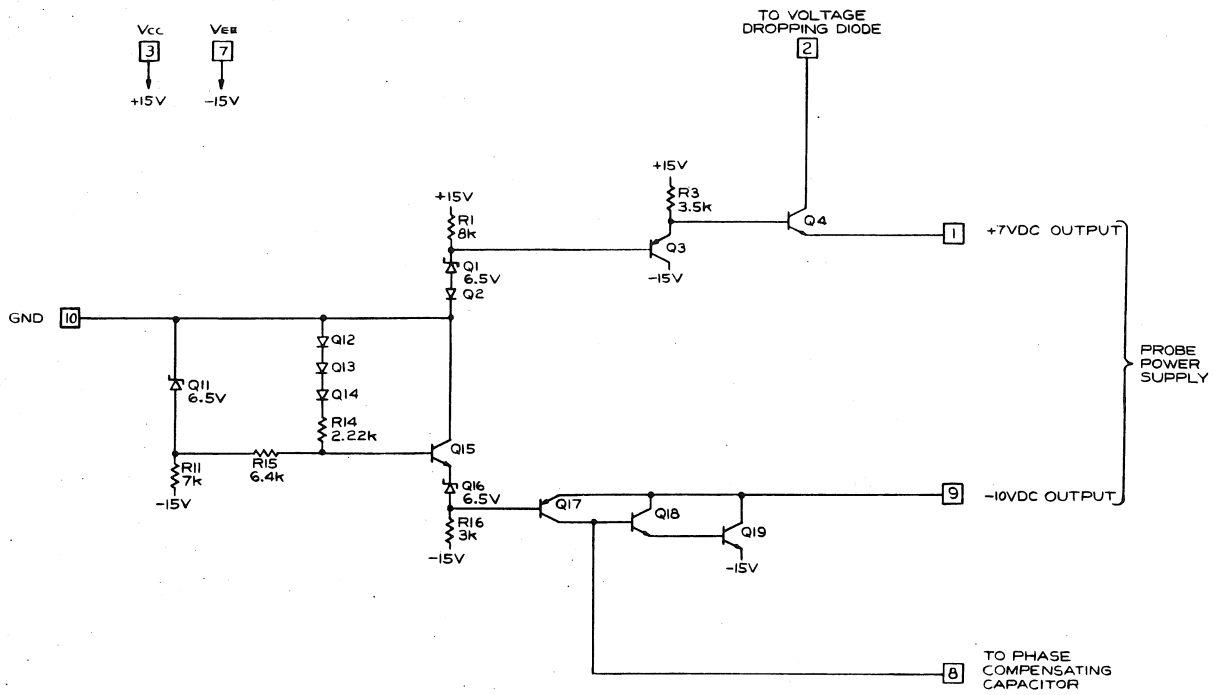
It also provides constant current sources of + 2 mA at $V_6 < +10$ V and
- 2 mA at $V_4 < -10$ V

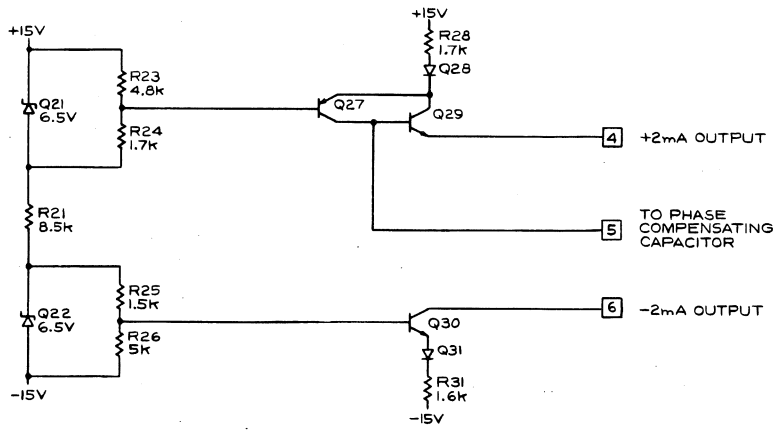
Package: 10 Lead TO-5

Designer: Glenn Bateman

ICE Contact: Einar Traa

Instrument Usage: 010-0227-00 (1)





ENGR	E Trae	2-24-75	PROCESS	200 n/p
DWN BY	J. Langley	2-11-75	PACKAGE	10 LEAD TO-5
CHK BY	David VanCleve	10-23-75	DIE SIZE	35 mil X 50 mil
TYPE	MONOLITHIC	PROBE POWER SUPPLY		M048
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0033-00		

IN Production

By CER

M094B 155-0076-00 INPUT PROTECTION & PROBE LOGIC

Description:

The M094 controls the 50 Ω/1 Megohm mode of the 485. It provides input protection and controls a "Mode Switch" lamp and lights a "Reset" lamp during overload. This device also performs an approximate RMS conversion on the input signal voltage and, with an external capacitor, integrates the result to obtain a signal proportional to heat generated in a 50 Ω attenuator. Excess signal trips a relay which can be used to open the the input signal and protect the input (50 Ω) attenuator.

As a secondary feature, the M094 also provides a X1, X10, X100, and trace identify functions for readout from a readout coded BNC. Lights appropriate LED and extinguishes all LEDs during trace I<D< mode.

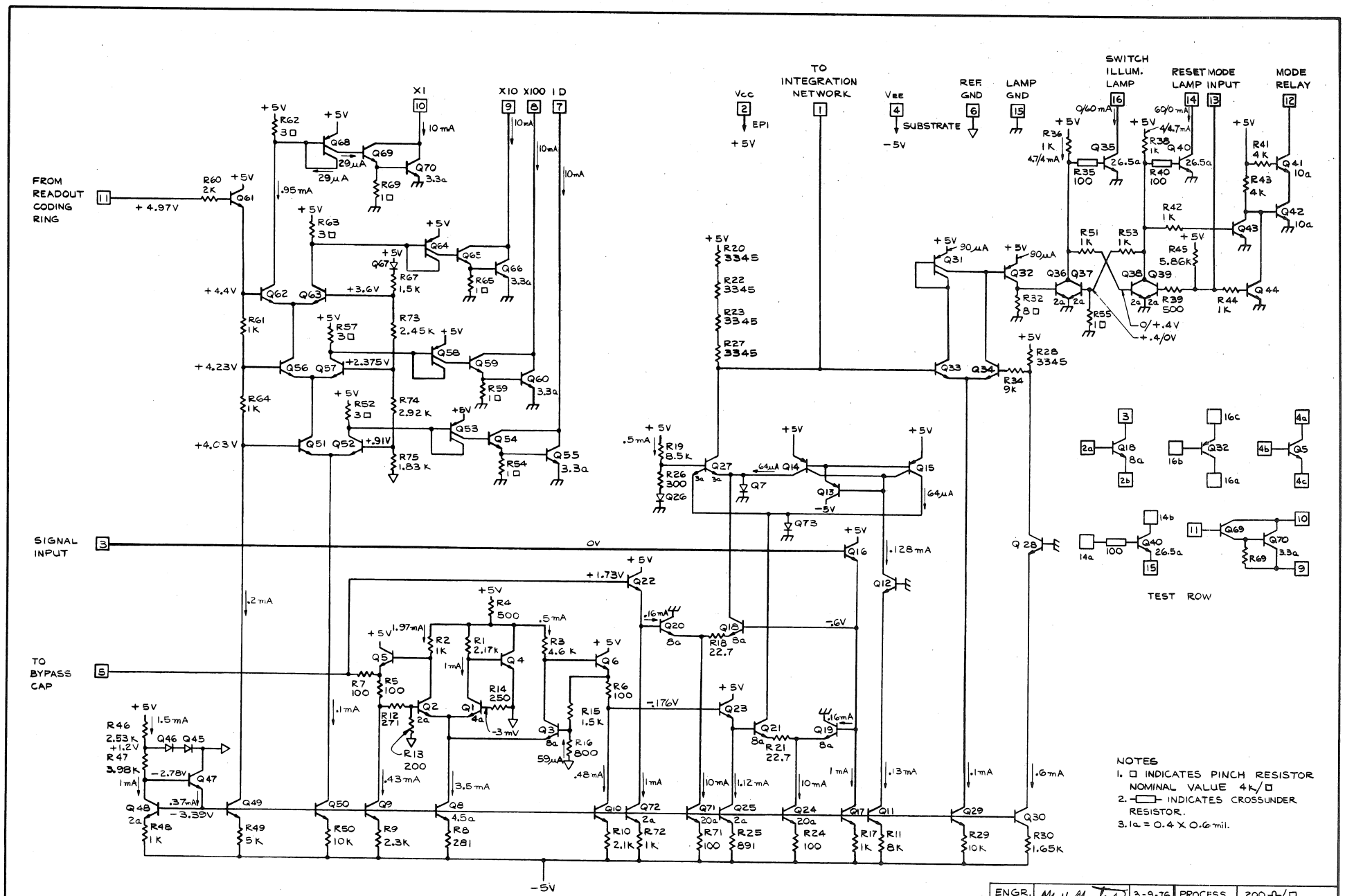
Power Supply: V_{CC} + 5
V_{EE} - 5 volts.

Package: 16 Minipac

Designer: John Addis

ICE Contact: Mike Metcalf

Instrument Usage: 485 (2)
4851 (2)
4852 (2)



ENGR.	M. H. Mulder	3-9-76	PROCESS	200 Ω/□
DWN. BY	S. POLENDEY	2-1-76	PACKAGE	16 PIN MINIPAC
CHK. BY	Linda Berg	6-1-76	DIE SIZE	60 mil X 60 mil
TYPE	MONOLITHIC	PROBE LOGIC & INPUT PROTECTION		M094B
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0070-00		

X. 2.

IN Production
By CER

M096F 203-0096-00 LOGIC PROBE LOGIC

Description:

M096 is used only with H116 logic probe substrate. Several components necessary for proper functioning are contained on the H116. The main input is connected to two voltage comparators set at different levels. Each comparator is coupled to a 60 mA lamp driver and a mono=stable multi-vibrator that allows short pulses to activate the lamps for a minimum of 100 m sec. An independent 1.34 volt temp. comp. reference maintains a 4.0 volt regulated power supply to run the reference dividers in the voltage comparator circuits.

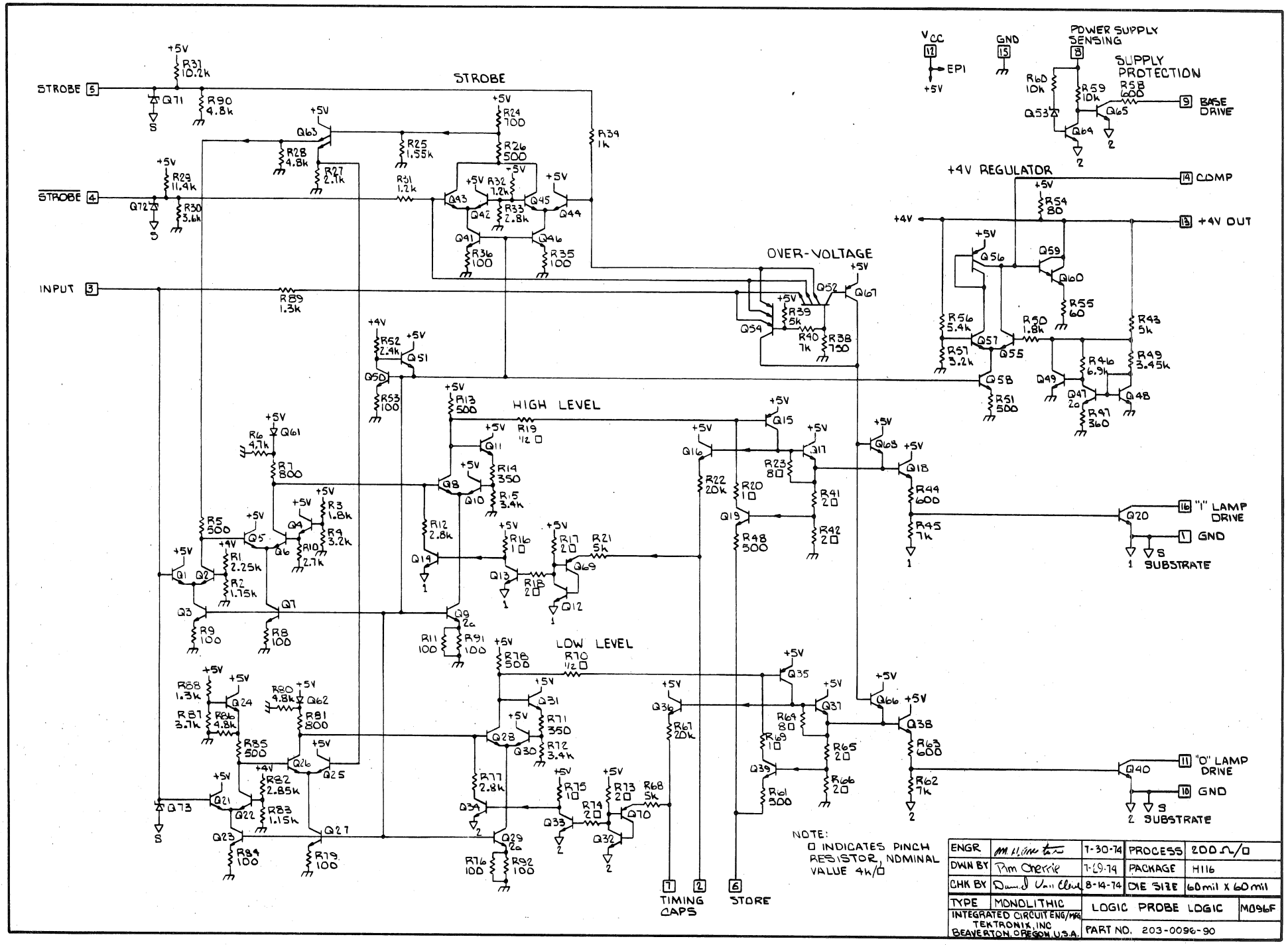
A strobe and $\overline{\text{strobe}}$ inputs also operate comparator circuits with a single 1.4 volt decision point. The entire function of the main input can be gated on or off with these inputs. A separate block of circuitry turns both lamp drivers on when any input is over-voltaged either positive or negative.

Package: See H116

Designer: Mike Metcalf

ICE Contact: Mike Metcalf

Instrument Usage: Logic Probe (1)


STROBE
STROBE
INPUT
STROBE
HIGH LEVEL
LOW LEVEL
OVER-VOLTAGE
+4V REGULATOR
POWER SUPPLY SENSING
SUPPLY PROTECTION
BASE DRIVE
COMP
+4V OUT
"1" LAMP DRIVE
GND
SUBSTRATE
"0" LAMP DRIVE
GND
SUBSTRATE
TIMING CAPS
STORE
NOTE:
□ INDICATES PINCH RESISTOR, NOMINAL VALUE 4k/□
ENGR
DWN BY
CHK BY
TYPE MONOLITHIC
INTEGRATED CIRCUIT ENG/MFG
TEKTRONIX, INC
BEAVERTON, OREGON, U.S.A.
T-30-74
T-29-74
8-14-74
PROCESS 200Ω/□
PACKAGE H116
DIE SIZE 60 mil X 60 mil
LOGIC PROBE LOGIC
M096F
PART NO. 203-0096-90

XI. DISCRETE DEVICES

D32 (Fabricated with D45 Mask)

204-0677-90 Schottky diode chip.
Die Size: 0.015 x 0.015 in.

Electrical Parameters:

Parameter	Conditions	Typical	Min.	Max.
R_f	I_f = 10 mA	5Ω		8Ω
C	0 bias, 1 MHz	0.5 pF		0.8 pF
V_B	1 μA, 25°C	5 V	3V	

Maximum allowable forward current: 50 mA

Uses:		
	152-0646-00	2 diode mixers
	152-0646-02	
	119-0338-04	Hybrid for 7L12
	119-0510-01	Hybrid for 7L13
	155-0136-00	Hybrid for TR502
	155-0133-00	Hybrid for TR502
	155-0170-00	Comparator hybrid for R7612D
	H548	Pulse Generator hybrid for CG551P

ICE/ICM Contact Krishna Verma/Hal Lillywhite

D058C

A Tek made transistor (NPN) used in the H125. It will carry a reasonably high current (100 to 120 mA) and has an f_T near 900 MHz.

BETA (120 mA & 4.V.)	I_{CES} (at 5 V.)	BV_{CEO} (at 1 mA)	BV_{CBO} (at 1 mA)	f_T
>40	<70 μA	>35V	>50 V	∿900 MHz

Designer: Mike Dickman

ICE Contact: Krishna Verma

D075D

A Tek made transistor (NPN) used in the 7L12 and 7L13 Oscillators and may be used as an amplifier in the H101. It has an output capacitance (C_{OB}) of about 0.8 pf at 6 V and an f_T of about 3 GHz.

BETA (5 ma & 5 V)	BV_{CBO} (at 1 mA)	LV_{CEO} (at 1 mA)	f_T	C_{OC} (at 6 V)
100	15 V	8 V	3 GHz	0.8 pf

Designer: Mike Dickman

ICE Contact: Krishna Verma

D84 Tear Tab Diode Schottky Diode Chip

204-0553-90 Die Size: 0.030 x 0.045 in.

Electrical Parameters:

Parameter	Conditions	Typical	Min.	Max.
R_f	I_f = 10 mA	8Ω		20 Ω
C	0 bias, 1 MHz	0.1 pF		
V_B	1 μA	8 V	5 V	

Maximum allowable forward current: 11 mA

Uses: 155-0053-00 plug gate for S-6

ICE/ICM Contact Krishna Verma/Hal Lillywhite

D102

A Tek made transistor (PNP) used as a protection device in the H116 for the M096. It will carry 150 mA at 5 V and has a very low leakage current.

BETA (150 mA & 5 V)	I_{CES} (at 25 V)	BV_{CEO} (at 100 μA)	BV_{CBO} (at 100 μA)
>40	<50 nA	>32 V	>32V

Designer: Mike Metcalf

ICE Contact: Krishna Verma

D113C

A Darlington photo transistor made at Tek using the standard 200 Ω/sq. IC process. The emitter is internally shorted to the substrate while the collectors are isolated so that it may be scribed into common emitter arrays. The device is normally operated open base but a base contact pad is provided. The device responds to visible and infrared radiation with a peak efficiency around 0.7μm.

Composite BETA (6V, 1mA):	1600 to 10000
I_{CEO} (DARK, V_{CE} = 8V)	$\leq$ 0.1μA
BV_{CEO} (10μA) Typical	= 15V
I_{MAX}	$\geq$ 5mA
V_{CESAT} (1mA) Typical	= 1.1V

D113C is 35 mil by 45 mil
D113B is 35 mil by 35 mil
D113A is 35 mil by 35 mil, but not Darlington.

Designer: Bob Nordstrom

ICE Contact: Krishna Verma

D143

Description:

This device was designed as a target for the T7610 EBS Digitizer tube, which is used in the 7612D Waveform Digitizer instrument. The die is approximately 250 x 40 mils. in size and contains 10 adjacent diodes, each 230 mils. long by 1.26 mils. wide, formed by a boron diffusion on an n-type epitaxial substrate. The active area of the diodes is covered by a pattern of thick and thin aluminum in the form of a digital gray code.

For the Digitizer application, die are attached to an alumina substrate which is mounted on a special header and sealed to an electron tube. In operation the diodes are reverse biased and bombarded by an electron beam. An output signal is obtained from a diode when the beam penetrates a thin metal area. The combined outputs of all the diodes provides an 8 bit digital code which is dependent on the beam position.

Specification

Forward bias (at 1mA)	1 V maximum
Reverse bias breadown (at 1 μA)	30 V minimum
Reverse leakage (20V bias)	30 nA maximum
Interdiode leakage (at 10V)	100 nA maximum
Diode capacitance (11.5V bias)	5 pF maximum

ICE Contact: Ray Hayes

D156

A Tek made transistor (NPN) for high voltage, common base applications requiring a gain bandwidth product of 1 GHz.

P_D	f_t	C_{CB}
V_{CE} = 30 volts	V_{CE} = 14 volts	
T_j = $\leq$200°C	I_c = 160 mA	V_{CB} = 4 volts
3 watts (Guaranteed safe operating area.)	1 GHz	2.5 pf

Designer: Krishna Verma

ICE Contact: Krishna Verma

D180 NPN TRANSISTOR

Description:

The D180 is a Tek made power (NPN) transistor. It has a totem pole configuration for Z axis drive in 7104 and z-axis drive for RASCAL (IDG).

DC	RF
BV_{CBO} = 150V	f_T = 500 MHz--1.0 GHz
I_c = 150mA	t_r = 700ps in 7904 VERTICAL AMPLIFIER
C_{CB} = 2.0pF at 10V	
LV_{CEO} = 90V	
h_{fe} (5V, 100mA) = 30	

Safe operating are ∿ 5 watts

Designer: Krishna Verma

ICE Contact: Krishna Verma

D185

LOW SIGNAL MICROWAVE TRANSISTOR

Description:

The D185 is a Tek made low signal microwave transistor (NPN). It has a low noise level and is suitable for microwave amplifiers and oscillators.

DC		RF	
BV_{CBO}	= 25	f_T	= 8 GHz
I_c	= 40mA	f_{max}	= 19 GHz
LV_{CEO}	= 12V	NF	= 2.5 dB at 2 GHz
C_{CB}	= 0.4 pF at 10V		= 3.8 dB at 4 GHz
		$\|S_{21}\|^2$	= 10 dB at 2 GHz
			= 4 dB at 4 GHz

Designer: Krishna Verma

ICE Contact: Krishna Verma

D186 MICROWAVE TRANSISTOR

Description:

The D186 is a Tek made microwave transistor (NPN) used in the TR501/502. It has a low noise level.

DC		RF	
BV_{CBO}	= 25V	f_T	= 7.5 GHz
I_c	= 80mA	f_{max}	= 18 GHZ
C_{CB}	= 0.9pF at 10V	NF	= 2.6 dB at 2 GHz
LV_{CEO}	= 12V		= 4.3 dB at 4 GHz
		$\|S_{21}\|^2$	= 9 dB at 2 GHz
			= 3 dB at 4 GHz

Designer: Krishna Verma

ICE Contact: Krishna Verma

D206

HIGH CURRENT BIPOLAR TRANSISTOR

Description:

The D206 is a npn high current bipolar silicon transistor. It is designed and developed as a CCD clockdriver for fast clock rate. However, this device can be used in microwave power amplifier and oscillator application.

DC	RF
BV_{CBO} = 35V	f_t (5V, 150mA) ∿ 4 GHz
I_c = 400mA	
LV_{CEO} = 15V	
C_{CB} (at 4V) = 7 pF	

Designer: Krishna Verma

ICE Contact: Krishna Verma

APPENDIX #I: Circuit Number vs Tek Part Number

M001	155-0009-00
M004	155-0010-00
M012	155-0011-00
M015	155-0012-00
M018	155-0028-00
	155-0028-01
	155-0042-02
	155-0042-03
M019	155-0014-01
M020	155-0015-01
M022	155-0013-00
	155-0013-01
M025	155-0017-00
M026	155-0018-00
M027	155-0019-00
M028	155-0020-00
M029	155-0021-01
M033	155-0004-01
M034	155-0005-00
M035	155-0006-01
M036	155-0022-00
	155-0022-01
M038	155-0007-01
M039	155-0008-01
M042	155-0056-00
M045	155-0038-01
	155-0038-02
M048	155-0033-00
M050	155-0047-00
M052	155-0048-00
	155-0048-01
	155-0055-00
M053	155-0035-00
	155-0057-00
	155-0116-00
M055	155-0032-00
	155-0032-01
M059	155-0090-00
	155-0090-01
	155-0090-02
M061	155-0034-00
M065	155-0050-01
M068	155-0051-00
M071	203-0071-00
M077	155-0059-00
M080	203-0080-00
M083	155-0061-00
M084	155-0078-00
	155-0078-01
	155-0078-02
	155-0078-03
	155-0078-04
	155-0078-05
	155-0078-06
	155-0078-07
M089	203-0089-00
M091	155-0067-02
M094	155-0076-00
M095	155-0091-00
M096	203-0096-00
M101	155-0106-00
M102	203-0102-00
M105	155-0083-00
M112	155-0117-00
M115	155-0118-00
M116	
M119	155-0110-00
M120	155-0109-00
M121	155-0126-00
M122	155-0150-00
M123	155-0119-00
M124	155-0144-00
M127	155-0114-00
M130	203-0130-00
M131	155-0121-00
M132	155-0122-00
M133	155-0123-00
M134	
M138	155-0124-00
M150	
M151	155-0145-00
M159	155-0151-00
M160	155-0023-00
M161	155-0024-00
M162	155-0025-00
M163	155-0026-00
M164	155-0027-00
M165	155-0086-00
M166	155-0087-00
M167	155-0088-00
M169	155-0104-00
M170	155-0105-00
M171	155-0135-00
M182	155-0146-00
	155-0147-00

APPENDIX #II: Tek Part Number vs Circuit Number

155-0004-01	M033
155-0005-00	M034
155-0006-01	M035
155-0008-01	M039
155-0009-00	M001
155-0010-00	M004
155-0011-00	M012
155-0012-00	M015
155-0013-00	M022
155-0013-01	M022
155-0014-01	M019
155-0015-01	M020
155-0017-00	M025
155-0018-00	M026
155-0019-00	M027
155-0020-00	M028
155-0021-01	M029
155-0022-00	M036
155-0022-01	M036
155-0023-00	M160
155-0024-00	M161
155-0025-00	M162
155-0026-00	M163
155-0027-00	M164
155-0028-00	M018
155-0028-01	M018
155-0032-00	M055
155-0032-01	M055
155-0033-00	M048
155-0034-00	M061
155-0035-00	M053
155-0038-01	M045
155-0038-02	M045
155-0039-00	M025
155-0042-02	M018
155-0042-03	M-18
155-0047-00	M050
155-0048-00	M052
155-0048-01	M052
155-0049-01	M079
155-0050-01	M065
155-0051-00	M068
155-0055-00	M052
155-0056-00	M042
155-0057-00	M053
155-0059-00	M077
155-0061-00	M083
155-0067-02	M091
155-0076-00	M094
155-0078-00	M084
155-0078-01	M084
155-0078-02	M084
155-0078-03	M084
155-0078-04	M084
155-0078-05	M084
155-0078-06	M084
155-0078-07	M084
155-0083-00	M105
155-0086-00	M165 (R)
155-0087-00	M166 (C_1)
155-0088-00	M167 (C_2)
155-0090-00	M059
155-0090-01	M059
155-0090-02	M059
155-0091-00	M095
155-0104-00	M169
155-0105-00	M170
155-0106-00	M101
155-0109-00	M120
155-0110-00	M119
155-0114-00	M127
155-0116-00	M053
155-0117-00	M112
155-0118-00	M115
155-0119-00	M123
155-0121-00	M131
155-0122-00	M132
155-0123-00	M133
155-0124-00	M138
155-0126-00	M121
155-0135-00	M171
155-0144-00	M124
155-0145-00	M151
155-0146-00	M182
155-0147-00	M182
155-0150-00	M122
155-0151-00	M159
203-0071-00	M071
203-0080-00	M080
203-0089-00	M089
203-0096-00	M096
203-0102-00	M102
203-0126-00	M126
203-0130-00	M130