Tektronix®

PM 106/PM 107

PERSONALITY MODULE FOR 8086/8088 MICROPROCESSORS

INSTRUCTION MANUAL

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PM 106/PM 107

PERSONALITY MODULE FOR 8086/8088 MICROPROCESSORS

INSTRUCTION MANUAL

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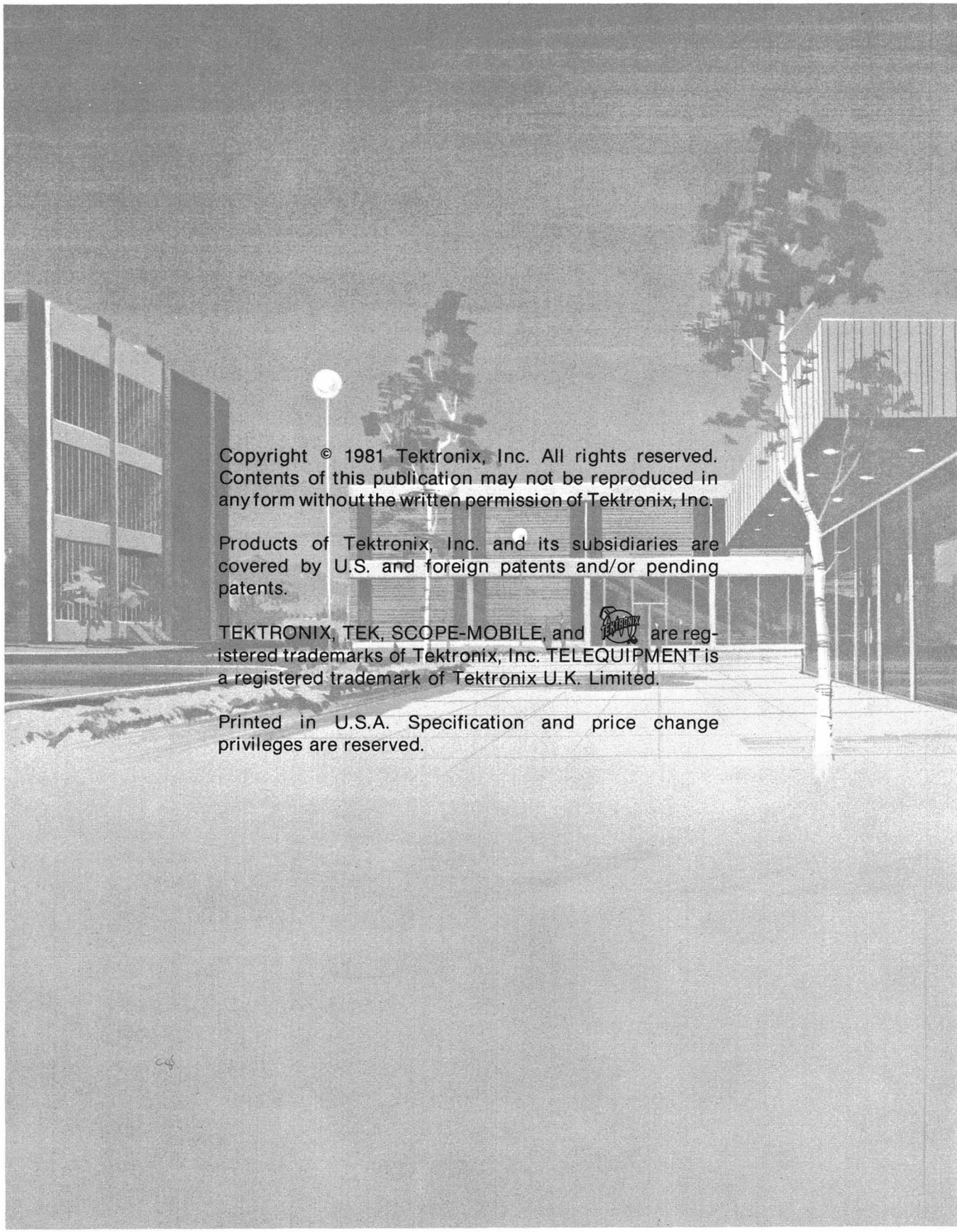

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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

In This Manual

This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment

DANGER — High voltage.

Protective ground (earth) terminal.

ATTENTION — refer to manual.

Power Source

This product is intended to operate from a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power module power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power module power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Fuse

To avoid fire hazard, use only the fuse of correct type, voltage rating and current rating as specified in the parts list for your product.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Operate Without Covers

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.

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SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

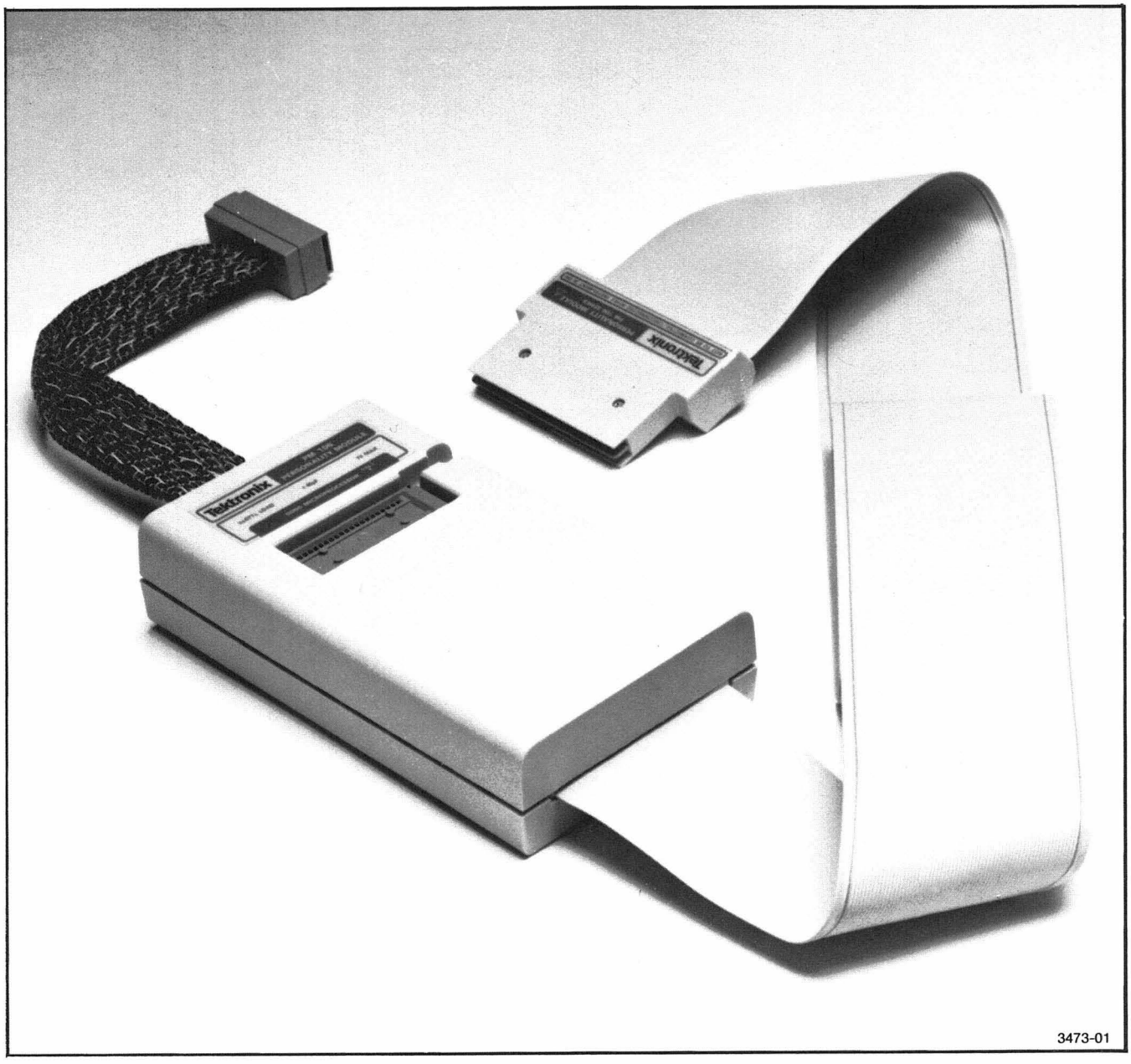
Use Care When Servicing With Power On

Dangerous voltages may exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate in a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.



The PM 106 Personality Module used with the 8086 Microprocessor.

INTRODUCTION

ABOUT THIS MANUAL

This manual describes the operation and servicing of the PM 106 Personality Module which is used with the 8086 microprocessor, and the PM 107 Personality Module which is used with the 8088 microprocessor.

The first part of this manual, the operator's portion, provides an overview of the module, connection instructions, and operating information which supplements that in the 7D02 Operator's manual by personalizing it to the PM 106/107 Personality Modules and the 8086/8088 microprocessors.

The second part of this manual, the service portion, is found after the colored divider page. It contains maintenance information, circuit descriptions, diagnostics, schematics, and parts lists, and is intended to be used only by qualified service personnel. Refer to the table of contents for the specific location of information.

This manual makes frequent reference to the "logic analyzer"; this means the 7D02 Logic Analyzer. It is assumed that the reader has access to Operator's and Service manuals for the 7D02. This manual also makes frequent reference to *The 8086 Family User's Manual*, an Intel publication. The reader will also need access to this manual to understand the PM 106 and the PM 107.

OVERVIEW OF THE PERSONALITY MODULES

The PM 106 and PM 107 "personalize" the logic analyzer for use with the 8086 and 8088 microprocessors. They contain firmware which modifies the display and diagnostics of the logic analyzer for use with their microprocessors. Hardware in the personality modules isolates, buffers, latches, and, in many cases, translates the data on the bus of an 8086/8088-based system under test (SUT) into a form which is recognizable by the 7D02.

The personality module passively monitors the system under test; it does not interfere with processor operation or supply its own program, it only collects data and interprets it after it is stored.

Physically, the personality modules consist of a plastic pod containing three circuit boards. A four foot ribbon cable with a 64 pin connector serves as the interface to the logic analyzer, while a twisted pair, woven cable with a 40-pin connector connects the PM 106/107 to the system under test. A zero insertion force (ZIF) socket receives the microprocessor itself.

OPERATING INSTRUCTIONS

INTRODUCTION

This section of the manual provides information concerning the operation of the PM 106/107 Personality Module.

Storing the Personality Module

Keep the personality module in a clean area where the temperature remains between −62°C and +85°C. Humidity should not exceed 95%, non-condensing. The personality module should not be taken above 50,000 feet.

When storing the module, protect the microprocessor replacement plug with the plastic protector, Tektronix P/N 200-2445-00. This prevents damage to the pins during storage and protects the personality module from static electricity.

Connecting the Personality Module to the Logic Analyzer

CAUTION

Always be certain to turn OFF the mainframe (logic analyzer) power before connecting or disconnecting any personality module. Also, always be sure to turn OFF the power to the system under test before removing the microprocessor and installing the replacement plug. Failure to take these precautions may result in permanent damage to the logic analyzer, the personality module, or the system under test.

Turn off the mainframe power and insert the ribbon connector labeled PERSONALITY MODULE - PM 100 SERIES into the receptacle on the logic analyzer with the same name.

Connecting the Personality Module to the System Under Test (SUT)

1. Turn off the power to the logic analyzer and the SUT.

2. Ground yourself to drain static electricity.

3. Remove the microprocessor from the SUT and install it in the ZIF socket of the personality module. Be sure to insert it correctly, with pin 1 of the microprocessor toward the lever of the ZIF socket.

NOTE

The low profile DIP clip should not be used with the PM 106 or PM 107.

4. Plug the personality module microprocessor replacement plug into the microprocessor socket of the SUT. Make sure that pin 1 of the replacement plug goes to pin 1 of the SUT socket. Pin 1 of the microprocessor plug is marked with a notch and an arrow.

5. Turn on power to the logic analyzer and the SUT, and reset the SUT.

NOTE

Because of the set-up and hold times of the 7D02 and the PM 106/107, several system parameters are constrained. Refer to the Specification Section of this manual and to The 8086 Family User's Manual (an Intel publication).

Operation

To understand the operation of the PM 106/107 Personality Modules, the operator must also be familiar with the operation of the 7D02 Logic Analyzer and the 8086 family of microprocessors. Refer to the 7D02 Operator's Manual Tektronix P/N 070-2918-00) and *The 8086 Family User's Manual* (an Intel publication).

NOTE

For use with the PM 106 or PM 107, the 7D02 must be equipped with the Expansion Option. The PM 106 and PM 107 may be used with or without the Timing Option. Displays in this section are shown without the Timing Option, however.

Many of the displays shown in the 7D02 Operator's Manual will vary when the logic analyzer is used with the PM 106 or PM 107 because the displays in the 7D02 manuals were based on a different microprocessor and personality module. The operator's portion of this manual should therefore be viewed as a personalized supplement to, and in some cases substitute for, the 7D02 Operator's Manual.

The Instruction Stream Queue. The 8086/8088 actually consists of two processors working in tandem. The execution unit executes instructions, while the bus interface unit pre-fetches instructions, reads operands and writes results. The bus interface unit contains an instruction stream queue which can hold up to six bytes of instructions in the case of the 8086, four in the case of the 8088. The actual number of bytes in the queue varies with operating circumstances. (Refer to *The 8086 Family User's Manual*, an Intel publication.)

Because of this queue, a particular instruction appears on the bus at one time, while it is going into the queue, and is executed out of it at a later time (or not at all). In order to disassemble the mnemonics the PM 106 or PM 107 must therefore have some way of finding out when the first byte of an instruction is executed. This is accomplished by using information about the queue level and two additional lines which indicate when the last or second-to-last byte executed is a fetch of a new instruction.

Monitoring The Bus. The 7D02 - PM 106/107 system monitors activity on an 8086 or 8088 system bus. Data on the bus may or may not be relevant. For example, a particular instruction may be pre-fetched and yet never executed. At acquisition time, the 7D02 - PM 106/107 system has no way to determine which instructions will later be executed. This is the case because all triggering and qualification are done in real time relative to data on the bus. Execution of an instruction occurs later, if at all. Consequently, it is possible to trigger the logic analyzer on an instruction that is never executed. This is likely to occur if that instruction appears just past a loop; it will be recognized by the 7D02 as it enters the instruction stream queue, even though it is not to be executed because of a program jump.

In the absolute mode, this bus activity is displayed with little interpretation. In the mnemonic mode, post-processing algorithms are employed to decode the instructions that were actually executed. These mnemonics are displayed along with their operands. In those cases where there is insufficient information in memory to guarantee accurate disassembly, a question mark is displayed before the mnemonic along with asterisks where the operand would have appeared. Heavy use of the data qualification capabilities of the 7D02 (the QUALIFY command) can lead to erroneous data or loss of data which is essential to this post-processing procedure.

The Word Recognizer

ADDRESS Field. The 8086 can move data in two byte segments. In this case only the even byte is addressed; the odd address does not appear on the address bus and will not be recognized by this field. In other cases, such as the case of a jump or a non-[CODEFETCH] read or write to an odd address, odd addresses do occur on the bus and will be recognized.

DATA Field. The byte of data on the right is associated with an even address. The byte on the left is associated with the next address, an odd address. Transfers of 16 bits of valid data on one cycle only occur from word boundaries, i.e., even addresses. If, as a result of an execution transfer, a CODEFETCH occurs from an odd address boundary, an 8 bit transfer takes place. This is then followed by normal 16 bit transfers. If a 16 bit data value is split across a word boundary, it will be read or written as two 8 bit transfers (16 bit data values are stored with the least significant byte at the low address and the most significant byte at the high address).

[CODEFETCH]. This control line is extremely important to understanding word recognizer operation and the significance of data displays. When CODEFETCH = 1, the 8088 (or 8086) is moving one (or two) bytes of instruction data into the instruction stream queue. Note that CODEFETCH is true for any byte of an instruction, not just the opcode. When CODEFETCH = 0, the bus is in use for input, output, memory read or memory write.

[CODEFETCH] has additional significance to PM 106/107 operation, however. It controls the meaning of three other control lines from the PM 106/107 to the 7D02: BHE [/QDUMP], R/W [LST-F], and M/IO [2LST-F]. With CODEFETCH = 0, these lines have their first meaning. When CODEFETCH = 1, these lines have the meaning shown in brackets. On the 7D02 screen display, signals which are active when low are shown prefaced by a '/'. Low going signals not displayed on the screen are indicated with a bar, e.g., $\overline{SIG}$.

BHE [/QDUMP] (BHE, PM 106 Only). When [CODEFETCH] is low, this line carries byte high enable, BHE, information. When [CODEFETCH] is high, this line carries /QDUMP information.

BHE operates in conjunction with A0 to establish whether the high byte, the low byte, or the whole word is valid data.

When [CODEFETCH] is high, a low on the A0 line means that the data should be interpreted as a full word (high and low bytes), when A0 is high only the high byte is valid.

When [CODEFETCH] is low, Table 2-1 defines which bytes contain valid data.

Table 2-1
VALID AND INVALID DATA BYTES

BHE	A0	Valid	Displayed As
0	0	Low byte	L
0	1	Error	?
1	0	Both bytes	W
1	1	High byte	H

/QDUMP is high when the 8086/8088 has just emptied its queue and pulled in the first byte (or bytes) of the next instruction.

In the PM 107, BHE is permanently set low while CODEFETCH is low.

Caution must be applied in using /QDUMP for word recognition. This is because the coincidental occurrence of a /QDUMP and an interrupt will generate QFIL? indications in the STATUS column of the absolute display, while the word recognizer sees these QFIL?s as /QDUMPs.

R/W [LST-F]. When [CODEFETCH] is low, this line indicates whether the current operation is a memory or input-output read or write. When [CODEFETCH] is high, this line will be high when the last byte executed out of the instruction stream queue of the 8086/8088 was the first byte (opcode) of an instruction.

M/IO [2LS-F]. When [CODEFETCH] is low, this line indicates whether the current operation was a memory access or an input-output access. When [CODEFETCH] is high, this line is high when the second-to-last byte executed out of the instruction stream queue was the first byte (opcode) of a new instruction, a Fetch.

Note

The preceeding four lines are stored in the acquisition memory and are therefore available for absolute and mnemonic display. The following two lines are not stored and are not available for display purposes.

MIN/MAX MODE. This signal can be used for locating and analyzing transitions between minimum and maximum modes in systems which are capable of dynamically switching between them, and for finding glitches on this line in a system which is supposed to be operating continuously in one of them. In either case, the trigger section, user clock qualification delay-by field should be set to 0. Note, however, that this will cause incorrect mnemonic disassembly because extra cycles will be stored.

HOLD ACK. This line goes high whenever the 8086/8088 grants a request in response to an external HOLD in the minimum mode or request grant 0 or request grant 1 in the maximum mode.

Setting this line in the word recognizer to 1, the trigger delay-by field in the user clock qualification area to 0, and C8 and C9 in the user clock synthesis field to X, can give information about the bus traffic occurring during a time when another device has been granted the bus.

QLEVEL. This is an octal field which can be set to recognize any queue level from 0 to 6 in the PM 106, and 0 to 4 in the PM 107.

IRQ. This line is an ORed combination of INTR and NMI. (It indicates the request for an interrupt, not the acknowledgment.)

EXT TRIG IN. This line is from the TRIG IN jack on the logic analyzer.

Qualify Command

Qualifying on [CODEFETCH] alone will produce correct disassembly and is extremely useful. However, excessive use of data qualification can prevent meaningful mnemonic disassembly because the disassembly process requires continuous instruction code data.

Trigger Commands

User Clock Qualification. The default values are FALLING EDGE OF CLOCK and Xs for the C9-C4 ANDed clocks field.

The ANDed clocks are used to only clock data into memory on cycles in which these lines match the user defined values. Changing them from the default value of X (don't care) may cause incorrect disassembly. The C9-C4 (ANDed clocks) correspond to the following control lines.

Line	Name
C9	$\overline{\text{WAIT}}$
C8	$\overline{\text{T1}}$ (Machine State 1)
C7	HOLDACKnowledge
C6	$\overline{\text{CODEFETCH}}$
C5	HOLDACKnowledge
C4	MIN/$\overline{\text{MAX}}$

User Clock Synthesis. The default values are DELAY CLOCK BY 2, C6=X, C8=0, C7=X, and C9=0. These values cause storage on the falling edge of clock cycle T3, which is when data and status lines are valid. Use of any other values may disrupt mnemonic disassembly.

Entering a delay-by-0 allows storage of data on every clock pulse. Using a delay-by-0 is important for capturing events which do not last through other machine states. However, using delay-by-0 produces redundant data and produces meaningless information in the mnemonic mode.

HALTing the System Under Test. The PM 106/107 contains an optional HALT feature which allows the user to stop the program when a trigger occurs. If the strapping is altered to include this feature, selection of SYSTEM UNDER TEST HALT in the trigger section causes the PM 106/107 to put a pulse on the Request Grant (or Hold) line, stopping the microprocessor. When the processor has stopped, it puts a grant signal on the same line from which it received the request. The processor will then interpret the next pulse on that line as a release. It will not be able to distinguish another request (from some other device) from a release coming from the 7D02.

For example, the 7D02 Logic Analyzer requests the bus when the acquisition memory is full. The 8086/8088 grants it. The 7D02 sends a release when the START button is pushed again. If the processor has been reset before the release comes, the processor will begin running again. The release from the 7D02 START command then will cause the 8086/8088 to stop instead of start.

Because misuse of this feature can cause bus contention in a user's system, the PM 106/107 comes with jumper straps in place which disable it. If, after reading and appreciating the significance of this explanation of the dangers and difficulties of using the HALT function, the reader wishes to use it, refer to the Troubleshooting and Maintenance section of this manual for information on strapping and how to change it.

If a LOCKed instruction sequence is occurring when the 7D02 requests the bus as part of a HALT sequence, the 8086/8088 will not grant the bus until that instruction sequence has been completed. In the case of a LOCKed REPEated instruction, this may be many machine cycles.

Triggering Past a Loop

Triggering on an event which occurs just past a loop is likely to occur on the first time through the loop rather than on the last time. This is because the 8086/8088 is pre-fetching instructions into the instruction stream queue. The 7D02 sees the instruction when it enters the queue, not when it leaves it. An instruction just past a loop is therefore seen every time the end of the loop is approached, not only when it is actually executed.

The simple solution is to trigger on an instruction more than the maximum queue level beyond the loop (6 for the 8086, 4 for the 8088).This simple solution does not work for complicated cases, such as nested loops or loops and jumps in very close proximity. The /QDUMP line in the word recognizer can be used to determine when an opcode has been reached by a jump rather than by being pre-fetched.

Absolute Data Displays

PM 106/107 Differences. The DATA column of the display is one byte wide for the PM 107, two bytes wide for the PM 106. The PM 106 display therefore includes a column which indicates with an H, an L, or a W which byte or bytes are valid.

Default Radices. All radices default to hexadecimal.

DATA Field (PM 106 Only). Data associated with even addresses appears on the right of the data display. Data associated with odd addresses appears on the left side of the DATA column of the display. Refer to H, L, W (PM 106 only) following.

Control Line Interpretation. Table 2-2 defines the significance of the major control lines and the corresponding STATUS indications in the absolute mode.

LST-F. This indication, called last fetch, means that the last byte executed out of the queue was the first byte of an instruction.

2LS-F. This indication, called second-to-last fetch, means that the second-to-last byte executed out of the queue was the first byte of an instruction.

L&2LS. This indication, called last and second-to-last, means that both the last and the second-to-last bytes executed out of the queue were the first bytes of instructions. (The first of these instructions must have only been one byte long.)

QFILL. This indication, queue fill, means that the third-, fourth-, fifth-, or sixth-to-last byte executed out of the queue was the first byte of an instruction.

Table 2-2
ABSOLUTE STATUS DERIVATION

Name - Line	[CODE FETCH] /C2	M/IO[2LS-F] C1	R/W[LST-F] C0	BHE[/QDUMP] A20
I/O W[a]	0	0	0	0
I/O W	0	0	0	1
I/O R	0	0	1	0
I/O R	0	0	1	1
MEM W	0	1	0	0
MEM W[b]	0	1	0	1
MEM R	0	1	1	0
MEM R	0	1	1	1
/QDUMP	1	0	0	0
QFILL	1	0	0	1
?(error)	1	0	1	0
LST-F	1	0	1	1
?(error)	1	1	0	0
2LS-F	1	1	0	1
?(error)	1	1	1	0
L&2LS	1	1	1	1

[a] **This case is displayed as HALT if A0 = 1 (PM 106 only).**
[b] **This case is displayed as INTA if A0 = 1 (PM 106 only).**

QFIL?. This indication occurs following the coincidental occurrence of a /QDUMP and an interrupt acknowledge. A queue fill is actually occurring, but the word recognizer will see a /QDUMP.

/QDUMP. This indicates a clearing of the queue caused by an interrupt, a RET, a CALL, or a JMP command. (The word recognizer will trigger on this for QFIL?s also.) /QDUMPs are only displayed on CODEFETCH cycles.

H, L, W (PM 106 only). These indications to the right of the STATUS column in PM 106 displays indicate which bytes of data are valid. H means that only the high byte, the one on the left, is valid. L means that only the low byte, the one on the right, is valid. The invalid byte shows data that happens to be on the bus at the time.

When [CODEFETCH] is high, a low on the A0 line means that the data should be interpreted as a full word (high and low bytes); when A0 is high only the high byte is valid.

When [CODEFETCH] is low, Table 2-3 indicates which bytes are valid.

Table 2-3
BYTE VALIDITY

BHE	A0	Valid	Displayed As
0	0	Low byte	L
0	1	Error	?
1	0	Both bytes	W
1	1	High byte	H

Q. This column of the display indicates the instruction stream queue level after the current bytes were pulled in and any executions out have occurred. The maximum queue level is 6 for the 8086 and 4 for the 8088.

I. This column indicates an interrupt request with a 1. (An interrupt request is caused by either INTR or NMI.)

Mnemonic Data Displays

Radices. All radices are hexadecimal and cannot be changed in the mnemonic mode.

ADDRESS. The mnemonic display generated by the PM 106 will occasionally contain two lines and two addresses

associated with one location number. This occurs whenever either of the bytes at that address is an opcode, the first byte of an instruction. The second address which is displayed never actually occurs on the bus; it is displayed for convenience.

DATA. In the mnemonic mode the PM 106 data display only contains relevant bytes of data. Bytes which were defined as invalid by BHE and A0 have been removed.

Multiple Lines at One Location. When one or two bytes at one location is an opcode, the first byte of an instruction, the mnemonic for that byte is displayed on a separate line of the display. (It is not possible to trigger on this address, since it does not appear on the bus.) Successive bytes of the same instruction are shown as CODEFETCHs with their hexadecimal value.

Because there is one instruction, TEST, whose operands may not fit on one line, there may sometimes be as many as three lines of display associated with one location.

Question Marks in the Display. When a **?** appears between the address and mnemonic in the display it means an opcode may not have been executed. The PM 106 ascertains this by tracking the opcode through the queue until it is executed or a queue dump or the end of memory is found. If the queue dump or end of memory is found first, the **?** is displayed. (Refer to the example programs toward the rear of this section.)

Asterisks in the Display. Asterisks in the OPERATION column indicate an illegal opcode, a legal opcode with an illegal operand, or insufficient data for the operand.

When an illegal opcode or operand occurs, three asterisks are displayed in place of the mnemonic and the hexadecimal value of the questionable instruction byte is displayed in parentheses.

When a queue dump or the end of memory occurs before the operand data is completely pulled into the queue, asterisks appear in the display (along with a question mark) in the operand field. The question mark appears before the mnemonic.

Missing Mnemonics. If an illegal opcode is executed, mnemonics for some opcodes may be missed. Due to the pre-fetch nature of the 8086/8088, the PM 106/107 may not disassemble the next opcode or opcodes. A similar lack of disassembly can occur at the beginning of memory if no LST-F, 2LS-F, or /QDUMP occurs for the opcode of the missing mnemonic.

INTA. This interrupt acknowledge indication occurs when there is a memory write with BHE and A0 high. No data is displayed.

HALT. This system halted indication occurs when there is an input-output write with BHE low and A0 high. No data is displayed.

CODEFETCH. This indication of instruction code occurs whenever CODEFETCH is high but the byte involved is not an opcode (the first byte of an instruction).

No Disassembly. This can occur when disassembly is impossible because a sequence of code as long as the 7D02 acquisition memory contains no instructions which generate a queue dump and no LST-F or 2LS-F occurs. No disassembly occurs as a result of certain types of user clock qualification or very long programs with a consistently high queue level and no transfers of control.

Mnemonic Format Differences (using Intel format)

B Suffixes. Many Intel mnemonics will appear on the logic analyzer display with a B suffix. This is additional information which distinguishes mnemonics which are applied to bytes from those which are applied to words. For example, ADC is Add-with-carry-word, while ADCB is Add-with-carry-byte.

 # Prefixes. Many Intel mnemonics will sometimes appear with a # in front of an operand. This means that operand is an immediate operand.

Brackets [ ]. Brackets have two uses: they surround all indirect operands and they also appear around registers used in indexed addressing.

CS:, ES:, DS:, and SS: Locations. In the PM 106/107 format these precede the instruction, coming on the line before, rather than showing up in the operands.

The S suffix indicates that an inter-segment instruction is being used.

A Note on IRQ Information

IRQ information is only displayed in the absolute mode, where it appears in the column labeled I.

@

Immediate - Display - Program

If this sequence of 7D02 commands is performed too quickly by the operator it may not result in a change of mode. This occurs because the display length must be increased after the IMMEDIATE button is pushed but before the PROGRAM button is. This problem is easily remedied by simply repeating the sequence of commands more slowly.

Examples

An 8088 Example. To illustrate the operation of the instruction stream queue and the method used by the 7D02 and PM 107 to disassemble it, the following example program is used.

Address	Code	Mnemonic
500	90	NOP
501	F6 E6	MULB DH
503	EB FB	JMP 00500
505	60	XX
506	90	XX
507	90	XX

When the logic analyzer is triggered on the first address of this subroutine, using 00500 in the address field and Xs everywhere else, the following is the display of the data in the absolute mode.

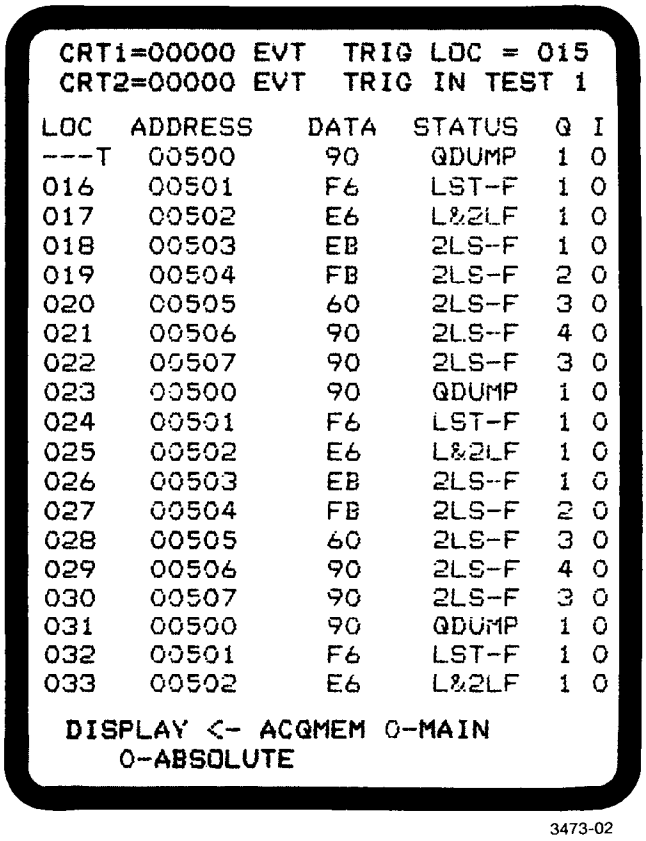


Figure 2-1. Absolute display of example program - 8088.

Notice that at the trigger location (the location which would be numbered 15), the first byte of our sample program appears along with a /QDUMP status indication which tells us that the queue was emptied at this point, just before the first byte of our program was pulled in. Consequently, the queue level, in the second column from the left, is now 1. Refer to Figure 2-1. Refer also to Figure 2-2, which illustrates the operation of the queue and can be used as a mental aid in figuring out how the PM 106 locates opcodes for disassembly.

At location 016 the next byte of the program has been pulled into the queue and the LST-F indication is telling us that the last byte executed out of the queue, 90, was an opcode. We know this because only one byte was executed and the absolute data display (refer to Figure 2-1) shows a LST-F in the status column.

At location 017 the next byte of our program appears in the DATA column of Figure 2-1 along with a 2LS-F indication in the status column. Notice, in Figure 2-2, that the queue level is 1. Therefore, we know that this byte is now the only one in the queue. The L&2LF indicates that the last and second-to-last bytes executed were both opcodes (the first bytes of an instruction). They are circled in Figure 2-2 to indicate that this location is the one at which the fact that these bytes are opcodes is established. With one byte entering the queue and the same level in the queue, one byte must have been executed.

NOTE

An opcode is the first byte of an instruction. Its location is identified by LST-F, 2LS-F, and L&2LF indications in the absolute display and is shown as its mnemonic in mnemonic data displays. Subsequent bytes are identified in the mnemonic display by CODEFETCH in the OPERATION column.

At location 018 a 2LS-F (second-to-last fetch) indicates that the byte which is 2 bytes plus the queue level bytes back must have been an executed opcode. One byte is pulled in each cycle and the queue level rose from 1 to 2, indicating that no bytes were executed this cycle. Counting back 2 + 1 bytes identifies the F6 at location 16 as the fetch. This is the same byte identified last time. The queue is being filled, but nothing is being executed out because of the time required by the execution unit (EU) for the multiplication operation.

At location 019 we have another 2LS-F status indication and the queue level has risen to 2. The EU is still busy with the multiplication operation.

At location 20 the queue level column in Figure 2-1 has risen to 3. Since one byte is pulled into the queue on each execution cycle, this indicates that no byte was executed out of the queue.

7D02 MEMORY LOCATION NUMBER		15	16	17	18	19	20	21	22	23	24	25
8088 QUEUE CONTENTS	IN	-	-	-	-	-	-	90	-	-	-	
		-	-	-	-	-	60	60	90	-	-	-
		-	-	-	-	FB	FB	FB	90	-	-	-
	OUT	90†	F6	E6	EB	EB	EB	EB	60	90†	F6	E6
LAST FETCHED (LST-F)		?	90*	F6*	E6	E6	E6	E6	FB	-	90*	F6*
SECOND-TO-LAST FETCHED (2LS-F)		?	?	90**	F6**	F6**	F6**	F6**	EB	-	-	90**
THIRD-TO-LAST FETCHED		?	?	?	90	90	90	90	E6	-	-	-
FOURTH-TO-LAST FETCHED		?	?	?	?	?	?	?	F6	-	-	-
NUMBER OF BYTEG EXECUTED		?[D]	1	1	1	0	0	0	2	?[D]	1	1

† Identified as first byte of an instruction by QDUMP
* Identified as first byte of an instruction by LST-F
** Identified as first byte of an instruction by 2LS-F
[D] Queue dump occurred

3473-03

Figure 2-2. Queue status during example program execution - 8088.

We can continue using this process to locate and identify opcodes, but once the PM 106/107 finds the beginning of one instruction by using this method, the beginning of the next instruction is found from the number of bytes associated with the last instruction.

In location 20 of Figure 2-3, note the triple asterisks where the mnemonic would appear. These indicate that the 60 shown in parenthesis was an illegal opcode. Examination of locations 21 through 23 in Figures 2-1 and 2-2 reveals that this byte of code is never executed; rather, it is dumped along with two 90s at location 23.

The 90s which entered the queue at locations 21 and 22 in Figure 2-1 are not displayed as NOPs, as was the one at location 15, but rather they appear as 90 CODEFETCH in Figure 2-3. This is because the number of bytes which were part of the illegal opcode is not known.

An 8086 Example. The following example illustrates the operation of an 8086 instruction stream queue and the method used by the 7D02 and the PM 106 to perform disassembly.

Address	Code	Mnemonic
100	90	NOP
101	F6 E6	MULB DH
103	EB FB	JMP 00100
105	60	XX
106	90	XX
107	90	XX

```
CRT1=00000 EVT  TRIG LOC = 015
CRT2=00000 EVT  TRIG IN TEST 1

LOC ADDRESS   OPERATION
---T00500 NOP
016 00501 MULB DH
017 00502  E6   CODE FETCH
018 00503 JMP 00500
019 00504  FB   CODE FETCH
020 00505?*** (60)
021 00506  90   CODE FETCH
022 00507  90   CODE FETCH
023 00500 NOP
024 00501 MULB DH
025 00502  E6   CODE FETCH
026 00503 JMP 00500
027 00504  FB   CODE FETCH
028 00505?*** (60)
029 00506  90   CODE FETCH
030 00507  90   CODE FETCH
031 00500 NOP
032 00501 MULB DH
033 00502  E6   CODE FETCH

DISPLAY <- ACQMEM 0-MAIN
   1-MNEMONIC
```

3473-04

Figure 2-3. Mnemonic display of example program - 8088.

When the logic analyzer is triggered on the first address of this subroutine, Figure 2-4 is the data display in the absolute mode.

We can use the absolute data display and a mental or pictorial construct of the instruction stream queue of the 8086, as shown in Figure 2-5, to understand how the mnemonic display is generated.

At the trigger location, location 15, the first byte of our program, 90, is on the right side of the DATA column. This is address 100. The byte on the left, F6, is from address 101. LST-F (last fetch), 2LS-F (second-to-last fetch), L&2LF (last and second-to-last fetch) and /QDUMP information is available to us from the STATUS column of the display. This information allows us to identify the first and second bytes of our example program as opcodes (the first bytes of new instructions). This is accomplished by locating the byte associated with LST-F indication at location 16 and tracking it backward through the queue. To do this we need to know how many bytes are in the queue now and how many were executed during the last cycle. The Q column provides past and present queue information by noting the change in the queue level from 2 to 3, in locations 15 and 16. Knowing that the 8086 pulled in two bytes, we can find out how many bytes were executed in this case 1.

There were 3 bytes in the queue at the end of the cycle shown in location 16. The LST-F indication in the STATUS column means that the last byte executed out of the queue

```
CRT1=00000 EVT    TRIG LOC = 015
CRT2=00000 EVT    TRIG IN TEST 1

LOC   ADDRESS      DATA   STATUS   G  I
---T   00100       F690   QDUMP   W  2  0
016    00102       EBE6   LST-F   W  3  0
017    00104       60FB   2LS-F   W  3  0
018    00106       9090   2LS-F   W  5  0
019    00108       9090   2LS-F   W  5  0
020    00100       F690   QDUMP   W  2  0
021    00102       EBE6   LST-F   W  3  0
022    00104       60FB   2LS-F   W  3  0
023    00106       9090   2LS-F   W  5  0
024    00108       9090   2LS-F   W  5  0
025    00100       F690   QDUMP   W  2  0
026    00102       EBE6   LST-F   W  3  0
027    00104       60FB   2LS-F   W  3  0
028    00106       9090   2LS-F   W  5  0
029    00108       9090   2LS-F   W  5  0
030    00100       F690   QDUMP   W  2  0
031    00102       EBE6   LST-F   W  3  0
032    00104       60FB   2LS-F   W  3  0
033    00106       9090   2LS-F   W  5  0

DISPLAY <- ACQMEM 0-MAIN
          0-ABSOLUTE
```

3473-05

Figure 2-4. Absolute display of example program - 8086.

7D02 MEMORY LOCATION NUMBER		15	16	17	18	19	20	21	22	23	24	25
8086 QUEUE CONTENTS	IN	-	-	-	-	-	-	-	-	-	-	-
		-	-	-	90	90	-	-	-	90	90	-
		-	-	-	90	90	-	-	-	90	90	-
		-	EB	60	60	90	-	EB	60	60	90	-
		F6	E6	FB	FB	90	F6	E6	FB	FB	90	F6
	OUT	90†	F6	EB	EB	60	90†	F6	EB	EB	60	90†
LAST FETCHED (LST-F)		?	90*	E6	E6	FB	-	90*	E6	E6	FB	-
SECOND-TO-LAST FETCHED (2LS-F)		?	?	F6**	F6**	EB**	-	-	F6**	F6**	EB**	-
THIRD-TO-LAST FETCHED		?	?	90	90	E6	-	-	90	90	E6	-
FOURTH-TO-LAST FETCHED		?	?	?	?	F6	-	-	-	-	F6	-
NUMBER OF BYTEG EXECUTED		?[D]	1	2	0	2	?[D]	1	2	0	2	?[D]

† Identified as first byte of an instruction by QDUMP
* Identified as first byte of an instruction by LST-F
** Identified as first byte of an instruction by 2LS-F
[D] Queue dump occurred

3473-06

Figure 2-5. Queue status during example program execution - 8086.

was the first byte of a new instruction, an opcode. Since two bytes are pulled into the queue whenever there is room (unless there is a JUMP, etc., to an odd address), and the queue level increased by one, we know that only one byte was executed out during this cycle. From this information we can track any particular byte through the queue. For instance, by knowing that only one byte was executed and that the last byte out was an opcode, we can track the 90 that was first in the queue in location 15 to its position as last out in location 16.

At location 17 the queue level has stayed the same while two bytes were pulled in, therefore two bytes must have been executed. With two bytes executed and a 2LS-F indication, it can be seen that the byte which was first in the queue at the beginning of the cycle was the opcode. Recalling that at location 16 we had a queue level of three and two bytes pulled in, the byte which was next out of the queue in location 16 must have been the last one in at location 15, i.e., F6. Therefore the last byte in at location 15 is the one which is indicated as being the opcode by the 2LS-F at location 17.

The PM 106 uses the method described above to establish the location of the first opcode whose location can be found by this method. After that the PM 106 takes a different approach. Once one opcode is located, the next opcode is predicted from the number of bytes required by the previous opcode. Only if an illegal opcode interrupts this process does the the PM 106 revert to the queue tracking method first described.

```
CRT1=00000 EVT   TRIG LOC = 015
CRT2=00000 EVT   TRIG IN TEST 1

LOC ADDRESS    OPERATION
---T00100 NOP
    00101 MULB DH
016 00102  E6    CODE FETCH
    00103 JMP 00100
017 00104  FB    CODE FETCH
    00105?*** (60)
018 00106  9090 CODE FETCH
019 00108  9090 CODE FETCH
020 00100 NOP
    00101 MULB DH
021 00102  E6    CODE FETCH
    00103 JMP 00100
022 00104  FB    CODE FETCH
    00105?*** (60)
023 00106  9090 CODE FETCH
024 00108  9090 CODE FETCH
025 00100 NOP
    00101 MULB DH
026 00102  E6    CODE FETCH

 DISPLAY <- ACQMEM 0-MAIN
    1-MNEMONIC
```

3473-07

Figure 2-6. Mnemonic display of example 08086.

Three asterisks in place of an opcode in the mnemonic data display (see Figure 2-6) indicates an illegal opcode. The number which follows it in parentheses is the illegal code. A question mark before an mnemonic occurs either because of a queue dump, or the end of memory, and indicates that there is uncertainty as to whether or not that byte was ever executed.

A second 8088 example. This second example program illustrates several of the more complex aspects of the mnemonic data display.

Address	Code	Mnemonic
480	E8 7D 00	CALL 00500
483	81 83 23	ADD 0123[BP][DI],#4567
...		
500	F7 70 24	DIV 24[BX][SI]
503	C3	RET
504	C7 06 23 00	MOV 0023,#XXXX

Figure 2-7 shows the absolute data display when the logic analyzer is triggered on address 00480. The steady queue level of 1 indicates that one byte is being executed at each location that is not a memory or input-output read or write. Therefore it is easy to see that the LST-F indication at location 16 is identifying the E8 byte that entered the queue at location 15 as the first byte of an instruction. The 2LS-F at location 17 is also identifying the E8 byte from location 15 as the first byte of an instruction. Figure 2-8 shows the status of the queue at these locations.

```
CRT1=00000 EVT    TRIG LOC = 015
CRT2=00000 EVT    TRIG IN TEST 1

LOC   ADDRESS     DATA   STATUS   Q  I
---T   00480       E8     QDUMP   1  0
016    00481       7D     LST-F   1  0
017    00482       00     2LS-F   1  0
018    00483       81     QFILL   1  0
019    00500       F7     QDUMP   1  0
020    007FD       83      MEMW   1  0
021    007FE       04      MEMW   1  0
022    00501       70     LST-F   1  0
023    00502       24     2LS-F   1  0
024    00503       C3     QFILL   1  0
025    00024       50      MEMR   1  0
026    00025       1B      MEMR   1  0
027    00504       C7     QFILL   2  0
028    00505       06     QFILL   3  0
029    00506       23     QFILL   4  0
030    007FD       83      MEMR   3  0
031    007FE       04      MEMR   3  0
032    00483       81     QDUMP   1  0
033    00484       83     LST-F   1  0

 DISPLAY <- ACQMEM 0-MAIN
    0-ABSOLUTE
```

3473-08

Figure 2-7. Absolute display of second example program - 8088.

7D02 MEMORY LOCATION NUMBER		15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33
8088 QUEUE CONTENTS	IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	23	-	-	-	-
		-	-	-	-	-	-	-	-	-	-	-	-	-	06	06	23	23	-	-
	OUT	-	-	-	-	-	-	-	-	-	-	-	-	C7	C7	C7	06	06	-	-
		E8†	7D	00	81	F7†	F7	F7	70	24	C3	C3	C3	C3	C3	C3	C7	C7	81†	83
LAST FETCHED (LST-F)		?	E8*	7D	00	-	-	-	F7*	70	24	24	24	24	24	24	C3	C3	-	81*
SECOND-TO-LAST FETCHED (2LS-F)		?	?	E8**	7D	-	-	-	-	F7**	70	70	70	70	70	70	24	24	-	-
THIRD-TO-LAST FETCHED		?	?	?	E8	-	-	-	-	-	F7	F7	F7	F7	F7	F7	70	70	-	-
FOURTH-TO-LAST FETCHED		?	?	?	?	-	-	-	-	-	-	-	-	-	-	-	F7	F7	-	-
NUMBER OF BYTEG EXECUTED		?[D]	1	1	1	?[D]	0	0	1	1	1	0	?[D]	0	0	0	1	0	?[D]	1

† Identified as first byte of an instruction by QDUMP
* Identified as first byte of an instruction by LST-F
** Identified as first byte of an instruction by 2LS-F
[D] Queue dump occurred

3473-09

Figure 2-8. Queue status during second example program - 8088.

Figure 2-9 shows the mnemonic display disassembled by the PM 107. Notice the indication at location 18, ?81 OPCODE. The 81 OPCODE portion of this display means that the byte 81 was only the first byte of a two byte opcode and the second byte was lost in the queue dump. The ? indicates that there is doubt that this opcode was executed. In this display all three question marks arise from the occurrence of queue dump operations.

```
 CRT1=00000 EVT  TRIG LOC = 015
 CRT2=00000 EVT  TRIG IN TEST 1
LOC ADDRESS   OPERATION
---T00480 CALL 00500
016 00481  7D   CODE FETCH
017 00482  00   CODE FETCH
018 00483?81 OPCODE
019 00500 DIV 24[BX][SI]
020 007FD  83 MEMORY WRITE
021 007FE  04 MEMORY WRITE
022 00501  70   CODE FETCH
023 00502  24   CODE FETCH
024 00503?RET
025 00024  50 MEMORY READ
026 00025  1B MEMORY READ
027 00504?MOV **23,#****
028 00505  06   CODE FETCH
029 00506  23   CODE FETCH
030 007FD  83 MEMORY READ
031 007FE  04 MEMORY READ
032 00483 ADD 0123[BP][DI],#4567
033 00484  83   CODE FETCH

 DISPLAY <- ACQMEM 0-MAIN
   1-MNEMONIC
```

3473-10

Figure 2-9. Mnemonic display of second example program - 8088.

Note also (in all three figures) that the memory write operations occurring at locations 20 and 21 are part of the CALL instruction at location 15 rather than the DIV instruction which immediately precedes it. Which memory or input-output operations go with which instructions can be established by tracking the last byte of the instruction through the queue. The memory or input-output operations which follow the execution of the last byte are the ones associated with that instruction. The last byte of the CALL at location 15 is executed at location 18. The /QDUMP for this CALL occurs at location 19. The stack MEMWs (memory writes) start at location 20.

The RET at location 24 is preceded by a question mark which indicates that it may not have been executed. In fact, it has been executed in this case. This can be ascertained by generating a picture or mental image of the queue (such as is shown in Figure 2-8) from the information in the displays. As we track the byte C3 through the queue, we find it emerging and being executed at location 30 which is before the queue dump at location 32. Notice that the absolute data display shows a memory read operation at location 30, not a LST-F. The algorithm which is used to initially acquire opcode information would therefore not see any of the codefetch indicators which are used to locate opcodes by the first method (LST-F, 2LS-F, L&2LS, and /QDUMP). However the return is properly identified, although the question mark incorrectly labels it as probably not executed.

One further aspect of the mnemonic display of this second program (refer to Figure 2-9) deserves discussion. The move instruction which is shown preceeded by a question mark at location 27 is followed by an operand which contains asterisks instead of the source data. This instruction was not executed, as we can see by examining Figure 2-8, the queue status diagram for the second example program. The first byte of this instruction, C7, enters the queue at

location 27, as we can see from the data displays. Tracking it through reveals that it was first in line waiting to come out when the queue dump occurred. The asterisks occur because one or more bytes of the operand had not entered the queue at the time of the return. Remember, this instruction was not part of the path taken by the program due to the return from address 503 to address 483.

A Second 8086 Example. The following program illustrates several of the more complicated features of the PM 106 data displays.

Address	Code	Mnemonic
480	E8 7D 00	CALL 00500
483	81 83 23	ADD 0123[BP][DI],#4567
...		
500	F7 70 24	DIV 24[BX][SI]
503	C3	RET
504	C7 06 23 00	MOV 0023,#XXXX

Triggering on the first address, 00480, produces the following display (Figure 2-10) in the absolute mode.

Using the same method used in the first example, we can construct a mental or actual picture of the activity in the queue such as that shown in Figure 2-11.

```
CRT1=00000 EVT    TRIG LOC = 015
CRT2=00000 EVT    TRIG IN TEST 1
LOC   ADDRESS     DATA   STATUS  Q I
---T   00480      7DE8   QDUMP W 2 0
016    00482      8100   2LS-F W 2 0
017    00484      2383   QFILL W 3 0
018    00500      70F7   QDUMP W 2 0
019    007FD      8304    MEMW H 2 0
020    007FE      8304    MEMW L 2 0
021    00502      C324   2LS-F W 2 0
022    00504      06C7   QFILL W 3 0
023    00024      1C01    MEMR W 3 0
024    00506      0023   QFILL W 5 0
025    007FD      83FF    MEMR H 4 0
026    007FE      FF04    MEMR L 4 0
027    00483      81FF   QDUMP H 1 0
028    00484      2383   LST-F W 2 0
029    00486      6701   2LS-F W 3 0
030    00488      1C45   QFILL W 3 0
031    00123      1CFF    MEMR H 3 0
032    00124      FF01    MEMR L 3 0
033    0048A      1C01   QFILL W 3 0

DISPLAY <- ACQMEM 0-MAIN
   0-ABSOLUTE
```

3473-11

Figure 2-10. Absolute display of second example program - 8086.

7D02 MEMORY LOCATION NUMBER		15	16	17	18	19	20	21	22	23	24	25
8086 QUEUE CONTENTS	IN	-	-	-	-	-	-	-	-	-	-	-
		-	-	-	-	-	-	-	-	-	00	-
		-	-	-	-	-	-	-	-	-	23	00
		-	-	23	-	-	-	-	06	06	06	23
		7D	81	83	70	70	70	C3	C7	C7	C7	06
	OUT	E8†	00	81	F7†	F7	F7	24	C3	C3	C3	C7
LAST FETCHED (LST-F)		?	7D	00	-	-	-	70	24	24	24	C3
SECOND-TO-LAST FETCHED (2LS-F)		?	E8**	7D	-	-	-	F7**	70	70	70	24
THIRD-TO-LAST FETCHED		?	?	E8	-	-	-	-	F7	F7	F7	70
FOURTH-TO-LAST FETCHED		?	?	?	-	-	-	-	-	-	-	F7
NUMBER OF BYTEG EXECUTED		?D	2	1	?D	0	0	2	1	0	0	1

† Identified as first byte of an instruction by QDUMP
* Identified as first byte of an instruction by LST-F
** Identified as first byte of an instruction by 2LS-F
D Queue dump occurred

3473-12

Figure 2-11. Queue status during second example program execution - 8086.

@

```
 CRT1=00000 EVT  TRIG LOC = 015
 CRT2=00000 EVT  TRIG IN TEST 1
LOC ADDRESS   OPERATION
---T00480 CALL 00500
    00481  7D   CODE FETCH
016 00482  00   CODE FETCH
    00483?ADD **23[BP][DI],#****
017 00484  2383 CODE FETCH
018 00500 DIV 24[BX][SI]
    00501  70   CODE FETCH
019 007FD  83   MEMORY WRITE
020 007FE  04   MEMORY WRITE
021 00502  24   CODE FETCH
    00503?RET
022 00504?MOV 0023,#****
    00505  06   CODE FETCH
023 00024  1C01 MEMORY READ
024 00506  0023 CODE FETCH
025 007FD  83   MEMORY READ
026 007FE  04   MEMORY READ
027 00483 ADD 0123[BP][DI],#4567
028 00484  2383 CODE FETCH

 DISPLAY <- ACQMEM 0-MAIN
    0-MNEMONIC
```

3473-13

Figure 2-12. Mnemonic display of second example program - 8086.

In the mnemonic mode the Figure 2-12 display is produced.

The question mark in front of the ADD at location 16, address 483 indicates that this instruction was probably not executed. The byte in address 483, 81, was never executed because the queue dump which was part of the CALL at location 15 occurs at location 18 and the three bytes in the queue at location 17 are flushed.

The ADD instruction is disassembled by knowing the length of the previous instruction. However, since only two of the three bytes of associated operand ever moved on the bus, the question mark and multiple asterisks in the display indicate an incomplete disassembly.

The question mark on the RET at location 21, address 503 is an example of the rare circumstance where such a question mark is associated with an instruction that is actually executed. It occurred in this case because the /QDUMP which was part of the RET prevented the PM 106 from seeing any indication of its being executed.

The MOV instruction preceeded by a question mark and containing asterisks in its operand (at location 22) is another example of an instruction being partially called into the queue just before a program jump and the resulting queue dump.

At location 27 we see the same ADD instruction that we saw at location 16, only now it is completely called in and is executed, so the question mark is gone and the asterisks have been replaced by real values.

SPECIFICATION

INTRODUCTION

This section of the manual lists the electrical (Table 3-2), mechanical (Table 3-3), and environmental (Table 3-4) characteristics of the PM 106 and PM 107 Personality Modules. Since the PM 106 and PM 107 operate only as part of a logic analyzer system, all operating voltages and currents are furnished by the logic analyzer to which the PM 106 or PM 107 is connected.

If verification of these listed electrical characteristics is required for customer incoming inspection or other purposes, the Performance Check section lists the necessary test equipment and procedures.

Items listed in the Supplemental Information columns are either explanatory notes or performance characteristics for which no limits are specified. They may not be verified.

OVERVIEW

The personality module connects the logic analyzer to a system under test (SUT). The microprocessor plug, see Table 3-5, of the personality module replaces the microprocessor in the SUT, allowing the logic analyzer access to all address, data, control, and clock lines.

The personality module consists of a 4.7 in. by 8 in. by 1.9 in. circuitry pod, with a ribbon cable and logic analyzer plug, see Table 3-6, on one end, and a twisted pair woven cable and microprocessor plug on the other. The logic analyzer plug connects to the logic analyzer, and the microprocessor plug connects to the SUT.

The pod contains an interface assembly that "personalizes" the logic analyzer to work with a specific microprocessor. This is why the pod is called the "personality module pod." The microprocessor is removed from its socket on the SUT and placed in the zero insertion force (ZIF) socket of the personality module pod. The microprocessor plug is then installed in the microprocessor socket of the SUT.

The personality module transfers data from the SUT to the logic analyzer in a standard format for the logic analyzer. The personality module also contains firmware that allows the logic analyzer to disassemble the information it received into the mnemonics of that microprocessor.

Circuitry in the personality module pod works together with the circuitry on the front end board of the logic analyzer to generate the state clock. The state clock strobes information from the personality module into the logic analyzer's acquisition memory.

Service Test Fixture

The personality module may be ordered with a service test fixture (067-1024-00). The microprocessor plug connects to a socket on the service test fixture pod and a cable from the fixture plugs into the personality module ZIF socket. An oscillator running at a frequency of 8.08 MHz (which is slightly faster than the 8 MHz version of the μP) is fed into a test signal generator. The service test fixture puts various combinations of data on the data, address, and control lines. The personality module acquires this data and disassembles it.

The service test fixture has a separate power supply and plug.

NOTE

The PM 106/107 Personality Modules will initially be used with the 7D02 Logic Analyzer. References to the 7D02 have been minimized in this Specification section, in order to ease the use of the personality modules with other logic analyzer devices. References to logic analyzer specifications and characteristics in this document are met by the 7D02; these specifications and characteristics must also be met by future logic analyzers that use the PM 106 and PM 107 Personality Module.

With the qualifications of Table 3-6, the personality module supports the following processors.

PM 106 – 8086
8086-2
8086-4
PM 107 – 8088

Table 3-1
TIMING RESPONSE-REQUIREMENTS DIFFERENCES

Mode	Parameter	PM 106/107 Specification	Intel 8086/8086-2 8086-4/8088
Minimum	Data:	a) Setup: 30 ns min.	(TDVCL)
Maximum		b) Hold: 0 ns min.	(TCLDX)
Maximum	READY line:	a) Setup: 80 ns min. prior to processor clock falling edge in machine state T3 or T4.	(TRYLCL) (TRYHCH)
		b) Hold: 0 ns min. hold to clock falling edge in machine state T4.	(TRYLCL) (TCHRYX)
Minimum	READY line:	a) Setup: 80 ns min. prior to processor clock falling edge in machine state T4.	(TRYHCH) (TRYLCL)
		b) Hold: 0 ns min. hold to clock falling edge in machine state T4.	(TCHRYX)
Minimum	ALE line:	a) ALE falling edge 55 ns max. after rising edge of machine state T1.	(TCHLL)
		b) Pulse width 60 ns min.	(TLHLL)
Minimum	M/$\overline{IO}$ and $\overline{INTA}$ lines:	110 ns delay time	(TCHCTV)
Minimum	DT/$\overline{R}$ line:	TCHCL + 100 ns max. where TCHCL = (1/3 TCLCL) + 2 and TCLCL = clock period	(TCHCTV)
Minimum	$\overline{DEN}$ line:	TCHCL + 80 ns max. where TCHCL = (1/3 TCLCL) + 2 and TCLCL = clock period	(TCVCTV) (TCVCTX)
Minimum	$\overline{WR}$ line:	80 ns max.	(TCVCTV) (TLVCTX)
Minimum	HLDA line:	Greater than 1 clock + 100 ns	Greater than 1 clock + 85 ns

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Table 3-2
ELECTRICAL SPECIFICATIONS

Characteristics	Performance Requirements	Supplemental Information
Data Input Channels		
Input Impedance		1/2 LSTTL Load 45 pF max
TTL Input Levels		
Voltage in Low Limits (operating)		−0.5 V to +0.5 V
Voltage in High Limits (operating)		+2.0 V to +.0 V
Current in Low Limits (V in low = +0.4 V)		+0.2 mA except MN/$\overline{MX}$ (+0.36) HOLD (+0.36), RESET (+0.36)
Current in High Limits (V in high = +5.5 V)		+0.1 mA all inputs
Maximum Voltage in, (non-operating, non-destructive)		−5 V, +7.0 V (except MN/$\overline{MX}$,HOLD, RESET +5.5, −1.0 V)
Threshold Voltage		+1.4 V nominal TTL compatible
Hysteresis		+0.2 V minimum
Input Impedance maximum mode additional series resistance (CPU pins 24-31)		10 Ω
Minimum Mode Signals ALE Falling Edge (TCHLL)		55 ns max. 0 ns after clock falling edge in machine state T2
ALE width (TLHLL)		60 ns min.
M/$\overline{IO}$ & $\overline{INTA}$ (TCHCTV)		110 ns max.
DT/$\overline{R}$ (TCHCTV)		Clock high width + 100 ns
$\overline{DEN}$ (TCVCTV) (TCVCTX)		Clock high width + 80 ns max.
$\overline{WR}$ (TCVCTV) (TCVCTX)		80 ns max.
HLDA		Greater than one clock + 100 ns max.
Minimum Simulation Nominal Delay		HLDA = >one clock + 33 ns $\overline{WR}$ = 45 ns M/$\overline{IO}$ = 33 ns (8086) IO/$\overline{M}$ = 48 ns (8088) DT/$\overline{R}$ = 33 ns $\overline{DEN}$ = 63 ns ALE = 51 ns $\overline{INTA}$ = 68 ns

Table 3-2 (cont)

Characteristics	Performance Requirements	Supplemental Information
Delay, all other channels including queue level and instruction fetch		Synchronous with clock falling edge +100 ns max.
Test Clock Frequency		8.08 MHz with service test fixture 067-1024-00
System Specifications		
Address		Set up time 45 ns Hold time = 20 ns beyond ALE falling edge
Data	Setup 30 ns Hold 0 ns	Clock falling edge of data in machine state T4
Control Lines Delay Time		
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$(TCHSV)		70 ns max.
QS0, QS1 (TCLAV)		60 ns max.
$\overline{RQ/GT0}$, $\overline{RQ/GT1}$ (TCLGL) (TCLGH)		50 ns max.
Personality Eprom Input Look to /SELP		75 ns min.
/SELP to Valid Data Out		560 ns max.
/HALT		Requires user modification to enable (see Maintenance and Troubleshooting Section)
Delay, Minimum (if enabled)		One clock cycle
Delay, Maximum (if enabled)		Indefinite (repeat instruction with LOCK prefix). Generally one machine cycle, + 80 ns max.
Output drive V_{oh}		open collector
V_{ol}		+0.8 V I_o = −6 mA
Clock Input		
Input Impedance		50 kΩ Nominal
Clock Period	125 ns min.	45 pF max.
Clock Pulse Width (min.)	43.7 ns	
Voltage in Low Limits (operating)		−0.5 V to +0.5 V
Voltage in High Limits (operating)		−2.0 V to +7.0 V

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Table 3-2 (cont)

Characteristics	Performance Requirements	Supplemental Information
Threshold Voltage		+1.4 V nominal
Hysteresis		+0.4 V nominal
Maximum Voltage in, (non-operating, non-destructive)		−5 V to +7 V
Propagation Delays through Personality Module		
Delay through ECL Clock		10 ns min., 16.5 ns max.
Data Channel Signal Prop. Delay		15 ns min., 51 ns max.
READY		
Rising Edge		80 ns max. prior to processor clock falling edge in machine state T4
Falling Edge		0 ns max. hold to clock falling edge in machine state T3 or Tw

Table 3-3
MECHANICAL SPECIFICATIONS

Characteristics	Description
Size	12 x 20 x 4.6 cm. (4.7 x 8 x 1.9 in.)
Weight	1.2 kg. (2.5 lbs.)
Cable Length (micro-processor plug to personality module)	33 cm ± 1.2 cm. (13 in. ± .5 in.)
Cable Length (logic analyzer plug to pod)	122 cm. ±2.6 cm. (4 ft. 1 in.)

Table 3-4
ENVIRONMENTAL SPECIFICATIONS

Characteristics	Description
Temperature	
Operating	−15°C to +55°C
Non-operating	−62°C to +85°C
Relative Humidity	95 to 97% non-condensing five 24-hour cycles @ 30°C to 60°C
Altitude	
Operating	4.5 kM (15,000 feet)
Non-operating	15 kM (50,000 feet)

Table 3-5
MICROPROCESSOR PLUG

MICROPROCESSOR PLUG TO POD CONNECTOR	PLUG PIN ZIF	INPUT PROTECTION	SIGNAL NAME
J6020-1	40	Yes[a]	Vcc
J6020-3	39	Yes	ADI15
J6020-5	38	Yes	AI16
J6020-7	37	Yes	AI17
J6020-9	36	Yes	AI18
J6020-11	35	Yes	AI19
J6020-13	34	Yes	$\overline{BHE}$
J6020-15	—	Yes[a]	MN/$\overline{MX}$
J6020-17	32	Yes[a]	$\overline{RD}$
J6020-19	31[b]	Yes	$\overline{RQ/GT0}$ (HOLD)
J6020-21	30[b]	Yes	$\overline{RQ/GT1}$ (HLDA)
J6020-23	29[b]	Yes	$\overline{LOCK}$ ($\overline{WR}$)
J6020-25	28[b]	Yes	$\overline{S2I}$ (M/$\overline{IO}$)
J6020-27	27[b]	Yes	$\overline{S1I}$ (DT/$\overline{R}$)
J6020-29	26[b]	Yes	$\overline{S0I}$ ($\overline{DEN}$)
J6020-31	25[b]	Yes	QS0 (ALE)
J6020-33	24[b]	Yes	QS1 ($\overline{INTA}$)
J6020-35	23	Yes[a]	$\overline{TEST}$
J6020-37	22	Yes	READY
J6020-39	21	Yes	RESET
J7020-1	1	No	GROUND
J7020-3	2	Yes	ADI14
J7020-5	3	Yes	ADI13
J7020-7	4	Yes	ADI12
J7020-9	5	Yes	ADI11
J7020-11	6	Yes	ADI10
J7020-13	7	Yes	ADI9
J7020-15	8	Yes	ADI8
J7020-17	9	Yes	ADI7
J7020-19	10	Yes	ADI6
J7020-21	11	Yes	ADI5
J7020-23	12	Yes	ADI4
J7020-25	13	Yes	ADI3
J7020-27	14	Yes	ADI2
J7020-29	15	Yes	ADI1
J7020-31	16	Yes	ADI0
J7020-33	17	Yes	NMI
J7020-35	18	Yes	INTR
J7020-37	19	Yes	CLK
J7020-39	20	No	GROUND

J7020-2, 4, 6,....40 All even-numbered lines are grounds.
J6020-2, 4, 6,....30 All even-numbered lines are grounds.

[a] Spark gap only.
[b] Through FET switching maximum mode only. Signal derived in minimum mode.

For use with the PM 106/107, the 7D02 must be equipped with the expansion option. The PM 106 may be used with or without the timing option.

Table 3-6
LOGIC ANALYZER PLUG

PM PIN J1010	SIGNAL	DESCRIPTION
1	GROUND	GROUND
2	CLOCK	ECL CLOCK
3	$\overline{\text{CLOCK}}$	$\overline{\text{ECL CLOCK}}$
4	GROUND	GROUND
5	A0	ADDRESS 0
6	A1	ADDRESS 1
7	A2	ADDRESS 2
8	A3	ADDRESS 3
9	A4	ADDRESS 4
10	A5	ADDRESS 5
11	A6	ADDRESS 6
12	A7	ADDRESS 7
13	A8	ADDRESS 8
14	A9	ADDRESS 9
15	A10	ADDRESS 10
16	A11	ADDRESS 11
17	A12	ADDRESS 12
18	A13	ADDRESS 13
19	A14	ADDRESS 14
20	A15	ADDRESS 15
21	A16	ADDRESS 16
22	A17	ADDRESS 17
23	A18	ADDRESS 18
24	A19	ADDRESS 19
25	A20	BHE [$\overline{\text{QDUMP}}$]
26	A21	QUEUE WORD LSB
27	A22	QUEUE WORD LSB
28	A23	QUEUE WORD MSB
29	AD0	DATA BIT 0
30	AD1	DATA BIT 1
31	AD2	DATA BIT 2
32	AD3	DATA BIT 3
33	AD4	DATA BIT 4
34	AD5	DATA BIT 5
35	AD6	DATA BIT 6
36	AD7	DATA BIT 7
37	AD8	DATA BIT 8
38	AD9	DATA BIT 9
39	AD10	DATA BIT 10
40	AD11	DATA BIT 11
41	AD12	DATA BIT 12
42	AD13	DATA BIT 13
43	AD14	DATA BIT 14

Table 3-6 (cont)

PM PIN J1010	SIGNAL	DESCRIPTION
44	AD15	DATA BIT 15
45	+5	+5 V POWER
46	C0	R/$\overline{\text{W}}$[LST-F]
47	C1	M/$\overline{\text{IO}}$[2LS-F]
48	C2	$\overline{\text{CODEFETCH}}$
49	C3	IRQ
50	C4	MIN/$\overline{\text{MAX}}$
51	C5	HOLD ACK
52	C6	$\overline{\text{CODEFETCH}}$
53	C7	HOLDACK
54	C8	$\overline{\text{T1}}$
55	C9	$\overline{\text{WAIT}}$
56	+5	POWER
57	+5	POWER
58	+15	POWER
59	−15	POWER
60	GROUND	GROUND
61	$\overline{\text{HALT}}$	STOP
62	LOOK	INPUT LOOK
63	$\overline{\text{SELP}}$	SELECT EPROM
64	GROUND	GROUND

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

THEORY OF OPERATION

GENERAL THEORY OF OPERATION

Overview

The PM 106/107 Personality Module acts as a bus monitor over the 8086/8088 bus in real time. The personality module generates information according to conditions present on the bus for 7D02 data qualification and triggering. This information may or may not correspond to the actual execution of instructions. After the 7D02 has triggered and filled the acquisition memory, algorithms are applied to the acquired data to determine the status of the queue and which instructions were actually executed. It is not possible to trigger or qualify directly on instructions as they are executed.

Function

The PM 106/107 Personality Module performs two basic functions. First, the PM 106/107 acts as a hardware interface between the microprocessor system and the logic analyzer. The PM 106/107 allows the selected microprocessor to operate as if it were in the system under test (SUT) with the address, data, control, and clock lines available to the logic analyzer. The second function of the PM 106/107 is to provide personalized interpretation and setup information which is specific to the 8086/8088 microprocessors, in a standard format for the logic analyzer. This information aids in mnemonic disassembly of the acquired information, customizing of the displays, and in providing default word recognition and timing data values.

Block Diagrams and Schematics

Figure 4-1 is a circuit block diagram which organizes the circuitry on board A1 into functional blocks with the circuitry of boards A2 and A3 shown as single board blocks. It should be useful in gaining an overview of the interaction between board A1 and the remainder of the circuitry within the personality module.

Figures 4-2 and 4-5 are detailed block diagrams which organize the circuitry of boards A2 and A3, respectively, into functional blocks. These block diagrams should be useful when troubleshooting certain problems.

Schematic diagrams are provided in the Diagrams section of the manual and are keyed to their respective circuit descriptions by numbered diamond symbols. For increased understanding of the detailed circuit descriptions, refer to both the appropriate schematic diagram and functional block diagram.

NOTE

Throughout the rest of this manual, a bar (—) over a signal name or portion of a signal name indicates that the signal is active when in the low state. For example, $\overline{HALT}$ indicates that $\overline{HALT}$ is an active low signal. R/W indicates 1-Read, 0-Write.

8086/8088 Differences

The 8086/8088 microprocessors are characterized by a 20 bit address bus with an identical instruction-function format. The essential difference between the 8086/8088 is the data bus width. The 8086 central processing unit (CPU) incorporates a 16 bit external data bus where the 8088 CPU incorporates an 8 bit external data bus. The 8086 16-bit data bus allows the advantage of accessing two bytes in a single bus cycle. The 8 bit data bus of the 8088 restricts byte accessing to one byte of code in a single bus cycle.

The 8086 CPU uses memory space that is divided into two banks. The lower bank, using data lines D0-D7, is reserved for even-addressed bytes. The upper bank, using data lines D8-D15, is reserved for odd-addressed bytes. Both memory banks are accessed by addressing lines A1-A19 while A0 and $\overline{BHE}$ select the proper bank.

NOTE

The PM 106 Personality Module for the 8086 microprocessor uses the inverted byte high enable line jumper strap P6020 positioned to enable the function of the $\overline{BHE}$ line. The PM 107 Personality Module for the 8088 microprocessor uses P6020 positioned to disable the $\overline{BHE}$ line operation.

The 8088 CPU memory space is organized as a linear array of byte space. Since the 8088 uses an 8 bit data bus,

memory resides in a single bank. This memory bank is accessed by address lines A1-A19, although only A0 is used for selection of the appropriate EPROM. A basic difference for the read and write cycles between the 8086 and 8088 CPUs is interpretation of the M/$\overline{IO}$ control line. When this line is in a high state, the 8086 CPU interprets this line as an access of a memory device. When M/$\overline{IO}$ is in a low state, the read or write is meant to access an input-output device. Conversely, the 8088 CPU interprets the line as an IO/$\overline{M}$ function. When the line is high, an input-output device is being accessed, and when low a memory device is being accessed.

NOTE

The PM 106 Personality Module for the 8086 microprocessor uses the jumper strap P6010 positioned to enable the M/$\overline{IO}$ line as an output. The PM 107 Personality Module for the 8088 microprocessor uses the jumper strap P6010 positioned to enable the IO/$\overline{M}$ line as an output.

Minimum and Maximum Modes

The PM 106/107 Personality Module has the option of operating either in a minimum or a maximum mode configuration as selected by the system under test (SUT). The microprocessor installed in the zero insertion force (ZIF) socket, however, always operates in the maximum mode configuration.

In the minimum mode, the PM 106/107 uses the 8086/8088 maximum mode outputs for emulation of a minimum mode condition to produce signals that are normally only available in the maximum mode. Outputs from the minimum mode emulation circuitry then provide control information back to the SUT. Information generated within this circuitry is also available to the logic analyzer. Some of the timing requirements or responses of the emulated signals differ from the specifications shown in *The 8086 Family User's Manual*, an Intel publication. Refer to the Specification section or to the individual detailed circuit descriptions for further reference.

In the maximum mode, the PM 106/107 uses the 8086/8088 maximum mode outputs to provide control information to the SUT. These outputs are used within the personality module to gather pertinent information that is made available to the logic analyzer in proper format.

The Queue

The instruction stream queue is a first-in-first-out (FIFO) data register within the 8086/8088 central processing unit (CPU) where instruction bytes are stored. Two processing units, both internal to the CPU, that interact with the instruction stream queue are the execution unit (EU) and the bus interface unit (BIU). The BIU has the ability to pre-fetch instructions, read operands, and store the results. The EU removes instruction bytes from the instruction stream queue and executes them as a part of normal program flow.

Instruction bytes that have entered the instruction stream queue have two possible destinations. Either the instruction is executed in program flow or the instruction is dumped from the queue when software or hardware causes a program transfer (e.g., a JUMP instruction or an interrupt).

Mnemonic disassembly of acquired information requires identification of the first byte of each instruction (the instruction fetch, INFT), executed out of the queue. The queue level and two lines which indicate when the last byte [LST-F] or the second-to-last byte [2LS-F] executed out of the queue was the first byte of a new instruction must be used to indirectly calculate the first byte of the instruction. The queue follower circuitry of board A3 supplies this information.

Bus Cycle Operation

All bus cycles consist of a minimum of four clock cycles (or "T states") identified as T1, T2, T3, and T4. Bus activity is referenced to these four states. Refer to the Machine State Generator discussion of the middle board, for additional information.

Another state "Twait", identified as Tw, may be activated by the READYB signal line from any peripheral and is inserted between machine states 3 and 4. Twait compensates for slow I/O or memory devices not able to transfer information at a maximum rate. Time between bus cycles when no bus activity is present is called "Tidle" and is identified as Ti.

Circuitry in the PM 106/107 tracks the bus cycle used by the microprocessor. The bus interface unit (BIU), in the central processing unit (CPU), controls the output on processor status lines $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$. When bus activity is to follow, the BIU changes the condition of the status lines appropriately (refer to Table 4-1). Circuitry within the PM 106/107 then decodes this status line change and generates a signal, ALE. The ALE signal in turn produces machine state T1 in the bus cycle sequence.

Bus operation can be understood by examining the multiplexed address-data lines during a bus cycle. During T1, the CPU places the address of the appropriate memory location or input-output device on the bus for both read and write operations. During a read bus cycle, the addressing lines in machine state T2 are tri-stated while the address is removed from the bus. For a write bus cycle, the addressing information is taken off the bus during machine state T2 and

the CPU places data on the multiplexed bus until machine state T4.

See *The 8086 Family User's Manual*, an Intel publication, for further explanation of bus cycle operation.

Interrupts

Interrupts to the central processing unit (CPU) may be initiated by software or hardware. Only the INTR and NMI interrupts are stored in the 7D02 or used by the 7D02 word recognizer. These two interrupts are classified as maskable (INTR) and non-maskable (NMI). All interrupts result in the transfer of program control to a new program location supplied by a vector table.

The CPU, upon receiving a maskable interrupt (INTR), executes two interrupt acknowledge ($\overline{INTA}$) bus cycles. If a non-maskable interrupt (NMI) is received, the CPU latches the interrupt at a higher priority.

DETAILED CIRCUIT DESCRIPTION UPPER BOARD

Overview

The address and data circuitry found on board A1 includes the following circuits.

1. Address and data buffers.
2. The personality EPROMS and associated buffer.
3. Minimum Mode FETs and Switchers.
4. Maximum Mode FETs and Switchers.
5. Clock Converter circuit.
6. Input Protection Hybrids.
7. Miscellaneous buffers and latches.

The block diagram of Figure 4-1 shows this circuitry in functional blocks. Refer to Figure 4-1 for an overview of board A1 and to aid in understanding the flow of signals between the personality module and the system under test or the flow between the personality module and the logic analyzer.

Schematic diagrams are provided in the Diagrams section of the manual and are keyed to their respective circuit descriptions by numbered diamond symbols. For increased understanding of the detailed circuit descriptions, refer to both the appropriate schematic diagram and functional block diagram.

NOTE

Throughout the rest of this manual, a bar (—) over a signal name or portion of a signal name indicates that the signal is active when in the low state. For example, $\overline{HALT}$ indicates that $\overline{HALT}$ is an active low signal. R/W indicates that 1-Read, 0-Write.

If a bracket ([ ]) appears around a signal name, it indicates that the signal line is a dual function line and the signal may appear in the same form on the logic analyzer screen display in the word recognizer. For example, the BHE[/QDUMP] line.

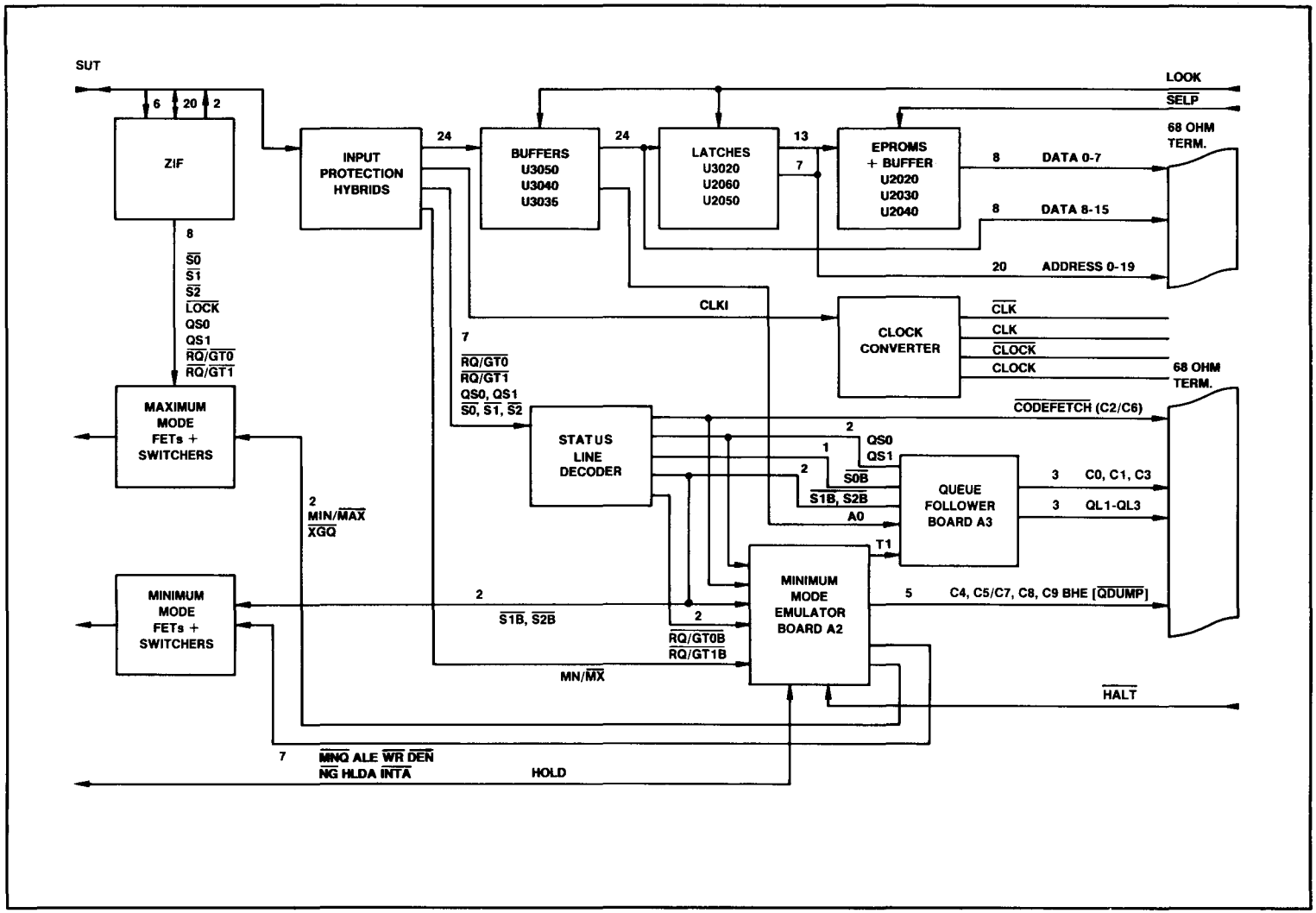
Component numbers in this manual are composed of an assembly number and a schematic circuit number. For example, A1U2030 indicates that component U2030 is located on assembly A1 (board 1) of the personality module.

A convention of minimizing lengthy parts references is used in this manual. For example, the reference A1U3050, A1U3040, and A1U3035 representing components on assembly A1 (board 1) may be referenced as A1U's 3050, 3040, and 3035.

Address and Data Circuitry ◇1

Address, data, and control lines from the system under test (SUT) are connected directly to the personality module through a 40 pin microprocessor replacement plug and woven cable. When the 8086/8088 microprocessor is installed in the zero insertion force (ZIF) socket within the module, the microprocessor still controls the circuitry from which it was removed. Multiplexed address-data lines AD0-AD15 as well as A16-A19 connect to J6020, J7020, and the ZIF. Each line connects to input protection hybrids. Address-data lines AD0-AD15 and A16-A19 are buffered in A1U's 3050, 3040, and 3035. The outputs of these buffers connect to latches (A1U's 2060, 2050, and 3020A). When the latching signal, ALE, is low, the information present on the inputs is latched. When ALE is high, the latches act as transparent buffers that allow the output to follow the input.

Multiplexed lines AD0-AD15 from the buffers connect through a 68 Ω termination to the logic analyzer interface. Address lines A0-A19 from the latches also connect to the 68 Ω termination resistors at J1010.



3473-14

Figure 4-1. Overview block diagram.

The address and data lines to the logic analyzer have two major functions,

1. In the acquisition mode, to provide the data that is to be stored in the logic analyzer acquisition memory.

2. To provide access to the information in the personality module EPROMs.

EPROMs and Buffer ◇1

The two 4K x 8 bit EPROMs, A1U2020 and A1U2030, provide personalized disassembly and display information for the logic analyzer. The EPROMs are addressed on lines A0-A11 with lines A12 and the complement $\overline{A12}$, providing selection between EPROMs. The control line $\overline{SELP}$, from the 7DO2, permits the output of information from either EPROM to the EPROM buffer, A1U2040. The information is then output on lines AD0-AD7 to the logic analyzer. The non-selected EPROM is powered down to reduce power consumption.

Maximum Mode FETs and Switchers ◇2

(Refer to the Specification section for signal line timing differences.)

When activated, the eight maximum mode field effect transistors (FETs) A1Q's 5024, 5022, 5020, 5018, 7012, 6012, 4020, and 4018 allow information to pass from the microprocessor installed in the zero insertion force (ZIF) socket to the system under test (SUT) when the personality module is operating in the maximum mode.

The eight maximum mode output lines ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$, $\overline{LOCK}$, QS0, QS1, $\overline{RQ}/\overline{GT0}$, and $\overline{RQ}/\overline{GT1}$) connect to the Input Protection Hybrids and provide information to the personality module in both minimum and maximum modes. The first four FETs (A1Q's 5020, 5022, 5024 and 5018) are tri-stated in the maximum mode by $\overline{RQ}/\overline{GTX}$ (0 or 1) through control line $\overline{XGQ}$ and switching transistors (A1Q's 6068, 6065, and 6060). The second four FETs (A1Q's 7012, 6012, 4018 and 4020) are not tri-stated in the maximum mode but are activated with the MIN/$\overline{MAX}$ control line through switch ing transistor A1Q6070. The switching transistors provide +15 volts or −5 volts to the gate of each FET to activate or deactivate that FET.

NOTE

The signal lines on pins 24-31 of the microprocessor to the system under test have a maximum of 10 Ω of series resistance due to the presence of the FETs in the personality module circuitry.

Minimum Mode FETs and Switchers ◇2

When activated, the eight minimum mode field effect transistors (FETs) A1Q's 7010, 5010, 5016, 5014, 5012, 4014, 6010, and 4012 allow information to pass from the emulation circuitry of the personality module to the system under test (SUT) in the minimum mode of operation.

The eight information lines are $\overline{S2}$(M/$\overline{IO}$) for the 8086 or $\overline{S2}$(IO/$\overline{M}$) for the 8088, $\overline{S1}$(DT/$\overline{R}$), $\overline{S0}$($\overline{DEN}$), QS1($\overline{INTA}$), QS0(ALE), $\overline{LOCK}$($\overline{WR}$), $\overline{RQ}/\overline{GT0}$(HOLD), and $\overline{RQ}/\overline{GT1}$ (HLDA) where the signal names in parenthesis are names common to the minimum mode of operation. The first five FETs (A1Q's 7010, 5010, 5016, 5014, and 5012) are tri-stated in response to the HLDA signal in the minimum mode by control line $\overline{NG}$ through switching transistors (A1Q's 7068, 3069, and 3065). The remaining three FETs (A1Q's 4014, 6010, and 4012) are not tri-stated in the minimum mode but are activated with the $\overline{MNQ}$ control line through switching transistor A1Q7070. The switching transistors provide +15 volts or −5 volts to the gate of each FET to activate or deactivate that FET.

NOTE

The signal lines on pins 24-31 of the microprocessor to the system under test have a maximum of 10 Ω of series resistance due to the presence of the FETs in the personality module circuitry.

Buffer A1U3030 ◇2

The integrated circuit A1U3030 serves as a buffer for signal lines $\overline{S0}$, $\overline{S1}$, $\overline{S2}$, QS0, QS1, $\overline{RQ}/\overline{GT0}$, and $\overline{RQ}/\overline{GT1}$.

The buffer receives these seven inputs from the Input Protection Hybrids. Refer to Tables 4-1 and 4-2 for the following discussion.

The first three buffered lines ($\overline{S0B}$, $\overline{S1B}$, and $\overline{S2B}$) carry status information to

1. A1U3020B for the latching of this status information

2. A2U1020 and A2U2020 to supply the ALE generator with status change information

3. A3U's 2030, 5030 and 7030 to indicate to the Queue Fill Decoder that a queue fill has occurred and information has been stored in the central processing unit's internal queue.

Buffered output QS0B connects to A3U's 5030A, 7010B, 3010A, 5020B, and 7030A.

Buffered output QS1B connects to A3U5030A and A3U5010C.

Both QS0B and QS1B carry information which describes bytes executed from the queue.

The buffered outputs $\overline{RQ}/\overline{GT0B}$ and $\overline{RQ}/\overline{GT1B}$ connect to A2U3010D and A2U3010C respectively to supply board 2 with information concerning the occurrence of a bus access request.

TABLE 4-1

STATUS LINE INPUTS

$\overline{S2}$ (M/$\overline{IO}$)	$\overline{S1}$ (DT/$\overline{R}$)	$\overline{S0}$ ($\overline{DEN}$)	CONDITION
0	0	0	INT ACK
0	0	1	READ I/O
0	1	0	WRITE I/O
0	1	1	HALT
1	0	0	CODEFETCH
1	0	1	READ MEM
1	1	0	WRITE MEM
1	1	1	IDLE

TABLE 4-2

QUEUE STATUS

QS1	QS0	QUEUE STATUS MEANING
0	0	No operation. Nothing taken from the queue.
0	1	The byte executed out of the queue was the first byte of an instruction.
1	0	Queue dump. Information dumped from the queue.
1	1	The byte executed out of the queue was a subsequent byte (not an instruction fetch, INFT).

Latch A1U3020B ◇2

The latch A1U3020B receives three inputs from the buffer A1U3030. When the latching signal ALE is low, the information present on input lines $\overline{S0B}$, $\overline{S1B}$, and $\overline{S2B}$ is latched on the output. When ALE is high, the latch acts as a transparent buffer to allow the information present on the output to follow the input.

The output line $\overline{S0L}(\overline{DEN})$ connects to A1U3010.

The output line $\overline{S1L}$(DT/$\overline{R}$) connects to A1U3010, A1Q5014, A2U's 2030A, 6020A, 3520A and A3U1010 and indicates the direction of data flow (transmit or receive).

The output line $\overline{S2L}$(M/$\overline{IO}$) connects to A1U3010, A1Q5012, A3U1020 and A2P6010 indicating the source or destination of the information (memory or input-output).

Demultiplexer A1U3010 ◇2

The integrated circuit A1U3010 acts as a demultiplexer for the input lines $\overline{S0L}(\overline{DEN})$, $\overline{S1L}$(DT/$\overline{R}$), and $\overline{S2L}$(M/$\overline{IO}$) producing the outputs $\overline{INTAX}$ and $\overline{CODEFETCH}$.

The first output, $\overline{INTAX}$, is inverted in U1020 on board 3 and connects to the NAND gate U1020C on board 2 to indicate an interrupt acknowledge condition is present. The second output, $\overline{CODEFETCH}$, connects to the buffer U1010 and U6020B on board 2 and A3U1020A and A3U1010 with information regarding bus operations taking place in the personality module.

Clock Converter ◇3

The Clock Converter circuit provides the PM 106/107 Personality Module with TTL level clock signals and the logic analyzer with ECL level clock signals.

The input CLK signal from the system under test (SUT) is protected against static discharge by an Input Protection Hybrid and a clamping diode (A1CR5070). The associated input circuitry attenuates the input while presenting a high input impedance to the SUT. The circuitry between pins 3 and 8 of the differential amplifier (A1U4070) provides hysteresis for enhanced noise immunity and provides feedback from the inverted output to the inverting input. A differential pair of outputs called CLOCK and $\overline{CLOCK}$ are the ECL level outputs from this differential amplifier to the logic analyzer. These two ECL level signals are also fed to transistor networks to aquire two TTL level signals, CLK and $\overline{CLK}$. Transistors A1Q3062 and A1Q3060 are the active pull-down and pull-up transistors for the TTL level $\overline{CLK}$ signal. Transistors A1Q3070 and A1Q3074 are the active pull-down and pull-up transistors for the TTL level CLK signal.

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Buffers A1U3035B and A1U3035H ◇3

The integrated circuits A1U3035B and A1U3035H serve as buffers for signal lines NMI, INTR, READY and $\overline{BHE}$. The NMI line provides the personality module with a non-maskable interrupt. The INTR line serves as a maskable interrupt to the personality module. The READY line, when asserted, allows the addition of a wait state (Tw) to be inserted between machine states T3 and T4. The $\overline{BHE}$ line, jumpered for operation (PM 107 only) by P6020, validates transferred data bytes. These lines originate at J7020 pins 33, 35, 37, and 13 respectively. After passing through the Input Protection Hybrids, they become inputs to A1U3035B at pins 11, 13, and 15 respectively, and A1U3035H pin 7. The buffered outputs at pins 9, 7, 5, and 3 are labeled NMIB, INTRB, READYB and $\overline{BHEB}$ which connect to J3070 pins 14, 13, 11, and 10 respectively.

Buffer A1U3020C ◇3

The integrated circuit A1U3020C serves as a buffer for the $\overline{BHE}$ line. When the latching signal address latch enable ALE is low, the information on the input pin 17 (from A1U3035H-3) is latched. When ALE is high, the buffer is transparent and the output pin 16 (to J3070-26) follows the input.

MIDDLE BOARD

Overview

The emulation circuitry found on board A2 includes the following circuits.

1. ALE Generator.
2. $\overline{DEN}$ Circuit.
3. Request Grant Generator.
4. Machine State Generator.
5. Request Grant (0 or 1) Divide-By-3.
6. Minimum/$\overline{Maximum}$ Mode Decoder.
7. Control Line Generators B and C.
8. $\overline{RESET3}$ Gate.
9. $\overline{WR}$ Flip-Flop.
10. $\overline{INTA}$ Gate.
11. Hold acknowledge detection circuitry.
12. $\overline{WAIT}$ and T1 (ESYNC) circuitry.
13. −5.2 Volt Regulator.
14. Miscellaneous buffers.

The block diagram of Figure 4-2 shows this circuitry in functional blocks. Refer to Figure 4-2 for an overview of assembly A2 and to aid in understanding the flow of signals to and from board A2.

Schematic diagrams are provided in the Diagrams section of the manual and are keyed to their respective circuit descriptions by numbered diamond symbols. For increased understanding of the detailed circuit descriptions, refer to both the appropriate schematic diagram and functional block diagram.

NOTE

Throughout the rest of this manual, a bar (—) over a signal name or portion of a signal name indicates that the signal is active when in the low state. For example, $\overline{HALT}$ indicates that $\overline{HALT}$ is an active low signal. R/$\overline{W}$ indicates that 1-READ, 0-WRITE.

If a bracket ([ ]) appears around a signal name, it indicates that the signal line is a dual function line and the signal may appear in the same form on the logic analyzer screen display in the 7D02 word recognizer. For example, the BHE[/QDUMP] line.

Component numbers in this manual are composed of an assembly number and a schematic circuit number. For example, A2U2030 indicates that component U2030 is located on assembly A2 (board 2) of the personality module.

A convention of minimizing lengthy parts references is used in this manual. For example, the reference A2U3050, A2U3040, and A2U3035 representing components on assembly A2 (board 2) may be referenced as A2U's 3050, 3040, and 3035.

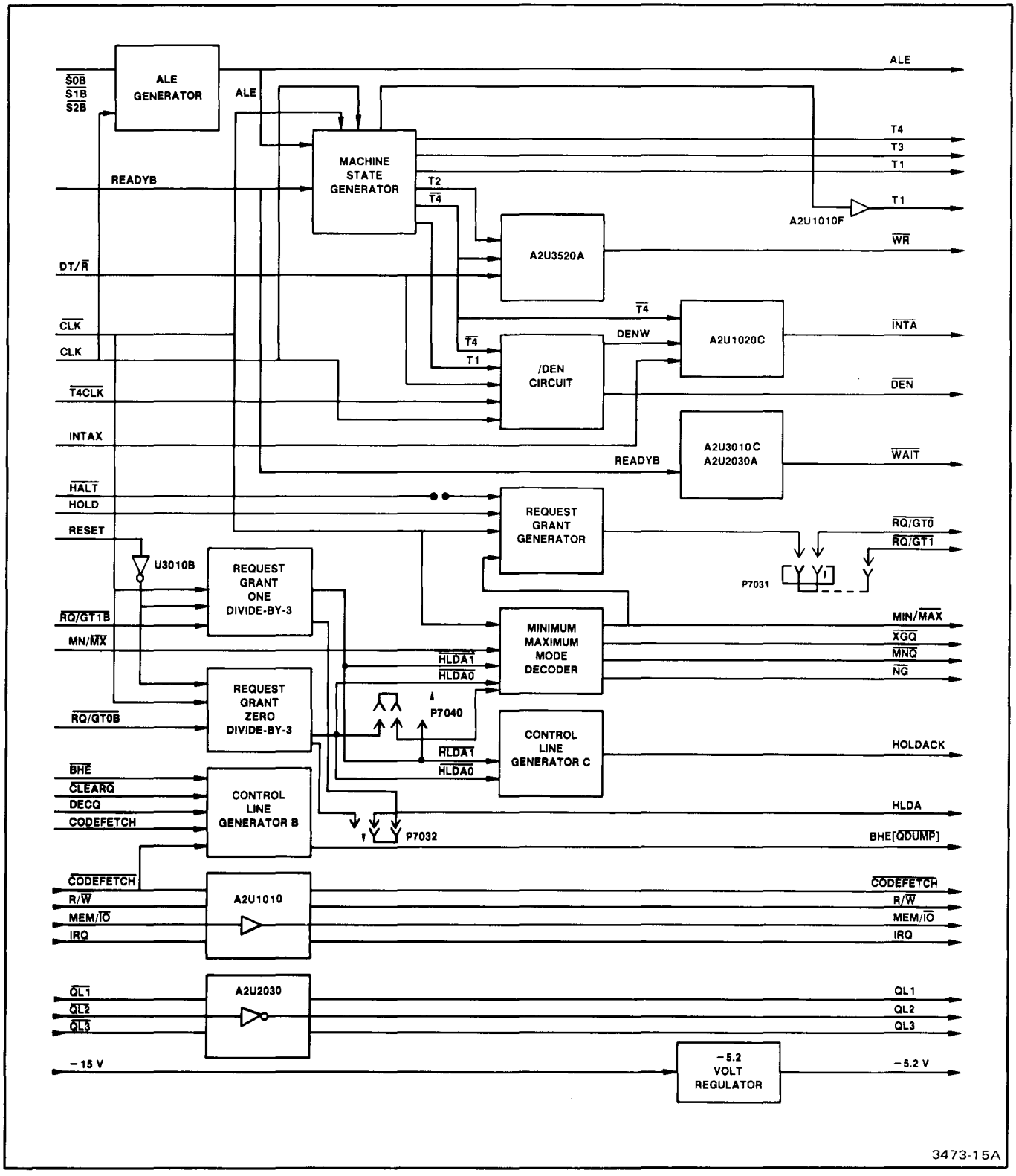

Figure 4-2. Middle board block diagram.

Machine State Generator 4

(Refer to the Specification section for signal line timing differences. Refer to Figure 4-3 for the following discussion.)

The Machine State Generator is basically a four stage shift register from which all bus activity is referenced. The ALE signal, produced by the ALE Generator, is shifted through to produce four machine states T1, T2, T3, and T4.

When $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ leave the idle state (no bus activity present) and ALE goes high, the inverted ALE signal from A2U2030C-7 provides a set pulse to A2U1030A-4 and pin 5 goes high, indicating machine state T1.

Machine state T2 is generated when T1 appears on A2U5020A-2 and is latched by the rising edge of $\overline{CLK}$ on the output pin 5. Meanwhile, ALE has been sent low again by the ALE Generator and this low is clocked through to A2U1030A-5 making T1 go low.

Machine state T3 is generated when T2 appears on A2U2010A-3 and is latched by the falling edge of CLK pin 5. The low condition from A2U1030A-5 is also latched on A2U5020A-5 and machine state T2 goes low. The READYB line and machine state T3 are inputs to A2U6030C pins 9 and 10 respectively.

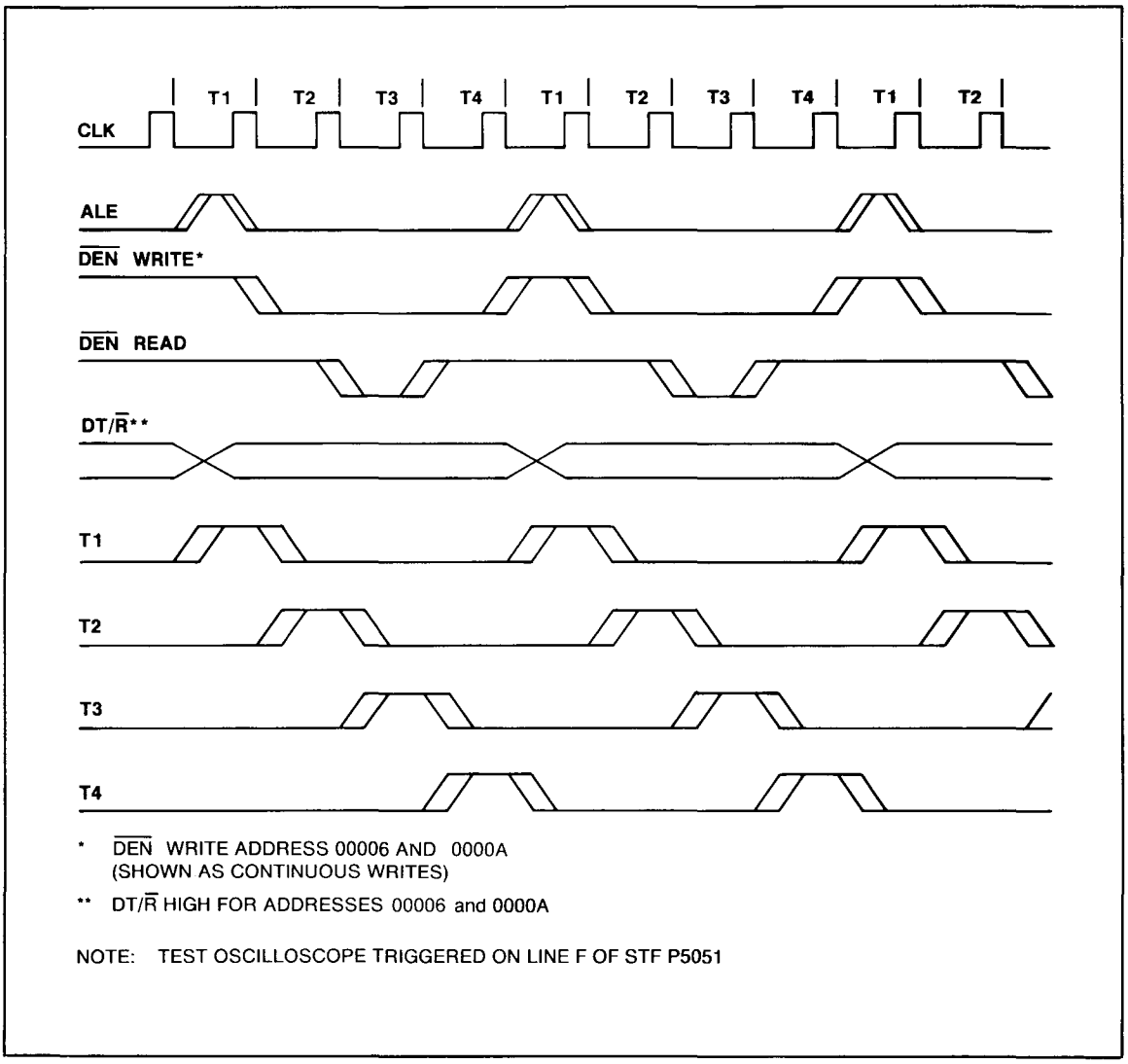

Figure 4-3. Bus cycle timing diagram.

If the system under test (SUT) requires "wait" states to compensate for a slow device in the system, a Tw machine state is inserted between machine states T3 and T4. To accomplish this, the READYB line is sent low. The low condition on A2U6030C pin 9 prevents the generation of machine state T4 and creates wait states until the SUT releases the READYB line to re-activate the Machine State Generator. As T3 is clocked through to A2U5020B-9, the low from A2U5020A-5 passes through A2U2010A and machine state T3 goes low.

Machine state T4 appears on A2U5030B-8 when the rising edge of $\overline{CLK}$ clocks A2U5020B. The low output from A2U2010A-5 (passing through A2U6030C) is shifted through to A2U5020B-8. Machine state T4 signals the end of the bus cycle and the bus is now in the idle state. If successive operations occur on the bus, the idle state will be passed through and another bus cycle sequence will be initiated. For a HALT instruction, A2U1030A of the Machine State Generator is cleared and T1 is not generated. $\overline{T1}$ to the logic analyzer receives a high signal.

ALE Generator ◇4

(Refer to the Specification section for signal line timing differences, to *The 8086 Family User's Manual*, an Intel publication, and to Figure 4-3 for the following discussion.)

The address latch enable (ALE) signal causes an address from the central processing unit (CPU) to be latched on ALE's falling edge. The ALE signal is generated at the beginning of machine state T1 when an address is placed on the bus. An ALE signal occurs on every clock cycle and when the clock goes high during T1, ALE goes low.

In the maximum mode, the system ALE signal is generated within the personality module (external to the CPU) from the maximum mode status lines $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$. These three status lines are high prior to machine state T4 of the previous bus cycle. At least one of these lines going low during the last third of machine state T4 (or first part of T1) indicates the start of a new bus cycle. This occurrence is cause for the generation of the ALE signal. Note that the CLK signal is high during the last third of all machine states.

Prior to $\overline{S0}$, $\overline{S1}$, or $\overline{S2}$ going low, A2U2020 has the following initial conditions.

1. Gate G1 output (to gate G5) is low due to A2U5030B in the reset condition by A2U1020B.

2. Gate G2 output (to gate G5) is always low due to input conditions on pins 11, 12, and 13.

3. Gate G3 output (to gate G5) toggles following CLK and is high during the last third of T4.

4. Gate G4 output (to gate G5) is high due to $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ all being high.

5. Gate G5 output (pin 8) is low due to gate G3 and/or gate G4.

When status lines $\overline{S0}$, $\overline{S1}$, or $\overline{S2}$ go low during the last third of machine state T4, gate G4 output goes low and gate G5 output (pin 8) is low due to gate 3. When the CLK signal goes low (the start of T1), all gate G5 inputs are low causing ALE to go active high. Since $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ remain low during machine state T1 and T2, and ALE must go low during the last third of T1, ALE is driven inactive low first by the CLK signal (gate G3) and held low by gate G1. When $\overline{S0}$ and $\overline{S1}$ are both high for a HALT instruction, NAND gate A2U6030 outputs a low 3 signal to A2U1030A, clearing it and stopping it from producng the T1 cycle.

$\overline{DEN}$ Circuit ◇4

(Refer to the Specification section for signal line timing differences, to *The 8086 Family User's Manual*, an Intel publication, and to Figure 4-3 for the following discussion).

The $\overline{DEN}$ Circuit produces:

1. The DENW1 (data enable write) signal which is used when data on the bus is being written.

2. The DENR (data enable read) signal which is used when data on the bus is being read.

3. The $\overline{DEN}$ (data enable) signal which is a combination of both DENW1 and DENR that is a minimum mode output generated during every bus cycle.

The DENW1 signal is generated in machine state T1 by A2U1030B with the generation of ALE by the ALE Generator. The rising edge of the ALE signal clocks the high input from A2U1030B-12 to the Q output pin 9. The DENW1 signal is an input to A2U6020A at pin 11. The DENW signal is generated when the falling edge of CLK shifts the high condition of machine state T1 from A2U2010B pin 12 to the $\overline{Q}$ output pin 8. The DENW signal is an input to A2U5030A-2 and A2U1020C-10. The rising edge of CLK in the middle of T2 clocks the high DENW signal from the input of A2U5030A to the output pin 5. This output, DENR, is an input to A2U6020A at pin 1. To select between the DENW1 and DENR functions, the DT/$\overline{R}$ signal line is set accordingly. The output of A2U6020A is the minimum mode signal, $\overline{DEN}$. The $\overline{DEN}$ signal will remain low until the bus cycle reaches machine state T4. During T4, the $\overline{T4}$ line clears the latch

A2U5030A and the DENR signal returns to the inactive low state. When the CLK and T4 signals are both high, the NANDed $\overline{T4CLK}$ signal becomes an active low and resets A2U1030B at pin 13 and A2U2010B at pin 10. The signals DENW1 and DENW then go to the inactive states.

Request Grant Zero Divide-By-3 ◇4

(Refer to the Specification section for signal line timing differences and to Table 4-3 for the following disucssion.)

The Request Grant Zero Divide-By-3 circuitry is used in the request, grant, and release sequence necessary for another controller to access the bus. This circuitry uses the $\overline{RQ/GT0B}$ signal to generate HLDA0 and $\overline{HLDA0}$ for both minimum and maximum modes of operation. The operation of this circuit is identical to that of the Request Grant One Divide-By-3 circuit, which uses the $\overline{RQ/GT1B}$ line as an in put to generate the HLDA1 and $\overline{HLDA1}$ lines.

After a reset of the circuitry by the $\overline{RESET3}$ signal (from A2U3010B), the idle conditions of A2U5010B-8 and A2U5010A-6 are both low. This condition is called the idle state.

Upon request of the bus by a controller, the Request Grant Generator produces a low on the $\overline{RQ/GT0}$ line ($\overline{RQ/GT1}$ line for the One Divide-By-3 circuit) that also appears on the $\overline{RQ/GT0B}$ line to the Divide-By-3 circuit at A2U3010D-11. The low on pin 11 combined with the toggling low condition of $\overline{CLK}$ on A2U3010D-12 will produce a positive pulse for the duration of $\overline{CLK}$ on pin 13. This is the first clock in Table 4-3 which shifts the preset high from A2U5010B-8 through to the output A2U5010A-6. The low shifted through to the $\overline{Q}$ output A2U5010A-6 is the inactive condition of the HLDA0 signal. The high on A2U5010A-5 remains a high condition for the $\overline{HLDA0}$ signal line.

The second low (the next clock) on the $\overline{RQ/GT0B}$ line, indicates the microprocessor has granted use of the bus. The high condition from A2U5010B pin 8 is shifted through to the $\overline{Q}$ output on A2U5010A pin 6. The HLDA0 line is now active (minimum mode only) and a hold acknowledge (HLDA) is generated to the system under test (SUT).

The third low on the $\overline{RQ/GT0B}$ line initiates the release (idle) state of the 3 cycle sequence. The low is clocked through to A2U5010B-8 and the previous low on that output (from clock 2) is shifted through to A2U5010A-6. This low condition on the $\overline{Q}$ output releases the active condition of the HLDA0 (hold acknowledge) signal. The low condition on A2U5010A-5 is toggled by this clock to a high condition, changing the $\overline{HLDA0}$ signal back to an inactive high. Both flip-flops are in their original idle conditions and ready for the next request grant signal.

TABLE 4-3

REQUEST GRANT ZERO DIVIDE-BY-3

CLOCK	PREHOLD U5010B-8	HLDA0 U5010A-6	MINIMUM MODE STATE	MAXIMUM MODE STATE
RESET (0)	0	0	NORMAL (running)	IDLE
				REQUEST
1st	1	0	HOLD REQUESTED	
				GRANT
2nd	0	1	HOLD ACKNOWLEDGED	
				RELEASE
3rd	0	0	NORMAL (running)	IDLE

Request Grant Generator 4

(Refer to Figure 4-4 for the following discussion).

The Request Grant Generator operates on a three phase cycle: request, grant, and release. The central processing unit (CPU) uses the request grant lines ($\overline{RQ/GT0}$ pin 31 of the CPU and $\overline{RQ/GT1}$ pin 30 of the CPU) as a bus access mechanism in the maximum mode. This function replaces the HOLD-HLDA function (pins 31 and 30 of the CPU) that are used for the minimum mode of operation.

A HOLD request signal is generated by the system under test (SUT) when another controller signals its wish to use the bus. The minimum mode HOLD signal (or $\overline{HALT}$ from the 7D02) is a low pulse on the $\overline{RQ/GT0}$ line (or $\overline{RQ/GT1}$ line if strapped) to the Request Grant Generator and the zero insertion force (ZIF) socket. The microprocessor will grant the use of the bus upon completion of the currently executing instruction with a second low pulse on that specific line causing a HLDA signal to be output in the minimum mode. When the requesting processor has finished, HOLD goes low (or $\overline{HALT}$ goes high) and a third low pulse from the Request Grant Generator on $\overline{RQ/GT0}$ (or $\overline{RQ/GT1}$) to the ZIF signals the restart of the original processor.

Requests. When a $\overline{HALT}$ signal arrives at A2U4010B-5 or a HOLD signal (minimum mode) combined with the MIN/$\overline{MAX}$ line passes through A2U4010D to A2U4010B pin 4, the result is a high output at pin 6. This output, connected to the latch A2U3530D at pin 13, when clocked by the positive-going edge of $\overline{CLK}$, will shift a high through to the out put pin 15. The pin 15 output and the high present on A2U3530C-11 are inputs to A2U4010A pins 2 and 1 respectively. The two high inputs on the NAND gate send the output pin 3 low. This active low is the request phase that will last for one clock cycle to request the use of the bus by another controller. The request pulse is transmitted to the following.

1. The zero insertion force (ZIF) socket.

2. The system under test (SUT).

3. The appropriate Request Grant Divide-By-3 circuit (0 or 1).

The next positive-going edge of $\overline{CLK}$ shifts the high at the latch A2U3530C-12 to the output pin 10. The high conditions (1s) will continue to be clocked through A2U3530D and C with no further effect on the request grant 0 or 1 lines.

Grant. When the microprocessor finishes the current task being performed, it responds to the request for use of the bus with a low pulse for one clock cycle on the appropriate grant line ($\overline{RQ/GT0B}$ or $\overline{RQ/GT1B}$). The corresponding Request Grant Divide-By-3 circuit will then produce an acknowledge signal (see the Divide-By-3 circuit description) on either HLDA0 or HLDA1. The hold acknowledge signal is transmitted to the SUT to indicate that use of the bus has been granted by the microprocessor.

Release. When the SUT is no longer in need of the bus, it sends a low pulse on the HOLD (or a high pulse for $\overline{HALT}$) signal line. The low condition passes through A2U4010B and is clocked into the first latch, A2U3530D, at pin 13. The high on the $\overline{Q}$ output pin 14 serves as one input to the NAND gate A2U4010C-9. With a high condition existing on pin 10 of A2U3530C as the other input at A2U4010C-10, the output pin 8 is low for one clock cycle. This low is the release pulse on the appropriate request grant line that is transmitted to the following.

1. The ZIF socket.

2. The SUT in the maximum mode.

3. The appropriate Request Grant Divide-By-3 line.

With the last pulse on the $\overline{RQ/GT0B}$ or $\overline{RQ/GT1B}$ line, the Divide-By-3 circuit signals the response by releasing the hold acknowledge signal. This action enables the system to resume normal operation.

Minimum/$\overline{\text{Maximum}}$ Mode Decoder 4

The Minimum/$\overline{Maximum}$ Mode Decoder provides signals to the minimum and maximum mode switching transistors to select the appropriate field effect transistors (FETs) for the minimum or maximum mode of operation. The decoding circuitry accepts inputs from the Request Grant Zero Divide-By-3 circuit, the Request Grant One Divide-By-3 circuit, and the system under test (SUT). The output switching signals are MIN/MAX and $\overline{XGQ}$ for the maximum mode and $\overline{MNQ}$ and $\overline{NG}$ for the minimum mode.

The minimum/$\overline{maximum}$ mode control line MN/$\overline{MX}$ is the input to the latch A2U3530B at pin 5. In the maximum mode, the MN/$\overline{MX}$ line from the SUT is low and on the first rising edge of $\overline{CLK}$, the low is clocked to the output A2U3530B-7. This output, called MIN/$\overline{MAX}$, is one of the two maximum mode switching signals. The other signal, $\overline{XGQ}$, is derived from $\overline{HLDA0}$, $\overline{HLDA1}$ and A2U3530B-6. When in the maximum mode, the minimum mode switching

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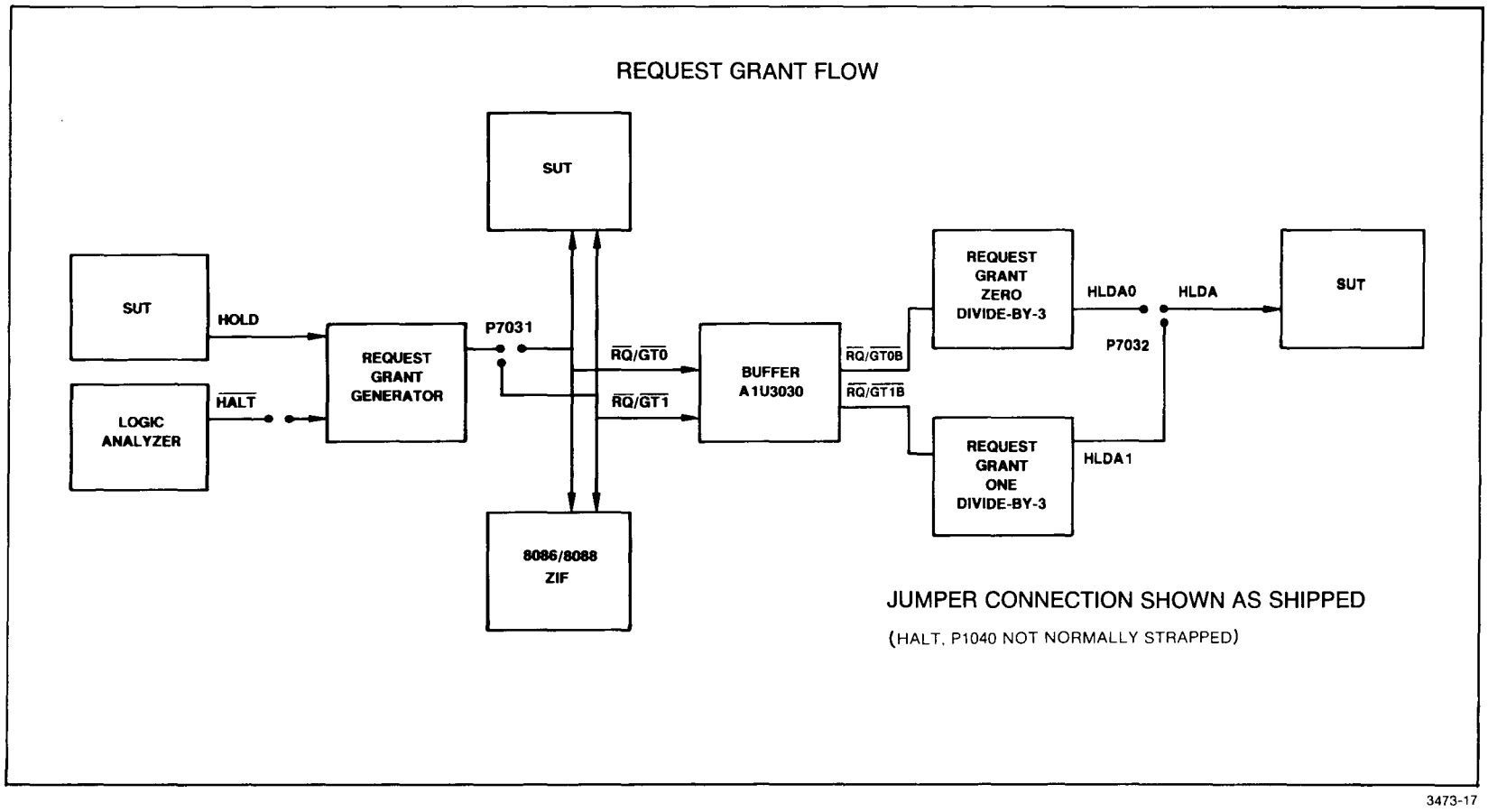

Figure 4-4. Request grant flow.

signals are inactive high. If a hold acknowledge state does not exist, the $\overline{HLDA1}$ is an inactive high and the One Divide-By-3 signal $\overline{HLDA0}$ from A2U5010A-5, is also high. The signals are inputs to A2U1020A-2, and 1 respectively. The three highs on the inputs of A2U1020A produce a low output on pin 12, which is the active state of the $\overline{XGQ}$ line.

NOTE

The PM 106/107 requires approximately 50 ms of switching time to change between the minimum and maximum modes of operation.

In the minimum mode of operation, a high condition exists on the MN/$\overline{MX}$ line at the input pin 5 of the latch A2U3530B. When a positive-going edge of $\overline{CLK}$ shifts the high through A2U3530B-7, the $\overline{Q}$ output $\overline{MNQ}$ goes to an active low condition. The other minimum mode switching signal, $\overline{NG}$, is derived from the MIN/$\overline{MAX}$ signal output from A2U3530-7 and the $\overline{HLDA0}$ output from A2U5010A-5. When in the minimum mode the maximum mode signals are inactive high. If a hold acknowledge state does not exist, the $\overline{HLDA0}$ and MIN/$\overline{MAX}$ lines are inactive high. These two highs on A2U6030D pins 12 and 13 respectively produce a low output on pin 11 indicating the active state of $\overline{NG}$. The low condition of $\overline{MNQ}$ and $\overline{NG}$ select the minimum mode of operation for the personality module.

$\overline{WR}$ Flip-Flop A2U3520A ◇4

(Refer to the Specification Section for signal line timing differences and to Table 4-2 for the following discussion).

The write ($\overline{WR}$) signal distinguishes whether a read operation from an I/O device or memory occurs or when a write operation to an I/O device or memory takes place. The flip-flop A2U3520A produces the output signal $\overline{WR}$ from the data transmit/receive (DT/$\overline{R}$) input signal.

The rising edge of machine state T2 will shift the condition of the DT/$\overline{R}$ line on A2U3520A-2 to the $\overline{Q}$ output pin 6. As shown by Table 4-2, when a write operation is taking place, the DT/$\overline{R}$ line will be high. This inverted condition appears as the output of $\overline{WR}$. During machine state T4, the signal is cleared back to an inactive state by the $\overline{T4}$ signal at A2U3520A-1.

$\overline{INTA}$ Gate A2U1020C ◇4

(Refer to the Specification section for signal line timing differences and to *The 8086 Family User's Manual*, an Intel publication, for the following discussion.)

The 3-input NAND gate A2U1020C produces the minimum mode interrupt acknowledge $\overline{INTA}$ signal for the system under test (SUT). The $\overline{INTA}$ signal is derived from the following inputs.

1. INTAX (inverted in A3U1020 from A1U3010).
2. $\overline{T4}$ (from A2U5020B-9).
3. DENW (from A2U2010B-8).

The acknowledge, $\overline{INTA}$, signal can only be active during machine states T2 and T3. When the interrupt signal INTAX status is active, the input to A2U2010C-9 is high. Since the input, $\overline{T4}$, on pin 11 is only low during machine state T4, the input is a high condition for machine states T1 through T3. The lockout for a non-active $\overline{INTA}$ signal during machine state T1 is the DENW signal on A2U1020C-10. DENW is not high during machine state T1 but goes high during machine state T2. With all inputs on A2U1020C pins 9, 10, and 11 high during machine states T2 and T3, the result is an active low $\overline{INTA}$ on pin 8 for these machine states.

$\overline{RESET3}$ Gate A2U3010B ◇5

The NOR gate A2U3010B provides a reset pulse called $\overline{RESET3}$ to both Request Grant Zero Divide-By-3 (A2U5010B-10 and A2U5010A-4) and Request Grant One Divide-By-3 (A2U6010B-10 and A2U6010A-4) circuits. The input is from the RESET signal line on pin 6 of A1U7010D-9. When the RESET signal is an active high, the output on pin 4 goes low and $\overline{RESET3}$ is then in the proper state to clear the Divide-By-3 circuits.

Control Line Generator C ◇4

(Refer to the Specification section for signal line timing differences.)

The Control Line Generator C circuitry provides the logic analyzer with a method of determining when a hold acknowledge condition exists within the personality module. This section is composed of the integrated circuits A2U6030A and A2U1010A with inputs $\overline{HLDA0}$ and $\overline{HLDA1}$ connecting to A2U6030A pins 1 and 2 respectively. When either input is in active low state (indicating a hold acknowledge condition), the output on A2U6030A-3 is high. This high, buffered in A2U1010A, becomes output control lines C5 and C7 (HOLDACK) to the logic analyzer.

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Buffer A2U1010 ◇5

The integrated circuit A2U1010 provides buffering to four control lines before they become outputs at the 68 Ω termination resistors to the logic analyzer. The four control line inputs at A2U1010-4, 6, 8, and 11 are the following.

1. R/$\overline{W}$ from A3U1010-8.
2. MEM/$\overline{IO}$ from A3U1010-6.
3. $\overline{CODEFETCH}$ from A1U3010-11.
4. IRQ from A3U2010A-3.

The four control line outputs on A2U1010-16, 14, 12 and 9 are the following.

1. R/$\overline{W}$ (C0) from P3010-10 to J1010-46.
2. MEM/$\overline{IO}$ (C1) from P3010-9 to J1010-47.
3. $\overline{CODEFETCH}$ (C2) from P3010-5 to J1010-4.
4. IRQ (C3) from P3010-6 to J1010-49.

Buffer A2U2030 ◇5

The integrated circuit A2U2030 serves as an inverting buffer to the three output lines (QL1, QL2, and QL3) of the Queue Level Tracker on board 3. These three input lines at A2U2030-12, 10, and 14 are the following.

1. QL1 from A3U3030-6 to P1010-16.
2. QL2 from A3U3030-14 to P1010-15.
3. QL3 from A3U3030-11 to P1010-17.

The three inverted outputs at A2U2030-11, 9, and 13 are the following.

1. QL1 from P3070-4 to J1010-26.
2. QL2 from P3070-3 to J1010-27.
3. QL3 from P3070-5 to J1010-28.

−5.2 Volt Regulator ◇5

The −5.2 Volt Regulator circuit supplies the personality module field effect transistors (FETs) with the necessary −5.2 volts for operation. The circuitry consists of the LM337 negative voltage regulator A2U7030 and associated circuitry. The input to the circuitry is the −15 volt supply. The output of the regulator is set by the resistors A2R 6034 and A2R6040 for a value of −5.2 volts.

Control Line Generator B ◇5

(Refer to Table 4-4 for the following discussion.)

TABLE 4-4

CONTROL LINE GENERATOR B
BHE[$\overline{QDUMP}$] LINE

$\overline{CODEFETCH}$ (Control Line C2) LOW		$\overline{CODEFETCH}$ (Control Line C2) HIGH	
BHE (byte high enable)	HIGH = VALID	$\overline{QDUMP}$ (queue dump)	HIGH = NO QUEUE DUMP
	LOW = INVALID		LOW = QUEUE DUMP OCCURRED

The Control Line Generator B circuit produces a multiplexed signal line called BHE[$\overline{\text{QDUMP}}$] (byte high enable [queue dump]).When $\overline{\text{CODEFETCH}}$ (C2) is low, this line reflects whether the high byte information is valid or not. When the $\overline{\text{CODEFETCH}}$ line is high, the line reflects information concerning the presence of a queue dump (information flushed from the queue) event from gate G2.

The output of A2U6020B is from either input condition of gate G1 or gate G2. Gate G1 uses inputs from lines $\overline{\text{BHE}}$ and $\overline{\text{CODEFETCH}}$ on A2U6020B pins 2 and 3 respectively. The $\overline{\text{CODEFETCH}}$ line, when high, enables the $\overline{\text{BHE}}$ line information through gate G1 to the output pin 6. Gate 2 uses inputs from the CODEFETCH and $\overline{\text{QDUMP}}$ lines on A2U6020B pins 5 and 4 respectively. The $\overline{\text{QDUMP}}$ information is available when the CODEFETCH line is active low.

When the the flip-flop A2U3520 is initialized by the $\overline{\text{CLEARQ}}$ signal on pin 13, the $\overline{\text{Q}}$ output pin 8 is high. When any decrement of the queue takes place, the DECQ line shifts an inverted high condition from the D input to the $\overline{\text{Q}}$ output pin 8. This active low signal on the $\overline{\text{QDUMP}}$ line remains until the $\overline{\text{CLEARQ}}$ signal resets the line to an inactive high.

BOTTOM BOARD

Overview

The queue follower circuitry found on board A3 includes the following circuits.

1. Queue Fill Decoder.
2. Count Decoder.
3. Queue Level Tracker.
4. Queue Dump Detector.
5. Interrupt Detector.
6. Instruction Fetch Tracker.
7. Control Line Generator A.
8. Miscellaneous buffers.

The block diagram of Figure 4-5 shows the circuitry in functional blocks. Refer to Figure 4-5 for an overview of assembly A3 to aid in understanding the flow of signals to and from the board.

Schematic diagrams are provided in the Diagrams section of the manual and are keyed to their respective circuit descriptions by numbered diamond symbols. For increased understanding of the detailed circuit descriptions, refer to both the appropriate schematic diagram and functional block diagram.

NOTE

Throughout the rest of this manual, a bar (—) over a signal name or portion of a signal name indicates that the signal is active when in the low state. For example, $\overline{\text{HALT}}$ indicates that $\overline{\text{HALT}}$ is an active low signal. R/$\overline{\text{W}}$ indicates 1-READ, 0-WRITE.

If a bracket ([ ]) appears around a signal name, it indicates that the signal line is a dual function line and the signal may appear in the same form on the logic analyzer screen display in the 7D02 word recognizer. For example, the BHE[/QDUMP] line.

Component numbers in this manual are composed of an assembly number and a schematic circuit number. For example, A3U2030 indicates that component U2030 is located on assembly A3 (board 3) of the personality module.

A convention of minimizing lengthy parts references is used in this manual. For example, the reference A2U3050, A2U3040, and A2U3035 representing components on assembly A3 (board 3) may be referenced as A3U's 3050, 3040, and 3035.

Queue Dump Detector ◇6

(Refer to Table 4-2 for the following discussion.)

The occurrence of a queue dump (information dumped out of the queue) is decoded in the NAND gate A3U5010C. The inputs are QS0V, QS1B, and CLK on A3U5010C pins 9, 10, and 11. When CLK is high, the conditions of QS0 (low) and QS1 (high) indicate the queue has been dumped. The resulting low on the output pin 8 is the $\overline{\text{CLEARQ}}$ signal which reinitializes the following circuits.

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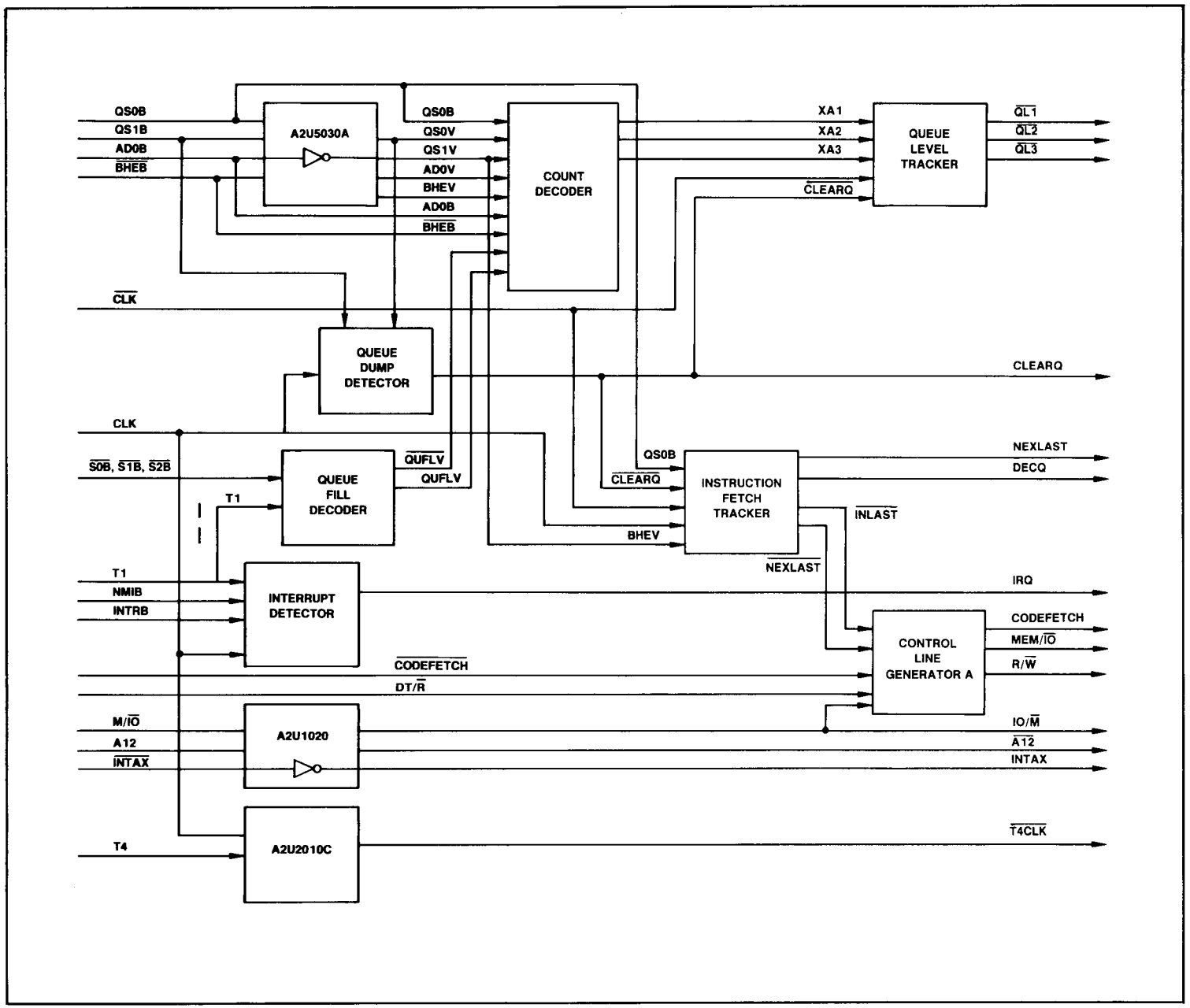

3473-18

Figure 4-5. Bottom board block diagram.

1. A3U3030-1, the Queue Level Tracker.

2. A2U3520B-13, the Control Line Generator B.

3. A3U1030A-1 and A3U1030B-13, the Instruction Fetch Tracker.

Inverter A3U5030A 6

(Refer to Tables 4-2 and 4-5 for the following discussion).

TABLE 4-5
BYTE SELECTION

(Only valid in a read/write operation, not valid during a queue fill operation)

BHE	A0	SELECTION
0	0	8086 WHOLE WORD 8088 ILLEGAL STATE
0	1	8086 UPPER BYTE ODD ADDRESS; 8088 ILLEGAL STATE
1	0	8086/8088 LOWER BYTE EVEN ADDRESS
1	1	8088 UPPER BYTE ODD ADDRESS; 8086 ILLEGAL STATE

The four input lines to buffer inverter A3U5030A are the following.

1. QS0B from A1U3030-5 to A3U5030-13.

2. QS1B from A1U3030-7 to A3U5030-1.

3. AD0B from A1U3030E-9 to A3U5030-5.

4. $\overline{\text{BHEB}}$ from A1U3035H-3 to A3U5030-3.

The output lines QS1V, BHEV, AD0V, and QS0V at A3U5030 pins 2, 4, 6, and 12 are used by the Count Decoder circuitry, the Queue Dump Detector, and the Instruction Fetch Tracker on assembly A3.

Inverter A3U1020 6

The three input lines to buffer inverter A3U1020 at pins 3, 5, and 13 are M/$\overline{\text{IO}}$, $\overline{\text{INTAX}}$, and A12. The output lines IO/$\overline{\text{M}}$, INTAX, and $\overline{\text{A12}}$ are described in the following.

1. IO/$\overline{\text{M}}$: A minimum mode output for the 8088 microprocessor found on schematic 2.

2. INTAX: One of the three inputs of U1020 on assembly A2 used to generate the $\overline{\text{INTA}}$ (interrupt acknowledge) signal.

3. $\overline{\text{A12}}$: An input to A1U2030 on schematic 1 used to select between the two EPROMs A1U2020 and A1U2030.

T4CLK Gate A3U2010C 6

The NAND gate A3U2010C provides the $\overline{\text{T4CLK}}$ signal (to the $\overline{\text{DEN}}$ Circuit) as a preset pulse to A2U2010B-10 and A2U1030B-13. The inputs are CLK and T4 (from A2U5020B-8) on pins 12 and 13 of A3U2010C. The output, $\overline{\text{T4CLK}}$, is from pin 11.

Interrupt Detector 6

The Interrupt Detector circuitry recognizes the presence of an interrupt on the non-maskable interrupt (NMIB) line and the interrupt (INTRB) line to provide the logic analyzer with a request for an interrupt on the IRQ(C3) control line. The circuitry recognizes the changing edge of the NMIB line and the level of the INTRB line. The output signal, IRQ(C3), will be active for the central processing unit (CPU) for at least one occurrence of machine state T4.

NOTE

When the NMIB interrupt is activated, the CPU latches this non-maskable interrupt with a higher priority than the INTRB interrupt, and control is transferred to the interrupt service routine. This routine performs the necessary steps to store important information from the CPU. For more information, refer to The 8086 Family User's Manual, an Intel publication.

The IRQ(C3) control line is normally low due to the input conditions (pins 1 and 2 of A3U2010A high). When the NMIB interrupt is sent high by the system under test (SUT), the positive-going edge is detected by the latches A3U2020B and A and a low is clocked to both $\overline{\text{Q}}$ output pins (8 and 6 respectively). The NMIB interrupt may now be sent

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low with no change to the Interrupt Detector circuitry. The low output from A3U2020A-6 sends the NAND gate A3U2010A-3 high (i.e., the active state of the IRQ line). If the interrupt occurs during machine state T1, the low-going $\overline{T1CLK}$ signal will temporarily send A3U2020A-6 back high. When $\overline{T1CLK}$ goes inactive high again, the low from A3U2020B-8 to A3U2020A-4 will send the $\overline{Q}$ output pin 6 low again. No change will occur in machine state T2, but in machine state T3, the $\overline{T3CLK}$ line clears A3U2020B-8 to a high output. The low from A3U2020A-6 ensures that the IRQ signal remains an active high during this time. No change occurs in machine state T4 and the IRQ line remains an active high. The next machine state, T1, sets the $\overline{T1CLK}$ line low which sets the output of A3U2020A-6 high. This condition sends the output of A3U2010A at pin 3 (IRQ) to a low.

The INTRB interrupt is set high by the SUT, inverted in A3U1020D, and connected to A3U2010A-1. The other input, A3U2010A-2, is normally high which sends the output pin 3 high (i.e., the active state of the IRQ line). When the SUT releases the high on the INTRB line, the resulting low on that line is detected and transmitted through A3U1020D and A3U2010A to send the IRQ signal to a low condition.

Count Decoder ◇6

(Refer to Tables 4-2, 4-4, and 4-5 for the following discussion.)

The Count Decoder monitors the $\overline{BHEB}$, AD0B, QS0B, and QS1B lines to decode the changes occurring in the queue level. This information is provided on the output lines XA1, XA2, and XA3 to the Queue Level Tracker for a zero, one, two, or seven (minus one) change in the latched value of the queue level. The XA1 and XA2 lines may be activated indepedently, but the XA3 line is used in conjunction with the XA2 line to obtain a decrement of the queue by a value of one.

XA1. The active high XA1 line from the Count Decoder circuitry will increase the latched value of the queue by one. The three conditions under which the XA1 line (pin 6 of A3U5010B) is activated are as follows.

1. Two bytes into the queue and one executed out of the queue.

2. An upper byte moved into the queue and nothing executed out of the queue.

3. A lower byte moved into the queue and nothing executed out of the queue.

A low condition can be produced on A3U's 7010B, 6010, or 7010A outputs for the XA1 line by any one of three distinct situations occurring within the personality module.

The signal lines BHEV, AD0V, QS0B, and QUFLV provide input information at A3U7010B pins 9, 10, 12, and 13 to describe one situation in which the XA1 line will be activated. The high condition of AD0V and BHEV indicate that two bytes, a whole word, have been moved into the queue. A high condition on QS0B shows that a byte, first or subsequent, has been removed from the queue. The final input line, QUFLV, being high confirms that a CODEFETCH operation has taken place. This increase of two bytes and decrease of one byte results in an increase of the queue level by one.

The signal lines QUFLV, AD0B, QS1V, and QS0V provide input information at A3U6010-1, 4, 22 and 12 to describe a second distinct increment-by-one condition. A high on the inverted status lines QS0B and QS1B show that no operation has taken place and nothing has been removed from the queue. The high state of AD0V indicates an upper byte is being addressed and a high on the QUFLV line confirms a CODEFETCH is taking place. A high byte moved into the queue increments the Queue Level Tracker by one.

The signal lines QS1V, QUFLV, QS0V, and $\overline{BHEB}$ provide input information at A3U7010A-1, 2, 4, and 5 to describe the third and last distinct increment-by-one condition. The high condition on inverted signal lines QS0V and QS1V show that nothing has been removed from the queue. The high on the $\overline{BHEB}$ line indicates a lower byte is being addressed and the high QUFLV line confirms a CODEFETCH. A low byte moved into the queue increments the Queue Level Tracker by one.

XA2. The active high XA2 line from the Count Decoder circuitry will increase the latched value of the queue by two. The condition under which the XA2 line (pin 12 of A3U5010A) becomes activated is: two bytes into the queue and nothing executed from the queue.

The increase-by-two line, XA2, is decoded by the gates A3U's 4010, 5010A, and 3010A. The lines QUFLV, QS0V, AD0V, QS1V and BHEV at A3U4010-1, 2, 5, 6, and 11 respectively provide the input information. High conditions on the inverted signal lines QS0V and QS1V indicate that nothing has been removed from the queue. The high on the QUFLV line confirms a CODEFETCH operation. The output on A3U4010-8 is an inverted active low on the input A3U5010A-2. The NAND gate A3U3010A at pin 3 provides a high condition on the XA2B line when a no-operation low condition is present on pin 1 and the QUFLV line is low on pin 2 of A3U3010A. The highs on A3U5010A-1 and 13 com-

bined with the low on pin 2 provide a high on the XA2 line to increment the queue level by a value of two.

XA3. The active high XA3 line from the Count Decoder circuitry will increase the latched value of the queue by five (four on pin 14 plus one on the carry input C0, pin 7 of A3U4030). The XA3 line is used only in conjunction with the XA2 line which results in a total increase of seven (5+2). In a 3 bit adder, an increase of seven is the same as a decrease of one. The condition under which these lines become activated is: A byte (high or low) is taken from the queue with no CODEFETCH event occurring to refill the queue.

The XA3 line, which represents to the Queue Level Tracker an increase of five, is used in conjunction with the XA2 line. The net result is an increase of the Queue Level Tracker by seven.

The low condition used to achieve this operation on the XA2B line is from the high states on the inputs A3U3010A-1,and 2. These highs indicate that a byte is being taken from the queue and a no-CODEFETCH condition exists. The low on the XA2B line is transmitted through the NAND gate A3U3010B with the resulting high activating the XA3 line. The state of having both lines high accomplishes the task of an increment-by-seven (i.e., a decrement-of-one) in the Queue Level Tracker.

Queue Level Tracker 6

(Refer to Table 4-6 for the following discussion).

The Queue Level Tracker provides the logic analyzer with information indicating the current number of bytes in the queue. This is accomplished with the increment lines XA1, XA2, and XA3.

On the rising edge of the $\overline{CLK}$ signal, the changes on the XA1, XA2, and XA3 lines from the adder A3U4030 are latched into A3U3030. One set of outputs, QL1-QL3, provide the updated queue level back to the adder. The second set of outputs, $\overline{QL1}$-$\overline{QL3}$, provide the updated queue level to the logic analyzer through the inverter buffer A2U2030. If the queue is dumped (all information is dumped from the instruction stream queue), the $\overline{CLEARQ}$ signal at A3U3030-1 will clear the latch A3U3030 and tracking of the new queue level will begin.

In the following tables, B3=A3U4030-15
B2=A3U4030-2
B1=A3U4030-6

[a] = PM 107 Illegal state
[b] = PM 106/107 Illegal state

Table 4-6

ADDER TABLE

Notes: C0 = 0
XA3 = 0
XA2 = 0

XA1	B3	B2	B1	QUEUE LEVEL
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5[a]
0	1	1	0	6[a]
0	1	1	1	7[b]
1	0	0	0	1
1	0	0	1	2
1	0	1	0	3
1	0	1	1	4
1	1	0	0	5
1	1	0	1	6
1	1	1	0	7[b]
1	1	1	1	0[b]

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Table 4-6 (cont)

Notes: C0 = 1
XA3 = 1
XA2 = 1

Illegal state:
C0=1
XA3=1
XA2=0

XA1	B3	B2	B1	QUEUE LEVEL
0	0	0	0	2
0	0	0	1	3
0	0	1	0	4
0	0	1	1	5[a]
0	1	0	0	6[a]
0	1	0	1	7[b]
0	1	1	0	0[b]
0	1	1	1	1[b]
1	0	0	0	3
1	0	0	1	4
1	0	1	0	5[a]
1	0	1	1	6[a]
1	1	0	0	7[b]
1	1	0	1	0[b]
1	1	1	0	1[b]
1	1	1	1	2[b]

Table 4-6 (cont)

Notes: C0 = 1
XA3 = 1
XA2 = 1

Illegal state:
C0=1
XA3=1
XA2=1
XA1=1

XA1	B3	B2	B1	QUEUE LEVEL
0	0	0	0	7[b]
0	0	0	1	0
0	0	1	0	1
0	0	1	1	2
0	1	0	0	3
0	1	0	1	4
0	1	1	0	5[a]
0	1	1	1	6[a]

Instruction Fetch Tracker 6

The Instruction Fetch Tracker monitors the conditions of the queue status lines QS0B and QS1V to produce the signals $\overline{\text{INLAST}}$ and $\overline{\text{NEXLAST}}$ which indicate that the last ($\overline{\text{INLAST}}$) or second-to-last ($\overline{\text{NEXLAST}}$) byte executed out of the queue was the first byte of an instruction. Three possible conditions (one at a time) can exist for bytes taken out of the queue.

1. INFT, the first byte of an instruction has been executed.

2. A subsequent byte has been executed.

3. The queue was dumped and the information in the queue was not executed.

The circuitry also produces a signal called DECQ that indicates when the queue has been decremented due to the execution of a byte out of the queue. The two flip-flops A3U5020A and B delay the information in the Queue Level Tracker and the Instuction Fetch Tracker so it will be sent to the logic analyzer at the proper time.

When the first byte of an instruction is executed out of the queue, a high condition, called INFTCLK, is produced at A3U7030A-6 via the queue status lines QS0B and QS1V. The high state at A3U7030A-6 is shifted by CLK to the output at A3U5020A-5, and becomes INFTCLKD. The shift registers A3U1030A and B generate the signals $\overline{\text{INLAST}}$ and $\overline{\text{NEXLAST}}$ from the INFTCLKD signal.

When a cleared queue condition (from a queue dump) occurs, the $\overline{\text{CLEARQ}}$ signal from the Queue Dump Detector resets the shift registers A3U1030A and B. The DECQ signal, from the NANDed combination of A3U5020B-9 and $\overline{\text{CLK}}$ inverted in A3U1020E, clocks the signal on A3U1030B-12 to the output pin 8. A low on this output is the active condition of the $\overline{\text{INLAST}}$ signal which indicates that the last byte executed out of the queue was the first byte of an instruction. When any subsequent byte is executed out of the queue, the low from A3U1030B-9 is shifted through A3U1030A to pin 5. This low on pin 5 (the $\overline{\text{NEXLAST}}$ signal) indicates that the second-to-last byte executed out of the queue was the first byte of an instruction.

Queue Fill Decoder 6

(Refer to Table 4-1 for the following discussion.)

The Queue Fill Decoder circuitry interprets the information provided on the status lines $\overline{\text{S0B}}$, $\overline{\text{S1B}}$, and $\overline{\text{S2B}}$ to determine when the queue fill event occurs.

The AND gate A3U7030B receives the inputs $\overline{\text{S1B}}$, $\overline{\text{S0B}}$, $\overline{\text{S2B}}$, and T1 at pins 9, 10, 12, and 13 respectively. When $\overline{\text{S1B}}$ and $\overline{\text{S0B}}$ are low and $\overline{\text{S2B}}$ and T1 are high, a queue fill condition (CODEFETCH) is indicated as a high on the output QUFLV at A3U7030B-8.

The NAND gate A3U2030B receives the inputs T1, $\overline{\text{S0B}}$, $\overline{\text{S1B}}$, and $\overline{\text{S2B}}$ at pins 9, 10, 12, and 13. When T1 and $\overline{\text{S2B}}$ are high and $\overline{\text{S0B}}$ and $\overline{\text{S1B}}$ are both low the inverted output $\overline{\text{QUFLV}}$ is low indicating a queue fill or CODEFETCH on pin 8. A change of any one of the inputs will send the output high.

Control Line Generator A 6

(Refer to Table 4-7 for the following discussion.)

TABLE 4-7

STATUS INDICATIONS IN THE ABSOLUTE MODE

CONTROL LINE	C2 [$\overline{\text{CODEFETCH}}$]	C1 M/$\overline{\text{IO}}$ [2LS-F]	C0 R/$\overline{\text{W}}$ [LST-F]
WRITE I/O	0	0	0
READ I/O	0	0	1
WRITE MEM	0	1	0
READ MEM	0	1	1
Q FILL (A20=1)	1	0	0
Q DUMP (A20=0)	1	0	0
LST-F	1	0	1
2LS-F	1	1	0
L&2LS	1	1	1

The Control Line Generator A circuitry provides the logic analyzer with two control lines, C0 (R/$\overline{\text{W}}$[LST-F]) and C1 (MEM/$\overline{\text{IO}}$[2LS-F]), each describing current bus operations or when the first byte executed out of the queue was the first byte of an instruction. The selection depends upon the condition of the $\overline{\text{CODEFETCH}}$ line. If the $\overline{\text{CODEFETCH}}$ line is low, control line C0 indicates whether the current bus operation is a read or a write. Likewise, if $\overline{\text{CODEFETCH}}$ is low, the control line C1 indicates whether the current bus operation is a memory access or an input-output access. Conversely, when $\overline{\text{CODEFETCH}}$ is high, the high C0 control line indicates that the last byte executed out of the queue was the first byte of an instruction. Also at this time, a high C1 control line indicates that the second-to-last byte executed

out of the queue was the first byte of an instruction. When both control lines C0 (R/$\overline{W}$[LST-F]) and C1 (MEM/$\overline{IO}$[2LS-F]) are high, during the time when $\overline{CODEFETCH}$ is also high, the indication present is that the last and second-to-last bytes executed out of the queue were both the first byte of an instruction.

The AND/OR INVERT package, A3U1010, decodes these signals using the signals $\overline{INLAST}$ (from A3U1030B of the Instruction Fetch Tracker), $\overline{NEXLAST}$ (from A3U1030A of the Instruction Fetch Tracker), $\overline{CODEFETCH}$ (from A1U3010), DT/$\overline{R}$ (status line $\overline{S1}$ from A1U3020B), and IO/$\overline{M}$ (status line $\overline{S2}$, inverted in A3U1020, from A1U3020B).

PERFORMANCE CHECK

INTRODUCTION

The procedures which follow provide a method of checking the operation and performance requirements of the PM 106/107 Personality Module. It is assumed that the 7D02 Logic Analyzer has already passed its performance check according to the 7D02 Service Manual Performance Check section.

The performance check uses test programs from the 067-1024-00 service test fixture (STF) to perform some of the following checks. The test fixture, normally used during troubleshooting or verification procedures, produces signals on address, data, control, and clock lines.

Equipment List

The test equipment or equivalent equipment listed in Table 5-1 is required for the performance check of the PM 106/107 Personality Module. Detailed operating instructions for use of some of the test equipment are included in the appropriate test equipment manuals.

Table 5-1

REQUIRED TEST EQUIPMENT

Description	Usage	Item (w/Tektronix No.)
Logic Analyzer	To provide a system for the PM106/107	TEKTRONIX 7D02 Logic Analyzer w/Option 02 (Timing Option); w/Option 03 (Expansion Option)
Timing Option Probe	Data acquitision	TEKTRONIX P6451 Data Acquisition Probe
Service Test Fixture	To provide test patterns to check the PM 106/107	TEKTRONIX P/N 067-1024-00 Service Test Fixture and Power Supply Module
Mainframe	To provide an operating system for the logic analyzer	TEKTRONIX 7603 Oscilloscope 100 MHz minimum
Test Oscilloscope	To provide an operating system for 7000-Series plug-ins	TEKTRONIX 7603 Oscilloscope 100 MHz minimum
Time Base Plug-in	Time base sweep for test oscilloscope	TEKTRONIX 7B53A 5 ns/div
Vertical Plug-ins (2 required)	Vertical input for test oscilloscope	TEKTRONIX 7A18 75 MHz minimum
Oscilloscope Probes (5 required)	To provide signal input to the test oscilloscope	TEKTRONIX P6105 100 MHz minimum
TM 500 Mainframe	To provide an operating system for the TM 500 plug-ins	TEKTRONIX TM 503 mainframe
Digital Multimeter	To test voltages and resistances	TEKTRONIX DM 501A Digital Multimeter
Test Leads High—Red (1 required); Low—Black (1 required)	Signal connection for the Digital Multimeter	Lead Set; Tektronix P/N 012-0427-00
Power Supply	To provide dc signal levels	TEKTRONIX PS 503A Power Supply
Pulse Generator	To provide test signal patterns	TEKTRONIX PG 508 Pulse Generator

Table 5-1 (cont)

Description	Usage	Item (w/Tektronix No.)
Signature Analyzer	To provide a system for taking signatures	SONY/TEKTRONIX 308 Data Analyzer
Cable Set	To provide convenient connection of the Timing Option Probe	Cable Set; Tektronix P/N 012-0800-00
Microprocessor Plug Pin Assembly (Optional)	Replacement pin assembly for broken microprocessor plug	Pin Assembly; Tektronix P/N 352-0536-00
Shorting Strap	To provide signal connection	Shorting strap wire approx. 20 cm long
Jumper Wire	To provide signal connection	Jumper wire with one end stripped and one end with a square pin receptacle
40 Pin Adapter Socket	Test adapter socket for setup and hold checks	Zero Insertion Force (ZIF) Socket; Tektronix P/N 136-0537-01 (1 required). Square Pin Row; Tektronix P/N 131-1614-00 (2 required) 1) Square pins soldered to ZIF pins 1, 17-38, and 40 2) Square pins not soldered to ZIF pins 2-16, and 39 3) Pins not soldered, shorted together for PG 508 output connection
Flat Blade Screwdriver	To open the plastic door on the service test fixture or the personality module	Slot Screwdriver; Tektronix P/N 003-0199-00
Cross Head Screwdriver	To disassemble the microprocessor plug	Phillips Head Screwdriver; Tektronix P/N 003-0341-00
Allen Wrench	To disassemble the personality module	3/32 inch Allen Wrench; Tektronix P/N 003-0108-00

Preliminary Setup

CAUTION

Always be certain to turn off the mainframe power before connecting or disconnecting the personality module or service test fixture to avoid damage to any of the instruments.

1. Turn off mainframe power to the logic analyzer at the oscilloscope mainframe.

2. Insert the ribbon cable plug labeled PERSONALITY MODULE - PM 100 SERIES into the receptacle labeled the same on the front of the 7D02.

3. Remove the plastic cover door on the back of the service test fixture (STF) using a flat blade screwdriver.

4. Check all of the STF jumper positions according to Table 5-2.

Table 5-2

STF JUMPERS (SELF POSITION)[a]

Plug Number	Jumper Position
P3050	Not Jumpered
P4040	Pins 2 and 3 (INT)
P4050	Pins 1 and 2 (SELF)
P5045	Pins 2 and 3 (0)
P5060	Pins 1 to 2

Timing Option: To 5051 on STF

Table 5-3

P6451 TIMING OPTION CONNECTION TO STF

Color Code	Wire#	P5051 (SELF) P5052 (PROG)
WHITE	GND	GND
BLACK	0	0
BROWN	1	1
RED	2	2
ORANGE	3	3
YELLOW	4	4
GREEN	5	5
BLUE	6	6
VIOLET	7	7
GRAY	C	C

5. Connect the timing option according to Table 5-3.

NOTE

If the optional harmonica cable is used with the P6451 Timing Option, the wires from the P6451 should be connected to the harmonica cable with the proper size square pins. The harmonica cable can then be used as a convenient connection to timing option pins P5051 or P5052.

6. Insert the timing option cable plug into the receptacle labeled TIMING on the front of the 7D02.

7. Connect the STF, power supply module, personality module, and timing option shown in Figure 5-1.

NOTE

Observe pin 1 orientation on the zero insertion force (ZIF) sockets and 40 pin plugs to ensure proper installation.

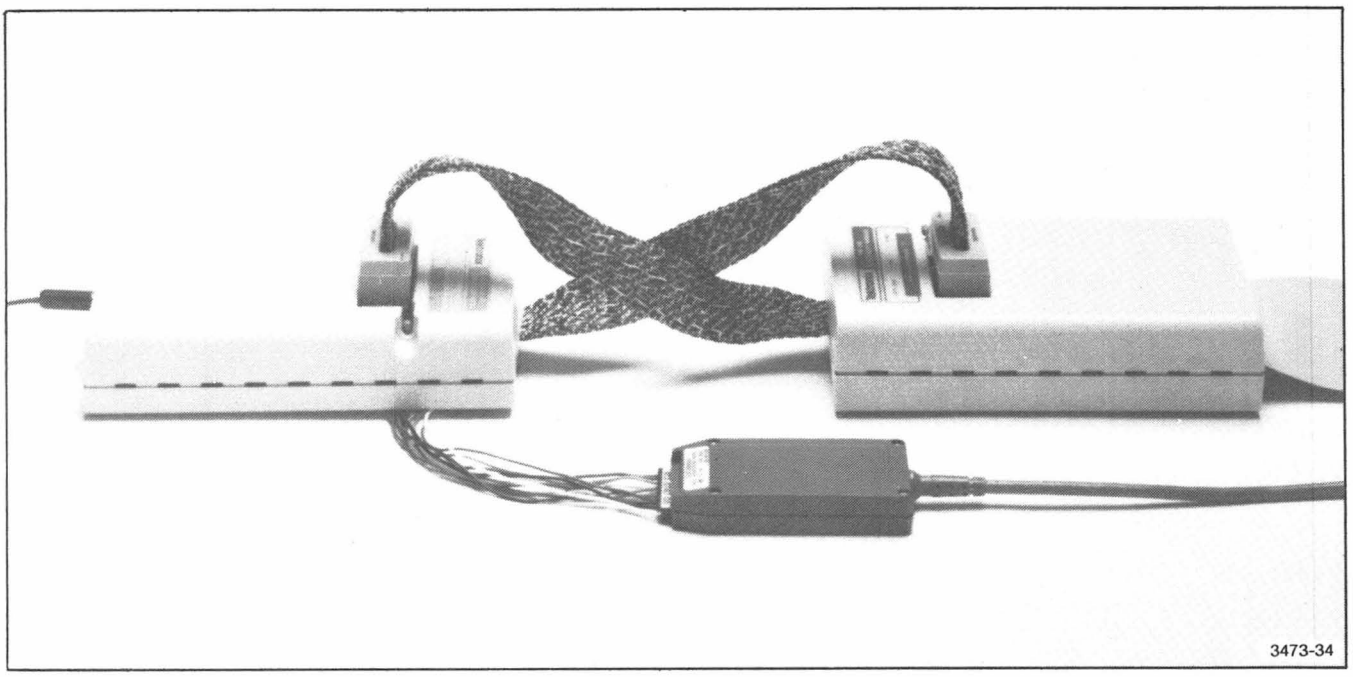


Figure 5-1. System layout.

DIAGNOSTIC MONITOR, PART I

Overview

The following describes the procedures needed to perform the 7D02 Diagnostic Modules for the personality module and timing option. These tests confirm the 7D02's ability to do the following.

1. Read and recognize pre-programmed word recognizers.

2. Compare the data in the personality module EPROMs to the logic information into the 7D02.

3. Fill the acquisition memory upon recognition of the appropriate word recognizers.

4. Compute acquisition memory checksums to checksum stored in the personality module EPROMs.

5. Display error codes.

Diagnostic Module 9 PER.MOD.-SYSTEM

To run the subtests of diagnostic module 9, use the following procedure.

NOTE

If the 7D02 screen displays the message PERSONALITY MODULE REQUIRED-POWER DOWN BEFORE ATTACHING!, NO CLOCK, or SLOW CLOCK, refer to the error list in the Maintenance and Troubleshooting section.

1. Turn on the mainframe power and depress any front panel key within two seconds. Keep the key down for at least five seconds to simulate a keyboard failure. Simulating a keyboard failure allows entry into the DIAGNOSTIC MONITOR.

2. Press the X key to get the DIAGNOSTIC MONITOR menu.

3. Press the 9 key to test the PER.MOD.-SYSTEM (personality module system).

4. Press the E key to select ENABLE LOOPING.

5. Press the START key to run Test 1.

6. A number, such as 0801-XX (the part number of the personality EPROM), is associated with Test 1 and is normal.

7. Wait at least 5 seconds and press the START key to run the next test.

8. Repeat part 7 until all seven tests have been completed.

9. A number associated with any test other than Test 1 is a failure. A number associated with any PASS message indicates a transient failure. A number associated with a FAIL message indicates a solid failure. Write down all numbers associated with PASS or FAIL messages. Refer to Diagnostic Module 9 PER.MOD.-SYSTEM, in the Maintenance and Troubleshooting section, for any failures.

10. Press the START key, then the X key to return to the menu.

Diagnostic Module B TIMING OPTION

To run the subtests of diagnostic module B, use the following procedure.

NOTE

Diagnostics for the timing option will not completely check the personality module. For further verification, complete the performance check.

1. If the 7D02 Diagnostic Module 9 PER.MOD.-SYSTEM was previously run, continue to part 2. If not, perform parts 1 and 2 of the PER. MOD.-SYSTEM test.

2. Press the B key to run the TIMING OPTION module.

3. Press the E key to select ENABLE LOOPING.

4. Press the START key.

5. Wait for five seconds in between all tests. Using the START key, run the remaining two tests.

6. A number associated with any test is a failure. A number associated with a PASS message indicates a transient failure. A number associated with a FAIL message indicates a solid failure. Write down all numbers associated with PASS or FAIL messages. Refer to 7D02 Diagnostic Module B TIMING OPTION, in the Maintenance and Troubleshooting section, for any failures.

FUNCTIONAL CHECKS, PART II

Overview

In performing the following checks, it is assumed that the PER.MOD.-SYSTEM and TIMING OPTION diagnostic modules have been run and the preliminary setup of equipment still exists. If not, perform the preliminary setup and diagnostic module tests before entering the following base program.

Base Program

1. Turn the mainframe power off, then on again.

2. When the logic analyzer finishes with the POWER-UP VERIFICATION, the 7D02 will be in the immediate mode (the lower band of inverse video will contain the message DISPLAY ← PROGRAM).

3. Press the WD RECOGNIZER key.

4. Using the CURSOR control keys, move the cursor to the ADDRESS box and enter 80000.

5. Move the cursor to the MIN/MAX MODE box and enter a 1 for the minimum mode tests.

6. Press the [ ] key.

7. Press the TRIGGER key.

8. Move the cursor to the STANDARD CLOCK QUAL. box and enter a 1 for USER CLOCK QUAL.

9. Enter a 0 in the FALLING EDGE OF CLOCK box to select RISING EDGE OF CLOCK.

10. Move the cursor to the STANDARD CLK SYNTHESIS box and enter a 1 for USER CLOCK SYNTHESIS.

11. Move the cursor to the 2 box of the DELAY CLOCK BY option.

12. Enter a 0 for no delay.

13. Press the TRIGGER key.

14. Enter a 1 for the TIMING trigger.

15. Enter a 1 for CENTERED trigger in the BEFORE DATA box.

16. Move the cursor to the ARM ASYNC box.

17. Enter a 0 for SYNC, TRIGGER IMMEDIATE.

18. Press the [ ] key.

19. Press the END key to complete the base program.

20. Position the STF jumpers according to Table 5-4.

Table 5-4

STF JUMPERS ($\overline{\text{PROG}}$ POSITION)[a]

Plug Number	Jumper Position
P3050	Not Jumpered
P4040	Pins 2 and 3 (INT)
P4050	Pins 2 and 3 ($\overline{\text{PROG}}$)
P5045	Pins 2 and 3 (0)
P5060	Pins 1 and 2

[a]Timing Option: To 5052 on STF

Test 1. Minimum mode lines HOLD and HLDA, $\overline{WR}$, M/$\overline{IO}$ (8086), IO/$\overline{M}$ (8088), DT/$\overline{R}$, $\overline{DEN}$, ALE, and $\overline{INTA}$

1. Press the START key.

2. Did the 7D02 trigger?

   - If no, refer to ERROR 4, in the Maintenance and Troubleshooting section, for troubleshooting aid.

   - If yes, proceed with part 3.

3. Move the cursor to the MAIN box and enter a 1 for the TIMING diagram display.

4. Compare the screen display to Figure 5-2.

NOTE

Exact timing of HOLD and HLDA (screen timing lines 0 and 1) changes with the clock frequency. The positive-going transition of HOLD must occur before the positive-going transition of HLDA. The PM 107 uses screen timing line 3 (M/$\overline{IO}$) inverted as compared to the PM 107, except during HLDA. Screen timing lines 2 through 5 ($\overline{WR}$, M/$\overline{IO}$, DT/$\overline{R}$, and $\overline{DEN}$) are tri-stated during HLDA. The return-high timing after tri-state is not critical.

5. If desired, compare the binary state table of Figure 5-3 by moving the cursor to the TIMING DIAGRAM box and entering a 0 for STATE DISPLAY.

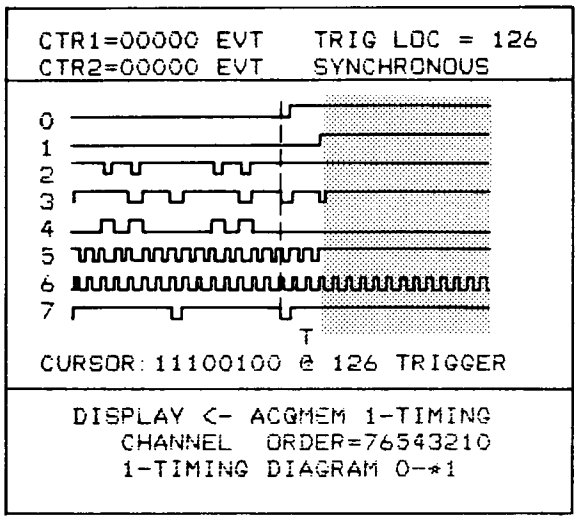
6. Using the DATA SCROLLING keys, compare the state display to Figure 5-3 (A-PM 106, B-PM 107).

NOTE

The Xs of Figure 5-3 imply that either a value of 1 or 0 is acceptable.

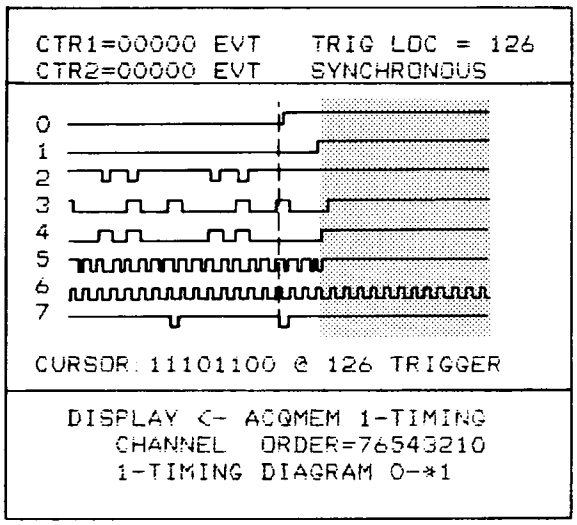
Refer to ERRORS 5-12 in the Maintenance and Troubleshooting section, for troubleshooting aid.

7. Return to the TIMING DIAGRAM by moving the cursor to the STATE DISPLAY box and entering a 1.



3473-19

Figure 5-2A. Timing diagram, minimum mode - PM 106 only.



3473-20

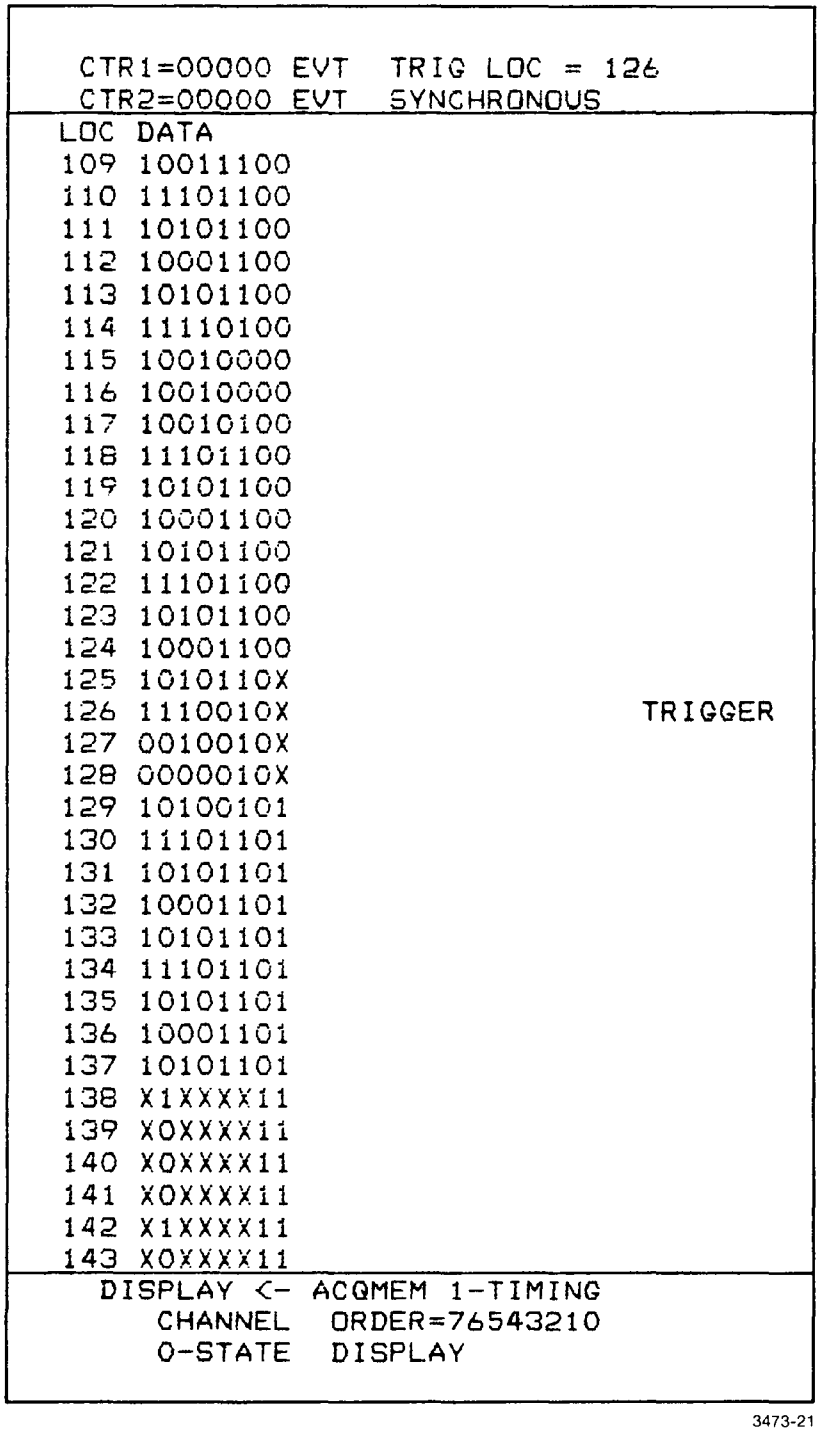
Figure 5-2B. Timing diagram, minimum mode - PM 107 only.

8. Press the IMMEDIATE, DISPLAY, and PROGRAM keys in sequence.

Test 2A. Maximum Mode Lines $\overline{RQ}$/$\overline{GT0}$, $\overline{LOCK}$, $\overline{S2}$, $\overline{S1}$, $\overline{S0}$, QS0, and QS1

1. If the base program prior to Test 1 has not been entered, perform parts 1 through 20 of the base program. Proceed to part 2.

2. Using the CURSOR control keys, enter the following correction in the base program.



3473-21

Figure 5-3A. State display, minimum mode - PM 106 only.

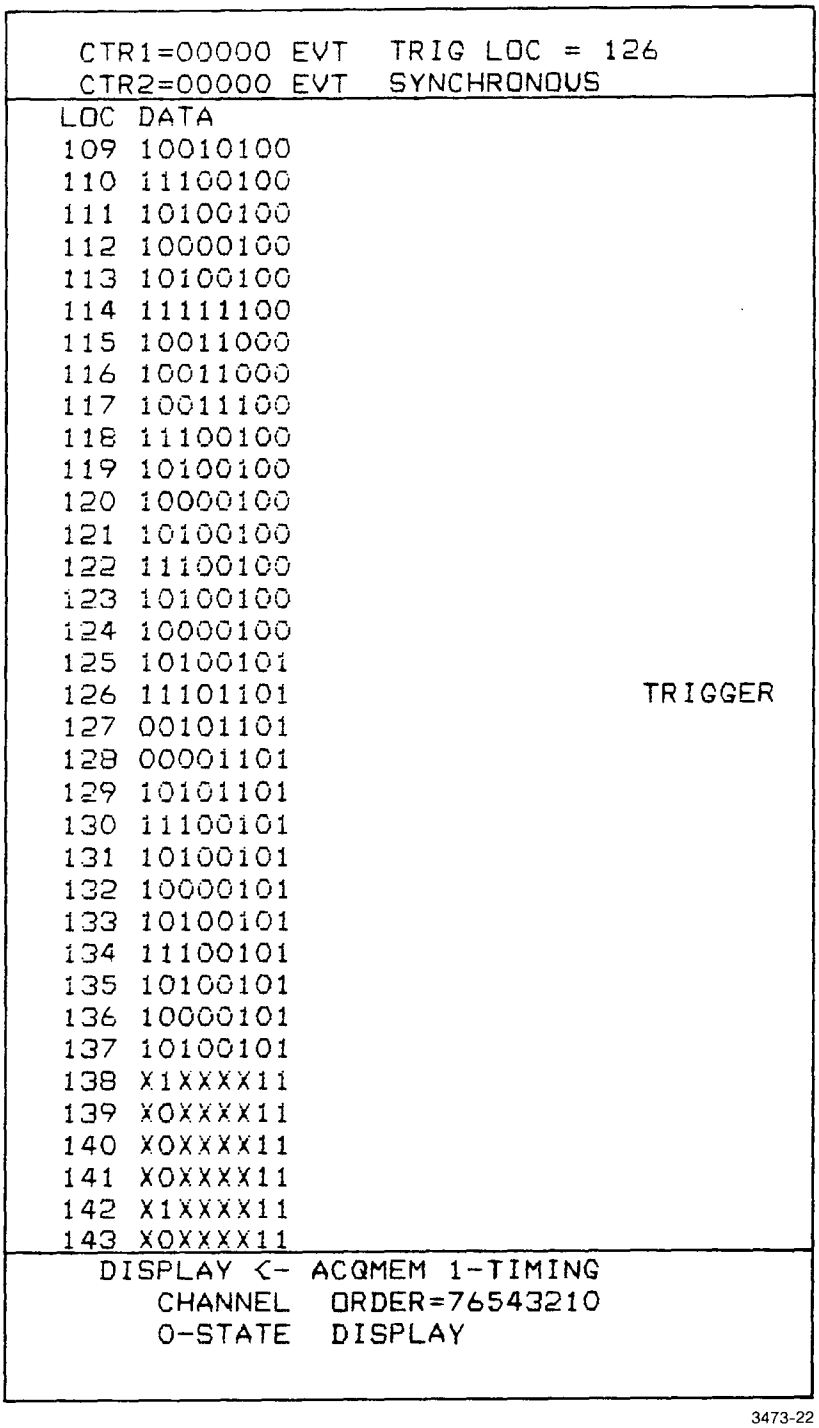


Figure 5-3B. State display, minimum mode - PM 107 only.

a. The MIN/MAX MODE box should be set to 0 for the maximum mode tests.

b. RISING (or FALLING) EDGE OF CLOCK box in the TRIGGER MAIN section should be set to 1 for FALLING EDGE OF CLOCK.

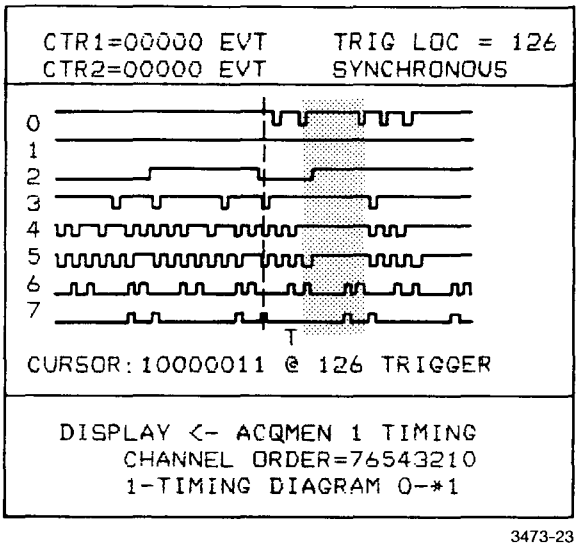
3. Press the START key.

4. Did the 7D02 trigger?

- If no, refer to ERROR 13, in the Maintenance and Troubleshooting section, for troubleshooting aid.
- If yes, continue to part 5.

5. Move the cursor to the MAIN box and enter a 1 for the TIMING diagram.

6. Compare the screen display to Figure 5-4.



3473-23

Figure 5-4. Timing diagram, maximum mode - PM 106 and PM 107.

NOTE

Screen Timing lines 2-5 ($\overline{LOCK}$, $\overline{S2}$, $\overline{S1}$, and $\overline{S0}$) are tri-stated during $\overline{RQ}/\overline{GT0}$ between the second and third pulses. The return-high timing during tri-state is not critical.

7. If desired, compare the STATE DISPLAY of Figure 5-5 by moving the cursor to the TIMING DIAGRAM box and entering a 0 for the STATE DISPLAY.

8. Using the DATA SCROLLING keys, compare the STATE DISPLAY to Figure 5-5.

9. Return to the TIMING DIAGRAM by moving the cursor to the STATE DISPLAY box and entering a 1.

NOTE

Refer to ERRORS 14-18, in the Maintenance and Troubleshooting section, for troubleshooting aid.

Test 2B. Maximum Mode Line $\overline{RQ}/\overline{GT1}$

1. Press the IMMEDIATE, DISPLAY, and PROGRAM keys in sequence.

2. Using the CURSOR control keys, move the cursor to the ADDRESS box and enter 80400.

3. Press the START key.

4. Move the cursor to the MAIN box and enter a 1 for the TIMING diagram.

5. Compare the screen display to Figure 5-6.

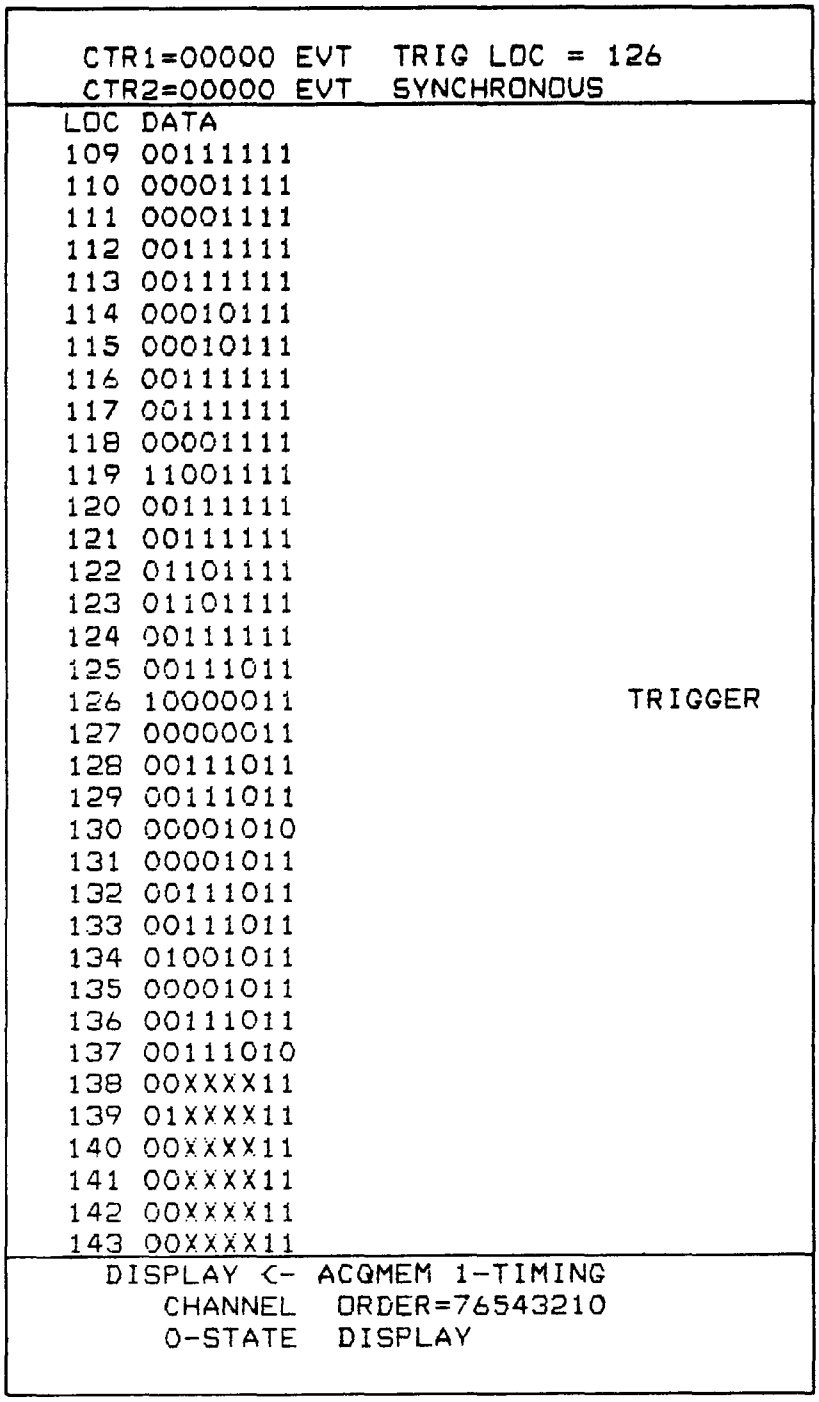
NOTE

Refer to ERROR 14, in the Maintenance and Troubleshooting section, for troubleshooting aid.

Test 3A. Status Display at Address 80000

Enter the following base program.

1. Turn the oscilloscope mainframe power off, then on again, to clear all previous programs.



3473-24

Figure 5-5. State display, maximum mode - PM 106 and PM 107.

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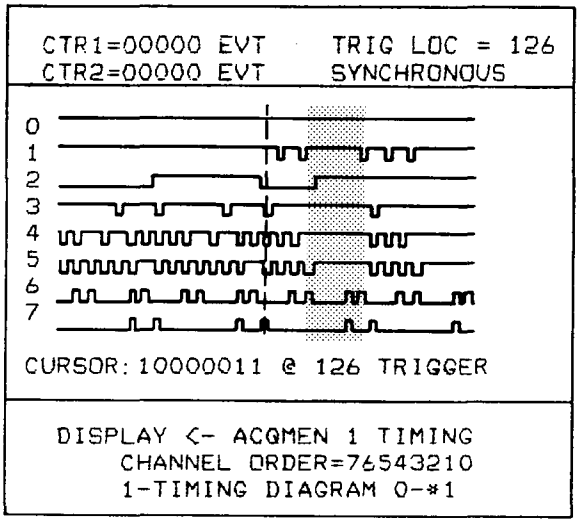


3473-25

Figure 5-6. Timing display $\overline{RQ}/\overline{GT1}$, maximum mode - PM 106 and PM 107.

2. Press the WD RECOGNIZER key.

3. Using the CURSOR control keys, move the cursor to the ADDRESS box and enter 80000.

4. Move the cursor to the MIN/MAX MODE box and enter a 1 for the minimum mode.

5. Press the TRIGGER, END, and START keys.

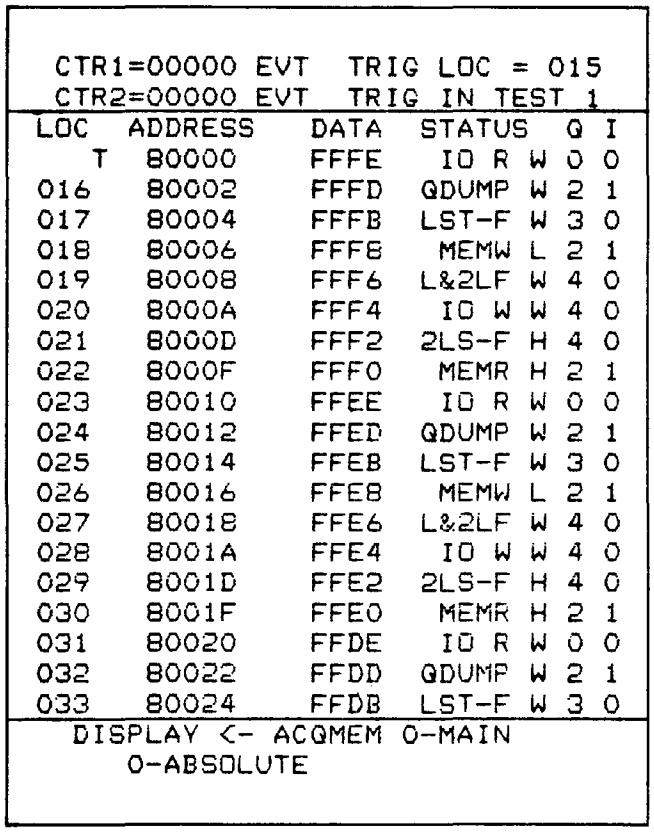
6. Enter a 0 for an ABSOLUTE listing.

7. Compare the screen display to Figure 5-7 (A or B).

8. Press the IMMEDIATE, DISPLAY, and PROGRAM keys in sequence.

9. Move the cursor to the MIN/MAX MODE box and enter a 0 for the maximum mode.

10. Press the IMMEDIATE, STORE MEM, and ACQ MEM keys in sequence.



3473-26

Figure 5-7A. Absolute display, address 80000 - PM 106 only.

11. Move the cursor to the EXECUTE field with the CURSOR right arrow (→) key.

12. Press the FORMAT key.

13. Move the cursor to the HIGHLIGHT MEMORY DIFFERENCE? box and enter a 0 for yes.

14. Press the FORMAT and START keys in sequence.

15. Check the screen display for highlighted errors.

NOTE

Refer to ERRORS 19 and 20, in the Maintenance and Troubleshooting section, for troubleshooting aid.

```
CTR1=00000 EVT  TRIG LOC = 127
CTR2=00000 EVT  TRIG IN TEST 1
LOC   ADDRESS   DATA  STATUS  Q I
  T    80000     FE     IO R  0 0
128    80002     FD    QDUMP  1 1
129    80004     FB    LST-F  1 0
130    80006     F8     MEMW  0 1
131    80008     F6    L&2LF  1 0
132    8000A     F4     IO W  1 0
133    8000D     F2    2LS-F  1 0
134    8000      F0     MEMR  7 1
135    80010     EE     IO R  0 0
136    80012     ED    QDUMP  1 1
137    80014     EB    LST-F  1 0
138    80016     E8     MEMW  0 1
139    80018     E6    L&2LF  1 0
140    8001A     E4     IO W  1 0
141    8001D     E2    2LS-F  1 0
142    8001F     E0     MEMR  7 1
143    80020     DE     IO R  0 0
144    80022     DD    QDUMP  1 1
145    80024     DB    LST-F  1 0
DISPLAY <- ACQMEM 0-MAIN
   0-ABSOLUTE
```

3473-27

Figure 5-7B. Absolute display, address 8000 - PM 107 only.

Test 3B. IRQ (from INTR) At Address 80C00 Through 80C10

1. Press the IMMEDIATE, DISPLAY, and PROGRAM keys in sequence.

2. Using the CURSOR control keys, move the cursor to the ADDRESS box and enter 80C00.

3. Press the START key.

4. Press the IMMEDIATE, STORE MEM, and ACQ MEM keys in sequence.

5. Move the cursor to the EXECUTE field with the CURSOR right arrow (→) key.

6. Check the screen display to verify that the interrupt column (far right column on the absolute screen display) is solid 1s from 80C00 through 80C10.

7. Press the IMMEDIATE, DISPLAY, and PROGRAM eys in sequence.

8. Move the cursor to the MIN/MAX MODE box and en- er a 1 for the minimum mode.

9. Press the START key.

10. Check the screen display for highlighted differences.

NOTE

Refer to ERROR 21, in the Maintenance and Troubleshooting section, for troubleshooting aid.

Test 3C. READY Line

1. Press the IMMEDIATE, DISPLAY, and PROGRAM keys in sequence.

2. Using the CURSOR control keys, move the cursor to the ADDRESS box and enter 80BX0.

3. Move the cursor to the MIN/MAX MODE box and enter an X.

4. Press the START key.

5. Check to verify that the upper inverse video band flashes the RUNNING message (blinking SLOW CLOCK message is normal).

6. Check that the 7D02 does not trigger. Wait at least 10 seconds.

7. Press the STOP key.

NOTE

Refer to ERROR 22, in the Maintenance and Troubleshooting section, for troubleshooting aid.

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Test 4. $\overline{\text{HALT}}$ Function

Refer to the $\overline{\text{HALT}}$ Line Strapping Procedure in the Maintenance and Troubleshooting section to implement.

1. To clear all previous word recognizer selections, turn the mainframe power off, then on again.

2. Press the WD RECOGNIZER key.

3. Using the CURSOR control keys, move the cursor to the ADDRESS box and enter 72152.

4. Press the TRIGGER key.

5. Move the cursor to the SYSTEM UNDER TEST CONT. box and enter a 1 for SYSTEM UNDER TEST HALT.

6. Press the END key.

7. Connect a jumper strap from the PM 106/107 test point TP5060 (H) to the STF $\overline{\text{HALT}}$ test point TP5040.

8. Position P4050 on the STF to the $\overline{\text{PROG}}$ position.

9. Position P5050 on the STF to the MIN position.

10. Press the IMMEDIATE, GOTO, and 2 keys in sequence.

11. Press the cursor right arrow (→) key to move the cursor to the EXECUTE field.

12. Connect channel 1 of the test oscilloscope to J3010 pin 1, to observe the HOLDACK (C5 or C7) line. Trigger the oscilloscope on the falling edge of the waveform.

13. Check that the waveform has a low-going pulse duration of between 200 ms and 300 ms.

NOTE

Refer to ERROR 23, in the Maintenance and Troubleshooting section, for troubleshooting aid.

PERFORMANCE CHECK, PART III

Overview

The following test checks the setup and hold times for lines AD0 through AD16 (PM 106 only) and AD0 through AD7 (PM 107 only).

Preliminary Setup

1. Set the test oscilloscope as follows.

   a. HORIZONTAL TIME/DIV . . . 2 ns/div

   b. HORIZONTAL DELAY TIME/DIV . . . 100 ns/div

   c. MAG . . . vary as required

   d. TRIGGER . . . channel 4, + slope

2. Connect the test oscilloscope vertical as follows.

   a. Channel 1 . . . STF P5052-10 (labeled C: CLOCK)

   b. Channel 2 . . . STF P5052-8 (labeled 6: ALE)

   c. Channel 3 . . . PG 508 OUTPUT

   d. Channel 4 . . . PG 508 TRIG OUT

3. Set the PG 508 as follows.

   a. TRIG'D/GATED . . . + SLOPE

   b. MODE . . . as specified

   c. PERIOD . . . EXT TRIG OR MAN

   d. DELAY . . . 0.1 ns (vary as required)

e. DURATION . . . 0.1 ns (vary as required)

f. TRANSITION TIME . . . 5 ns

g. LEADING . . . ×1

h. TRAILING . . . ×1

i. OUTPUT (volts) . . . LOW LEVEL to 0 volts, HIGH LEVEL to +5 volts

4. Connect the PG 508 as follows.

a. TRIG/GATE IN . . . STF P5051-5 (labeled f)

b. Check PG 508 output level with multimeter before connecting.

c. Connect PG 508 output to AD0 through AD16 using the 40 pin adapter socket.

5. Set the STF jumpers as follows.

a. P3040 to P3050 pin 3 (change to +5 va)

b. P3050 . . . not used

c. P4040 . . . INT

d. P5045 . . . 0

e. P5050 . . . MIN

f. P5060 . . . present

6. Set the 7D02 as follows.

a. Clear all previous word recognizers by turning the mainframe power off, then on again.

b. Press the WD RECOGNIZER key.

c. Using the CURSOR control keys, move the cursor to the ADDRESS box and enter 0FFFF.

d. Press the TRIGGER and END keys.

Test 1. Setup and Hold

1. Procedure For Checking Setup Times

a. Set the PG 508 to DELAY MODE, duration variable (approximately 400 ns).

b. The falling edge of the ALE signal is prior to machine state T2. Data is latched with the falling edge of CLK in machine state T4.

c. Adjust the PG 508 delay for 30 ns prior to the falling edge of CLK in machine state T4 (TTL level).

d. Press the START key.

e. Press 0 for an absolute listing.

f. Press the DATA SCROLLING up arrow (↑) to observe location 14 and location 15.

g. The data at location 14 (prior to the trigger) is FFFF for the PM 106 (or FF for the PM 107).

NOTE

Refer to ERROR 24, in the Maintenance and Troubleshooting section, for troubleshooting aid.

2. Procedure for Checking Hold Times

a. Set the PG 508 to UNDLY MODE, duration variable for the falling edge of the output waveform coincident with the falling edge of CLK in machine state T4 (TTL level).

b. Press the START key.

c. The data at location 15 is FFFF for the PM 106 (or FF for the PM 107).

NOTE

Refer to ERROR 24, in the Maintenance and Troubleshooting section, for troubleshooting aid.

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MAINTENANCE AND TROUBLESHOOTING

MAINTENANCE

Repair

The PM 106/107 requires no periodic maintenance. Properly handled and cared for, your personality module will give dependable service for many years. However, should repair service be needed at any time, Tektronix, Inc. provides complete instrument repair at local Field Service Centers and at the Factory Service Center. Contact your local Tektronix Field Office or representative for further information.

Obtaining Replacement Parts

Most electrical and mechanical parts can be ordered through your local Tektronix Field Office or representative. Many of the standard electronic components may also be available from a local commercial source in your area. However, before you purchase or order a part from a source other than Tektronix, Inc., please check the Replaceable Electrical Parts List and the Replaceable Mechanical Parts List, for the proper value, rating, tolerance, and description.

Ordering Parts

When ordering replacement parts from Tektronix, Inc., it is important that all of the following information be included to ensure receiving the proper parts.

1. Instrument type (include modification or option numbers).

2. Instrument serial number.

3. A description of the part (if electrical, include component number from the Replaceable Electrical Parts Lists.)

4. The Tektronix part number.

5. The quantity of each part desired.

Cleaning Instructions

This instrument should be cleaned as often as the operating environment requires. Accumulation of dirt on components acts as an insulating blanket and prevents efficient heat dissipation. This condition can cause overheating and component breakdown within the instrument.

Exterior. Loose dust on the personality module pod can be brushed off. Dirt that remains can be removed with a soft cloth dampened with a mild detergent and water solution. Abrasive cleaners should not be used.

CAUTION

Use only enough water to dampen the cloth or swab. Prevent water from getting inside the pod. Do not get the microprocessor plug or the logic analyzer plug wet. Do not use chemical agents as they may damage the plastic. In particular, avoid chemicals that contain benzene, toluene, xylene, acetone, or other organic solvents.

Interior. Use a jet of dry, low pressure air and a soft brush to remove dust from the interior of the pod and circuit boards. After soldering or when otherwise required, use isopropyl alcohol with a soft cloth or cotton swab to remove flux, resin, or dirt. As the board is cleaned, make certain that square pins are not contaminated with residual flux to ensure good electrical contact.

Personality Module Disassembly

Access to test points and other interior features can only be gained by disassembling the module case. If it becomes necessary to do so, find a clean open space on a table or bench top and be sure that screws and other small parts are placed where they will not be lost.

CAUTION

Always turn off the mainframe power before connecting or disconnecting any personality module. Static precautions should be observed at all times when disassembly or repair of the personality module is performed.

The procedure for disassembly is described below.

1. To remove the top cover, unscrew the four middle screws on the bottom of the personality module.

2. Lift the top cover off. The top board, A1, is now accessible.

3. To access the bottom board, A3, remove the two end screws and nuts on the twisted pair woven cable end.

4. Remove the two end screws and nuts on the opposite end of the pod and remove all 3 boards as a unit. The bottom board is now accessible.

5. To troubleshoot the middle board, A2, carefully remove the bottom board, A3, which is attached only by square pins and their receptacles on board A2.

6. To reassemble the instrument, reverse the above procedure.

Logic Analyzer Plug Disassembly

When it becomes necessary to disassemble the logic analyzer plug, use the following procedure.

1. Remove the four screws holding the plug together with a 3/32"Allen wrench.

2. Pull the halves of the connector apart and remove the cable hold-down clamp.

3. Remove the circuit board by lifting up on the connector end and sliding the board out of the plastic hold-down flanges.

4. Reverse the above procedure for reassembly of the logic analyzer plug.

Microprocessor Replacement Plug Disassembly

The pins on the microprocessor plug are delicate and may become bent or broken. If this occurs, the pins can be replaced as a unit. The procedure for disassembly is described below. Refer to Figure 6-1.

1. Remove the two Phillips head screws holding the protective face on the plug.

2. Lift off the protective face and remove the pin assembly from the plug.

3. Install the new pin assembly, matching pin one to pin one of the plug assembly.

4. In fitting the protective face over the pins, be sure that all of the pins and their respective holes are properly aligned and that none of the pins are bent over.

5. When all parts have been properly fitted back together, reinsert the two screws.

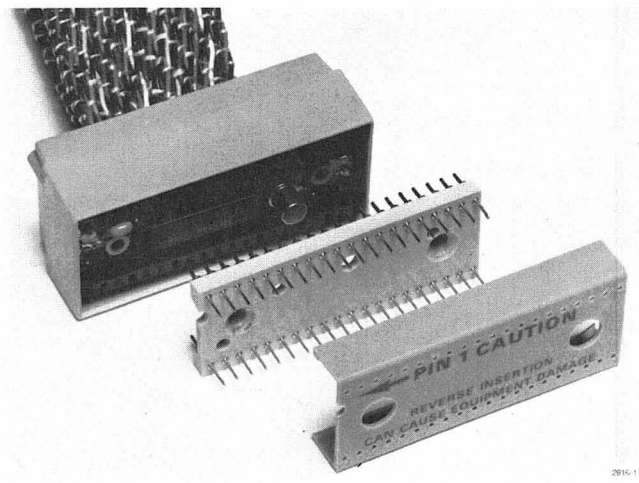

Figure 6-1. Microprocessor plug disassembly.

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TROUBLESHOOTING

Overview

When trouble occurs in the PM 106/107, several methods are available to the service technician for localizing and identifying the faulty circuit. Always repeat that section of the check that deals with any repaired line to verify repair work.

Diagnostic Monitor. Power-up Diagnostic routines are built in and automatically run each time the 7D02 Logic Analyzer-PM 106/107 Personality Module system is powered on. If a failure is detected, the POWER-UP VERIFICATION test results display this failure. The display offers the operator the choice between beginning operation or displaying the DIAGNOSTIC MONITOR MENU. Depressing any keyboard button within approximately 2 seconds of the power-up and holding the button for approximately 5 seconds will simulate a keyboard failure and allow the operator to access the DIAGNOSTIC MONITOR. The menu offers the choice of running any or all of the module tests or of exiting the diagnostic monitor. Refer to the Diagnostic Monitor, Part 1 in the Performance Check section for failures.

Functional Checks. Testing of individual signal lines is provided by the Functional Checks, Part II, in the Performance Check section.

Performance Checks. Testing of specific parameters in the Performance Requirements column of the Specification section is provided through use of listed test equipment, the 7D02 word recognizers, and test programs. Refer to the Performance Check, Part III, in the Performance Check section.

Troubleshooting Error List and Procedures

When troubleshooting detects a failure, reference notes will direct the service technician to a specific error number listing. This list may in turn direct the technician to a specific procedure to isolate the problem.

Substitution Method

If other logic analyzers or personality modules are available, try substituting them and running the diagnostics again.

CAUTION

Exercise caution when you suspect power supply problems, since a supply that is seriously out of tolerance could cause secondary damage in more than one unit.

Service Test Fixture

The service test fixture (STF) generates address, data, and control signal patterns used to test the PM 106/107 Personaltiy Module. Two testing positions, $\overline{\text{SELF}}$ and $\overline{\text{PROG}}$, are provided. The $\overline{\text{SELF}}$ position enables a short maximum mode program for the 7D02 diagnostics. The $\overline{\text{PROG}}$ position enables a longer program (for both minimum and maximum modes) used to test the minimum mode emulation circuitry.

A 32 X 8 bit PROM provides an 8-address-repetitive program to test the queue level tracking circuitry. It also tests status line from which ALE, DT/$\overline{\text{R}}$, M/$\overline{\text{IO}}$, IO/$\overline{\text{M}}$, $\overline{\text{DEN}}$ and queue fill operations are decoded; lines NMI and BHE; and address-data line AD0.

In the $\overline{\text{SELF}}$ position, the upper four addresses (A19-A16) are the same as (or are the complement of) the second-highest four addresses (A15-A12). The addresses are stepped as follows.

00XXX, 11XXX, 22XXX...FFXXX;
and F0XXX, E1XXX...FFXXX;
and F0XXX, E1XXX...0FXXX.

Signal line A0 is controlled by the PROM. The displayed data is the complement of the corresponding address bits except for D0. In the $\overline{\text{SELF}}$ position, a short RESET signal around address 00000 is applied to the personality module.

In the $\overline{\text{PROG}}$ position, the STF steps through all address combinations from address 00000 to FFFFF for address lines A19 through A1. Address line A0 is generated by the PROM and does not allow access of all possible addresses. Lines HOLD and HLDA (minimum mode), $\overline{\text{RQ}}$/$\overline{\text{GT0}}$ and $\overline{\text{RQ}}$/$\overline{\text{GT1}}$ (maximum mode), READY, RESET, and INTR are tested beginning at address 80000 in the $\overline{\text{PROG}}$ position. Depending upon the clock frequency, the personality module changes between minimum and maximum modes around address 00000. For this mode change, the STF stops the output of the test program (except for the clock) for approximately 50 ms. During this time, the RESET signal is applied to the personality module.

Table 6-1 lists the jumper plugs and test points available on the STF.

Table 6-1

STF JUMPER PLUGS AND TEST POINTS

Jumper Plug/ Test Point #	Description
P3040	CHG (eliminates mode change delay)
TP3041	Unlabeled (A0 test point)
P3050	+5 — +5 va (for +5 volt loop test)
P4040	INT-EXT (clock input control)
P4050	SELF-PROG ($\overline{\text{SELF}}$ or $\overline{\text{PROG}}$ selection)
P5040	SS (START-STOP for signature analysis)
TP5040	HALT (to prevent address, data, or control change upon 7D02 $\overline{\text{HALT}}$)
P5045	0-1 (selects between $\overline{\text{RQ}}/\overline{\text{GT0}}$ and $\overline{\text{RQ}}/\overline{\text{GT1}}$)
P5050	MIN-MAX (for $\overline{\text{PROG}}$ position, selects minimum, maximum or alternating modes)
P5051	SELF (timing pins for the timing option probe)
P5052	PROG (timing pins for the timing option probe)
P5060	Unlabeled (enables line A0)

Timing Option

The service test fixture (STF) provides stimuli for the Timing Option Probe, P6451. This stimulii is the reference for the TIMING OPTION test (test B) on the Diagnostic Monitor menu. Subtests 1 and 2 are internal to the 7D02 and run even without the timing option probe connected. Connection of the timing option probe is described in the preliminary setup of the Performance Check section.

Diagnostic Module 9 PER. MOD. -SYSTEM

Diagnostic Module 9 contains 7 subtests. The PM 106/107 supports only subtests 1, 2, 3, 4, and 7. Subtests 3, 4, and 7 require that the service test fixture be connected. Refer to the preliminary setup in the Performance Check section.

Subtest 1. This test reads a byte at address 3:E010 in the personality module EPROM to determine the EPROM length. This tells the location of the EPROM trailer, YY. The value at YYFC is compared with the value in the next byte, YYFD, which should be its complement. If the two bytes are not complementary, a failure message is printed as follows.

```
1    FAIL   3FFFD-X
1    FAIL   3YYFD-X   ; INCORRECT VALUE @
                        3:E010
```

where YY is the value read from E010.

X is the first non-complementary bit after the two bytes are compared on a bit-by-bit basis.

If the part number is correct, the following message is printed.

```
1    PASS   0801-XX   ; PM 106
1    PASS   1081-XX   ; PM 107
```

Subtest 2. This test calculates a 16 bit checksum on the EPROM. If the checksum does not match the expected value of 1E57, the calculated value is reported as the following failure.

```
2    FAIL    XXXX
```

where XXXX = the calculated value.

The following figures (6-2, 6-3, 6-4, and 6-5) represent the Word Recognizer setups used in the following diagnostic modules and an approximation of subtest 4.

Subtest 3. The personality module microprocessor plug must be connected to the service test fixture for this and the following subtests. The following program is assigned to the State Machine.

```
IF WRI = TRUE
THEN TRIGGER TIMING AND MAIN
```

The 7D02 Acquisition Memory board is set for zero delay. The 7D02 front end qualifiers and the clock shifter/divider are programmed to default values (falling clock edge, C9-C4=X, Delay-by-2, ESYNC: C8=1, WAIT: C9=0) according to data stored in the personality module EPROM. After all setups are complete, a DISPLAY command is sent and the 7D02 slow clock detector is checked. A slow clock indication will result in the following failure.

```
3    FAIL    0FF60-1   ; SLOW, OR NO CLOCK
```


@

```
            PM 106
  DIAGNOSTIC WORD RECOGNIZERS
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=96F6
1 ADDRESS=66908
1 [CODE FETCH]=1 BHE [/QDUMP]= 1
1 R/W [LST-F]= 1 M/IO [2LS-F]= 1
1 MIN/MAX MODE=0 HOLD ACK=     0
1 QLEVEL=4 IRQ=0 EXT TRIG IN=  X
1 TIMING WR=X
1THEN DO
1
1 COUNTER # 1 0-EVENTS
1     1-RESET
1 COUNTER # 2 0-EVENTS
1     1-RESET
1 GOTO 2
1
 END TEST 1
 TEST 2
2IF
2 WORD RECOGNIZER # 2
2 DATA=B00B
2 ADDRESS=44FF4
2 [CODE FETCH]=1 BHE [/QDUMP]= 1
2 R/W [LST-F]= 1 M/IO [2LS-F]= 0
2 MIN/MAX MODE=0 HOLD ACK=     0
2 QLEVEL=3 IRQ=0 EXT TRIG IN=  X
2 TIMING WR=X
2THEN DO
2 GOTO 3
2ELSE DO
2 COUNTER # 1 0-EVENTS
2     0-INCREMENT

END TEST 2
```

```
 TEST 3
3IF
3 WORD RECOGNIZER # 3
3 DATA=FFFE
3 ADDRESS=F0000
3 [CODE FETCH]=0 BHE [/QDUMP]= 1
3 R/W [LST-F]= 1 M/IO [2LS-F]= 0
3 MIN/MAX MODE=0 HOLD ACK=     0
3 QLEVEL=0 IRQ=0 EXT TRIG IN=  X
3 TIMING WR=X
3THEN DO
3 GOTO 4
3ELSE DO
3 COUNTER # 2 0-EVENTS
3     0-INCREMENT
3       0 INCREMENT
3       1 RESET
 END TEST 3
 TEST 4
4IF
4 WORD RECOGNIZER # 4
4 DATA=0000
4 ADDRESS=0FFFF
4 [CODE FETCH]=0 BHE [/QDUMP]= 1
4 R/W [LST-F]= 1 M/IO [2LS-F]= 1
4 MIN/MAX MODE=0 HOLD ACK=     0
4 QLEVEL=2 IRQ=1 EXT TRIG IN=  X
4 TIMING WR=X
4THEN DO
4
4 TRIGGER 0-MAIN
4     0-BEFORE DATA
4     0-SYSTEM UNDER TEST CONT.
4     0-STANDARD CLOCK QUAL.
4 TRIGGER 1-TIMING
4             0 MAIN
4             1 TIMING
4     0-BEFORE DATA
4     THRESHOLD V.  = 0-PLUS 1.40
4     0-SYNC. TRIGGER IMMEDIATE
4
4ELSE DO
4 QUALIFY
END TEST 4
```

3473-28

Figure 6-2. PM 106 diagnostic word recognizers.

PM 106 DIAGNOSTIC MEMORY DISPLAY

CTR1=62325 EVT TRIG LOC = 015
CTR2=22533 EVT TRIG IN TEST 4

LOC	ADDRESS	DATA	STATUS	Q	I
T	0FFFD	0002	2LS-F H	4	0
016	00000	FFFE	IO R W	0	0
017	00002	FFFD	QDUMP W	2	1
018	00004	FFFB	LST-F W	3	0
019	00006	FFF8	MEMW L	2	1
020	00008	FFF6	L&2LF W	4	0
021	0000A	FFF4	IO W W	4	0
022	0000D	FFF2	2LS-F H	4	0
023	0000F	FFF0	MEMR H	2	1
024	00010	FFEE	IO R W	0	0
025	00012	FFED	QDUMP W	2	1
026	00014	FFEB	LST-F W	3	0
027	00016	FFE8	MEMW L	2	1
028	00018	FFE6	L&2LF W	4	0
029	0001A	FFE4	IO W W	4	0
030	0001D	FFE2	2LS-F H	4	0
031	0001F	FFE0	MEMR H	2	1
032	00020	FFDE	IO R W	0	0
033	00022	FFDD	QDUMP W	2	1

3473-29

Figure 6-3. PM 106 diagnostic memory display.

This can be caused by an erratic or missing clock from the personality module. Anything that generates or transfers the test clock to the 7D02 should be checked. Check STF power and jumper positions.

If the clock appears to be running, the personality module EPROM is read to determine how long to wait for a trigger to occur. Then, a STORE command is sent. After waiting the specified length of time (512 ms), the activity monitor on the Acquisition Memory board is examined to see if the Main Section has triggered and returned to DISPLAY mode. If the Main Section is still in STORE mode, the following failure is generated.

3 FAIL 2E803-7 ; MAIN SECTION FAILED TO TRIGGER

Failure to trigger can be caused by failure of the personality module to generate the Word Recognizer 1 (WR1) value. Check STF jumper positions.

Subtest 4. This test involves all four 7D02 Word Recognizers, the two 7D02 Counters, the 7D02 State Machine and the 7D02 Acquisition Memory.

The 7D02 Word Recognizers are programmed the same as for subtest 3. The 7D02 State Machine is also programmed with the following program.

IF WR1 THEN GO TO 2, AND RESET CTR 1 AND 2
IF WR2 THEN GO TO 3
ELSE INC. CTR 1
IF WR3 THEN GO TO 4
ELSE INC. CTR 2
IF WR4 THEN TRIGGER MAIN AND DON'T QUALIFY
ELSE QUALIFY

The 7D02 front end qualifiers are programmed to default values. After all steps are complete, a DISPLAY command is sent and the slow clock detector is checked. A slow clock indication results in the following failure.

4 FAIL 0FF60-1 ; SLOW, OR NO CLOCK

This can be caused by an erratic or missing clock from the personality module. Anything in the personality module that generates or transfers the test clock should be checked. Check the STF power and jumper positions.

If the clock appears to be running, the personality module EPROM is read to determine how long to wait for a trigger. Then, a STORE command is sent. After waiting 512 ms, the Activity Monitor on the 7D02 Acquisition Memory board is examined to see if the Main Section has triggered and returned to DISPLAY mode. If still in the STORE mode, the following failure is generated.

4 FAIL 2E803-7 ; MAIN SECTION FAILED TO TRIGGER

Failure to trigger can be caused by failure of the personality module to generate any one of the four 7D02 Word Recognizer values. Check STF power and jumper positions.

Next, all bytes in the 7D02 Acquisition Memory between 2:E000 and 2:E3FF are summed and the result of the checksum is compared with the expected data stored in the personality module EPROM.

Failure of the comparison results in the following failure message.

4 FAIL 3E035-X ; MAIN ACQ. MEM. FAILS CHECKSUM

@

```
            PM 107
   DIAGNOSTIC WORD RECOGNIZERS
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=DD
1 ADDRESS=2DD22
1 [CODE FETCH]=1 [/QDUMP]=      0
1 R/W [LST-F]= 0 M/IO [2LS-F]= 0
1 MIN/MAX MODE=0 HOLD ACK=      0
1 QLEVEL=1 IRQ=1 EXT TRIG. IN=  X
1 TIMING WR=X
1THEN DO
1
1 COUNTER # 1 0-EVENTS
1     1-RESET
1 COUNTER # 2 0-EVENTS
1     1-RESET
1 GOTO 2
1
 END TEST 1
 TEST 2
2IF
2 WORD RECOGNIZER # 2
2 DATA=0B
2 ADDRESS=44FF4
2 [CODE FETCH]=1 [/QDUMP]=      1
2 R/W [LST-F]= 1 M/IO [2LS-F]= 0
2 MIN/MAX MODE=0 HOLD ACK=      0
2 QLEVEL=1 IRQ=0 EXT TRIG IN=   X
2 TIMING WR=X
2THEN DO
2 GOTO 3
2ELSE DO
2 COUNTER # 1 0-EVENTS
2     0-INCREMENT
END TEST 2
```

```
 TEST 3
3IF
3 WORD RECOGNIZER # 3
3 DATA=FE
3 ADDRESS=F0000
3 [CODE FETCH]=0 [/QDUMP]=      0
3 R/W [LST-F]= 1 M/IO [2LS-F]= 0
3 MIN/MAX MODE=0 HOLD ACK=      0
3 QLEVEL=0 IRQ=0 EXT TRIG IN=   X
3 TIMING WR=X
3THEN DO
3 GOTO 4
3ELSE DO
3 COUNTER # 2 0-EVENTS
3     0-INCREMENT
 END TEST 3
 TEST 4
4IF
4 WORD RECOGNIZER # 4
4 DATA=00
4 ADDRESS=0FFFF
4 [CODE FETCH]= 0 [/QDUMP]=     0
4 R/W [LST-F]= 1 M/IO [2LS-F]= 1
4 MIN/MAX MODE=0 HOLD ACK=      0
4 QLEVEL=7 IRQ=1 EXT TRIG IN=   X
4 TIMING WR=X
4THEN DO
4
4 TRIGGER 0-MAIN
4     0-BEFORE DATA
4     0-SYSTEM UNDER TEST CONT.
4     0-STANDARD CLOCK QUAL.
4 TRIGGER 1-TIMING
4     0 BEFORE DATA
4     1 CENTERED
4     2 AFTER DATA
4     3 DELAYED
4     THRESHOLD V. = 0-PLUS 1.40
4     0-SYNC, TRIGGER IMMEDIATE
4
4ELSE DO
4 QUALIFY
END TEST 4
```

3473-30

Figure 6-4. PM 107 diagnostic word recognizers.

PM 107 DIAGNOSTIC MEMORY DISPLAY

CTR1=14696 EVT TRIG LOC = 015
CTR2=22533 EVT TRIG IN TEST 4

LOC	ADDRESS	DATA	STATUS	Q	I
T	0FFFD	02	2LS-F	1	0
016	00000	FE	IO R	0	0
017	00002	FD	GDUMP	1	1
018	00004	FB	LST-F	1	0
019	00006	F8	MEMW	0	1
020	00008	F6	L&2LF	1	0
021	0000A	F4	IO W	1	0
022	0000D	F2	2LS-F	1	0
023	0000F	F0	MEMR	7	1
024	00010	EE	IO R	0	0
025	00012	ED	GDUMP	1	1
026	00014	EB	LST-F	1	0
027	00016	E8	MEMW	0	1
028	00018	E6	L&2LF	1	0
029	0001A	E4	IO W	1	0
030	0001D	E2	2LS-F	1	0
031	0001F	E0	MEMR	7	1
032	00020	DE	IO R	0	0
033	00022	DD	GDUMP	1	1

3473-31

Figure 6-5. PM 107 diagnostic memory display.

Failure of the checksum to match is either an intermittent channel, or the fetch predictor circuitry operating erratically. Also, the upper address lines (A23-A16) and upper data lines (D15-D8) are checked by checksumming the Expansion Option Memory at address 2:E400 to 2:E7FF. The resulting sum is compared against a value in the EPROM.

Failure of the comparison results in the following failure message.

```
4    FAIL    3E036-X   ; EXP. OPT. ACQ. MEM.
                         FAILS CHECKSUM
```

Subtest 7. This test checks the clock qualifier lines C9-C4 on the 7D02 Front End board.

The 7D02 State Machine is programmed with the following test sequence.

```
1   IF WR1 THEN TRIGGER MAIN
1           ELSE GO TO 1
```

C9-C4 are given the following values, respectively.

011111

Word Recognizer 1 was programmed in an earlier subtest to a value specified by the personality module EPROM. This test uses each of the control lines in turn to qualify out the value to which Word Recognizer 1 has been programmed.

If the control line works correctly, the State Clock that occurs with Word Recognizer 1 will be inhibited and the State Machine will not see the Word Recognizer output. A PASS condition, then, is indicated by the failure of the Main Section to trigger. The processor waits 512 ms to trigger.

Six bytes in the personality module EPROM specify the value to be sent to the 7D02 Front End to inhibit State Clocks when Word Recognizer 1 occurs for each of the six control lines. The following sequence is repeated six times, once for each control line or until a failure occurs.

- Read value from personality module EPROM
- Write value to Front End latch
- Send STORE command
- Wait specified length of time
- Check Activity Monitor on Acquisition Memory board
- If in DISPLAY mode, print FAIL and stop

If subtests 3 and 4 pass, it is safe to assume that this test is operating correctly.

The test results are interpreted as follows.

```
7    FAIL    3E039    ; C4 DIDN'T INHIBIT
                         TRIGGER
7    FAIL    3E03A    ; C5 DIDN'T INHIBIT
                         TRIGGER
7    FAIL    3E03B    ; C6 DIDN'T INHIBIT
                         TRIGGER
7    FAIL    3E03C    ; C7 DIDN'T INHIBIT
                         TRIGGER
7    FAIL    3E03D    ; C8 DIDN'T INHIBIT
                         TRIGGER
7    FAIL    3E03E    ; C9 DIDN'T INHIBIT
                         TRIGGER
```


@

Diagnostic Module B
TIMING OPTION

This module consists of 3 subtests. The only subtest supported by the PM 106/107 is subtest 3.

This test requires stimulus from the service test fixture, via the P6451, and is not run during the POWER-UP VERIFICATION.

The timing option word recognizer is set to trigger on the occurrence of 3FH.

Subtest 3. The 7D02 State Machine is programmed similar to the following.

```
1 IF TIMING OPTION WR = 3F WR1 = TIMING WR
1 AND WR2, 3, 4, = DON'T CARE
1 THEN
1 GO TO 4

4 IF TIMING OPT WR = 3F WR1 = TIMING WR
4 WR 2, 3, 4, = DON'T CARE
4 THEN TRIGGER
4 TIMING
4 AND
4 MAIN
```

The timing option memory address counter is set to 0. All word recognizers except the timing option are set to x (don't care).

The slow clock indicator is checked for the presence of a clock. If none is detected, the following failure is printed.

```
3    FAIL    0FF60-1    ; SLOW, OR NO CLOCK
                           DETECTED
```

Check STF power and jumper positions.

If the clock appears to be running, a byte is read from the personality module EPROM that specifies how long to wait for a trigger. Then a STORE command is sent. After waiting the specified time (2 ms) the 7D02 Acquisition Memory Activity Monitor is examined to see if the Main Section has triggered. If it hasn't, the following failure is reported.

```
3    FAIL    2E803-7    ; MAIN SECTION FAILED TO
                           TRIGGER
```

This can be caused by the service test fixture not generating the 3FH value or the P6451 not transferring data properly.

If the trigger occurred, the timing option memory address counter is examined to determine the last data location and the trigger location is calculated. The value saved in the trigger location is then compared with the value in the personality module EPROM that was used to program the timing option word recognizer. If the two are not complementary (data inverted), the following failure is reported.

```
3    FAIL    3E03F-X    ; TRIGGER VALUE
                           INCORRECT
```

This can be caused by a bad timing relationship between the clock and data.

If the trigger test passes, the timing option acquisition memory at address 2:F000-2:F0FF is checksummed (with the exception of one data byte which is Xs), and the result compared with the expected value stored in the personality module EPROM. If the values are not the same, the following failure is reported.

```
3    FAIL    3E040-X    ; CHECKSUM ERROR
                           2:F000-2:F0FF
```

where X indicates the bit that didn't match.

This can be caused by the service test fixture not generating the correct pattern all the time or an intermittent failure in the P6451. Check STF power and jumper positions.

TROUBLESHOOTING ERROR LIST

The following error list pertains to errors found when performing the Functional Checks, Part II and the Performance Checks, Part III.

This error list assumes the 7D02 and STF are known to be good, the STF and personality module are properly connected, and all power supplys are within specified tolerances. Referenced procedure routines follow the troubleshooting error list.

TROUBLESHOOTING ERROR LIST

ERROR No.	SYMPTOM	POSSIBLE CAUSES
1.	*Message displayed:* PERSONALITY MODULE REQUIRED POWER DOWN BEFORE ATTACHING!	1. 7D02 failing to read AA in the first byte of address 0 in personality module EPROM. 2. Bad ribbon cable. 3. Bad EPROM, A1U2020. 4. Bad EPROM driver, A1U2040. 5. Stuck address, data, $\overline{\text{SELP}}$ or LOOK line.
2.	*Message displayed:* NO CLOCK (in inverse video while program is running.)	1. Bad A1U4070 or associated transistors. 2. Service test fixture incorrectly jumpered.
3.	*Message displayed:* SLOW CLOCK (in inverse video). Note: Blinking SLOW CLOCK message is normal condition with the service test fixture in $\overline{\text{PROG}}$ (Program) position	1. System under test clock slow. 2. No T1 (ESYNC) signal. 3. Service test fixture incorrectly jumpered. 4. Refer to following Procedure A.
4.	7D02 will not trigger in the minimum mode. (STF in the $\overline{\text{PROG}}$ position)	1. Service test fixture P4050 is not jumpered correctly. 2. STF P5050 not jumpered to centered position. 3. Check the Minimum/$\overline{\text{Maximum}}$ Mode Decoder, minimum mode FETs and switching transistors. 4. See following Procedure A.
5.	Timing display problem (minimum mode)	1. Timing Option Probe P6451 not properly connected. 2. STF not jumpered correctly. 3. Clock not programmed to delay by zero. 4. See screen timing lines 0–7 and check respective circuitry. 5. Check all screen timing lines (except 0 and 1) at address 90000. If the 7D02 triggers, the personality module is not responding to the reset pulse around address 00000. 6. See ERRORS 6–12 in ascending order.
6.	ALE line problems (timing diagram line 6)	1. Check signal lines $\overline{\text{S0}}$, $\overline{\text{S1}}$, and $\overline{\text{S2}}$. 2. See following Procedure C.
7.	DT/$\overline{\text{R}}$ line problems (timing diagram line 4)	Check A1U3020, A1Q5040, and A1Q5022.

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TROUBLESHOOTING ERROR LIST (cont)

ERROR No.	SYMPTOM	POSSIBLE CAUSES
8.	M/$\overline{IO}$ line problems (timing diagram line 3)	Check A1U3020, A1Q5012, A1Q5020, and A1P6010.
9.	$\overline{DEN}$ line problems (timing diagram line 5)	1. Check board A3 for proper T1, T3, T4 and $\overline{T4CLK}$ signals. 2. See following Procedure D.
10.	$\overline{WR}$ line problems (timing diagram line 2)	Check A2U5020B and A2U3520A.
11.	$\overline{INTA}$ line problems (timing diagram line 7)	Check A1U3010, A2U1020, A3U1020, A1Q7010, A1Q7012 and switching transistors.
12.	HOLD or HLDA line problems (timing diagram lines 0 and 1 respectively)	1. Check the maximum mode timing diagram for correct signals. 2. If OK, check A1Q's 4018, 4020, 4012, 4014, A2U's 4010, 3530, 1030, $\overline{RESET3}$, straps on board A2.
13.	7D02 will not trigger in the maximum mode and give an absolute listing. (STF in the $\overline{PROG}$ position)	1. Service test fixture P4050 is not jumpered correctly. 2. STF P5050 not jumpered to centered position. 3. Check Minimum/$\overline{Maximum}$ Mode Decoder, maximum mode FETs and switching transistors. 4. Check A2U3530B.
14.	Timing display problem (maximum mode)	1. Timing Option Probe P6451 not properly connected. 2. STF not jumpered correctly. 3. See ERRORS 15–18 in ascending order.
15.	$\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ timing problems	Check A1Q's 5020, 5022, 5024, 5012, 5014, 5016 and associated switching transistors.
16.	$\overline{RQ}$/$\overline{GT0}$, $\overline{RQ}$/$\overline{GT1}$ problems (timing diagram lines 0 and 1 respectively)	Check A1Q's 4012, 4014, 4018, A2U's 3010, 5010, 6010, jumper straps on board A2.
17.	QS0 and QS1 line problems (timing diagram lines 6 & 7)	Check A1Q's 6012, 7012, 6010, and 7010.
18.	$\overline{LOCK}$ line problems (timing diagram line 2)	Check A1Q5018 and A1Q5010.
19.	Incorrect STATUS indication	1. Check $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ timing diagram. 2. See following Procedure E.
20.	Incorrect queue level	1. Check A2U2030. 2. See following Procedure E.
21.	IRQ line problem	Check A3U1020, A2U1010, or A1U3035.

TROUBLESHOOTING ERROR LIST (cont)

ERROR No.	SYMPTOM	POSSIBLE CAUSES
22.	READY line problem	Check A1Q3035 and A2U3010.
23.	$\overline{\text{HALT}}$ line problems	Personality module not strapped for $\overline{\text{HALT}}$ function. See Maintenance and Troubleshooting section.
24.	Setup and Hold problem	Check respective Input Protection Hybrids, A1U3050, A1U3040, or the 68 Ω termination resistors.
25.	System under test problem in minimum mode	1. Check the RESET and READY lines. 2. Check minimum mode timing diagram.
26.	System under test problem in maximum mode	1. Check the RESET and READY lines. 2. Check maximum mode timing diagram.
27.	System under test problem when switching between minimum and maximum modes	Ensure 50 ms minimum setup time for mode switching.
28.	Incorrect mnemonic mode disassembly can be caused by many things. Eliminate possible causes by completing the performance checks. If all OK except mnemonics, check possible causes column.	Bad EPROMS or buffer. Check A1U's 2020, 2030, and 2040.

@

PROCEDURE A

1. Position the following STF jumpers:

   a. P4050 to pins 2 and 3.

   b. P5050 to the center two pins.

2. Turn the mainframe power off, then on again to delete any previous programs.

3. Press the ELSE, TRIGGER, and END keys in sequence.

4. Using the CURSOR control keys, move the cursor to the BEFORE DATA box and enter a 3 for ZERO DELAY.

5. Move the cursor to the STANDARD CLOCK QUAL. box and enter a 1 for USER CLOCK QUAL.

6. Move the cursor to the STANDARD CLK. SYNTHESIS box and enter a 1 for USER CLOCK SYNTHESIS.

7. Move the cursor right to the 2 box and enter a 0.

8. Press the START key.

9. Did the 7D02 trigger?

   - If no, proceed to Procedure B.

   - If yes, proceed to step 10.

10. Press the IMMEDIATE, DISPLAY, and PROGRAM keys in sequence.

11. Move the cursor to the end of any existing program and hold the DELETE key until the entire program has been deleted.

12. Press the WD RECOGNIZER key.

13. Move the cursor to the MIN/MAX MODE box and enter a 1 for minimum mode.

14. Press the [ ] key.

15. Press the TRIGGER key twice.

16. Press the 1 key for a TIMING diagram.

17. Press the [ ], END, and START keys in sequence.

18. Did the 7D02 trigger?

   - If no, proceed to step 19.

   - If yes, proceed to step 20.

19. Note that a secondary error now exists. No trigger was received in the maximum mode before, and now no trigger was received in the minimum mode. Possible problem with the MIN/$\overline{\text{MAX}}$ line. Proceed to step 20.

20. Check the ALE signal at J3010-30 with the test oscilloscope.

NOTE

Blinking display and width variation is due to STF mode changing. ALE must conform to TTL levels in both modes.

21. Is ALE present and correct?

   - If no, proceed to step 22.

   - If yes, check:

     a. Ribbon cable.

     b. A2U1030A or A2U1010H.

     c. Bad A1Q6010 or switcher transistor.

22. Press the IMMEDIATE, DISPLAY, and PROGRAM keys in sequence.

23. Move the cursor to the ADDRESS box and enter 80000.

24. Move the cursor to the MIN/MAX MODE box and enter a 0 for the maximum mode.

25. Press the START key.

26. Are the signals $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ present and correct?

- If yes, check A2U's 1020B, 2020A, 2030C, and 1010.
- If no, proceed to step 27 Secondary problem exists with the MIN/$\overline{MAX}$ line or the STF is improperly jumpered.

27. Check FETs and associated circuitry for the $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ signal lines.

PROCEDURE B

1. Press the IMMEDIATE, DISPLAY, and PROGRAM keys in sequence.

2. Using the CURSOR control keys, move the cursor to the C9 box and enter an X for a don't care.

3. Press the START key.

4. Did the 7D02 trigger?

- If no, check:
  a. Clock missing - See Error No. 2.
  b. Bad ribbon cable.
  c. Check +5 volts on STF P3050 pin 1.
- If yes, check the READY line.

PROCEDURE C

1. Are $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ OK?

- If no, check respective line, A1U3030, A2U's 1020B, 5030B, 2020A, 1010B, and 2030C.
- If yes, proceed to step 2.

2. If:

a. MEM/$\overline{IO}$ line problem, proceed to step 4.

b. Queue information problem, proceed to step 5.

c. Missing or erroneous STATUS code problem, proceed to step 6.

3. Check A1U3010, A3U1010-2, 3, 4, 5, and 6 or A3U1020.

4. Check A1U3010, A3U1010-1, 8, 9, 10, 11, 12, and 13, A3U1020, 1030, and 5020.

5. Check:

a. QDUMP: A3U5020, A3U1030, A2U3520B, A2U6020.

b. QFILL: Not seen when using STF.

c. LST-F: A3U5020, 1030, 1010, 3010, 1020.

d. 2LS-F: A3U1030, A3U1010.

e. MEM/$\overline{IO}$: A3U1010, A3U1020, A1U3020.

f. R/$\overline{W}$: A3U1010, A3U1020, A1U3020.

6. Does the queue level clear?

- If no, check $\overline{S0B}$, $\overline{S1B}$, $\overline{S2B}$, T1, A1U3030, A3U5030 and A3U5010.
- If yes, proceed to step 3.

@

7. Check A3U5030, A3U5010, A3U3030, and A3U4030.

NOTE

When queue is cleared, XA1, XA2, and XA3 = 0.

Queue level is incremented by 2 on STF address ending in 2, 4, or 8 (PM 106 only).

Queue level is incremented by 1 on STF address ending in D (PM 106 only) and addresses ending in 2, 4, 8, and D (PM 107 only).

Queue level is cleared on STF address ending in 0.

Queue level is decremented by 1 on STF address ending in 4, 6, and D.

Queue level is decremented by 2 on STF address ending in F.

8. Are the queue level increments correct?

- If no, proceed to step 4.
- If yes, proceed to step 5.

9. Check A3U's 5030, 7030, and 2030. Check that XA1 increments queue by one and XA2 increments queue by two.

10. Check:

a. that XA1=0 on decrement, XA2+XA3=1 on decrement.

b. A3U4030 and A3U3030

PROCEDURE D

1. Are T1, T2, T3, T4, and $\overline{\text{T4CLK}}$ correct?

- If yes, perform the Personality Module Disassembly procedure to remove the bottom board. Check: A2U's 2010B, 5030A, and 6020A.

NOTE

It may be necessary to inject a signal from A2U5020-9 into the $\overline{T4CLK}$ line. With signal injection, the DENW1 signal will be one half cycle shorter on the rising edge.

- If no, is only $\overline{\text{T4CLK}}$ bad?
- If no, perform the Personality Module Disassembly procedure to remove the bottom board. Check A2U;s 1030, 2010, 6030, and 5020.

Table 6-2

PERSONALITY MODULE TEST POINTS

Board #	Test Pin #	Label on Board	Common Name
A1	1010	GND	GROUND
A1	1070	CLK	TTL $\overline{\text{CLOCK}}$
A1	1075	CLK	TTL CLOCK
A1	2020	GND	GROUND
A1	3060	GND	GROUND
A1	5060	H	$\overline{\text{HALT}}$
A1	6010	GND	GROUND
A2	7010	HLD1	HLDA1

TROUBLESHOOTING WITH SIGNATURE ANALYSIS PROCEDURE

1. Jumper the STF according to Table 5-2 in the Performance Check section.

2. Turn the Data Analyzer on.

3. Press the SIGNATURE (labeled c) key.

4. Press the down arrow (labeled 6) key three times.

5. Press the REPEAT (labeled 3) key.

6. Connect the P6451 probe plug to the data analyzer at the input marked P6451 INPUT ONLY.

7. Connect the P6451 probe wires as follows.

   a. GND wire to STF P5051 or P5052 GND.

   b. C (clock) wire to STF P5051 or P5052 C.

   c. 0 (start) and 1 (stop) wires to STF P5040 SS pins.

8. Connect the data input probe to the data analyzer at the SERIAL SIGNATURE DATA INPUT.

9. Connect the data input probe ground to the personality module ground.

10. Turn the oscilloscope mainframe power off, then on again.

11. Press the WD RECOGNIZER.

12. Using the CURSOR control keys, move the cursor to the EXT TRIG IN box and enter a 1.

13. Press the TRIGGER and END keys in sequence.

14. Press the START key. The 7D02 should show the blinking RUNNING message and should not trigger.

15. Use the data input probe to obtain the signature values shown in the following Table 6-3.

The following Figures 6-6 and 6-7 are component locators for boards A2 and A3 respectively.

NOTE

The signatures for the middle board (A2) should be taken with the bottom board (A3) off and board A2 to board A3 interconnects open. To remove the bottom board, refer to the Personality Module Disassembly instructions at the beginning of this section.

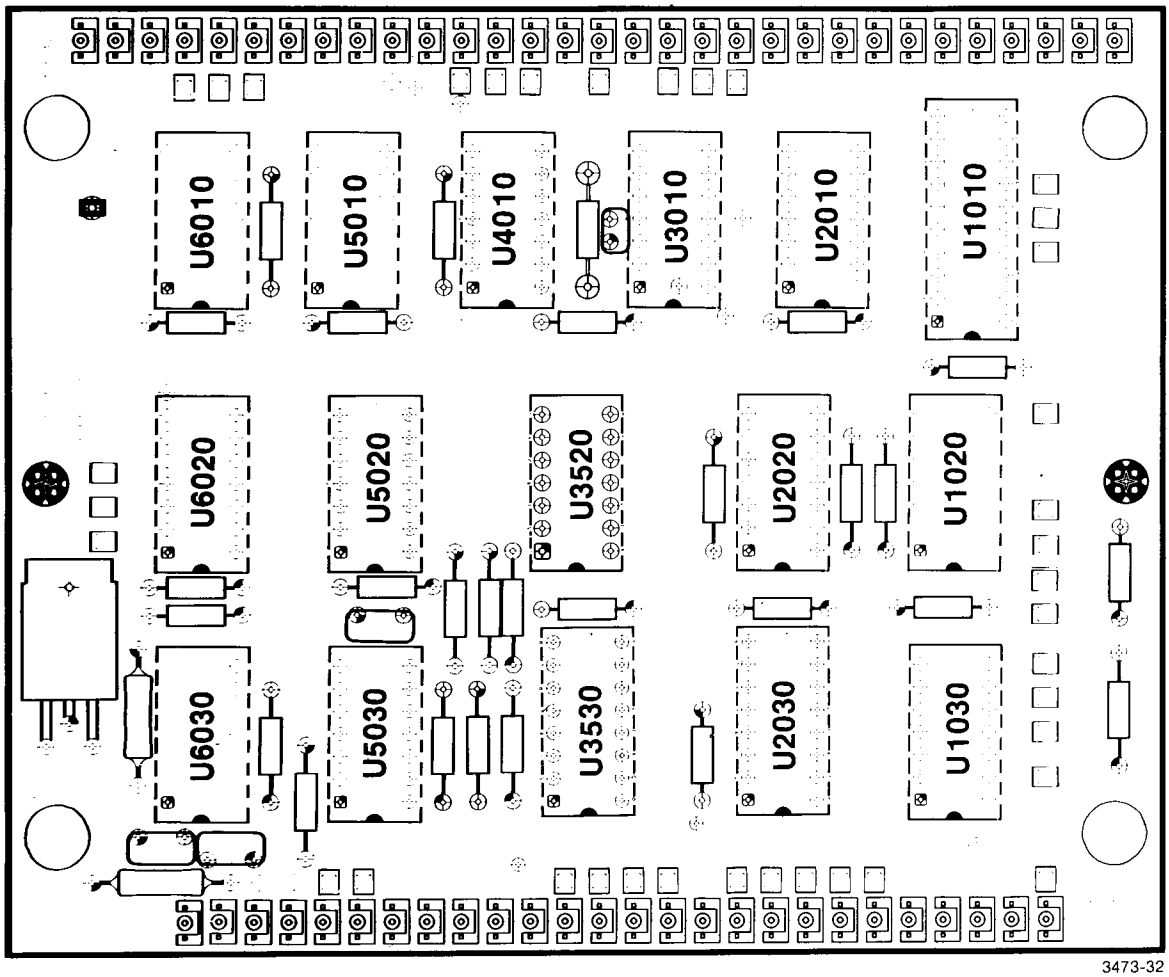


Figure 6-6. Board A2 Reverse side.

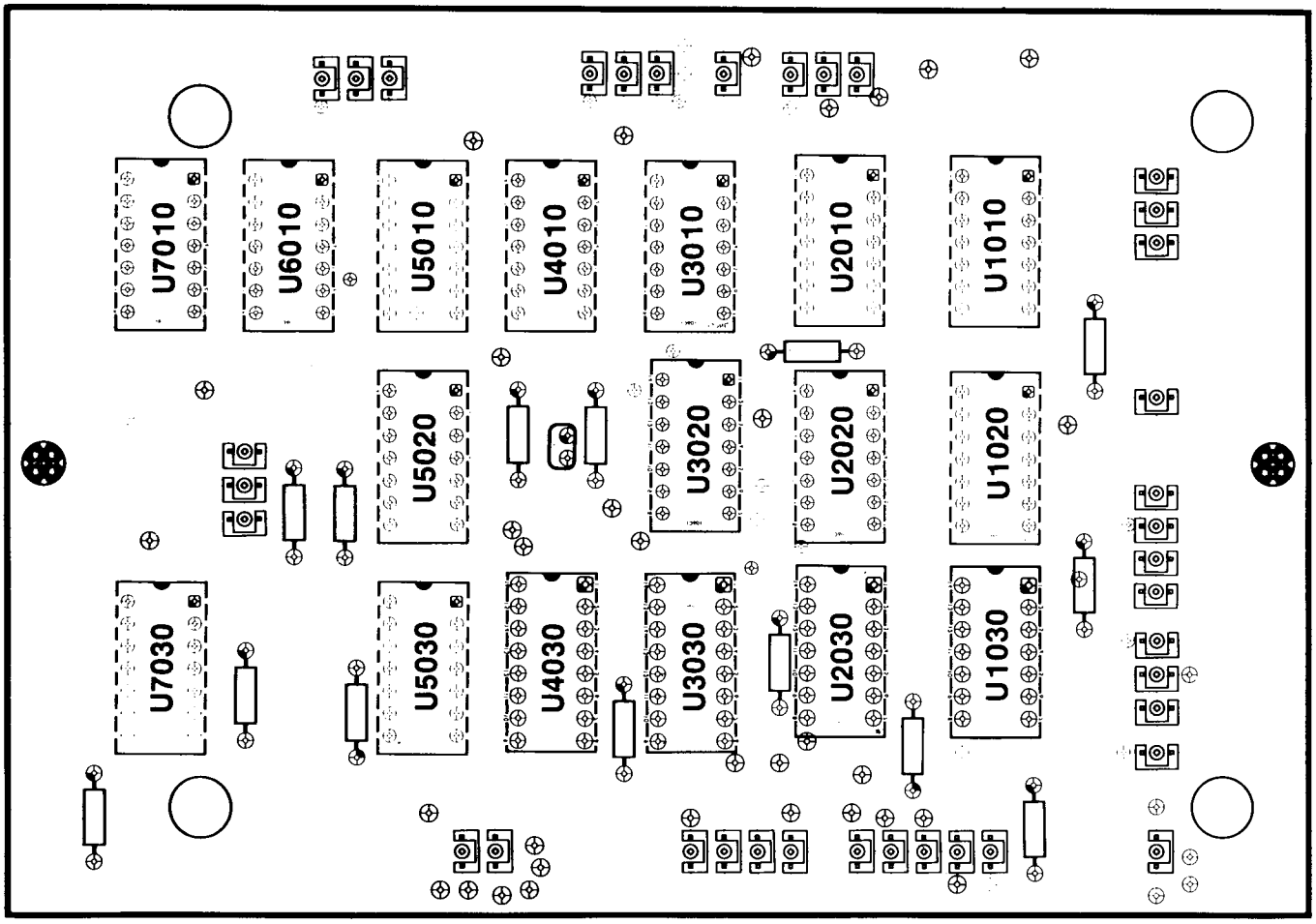


Figure 6-7. Board A3 Reverse side.

Table 6-3

Signature Analysis Values

NOTE

Signature values not listed in the PM 107 column are assumed to be the same as the PM 106.

0000 = 0 volts

A70F = 5 volts

* = pins not exercised with board A3 off or in $\overline{\text{SELF}}$ mode

--- = indeterminate

Location	Signature	
J3010	**PM 106**	**PM 107**
1	0000	
2	A70F	
3	0000	
4	703A	
5	---	
6	U844	
7	0000	
8	---	
9	---	
10	---	
11	4027	
12	H4H0	
13	F8CA	
14	C598	
15	A70F	
16	---	
17	A70F	
18	A70F	
19	56P4	
20	A580	
21	A70F	
22	0000	
23	---	
24	0000	
25	88CH	
26	5631	
27	U13H	
28	---	
29	AAA8	
30	H736	
31	397P	

Table 6-3 (cont)

Location	Signature	
J3070	**PM 106**	**PM 107**
1	0000	
2	A70F	
3	9251	4F65
4	53U0	H100
5	8FC3	3238
6	A38U	
7	44F3	
8	---	---
9	---	
10	415C	A70F
11	A70F	
12	53FH	
13	0000	
14	36AC	
15	08AA	
16	0000	
17	0000	
18	0000	
19	0000	
20	A70F	
21	0000	
22	A70F	
23	---	
24	0000	
25	A70F	
26	PH57	A70F
J1010 (A3)	**PM 106**	**PM 107**
1	0PPU	
2	7373	
3	---	
4	---	
5	---	
6	---	
7	---	
8	73HF	
9	---	
10	8455	
11	98H1	
12	---	
13	---	
14	---	
15	355H	PC69
16	U4UF	760F
17	2CC0	9534
18	H736	

Table 6-3 (cont)

Location	Signature	
J6020 (A3)	**PM 106**	**PM 107**
1	AP6F	
2	C5FH	
3	---	
Top Board (A1)		
A1U2020	**PM 106**	**PM 107**
1	1F13	
2	A1A8	
3	0L75	
4	6822	
5	CCF9	
6	U8H5	
7	3H28	
8	F0U1	
9	---	
10	---	
11	---	
12	---	
13	---	
14	---	
15	---	
16	---	
17	---	
18	A580	
19	P419	
20	A70F	
21	H953	
22	F06P	
23	220H	
24	A70F	

Table 6-3 (cont)

Location	Signature	
A1U2030	**PM 106**	**PM 107**
1	1F13	
2	A1A8	
3	0C75	
4	6822	
5	CCF9	
6	U8H5	
7	3H28	
8	F0U1	
9	---	
10	---	
11	---	
12	---	
13	---	
14	---	
15	---	
16	---	
17	---	
18	028F	
19	P419	
20	A70F	
21	H953	
22	F06P	
23	220H	
24	A70F	
A1U2040	**PM 106**	**PM 107**
1	A70F	
2	---	
3	0U65	
4	---	
5	7412	
6	---	
7	21A9	
8	---	
9	P707	
10	0000	
11	40H0	
12	---	
13	F6P9	
14	---	
15	4H12	
16	---	
17	53FH	
18	---	
19	A70F	
20	A70F	

Table 6-3 (cont)

Location	Signature	
A1U2050	**PM 106**	**PM 107**
1	0000	
2	H953	
3	85P4	
4	UU71	
5	P419	
6	F06P	
7	C79P	
8	7358	
9	220H	
10	0000	
11	H736	
12	A580	
13	7F42	
14	0AH5	
15	9PFC	
16	9APF	
17	---	
18	CFAH	
19	F5U7	
20	A70F	
A1U2060	**PM 106**	**PM 107**
1	0000	
2	3H28	
3	4H12	
4	F6P9	
5	U8H5	
6	6822	
7	P707	
8	40H0	
9	CCF9	
10	0000	
11	H736	
12	F0U1	
13	53FH	
14	21A9	
15	0C75	
16	A1A8	
17	7412	
18	0U65	
19	1F13	
20	A70F	

Table 6-3 (cont)

Location	Signature	
A1U3010	**PM 106**	**PM 107**
1	A2AU	
2	F8CA	
3	U13H	
4	0000	
5	0000	
6	A70F	
7	A70F	
8	0000	
9	---	
10	05A3	
11	19F9	
12	A70F	
13	82P1	
14	A70F	
15	H4H0	
16	A70F	
A1U3020	**PM 106**	**PM 107**
1	0000	
2	814H	
3	029C	
4	CFAH	
5	HP56	
6	856A	
7	0AH5	
8	7F42	
9	CP21	
10	0000	
11	H736	
12	A2AU	
13	A38U	
14	44F3	
15	F8CA	
16	PH57	A70F
17	415C	A70F
18	C598	
19	U13H	
20	A70F	

Table 6-3 (cont)

Location	Signature	
A1U3030	**PM 106**	**PM 107**
1	0000	
2	A70F	
3	A38U	
4	A70F	
5	08AA	
6	C598	
7	56P4	
8	44F3	
9	53FH	
10	0000	
11	53FH	
12	44F3	
13	56P4	
14	C598	
15	08AA	
16	A70F	
17	A38U	
18	A70F	
19	0000	
20	A70F	
A1U3035	**PM 106**	**PM 107**
1	0000	
2	7F42	
3	415C	A70F
4	0AH5	
5	A70F	
6	CFAH	
7	0000	
8	029C	
9	36AC	
10	0000	
11	36AC	
12	029C	
13	0000	
14	CFAH	
15	A70F	
16	0AH5	
17	415C	A70F
18	7F42	
19	0000	
20	A70F	

Table 6-3 (cont)

Location	Signature	
A1U3040	**PM 106**	**PM 107**
1	0000	
2	7F42	
3	7358	
4	0AH5	
5	C79P	
6	029C	
7	UU71	
8	CFAH	
9	85P4	
10	0000	
11	85P4	
12	CFAH	
13	UU71	
14	029C	
15	C79P	
16	OAH5	
17	7358	
18	7F42	
19	0000	
20	A70F	
A1U3050	**PM 106**	**PM 107**
1	0000	
2	21A9	
3	4H12	
4	7412	
5	F6P9	
6	0U65	
7	40H0	
8	53FH	
9	P707	
10	0000	
11	P707	
12	53FH	
13	40H0	
14	0U65	
15	F6P9	
16	7412	
17	4H12	
18	21A9	
19	0000	
20	A70F	

Table 6-3 (cont)

Location	Signature	
Middle Board (A2)		
A2U1010	**PM 106**	**PM 107**
1	0000*	
2	0000	
3	A70F*	
4	---*	
5	0000*	
6	---*	
7	703A	
8	19F9	
9	A70F*	
10	0000	
11	---*	
12	---	
13	703A	
14	703A	
15	---*	
16	A70F*	
17	A70F	
18	0000*	
19	0000	
20	A70F	
A2U1020	**PM 106**	**PM 107**
1	A70F*	
2	A70F*	
3	C598	
4	44F3	
5	A38U	
6	CFAH	
7	0000	
8	AP6F	
9	---*	
10	A70F*	
11	0960	
12	0000*	
13	A70F*	
14	A70F	

Table 6-3 (cont)

Location	Signature	
A2U1030	**PM 106**	**PM 107**
1	CFAH	
2	H736	
3	---	
4	703A	
5	H736	
6	703A	
7	0000	
8	---*	
9	A70F	
10	A70F	
11	703A*	
12	A70F	
13	A70F*	
14	A70F	
A2U2010	**PM 106**	**PM 107**
1	---	
2	A70F*	
3	6C9C	
4	A70F	
5	C5FH	
6	12F1	
7	0000	
8	A70F*	
9	0000	
10	A70F*	
11	0000	
12	H736	
13	---	
14	A70F	
A2U2020	**PM 106**	**PM 107**
1	A70F	
2	A70F	
3	---	
4	A70F	
5	44F3	
6	A38U	
7	0000	
8	H736	
9	6C9C	
10	A70F	
11	A70F	
12	0000	
13	A70F	
14	A70F	

Table 6-3 (cont)

Location	Signature	
A2U2030	**PM 106**	**PM 107**
1	0000	
2	0000*	
3	A70F*	
4	F8CA	
5	6UC6	
6	H736	
7	703A	
8	0000	
9	0000*	
10	0000*	
11	0000*	
12	0000*	
13	0000*	
14	0000*	
15	0000	
16	A70F	
A2U3010	**PM 106**	**PM 107**
1	0000*	
2	12F1	
3	A70F*	
4	H204*	
5	0000	
6	---*	
7	0000	
8	A70F*	
9	---	
10	0000*	
11	A70F*	
12	---	
13	0000*	
14	A70F	
A2U3520	**PM 106**	**PM 107**
1	0960	
2	F8CA	
3	6C9C	
4	A70F	
5	2UC1	
6	88CH	
7	0000	
8	0000*	
9	A70F	
10	A70F	
11	0000*	
12	A70F	
13	---*	
14	A70F	

Table 6-3 (cont)

Location	Signature	
A2U3530	**PM 106**	**PM 107**
1	---*	
2	A70F*	
3	0000*	
4	A70F*	
5	0000*	
6	A70F*	
7	0000*	
8	0000*	
9	---*	
10	0000*	
11	A70F*	
12	0000*	
13	0000*	
14	A70F*	
15	0000*	
16	A70F*	
A2U4010	**PM 106**	**PM 107**
1	A70F*	
2	0000*	
3	A70F*	
4	A70F*	
5	A70F*	
6	0000*	
7	0000*	
8	A70F*	
9	A70F*	
10	0000*	
11	A70F*	
12	---*	
13	0000*	
14	A70F*	
A2U5010	**PM 106**	**PM 107**
1	0000*	
2	0000*	
3	A70F*	
4	---*	
5	A70F*	
6	0000*	
7	0000*	
8	0000*	
9	A70F*	
10	---*	
11	A70F*	
12	A70F*	
13	0000*	
14	A70F*	

Table 6-3 (cont)

Location	Signature	
A2U5020	**PM 106**	**PM 107**
1	A70F	
2	H736	
3	---	
4	A70F	
5	6C9C	
6	FF97	
7	0000	
8	AP6F	
9	0960	
10	A70F	
11	---	
12	12F1	
13	A70F	
14	A70F	
A2U5030	**PM 106**	**PM 107**
1	0960	
2	A70F*	
3	---	
4	A70F	
5	HP56	
6	795A	
7	0000	
8	FF97	
9	6C9C	
10	A70F	
11	---	
12	CFAH	
13	CFAH	
14	A70F	
A2U6010	**PM 106**	**PM 107**
1	0000*	
2	0000*	
3	A70F*	
4	---*	
5	A70F*	
6	0000*	
7	0000*	
8	0000*	
9	A70F*	
10	---*	
11	A70F*	
12	A70F*	
13	0000*	
14	A70F*	

Table 6-3 (cont)

Location	Signature	
A2U6020	**PM 106**	**PM 107**
1	HP56	
2	PH57 A70F	
3	19F9	
4	0000* A70F*	
5	0000*	
6	---*	
7	0000	
8	9P51	
9	A70F	
10	F8CA	
11	A70F*	
12	A70F	
13	6UC6	
14	A70F	
A2U6030	**PM 106**	**PM 107**
1	A70F*	
2	A70F*	
3	0000*	
4	A38U	
5	44F3	
6	CFAH	
7	0000	
8	12F1	
9	A70F*	
10	C5FH	
11	A70F	
12	0000	
13	A70F	
14	A70F	
A2U7030	**PM 106**	**PM 107**
1	0000	
2	0000	
3	0000	

Table 6-3 (cont)

Location	Signature	
Bottom Board (A3)		
A3U1010	**PM 106**	**PM 107**
1	A70F	
2	5631	
3	19F9	
4	3UHH	
5	CPF5	
6	7373	
7	0000	
8	P9H1	
9	HH02	
10	---	
11	A70F	
12	19F9	
13	F8CA	
14	A70F	
A3U1020	**PM 106**	**PM 107**
1	19F9	
2	---	
3	U13H	
4	5631	
5	H4H0	
6	73HF	
7	0000	
8	A70F	
9	0000	
10	8455	
11	2359	
12	028F	
13	A580	
14	A70F	
A3U1030	**PM 106**	**PM 107**
1	A70F	
2	7A0P	
3	8455	
4	A70F	
5	98H1	
6	3UHH	
7	0000	
8	HH02	
9	7A0P	
10	A70F	
11	8455	
12	3C7C	
13	A70F	
14	A70F	

Table 6-3 (cont)

Location	Signature	
A3U2010	**PM 106**	**PM 107**
1	A70F	
2	A9P3	
3	0PPU	
4	---	
5	H736	
6	A70F	
7	0000	
8	---	
9	---	
10	---	
11	A70F	
12	---	
13	AP6F	
14	A70F	
A3U2020	**PM 106**	**PM 107**
1	---	
2	A70F	
3	36AC	
4	2327	
5	0PPU	
6	A9P3	
7	0000	
8	2327	
9	842C	
10	A70F	
11	36AC	
12	A70F	
13	---	
14	A70F	
A3U2030	**PM 106**	**PM 107**
1	A70F	
2	A70F	
3	0000	
4	A70F	
5	A70F	
6	0000	
7	0000	
8	1H0C	
9	H736	
10	0483	
11	0000	
12	P3FU	
13	C598	
14	A70F	

Table 6-3 (cont)

Location	Signature	
A3U3010	**PM 106**	**PM 107**
1	08AA	
2	1H0C	
3	C18P	
4	C18P	
5	A70F	
6	1682	
7	0000	
8	2359	
9	8455	
10	---	
11	U1P8	
12	56P4	
13	56P4	
14	A70F	
A3U3020	**PM 106**	**PM 107**
1	---	
2	---	
3	---	
4	---	
5	A70F	
6	0000	
7	0000	
8	---	
9	---	
10	A70F	
11	C5FH	
12	A70F	
13	---	
14	A70F	
A3U3030	**PM 106**	**PM 107**
1	---	
2	C350	
3	145F	
4	A70F	
5	5C5A	
6	U4UF	760F
7	53U0	H100
8	0000	
9	---	
10	BFC3	3238
11	2CCU	9534
12	A378	A5HH
13	CH9A	
14	355H	PC69
15	9251	4F65
16	A70F	

Table 6-3 (cont)

Location	Signature	
A3U4010	**PM 106**	**PM 107**
1	CA07	
2	AUA6	
3	A70F	
4	A70F	
5	U4F1	
6	U1P8	
7	0000	
8	UU99	A70F
9	0000	
10	0000	
11	P657	0000
12	A70F	
13	0000	
14	A70F	
A3U4030	**PM 106**	**PM 107**
1	P50U	
2	9251	4F65
3	4P17	1682
4	5C5A	
5	P292	A42U
6	53U0	H100
7	1682	
8	0000	
9	A70F	
10	1682	8167
11	A70F	
12	A70F	
13	1966	A5HH
14	1682	
15	8FC3	3238
16	A70F	
A3U5010	**PM 106**	**PM 107**
1	C18P	
2	UU99	A70F
3	A70F	0323
4	5CC6	
5	C924	A70F
6	P292	A42U
7	0000	
8	A70F	
9	AUA6	
10	56P4	
11	---	
12	4P17	1682
13	A70F	
14	A70F	

Table 6-3 (cont)

Location	Signature	
A3U5020	**PM 106**	**PM 107**
1	A70F	
2	76U7	
3	---	
4	A70F	
5	3C7C	
6	9F77	
7	0000	
8	2359	
9	8455	
10	A70F	
11	---	
12	08AA	
13	A70F	
14	A70F	
A3U5030	**PM 106**	**PM 107**
1	56P4	
2	U1P8	
3	415C	A70F
4	P657	0000
5	53FH	
6	U4F1	
7	0000	
8	0483	
9	A38U	
10	P3FU	
11	44F3	
12	AUA6	
13	08AA	
14	A70F	
A3U6010	**PM 106**	**PM 107**
1	CA07	
2	A70F	
3	A70F	
4	53FH	
5	A70F	
6	A70F	
7	0000	
8	5CC6	
9	0000	
10	0000	
11	U1P8	
12	AUA6	
13	0000	
14	A70F	

Table 6-3 (cont)

Location	Signature	
A3U7010	**PM 106**	**PM 107**
1	U1P8	
2	CA07	
3	---	
4	AUA6	
5	415C	A70F
6	A70F	0323
7	0000	
8	C924	A70F
9	P657 0000	
10	U4F1	
11	---	
12	08AA	
13	CA07	
14	A70F	
A3U7030	**PM 106**	**PM 107**
1	U1P8	
2	08AA	
3	---	
4	A70F	
5	A70F	
6	76U7	
7	0000	
8	CA07	
9	P3FU	
10	0483	
11	---	
12	C598	
13	H736	
14	A70F	

TROUBLESHOOTING WITH BOARD 3 REMOVED

Preliminary Setup

1. Turn off the power to the personality module at the oscilloscope mainframe.

2. Remove the power supply module plug from the service test fixture (STF).

3. Using the Personality Module Disassembly instructions remove the bottom board.

4. Solder a jumper wire from A2U5020-8 to the $\overline{\text{T4CLK}}$ pin at P7030 to troubleshoot the $\overline{\text{DEN}}$ circuit and associated circuitry.

NOTE

To perform this check, a single wire having one end stripped and one end with a square pin socket is required.

5. Turn on the power to the personality module at the oscilloscope mainframe.

6. The POWER-UP VERIFICATION will display the error message PER.MOD.-SYSTEM.

7. Press the START key. The RUNNING and SLOW CLOCK messages will be displayed in the upper inverse video.

8. Press the START key again. The NO DATA ACQUIRED message will be displayed in the upper inverse video area.

9. Enter a 0 for the absolute listing.

10. Reconnect the power plug from the power supply module to the STF.

11. Proceed with board A2 troubleshooting.

Disabled Circuits

When troubleshooting with board A3 removed, the following circuits are disabled and do not operate normally.

1. A2U1020C: Schematic 4.

2. $\overline{\text{DEN}}$ circuit: Schematic 4 (complete with jumper from previous preliminary setup step 4).

3. Control Line Generator B: Schematic 5.

4. A2U1010: Schematic 5.

5. A2U2030: Schematic 5.

If one of the disabled circuits is suspected of being faulty, an alternate method of troubleshooting using conventional methods should be used.

CAUTION

To avoid static damage to components on board A2 with board A3 removed, all troubleshooting should be performed in a static-free environment.

ADDITIONAL INFORMATION

Delay Through ECL CLOCK

The specified delay through the ECL CLOCK for the PM 106/107 is 10 ns minimum to 16.5 ns maximum. To perform the following check, refer to the Logic Analyzer Plug Disassembly procedure in this section.

1. Connect the channel 1 test oscilloscope probe to the input clock signal, CLK, on J7020 pin 37.

2. Connect the channel 2 test oscilloscope probe to the ECL CLOCK signal at the logic analyzer plug, pin 2.

3. Measure the delay time between the rising edge of channel 1 and the rising edge of channel 2.

4. Check that the measured delay time is within the specified range to confirm correct operation.

@

ECL CLOCK Mismatch

A small amount of timing mismatch (1 to 2 ns) between the ECL clock signals CLOCK and $\overline{\text{CLOCK}}$ is normal. Any amount exceeding this is cause to suspect existing or future problems and warrants further investigation.

1. Connect the channel 1 test oscilloscope probe to the ECL $\overline{\text{CLOCK}}$ (labeled CLK) test point TP1070 on the per sonality module.

2. Connect the channel 2 test oscilloscope probe to the ECL CLOCK (labeled CLK) test point TP1075 on the personality module.

3. Adjust the test oscilloscope for a vertical deflection approximately four divisions high and a horizontal repetition rate of 5 ns/div. Trigger on channel 1.

4. Invert channel 2 input and check delay from

   a. Rising edge of CH1 to CH2

   b. Falling edge of CH1 to CH2.

Strapping Procedures

NOTE

If jumper straps are relocated within the personality module, be sure to tag the instrument externally with the current configuration. This will signal service personnel that the instrument has been changed from its original condition.

Changing HOLD (and $\overline{\text{HALT}}$ if implemented) from $\overline{\text{RQ}}/\overline{\text{GT0}}$ to $\overline{\text{RQ}}/\overline{\text{GT1}}$

Personality Module change:

1. P7031, move jumper strap from C and 0 to C and 1.

2. P7032, move jumper strap from HLDA0 and HLDA to HLDA1 and HLDA.

3. P7040, move jumper strap from T0 and TC to TC and T1.

Service test fixture change:

1. P5045, move jumper from 0 to 1.

$\overline{\text{HALT}}$ Line Strapping Procedure

Connect jumper strap across A2P1040 on the personality module (board A2).

CAUTION

It should be noted that the following precautions should be observed when implementing the $\overline{\text{HALT}}$ function.

1. If both $\overline{\text{RQ}}/\overline{\text{GT0}}$ and $\overline{\text{RQ}}/\overline{\text{GT1}}$ lines are used by the SUT, implementation of the $\overline{\text{HALT}}$ line may cause bus contention (more than one controller talking at once) in some situations.

2. If the $\overline{\text{RQ}}/\overline{\text{GT0}}$ line is used by the SUT, the $\overline{\text{HALT}}$ line may be used in conjunction with the $\overline{\text{RQ}}/\overline{\text{GT1}}$ line.

3. If the $\overline{\text{RQ}}/\overline{\text{GT1}}$ line is used by the SUT, the HALT line may be used in conjunction with the $\overline{\text{RQ}}/\overline{\text{GT0}}$ line.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

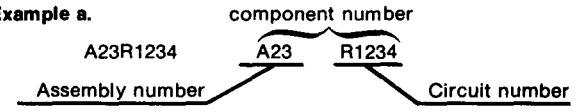
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

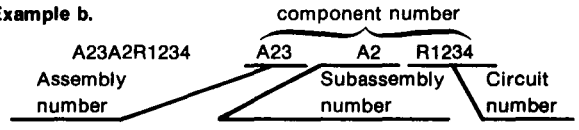
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867, 19TH AVE. SOUTH	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
24546	CORNING GLASS WORKS, ELECTRONIC COMPONENTS DIVISION	550 HIGH STREET	BRADFORD, PA 16701
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
52648	PLESSEY SEMICONDUCTORS	1641 KAISER	IRVINE, CA 92714
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A01	670-6710-00	B010100	B010124	CKT BOARD ASSY:TOP	80009	670-6710-00
	----- -----			(PM106 ONLY)		
A01	670-6710-01	B010125	B010224	CKT BOARD ASSY:TOP	80009	670-6710-01
	----- -----			(PM106 ONLY)		
A01	670-6710-02	B010225		CKT BOARD ASSY:TOP	80009	670-6710-02
	----- -----			(PM106 ONLY)		
A01	670-7206-00	B010100	B010109	CKT BOARD ASSY:TOP	80009	670-7206-00
	----- -----			(PM107 ONLY)		
A01	670-7206-01	B010110	B010129	CKT BOARD ASSY:TOP	80009	670-7206-01
	----- -----			(PM107 ONLY)		
A01	670-7206-02	B010130		CKT BOARD ASSY:TOP	80009	670-7206-02
	----- -----			(PM107 ONLY)		
A02	670-6838-00	B010100	B010124	CKT BOARD ASSY:MIDDLE	80009	670-6838-00
	----- -----			(PM106 ONLY)		
A02	670-6838-01	B010125	B010224	CKT BOARD ASSY:MIDDLE	80009	670-6838-01
	----- -----			(PM106 ONLY)		
A02	670-6838-02	B010225		CKT BOARD ASSY:MIDDLE	80009	670-6838-02
	----- -----			(PM106 ONLY)		
A02	670-6838-00	B010100	B010109	CKT BOARD ASSY:MIDDLE	80009	670-6838-00
	----- -----			(PM107 ONLY)		
A02	670-6838-01	B010110	B010129	CKT BOARD ASSY:MIDDLE	80009	670-6838-01
	----- -----			(PM107 ONLY)		
A02	670-6838-02	B010130		CKT BOARD ASSY:MIDDLE	80009	670-6838-02
	----- -----			(PM107 ONLY)		
A03	670-6711-00	B010100	B010224	CKT BOARD ASSY:BOTTOM	80009	670-6711-00
	----- -----			(PM106 ONLY)		
A03	670-6711-01	B010225		CKT BOARD ASSY:BOTTOM	80009	670-6711-01
	----- -----			(PM106 ONLY)		
A03	670-6711-00	B010100	B010129	CKT BOARD ASSY:BOTTOM	80009	670-6711-00
	----- -----			(PM107 ONLY)		
A03	670-6711-01	B010130		CKT BOARD ASSY:BOTTOM	80009	670-6711-01
	----- -----			(PM107 ONLY)		
A04	670-6149-00			CKT BOARD ASSY:PROBE CONNECTOR	80009	670-6149-00
	----- -----			(NO ELECTRICAL PARTS)		
A05	----- -----			CKT BOARD ASSY:PROBE		
	----- -----			(NOT REPL ORDER 175-3030-00. NO ELEC PARTS)		
A01	----- -----			CKT BOARD ASSY:TOP		
A01C1070	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A01C2030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C2050	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3015	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3050	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C5070	283-0339-00			CAP.,FXD,CER DI:0.22UF.10%,50V	72982	8131N075W5R224K
A01C5072	283-0159-00			CAP.,FXD,CER DI:18PF,5%,50V	72982	8111B065C0G0180J
A01C5074	283-0175-00			CAP.,FXD,CER DI:10PF,5%,200V	72982	8101B210C0G0100J
A01C6010	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A01C6050	281-0810-00			CAP.,FXD,CER DI:5.6PF,0.5%,100V	04222	GC10-1A5R6D
A01C7010	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	273C5
A01C7020	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	273C5
A01C7070	283-0100-00	B010100	B010163	CAP.,FXD,CER DI:0.0047UF,10%,200V	56289	273C3
	----- -----			(PM106 ONLY)		

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A01C7070	283-0144-00	B010164		CAP.,FXD,CER DI:33PF,1%,500V (PM106 ONLY)	72982	801-547P2G330G
A01C7070	283-0100-00	B010100	B010123	CAP.,FXD,CER DI:0.0047UF,10%,200V (PM107 ONLY)	56289	273C3
A01C7070	283-0144-00	B010124		CAP.,FXD,CER DI:33PF,1%,500V (PM107 ONLY)	72982	801-547P2G330G
A01CR5070	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A01Q2070	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A01Q2074	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A01Q3060	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A01Q3062	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A01Q3065	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A01Q3069	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A01Q3070	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A01Q3074	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A01Q4012	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q4014	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q4018	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q4020	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q5010	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q5012	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q5014	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q5016	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q5018	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q5020	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q5022	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q5024	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q6010	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q6012	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q6060	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A01Q6065	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A01Q6068	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A01Q6070	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A01Q7010	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q7012	151-1098-00			TRANSISTOR:SILICON,FE,N-CHANNEL	80009	151-1098-00
A01Q7068	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A01Q7070	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A01R1030	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R1036	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R1039	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R1040	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R1046	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R1060	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R1070	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R1075	301-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.50W	01121	EB5115
A01R1076	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R2010	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R2013	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R3072	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A01R3074	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A01R4031	317-0511-00	XB010125		RES.,FXD,CMPSN:510 OHM,5%,0.125W (PM106 ONLY)	01121	BB5115
A01R4031	317-0511-00	XB010110		RES.,FXD,CMPSN:510 OHM,5%,0.125W (PM107 ONLY)	01121	BB5115
A01R4060	315-0152-00	B010100	B010224	RES.,FXD,CMPSN:1.5K OHM,5%,0.25W (PM106 ONLY)	01121	CB1525
A01R4060	315-0821-00	B010225		RES.,FXD,CMPSN:820 OHM,5%,0.25W (PM106 ONLY)	01121	GB8215

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A01R4060	315-0152-00	B010100	B010129	RES.,FXD,CMPSN:1.5K OHM,5%,0.25W (PM107 ONLY)	01121	CB1525
A01R4060	315-0821-00	B010130		RES.,FXD,CMPSN:820 OHM,5%,0.25W (PM107 ONLY)	01121	CB8215
A01R4070	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A01R4072	321-0208-00			RES.,FXD,FILM:1.43K OHM,1%,0.125W	91637	MFF1816G14300F
A01R4074	321-0631-00			RES.,FXD,FILM:12.5K OHM,1%,0.125W	91637	MFF1816G12501F
A01R5070	321-0281-00			RES.,FXD,FILM:8.25K OHM,1%,0.125W	91637	MFF1816G82500F
A01R5072	321-0286-00			RES.,FXD,FILM:9.31K OHM,1%,0.125W	91637	MFF1816G93100F
A01R6012	317-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.125W	01121	BB1035
A01R6020	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A01R6064	321-0344-00			RES.,FXD,FILM:37.4K OHM,1%,0.125W	91637	MFF1816G37401F
A01R7066	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A01R7068	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A01R7069	315-0363-00			RES.,FXD,CMPSN:36K OHM,5%,0.25W	01121	CB3635
A01U2020	160-0801-00	B010100	B010124	MICROCIRCUIT,DI:4096 X 8 EPROM (PM106 ONLY)	80009	160-0801-00
A01U2020	160-0801-01	B010125		MICROCIRCUIT,DI:4096 X 8 EPROM,PRGM (PM106 ONLY)	80009	160-0801-01
A01U2020	160-1081-00	B010100	B010109	MICROCIRCUIT,DI:4096 X 8 EPROM (PM107 ONLY)	80009	160-1081-00
A01U2020	160-1081-01	B010110		MICROCIRCUIT,DI:4096 X 8 EPROM,PRGM (PM107 ONLY)	80009	160-1081-01
A01U2030	160-1083-00	B010100	B010124	MICROCIRCUIT,DI:4096 X 8 EPROM (PM106 ONLY)	80009	160-1083-00
A01U2030	160-1083-01	B010125		MICROCIRCUIT,DI:4096 X 8 EPROM,PRGM (PM106 ONLY)	80009	160-1083-01
A01U2030	160-1082-00	B010100	B010109	MICROCIRCUIT,DI:4096 X 8 EPROM (PM107 ONLY)	80009	160-1082-00
A01U2030	160-1082-01	B010110		MICROCIRCUIT,DI:4096 X 8 EPROM,PRGM (PM107 ONLY)	80009	160-1082-01
A01U2040	156-0916-02			MICROCIRCUIT,DI:8-2 INP 3-STATE BFR,BURN	27014	DM81LS97
A01U2050	156-1065-00			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	01295	SN74LS373N OR J
A01U2060	156-1065-00			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	01295	SN74LS373N OR J
A01U3010	156-0469-00			MICROCIRCUIT,DI:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
A01U3020	156-1065-00			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	01295	SN74LS373N OR J
A01U3030	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A01U3035	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A01U3040	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A01U3050	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A01U4030	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A01U4035	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A01U4037	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A01U4039	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A01U4050	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A01U4055	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A01U4057	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A01U4059	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A01U4070	156-1344-00			MICROCIRCUIT,LI:COMPARATOR	52648	SP9685CM
A01U6060	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A01U7010	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A01U7040	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A01U7060	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A02	----- -----			CKT BOARD ASSY:MIDDLE		
A02C1010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C1020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C2010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C2030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C3510	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C3530	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C5010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C5020	283-0144-00			CAP.,FXD,CER DI:33PF,1%,500V	72982	801-547P2G330G
A02C5030	283-0100-00			CAP.,FXD,CER DI:0.0047UF,10%,200V	56289	273C3
A02C6010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C6020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C6030	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A02C6031	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A02R1020	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A02R1030	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A02R1420	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A02R1820	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A02R2020	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A02R3010	315-0103-00 ----- -----	B010100	B010224	RES.,FXD,CMPSN:10K OHM,5%,0.25W (PM106 ONLY)	01121	CB1035
A02R3010	315-0472-00 ----- -----	B010225		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W (PM106 ONLY)	01121	CB4725
A02R3010	315-0103-00 ----- -----	B010100	B010129	RES.,FXD,CMPSN:10K OHM,5%,0.25W (PM107 ONLY)	01121	CB1035
A02R3010	315-0472-00 ----- -----	B010130		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W (PM107 ONLY)	01121	CB4725
A02R3035	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A02R3532	315-0154-00			RES.,FXD,CMPSN:150K OHM,5%,0.25W	01121	CB1545
A02R4010	315-0103-00 ----- -----	B010100	B010224	RES.,FXD,CMPSN:10K OHM,5%,0.25W (PM106 ONLY)	01121	CB1035
A02R4010	315-0202-00 ----- -----	B010225		RES.,FXD,CMPSN:2K OHM,5%,0.25W (PM106 ONLY)	01121	CB2025
A02R4010	315-0103-00 ----- -----	B010100	B010129	RES.,FXD,CMPSN:10K OHM,5%,0.25W (PM107 ONLY)	01121	CB1035
A02R4010	315-0202-00 ----- -----	B010130		RES.,FXD,CMPSN:2K OHM,5%,0.25W (PM107 ONLY)	01121	CB2025
A02R4020	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A02R4025	315-0154-00			RES.,FXD,CMPSN:150K OHM,5%,0.25W	01121	CB1545
A02R4030	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A02R4032	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A02R6012	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A02R6020	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A02R6030	315-0363-00			RES.,FXD,CMPSN:36K OHM,5%,0.25W	01121	CB3635
A02R6032	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A02R6034	321-0808-07			RES.,FXD,FILM:300 OHM,0.1%,0.125W	24546	NE55E3000B
A02R6040	321-0817-07			RES.,FXD,FILM:949.2 OHM,0.1%,0.125W	24546	NE55E949.2 OHM
A02TP7010	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A02U1010	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A02U1020	156-0386-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	04713	SN74LS10N OR J
A02U1030	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A02U2010	156-0567-00			MICROCIRCUIT,DI:DUAL J-K NEG EDGE TRIG F-F	01295	SN74LS113
A02U2020	156-0703-00			MICROCIRCUIT,DI:4-2-3-2 INPUTAND-OR GATES	07263	74S64PC
A02U2030	156-0702-00			MICROCIRCUIT,DI:3 STATE INVERTING HEX BFR	01295	SN74LS366
A02U3010	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	80009	156-0383-00
A02U3520	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A02U3530	156-0392-00			MICROCIRCUIT,DI:QUAD LATCHLEAR	34335	SN74LS175N OR J

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A02U4010	156-0384-00 ----- -----	B010100	B010224	MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE (PM106 ONLY)	80009	156-0384-00
A02U4010	156-0303-01 ----- -----	B010225		MICROCIRCUIT,DI:QUAD 2 INP NAND GATE (PM106 ONLY)	01295	SN74S03NP3
A02U4010	156-0384-00 ----- -----	B010100	B010129	MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE (PM107 ONLY)	80009	156-0384-00
A02U4010	156-0303-01 ----- -----	B010130		MICROCIRCUIT,DI:QUAD 2 INP NAND GATE (PM107 ONLY)	01295	SN74S03NP3
A02U5010	156-0567-00			MICROCIRCUIT,DI:DUAL J-K NEG EDGE TRIG F-F	01295	SN74LS113
A02U5020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A02U5030	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A02U6010	156-0567-00			MICROCIRCUIT,DI:DUAL J-K NEG EDGE TRIG F-F	01295	SN74LS113
A02U6020	156-0875-00			MICROCIRCUIT,DI:DUAL 2 WIDE 2INP AOI GATE	27014	DM74LS51(N OR J)
A02U6030	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A02U7030	156-1451-00			MICROCIRCUIT,DI:3-TERM NEG VOLTAGE RGLTR	27014	LM337T

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A03	----- -----			CKT BOARD ASSY:BOTTOM		
A03C1010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C1030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C1035	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C2010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C2030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C2039	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C3030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C4020	283-0330-00			CAP.,FXD,CER DI:100PF,5%,50V	51642	150-050-NP0-101J
A03C4021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C5020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C5030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C6020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C6030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C7030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03R4020	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A03U1010	156-0875-00			MICROCIRCUIT,DI:DUAL 2 WIDE 2INP AOI GATE	27014	DM74LS51(N OR J)
A03U1020	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0385-00
A03U1030	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A03U2010	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A03U2020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A03U2030	156-0464-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	07263	74LS20PC OR DC
A03U3010	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A03U3020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A03U3030	156-0392-00			MICROCIRCUIT,DI:QUAD LATCHLEAR	34335	SN74LS175N OR J
A03U4010	156-0465-00			MICROCIRCUIT,DI:8-INPUT NAND GATE	27014	DM74LS30NOR J
A03U4030	156-0679-00			MICROCIRCUIT,DI:4-BIT BINARY FULL ADDER	01295	SN74LS283N
A03U5010	156-0386-00 ----- -----	B010100	B010224	MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE (PM106 ONLY)	04713	SN74LS10N OR J
A03U5010	156-0321-02 ----- -----	B010225		MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE (PM106 ONLY)	01295	SN74S10
A03U5010	156-0386-00 ----- -----	B010100	B010129	MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE (PM107 ONLY)	04713	SN74LS10N OR J
A03U5010	156-0321-02 ----- -----	B010130		MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE (PM107 ONLY)	01295	SN74S10
A03U5020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A03U5030	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0385-00
A03U6010	156-0465-00			MICROCIRCUIT,DI:8-INPUT NAND GATE	27014	DM74LS30NOR J
A03U7010	156-0464-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	07263	74LS20PC OR DC
A03U7030	156-0478-00			MICROCIRCUIT,DI:DUAL 4-INPUT AND GATE	01295	SN74LS21N

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966 Drafting Practices.
Y14.2, 1973 Line Conventions and Lettering.
Y10.5, 1968 Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

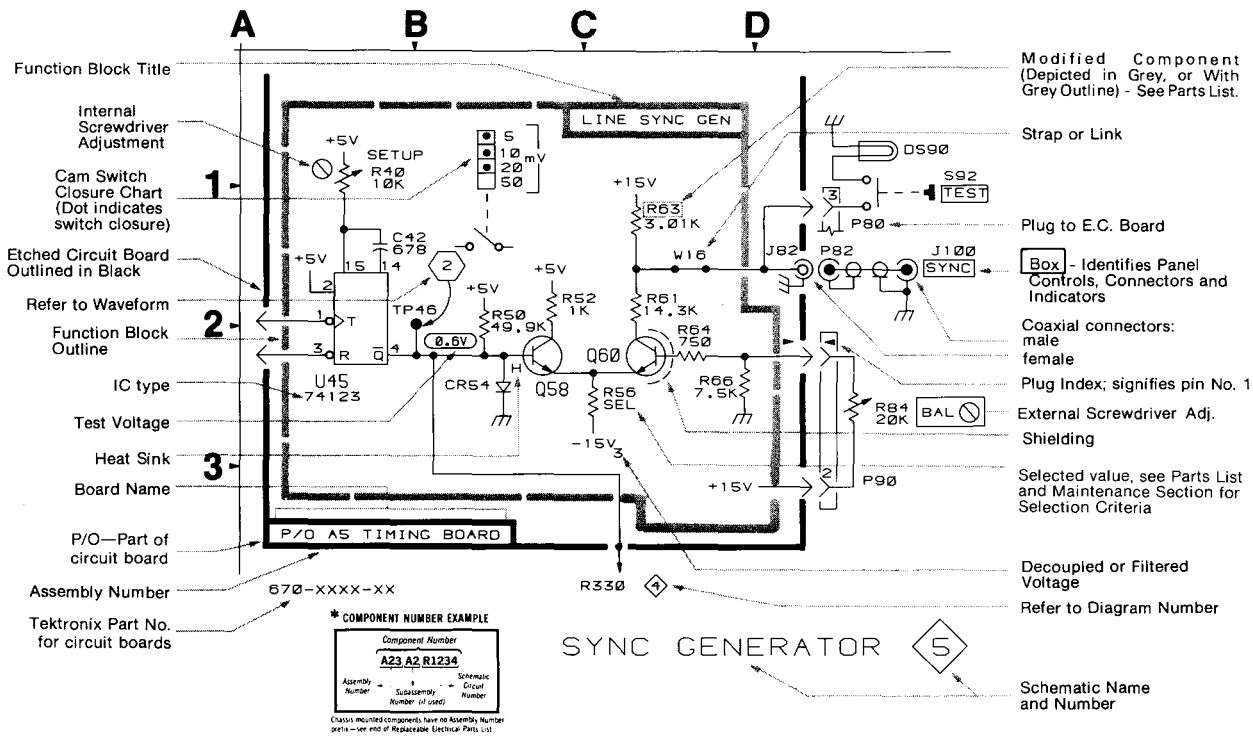
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



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PMI06/PMI07

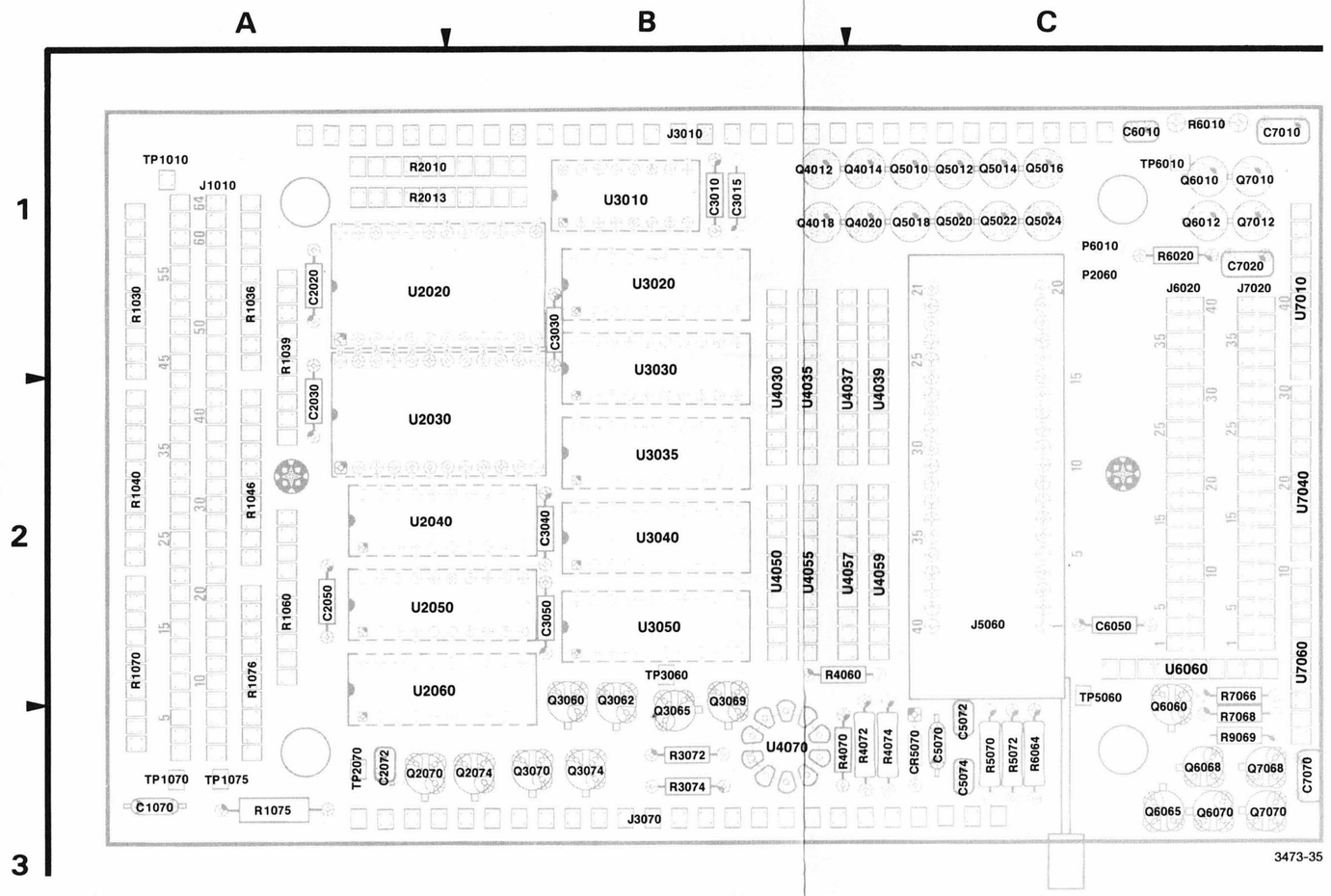

Figure 8-1. A1-Upper board component locations.

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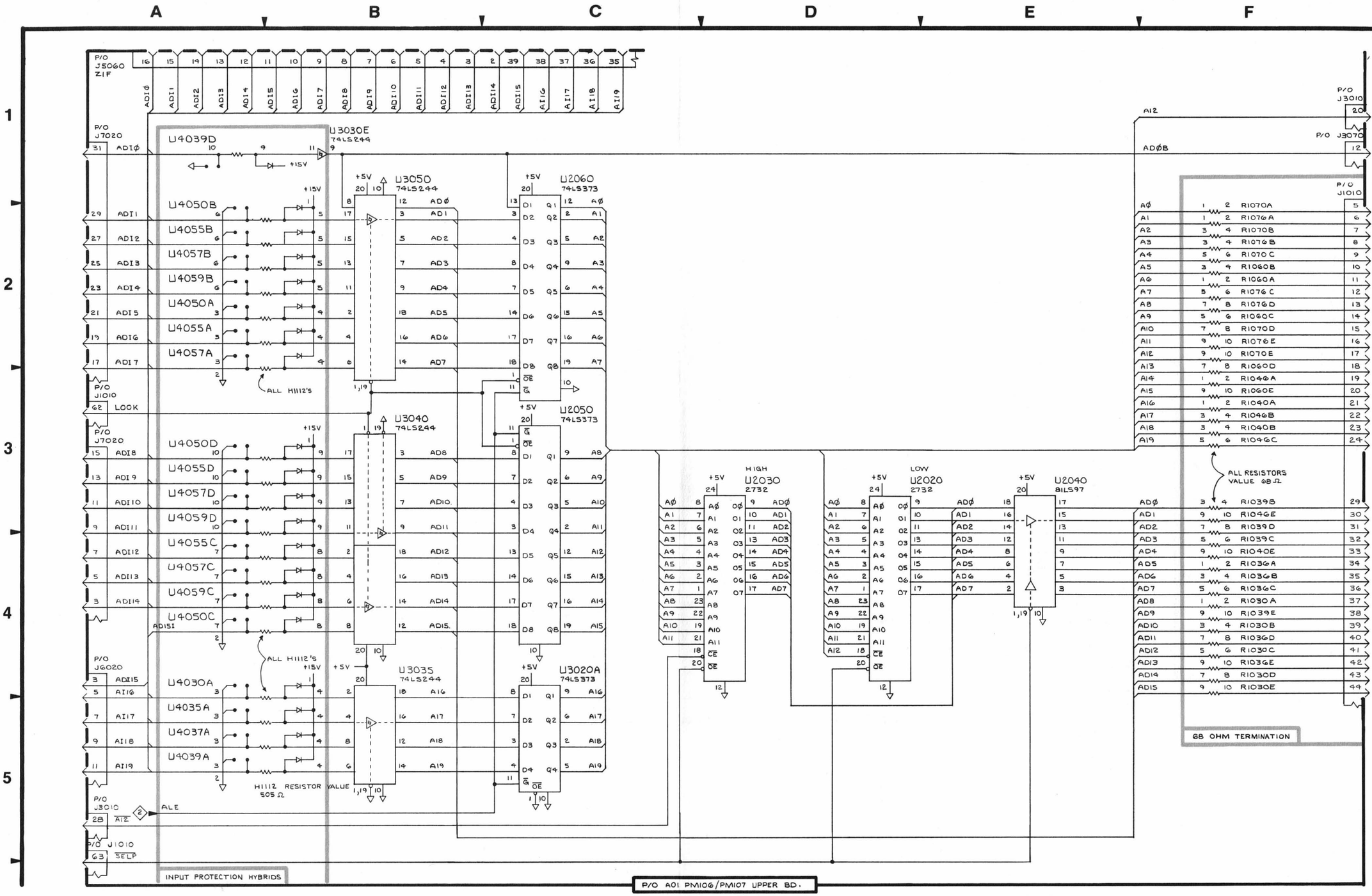
IC PIN INFORMATION

Device Type	VCC	GND
2732	24	12
74LS00	14	7
74LS02	14	7
74LS03	14	7
74LS04	14	7
74LS10	14	7
74LS20	14	7
74LS21	14	7
74LS30	14	7
74LS51	14	7
74LS74	14	7
74LS113	14	7
74LS138	16	8
74LS175	16	8
74LS244	20	10
74LS283	16	8
74LS366	16	8
74LS373	20	10
81LS97	20	10
SP9685	2, 8	1, 16

COMPONENT LOCATIONS
DIAGRAM 1 P/O UPPER BOARD

ASSEMBLY A01

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1010	A3	A1	R1070C	F2	A2
J1010	A5	A1	R1070D	F2	A2
J1010	F2	A1	R1070E	F2	A2
J3010	A5	B1	R1076A	F2	A2
J3010	F1	B1	R1076B	F2	A2
J3070	F1	B3	R1076C	F2	A2
J5060	A1	C2	R1076D	F2	A2
J6020	A4	C2	R1076E	F2	A2
J7020	A3	C2			
J7020	A1	C2	U2020	D4	A1
			U2030	D4	A2
R1030A	F4	A1	U2040	E4	A2
R1030B	F4	A1	U2050	C3	A2
R1030C	F4	A1	U2060	C2	A2
R1030D	F4	A1	U3020A	C5	B1
R1030E	F4	A1	U3030E	B1	B1
R1036A	F4	A1	U3035	B5	B2
R1036B	F4	A1	U3040	B3	B2
R1036C	F4	A1	U3050	B2	B2
R1036D	F4	A1	U4030A	A4	B1
R1036E	F4	A1	U4035A	A5	B1
R1039B	F3	A1	U4037A	A5	C1
R1039C	F4	A1	U4039A	A5	C1
R1039D	F3	A1	U4039D	A1	C1
R1039E	F4	A1	U4050A	A2	B2
R1040A	F3	A2	U4050B	A2	B2
$1040B	F3	A2	U4050C	A4	B2
R1040E	F4	A2	U4050D	A3	B2
R1046A	F3	A2	U4055A	A2	B2
R1046B	F3	A2	U4055B	A2	B2
R1046C	F3	A2	U4055C	A4	B2
R1046E	F3	A2	U4055D	A3	B2
R1060A	F2	A2	U4057A	A2	C2
R1060B	F2	A2	U4057B	A2	C2
R1060C	F2	A2	U4057C	A4	C2
R1060D	F3	A2	U4057D	A3	C2
R1060E	F3	A2	U4059B	A2	C2
R1070A	F2	A2	U4059C	A4	C2
R1070B	F2	A2	U4059D	A3	C2



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P/O UPPER BOARD ⟨1⟩

A1 - UPPER BOARD ⟨1⟩

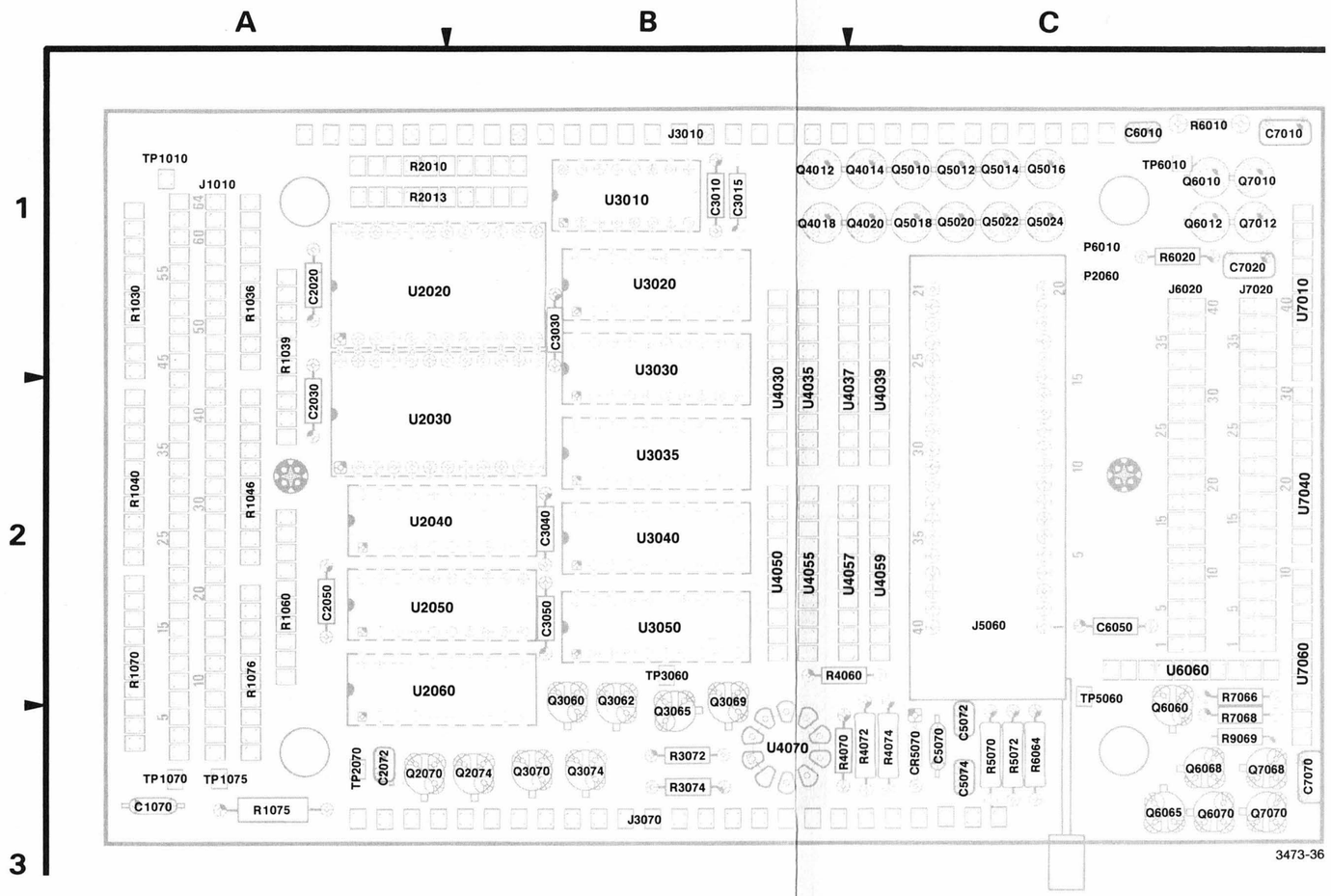
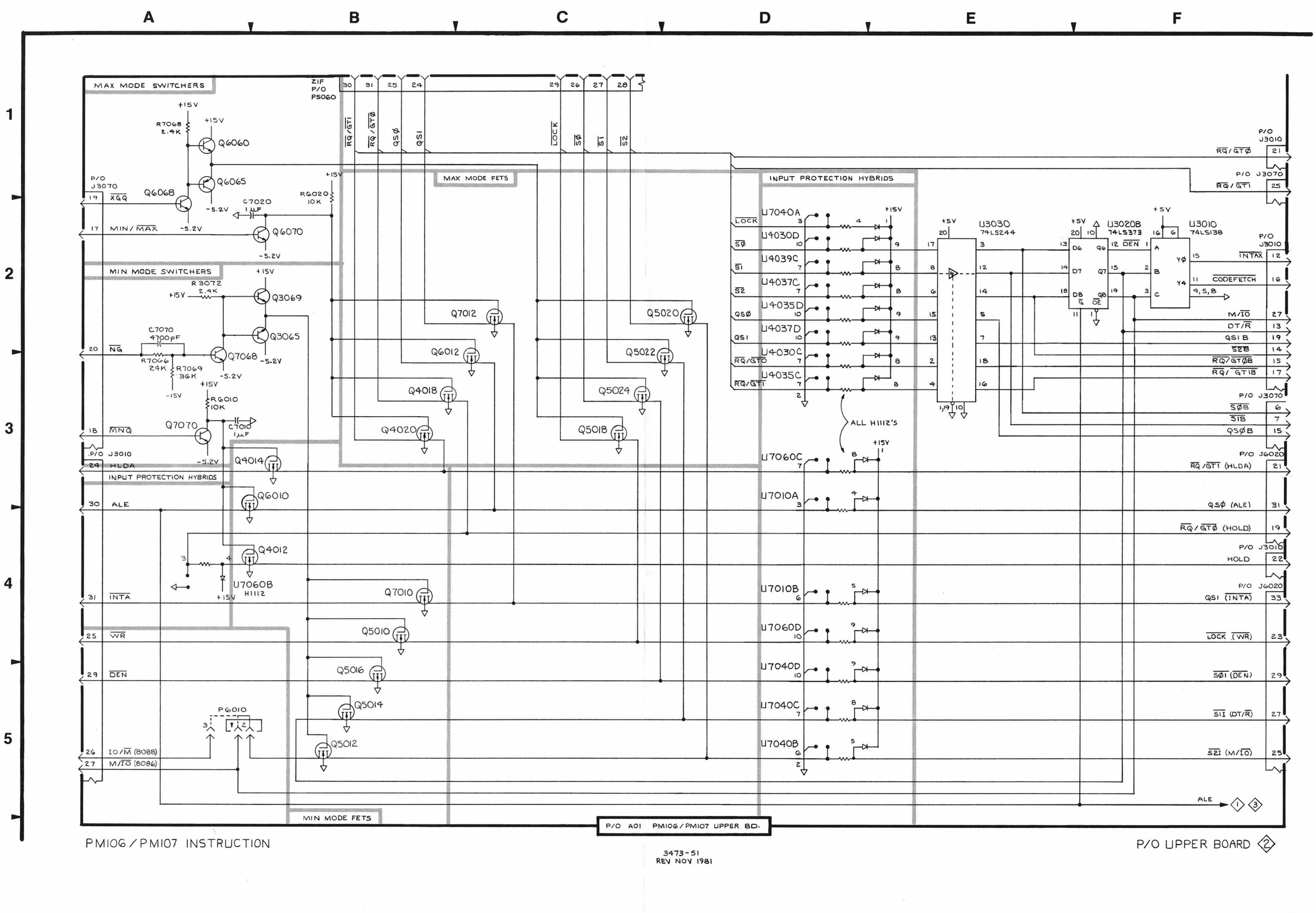


Figure 8-2. A1-Upper board component locations.

COMPONENT LOCATIONS
DIAGRAM 2 P/O UPPER BOARD

ASSEMBLY A01

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C7010	A3	C1	Q6065	A1	C3
C7020	A2	C1	Q6068	A2	C3
C7070	A2	C3	Q6070	B2	C3
			Q7010	B4	C1
J3010	F2	B1	Q7012	C2	C1
J3010	A3	B1	Q7068	A3	C3
J3010	F1	B1	Q7070	A3	C3
J3010	F4	B1			
J3070	F3	B3	R3072	A2	B3
J3070	F1	B3	R6010	A3	C1
J3070	A2	B3	R6020	B2	C1
J5060	B1	C2	R7066	A3	C2
J6020	F3	C2	R7068	A1	C3
J6020	F4	C2	R7069	A3	C3
P6010	A5	C1	U3010	F2	B1
			U3020B	F2	B1
Q3065	B2	B3	U3030	E2	B1
Q3069	B2	B2	U4030C	D3	B1
Q4012	A4	B1	U4030D	D2	B1
Q4014	B3	C1	U4035C	D3	B1
Q4018	B3	B1	U4035D	D2	B1
Q4020	B3	C1	U4037C	D2	C1
Q5010	B4	C1	U4037D	D2	C1
Q5012	B5	C1	U4039C	D2	C1
Q5014	B5	C1	U7010A	D3	C1
Q5016	B5	C1	U7010B	D4	C1
Q5018	C3	C1	U7040A	D2	C2
Q5020	D2	C1	U7040B	D5	C2
Q5022	C3	C1	U7040C	D5	C2
Q5024	C3	C1	U7040D	D5	C2
Q6010	A4	C1	U7060B	A4	C2
Q6012	C3	C1	U7060C	D3	C2
Q6060	A1	C2	U7060D	D4	C2



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P/O UPPER BOARD 2

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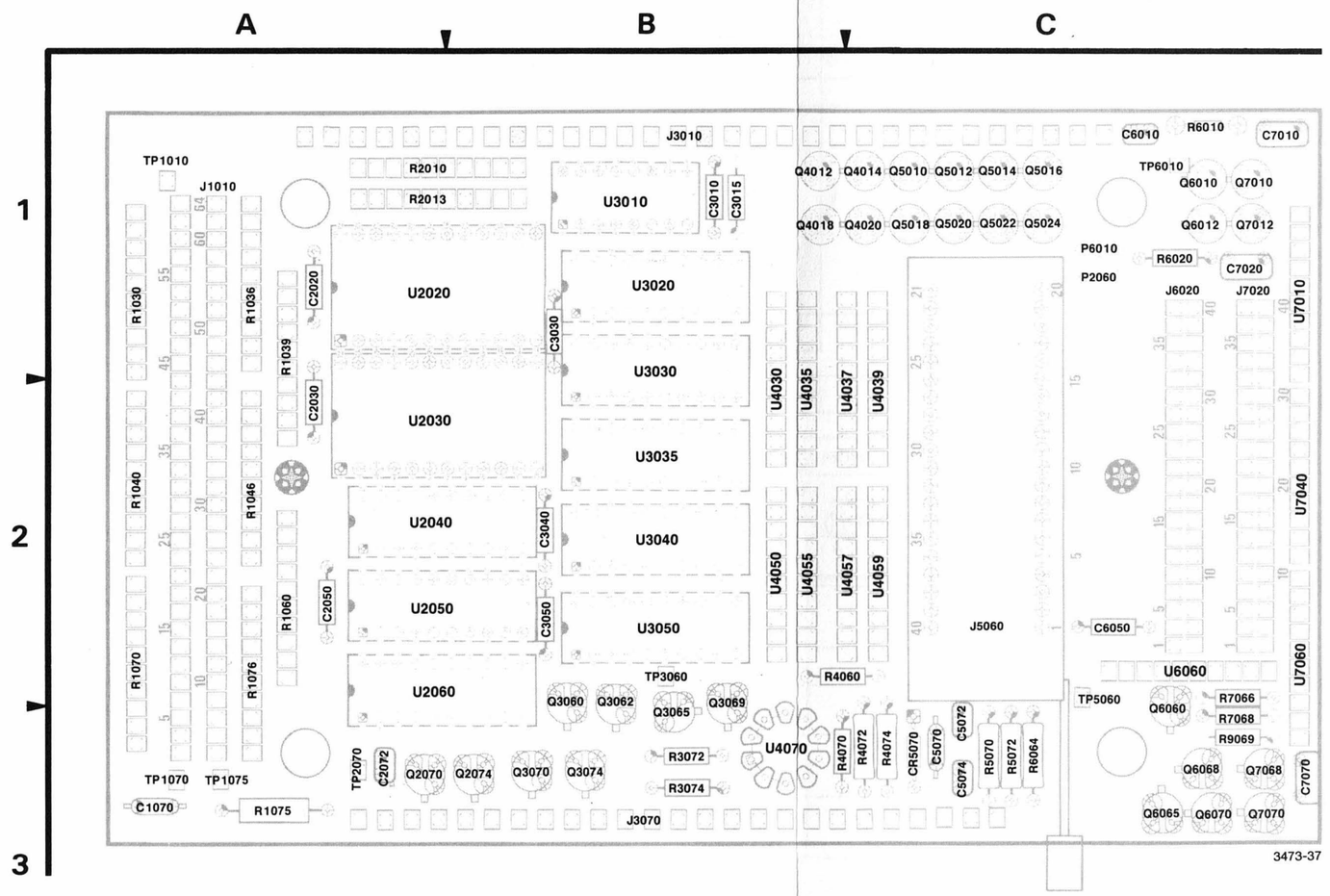
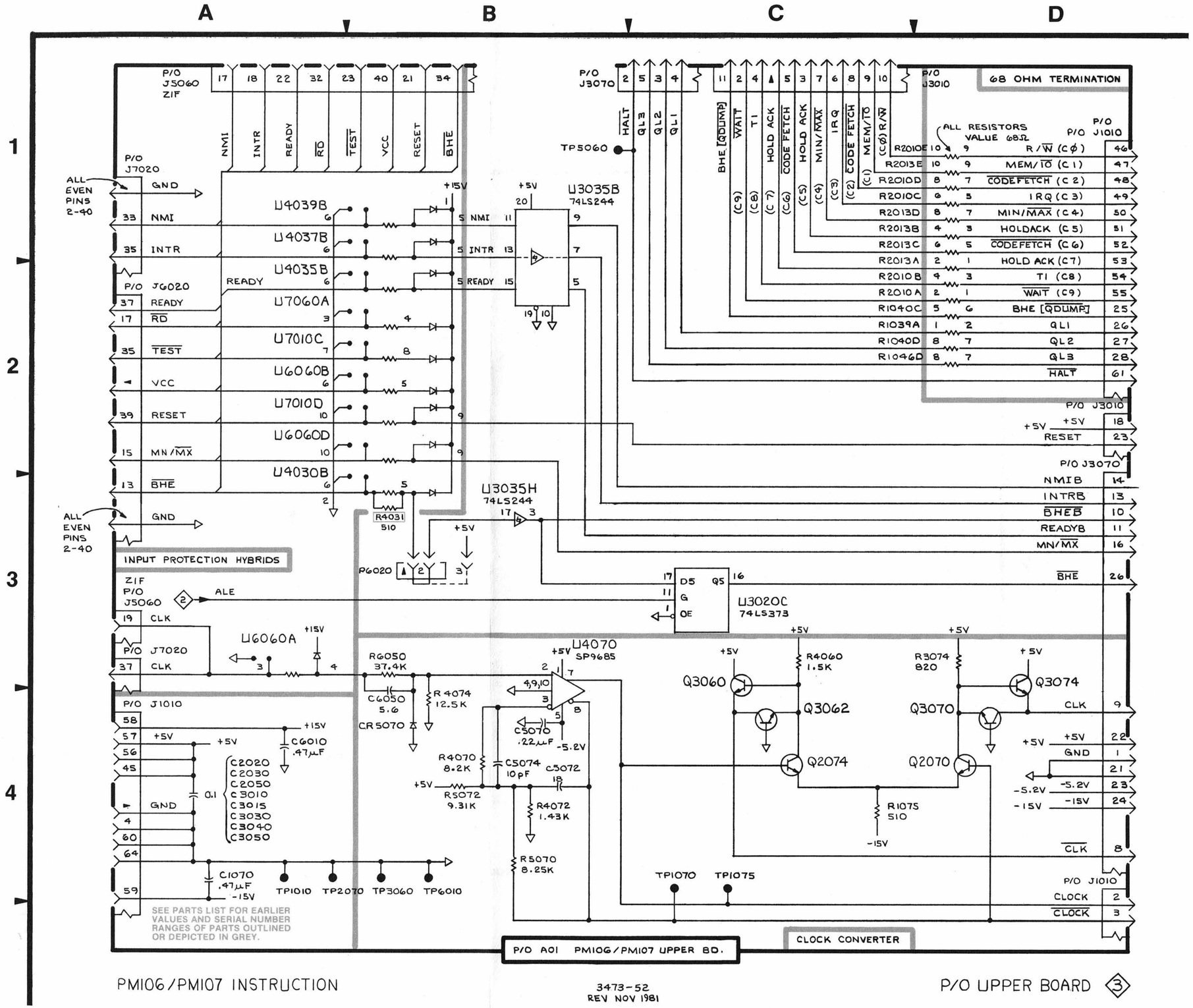


Figure 8-3. A1-Upper board component locations.

COMPONENT LOCATIONS
DIAGRAM 3 P/O UPPER BOARD

ASSEMBLY A01

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1070	A4	A3
C2020	A4	A1
C2030	A4	A2
C2050	A4	A2
C3010	A4	B1
C3015	A4	B1
C3030	A4	B1
C3040	A4	B2
C3050	A4	B2
C5070	B4	C3
C5071	B4	C3
C5072	B4	C3
C6010	A4	C1
C6050	B4	C2
CR5070	B4	C3
J1010	D4	A1
J1010	A4	A1
J1010	D1	A1
J3010	C1	B1
J3010	D2	B1
J3070	C1	B3
J3070	D3	B3
J5060	A1	C2
J5060	A3	C2
J6020	A2	C2
J7020	A1	C2
J7020	A3	C2
P6020	B3	C1
Q2070	D4	A3
Q2074	C4	B3
Q3060	C3	B2
Q3062	C4	B2
Q3070	D4	B3
Q3074	D3	B3
R1039A	D2	A1
R1040C	D2	A2
R1040D	D2	A2
R1046D	D2	A2
R1075	C4	A3
R2010A	D2	A1
R2010B	D2	A1
R2010C	D1	A1
R2010D	D1	A1
R2010E	D1	A1
R2013A	D2	A1
R2013B	D1	A1
R2013C	D1	A1
R2013D	D1	A1
R2013E	D1	A1
R3074	D3	B3
R4060	C3	B2
R4070	B4	B3
R4072	B4	C3
R4074	B4	C3
R5070	B4	C3
R5072	B4	C3
R6050	B3	C3
TP1010	A4	A1
TP1070	C4	A3
TP1075	C4	A3
TP2070	A4	A3
TP3060	B4	B2
TP5060	C1	C2
TP6010	B4	C1
U3020C	C3	B1
U3035B	B1	B2
U3035H	B3	B2
U4030B	A3	B1
U4035B	A2	B1
U4037B	A1	C1
U4039B	A1	C1
U4070	B4	B3
U6060A	A3	C2
U6060B	A2	C2
U6060D	A2	C2
U7010C	A2	C1
U7010D	A2	C1
U7060A	A2	C2



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P/O UPPER BOARD ③

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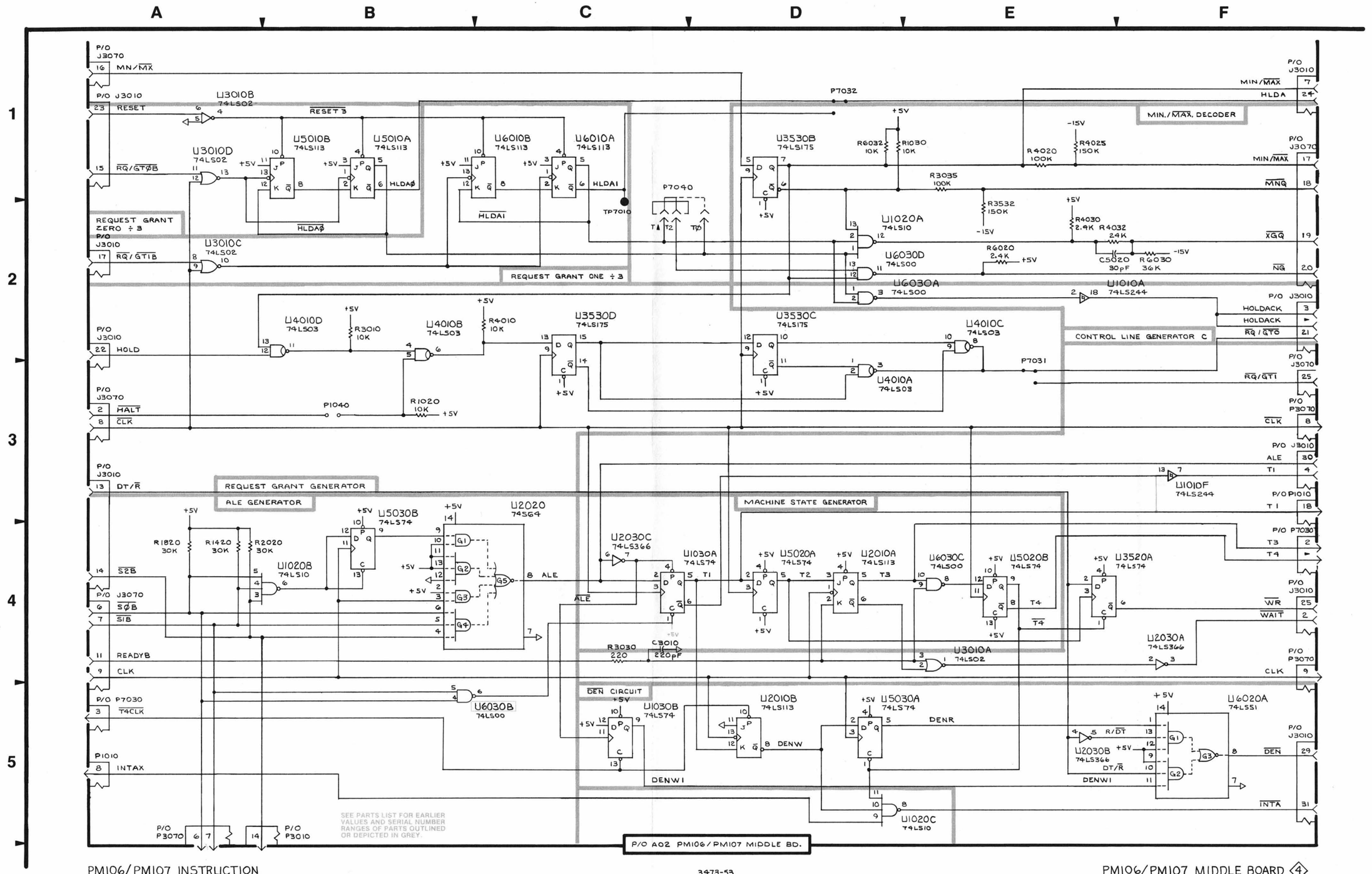
Figure 8-4. A2-Middle board component locations.

COMPONENT LOCATIONS
DIAGRAM 4 P/O MIDDLE BOARD

ASSEMBLY A02

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C3010	C4	B1	R6020	E2	C2
C5030	E2	B2	R6030	F2	B3
			R6032	D1	B2
J3010	A1	B1			
J3010	F5	B1	TP7010	C2	C1
J3010	F1	B1			
J3010	A2	B1	U1010A	E2	A1
J3010	F2	B1	U1010F	F3	A1
J3010	A3	B1	U1020A	D2	A2
J3010	F4	B1	U1020B	B4	A2
J3010	F3	B1	U1020C	D5	A2
J3070	F3	B3	U1030A	C4	A2
J3070	F1	B3	U1030B	C5	A2
J3070	A4	B3	U2010A	D4	A1
J3070	A1	B3	U2010B	D5	A1
J3070	A3	B3	U2020	C4	A2
			U2030A	F4	A2
P1010	A5	A2	U2030B	E5	A2
P1010	F3	A2	U2030C	C4	A2
P1040	B3	A3	U3010B	A1	B1
P3010	A5	B1	U3010C	A2	B1
P3070	F3	A3	U3010C	E4	B1
P3070	F4	A3	U3010D	A1	B1
P3070	A5	A3	U3520A	E4	B2
P7030	F4	C2	U3530B	D1	B2
P7030	A5	C2	U3530C	D2	B2
P7031	E3	C2	U3530D	C2	B2
P7032	D1	C2	U4010A	D3	B1
P7040	C2	C3	U4010B	B2	B1
			U4010C	E2	B1
R1020	B3	A2	U4010D	B2	B1
R1030	D1	A2	U5010A	B1	B1
R1420	A4	A2	U5010B	B1	B1
R1820	A4	A2	U5020A	D4	B2
R2020	A4	B2	U5020B	E4	B2
R3010	B2	B1	U5030A	D5	B2
R3030	C4	B2	U5030B	B4	B2
R3035	E1	B2	U6010A	C1	C1
R3532	E2	B2	U6010B	C1	C1
R4010	C2	B1	U6020A	F5	C2
R4020	E1	B2	U6030A	D2	C2
R4025	E1	B2	U6030C	E4	C2
R4030	E2	B2	U6030D	D2	C2
R4032	E2	B2			



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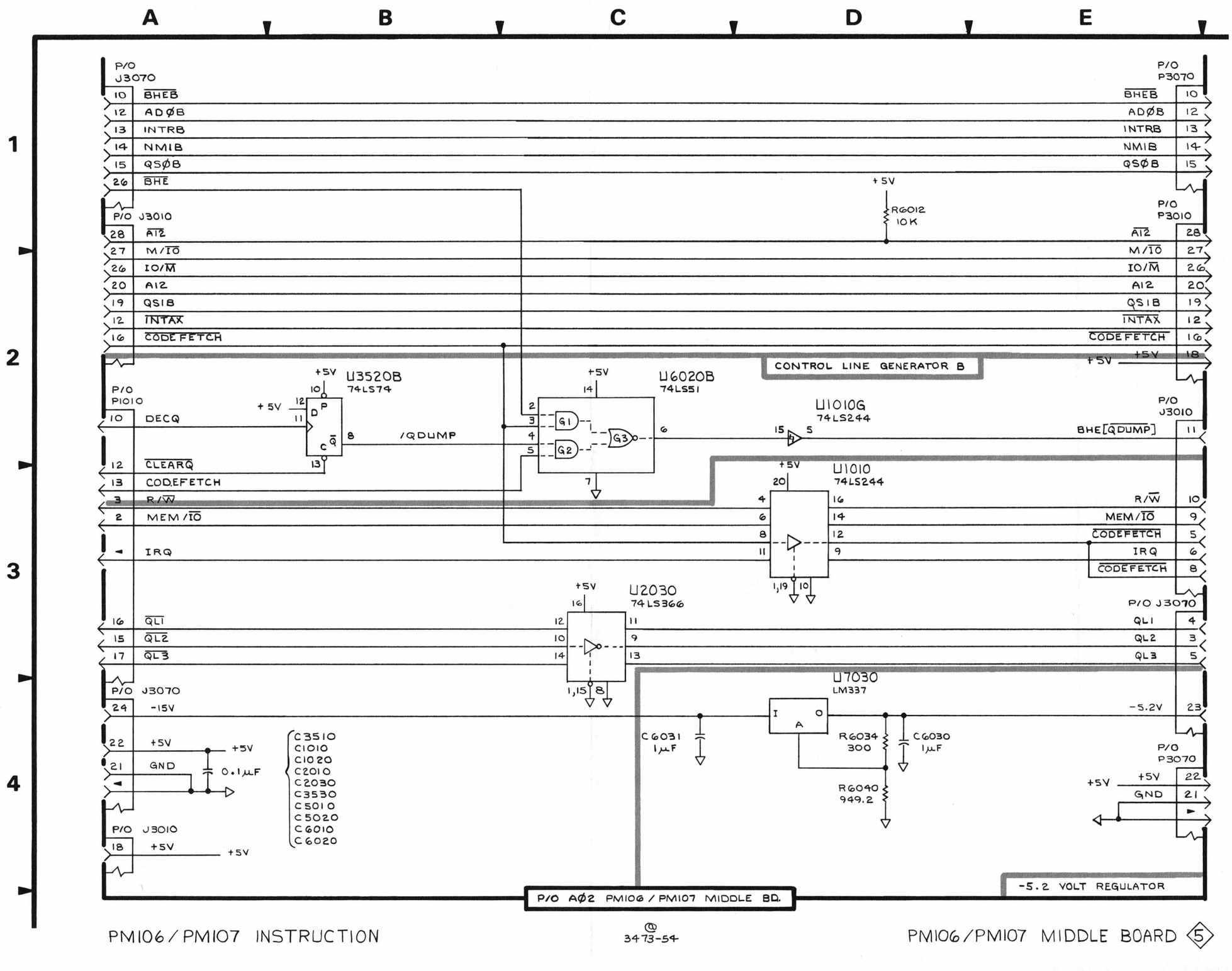
PM106/PM107 MIDDLE BOARD 4

Figure 8-5. A2-Middle board component locations.

COMPONENT LOCATIONS
DIAGRAM 5 P/O MIDDLE BOARD

ASSEMBLY A02

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1010	A4	A2
C1020	A4	A2
C2010	A4	A1
C2030	A4	A2
C3510	A4	B1
C3530	A4	B2
C5010	A4	B1
C5020	A4	B2
C6010	A4	C1
C6020	A4	C2
C6030	D4	B3
C6031	C4	C3
J3010	A4	B1
J3010	E2	B1
J3010	A1	B1
J3070	A4	B3
J3070	E3	B3
J3070	A1	B3
P1010	A2	A2
P3010	E1	B1
P3070	E4	A3
P3070	E1	A3
R6012	D1	B1
R6034	D4	C2
R6040	D4	C3
U1010	D3	A1
U1010G	D2	A1
U2030	C3	A2
U3520B	B2	B2
U6020B	C2	C2
U7030	D4	C2



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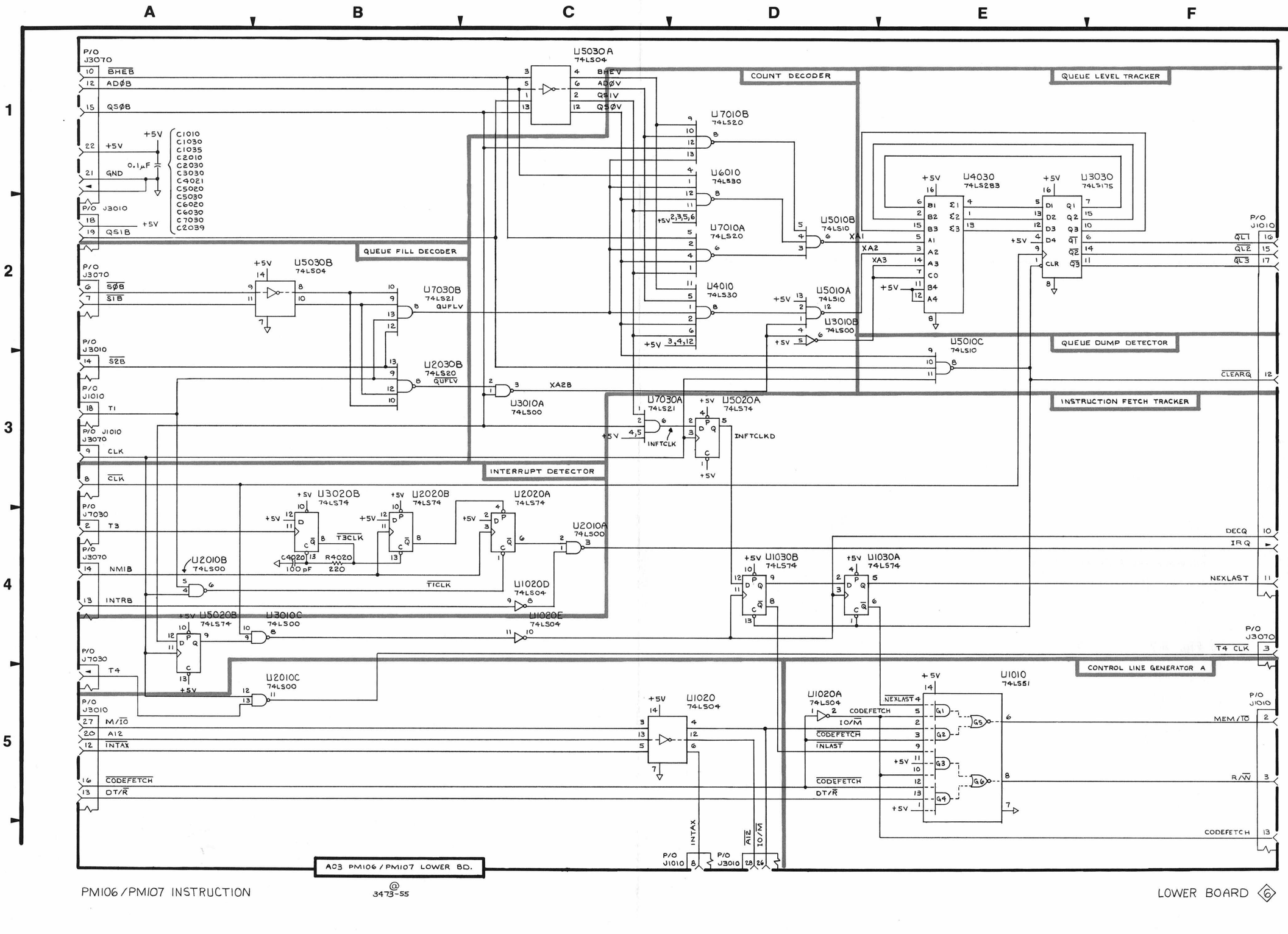
PM106/PM107 MIDDLE BOARD 5

Figure 8-6. A3-Lower board component locations.

COMPONENT LOCATIONS
DIAGRAM 6 P/O LOWER BOARD

ASSEMBLY A03

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1010	A1	A2	U1010	E5	A1
C1030	A1	A3	U1020	D5	A2
C1035	A1	A2	U1020A	D5	A2
C2010	A1	B2	U1020D	C4	A2
C2030	A1	A3	U1020E	C4	A2
C2039	A1	B2	U1030A	D4	A2
C3030	A1	B2	U1030B	D4	A2
C4020	B4	B2	U2010A	C4	B1
C4021	A1	B2	U2010B	A4	B1
C5020	A1	C2	U2010C	B5	B1
C5030	A1	C2	U2020A	C4	B2
C6020	A1	C2	U2020B	B4	B2
C6030	A1	C2	U2030	B3	B2
C7030	A1	C3	U3010A	C3	B1
			U3010B	D2	B1
J1010	F5	A2	U3010C	B4	B1
J1010	A3	A2	U3020B	B4	B2
J1010	D5	A2	U3030	E2	B2
J1010	F2	A2	U4010	D2	B1
J3010	A3	B1	U4030	E2	B2
J3010	A5	B1	U5010A	D2	B1
J3010	D5	B1	U5010B	D2	B1
J3010	A2	B1	U5010C	E3	B1
J3070	A2	A3	U5020A	D3	B2
J3070	A1	A3	U5020B	A4	B2
J3070	F4	A3	U5030A	C1	B2
J3070	A3	A3	U5030B	B2	B2
J3070	A4	A3	U6010	D2	C1
J7030	A5	C2	U7010A	D2	C1
J7030	A4	C2	U7010B	D1	C1
			U7030A	C3	C2
R4020	B4	B2	U7030B	B2	C2



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LOWER BOARD 6

A3 - LOWER BOARD 6

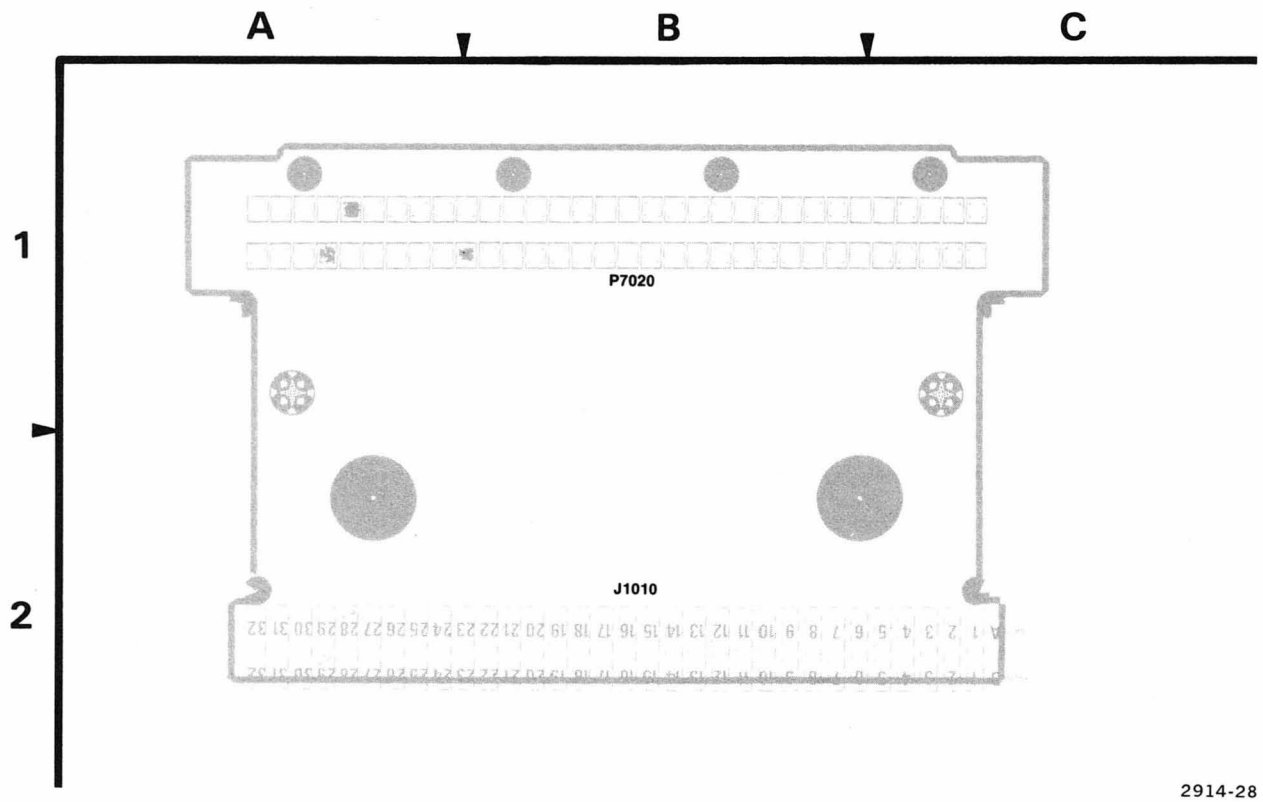
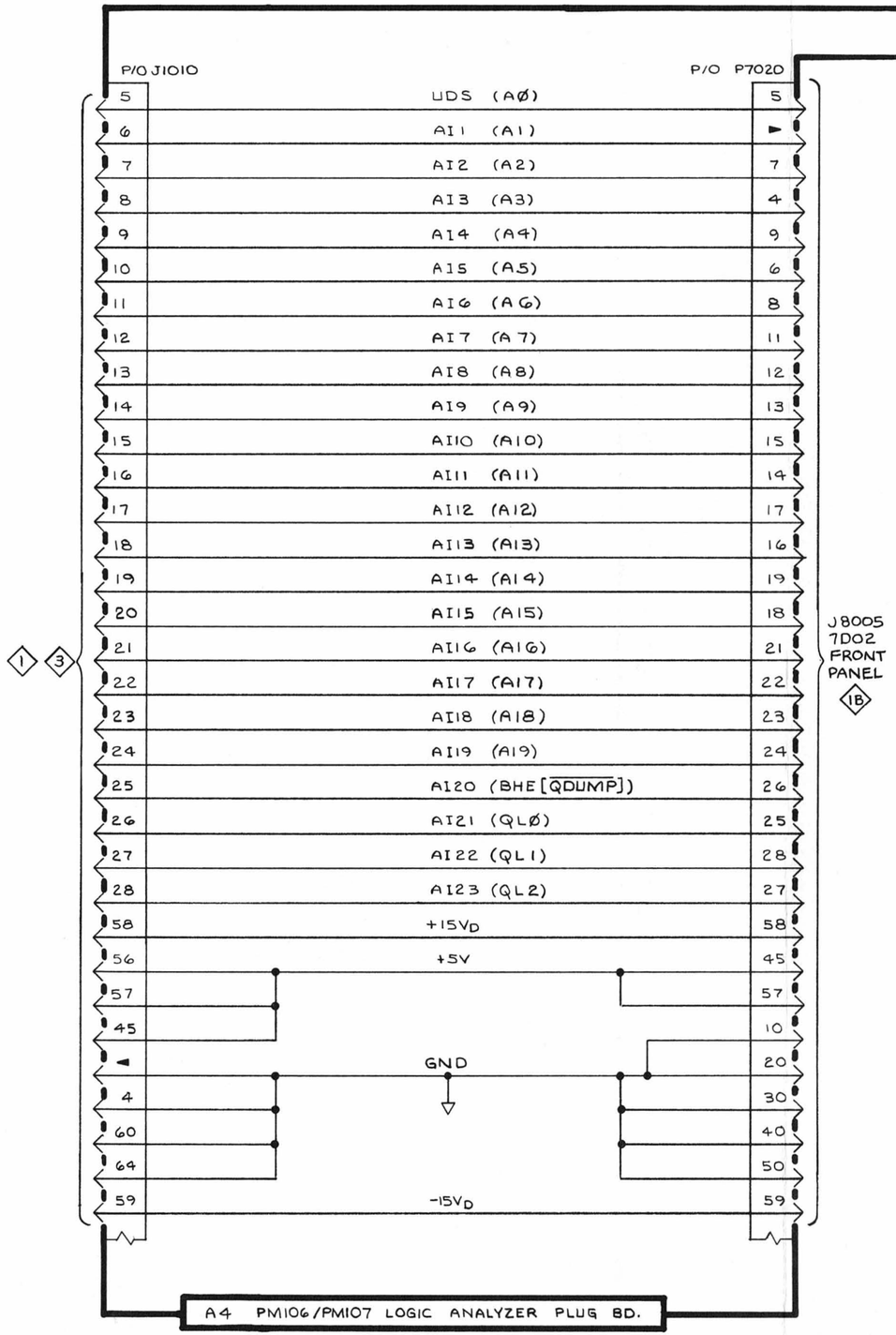


Fig. 8-7. PMI06/PMI07 Logic Analyzer Plug Bd.



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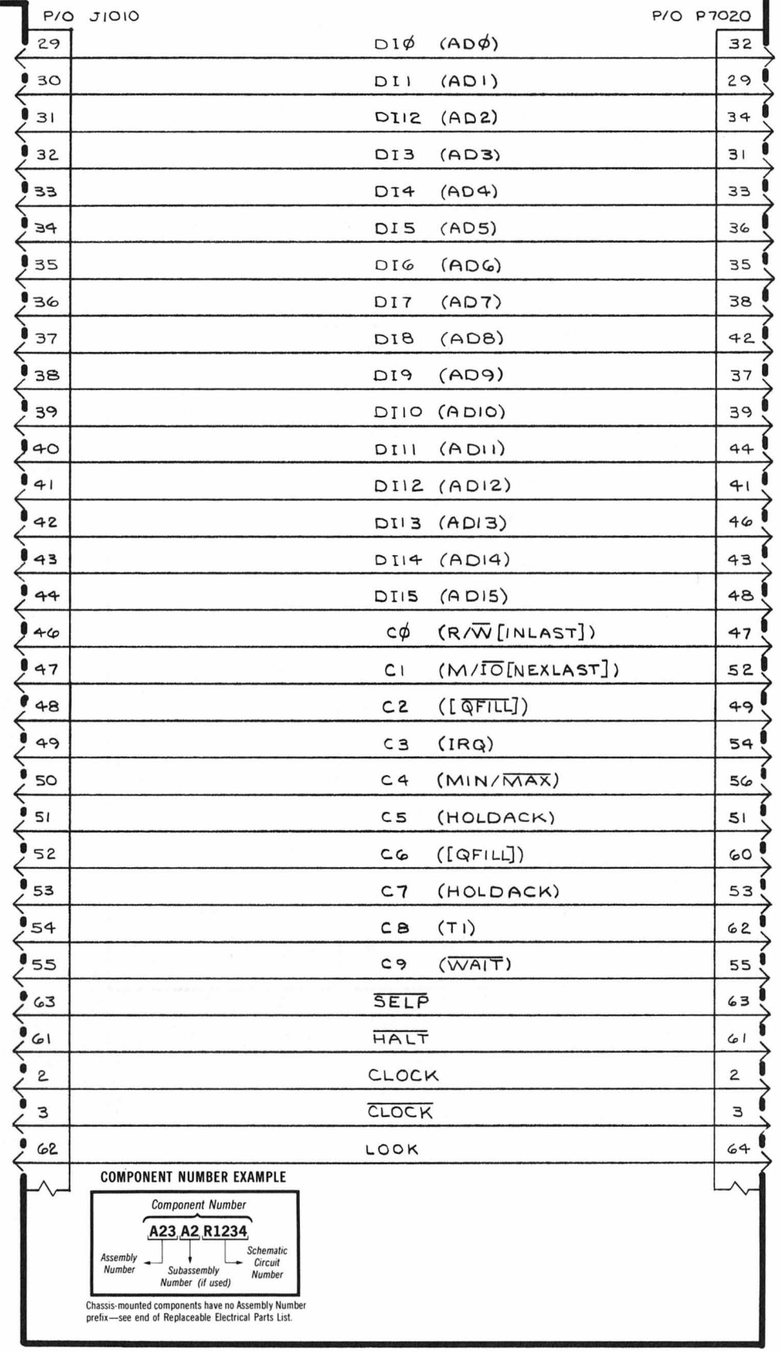


PM106/PM107 LOGIC ANALYZER PLUG ◇7◇

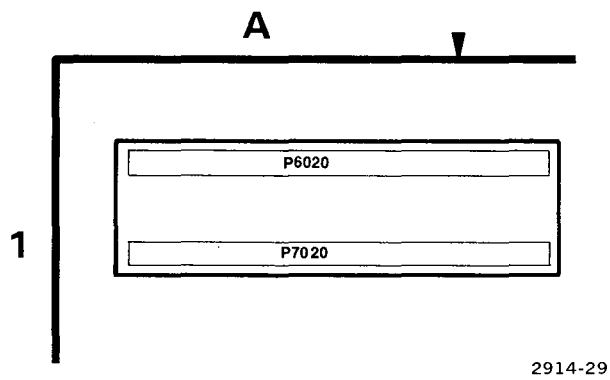
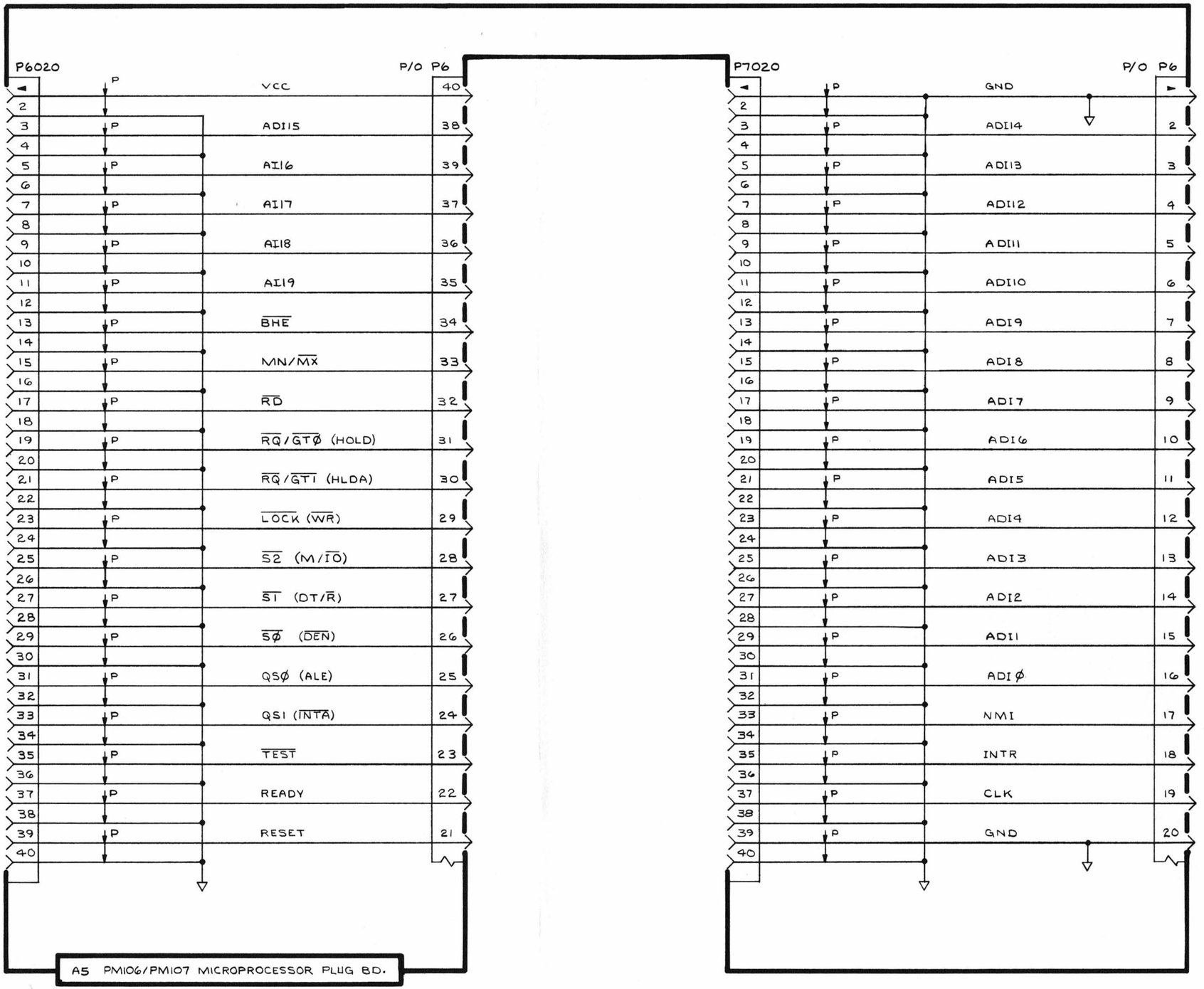


Fig. 8-8. PMI06/PMI07 Microprocessor Plug Bd.



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PM106/PM107 MICROPROCESSOR PLUG BD. ◇8

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
\- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
\- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
\- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000AH	STANDARD PRESSED STEEL CO., UNBRAKO DIV.	8535 DICE ROAD	SANTA FE SPRINGS, CA 90670
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
19613	TEXTOOL PRODUCTS, INC.	1410 W PIONEER DRIVE	IRVING, TX 75061
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
23880	STANFORD APPLIED ENGINEERING, INC.	340 MARTIN AVE.	SANTA CLARA, CA 95050
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
78488	STACKPOLE CARBON CO.		ST. MARYS, PA 15857
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83294	ARROW FASTENER CO., INC.	271 MAYHILL ST.	SADDLE BROOK, NJ 07662
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
93907	TEXTRON INC. CAMCAR DIV	600 18TH AVE	ROCKFORD, IL 61101

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	334-3963-00			1		PLATE,IDENT:MKD PM106	80009	334-3963-00
	----- -----			-		(PM106 ONLY)		
	334-4068-00			1		PLATE,IDENT:MKD 8088	80009	334-4068-00
	----- -----			-		(PM107 ONLY)		
-2	380-0593-01			1		HSG HALF,CKT BD:TOP	80009	380-0593-01
						(ATTACHING PARTS)		
-3	211-0306-00			4		SCREW,CAP:4-40 X 1.125,HEX,SKT HD	83294	OBD
						- - - * - - -		
-4	380-0652-00			1		HSG HALF,CKT BD:BOTTOM	80009	380-0652-00
-5	343-0836-00			4		CLAMP,CABLE:3.72 L,ALUMINUM	80009	343-0836-00
						(ATTACHING PARTS)		
-6	211-0093-00			4		SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
-7	210-0586-00			4		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
	175-3030-00			1		CA ASSY,SP,ELEC:40,28 AWG,15.0 L	80009	175-3030-00
	200-2445-00			1		. COVER,PROBE:PIN PROTECTOR,PLASTIC	80009	200-2445-00
-8	386-3814-00			1		. PLATE,CONN BODY:	80009	386-3814-00
-9	352-0536-00			1		. HOLDER,CONTACT:40 PIN,NYLON	80009	352-0536-00
						(ATTACHING PARTS)		
-10	211-0102-00			2		. SCREW,MACHINE:4-40 X 0.500",FLH,STL	83385	OBD
						- - - * - - -		
-11	334-3754-00			1		. MARKER,IDENT:P7020	80009	334-3754-00
-12	334-3753-00			1		. MARKER,IDENT:P6020	80009	334-3753-00
-13	----- -----			1		. CKT BOARD ASSY:8086/8088 PROBE(SEE A05 REPL)		
-14	131-2093-00			2		. . SKT,PL-IN ELEK:MICROCKT,20 CONT,LOW PF	23880	CSA-3200-208
	276-0507-00			1		. . SHIELDING BEAD,:FERRITE	78488	57-3443
-15	200-2429-00			1		. . CABLE NIP,ELEC:0.69 L X 3.6 W,PLASTIC	80009	200-2429-00
	131-2749-00			1		CONN,RCPT,ELEC:CABLE,32/64 MALE	80009	131-2749-00
-16	334-3722-00			1		. PLATE,IDENT:P6460 MICROPROC PROBE	80009	334-3722-00
-17	380-0591-00			1		. HSG HALF,CKT BD:TOP	80009	380-0591-00
						(ATTACHING PARTS)		
-18	211-0225-00			2		. SCR,CAP,SOC HD:4-40 X 0.312 INCH,STL	000AH	OBD
-19	211-0093-00			2		. SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
-20	210-0551-00			4		. NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	000BK	OBD
	213-0055-00			4		. SCR,TPG,THD FOR:2-32 X 0.188 INCH,PNH STL	93907	OBD
						- - - * - - -		
-21	380-0590-01			1		. HSG,HALF:	80009	380-0590-01
-22	343-0836-00			2		. CLAMP,CABLE:3.72 L,ALUMINUM	80009	343-0836-00
-23	200-2412-00			2		. CABLE NIP,ELEC:3.45 L X 0.05ID,PLASTIC	80009	200-2412-00
-24	175-4741-01			1		. CA ASSY,SP,ELEC:64,28 AWG,48.0 L,RIBBON	80009	175-4741-01
	213-0055-00			4		. SCR,TPG,THD FOR:2-32 X 0.188 INCH,PNH STL	93907	OBD
-25	----- -----			1		. CKT BOARD ASSY:PROBE CONNECTOR(SEE A04 REPL)		
-26	131-0608-00			64		. . TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-27	361-0998-00			8		SPACER,CKT BD:0.245 ID X 0.380 OD X 0.23 H	80009	361-0998-00
-28	----- -----			1		CKT BOARD ASSY:UPPER(SEE A01 REPL)		
-29	131-0608-00			111		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-30	131-0590-00			55		. CONTACT,ELEC:0.71 INCH LONG	22526	47351
-31	131-0589-00			40		. TERMINAL,PIN:0.46 L X 0.025 SQ	22526	47350
-32	136-0252-07			10		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-33	136-0537-00			1		. SOCKET,PLUG-IN:40 PIN,W/LOCKING LEVER	19613	240-0333-00-0602
-34	136-0578-00			2		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-35	----- -----			1		CKT BOARD ASSY:MIDDLE(SEE A02 REPL)		
-36	136-0263-04			55		. SOCKET,PIN TERM:FOR 0.025 INCH SQUARE PIN	22526	75377-001
	----- -----			1		. TEST POINT:(SEE A02TP7010 REPL)		
-37	131-0590-00			37		. CONTACT,ELEC:0.71 INCH LONG	22526	47351
-38	----- -----			1		. MICROCIRCUIT,DI:(SEE A02U7030 REPL)		
						(ATTACHING PARTS)		
-39	211-0008-00			1		. SCREW,MACHINE4-40 X 0.250,PNH,STL,CD PL	83385	OBD
-40	210-0406-00			1		. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
						- - - * - - -		
-41	----- -----			1		CKT BOARD ASSY:LOWER(SEE A03 REPL)		
-42	136-0263-04			35		. SOCKET,PIN TERM:FOR 0.025 INCH SQUARE PIN	22526	75377-001

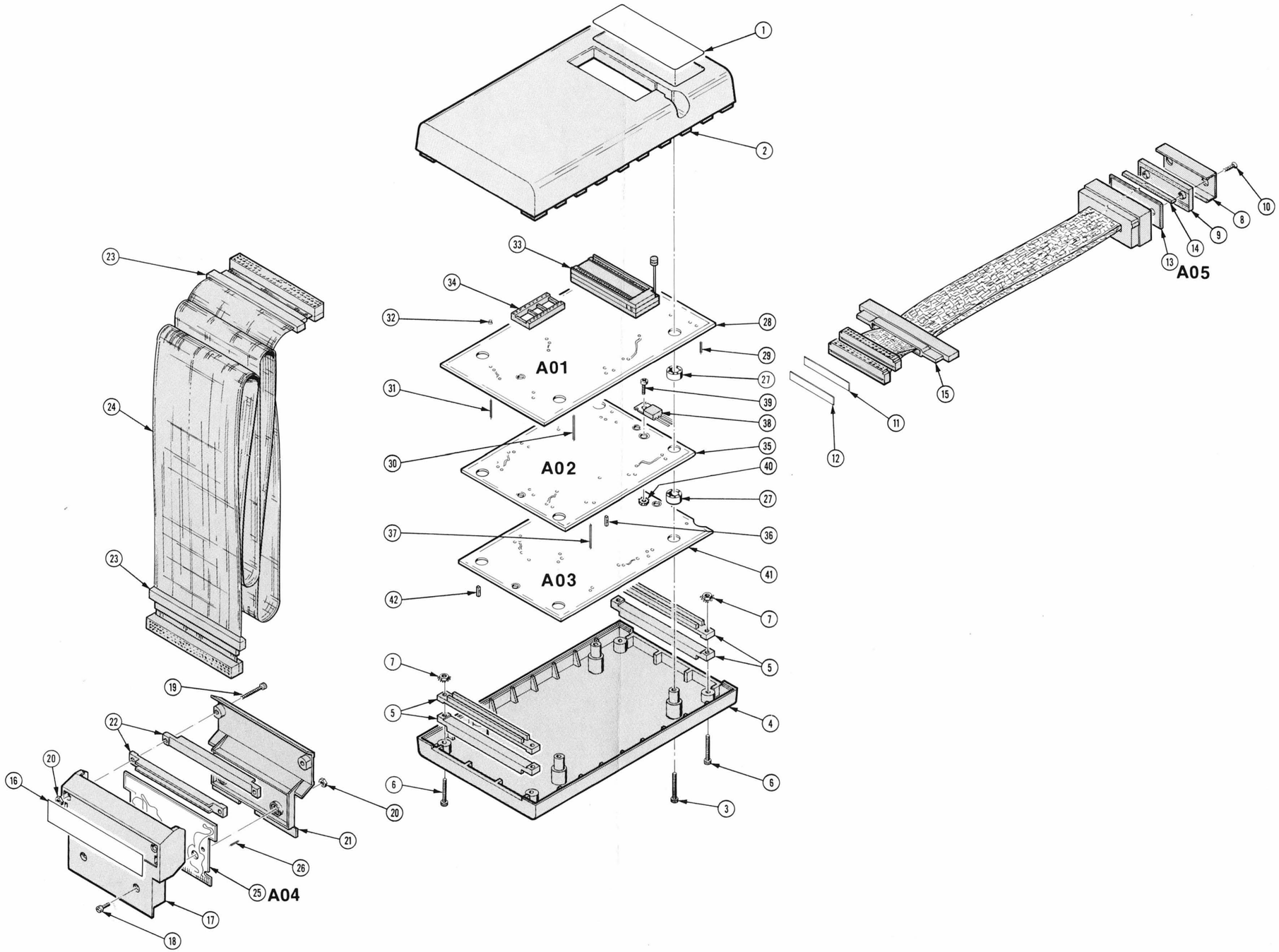

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						STANDARD ACCESSORIES		
	070-3473-00			1		MANUAL,TECH:INSTRUCTION	80009	070-3473-00

@

SIGNAL GLOSSARY

This section contains an alphabetical listing of all the signals which go to or from the PM106/107 Personality Module as well as a brief description of what each signal does.

SIGNAL	DESCRIPTION
A0-A19	Address lines from the personality module to the logic analyzer. (A0-A12 bidirectional).
A20	Multiplexed address line from the personality module to the logic analyzer; also called BHE[/QDUMP].
A21-A23	Address lines from the personality module to the logic analyzer; also called QL1-QL3.
AD0-AD15	Multiplexed address data lines from the personality module to the logic analyzer. (AD0-AD7 bidirectional).
ADI0-ADI15	Bidirectional multiplexed address data lines from the system under test to the personality module.
ALE	Address latch enable (ALE) line from the personality module to the system under test; emulated in the minimum mode to latch information on the address data bus.
$\overline{\text{BHE}}$	Inverted byte high enable ($\overline{\text{BHE}}$) line from the microprocessor to the system under test; used to validate bytes that are transferred on the data bus.
CLK	External clocking signal line from the system under test to the personality module; provides a clock signal to the microprocessor and the clock converter circuit.
CLOCK	ECL clock line from the personality module to the logic analyzer; derived from the CLK signal.
$\overline{\text{CLOCK}}$	Inverted ECL clock line from the personality module to the logic analyzer; derived from the CLK signal.

SIGNAL	DESCRIPTION
$\overline{\text{CODEFETCH}}$	Control line C2 and C6 from the personality module to the logic analyzer; selects the meaning of lines C0, C1 and A20.
C0	Control line R/$\overline{\text{W}}$ from the personality module to the logic analyzer; represents the read/$\overline{\text{write}}$ selection or last fetched [LST-F] information.
C1	Control line MEM/$\overline{\text{IO}}$ from the personality module to the logic analyzer; represents the memory/$\overline{\text{input-output}}$ selection or second last fetched [2LS-F] information.
C2	Control line from the personality module to the logic analyzer; selects the meaning of the lines C0, C1, and A20. See $\overline{\text{CODEFETCH}}$.
C3	Control line IRQ from the personality module to the logic analyzer; signals the presence of an interrupt request state.
C4	Control line MIN/$\overline{\text{MAX}}$ from the personality module to the logic analyzer; represents the minimum or maximum mode selection.
C5	Control line HOLDACK from the personality module to the logic analyzer; signals the presence of a hold acknowledge state.
C6	Control line from the personality module to the logic analyzer; selects the meaning of the lines C0, C1 and A20. See $\overline{\text{CODEFETCH}}$.
C7	Control line from the personality module to the logic analyzer; carries hold acknowledge information the same as control line C5.

SIGNAL	DESCRIPTION
C8	Control line from the personality module to the logic analyzer; carries the condition of machine state T1 (ESYNC).
C9	Control line from the personality module to the logic analyzer; carries the condition of the $\overline{WAIT}$ control signal.
$\overline{DEN}$	Data enable signal from the personality module to the system under test; emulated in the minimum mode on the $\overline{S0}$ line.
DT/$\overline{R}$	The data transmit/$\overline{receive}$ signal from the personality module to the system under test; emulated in the minimum mode on the $\overline{S1}$ line.
$\overline{HALT}$	Interrupt command from the logic analyzer to the personality module; halts the processor under test. See the strapping procedure to implement this interrupt command (in the Maintenance and Troubleshooting section).
HOLD	Hold request signal line from the system under test to the personality module; used in the minimum mode on the $\overline{RQ}$/$\overline{GT0}$ or $\overline{RQ}$/$\overline{GT1}$ lines.
HOLDACK	Hold acknowledge signal line from the personality module to the logic analyzer; also called control lines C5 and C7.
HLDA	Hold acknowledge signal line from the personality module to the system under test; emulated in the minimum mode on the $\overline{RQ}$/$\overline{GT0}$ or $\overline{RQ}$/$\overline{GT1}$ lines.
$\overline{INTA}$	Interrupt acknowledge signal from the personality module to the system under test; emulated in the minimum mode on the QS1 line.
INTR	Interrupt request signal from the system under test to the personality module.
IRQ	Interrupt request signal from the personality module to the logic analyzer; also called control line C3.
$\overline{LOCK}$	Bus priority $\overline{LOCK}$ signal from the personality module to the system under test; locks out the maximum mode of operation.
LOOK	Input look signal from the logic analyzer to the personality module; controls address and data transmission.
MEM/$\overline{IO}$	The memory/$\overline{input\text{-}output}$ signal from the personality module to the logic analyzer also called control line C1; signals a Memory or an Input-Output device access.
MIN/$\overline{MAX}$	The minimum/$\overline{maximum}$ mode signal from the personality module to the logic analyzer also called control line C4; signals the selected mode of operation.
M/$\overline{IO}$	The memory/$\overline{input\text{-}output}$ signal from the personality module to the system under test; emulated in the minimum mode on the $\overline{S2}$ line to select either device.
MN/$\overline{MX}$	The minimum/$\overline{maximum}$ mode signal from the system under test to the personality module; selects the mode of operation.
NMI	The non-maskable interrupt request from the system under test to the personality module.
$\overline{QDUMP}$	The queue dump signal line from the personality module to the logic analyzer; multiplexed with BHE on A20 to indicate a queue dump event.
QL1	Queue level 1 signal line from the personality module to the logic analyzer also called A21; provides level 1's bit of queue level information for instruction fetch calculation.
QL2	Queue level 2 signal line from the personality module to the logic analyzer also called A22; provides level 2's bit of queue level information for instruction fetch calculation.
QL3	Queue level 3 signal line from the personality module to the logic analyzer also called A23; provides level 4's bit of queue level information for instruction fetch calculation.

SIGNAL	DESCRIPTION
QS0	Instruction queue status line 0 from the personality module to the system under test; provides information on bytes taken from the queue.
QS1	Instruction queue status line 1 from the personality module to the system under test; provides information on bytes taken from the queue.
READY	The wait state (Tw) control line from the system under test to the personality module; enables the insertion of Tw between machine states T3 and T4.
RESET	System reset line from the system under test to the personality module.
$\overline{RQ}/\overline{GT0}$	Bidirectional request/grant 0 access line between the personality module and the system under test.
$\overline{RQ}/\overline{GT1}$	Bidirectional request/grant 1 access line between the personality module and the system under test.
R/$\overline{W}$	The read/$\overline{write}$ signal line from the personality module to the logic analyzer also called control line C0; selects the Read or Write function.
$\overline{SELP}$	Select PROM signal line from the logic analyzer to the personality module; selects the contents of the personality EPROMS.
$\overline{S0}$	Bus cycle status line 0 from the personality module to the system under test; used in determining current bus operations.
$\overline{S1}$	Bus cycle status line 1 from the personality module to the system under test; used in determining current bus operations.
$\overline{S2}$	Bus cycle status line 2 from the personality module to the system under test; used in determining current bus operations.
$\overline{TEST}$	Signal line from the system under test to the personality module; used with the $\overline{WAIT}$ instruction wherein the CPU may enter an idle state depending upon the condition of the $\overline{TEST}$ line.
$\overline{T1}$	Machine state T1 line from the personality module to the logic analyzer; also called control line C8.
$\overline{WAIT}$	The $\overline{WAIT}$ control line from the personality module to the logic analyzer; also called control line C9.
$\overline{WR}$	Inverted write control line from the personality module to the system under test; emulated in the minimum mode on the $\overline{LOCK}$ signal line.

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

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MANUAL CHANGE INFORMATION

Date: 4-22-82 **Change Reference:** C3/482

Product: PM 106/PM 107 Personality Module **Manual Part No.:** 070-3473-00

DESCRIPTION

REPLACEABLE ELECTRICAL PARTS LIST AND DIAGRAM CORRECTIONS

Electrical Parts List A02C5020 and A025030

CHANGE TO:

A02C5020	281-0775-00	CAP.,FXD,CER DI:0.1UF,20%,50V
A02C5030	283-0144-00	CAP.,FXD,CER DI:33PF,1%,500V

Diagram 4 grid location E2, C5020 30pf

CHANGE TO:
C5030 33pf

NOTE: C5020 was shown twice, once on Diagram 4 grid location E2 and again on Diagram 5 grid location A4. It should only appear on Diagram 5 grid location A4. Change Diagram 4 as indicated above.

000-2775-00D

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MANUAL CHANGE INFORMATION

Date: 2-5-82 Change Reference: C4/282

Product: PM 106/107 PERSONALITY MODULE Manual Part No.: 070-3473-00

DESCRIPTION

TEXT CORRECTION

SECTION 6 MAINTENANCE AND TROUBLESHOOTING

page 6-4 2nd column under sentence which starts If the part number....

CHANGE TO:

1 PASS 1083-XX ; PM 106

1 PASS 1082-XX ; PM 107

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MANUAL CHANGE INFORMATION

Date: 4-1-82 Change Reference: C5/482

Product: PM 106/PM 107 PERSONALITY MODULE Manual Part No.: 070-3473-00

DESCRIPTION

TEXT CORRECTIONS

SECTION 3 SPECIFICATION

page 3-2 Table 3-1 partial

CHANGE AS SHOWN:

Minimum	READY line:	a)Setup: 80 ns min . prior to processor clock falling edge in machine state T4 or T3 b) Hold: 0 ns min. hold to clock falling edge in machine state T4 or T3.

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MANUAL CHANGE INFORMATION

Date: 12-2-81 Change Reference: M45158

Product: PM 106/PM 107 PERSONALITY MODULE Manual Part No.: 070-3473-00

DESCRIPTION

PARTS LIST AND SCHEMATIC CHANGES

EFF SN: PM 106 B010225 and up
PM 107 B010130 and up

CHANGE TO:

A01	670-6710-02	CKT BOARD ASSY:TOP (PM106 ONLY)
A01	670-7206-02	CKT BOARD ASSY:TOP (PM107 ONLY)
A02	670-6838-02	CKT BOARD ASSY:MIDDLE
A03	670-6711-01	CKT BOARD ASSY:BOTTOM
A01R4060	315-0821-00	RES.,FXD,CMPSN:820 OHM,5%,0.25W
A02R3010	315-0472-00	RES.,FXD,CMPSN:4.7K OHM,5%,0.25W
A02R4010	315-0202-00	RES.,FXD,CMPSN:2K OHM,5%,0.25W
A02U4010	156-0303-01	MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE
A03U5010	156-0321-02	MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE

A01R4060 is located on diagram 3

A02R3010, A02R4010, and A02U4010 are located on diagram 4

A03U5010 is located on diagram 6

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MANUAL CHANGE INFORMATION

Date: 2-23-83 Change Reference: M47559 REV

Product: PM 106/PM 107 PERSONALITY MODULE Manual Part No.: 070-3473-00

DESCRIPTION

PM 106 SN B010373 & UP
PM 107 SN B010186 & UP

PARTS AND DIAGRAM CHANGES

SECTION 7 REPLACEABLE ELECTRICAL PARTS

A02 670-6838-02

CHANGE TO:
A02 670-6838-03

A02C5030	283-0144-00	Cap, 33pf, 500V
A02C6030	283-0024-00	Cap, 0.1uf, 50V
A02C6031	283-0024-00	Cap, 0.1uf, 50V

CHANGE TO:

A02C5030	281-0819-00	Cap,33pf, 50V
A02C6030	283-0198-00	Cap,0.22uf, 50V
A02C6031	283-0198-00	Cap,0.22uf, 50V

A02C5030 is located on diagram 4 (refer to Manual Change Information C3/482). Grid location A4.

A02C6030 is located on diagram 5 grid location D4.

A02C6031 is located on diagram 5 grid location C4.

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MANUAL CHANGE INFORMATION

Date: 1-18-83 Change Reference: M44210

Product: PM106/PM107 PERSONALITY MODULE Manual Part No.: 070-3473-00

DESCRIPTION

PM 106 SN B010363 & UP

PM 107 SN B010176 & UP

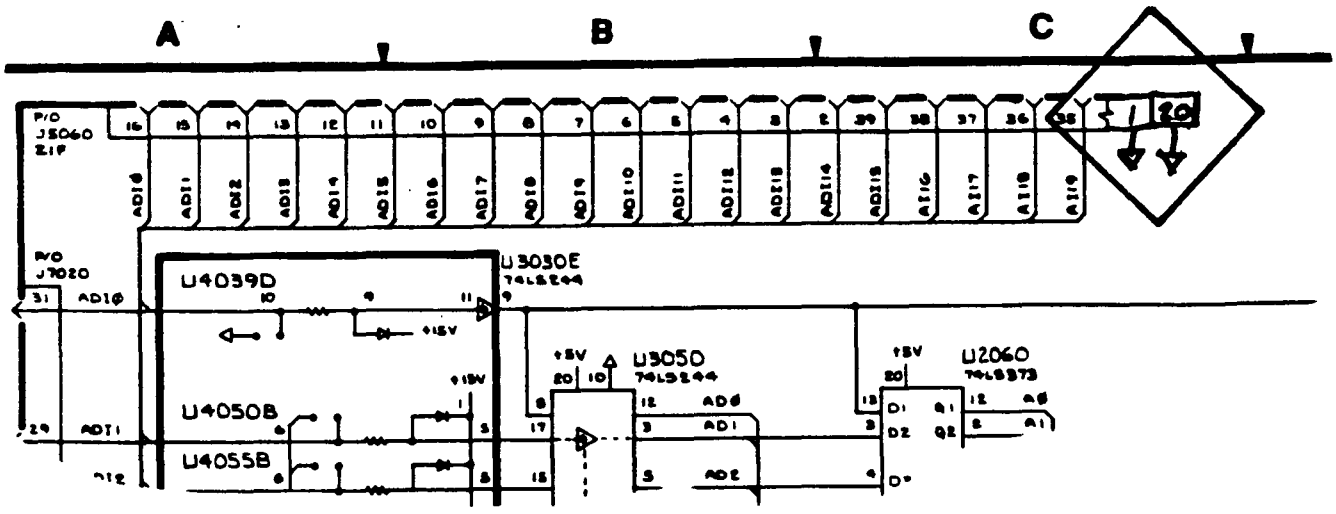
DIAGRAM CORRECTIONS

SECTION 8 DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Diagram 1
CHANGE AS SHOWN:

NOTE

THIS CHANGE FOR PM106 AND PM107 BOTH



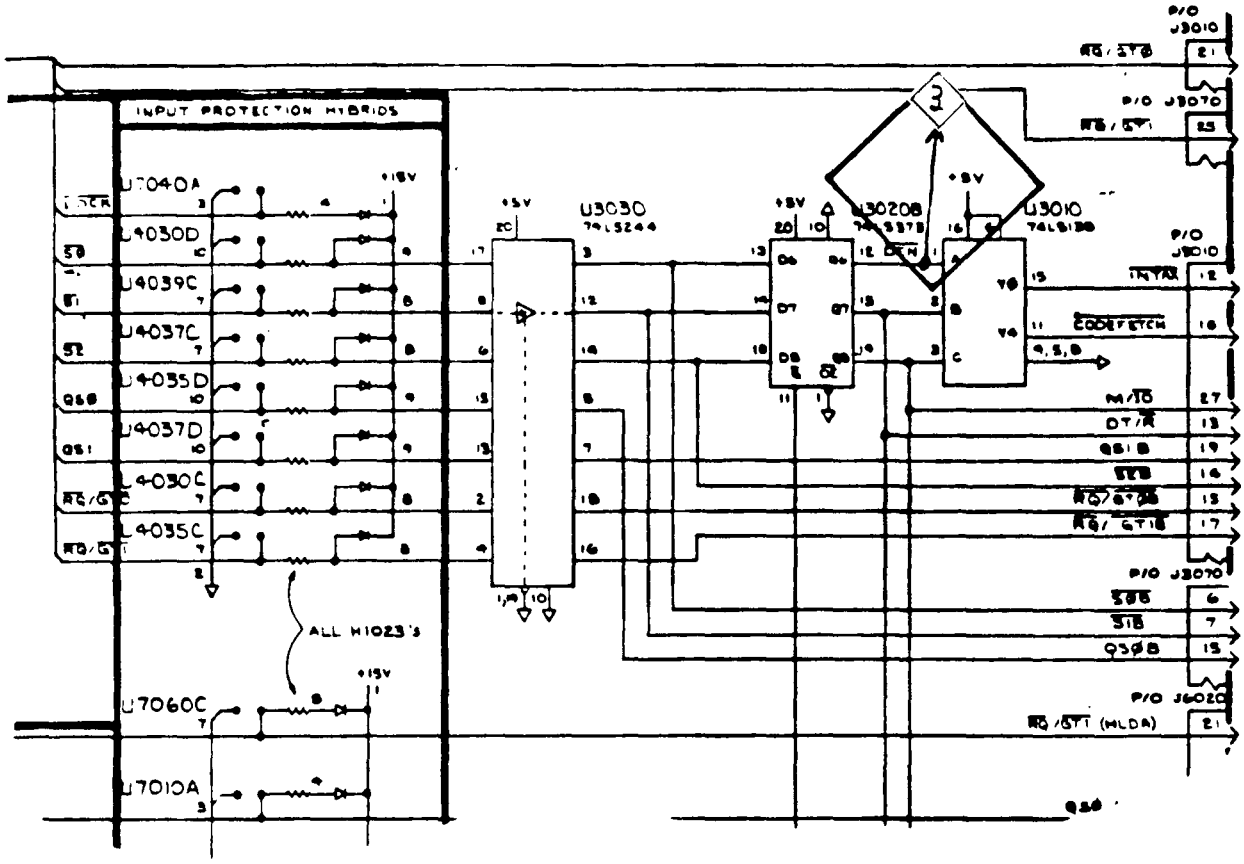
Product: PM106/PM107 Date: 1-18-83 Change Reference: M44210

DESCRIPTION

Diagram 2
CHANGE AS SHOWN:

NOTE

THIS CHANGE FOR PM107 ONLY

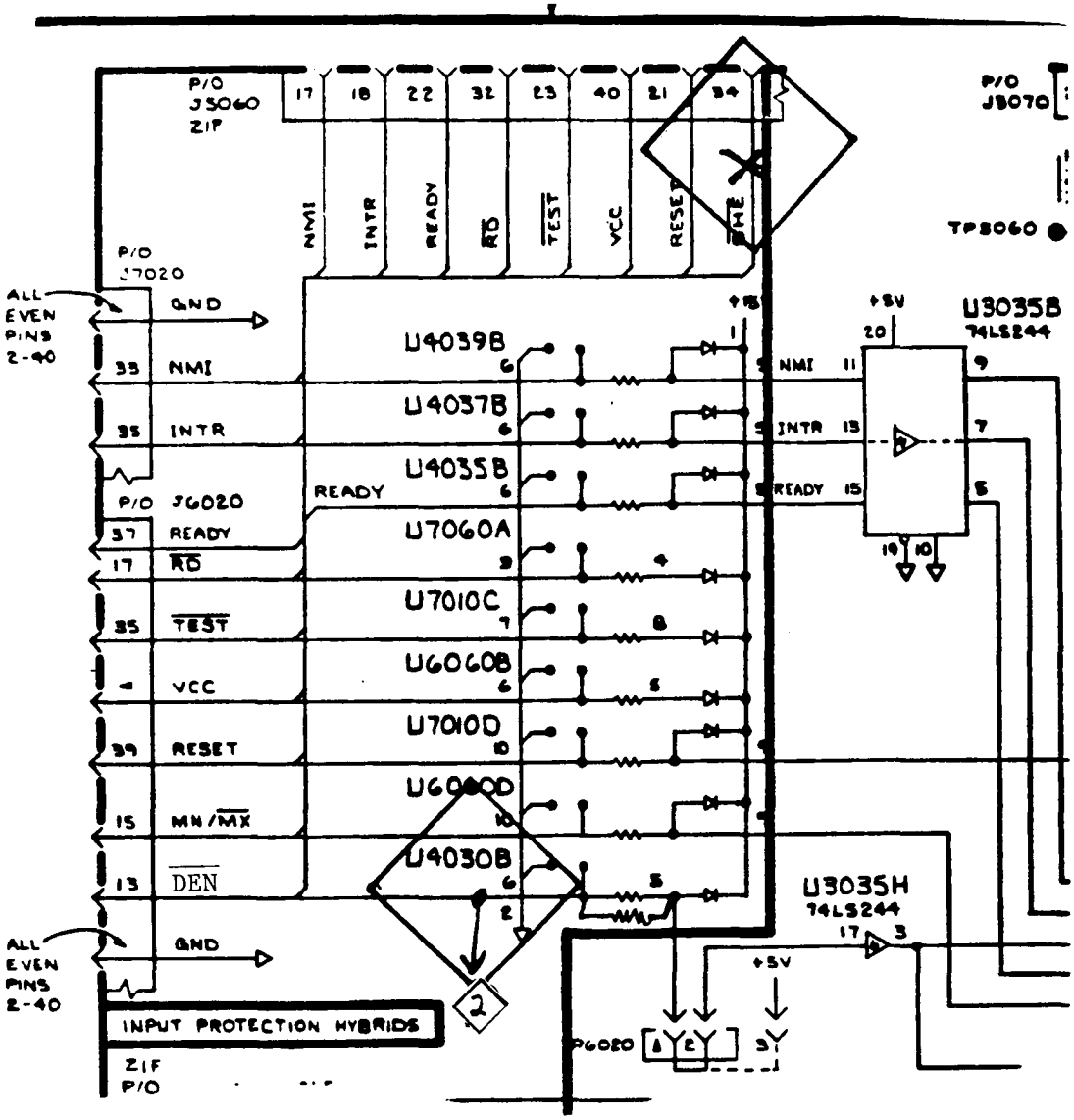


DESCRIPTION

Diagram 3
CHANGE AS SHOWN:

NOTE

THIS CHANGE FOR PM107 ONLY



Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: 12-1-82 Change Reference: C7/1282

Product: PM 106/PM 107 PERSONALITY MODULE Manual Part No.: 070-3473-00

DESCRIPTION

THIS IS A PAGE REPLACEMENT PACKAGE.

1. Remove the designated pages from your manual and insert the attached pages.
2. Keep this cover sheet in the Change Information section at the back of your manual for permanent record.

TEXT CHANGES

REMOVE THE FOLLOWING PAGES AND REPLACE THEM WITH THE ENCLOSED PAGES:

Pages 5-13 and 5-14

Test 4. $\overline{\text{HALT}}$ Function

Refer to the $\overline{\text{HALT}}$ Line Strapping Procedure in the Maintenance and Troubleshooting section to implement.

1. To clear all previous word recognizer selections, turn the mainframe power off, then on again.

2. Press the WD RECOGNIZER key.

3. Using the CURSOR control keys, move the cursor to the ADDRESS box and enter 72152.

4. Press the TRIGGER key.

5. Move the cursor to the SYSTEM UNDER TEST CONT. box and enter a 1 for SYSTEM UNDER TEST HALT.

6. Press the END key.

7. Connect a jumper strap from the PM 106/107 test point TP5060 (H) to the STF $\overline{\text{HALT}}$ test point TP5040.

8. Position P4050 on the STF to the $\overline{\text{PROG}}$ position.

9. Position P5050 on the STF to the MIN position.

10. Press the IMMEDIATE, GOTO, and 2 keys in sequence.

11. Press the cursor right arrow (→) key to move the cursor to the EXECUTE field.

12. Connect channel 1 of the test oscilloscope to J3010 pin 1, to observe the HOLDACK (C5 or C7) line. Trigger the oscilloscope on the falling edge of the waveform.

13. Check that the waveform has a low-going pulse duration of between 200 ms and 300 ms.

NOTE

Refer to ERROR 23, in the Maintenance and Troubleshooting section, for troubleshooting aid.

PERFORMANCE CHECK, PART III

Overview

The following test checks the setup and hold times for lines AD0 through AD16 (PM 106 only) and AD0 through AD7 (PM 107 only).

Preliminary Setup

1. Set the test oscilloscope as follows.

   a. HORIZONTAL TIME/DIV . . . 100 ns/div

   b. HORIZONTAL DELAY TIME/DIV . . . 100 ns/div

   c. MAG . . . vary as required

   d. TRIGGER . . . channel 4, + slope

2. Connect the test oscilloscope vertical as follows.

   a. Channel 1 . . . STF P5052-10 (labeled C: CLOCK)

   b. Channel 2 . . . STF P5052-8 (labeled 6: ALE)

   c. Channel 3 . . . PG 508 OUTPUT

   d. Channel 4 . . . PG 508 TRIG OUT

3. Set the PG 508 as follows.

   a. TRIG'D/GATED . . . + SLOPE

   b. MODE . . . as specified

   c. PERIOD . . . EXT TRIG OR MAN

   d. DELAY . . . 0.1 μs (vary as required)

e. DURATION . . . 0.1 μs (vary as required)

f. TRANSITION TIME . . . 5 ns

g. LEADING . . . ×1

h. TRAILING . . . ×1

i. OUTPUT (volts) . . . LOW LEVEL to 0 volts, HIGH LEVEL to +5 volts

4. Connect the PG 508 as follows.

a. TRIG/GATE IN . . . STF P5051-5 (labeled f)

b. Check PG 508 output level with multimeter before connecting.

c. Connect PG 508 output to AD0 through AD16 using the 40 pin adapter socket.

5. Set the STF jumpers as follows.

a. P3040 to P3050 pin 3 (change to +5 va)

b. P3050 . . . not used

c. P4040 . . . INT

d. P5045 . . . 0

e. P5050 . . . MIN

f. P5060 . . . present

6. Set the 7D02 as follows.

a. Clear all previous word recognizers by turning the mainframe power off, then on again.

b. Press the WD RECOGNIZER key.

c. Using the CURSOR control keys, move the cursor to the ADDRESS box and enter 0FFFF.

d. Press the TRIGGER and END keys.

Test 1. Setup and Hold

1. Procedure For Checking Setup Times

a. Set the PG 508 to DELAY MODE, duration variable (approximately 400 ns).

b. The falling edge of the ALE signal occurs at the end of machine state T1. Data is latched with the falling edge at the end of CLK in machine state T3.

c. Adjust the PG 508 delay for 30 ns prior to the falling edge at the end of CLK in machine state T3 (TTL level).

d. Press the START key.

e. Press 0 for an absolute listing.

f. Press the DATA SCROLLING up arrow (↑) to observe location 14 and location 15.

g. The data at location 14 (prior to the trigger) is FFFF for the PM 106 (or FF for the PM 107).

NOTE

Refer to ERROR 24, in the Maintenance and Troubleshooting section, for troubleshooting aid.

2. Procedure for Checking Hold Times

a. Set the PG 508 to UNDLY MODE, duration variable for the falling edge of the output waveform coincident with the falling edge at the end of CLK in machine state T3 (TTL level).

b. Press the START key.

c. The data at location 15 is FFFF for the PM 106 (or FF for the PM 107).

NOTE

Refer to ERROR 24, in the Maintenance and Troubleshooting section, for troubleshooting aid.

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MANUAL CHANGE INFORMATION

Date: 6-30-82 Change Reference: C6/682

Product: PM 106/PM 107 PERSONALITY MODULE Manual Part No.: 070-3473-00

DESCRIPTION

TEXT CORRECTIONS

SECTION 5 PERFORMANCE CHECK

page 5-8 Fig. 5-3B items 125 through 128 under DATA

CHANGE TO:
XXXXXXXX

page 5-12 Fig. 5-7B all items under LOC

CHANGE AS SHOWN:

LOC
T
016
017
018
019
020
021
022
023
024
025
026
027
028
029
030
031
032
033

DESCRIPTION

page 5-13 1st column

DELETE:

steps 10 & 11

ADD TO STEP 12:
Trigger in NORM mode and press START/STOP repeatedly.

Renumber steps 12 & 13 as 10 & 11