Margaret Pedersen 94.461

REV A

PART NUMBER 155-0082-00

| REV | REF | DESCRIPTION OF CHANGE | CHK BY | DATE |
|---|---|---|---|---|
| OR | | Initial Documentation. | | 1-24-72 |
| A | | Major format revision (16 pages) per ECN # 2876. | Leventhal | 4-30-79 |

Linda Berg 5/3/79
Writer Originator

Tektronix, Inc. H126 155-0082-00



THE DRAWING TYPE DESIGNATION AND APPROVED SOURCES OF SUPPLY FOR THIS ITEM ARE LISTED ON THE PURCHASED ITEM SOURCE LIST (PISL) FOR THIS PART NUMBER.

TEKTRONIX, INC.
P. O. BOX 500
BEAVERTON, OREGON U.S.A. 97077

| | | | |
|---|---|---|---|
| DWN/ WR | | DIMENSIONS ARE IN INCHES / MM<br>TOLERANCES: UNLESS OTHERWISE SPECIFIED | |
| COMP ENGR | | DEC | ANLR |
| CHKR/ COORD | | SCALE | FIRST USED ON |
| INSTR DSGN | | | |

MATERIAL

FINISH

TITLE: Vertical Output Amplifier

| | | CODE IDENT NO | SIZE | PART NUMBER | REV |
|---|---|---|---|---|---|
| | SH 1 OF 16 | 80009 | A | 155-0082-00 | A |

000-7242-00 D

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## 1.0 DESCRIPTION

The H126 is a Monolithic Integrated Circuit/Transistor Hybrid. It was designed specifically as a Vertical Deflection Plate Driver in the 475 Portable Oscilloscope. The Bandwidth required by this instrument is DC to 200 MHz.

### 1.1 Features

200 MHz -3 dB Instrument Bandwidth.

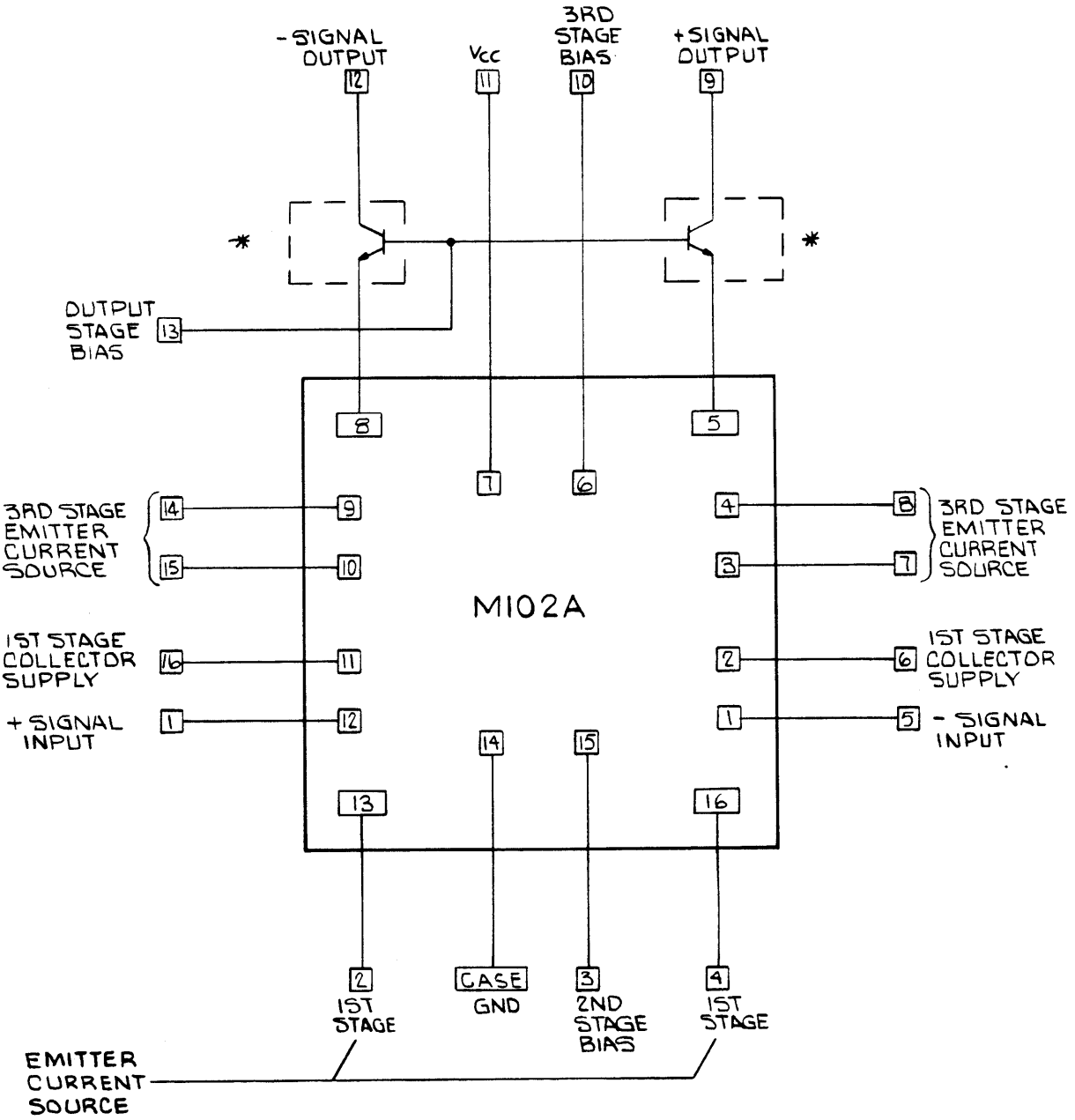
Discrete Transistor Outputs.

Cascode "$f_T$" Doubler Circuit.

## 2.0 ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Dissipation ($P_D$) | 4.9 watts |
| Voltage, Pin 15 to Ground | +15.0 Volts |
| Voltage, Pins 9 & 12 | +55.0 Volts |
| Total Current, into Pins 9 & 12 | 160.0 mA |
| Storage Temperature Range ($T_{STG}$) | -55°C to +125°C |
| Range ($T_A$) | -15°C to +70°C |

## 3.0 SCHEMATIC DIAGRAM

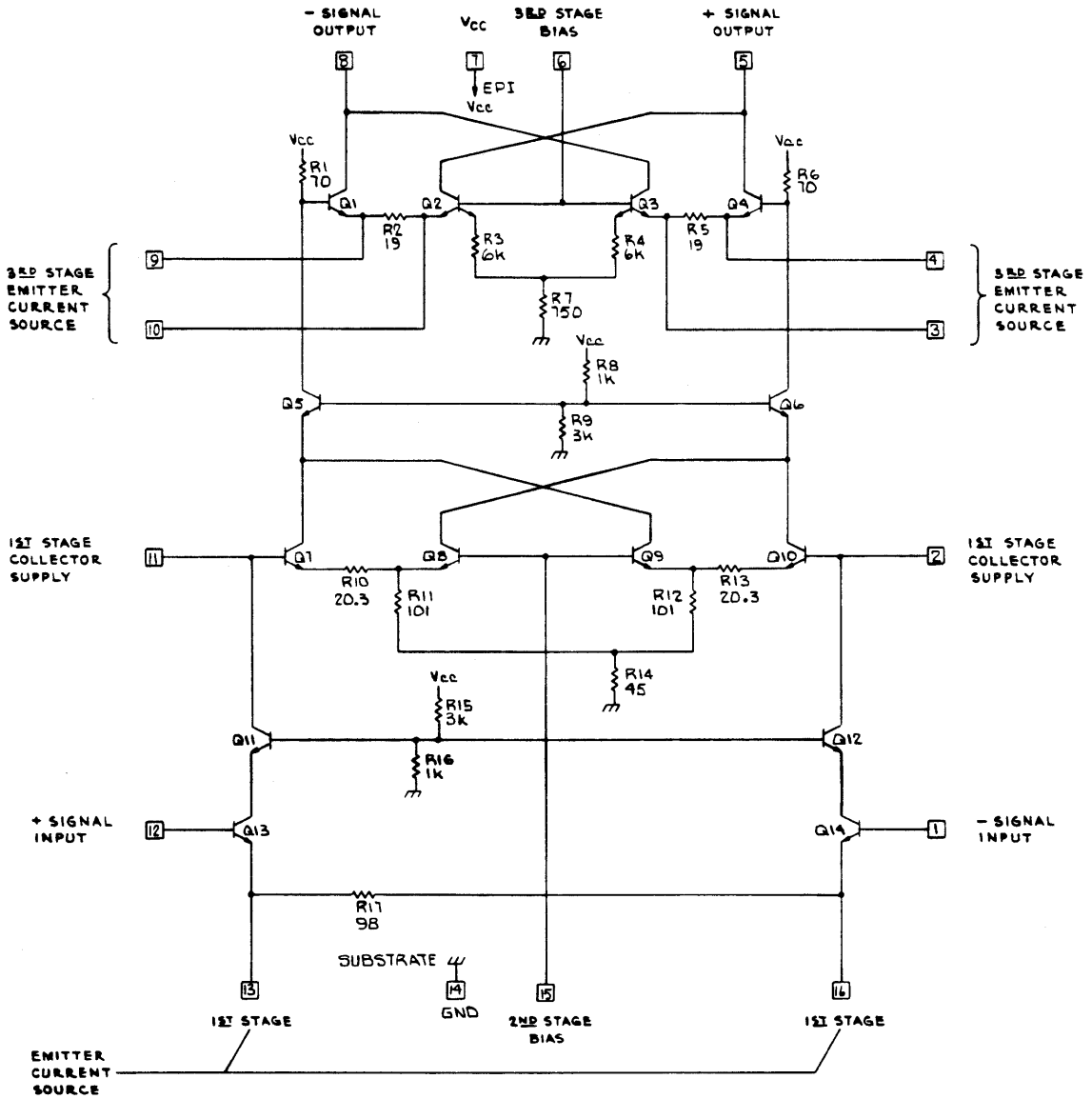



* 153-0637-00
SELECTABLE TRANSISTORS

See ICM-0-194 - Table I for options available. See "Applications Information" section of this spec for general comments.

3.0 SCHEMATIC DIAGRAM (continued) *

M102A




*Refer to 203-0102-XX component specification for IC details. Refer to "Applications Information" section of this spec for general comments.

## 3.1 Layout Drawing

Refer to Bonding Diagram ICM-39-204.

## 4.0 PARAMETRIC DEFINITIONS

### 4.1 Gain

Total DC current Gain of circuit: $\frac{I_{Pin\ 12} + I_{Pin\ 9}}{I_{Pin\ 1} + I_{Pin\ 5}}$

DC current out over DC current in.

### 4.2 Compression

Gain compression or linearity expressed as maximum percentage of total amplitude.

### 4.3 Balance

Output offset voltage with inputs grounded.

### 4.4 Risetime

10% to 90% of leading edge trace measured at the output in response to an input step function.

### 4.5 Aberrations

Front corner deviations of amplitude from steady state reference usually above 90% point of leading edge (i.e. deviations from an ideal flat step square wave at the output in response to an ideal step input forcing function. Time frame is in the 20 ns range).

### 4.6 Position Effect

Percentage change in front corner aberration amplitude from trace mid-screen CRT position to maximum top or bottom screen deflection.

### 4.7 Thermals

Front corner deviations similar to "aberrations" above but in a 10 µs to 1 ms time frame. Called "thermals" because the effect has been shown to be related to thermal time constants. This effect and its compensation with external resistors is directly affected by the accuracy at the final stage 19 ohm emitter resistors.

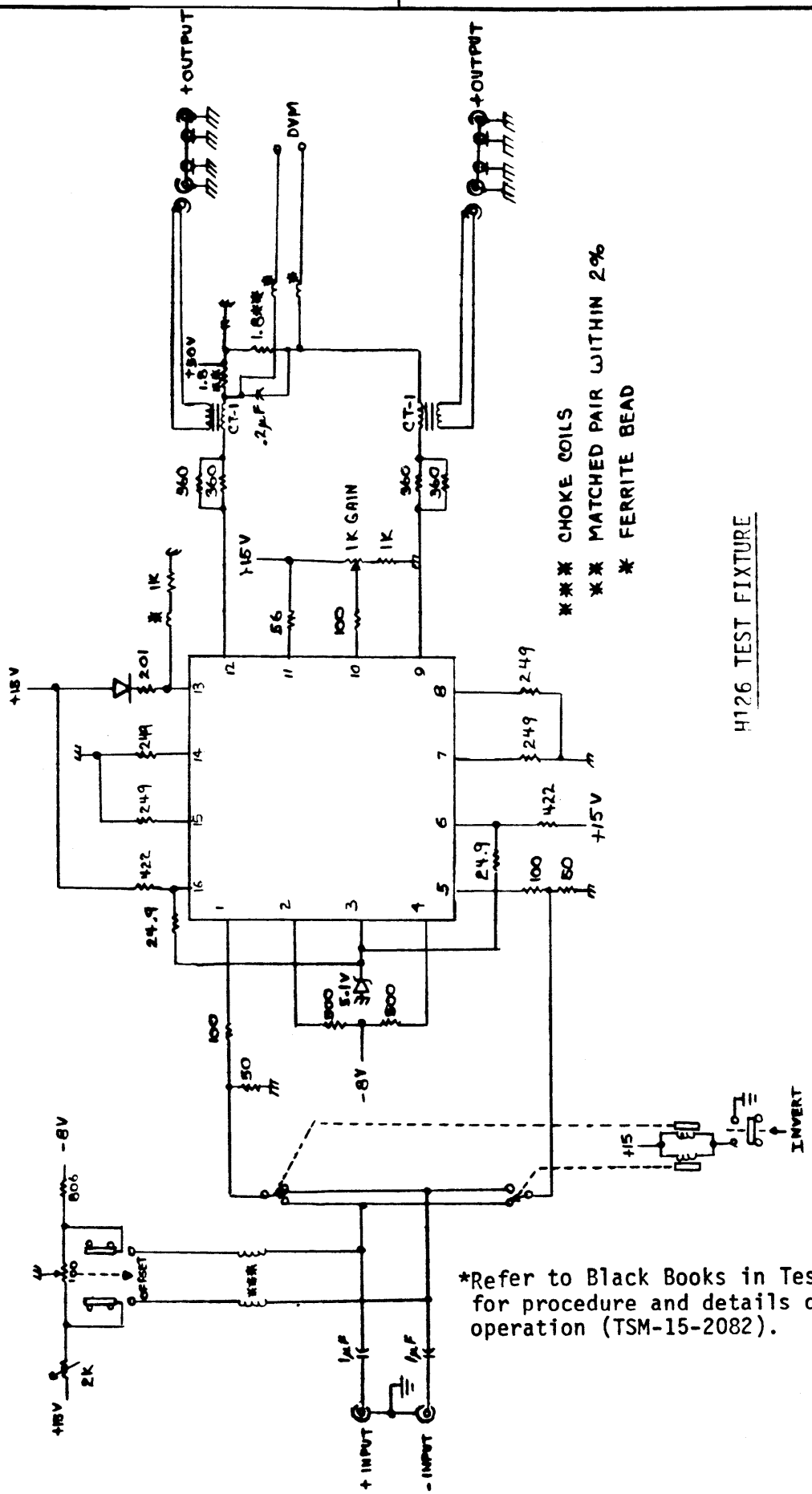
## 4.8 Beam Find Effect

At present no adequate spec has been formulated to specify this behavior which can be affected by device parameters. However, the beam find circuit used in the 7704A is recommended as being nearly independant of device parameters and free of troublesome behavior. The "beam find effect" evidences itself as a small offset in the vertical position which is erratic in magnitude, direction, and occurance after the beam is positioned in the beam find mode and released.

## 5.0 PARAMETRIC SUMMARY

| NO. | PARAMETER | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| 1 | Gain | 14.0 | 20.1 | |
| 2 | Balance | -23.0 | +23.0 | mV |
| 3 | Compression | -5.0 | +5.0 | % |
| 4 | Risetime | | 1.06 | ns |
| 5 | Aberrations | -3.0 | +3.0 | % |
| 6 | Position Effect | -8.0 | +8.0 | % |
| 7 | Thermals | -3.0 | +3.0 | % |
| 8 | Beam Find Effect | See Parametric Definitions Section | | |

NOTE: Refer to Test Fixture Schematic on next page and TSM-15-2082.




| TEKTRONIX, INC. BEAVERTON, OREGON | SHT 8 OF 16 | CODE IDENT NO 80009 | SIZE A | PART NUMBER 155-0082-00 | REV A |
|---|---|---|---|---|---|

000-7243-00D

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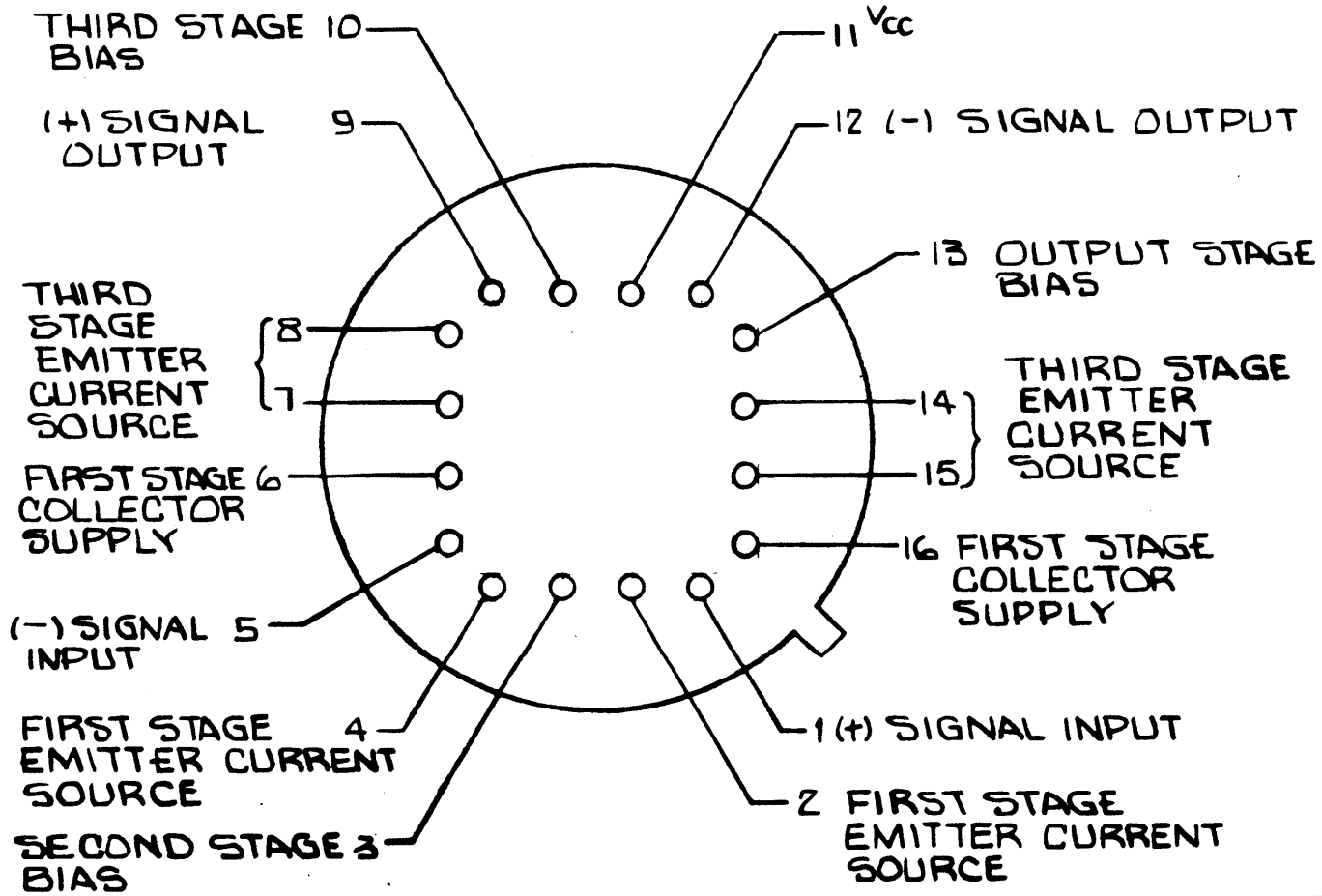
## 6.0 PACKAGING

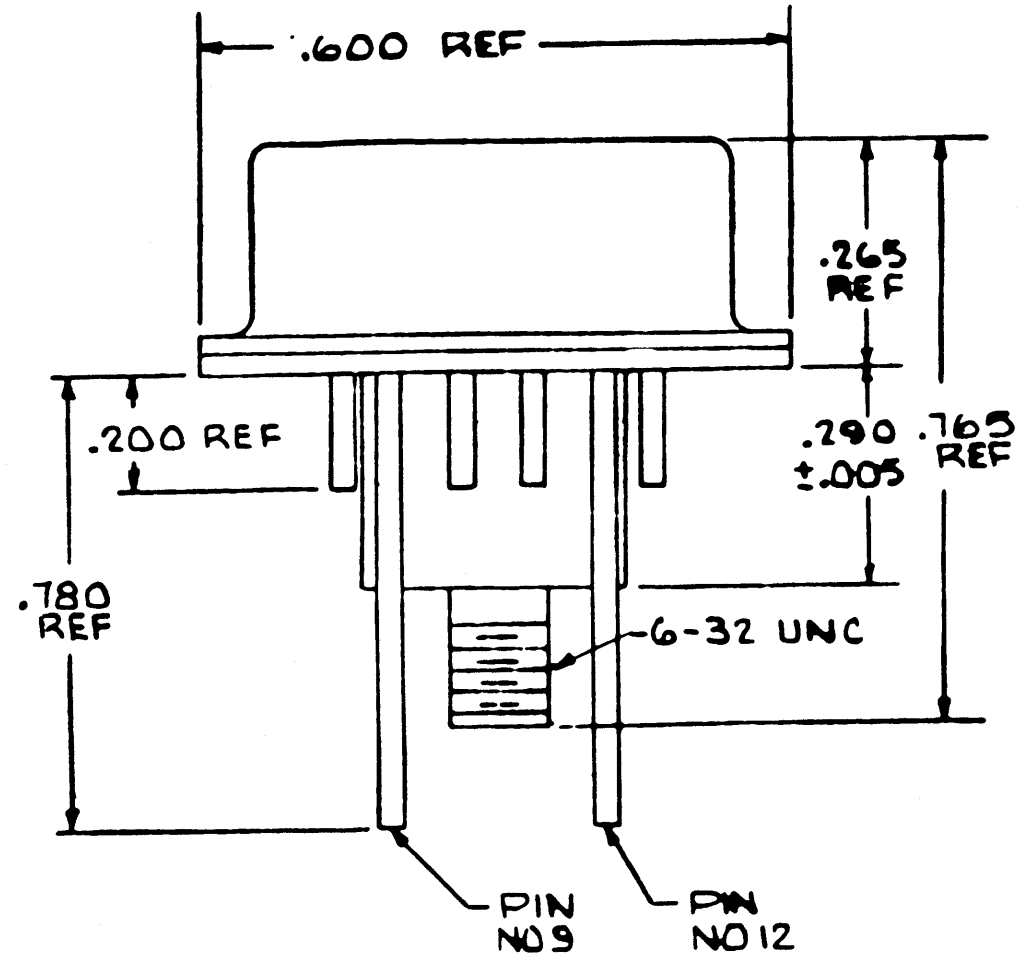
### 6.1 Terminal Identification

| Pin | Function |
|---|---|
| 1 | Input |
| 2 | Bias |
| 3 | Bias |
| 4 | Bias |
| 5 | Input |
| 6 | Bias |
| 7 | Bias |
| 8 | Bias |
| 9 | Output |
| 10 | Bias |
| 11 | Bias |
| 12 | Output |
| 13 | Bias |
| 14 | Bias |
| 15 | Bias |
| 16 | Bias |

Substrate connected to case



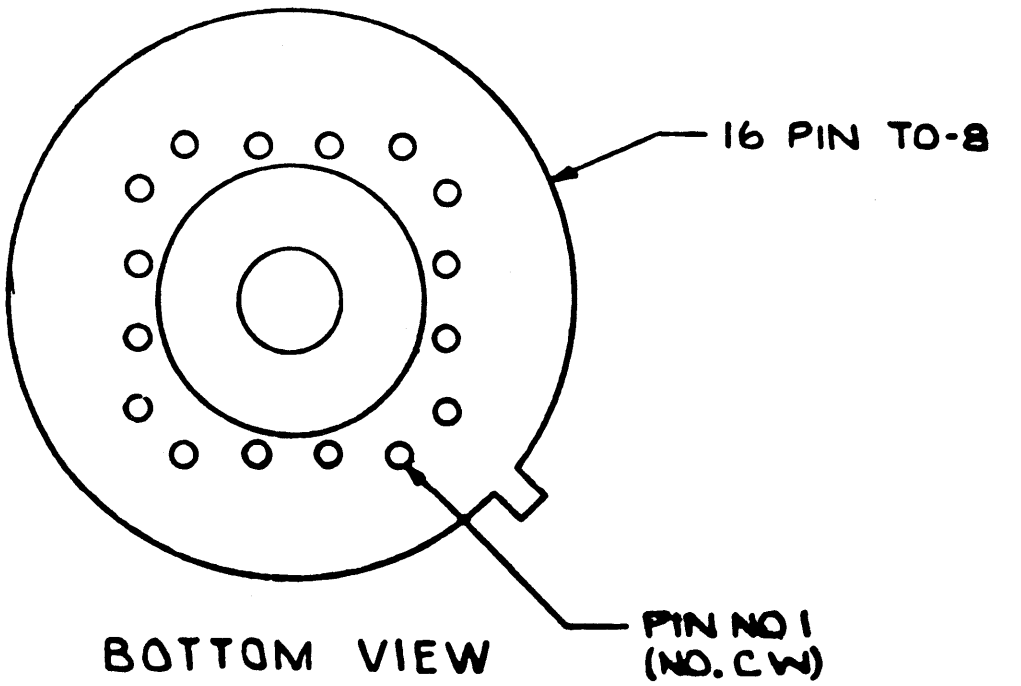
6.2 Outline Drawing (For Mechanical Reference only)




PACKAGE DESCRIPTION

Package Material:
16 Pin, TO-8 Large Pattern
W/Brazed-on
Stud and BeO Substrate
Gold Electro-Plated

See ICM-49-204 for marking information.




| TEKTRONIX, INC. BEAVERTON, OREGON | SHT 10 OF 16 | CODE IDENT NO 80009 | SIZE A | PART NUMBER 155-0082-00 | REV A |
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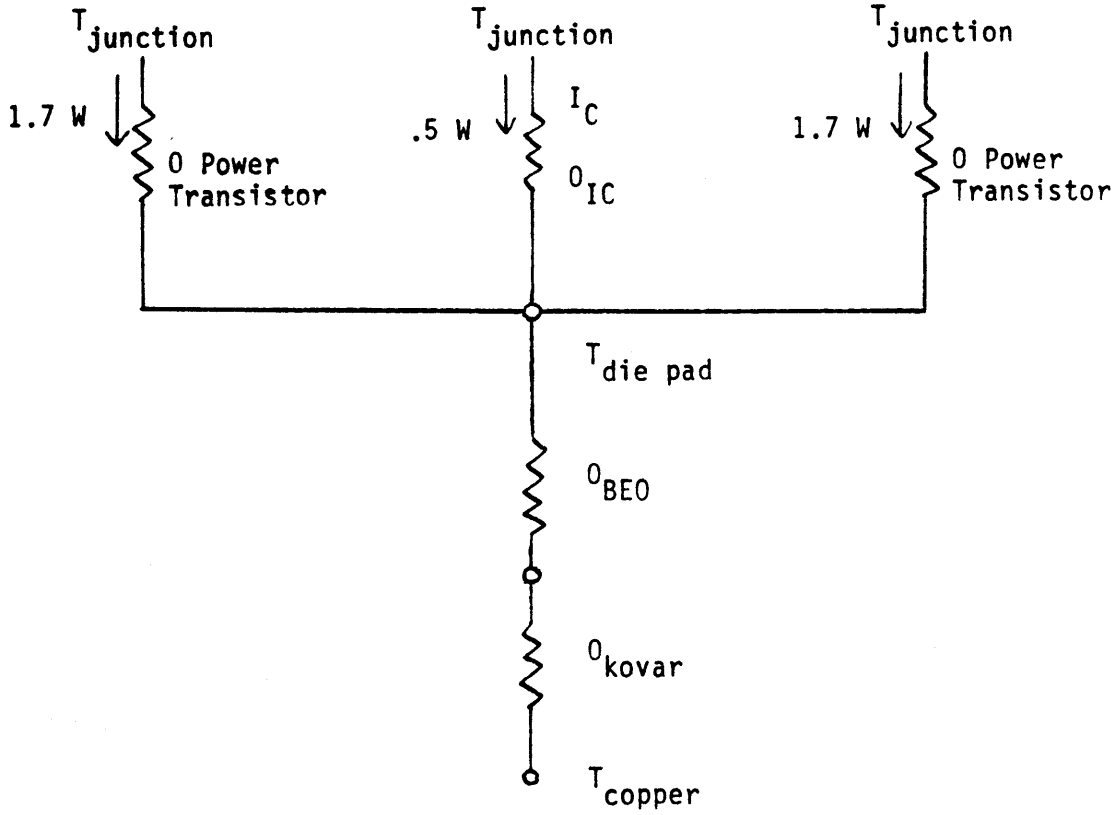
## 6.3 Thermal Characteristics




$\theta_{\text{power transistor}}$ = from 30°C/W to 50°C/W depending on device and die bond (measured).

$O_{BEO}$ = 2°C/W (calculated)

$O_{kovar}$ = 1.8°C/W (calculated)

$T_j - T_{cu} = \begin{cases} 30 * 1.7\ W + (3.8 * 3.9\ W) \\ 50 * 1.7\ W \end{cases}$

$\Longrightarrow$ $\boxed{66^{\circ}C \leq T_j - T_{cu} \leq 100^{\circ}C}$

## 7.0 RELIABILITY STATEMENT

### Reliability Goal

$\lambda$, Failure Rate $\leq$ 1%/1K hours at 158°C Tj.
$\lambda$, Failure Rate $\leq$ 0.002%/1K hours at 75°C Tj.
MTTF $\geq$ 100K hours at 158°C Tj.
Expected instrument life, 10,000 hours.

## 8.0 APPLICATIONS INFORMATION

### 8.1 M102 Monolithic Vertical Amplifier Die

This die is a high frequency monolithic 3 stage integrated current gain amplifier circuit. The circuit is differential input-differential output in a cascode arrangement known as the "$f_t$ multiplier circuit". It is designed to be driven from a balanced 50 ohm source. The die is fabricated from the SHF-II or "Super-Hi Two" process with nichrome resistors on the topside. Die from this process are targeted from data at manual probe thru a computer predictive program for this and similar hybrids. $F_t$ on this chip is about 600 Mhz.

### 8.2 Output Amplifier Die

Four sources of output transistor die are qualified for this product. This includes the Tektronix D156 and D58 fabricated with the SHF-II process. The other sources are the Motorola 2N3866 in chip form and the CTCE1-28. When the specifications on these devices are met a single chip is used as an output driver on each side of the differential output. However, since assuring an adequate supply of output die has been difficult, ICM has resorted to the practice of using two die per side bonded in parallel. Since one die is adequate to carry the power load, matching is not a problem with a 30% to 70% match being quite adequate. Breakdowns on these devices are 55 volts $BV_{CBO}$, $f_t$'s are 500 MHz, and Betas are supposed to hold up out to 200 mA failry well.

### 8.3 Substrate

The substrate is BeO with a layer of tungsten and then a layer of glass-frit gold in the die bonding areas. These metal layers are brazed on.

## 8.4 Package

As can be seen from Section 6.2, this copper heat studed, BeO substrate in a TO-8 can is designed for maximum heat transfer capabilities. The power dissipation rating of about 5 watts over the instrument ambient conditions required such careful thermal design. Production parts are sample burned-in, or 100% power burned-in if necessary, in order to meet reliability goals. The stud and substrate are brazed together with the header.

## 8.5 Characterization

Contact Technical Product Management in ICM for further information on this part. As characterization activities are completed they will be thoroughly documented. In the interim the responsible product engineer will be your best source of information on this hybrid.

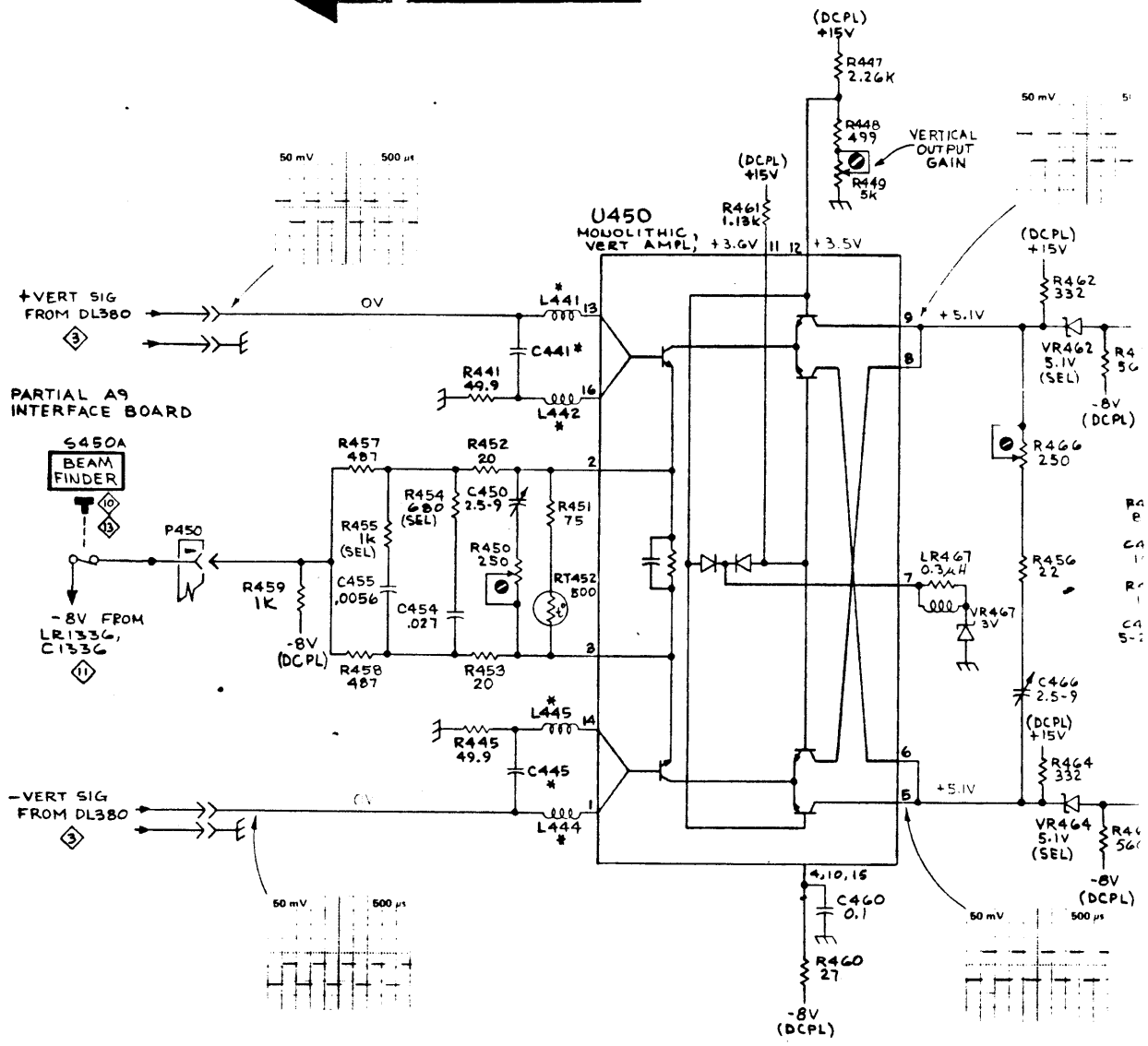
## 8.6 Typical Applications

See following pages.

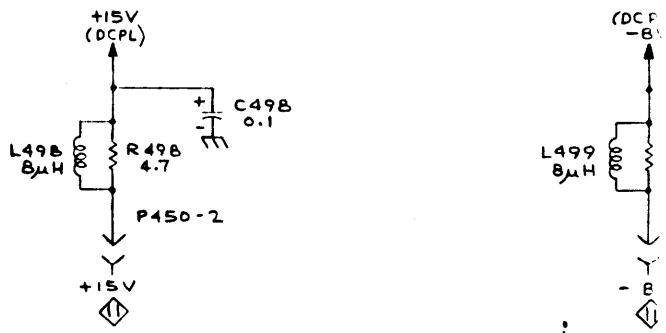
## 9.0 REFERENCE LIST

| | |
|---|---|
| 151-0498-00 | 3866 transistor die |
| 153-0638-00 | Selectable transistors |
| 155-0168-00 | Similar vertical output amplifier |
| 203-0102-90 | Monolithic vertical amplifier |
| 204-0565-90 | D58 transistor die |
| 204-0707-00 | D156 transistor die |
| ICM-0-194 | Selection table for output |
| ICM-39-204 | Bonding Diagram |
| ICM-49-204 | Marking Diagram |
| ICM-50-0082 | Top Assembly Drawing |
| TSM-15-2082 | Final test procedure |

## VOLTAGE & WAVEFORM CONDITIONS




* PART OF ETCHED CIRCUIT BOARD




REV. A, OCT. 1975

475 OSCILLOSCOPE

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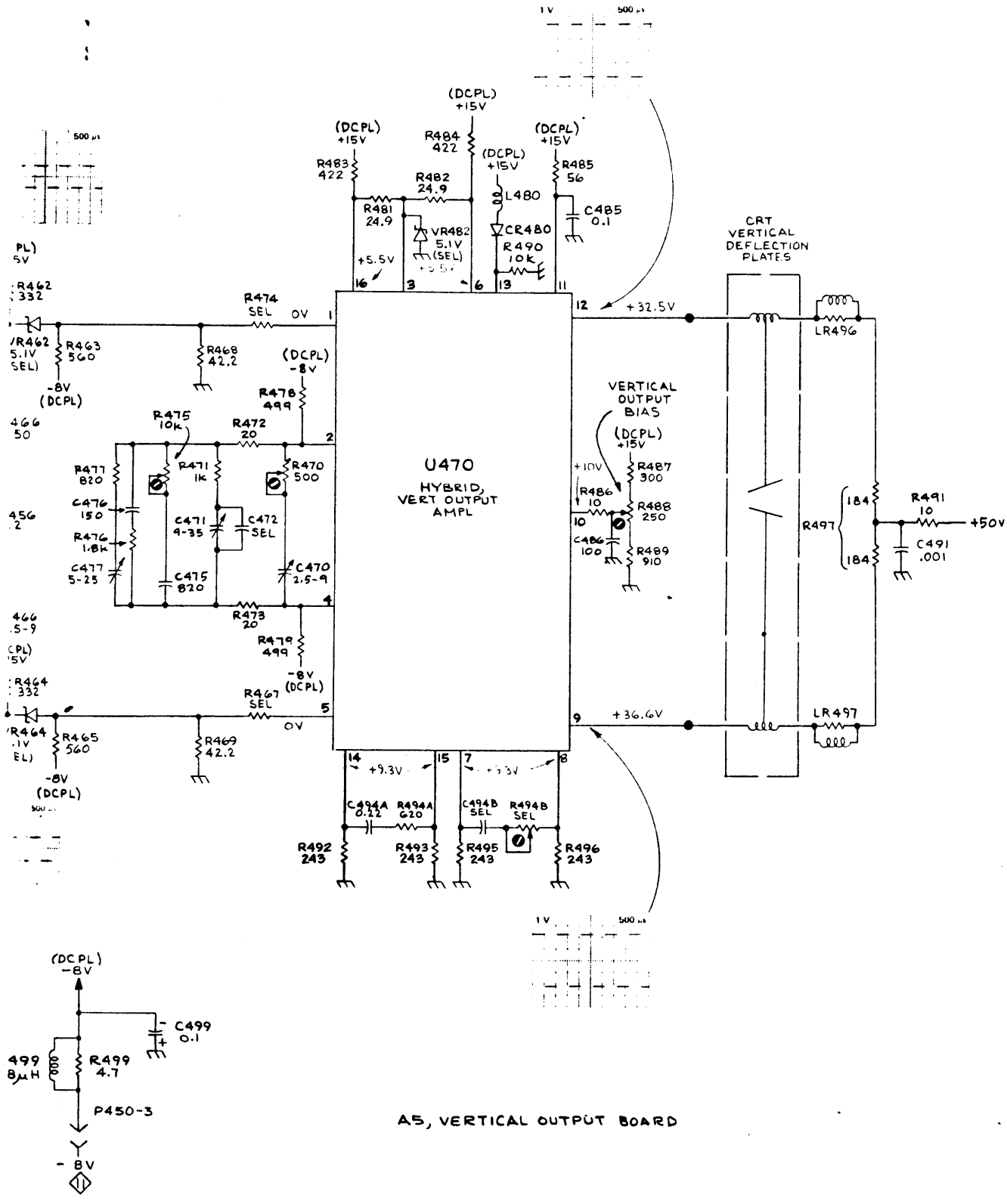


A5, VERTICAL OUTPUT BOARD

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SN B250000 - UP

## VERTICAL OUTPUT AMPLIFIER ④

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