component news

Sept 21, 1978 COMPANY CONFIDENTIAL Issue 263

16K RAM process evaluation

Component Engineering is performing a detailed process evaluation on 16K dynamic random access memories (RAMs). These devices are critical to the overall performance of many of our products, and are used at Tek in ever-increasing quantities. In systems where a large number of RAMs are used, the system failure rate is largely dependent on this device's failure rate – necessitating more precise characterization.

Dynamic RAM manufacturers typically use their most advanced MOS circuit designs and fabrication techniques in producing the 16K chips. Because the competition within the semiconductor industry is especially fierce in producing this part, manufacturers are reluctant to supply Tektronix with much processing and design information. Therefore, our evaluation activities have concentrated on specific techniques that can be applied to the parts purchased by Tek, alleviating our dependence on vendor-supplied test structures and information.

Although the electrical specifications of 16K RAMs may be the same for different manufacturers, the fabrication techniques can be radically different. These differences in fabrication affect the performance of the device in many ways – distribution of specified characteristics, limits outside the specifications that the part can tolerate, and performance in areas not specified, such as reliability.

Not only are fabrication techniques important, but the manufacturer's ability to control these processing techniques also impacts the quality of the device. Therefore, the need to periodically monitor processing techniques was also considered when devising the process evaluation program which follows.

evaluation techniques

Semiconductor manufacturers usually have test structures directly on their wafers to evaluate processing parameters. Unfortunately, these test patterns are not available on 16K dynamic RAMs, and other testing techniques need to be used.

Techniques which were found to be useful include: (1) electrically probing the chips, (2) analysis on a scanning electron microscope (SEM), and (3) computer simulation of circuits on the chips.

electrical probe

Using a high-quality probe station, electrical measurements can be made of transistor characteristics and breakdown voltages on the chips. In addition, capacitance of cell capacitors, diffusion resistance and capacitance, and some of the internal clock pulses can be measured.

An example of measured cell capacitance is illustrated in Figure 1. Oxide capacitance measurements can indicate the quality of the silicon dioxide (SiO_2) and the silicon dioxide-to-silicon interface. It is also useful for measuring (1) oxide thickness, (2) doping levels near the silicon surface, (3) lifetime of the minority carriers at the surface, (4) surface states, and (5) mobile ion impurities in the oxide layer.

continued on page 2

also in this issue

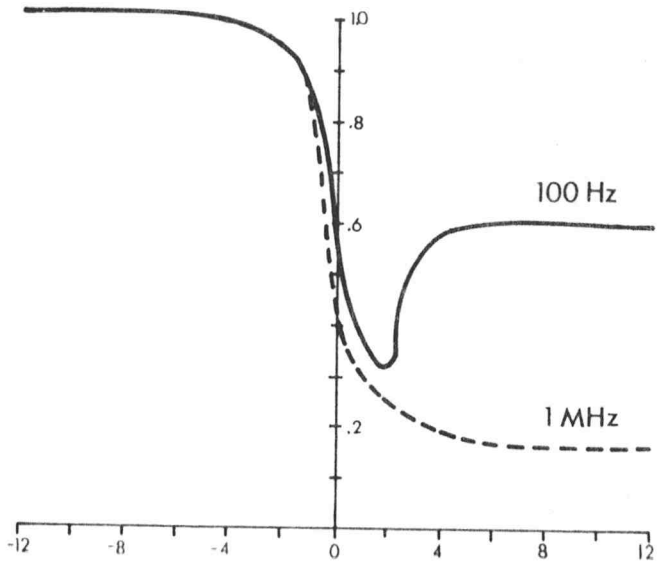

Figure 1 — Cell capacitance versus applied voltage for MOSTEK chip

Measurements of some internal clocks have been made using a probe with a ≈2pF, 100MΩ input impedance. The probe can cause loading problems on some clocks on the chip. However, we can measure the clocks which operate the sense amp circuit. These measurements are illustrated in Figure 2A, with a schematic of the sense amplifier shown in Figure 2B.

The sense amp is a very critical circuit on the chip — required to detect a few tenths of a volt difference on the bit lines in 10 to 20 nS. Unfortunately, the actual voltages on the bit line and parts internal to the sense amp cannot be measured with the probe. Therefore, we simulate these responses with computer models using measured driving clocks.

scanning electron microscope measurements

The SEM is useful for identifying the circuit layout and the accurate dimensions needed for computer modeling. The SEM is also an excellent tool for process analysis, by analyzing cleaved sections and by chemical analysis using an X-ray attachment.

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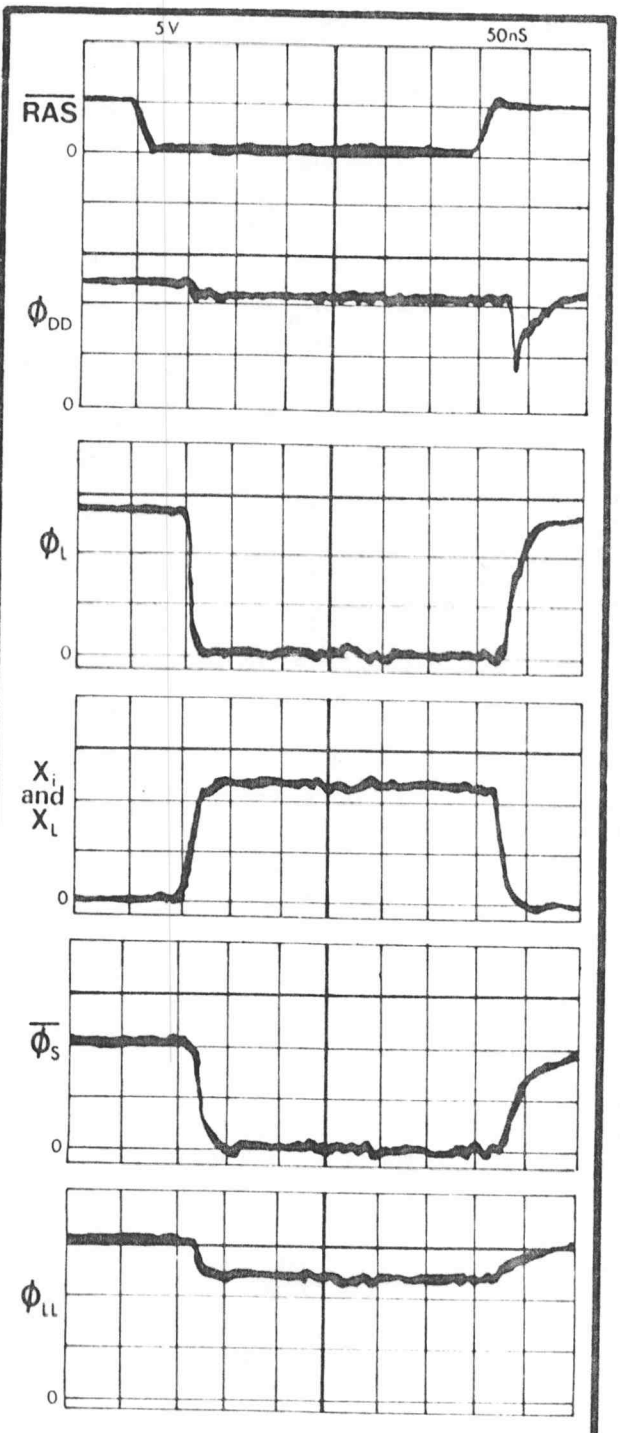


Figure 2A — Some internal clocks on chip generated by $\overline{RAS}$ signal, used to operate sense amp.

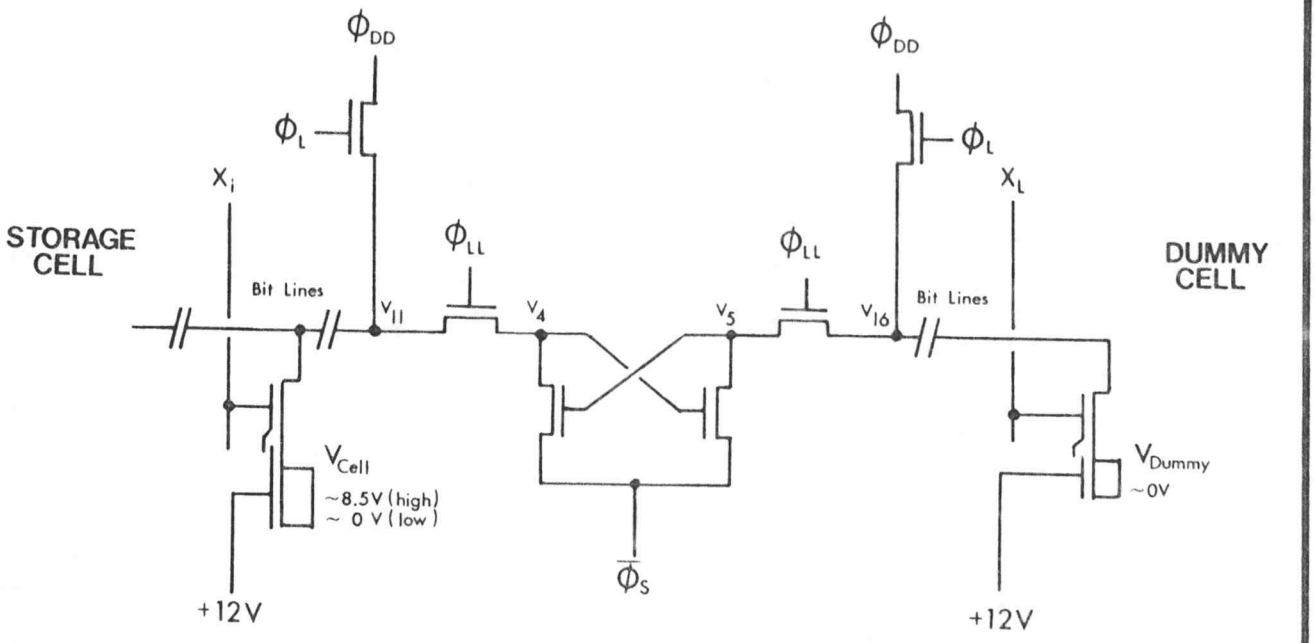
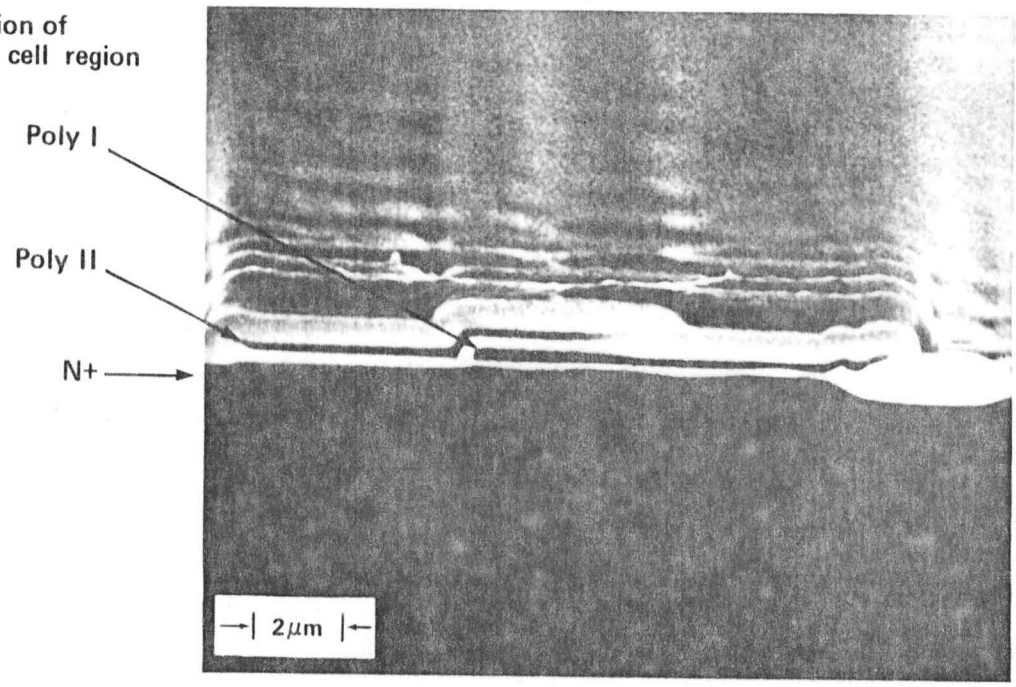


Figure 2B – Sense Amplifier circuits and clocks used to operate the circuit.

A cleaved section of the MOSTEK cell and access transistor is depicted in Figure 3. Prior to SEM analysis the cleaved section was etched in a silicon etch, which increased the contrast between silicon (dark) and oxide (light) layers by creating a charge buildup on the oxides. This technique can be used to reveal oxide and polysilicon thicknesses, diffusion depth, metallization thickness, and some of the techniques used in producing the chip. The difference between oxides grown or deposited on the polysilicon can be seen. Likewise, reflow glasses become very apparent.

continued on page 4

Figure 3 – Cross-section of MOSTEK cell region



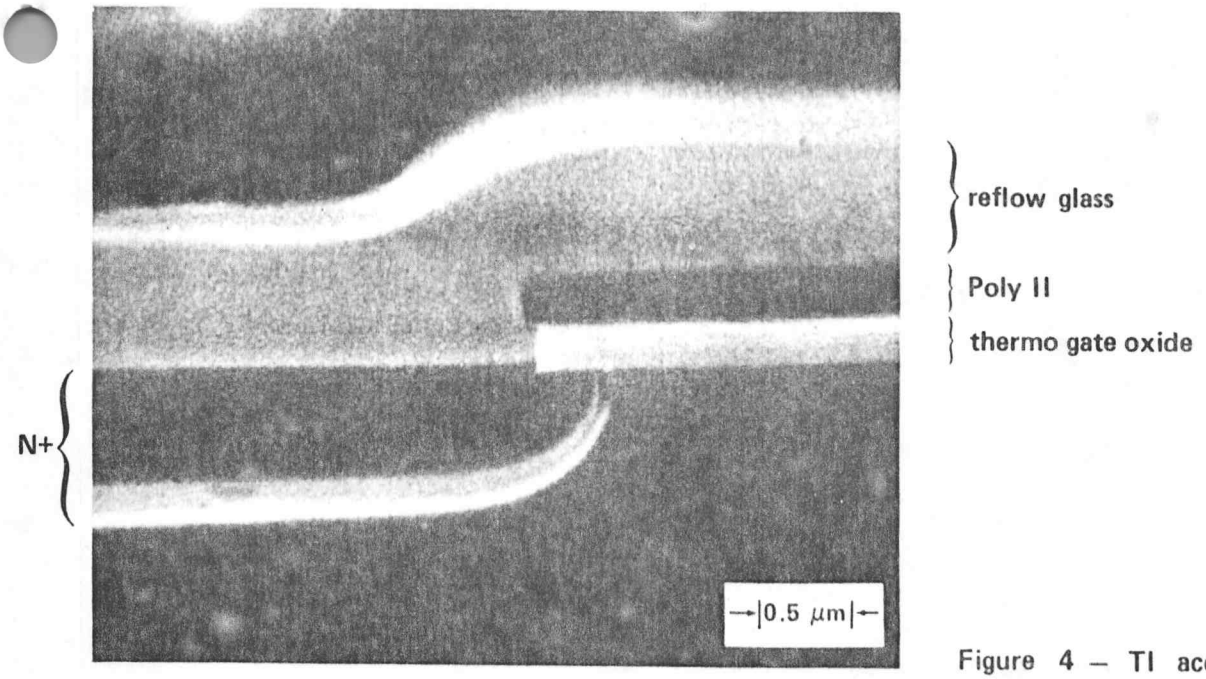


Figure 4 – TI access transistor

Figure 4 shows a chip made by TI which uses reflow glass deposition to improve aluminum step coverage. Unlike MOSTEK, which grows a thermo-oxide (≈1000-2000Å) on the second polysilicon layer after diffusion, TI has deposited reflow glass on top of very thin thermo-oxide material. TI's method is questionable because this lower quality glass must withstand about 20 volts with a thickness of only 800Å in certain places on the circuit.

The reflow glass of TI is also in contact with the aluminum metallization. Phosphorus in the reflow glass can react with this aluminum if moisture is present, etching the aluminum layer. This condition could cause serious reliability problems for the device. This would be expected to be more serious for plastic packages.

computer modeling

Some circuits in 16K dynamic RAMs cannot be probed without disrupting the operation of the device. One such circuit is the sense amplifier shown in Figure 2B. Here, the bit lines are balanced so that loads of approximately 0.02 pF will alter the circuit operation.

To understand the design features of this critical circuit, computer modeling techniques are used, with the driving voltages obtained from measured values. Results of the simulation of this circuit are shown in Figure 5A, where the measured values (Figure 2) have been approximated by piece-wise linear curves, with compensation given to loading from probe during these measurements (Figure 5B).

continued on page 5

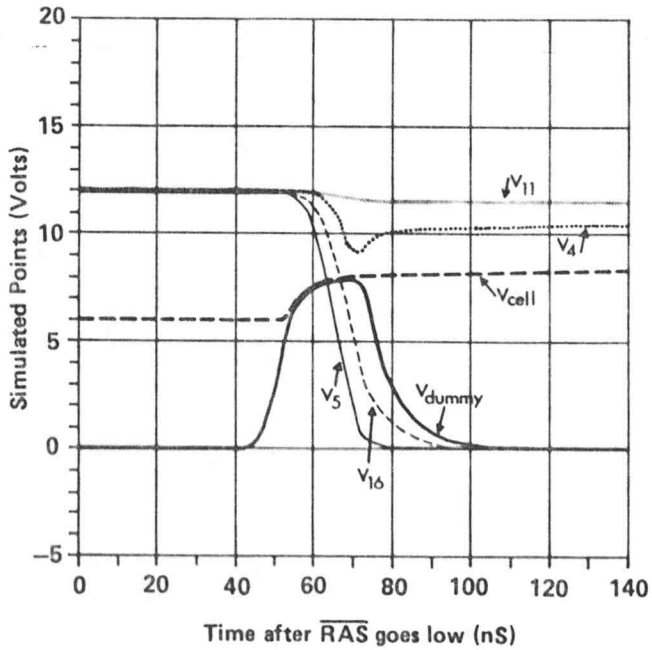


Figure 5A – Simulated voltages on sense amp

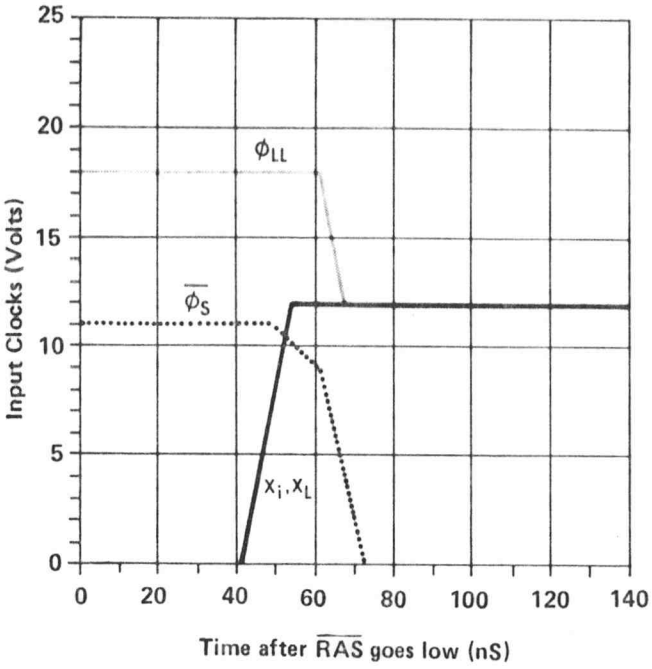


Figure 5B — Driving voltages for sense amp

Modeling techniques have provided insight into critical circuits on 16Ks, and are also expected to be very valuable in evaluating 64K dynamic RAMs. Samples of the 64K RAMs should be available in 1979.

more information

If you'd like to know more about Component Engineering's evaluation and characterization of 16K dynamic RAMs, contact **Ron Burghard or Eric Peterson (58-299), ext. 6302.**

Because there are several changes and corrections in the Component/Engineer listing, we are running an update on page 15.

Berg PV receptacles modified

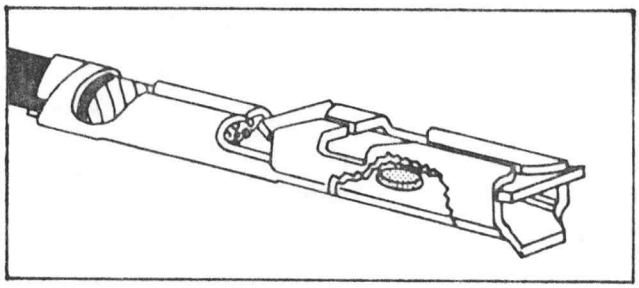
Crimp reliability problems have been encountered with the Berg Maxi-PV receptacle. The problems have become more pronounced due to a change in the body material from gold-plated brass to a selective gold copper/nickel alloy.

Because this copper/nickel alloy is more sensitive to crimp height variations, stock is being switched to the gold-plated version. Therefore, until Berg establishes crimp height specs for individual wire sizes, **all** copper/nickel selective gold Maxi-PV receptacles should be rejected and sent to **Bob Thorpe (70-588)** for stock exchange. The following three part numbers are affected:

131-0621-00
131-0622-00
131-0792-00

New parts (overall gold-plated) should be requisitioned to replace the rejected receptacles. The copper/nickel parts can be identified by vendor number 75694-001 through 75694-009, or by an overall silver color. The gold-plated brass parts have an overall gold finish.

In addition to this, more detailed inspection and QC procedures have been instituted in Wire Prep to assure better reliability of production crimps. Better control of crimping machines outside Wire Prep is also being considered.



If you have questions concerning this change, contact **Peter Butler (ext. 5417) or Emerson Beer (ext. 5034).**

8085/8085A microprocessor comparison

Intel has shipped Tek several versions of their 8085/8085A microprocessor (Tek P/N 156-1088-00). Some of these devices have problems which need to be recognized.

The following list shows the unique markings on the packages, and the problems that some versions exhibit:

Part	Spec number		Comments
8085	S2608	TAL=70nS	These parts will not execute an opcode correctly when hold is high. Trap destroys the 'EI' flag.
	S2609	TAL=90nS	
8085	S2632	TAL=70nS	No hold problem. Trap destroys the 'EI' flag.
8085	S2631	TAL=90nS	
8085A	S2629	TAL=90nS	These parts have a power up reset problem (see comparison, below).
8085A	S2630	TAL=70nS	
8085A	No S number		These are the latest parts with the problems corrected.

8085 vs. 8085A

8085

- ALE is generated during bus idle states of the DAD instruction, falsely indicating a bus cycle. Applies only to DAD instruction.

  Does not apply to BI states generated by RST, HALT or INTR.

- Internal interrupts cause a bus idle state which has identical status to regular bus states.

  IO/M = 0
  Si = 1
  So = 1

  t_{INS} = 360nS min from the falling edge.

  Users affected: ALL

- ALE floats during RESET, HALT & HOLD. Coming out of the float state causes false trailing edge.

- Trap interrupt resets the interrupt enable status, making it difficult to know what the previous state was.

8085A

- ALE is not generated during bus idle states for DAD instruction (i.e. Inhibit ALE during M_2 & M_3 of DAD).

  Large Systems (using dynamic memories)

- Change IO/M status during INA so that INA cycle will have a Unique status.

  IO/M = 1
  Si = 1
  So = 1

  Sample all interrupts one cycle earlier

  t_{INS} = 680nS min

- ALE does not float during RESET, HALT & HOLD. ALE is never tri-stated.

- Have TRAP latch the previous status until after next RIM, which restores regular operation.

  (Thus, keep Interrupt Enable status prior to last Interrupt/Trap in RIM byte. TRAP input will still clear Interrupt Enable. RIM must follow TRAP routine to restore Interrupt Enable Flag.)

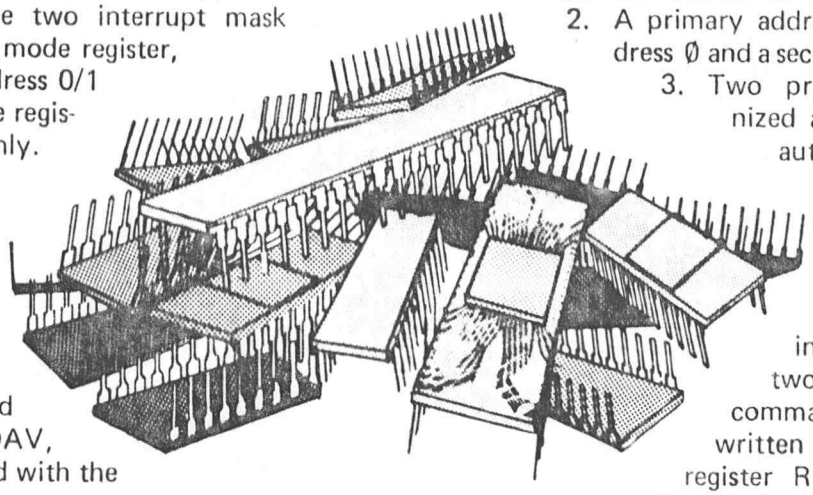
This information was supplied to Tektronix by Intel. They have agreed to replace all 8085 or 8085A parts which have S numbers stamped on their top.

To work out the details on how to get replacement parts, please contact **Wilton Hart (58-125), ext. 7607.**

Intel 8291 GPIB chip

Early samples of the Intel 8291 GPIB* chip have been evaluated in Component Engineering. With two exceptions, the device seems to conform to IEEE 488 (1975), as well as being free of major "user traps."

A programming model of the 8291 is shown in Figure 1 (page 9). There are 16 directly addressed registers, eight read and eight write; with three other write registers indirectly addressed via register five write (R5W). After power up, it is necessary to write to the two interrupt mask registers, the address mode register, and twice to the address 0/1 register, because these registers power up randomly.



The design is entirely random logic with the exception of the timing of the delay between the placing of data on the bus and the assertion of DAV, which is synchronized with the CLK input.

interrupt structure

There are 12 readable bits of interrupt status which are capable of generating an IRQ.

These bits are first stored in a master register and then transferred to a slave register, which is the readable register. The interrupt mask bits are ANDed with the contents of the slave register, with these resultants ORed to generate the INT bit, which is the same as the INT pin. Transfer from master to slave is inhibited any time the INT bit is true. Interrupts after the first are allowed to pile up in the master register until the first is serviced, then they are transferred to the slave.

Interrupt status bits are cleared by reading the register in which they are contained. The 'BI' and 'BO' interrupts are also cleared by reading from or writing to the data I/O register Ø.

This structure seems to guarantee that there will be no lost interrupt status bits, and that overlapping interrupts will generate interrupt requests.

addressing modes

There are five address modes in this device. Two are the 'and listen-only' modes, to be used with the controller function. The other three modes are:

1. Two primary addresses are recognized, which are stored in address Ø and 1.
2. A primary address is stored in address Ø and a secondary in address 1.
3. Two primaries are recognized as in mode 1, with automatic hold off of data accepted for secondary command group messages, with generation of the APT interrupt. One of the two handshake release commands must be written to the AUX MODE register R5W to release the handshake.

data in

When an active listener, the Acceptor Handshake (AH) function is allowed to proceed automatically one full cycle on the first data byte received. Assuming that the μP doesn't get around to reading the data-in register in time, the AH function will be held in Accept Data State (ACDS) for the second data byte until the first byte is read from register Ø. Therefore, there can be one accepted but unread byte in the data-in register, and one new unaccepted byte already valid on the bus. In this way, there can be some overlap between a talker and the 8291 as a listener.

function of EOI in Talker Active State

EOI is asserted in Source Transfer State (STRS), which is the state in the source handshake where DAV is asserted. We have told Intel that we feel that EOI should be asserted in both Source Delay State (SDYS) and STRS, which are the states in the source handshake where data is

*General Purpose Interface Bus

continued on page 8

allowed to settle on the bus and then held unchanging. Intel has verbally agreed to make this change.

There are two ways of generating the END message. One is through the 'feoi' command to reg. 5; the other is through the use of the EOS register, where EOI is asserted on a coincidence of the data byte with the contents of the EOS register.

When transferring the ASCII data, the usual choice for generating EOI will be via a compare with the EOS register. When transferring binary data, it is necessary to use the 'feoi' command. It has been found, however, that there is a problem with the 'feoi' command, under conditions of taking control synchronously, that the command is not cleared when the output data stream is aborted by the controller. It is possible that the first character sent after an abort will have EOI asserted if 'feoi' preceded the abort.

A way around this is to enable the EOI on EOS sent feature just prior to the last character in a data stream, and disabling the feature for all other characters. Intel has stated that the device will be modified so that a pending 'feoi' is aborted when entering Talker Idle State (TIDS), just as are data bytes.

response to EOI in Listener Active State

Asserting EOI for any amount of time at any point in the handshake will generate an 'END' interrupt. However, the EOI bit in the address status register 4 is set only when the EOI line is asserted during a window of time following the assertion of DAV. This response will be modified so that the 'END' interrupt status bit will be set each time EOI is detected true when the AH function enters ACDS.

If the RFD/DAV Holdoff on END bit is set (bit A1), and EOI is true, then the AH function will either remain in ANRS or will halt the next time it enters ANRS.

response to Group Execute Trig

When the device is in Listener Active State and the 'GET' command is on the bus, the TRIG pin will produce a one- to two-microsecond pulse within 800 nS following the assertion of DAV.

the AUX MODE register

The AUX MODE register allows the instrument μP to issue commands to the 8291, to preset the number of clock cycles of delay for DAV, to configure or unconfigure for parallel poll, and to write to auxiliary registers 'A' and 'B' (see Figure 1).

major problems with the 8291

There are two bugs in the present design. One has to do with Serial Poll; the other deals with the process of aborting an output data stream.

The 8291 will, under certain circumstances, transmit a dummy character after having been serial polled. The reason is that the 'new byte available' (nba) local message is true while the device is in Serial Poll Active State, and remains true on existing SPAS, and unless the 8291 re-enters Talker Idle State, the 'nba' message will be true when the device next enters Talker Active State.

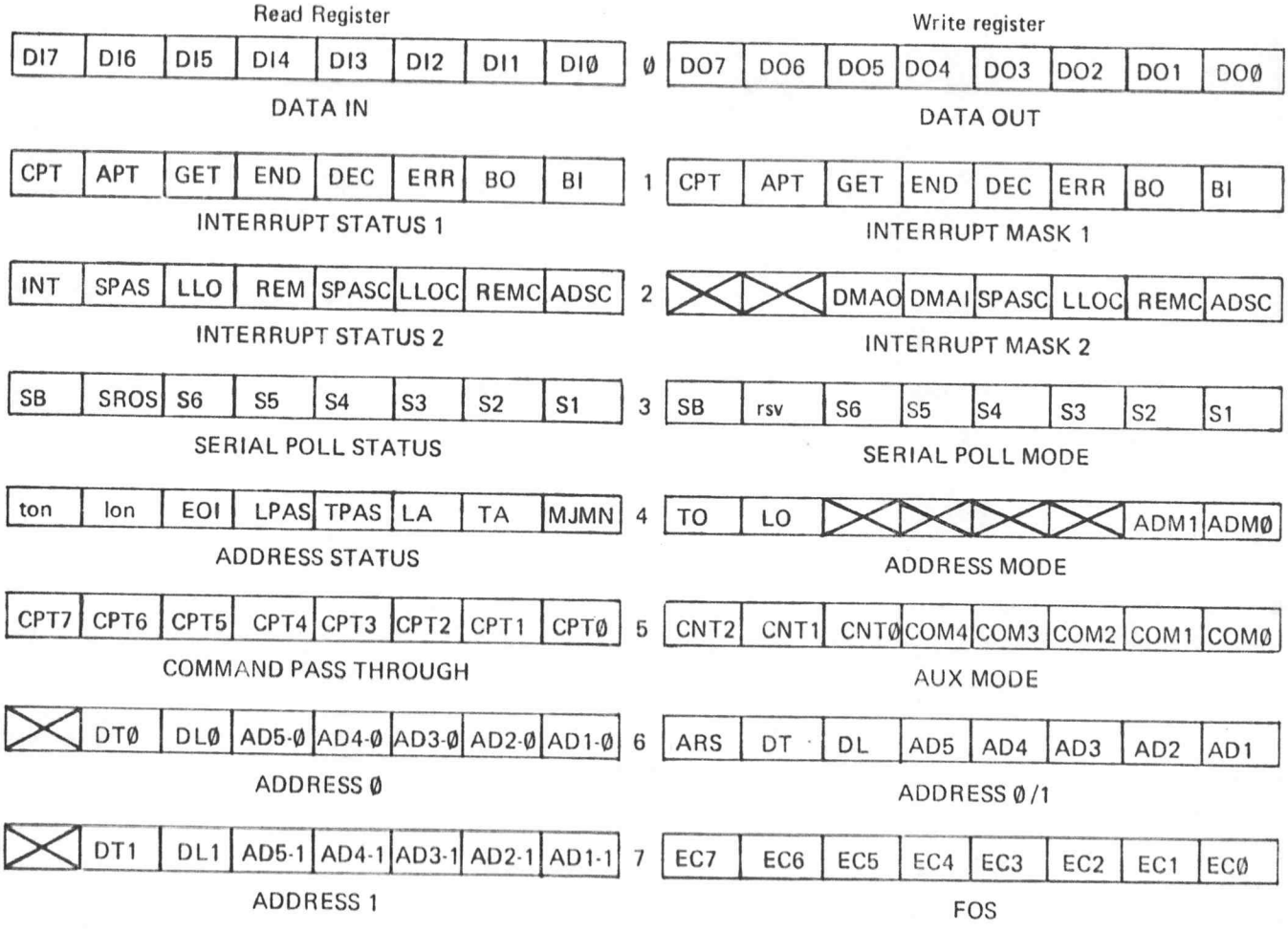
If the 8291, as it now stands, is used in a GPIB system with a 4051 controller, there will be no problem because the 4051 issues the UNT message to terminate the Serial Poll sequence. There may be problems, however, with other GPIB controllers on the market.

The facility for aborting an output data stream has several problems which must be corrected if we are to use the device. The first is this: if the instrument μP has written a byte to the output data register, and subsequently the GPIB controller takes control of the bus to terminate the current process, the next time the 8291 is made a talker there will no 'BO' interrupt generated.

The other problem is similar to the problem that the 68488 has with Serial Poll (see **Component News 262**, page 20). It is possible with the 8291 that a data-out byte can be aborted without the instrument μP being made aware of the loss. The reason is that the 8291 automatically aborts output data on entering Talker Idle State, then lets the μP decide whether to continue the old data stream or start a new one on re-entering Talker Active State. Unless the μP monitors the 'Addressed State Change' interrupt bit, there is a possibility that the loss of the data byte will go unnoticed.

text continued on page 10

Figure 1 – 8291 Registers



AUXILIARY REGISTERS (via AUX MODE) (reg-5-write)

CNT2	CNT1	CNT0
1	0	0
1	0	1
0	1	1

8-bit EOS COMPARE	EOI on EOS sent	END on EOS rcv'd	RFD/ DAV hlde	RFD/ DAV hlda

'A' Register

	INT Sense	HIGH SPEED	EOI in SPAS	UCPT

'B' Register

U	S	P_3	P_2	P_1

Parallel Poll Configure

good features of the 8291

The 'ADSC' bit, bit Ø R2R, will cause an interrupt when entering or exiting Talker Active or Listener Active states, making unnecessary the polling of the address status register.

The 'EOI' bit, bit 5 R4R, indicates that the last data byte brought in was the valid end-of-string. This bit is only set if the EOI line was true during a window of time following DAV, or if there was match with the EOS register if that feature is enabled. This means that the 'END' interrupt status bit may be ignored if desired.

The data in register is a true 1 byte buffer. This should allow higher data transfer rates than other implementations. The device has shown itself to be capable of 500K byte/sec transfer rates and may be capable of full 1M byte/sec.

Because of the way in which interrupt status bits are stored until read, there are few reasons for holding up the bus while the instrument μP determines the cause of an interrupt.

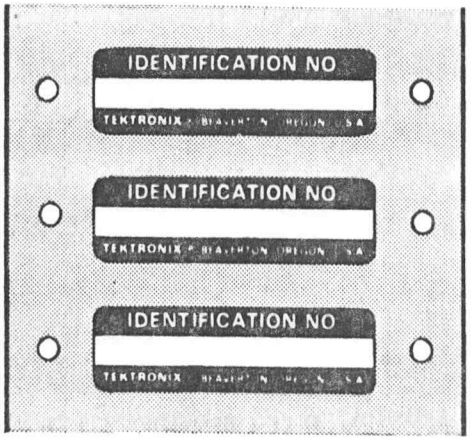
Assuming that the bugs can be ironed out, the 8291 has the capability of aborting output data streams by clearing the data-out register upon entering TIDS. With this feature, the instrument μP may either continue the old data stream or start a new stream, with no time constraint on the decision.

more information

For more details on the 8291, contact **Jim Howe (58-125), ext. 6303.**

Identification tags will drop pin-feed liner

The identification tags shown below are currently being supplied to Tek on a pin-feed liner. The vendor has notified me that the die for this process is wearing out and needs to be replaced.



As far as I have found, no areas use these tags on a machine requiring this special liner. Most areas choose to use a typewriter instead.

Therefore, I would like to have the tags supplied to us *without* the pin-feed liner, which is very expensive.

Please contact me as soon as possible if there are any objections to removing this liner.

Sharon Webb
(58-274), ext. 7912

Digital group staff changes

I am pleased to announce the addition of two engineers to the Digital Group.

Don VanBeek, (ext. 6301), BSEE from Portland State University, will be handling high speed logic, STTL and ECL devices.

Ernesto (Ernie) Estrada, (ext. 7148), BSEE from University of Texas at El Paso, has assumed responsibility for LSTTL devices.

Ted Olivarez
Manager

Testing underway on 32K ROMs

Evaluation and characterization of several 32K read-only memory (ROM) devices has been completed. Sources included in the evaluation were Signetics (2632), Motorola (MCM68A332), Synertek (SY2332), General Instruments (RO-3-8332C) and Rockwell (R2332). Sample devices were requested from AMD, National, NEC and Intel, but these did not arrive in time for analysis. (Texas Instruments is an unusual case, and will be discussed later in the article.)

Table 1 lists data which may be useful to many design groups. Although the Rockwell devices exhibited low power consumption, their access times failed to meet specification at 70°C. In the case of Synertek, the margin on access time is close to the maximum specified value (70°C case). Process variations could easily cause the device to exceed the specification value. Designs which do not allow for some safety margin might be in trouble if the Synertek part is used.

Texas Instruments' was the first 32K ROM (4732) in volume production. Parts from TI were purchased for use in some Tek instruments. However, minimum order requirements became a problem because our needs were small (approx. 1000/year). After many processing problems, TI finally told us they were not interested in small volume business. They also requested we not place a ROM order unless volume was 8,000 to 10,000+ per year. Small orders just get lost in their system!

We will publish additional evaluation information as new 32K ROM sources become available and testing is completed.

For more information, please contact Bob Goetz (58-299), ext. 6302.

32K ROMs

	Motorola MCM 68A332 (3 samples)		General Instruments RO-3-9332C (2 samples)		Synertek SY2332 (2 samples)		Signetics 2632 (6 samples)		Rockwell R2332 (4 samples)	
	25°C	70°C	25°C	70°C	25°C	70°C	25°C	70°C	25°C	70°C
Access time* t_{acc} (nS)	188	215	255	297	328	400	280	385	334	>450
I_{cc} (static) (mA)	34.7	29.6	113	167.5	63.8	92.8	53.5	45.8	52.5	67.8
I_{cc} (dynamic) (mA)	70.5	54.8	95.8	149	54.4	76	82.1	71.4	43	59

Table 1 (average values)

*Measured at nominal voltages

ComponentNewsNewComponents

This column is designed to provide timely information regarding new components, vendors, availability and price. "New Components" can also be used as an informal update to the Common Design Parts Catalogs. Samples may or may not be available in Engineering Stock.

Vendor	No.	Description	When Available	TekP/N	Approx. Cost	Engineer to contact
		analog devices				
Beckman	7545	D/A, 12-bit, CMOS μP compatible	now	no P/N	$20.00	Don Gladden, 6700
Beckman	7546	D/A, 12-bit, CMOS μP compatible, with voltage reference and op amp	now	no P/N	24.00	Don Gladden, 6700
Beckman	7580	DAC-80, 12-bit CMOS	now	no P/N	17.50	Don Gladden, 6700
Analog Devices	AD536AJD	Converter, RMS to DC	now	156-1259-00	10.00	Don Gladden, 6700
Analog Devices	AD590	Temperature Sensor	now	no P/N	1.95	Don Gladden, 6700
EXAR	XR-L555	Timer, CMOS 555, 900μW power dissipation	——	no P/N	.90	Don Gladden, 6700
Texas Instruments	uA 2240	Timer/counter, programmable	now	no P/N	2.14	Don Gladden, 6700
Signetics	5009	D/A 8-bit 135 nS	now	156-1255-00	2.00	Don Gladden, 6700
Signetics	5018	D/A, 8-bit μP compatible, with voltage output and internal reference	now	soon	5.00	Don Gladden, 6700
Precision Monolithics	SMP-81	Sample-and-hold circuit	now	soon	1.75	Don Gladden, 6700
PMI	OP-20	Micropower op amp, 300μV max. offset voltage, single supply	now (samples)	no P/N	2.00	John Hereford, 6700
National	LMI3600	Amplifier, dual operational transconductance with linearizing diodes and buffers	soon	no P/N	——	John Hereford, 6700
Motorola	MC3476	Op amp, programmable	1979	no P/N	——	John Hereford, 6700
Signetics	NE5532	Dual op amp, 9V/μS slew rate, low noise, high output drive	soon	156-1272-00	1.50	John Hereford, 6700
Motorola	MC1410G	Microcircuit, linear, wideband video amplifier, 8-pin DIP, TO-99	now	156-1271-00	1.50	Matt Porter, 7461
		digital devices				
Signetics	82S100	FPLA	now	156-1269-00	10.50	Ted Olivarez, 7607
Signetics	82S107	FPLA	now	156-1254-00	10.50	Ted Olivarez, 7607
TI	74LS145	Decoder, BCD-to-decimal	now	soon	——	Wilton Hart, 7607
TI	74LS147	Encoder, 10-line to 4-line	now	soon	——	Wilton Hart, 7607
TI	74LS112	Flip-flop, dual J-K	now	soon	——	Wilton Hart, 7607
Intersil	IM7213	Clock, precision	now	soon	——	Wilton Hart, 7607
Harris	HM6514	RAM, 1024x4 CMOS	now	soon	——	Wilton Hart, 7607
RCA	CDP401150	Buffer, level shifting	now	soon	——	Wilton Hart, 7607
RCA	CDP1857D	Buffer, 4-bit, 3-state	now	soon	——	Wilton Hart, 7607
RCA	CDP1802D	MPU, 8-bit	now	soon	——	Wilton Hart, 7607
AMD	25LS2521	Comparitor, 8-bit	now	soon	——	Wilton Hart, 7607
TI	74LS96	Shift register, 5-bit	now	soon	——	Wilton Hart, 7607
TI	74LS13	Schmitt trigger, dual 4-input	now	soon	——	Wilton Hart, 7607
National	81LS95	Buffer, tri-state octal	now	soon	——	Wilton Hart, 7607
Motorola	MC14532	Encoder, 8-bit priority	now	soon	——	Wilton Hart, 7607

TECHNICAL STANDARDS

The function of Technical Standards is to identify, describe, and document standard processes, procedures, and practices within the Tektronix complex, and to insure these standards are consistent with established national and international standards. Technical Standards also provides a central repository for standards and specifications required at Tektronix. *Chuck Sullivan, manager (58-187)*

new and revised standards available from Technical Standards

ANSI B4.2 Preferred Metric Limits and Fits 1978
ANSI B4.3 General Tolerances for Metric Dimensioned Products 1978 ($3.00)
ANSI X3.26 Hollerith Punched Card Code (Draft)
ANSI X3/TR American National Dictionary for Information Processing (Sept. 1977)
ASA Z32.2.3 Graphical Symbols for Pipe Fittings, Valves, and Piping (1953)
ASTM A 623 General Requirements for Tin Mill Products (1977)
ASTM D 1351 Polyethylene Insulated Wire and Cable (1978)
ASTM D 2002 Isolation of Representative Saturates Fraction (1973)
ASTM E 140 Standard Hardness Conversion Tables for Metals (1978)
DIN 19004 Screw Threads of Shutter Cable Release, Tip and Socket (Nov. 1973)
ISA S61.2 Industrial Computer System Fortran Procedure for File Access (1977)
MIL-C 24308A Supplement 1B – Connectors, Electric, Rectangular, Miniature Polarized Shell, (June 1973)
MIL-C 60921A Cable Assembly, Test, Electric Switch for Use on Suu-14/A Dispenser (June 1978)
MIL-F 9882B Note 1 – Food Service Attendants (July 1978)
MIL-F 9892C(2) Note 1 – Food Service Contracts (July 1978)
MIL-M 38510/14B Amendment 3 – Microcircuits, Digital, TTL Data Selectors (April 1978)
MIL-M 38527B Supplement 1A – Mounting Pads and Insulator Disks, Electric Component (7/78)
MIL-P 55110C Printed Wiring Boards (April 1978)
MIL-P 58102 Plastic Sheet and Laminates, Flex, for Environment Protective Storage (May 1978)
MIL-R 10509F Amendment 4 – Resistors, Fixed Film (High Stability) (July 1978)
MIL-S 24187D Switch, Assembly, Linear Movement, Manual and Remote Operation (June 1978)
MIL-S 24187D Supplement 1 – Switch, Assembly, Linear Movement, Manual and Remote Operation (June 1978)
MIL-STD 199B Note 5 – Resistors, Selection and Use of (May 1978)
MIL-STD 2073-2 Packaging Requirement Codes (May 1978)
MIL-STD 454F Standard General Requirements for Electric Equipment (March 1978)
MIL-STD 750B Note 8 – Test Methods for Semiconductor Devices (January 1978)
NASA GSC-12225 Technical Support Package for Improved Optical Filter
NAV 4030.28A, CH-3 Packaging of Materiel (June 1978)
NBS Relevancy of Measurements by a Systems Approach
NBSIR 73-219 Eight Techniques for the Optical Measurement of Surface Roughness (May 1973)
NF X08-003 Safety Colours and Safety Signs (June 1976)
NFPA 75 Electric Computer/Data Processing Equipment (1976)
OO-P 631C Press Brakes, Power Operated, Mech., Sheet and Plate (Feb. 1975)
OO-S 260A Sealing and Packaging Machine, Plastic Film (April 1978)
UL 478 Revision – Standard for Electronic Data-Processing Units and Systems (August 1978)
VDE List of VDE Specifications, German (April 1978)

for information on the above publications, please call Carol Whitmore, Technical Standards, ext. 7976.

Fiber optics experimenter kits

Tektronix engineers have indicated an interest in a variety of fiber optic experimenter kits now on the market. Typical of these are the Amp ($350) and Augat ($200) kits.

Persons interested in getting the kits for first-hand experience with optical data links might consider a recently published "Experimenters Guide" from Motorola. It describes a one mega-bit data link, which can be built with less than $40 in components. (The Amp Experimenters Kit uses the same design.) Tek-made circuit boards are available. These boards are similar to those in the Motorola Experimenters Guide, but slightly modified to make construction easier.

If you would like a Tek-made kit, please complete and return the form below. If you already have a fiber optic kit that would be available for loan to other engineers, please send that information.

We would also like to know how extensively fiber optics are presently being utilized at Tek. If you are using fiber optics in your area, I would appreciate a brief description of your application.

We are evaluating the various F.O. data links that are on the market as time and availability permit. We presently have samples from Meret and Augat, and expect to have a duplex unit from 3M early in October. If you would like to try any of these in your applications, please let me know.

Louis Mahn
58-299 (ext. 6389)

Name _____ Ext. _____ Del. Sta. _____

Please send me _____ of the Tek-made data links. Cable length required _____

Resp. Acct. No. _____

I have a data link or kit I could loan to other engineers.

Brand _____ Model or P/N _____

I presently use fiber optics in Tek processes or products. (Briefly describe)

_____

_____

_____

_____

_____

_____

Please return to Louis Mahn, 58-299.

Component/Engineer listing

Call the appropriate engineer listed below or stop by 58-299 for information on purchased components.
(**Note:** The Digital Group is now located at 58-125.)

ATTENUATORS	Byron Witt 5417
BATTERIES	Byron Witt 5417
BULBS	Peter Butler 5417
CABLES	Rod Christiansen 5953
CAPACITORS	
ceramic, high-voltage, mica	Harry Ford 6520
electrolytic, film	Don Anderson 5415
variable	Alan LaValle 5415
COILS	Harry Ford 6520
CONNECTORS	Peter Butler 5417
CORES, ferrite	Byron Witt 5417
CRYSTALS & SAW	Byron Witt 5417
DELAY LINES	Byron Witt 5417
DIODES	
visible LEDs	Betty Anderson 6389
IR emitter, laser diode	Louis Mahn 6389
all others	Gary Sargeant 5345
DISPLAYS	Betty Anderson 6389
ELECTROMECHANICAL PRINTERS	Jim Deer 7711
FANS	Bill Stadelman 7711
FETs	Jerry Willard 7461
FIBER OPTICS	
cables, emitters, decoders	Louis Mahn 6389
FILTERS	
air	Bill Stadelman 7711
crystal	Byron Witt 5417
light	Jim Deer 7711
line	Joe Joncas 6365/Herb Zajac 7887
FUSES, FUSEHOLDERS	Joe Joncas 6365
GASKETS	Rod Christiansen 5953
GENERATORS	Bill Stadelman 7711
HARDWARE	Rod Christiansen 5953
HEAT SINKS	Jim Williamson 5345
INDUCTORS	Byron Witt 5417
INTEGRATED CIRCUITS	see microcircuits
JOYSTICKS	Jim Deer 7711
KEYBOARDS	Jim Deer 7711
KNOBS	Rod Christiansen 5953
LAMPS, LAMP SOCKETS	Peter Butler 5417
LIGHT-EMITTING DIODES	Betty Anderson 6389
MAGNETIC TAPE HEADS	Bill Stadelman 7711
METERS	
digital panels	Chris Martinez 7709
general	Joe Joncas 6365
MICROCIRCUITS	
A/D converters	Chris Martinez 7709
bubble memory devices	Eric Peterson 6302
CCD-analog	John Hereford 6700
CCD-digital	Eric Peterson 6302
CMOS devices	Wilton Hart 7607
communications	Matt Porter 7461
comparitors	John Hereford 6700
D/A converters	Don Gladden 6700
digital semiconductor storage	Eric Peterson 6302
EAPROMs, EPROMs, PROMs	Bob Goetz 6302
ECL devices	Don VanBeek 5414
FPLAs, PALs	Ted Olivarez 7607

MICROCIRCUITS, continued	
high speed logic	Don VanBeek 5414
hybrids	Jerry Willard 7461
linear devices	Don Gladden 6700
low-power Schottky TTL	Ernie Estrada 7148
MOS(general)	Bill Pfeifer 6303
operational amplifiers	John Hereford 6700
regulators	
linear	Chris Martinez 7709
switching	Jim Williamson 5345
RAMs	Eric Peterson 6302
ROMs	Bob Goetz 6302
Schottky TTL	Don VanBeek 5414
TTL devices	Ted Olivarez 7607
MICROPROCESSORS	Carl Teale 7148
bit-slice microprocessors	Ted Olivarez 7607
peripherals and interfaces	Jim Howe/Bill Pfeifer 6303
Z80, 8080, 8085	Wilton Hart 7607
MICROWAVE components	Byron Witt 5417
MONITORS	Harry Ford 6520
MOTORS	Bill Stadelman 7711
MULTIPLIERS, high-voltage	Gary Sargeant 5345
OSCILLATORS	Byron Witt 5417
PHOTOCOUPLERS	Louis Mahn 6389
POTENTIOMETERS	Gene Single 5302
POWER CORDS/receptacles/plugs	Joe Joncas 6365
RAW MATERIALS, metals, plastics	Rod Christiansen 5953
READOUT DEVICES	Louis Mahn 6389
RELAYS, mechanical & solid state	Paul Johnson 6365
RESISTORS	
fixed	Ray Powell 6520
variable	Gene Single 5302
SCRs, SCSs	Paul Johnson 6365
SHIELDS	Harry Ford 6520
SPARK GAPS	Peter Butler 5417
SLEEVES, insulating	Peter Butler 5417
SPEECH, input/output	Jim Deer 7711
SOCKETS	
crystal	Byron Witt 5417
all others	Peter Butler 5417
SWITCHES	
general, solid state	Joe Joncas 6365
reed	Paul Johnson 6365
TERMINAL PINS	Peter Butler 5417
TERMINATIONS	Byron Witt 5417
THERMISTORS	Ray Powell 6520
TRANSDUCERS	Byron Witt 5417
TRANSFORMERS	Byron Witt 5417
power	Bill Stadelman 7711
TRANSISTORS	
field-effect	Jerry Willard 7461
phototransistors	Louis Mahn 6389
power	Jim Williamson 5345
small signal, arrays	Matt Porter 7461
triacs, unijunctions	Paul Johnson 6365
TUBING, metal	Rod Christiansen 5953
WIRE	Rod Christiansen 5953

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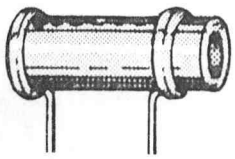

"Dog-bone" cap use re-evaluated

"Dog-bone" ceramic tubular capacitors are manufactured with a hole in the center. A resistor is sometimes placed through this hole to form a frequency-compensation network.

Because of the continuing problems associated with "dog-bone" caps (price, availability, leadtime), we are re-evaluating our applications of these devices.

Therefore, if you are in an area that utilizes the center hole in the capacitor, please contact me or Harry Tanielian (19-384) *in writing,* as soon as possible.

Negotiations are currently underway to approve another source for ceramic tubular caps. Until these negotiations are complete, though, the parts are not recommended for new design.

Harry Ford
58-299

AMD/Zilog information exchange

On August 25, Advanced Micro Devices (AMD) and Zilog signed a technical exchange and cross-licensing agreement. Under the terms of the agreement AMD will alternate source the Zilog Z-8000 16-bit microprocessor, and the two companies will cooperate on the development of peripheral circuits to support the CPU.

To accomplish this, AMD will receive Z-8000 mask sets, test and other pertinent information. The two companies have agreed to the development and cross-licensing of specific peripheral circuits to expand the Z-8000 family.

Plans call for the development of a high-speed unit with a higher through-put than any 16-bit MPU on the market today. This device should be available by the fourth quarter of 1978.

For more information on this agreement, contact Tom Stevenson (Jas. J. Backer Co. representative), 297-3776.

users of dielectric withstand testers:

There has been some confusion about the proper trip current settings for dielectric withstand testers (EPA-ROD-L models M100AV and M100B).

Product Safety recommends that instruments which have a trip current adjustment be set to trip slightly above the normal current level for the particular instrument under test. This will help locate a fault which otherwise might not be detected.

The Standards Lab will indicate setting points for the trip current adjustment when requested, and the normal operating current and voltage for an instrument provided.

Ed Wesel
Product Safety

component news

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