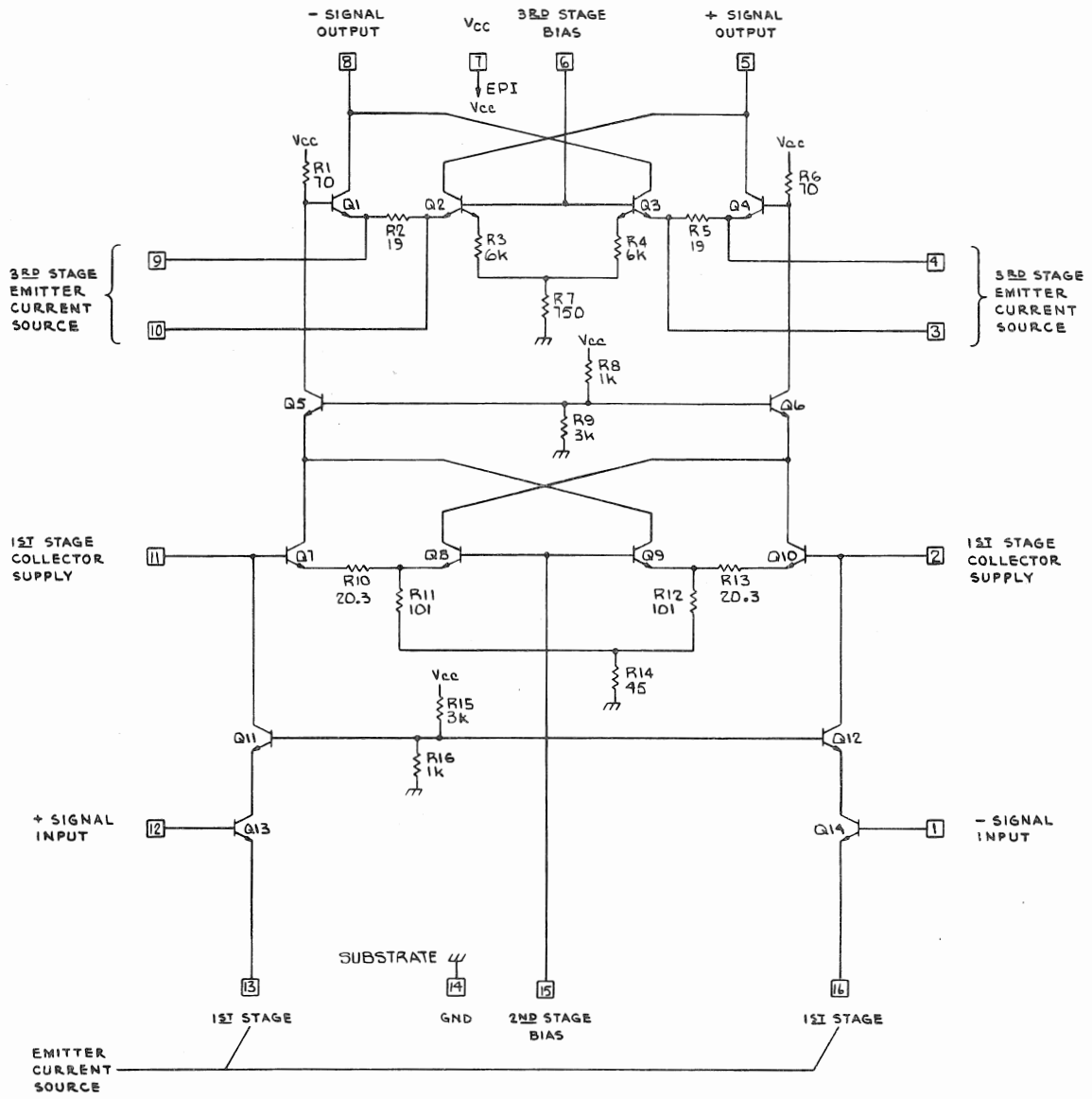
VERTICAL OUTPUT AMPLIFIER 203-0089-90 M89

DESCRIPTION

This circuit consists of three cascode stages. The first stage serves as high frequency compensation and termination for the delay line. The second stage will do gain peaking at high frequencies to compensate for the R-C roll-off at the CRT, in addition to low-frequency gain. The last stage has a fixed gain, and has terminals brought out for thermal distortion compensation, and also for external long-tails. The common base devices of the last cascode remain discrete in order to have enough breakdown voltage for a CRT. Bandwidth of the integrated circuit into a low impedance load is 600 MHz.

PROCESS	SHF II With Nichrome
POWER SUPPLY.	15 Volts
PACKAGE	TO-8 With Stud
DESIGNER	Jim Cavoretto/Einar Traa
INSTRUMENT USAGE	465G 465H 465K 7704A 335K D7704G 464 D7704H 466



ENGR	Ewan Trea	10-15-74	PROCESS	SH II
DWN BY	Pam Cherrie	8-8-74	PACKAGE	WAFER FORM
CHK BY	[illegible]	11-1-74	DIE SIZE	50mil x 55mil
TYPE	MONOLITHIC	VERTICAL OUTPUT AMPLIFIER		M089A
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A		PART NO. 203-0089-90		