ENGINEERING NEWS

COMPANY CONFIDENTIAL

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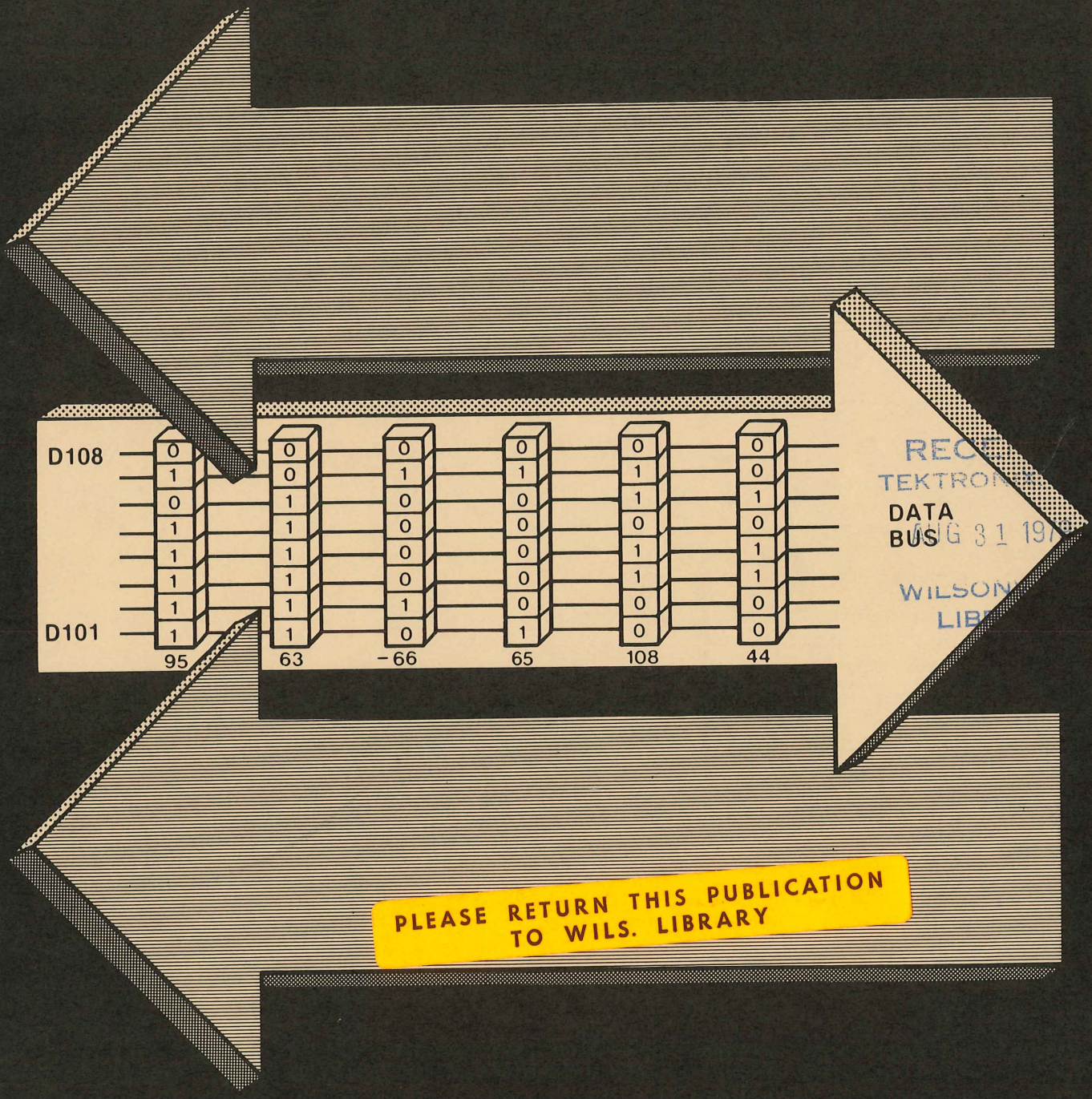
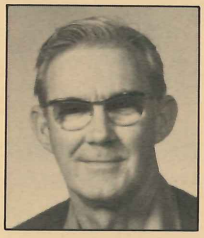


GPIB System Concepts

GPIB SYSTEM CONCEPTS



Arnold Farley, TM 500 Manuals, ext. 1552 (Walker Road).

This series of articles describes the digital interface specified in IEEE Standard 488-1975, "Standard Digital Interface for Programmable Instrumentation." At Tektronix, the digital interface is commonly called the General Purpose Interface Bus (GPIB).

This first article discusses signal-line definitions. The next article will discuss interface functions and the protocol for transferring data between instruments on the bus.

WHAT IS THE GPIB?

The GPIB is a digital interface that allows efficient communication between the components of an instrumentation system.

The primary purpose of the GPIB is to connect self-contained instruments to other instruments or devices. This means that the GPIB is an interface system independent of device functions.

There are four elements of the GPIB: mechanical, electrical, functional, and operational.

Of these four, only the last is device-dependent. Operational elements state the way in which an instrument reacts to a signal on the bus. These reactions are device-dependent characteristics and state the way in which the instruments use the GPIB via application software.

Mechanical Elements. The standard defines the mechanical elements : cables and connectors. Standardizing the connectors and cables ensures that GPIB-compatible instruments can be physically linked together with complete pin compatibility.

The connector has 24 pins, with 16 assigned to specific signals and eight to shields and grounds. Instruments on the bus may be arranged in a linear or star configuration.

Electrical Elements. The voltage and current values required at the connector nodes for the GPIB are based on TTL technology (power source not to exceed +5.25V referenced to logic ground). The standard defines the logic levels as follows. Logical 1 is true state, low-voltage level ($\leq$+0.8V), signal line is **asserted.** Logical 0 is false state, high-

BACKGROUND

The General Purpose Interface Bus (GPIB) is a control bus that interfaces with a microcomputer (processor) and external peripheral devices.

Prior to the original development of the GPIB by Hewlett-Packard in 1975, the CAMAC (Computer Automated and Measurement Control) interface was developed by the nuclear industry. The IEEE promulgated this interface under several standards: Std 583 (Basic CAMAC), Std 595 (CAMAC), and Std 596 (Parallel CAMAC). CAMAC was comprised of a rigorously-specified mainframe (chassis) housing 25 plug-in modules. Outside of the nuclear industry and some electrical power companies, CAMAC was rarely used in industrial applications. The Parallel CAMAC transmitted data at a rate near 5 megabits/second over 86 lines. The major obstacles to its acceptance has been its expense and impracticality for microprocessor control.

The GPIB was developed as a control bus for instruments. This interface is oriented toward system configurations that use a variety of peripherals. Any type of 8-bit data is sent or received over the data bus in a byte-serial, bit-parallel fashion. Bus extenders can be used, at reduced data rates, to interface with common carriers. The GPIB is a very practical and inexpensive means to transmit or receive data from microcomputers over relatively short distances (up to 20 meters without bus extenders).

INTERFACE FUNCTION	SYMBOL
Source Handshake	SH
Acceptor Handshake	AH
Talker or Extended Talker	T or TE
Listener or Extended Listener	L or LE
Service Request	SR
Remote-Local	RL
Parallel Poll	PP
Device Clear	DC
Device Trigger	DT
Controller	C

Table 1. The ten major interface functions for the GPIB.

voltage level (≥+2.0V), signal line is **not asserted.**

Messages can be sent over the GPIB as either active-true or passive-true signals. Passive-true signals occur at a high-voltage level and must be carried on a signal line using open-collector devices. Active-true signals occur at a low-voltage level.

Functional Elements. The functional elements of the GPIB cover three areas:

Ten interface functions that define the use of specific signal lines so that an instrument can receive, process, and send messages (the ten interface functions - with their allowable subsets - provide an instrumentation system with complete communications and control capabilities).

The **specific protocol** by which the interface functions send and receive their limited set of messages.

The **logical and timing relationships** between allowable states for the interface signal lines.

INTERFACE FUNCTIONS

Not every instrument on the bus has all ten functions (listed in table 1), because only those functions important to a particular instrument's purpose need be implemented.

A TYPICAL SYSTEM ON THE GPIB

Figure 1 illustrates an example of the GPIB and the nomenclature for the 16 active signal lines. Only four instruments are shown, but the GPIB can support up to 15 instruments connected directly to the bus. However, more than 15 devices can be interfaced to a single bus if they do not connect directly to the bus but are interfaced through a primary device. Such a scheme can be used for programmable plug-ins housed in a mainframe where the mainframe is addressed with a primary address code and the plug-ins are addressed with a secondary address code.

The instruments connected to a single bus cannot be separated by more than 20 meters (total cable length) and at least one more than half the number of instruments must be in the power-on state. To maintain the electrical characteristics of the bus, a device load must be connected for each two meters of cable length. Although instruments are usually spaced no more than two meters apart, they can be separated farther if the required number of device loads are lumped at any one point.

CONTROLLERS, TALKERS, AND LISTENERS

A **talker** is an instrument that can send data over the bus; a **listener** is an instrument that can accept data from the bus. No instrument can communicate until it is enabled to do so by the controller in charge of the bus.

A **controller** is an instrument that determines, by a software routine, which instrument will talk and which instruments will listen during any given time interval. The controller also has the ability to assign itself as a talker or listener whenever the program routine requires. In addition to designating the current talker and listeners for a particular communication sequence, the controller has the task of sending special codes and commands (called **interface messages**) to any or all of the instruments on the bus.

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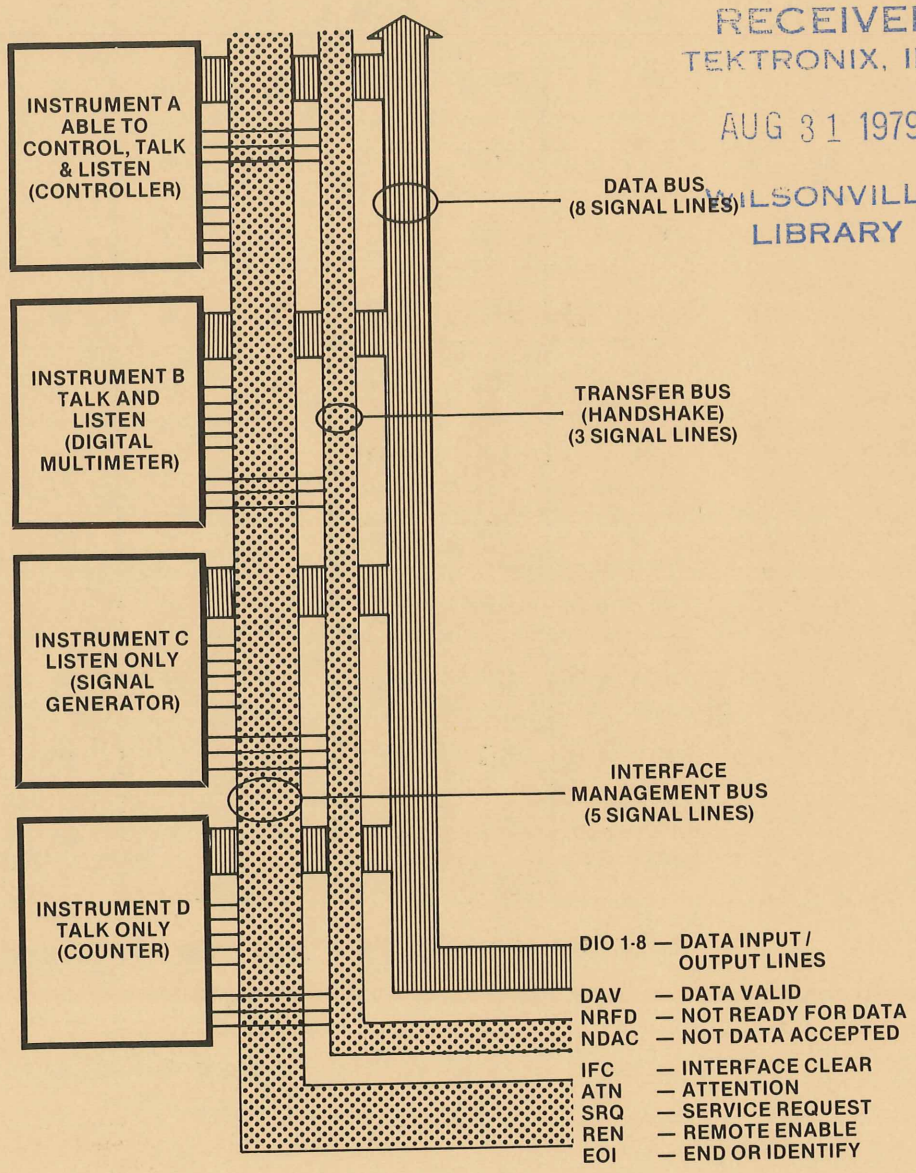

Figure 1. A typical system using the general purpose interface bus (GPIB).

ASCII & IEEE 488 (GPIB) CODE CHART

B7 B6 B5 BITS / B4 B3 B2 B1	ø ø ø	ø ø 1	ø 1 ø	ø 1 1	1 ø ø	1 ø 1	1 1 ø	1 1 1
	CONTROL		NUMBERS SYMBOLS		UPPER CASE		LOWER CASE	
ø ø ø ø	0 NUL 0 0	20 DLE 10 16	40 SP 20 32	60 0 30 48	100 @ 40 64	120 P 50 80	140 ` 60 96	160 p 70 112
ø ø ø 1	1 GTL SOH 1 1	21 LLO DC1 11 17	41 ! 21 33	61 1 31 49	101 A 41 65	121 Q 51 81	141 a 61 97	161 q 71 113
ø ø 1 ø	2 STX 2 2	22 DC2 12 18	42 " 22 34	62 2 32 50	102 B 42 66	122 R 52 82	142 b 62 98	162 r 72 114
ø ø 1 1	3 ETX 3 3	23 DC3 13 19	43 # 23 35	63 3 33 51	103 C 43 67	123 S 53 83	143 c 63 99	163 s 73 115
ø 1 ø ø	4 SDC EOT 4 4	24 DCL DC4 14 20	44 $ 24 36	64 4 34 52	104 D 44 68	124 T 54 84	144 d 64 100	164 t 74 116
ø 1 ø 1	5 PPC ENQ 5 5	25 PPU NAK 15 21	45 % 25 37	65 5 35 53	105 E 45 69	125 U 55 85	145 e 65 101	165 u 75 117
ø 1 1 ø	6 ACK 6 6	26 SYN 16 22	46 & 26 38	66 6 36 54	106 F 46 70	126 V 56 86	146 f 66 102	166 v 76 118
ø 1 1 1	7 BEL 7 7	27 ETB 17 23	47 ' 27 39	67 7 37 55	107 G 47 71	127 W 57 87	147 g 67 103	167 w 77 119
1 ø ø ø	10 GET BS 8 8	30 SPE CAN 18 24	50 (28 40	70 8 38 56	110 H 48 72	130 X 58 88	150 h 68 104	170 x 78 120
1 ø ø 1	11 TCT HT 9 9	31 SPD EM 19 25	51) 29 41	71 9 39 57	111 I 49 73	131 Y 59 89	151 i 69 105	171 y 79 121
1 ø 1 ø	12 LF A 10	32 SUB 1A 26	52 * 2A 42	72 : 3A 58	112 J 4A 74	132 Z 5A 90	152 j 6A 106	172 z 7A 122
1 ø 1 1	13 VT B 11	33 ESC 1B 27	53 + 2B 43	73 ; 3B 59	113 K 4B 75	133 [5B 91	153 k 6B 107	173 { 7B 123
1 1 ø ø	14 FF C 12	34 FS 1C 28	54 , 2C 44	74 < 3C 60	114 L 4C 76	134 \ 5C 92	154 l 6C 108	174 | 7C 124
1 1 ø 1	15 CR D 13	35 GS 1D 29	55 - 2D 45	75 = 3D 61	115 M 4D 77	135] 5D 93	155 m 6D 109	175 } 7D 125
1 1 1 ø	16 SO E 14	36 RS 1E 30	56 . 2E 46	76 > 3E 62	116 N 4E 78	136 ^ 5E 94	156 n 6E 110	176 ~ 7E 126
1 1 1 1	17 S1 F 15	37 US 1F 31	57 / 2F 47	77 UNL ? 3F 63	117 O 4F 79	137 UNT _ 5F 95	157 o 6F 111	177 RUBOUT (DEL) 7F 127
	ADDRESSED COMMANDS	UNIVERSAL COMMANDS	LISTEN ADDRESSES		TALK ADDRESSES		SECONDARY ADDRESSES OR COMMANDS	

Interface messages are sent with ATN asserted.

KEY

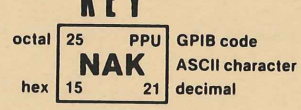

Figure 2. ASCII & IEEE 488 (GPIB) Code Chart.

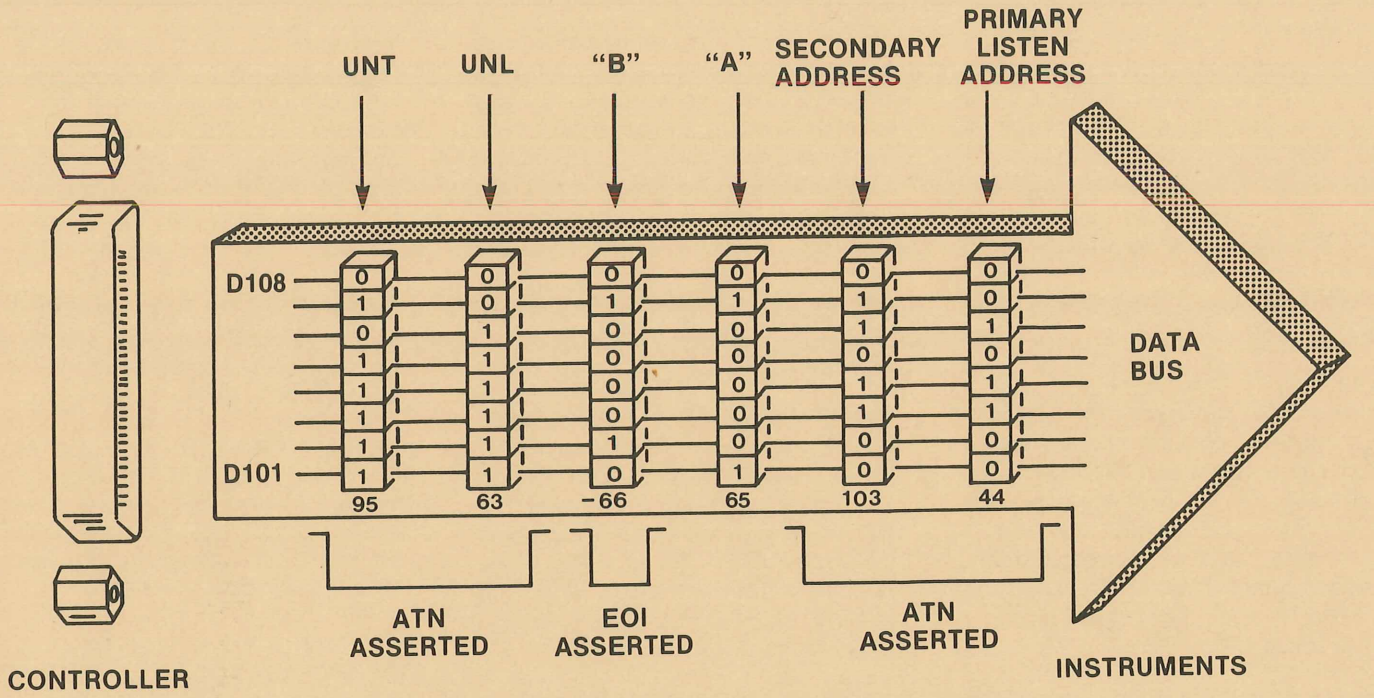

Figure 3. An example of data byte traffic on the GPIB.

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INTERFACE MESSAGES

The IEEE standard specifies that the interface messages, as shown in figure 2, ASCII & IEEE 488 (GPIB) Code Chart, be used to address and control instruments interfaced to the GPIB. Interface messages are sent and received only when the controller asserts the ATN bus line. The user can correlate interface message coding to the ISO 7-bit code by relating data bus lines DI01 through DI07 to bits 1 through 7, respectively.

Interface messages include the primary talk and listen addresses for instruments on the bus, addressed commands (only instruments previously addressed to listen respond to these commands), universal commands (all instruments, whether they have been addressed or not respond to these), secondary addresses for devices interfaced through their primary instrument, and secondary commands. At present, the standard classifies only two interface messages as secondary commands, Parallel Poll Enable (PPE) and Parallel Poll Disable (PPD). (Parallel Poll Enable means that *after* the controller configures the system for a parallel poll (PPC command), all instruments respond at the same time with status information on receipt of PPE.)

DEVICE-DEPENDENT MESSAGES

The IEEE 488-1975 does not specify coding of device-dependent messages, messages that control the device's internal operating functions. After addressing (via interface messages) a talker and listener(s), the controller unasserts the ATN bus line. When ATN becomes false, any commonly-understood 8-bit binary code may be used to represent a device-dependent message.

The standard recommends that the alphanumeric codes associated with the numbers, symbols, and upper case characters (decimal 32 to decimal 94) in the ASCII Code Chart be used for device-dependent messages. One example of a device-dependent message is the ASCII character string

MODE V; 2.5MV; FREQ 1E3

which may tell an instrument to set its front-panel controls to the voltage mode, with 2.5 millivolt output at a frequency of 1000Hz.

When 8-bit binary codes other than the ISO 7-bit code are used for device-dependent messages, the most significant bit must be on data line DI08 (for bit 8).

To summarize the difference between interface and device-dependent messages, remember that any message sent or received when the ATN line is asserted (true) is an interface message. Any message (data bytes) sent or received when the ATN line is unasserted (false) is a device-dependent message.

GPIB SIGNAL LINE DEFINITIONS

Figure 1 shows the 16 signal lines of the GPIB functionally divided into three component busses: an eight-line data bus, a three-line transfer control (handshake) bus, and a five-line management bus.

The Data Bus. The data bus has eight bidirectional signal lines, DI01 through DI08. Information, in the form of data bytes, is transferred over this bus. A handshake sequence between an enabled talker and the enabled listeners transfers one data byte (eight bits) at a time. Data bytes in an interface or device-dependent message are sent and received in a byte-serial, bit-parallel fashion over the data bus.

Since the GPIB handshake sequence is an asynchronous operation, the data transfer rate is only as fast as the slowest instrument involved in a data byte transfer at any one time. A talker cannot place data bytes on the bus faster than any one listener can accept them.

Figure 3 illustrates the flow of data bytes when a typical controller sends ASCII data to an assigned listener on the bus. The first data byte, decimal 44, enables device 12 as a primary listener and the secondary address, decimal 108, enables a plug-in device as the final destination of the data to follow. The data is the two ASCII characters, A and B (decimal 65 and decimal 66).

The decimal value for B is specified as negative to activate the EOI line and signify the end of the device-dependent message. The controller activates the ATN line again and sends the universal unlisten (UNL) and untalk (UNT) commands to clear the bus. Six handshake cycles on the Transfer Bus are required to send the six data bytes.

The Transfer Bus (Handshake). Each time a data byte is sent over the data bus, an enabled talker and all enabled listeners execute a handshake sequence via the **transfer bus**. The transfer-bus signal lines are defined below. Figure 4 illustrates the basic timing relationship between the three signals. The ATN line is shown to illustrate the controller's role in the process. A flowchart for the handshake sequence is shown in figure 5.

Not Ready For Data (NRFD). An asserted NRFD signal line indicates one or more assigned listeners are not ready to receive the next data byte from the talker. When all of the assigned listeners for a particular data byte transfer have released NRFD, the NRFD line becomes unasserted (high). The RFD message (Ready For Data) tells the talker it may place the next data byte on the data bus.

Data Valid (DAV). The DAV signal line is asserted (low) by the talker after the talker places a data byte on the data bus. When asserted, DAV tells each assigned listener that a new data byte is on the data bus. The talker is inhibited from asserting DAV as long as any listener holds the NRFD signal line asserted.

Not Data Accepted (NDAC). Each assigned listener holds the NDAC signal line low-true (asserted) until the listener accepts the data byte currently on the data bus. When all assigned listeners accept the current data byte, the NDAC line becomes unasserted, telling the talker to remove the data byte from the bus. The DAC message (Data Accepted) tells the talker that all assigned listeners accepted the current data byte.

When one handshake cycle transfers one data byte, the listeners reset the NRFD line high and the NDAC line low before the talker asserts DAV for the next data byte transfer. NDAC and NRFD both high at the same time is an invalid state on the bus.

The Management Bus. The management bus is a group of five signal lines which are used to control the operation of the GPIB: IFC, ATN, SRQ, REN, and EOI.

Interface Clear (IFC). The system controller asserts the IFC signal line to place all interface circuitry in a predetermined quiescent state which may or may not be the power-on state.

Only the system controller can generate this signal. IEEE 488-1975 specifies that only three interface messages (universal commands) be recognized while IFC is asserted: Device Clear (DCL), Local Lockout (LLO), and Parallel Poll Unconfigure (PPU).

Attention (ATN). A controller asserts the ATN signal line when instruments connected to the bus are being enabled as talkers or listeners and for other interface control traffic. As long as the ATN signal line

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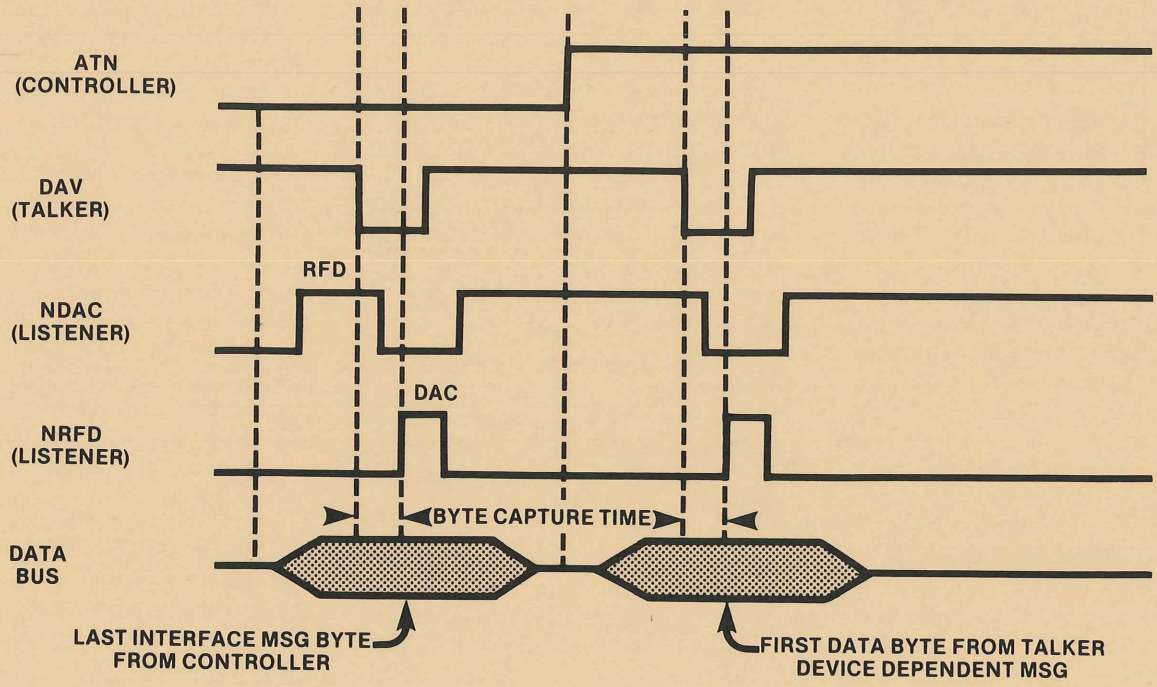

Figure 4. A typical handshake timing sequence (idealized). Byte capture time is dependent on the slowest instrument involved in the handshake.

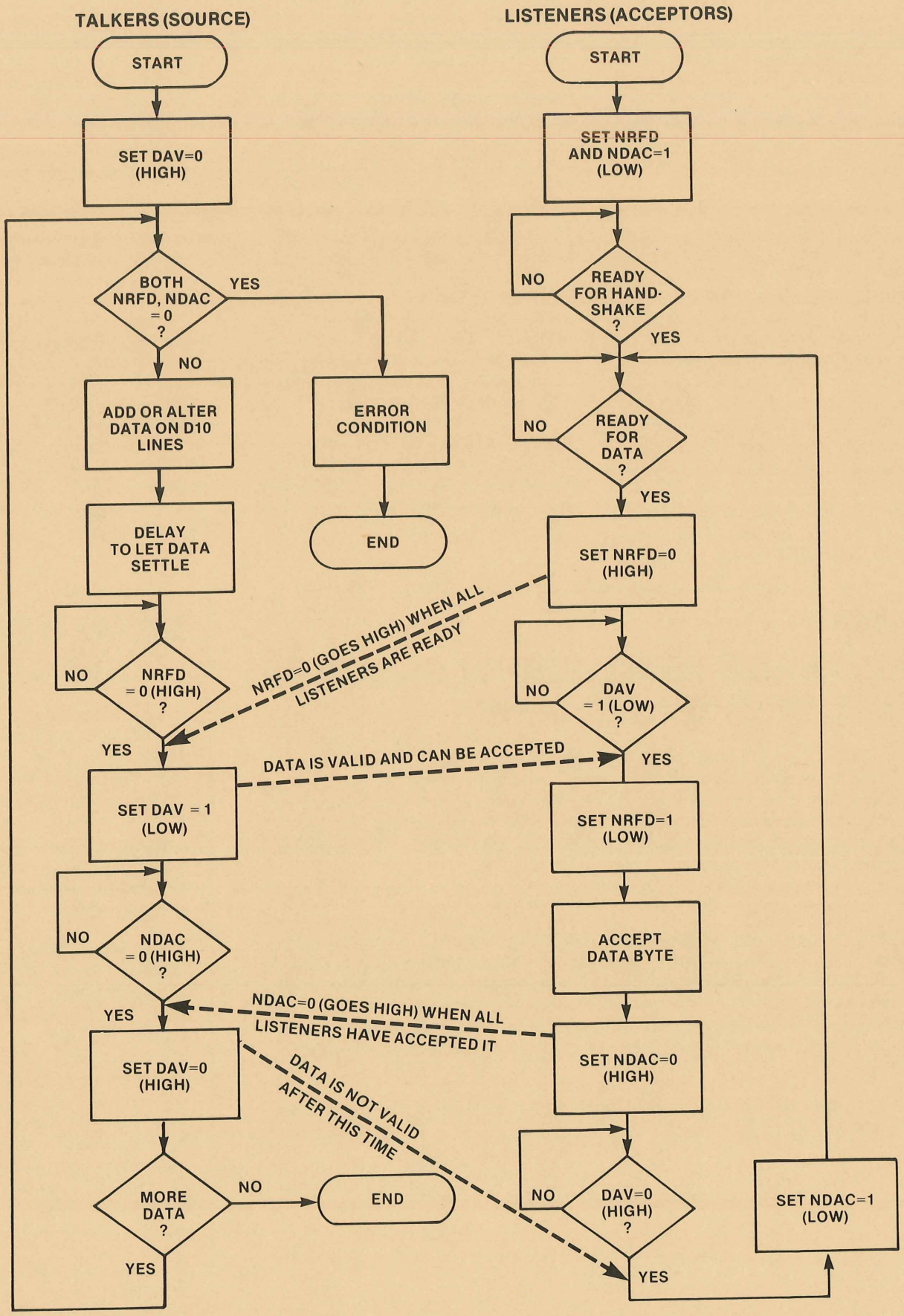

Figure 5. The handshake flow chart.

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is asserted (ATN = 1), only instrument address codes and control messages are transferred over the data bus. With the ATN signal line unasserted, only those instruments enabled as a talker and listener(s) can transfer data. Only the controller can generate the ATN signal.

Service Request (SRQ). Any instrument connected to the bus can request the controller's attention by asserting the SRQ line. The controller responds by asserting ATN and executing a serial poll to determine which instrument is requesting service. (An instrument requesting service identifies itself by asserting its DI07 line after being addressed.) After the instrument requesting service is found, program control is transferred to a service routine for that instrument. When the service routine is completed, program control returns to the main program. When polled, the instrument requesting service unasserts the SRQ line.

Remote Enable (REN). The system controller asserts the REN signal line whenever the interface system operates under remote program control. Used with other control messages, the REN signal causes an instrument on the bus to select between two alternate sources of programming data. A remote-local interface function indicates to an instrument that the instrument will use either information input from the front-panel controls (Local) or corresponding information input from the interface (Remote).

End or Identify (EOI). A talker can use the EOI to indicate the end of a data-transfer sequence. The talker asserts the EOI signal line as the last byte of data is transmitted. In this case, EOI is essentially a ninth data line and must observe the same setup times as the DI0 lines. When the controller is listening, it assumes that a data byte received is the last byte in the transmission (if the EOI signal line has been asserted). When the controller is talking, it may assert the EOI signal line as the last byte is transferred. The EOI signal is also asserted with the ATN signal if the controller conducts a parallel polling sequence. EOI is not used during serial polling.

FOR MORE INFORMATION

For detailed information on GPIB specifications, refer to IEEE 488-1975 (Revised 1978), published by the Institute of Electrical and Electronics Engineers, 245 East 47th Street, New York, New York 11117. To borrow a copy, call ext. 241 (Town Center). □

IN PRINT

HARDWARE EMULATION CONQUERS 16-BIT MICROPROCESSORS

Dick Lemke (Logic Analyzers and Digital Service Instruments Business Units), Doug Smith (Logic Instrument Division Marketing), and Tony Tunder (Semiconductor Test Systems Applications Engineering) have co-authored an article entitled "Hardware Emulation Conquers the Testing Mountain Created by 16-Bit Microprocessors" which appeared in the July 5, 1979 issue of **Electronic Design** Magazine.

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REVIEWERS NEEDED

Engineering News articles are becoming more technical and more detailed and that trend will continue. Although most articles are written and edited for a general engineering audience, only technical specialists can effectively review the content of very complex articles.

Engineering News publishes articles written by engineers and scientists in all the disciplines found at Tektronix. Examples include electrical engineering, mechanical engineering, chemistry, chemical engineering, materials research, human factors, and aspects of marketing and manufacturing of direct interest to the Tektronix engineering and scientific community.

If you are interested in reviewing a rough draft article in your specialty, call ext. 6795 or write to D.S. 19/313. □

NON-MANAGEMENT CAREER PATH OFFERS OPPORTUNITIES FOR TEK ENGINEERS AND SCIENTISTS

In December 1978, Wim Velsink (director, Tektronix Laboratories) called together the members of an Engineering/Scientific Approval Committee to approve engineers and scientists proposed for the new positions of engineer/scientist IV and V.

In this interview, members of the Approval Committee explain the new extensions of the technical career path for engineers and scientists.

What is the new technical career path?

Until December 1978, there were three job classifications for engineers and scientists at Tektronix: engineer/scientist I, II, and III.

The new technical career path adds two levels (IV and V) for those engineers and scientists who advance their technical knowledge and their influence on the technological direction of the company, but without entering management. Engineer/scientist levels IV and V have pay scales corresponding to engineering/scientific manager levels I and II.

What are the job descriptions for the new levels?

At Tektronix each engineering and scientific discipline (such as electronic engineering or physics) has its own level IV and V job description, but some generalizations apply to all level IV and V jobs covered by the Engineering Scientific Approval Committee (the Committee examines nominees only

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Thirty-eight Teks have been honored by the Engineering/Scientific Approval committee with the designation, Engineer/Scientist IV or V. Twenty-eight appointees assembled recently for a photo.

They are *first row,* from left, Fendall Winston, John Popa, Krishna Verma, Charlie Rhodes, George Wilson and Phil Snow. *Second row,* Dave Bates, Bob Holmes, Jim Woo, Sam Guthrie and Chuck Gold. *Third row,* Ian Getreu, Bill Price, John Moore, Ron Robinder and Gordon Roper. *Fourth row,* Carl Battjes, Gordon Long, Ralph Rose, Ralph Ulrich and Bill Stein. *Fifth row,* Val Garuts, Linley Gumm, John Addis, Jon Morris, Jon Mutton, Rod Bristol and Jerry McTeague.

Missing from photo are Morris Engelson, Delmer Fehrs, George Copeland, Pel Chow, Jack Gilmore, Chris King, Binoy Rosario, Ken Schlotzhauer and Kit Bradley.

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for IV and V positions ranged at 20 or higher).

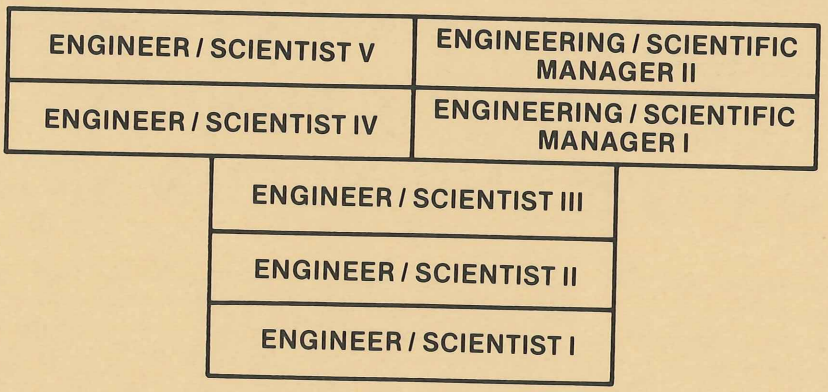
When evaluating nominees, Committee members look for quite a few characteristics, not *all* of which have to be met. A few are: education, past technical contributions (either inside or outside Tektronix), self-starting ability, and influence on other engineering and scientific people at Tektronix.

Other characteristics are: recognition as an expert by other people in the same field (the nominee's opinions should be highly respected and sought after by other Tektronix employees and — for V's — by people outside the company, as well), patents received, trade secrets acknowledged, and major contributions to major programs.

Still other characteristics are contributions to internal and external publications, successful efforts to attract top talent to Tektronix, major decisions coordinated, technical leadership exercised, acting as a product conscience for Tektronix ("Is this the right way for us to go?"), well-thought-out proposals, and influence on major corporate decisions.

The engineer/scientist IV position is the first level of the technical career path that parallels an engineering/scientific management position. The engineer or scientist in this position serves as a technical consultant for people within Tektronix. Level IV is a position involving the formulation of new principles and concepts, and includes the responsibility for originating, interpreting, organizing, executing, and coordinating assigned projects. An engineer/scientist IV may have an advanced engineering or science degree or 10 or more years experience.

An engineer/scientist V is well-known throughout his or her field, and would be consulted both inside and outside Tektronix. Responsible for developing new concepts and solutions, and being a technology and product conscience for the company, the engineer/scientist V may have an advanced degree or 12 or more years experience.



Adding engineer/scientist levels IV and V extends the technical career path at Tektronix for engineers and scientists who wish to advance their technical knowledge and their influence on the technological direction of the company, but without entering management. Engineer/scientist levels IV and V have pay scales corresponding to engineering/scientific managers I and II.

What prompted Tektronix to extend the technical career path?

First, with the new extensions, Tektronix has a true technical career path for engineers and scientists. Now, no one need feel a conflict between (1) wanting a technical career and (2) wanting more money and responsibility, but having to enter management to obtain them.

For many years, Tektronix has had senior-engineer positions placed beyond levels I, II, and III, but they were not ranged. So, a second reason for extending the technical career path was to identify ranges for these new levels and to apply those ranges throughout the company.

A third reason for extending the technical career path is giving recognition to the company's dependence on technical proficiency. Tektronix' financial success depends on advanced technology — much of which is developed here.

Why does a *committee* review nominations to the IV and V positions?

Primarily for two reasons. First, a committee of managers from around the company ensures more consistent application of the level IV and V requirements. Second, level IV and V engineers and scientists affect the whole company, not just the particular department they work for.

Does the Approval Committee have to approve a candidate for a level IV or V job before the manager can hire the candidate?

That depends on whether the candidate already works at Tektronix or will be a new-hire.

If, for example, an IC/Hybrid Process Engineer III applies for a level IV job, the manager can hire the III, but without promotion to level IV until the Committee approves it.

WHAT THE NOMINEE'S MANAGER DOES:

- Contact Jack Piercy (Compensation Department), ext. 7658 (Beaverton).
- Complete the Requirements Checklist.
- Send the nominee's up-to-date resume and the Requirements Checklist to Jack Piercy at d.s. 58-203.
- Appear before the Engineer/Scientist Approval Committee to answer questions about the nominee's qualifications.

Charlie Rhodes Morris Engelson Val Garuts	Electronics Engineer V
Fendall Winston Phil Snow Linley Gumm Gordon Long Jim Woo Rod Bristol Jon Mutton John Popa John Addis	Electronics Engineer IV
Jerry McTeague Ron Robinder Bill Stein	Electron Device Process Engineer IV
Chuck Gold Pel Chow Sam Guthrie Jon Morris Ralph Ulrich Delmer Fehrs Bob Holmes Kris Verma Ralph Rose Gordon Roper	IC / Hybrid Process Engineer IV
Binoy Rosario Ken Schlotzhauer Ian Getreu Carl Battjes George Wilson	Microelectronics Component Design Engineer IV
Bill Price	Software Engineer IV
Kit Bradley George Copeland Jack Gilmore	Software / Hardware Engineer IV
David Bates John Moore Chris King	Physicist IV

Table 1. The Engineering/Scientific Approval Committee named these engineers and scientists to positions IV and V.

For a would-be new-hire, the Committee must approve the candidate for a level IV or V job before the manager hires the candidate.

Is the extended technical career path open to people in Manufacturing as well as product development and research areas?

Yes, it is.

How many IV's and V's has the Committee named so far?

As of July 1979, 35 IV's and three V's. Table 1 lists them.

Who nominates engineers and scientists for the new positions? What's the nomination and approval procedure?

A candidate's manager makes the nomination to the Approval Committee and acts as the candidate's advocate before the Committee. The Committee listens to the manager's reasons for nominating the candidate and then votes on the nominee.

The names and qualifications of nominees approved by the Committee are sent to a group vice president for final review.

So far, about 65% of the level IV and V nominations have been approved.

Who selected the members of the Engineering/Scientific Approval Committee? What were the selection criteria? Do Committee members have a technical background?

Table 2 lists the Committee members. At the request of Bill Walker (executive vice president), Wim Velsink selected the Committee members (in November 1978) for their reputation for good judgement and their experience in managing engineering and scientific groups. Most Committee members have engineering or scientific backgrounds; three have doctorates in engineering or scientific fields.

How often does the Approval Committee meet? How long does the nomination and approval process take?

Ordinarily the Committee meets quarterly, but will meet more often as the need arises.

If the nomination is well-prepared and well-documented and if there is agreement among Committee members, then the nomination and approval process takes about a month. Controversial cases take longer.

Does the Approval Committee use a quota System? X% of engineers/scientists can be IV's and Y% can be V's?

The Committee does not use a quota system. For a healthy, professional technical community, there probably is an optimum number of engineer/scientists IV and V, but it is difficult to quantify. The committee believes that, at present, Tektronix certainly does not have an excess of IV's and V's.

What happens to a nominee who doesn't receive approval for a level IV position?

The nominee stays at level III.

How soon can the nominee be re-evaluated?

This question has not come up before, so the Committee has no

Continued on page 19

WIRE-WRAP FOR HI-SPEED LOGIC CIRCUITS

Glenna Jones, CAD Wire-Wrap, ext. 5781 (Beaverton).

*In the June **Engineering** News, Glenna discussed the many advantages, in prototype circuit boards, of wire-wrap connections compared to etched circuit board connections.*

In this article, Glenna examines the use of wire-wrap connections for prototype high-speed logic circuit boards — a special problem for circuit designers because such circuits are subject to line-ringing and crosstalk.

Because high-speed logic circuits are subject to line-ringing and crosstalk problems, multilayer etched circuit boards (ecb's) are often more suitable than wire-wrapped boards. On the other hand, wire-wrap prototype boards offer major advantages over ecb's (lower cost and shorter turnaround). Thus, circuit designers should carefully consider adapting special wire-wrap techniques to high-speed logic circuits.

CROSSTALK

Before examining the special techniques, consider the problems of crosstalk and line-ringing. **Crosstalk** is the electrical interference of one signal by another; it occurs when a signal has no proper current path returning to the driving gate. Without a proper return path, the signal will find a way back that may interfere with another signal.

Besides improper return paths, physically parallel transmission lines also produce crosstalk. On a wire-wrapped board, wires running in neat vertical and horizonal channels are very pleasing to the eye, but undesirable electrically because they may create **crosstalk.**

LINE-RINGING

Line-ringing (high-frequency damped oscillation) results from a signal passing along a transmission line either having varying impedance along its length or not being terminated in its characteristic impedance. If the termination's impedance is unequal to the transmission line's impedance, the signal will produce reflections and, thus, ringing. Whether or not the ringing is a problem depends on circuit speed and line length.

Crosstalk and line-ringing cause the same malfunctions: multiple threshold-crossings resulting in unintentional transitions.

TO MINIMIZE CROSS-TALK AND LINE RINGING:

Determine what lines are "long" in your circuit and which are especially sensitive to interference. Optimize package layout to shorten these lines.

Avoid wiring lines in parallel: use point to point wiring instead.

Provide separate return paths for fast signals: use twisted pairs and power and ground planes.

Terminate all long lines in their characteristic impedance.

PREVENTING CROSSTALK

One way to prevent crosstalk on a wire-wrapped board is by using **twisted pairs** (two wires twisted together with each wire, at each end, attached to separate but adjacent points on a board). One wire of the pair carries the signal from the driving gate to the driven gate; the other wire carries the return current. Using power and ground planes is another approach to reducing crosstalk.

Though not as aesthetically pleasing as routed (picture-frame) wiring, point-to-point (crow's-flight) wiring is the best way to prevent crosstalk by keeping transmission lines from running in parallel.

PREVENTING LINE-RINGING

Connecting a resistor between the signal line and the return current path is one way to reduce line-ringing resulting from improper termination. This resistor's value should be as nearly equal as possible to the line's characteristic impedance.

Using twisted pairs assures the signal current will return through a line having a controlled path. The characteristic impedance of a twisted pair remains constant within the pair. (In analog circuitry, twisted pairs can shield low signal levels from electromagnetic interference.)

A "long" line is one that rings with an undershoot amplitude greater than 15% of signal voltage change. Thus, the length of line that will produce maximum acceptable ringing is calculated by:

$$\text{Length} = \frac{T_F}{2 \times T_{pd}}$$

T_F is the falltime of the signal and T_{PD} is the line's propagation delay (the reciprocal of the speed at which signals travel on the line). The propagation delay varies from about 1.4 nanoseconds per foot, for twisted pairs in a wire-wrapped board, to about 2.2 nanoseconds per foot for lines between ground planes in a multilayer etched circuit board. Table 1 shows typical rise- and falltimes for commonly-used logic circuits.

Calculating from the values in table 1, the maximum ranges of line lengths that will prevent excessive line-ringing are shown in table 2.

Only signals especially sensitive to crosstalk need be restricted to the lengths shown in table 2.

The figures in table 2 are approximations. *Fast circuit* and *long lines* are relative terms. A circuit designer must consider additional

CIRCUIT TYPE	AVERAGE T_R or T_F
TTL	7ns
SCHOTTKY TTL	3ns
10K ECL	2ns
100K ECL	0.9ns

Table 1. Typical risetimes and falltimes for commonly-used logic circuits.

CIRCUIT TYPE	WIRE LENGTH @ 1.4ns/ft. (WIRE WRAP)	WIRE LENGTH @ 2.2ns/ft. (MULTILAYER)
TTL	30"	19"
SCHOTTKY TTL	13"	8"
10K ECL	9"	6"
100K ECL	4"	3"

Table 2. Shown here are the maximum line lengths that will prevent ringing.

factors such as noise immunity and clock speed.

A circuit designer must treat a circuit with a particular risetime or falltime as a high-speed circuit if the line it is driving is "long." After determining which lines are long or particularly sensitive, the designer can optimize component placement on the board to keep the lines short.

One approach to placement is to first assign alphanumeric designations to integrated circuit packages on the schematic and then cross-reference those packages to components on the board.

Start the arrangement with the packages that are directly connected to the input-output connector fingers or terminal pins. Arrange these packages either by sketching them or by dropping sockets into place on a blank board.

With the peripheral logic selected, look for clusters of integrated circuits on the schematic. Logic systems usually include subgroups of logic circuits; on schematics, the subgroups are recognizable by the many interconnections between their packages. Conversely, these subgroups have fewer connections to other areas of the schematic.

Place the subgroups in the arrangement you've started, keeping them visibly separated. Build outward from the subgroups, looking for opportunities (such as a separate, common IC, or a signal linking two groups together) to tie them together. Reposition and internally rearrange the subgroups if needed, but treat them as a unit.

OTHER AIDS

There are three other techniques that help the designer adapt wire-wrapped boards to high-speed logic circuits.

First, use electrolytic and disc capacitors with resistors or inductors for decoupling. Don't avoid using these as a design shortcut just because the board is a quick-turnaround, early design. Decoupling-networks minimize power distribution problems by providing isolation between circuit supplies. In addition, bypass capacitors (which are used adjacent to the device) provide a lower impedance on the power supply for high frequency signals. To keep the lead inductance low, keep the capacitor leads short.

A second technique is placing ferrite beads on twisted pairs to help suppress crosstalk (the beads suppress common-mode signals on the pairs).

A third technique for adapting wire-wrapped boards to high-speed logic circuits is avoiding wire-wrapping power and ground connections (because wires act like inductors). Instead, use power and ground tabs that slip over a component lead and strap to an adjacent bus. (To obtain these tabs, call Henry Bahrs on ext. 7988; the part number is CM1699B). In addition to these tabs, another option is to use wire-wrap boards that have power and ground planes. Several types are available within Tektronix and many are available from vendors (call Glenna Jones on ext. 5781 for more information and for part numbers). □

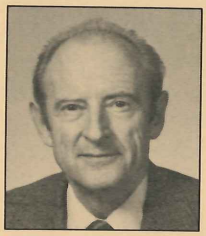
CAD WIRE-WRAP NEWSLETTER

The CAD/Wire-Wrap Group publishes, as the need arises, the **CAD Wire-Wrap Newsletter** which describes developments in CAD wire-wrap at Tektronix and related news such as the use of component carriers.

To receive the **CAD Wire-Wrap Newsletter,** send your name, delivery station and payroll code (required for processing the mailing list) to LIST, Glenna Jones, 50-126.

PATENT RECEIVED : No. 4,123,129

MODULAR ELECTRONIC INSTRUMENT CABINETS LOWER COSTS



Marlow D. Butler, Component Development Group (Tektronix Laboratories), ext. 7046 (Beaverton).

The modular packaging system (MPS) shown here provides different-sized packaging units with common parts and requires fewer fasteners than were used in previous instrument packaging systems.

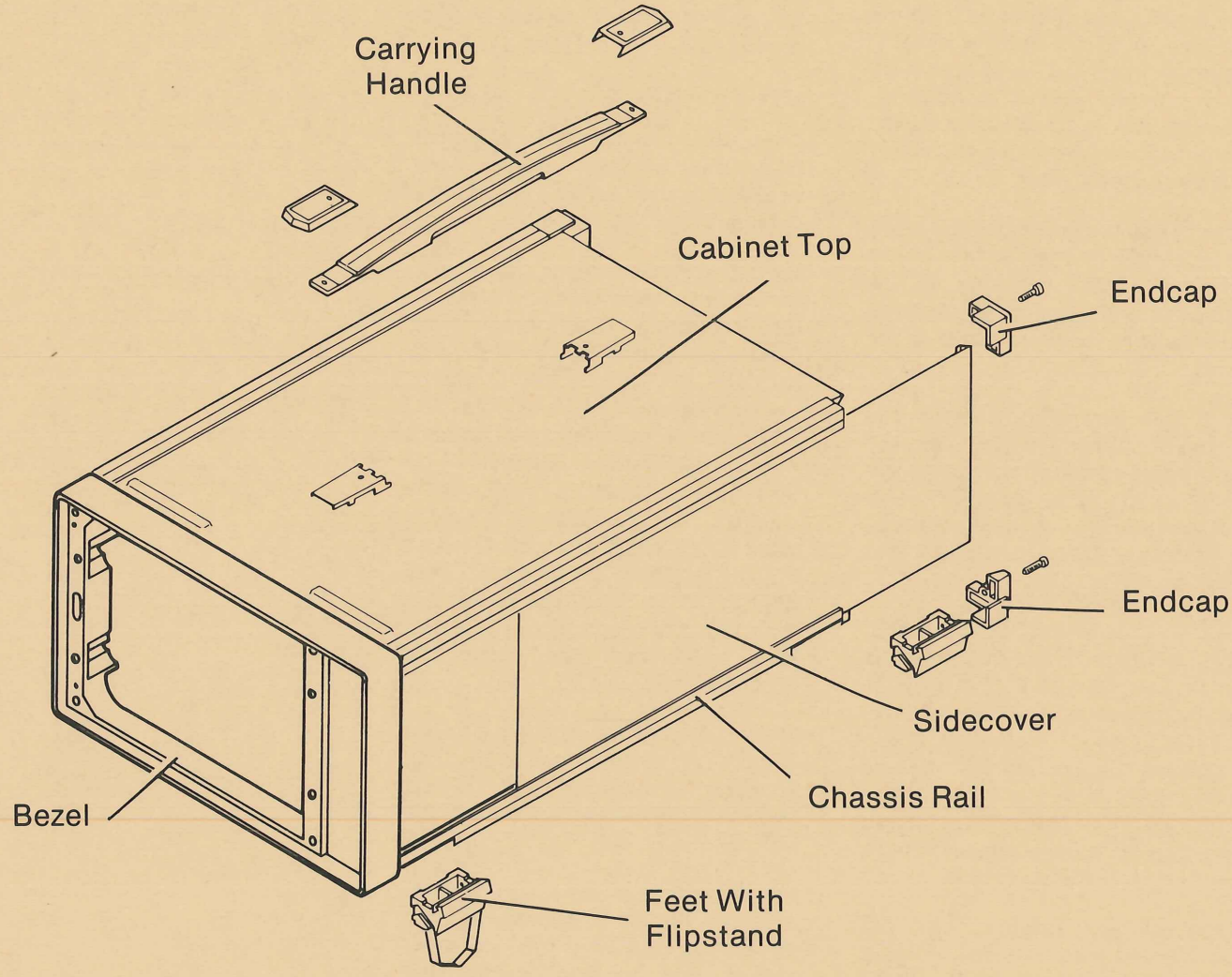
Compatible with the electronic industry's standard 19-inch rack cabinet, MPS packages are available in standard cabinet heights of 1¾ inches, 3½ inches, 5¼ inches and so on in 1¾-inch increments. MPS units are available in half-rack and full-rack widths, and (when required) one-sixth, one-third, and two-thirds rack widths.

For monolithic instrument applications, the MPS is a rack-and-stack system as units may be stacked or positioned side-by-side. Units can be locked together with either metal or plastic strips.

MPS units use common parts: structural parts, feet, flip-stands, handles, covers, and crt bezels. The crt mounting system suspends the crt from the front casting only, thereby not requiring rear support for either the crt or the shield. The basic MPS unit requires only 16 fasteners instead of the average 38 used in previous systems.

A section of the Tektronix Mechanical Parts Catalog containing MPS parts will be updated with each issue. Technical Standards is developing an MPS standard for uses of MPS.

Two Tektronix products using MPS packaging were released in 1978: the 634 Video Display and the 620 Display Monitor. □



PROFILE

AUTOMATED INSTRUMENT COMPATIBILITY EVALUATION GROUP

AICE Engineers want to help solve your GPIB interfacing problems.

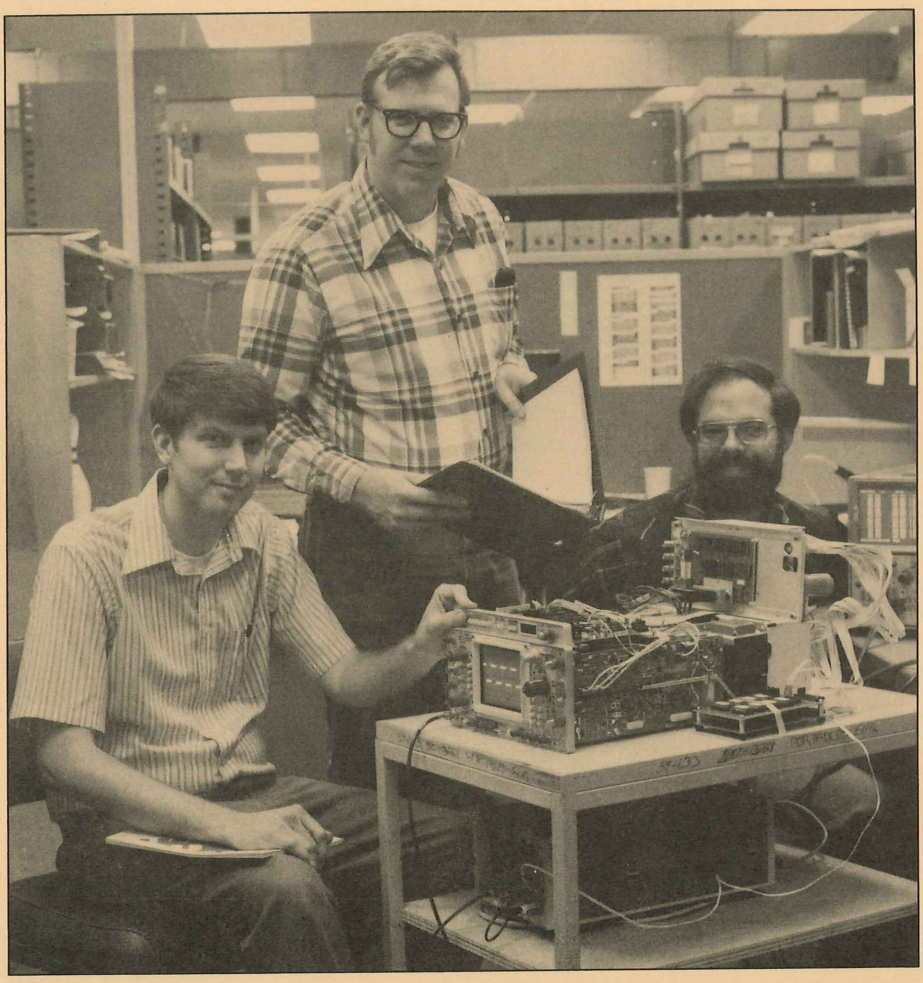
The Automated Instrument Compatibility Evaluation Group is a focal point for solving problems during the development of remotely-programmable instruments. The group's immediate goal is to insure compliance with the GPIB (IEEE-488) Standard and the Tektronix Codes and Formats Standard.

AICE's initial contact with product designers should be early in the design phase. This allows AICE personnel to take a brief look at the product to make sure it is compatible with other Tektronix programmable instruments; potential compatibility problems can be more easily dealt with at this stage. Also, a working relationship is established between AICE and designers, making later formal evaluations run more smoothly.

AICE does formally evaluate new products during both the Evaluation (A) and Verification (B) phases and whenever there are significant firmware changes.

Having developed a set of standardized device-independent tests, AICE engineers Bob Cram, John Burgess, and Steve Coan are continually modifying and expanding their methods. Controllers now available to the group are:

- Tektronix 4051 and 4052 BASIC computing systems
- Hewlett-Packard 9825A desktop computer
- Tektronix CP 4165
- Interface Technology 488 Analyzer
- Commodore PET 2001 personal computer



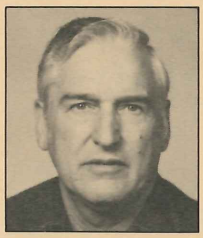
AICE members Bob Cram, Steve Coan, and John Burgess aim to start new product compatibility tests early in the design phase. These tests insure compliance with the GPIB Standard and Tektronix' Codes and Formats.

A Hewlett-Packard System 35 desktop computer is budgeted for later in the year.

Part of Measurement Standards under Standards/Maintenance Support, AICE members welcome suggestions for additional tests and comments on current tests and how they may improve their service.

If you're developing a new product, call Bob Cram at ext. 5397 or drop by d.s. 58-188. □

MINIMIZING ECB PRODUCTION COSTS



Don Branda, Business Analysis, ext. 7022 (Beaverton).

Engineers and draftspersons can minimize costs by properly utilizing standard etched circuit board flats. The tables on this page enable you to calculate the maximum number of boards per standard flat.

A standard flat (a large laminated sheet from which individual boards are cut) is 12 inches by 18 inches. Because circuit-board processing uses up a portion of each flat, circuit boards can't be designed using simple fractions of the standard flat size, such as 6 inches by 9 inches. Instead, etched circuit boards (ecb's) must be designed using the board dimensions shown in the tables on this page. (You may want to clip the tables out and post them for easy reference.)

To determine the maximum number of boards available in a flat, find the board length in the length column and the board width in the width column, and then multiply the corresponding image numbers found in the left-hand column. You may obtain more boards from a flat by reversing width and lengths: find the width in the length column and the length in the width column and multiply the image numbers as described above. Use whichever combination obtains the most images.

The dimensions for the proposed board must always be the same or smaller than the ones listed in the tables. (Odd-shaped boards can be rotated on a flat to obtain more images.)

For example, suppose a proposed board is a one- or two-sided circuit board, 2.180 inches by 1.600 inches. By reducing the figure of the shorter side by only .005 inches, it becomes a standard Tektronix size, 1.595 inches. Here's how to obtain the number of boards per flat:

- 2.180 in the width column indicates 5 images.
- 1.595 in the length column indicates 10 images.
- 5 times 10 equals 50 images per flat.

In this example, the user finds the board width in the length column and the board length in the width column to obtain a greater number of boards per flat.

The standard sizes calculated by using these tables are not valid for polysulfone or tab-routed boards. For some designs, larger board and flat sizes can be negotiated with Electrochem. Contact Charlene Ascher, ext. 7027 (Beaverton), or your department's Electrochem liaison for assistance.

For more information, call Don Branda at ext. 7022 (Beaverton) or Cam Kines at ext. 6103 (Beaverton). □

STANDARD CIRCUIT BOARD FLAT-SIZE REFERENCE CHART

1 & 2 LAYER BOARDS			MULTI-LAYER BOARDS		
IMAGES	LENGTH	WIDTH	IMAGES	LENGTH	WIDTH
1	17.300	11.500	1	16.375	11.500
2	8.575	5.675	2	8.113	5.675
3	5.667	3.733	3	5.358	3.733
4	4.213	2.763	4	3.981	2.763
5	3.340	2.180	5	3.155	2.180
6	2.758	1.792	6	2.604	1.792
7	2.343	1.514	7	2.211	1.514
8	2.031	1.306	8	1.916	1.306
9	1.789	1.144	9	1.686	1.144
10	1.595	1.015	10	1.503	1.015
11	1.436	.909	11	1.352	.909
12	1.304	.821	12	1.227	.821
13	1.192	.746	13	1.121	.746
14	1.096	.682	14	1.030	.682
15	1.013	.627	15	.952	.627
16	.941	.578	16	.883	.578
17	.876	.535	17	.822	.535
18	.819	.497	18	.768	.497
19	.768	.463	19	.720	.463
20	.723	.433	20	.676	.433

Dimensions shown are in inches.

PUBLISHING OR PRESENTING A PAPER OUTSIDE OF TEK?

All papers and articles to be published or presented outside Tektronix must pass through Technical Communications Services for confidentiality review. TCS helps Tektronix employees write, edit and present technical papers. Further, the department interfaces with Patents and Licensing to make sure that patent and copyright applications have been filed for all patentable and copyright-able material discussed in the paper or article.

For more information and for assistance in producing your paper, call ext. 6795. □

COMPUTER CONFERENCE MAY SPEED STANDARDS ACCEPTANCE

The Electronic Industries Association (EIA) is evaluating a world-wide computer conferencing system that may ultimately open communication among high technology centers and, as a result, speed acceptance of proposed industry standards.

Computer conferencing is a means of exchanging information via a common computer.

The computer conferencing program is geared toward people who design and develop electron devices such as cathode ray tubes, integrated circuits, microprocessors, and peripheral interface devices. For Tektronix, the program's success would allow those interested in establishing device standards to (1) speedily determine what is being discussed by the industry and (2) easily poll co-workers for their opinions.

In addition, computer conferencing would simplify registering new devices and assigning device type numbers. A company's engineering representative simply logs on the conference computer and enters the relevant data for a new device. The computer then compares that data with all previous records and identifies any similar device already registered. If no similar device has been registered, the computer assigns a type number to the new project.

Since the EIA, parent body of JEDEC (Joint Electron Device Engineering Council), is examining *world-wide* computer conferencing, the system would enable engineers to determine the status of *all* high-technology devices. The system operates over Telenet, a nation-wide telecommunications network, so no long distance charges are involved. A National Science Foundation grant is covering costs during this evaluation phase; if the system were fully implemented, the cost would be $3.75/hour for hook-up time with no charge for central processing unit time.

An employee from each major area of technology at Tektronix is needed to coordinate use of the system for their area. If you would like to be a coordinator, contact:

Jack Hessman, ex. secretary

Electronic Industries Association
2001 Eye Street, N.W.
Washington, D.C. 20006
(202) 457-4900

FOR MORE INFORMATION

For more information, call Ron Robinder, Materials and Process Development, at ext. 6643 (Beaverton). Ron will be happy to discuss the project with anyone who is interested. □

COORDINATORS NEEDED

Each major technology area at Tektronix needs to be represented to coordinate use of the Electronic Industries Association's computer conferencing system. The following is a list of areas already represented and by whom.

Optical Characteristics of CRT Screens	Ron Robinder
Electron Tube Safety	Richard Nute
RF Interference Filters	Richard Nute
Commercial and Industrial CRT's	Carlo Infante, Pete Keller, Boyd MacNaughton

If you would like to serve as a coordinator, contact:

Jack Hessman, executive secretary
Electronic Industries Association
2001 Eye Street, N.W.
Washington, D.C. 20006
(202) 457-4900

ENGINEERING NEWS PAPER POLICY

Engineering News, Software News and **Forum Reports** are printed on Exact Matte paper. We selected Exact Matte for its exceptional qualities and its low cost (15% less than the Howard Offset paper formerly used).

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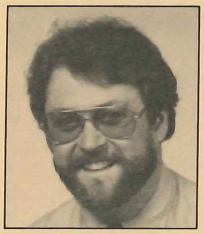
PCC WILL GRADUATE FIRST HARDWARE/SOFTWARE TECHNICIANS IN 1980



Mike Connell, Lab Scopes Marketing (but formerly with Business Analysis), ext. 5123 (Beaverton).

Since the fall of 1977, Mike Connell has assisted Portland Community College in their development of the training program described in this article. If you are interested in enrolling in the program, call Jim Sayer (ext. 5496, Beaverton). If you are interested in hiring a 1980 graduate of the software/hardware technician program, call Bob Connell (Professional Placement) (ext. 7866 Beaverton).

In the Spring of 1980, the first class of software/hardware technicians will graduate from Portland Community College (PCC). These graduates are pioneers in a program that Tektronix helped create: a combination of software and digital-hardware skills with special emphasis on microprocessor-based designs. With these skills, graduate technicians will support software and software/hardware engineers in the same manner electronic technicians support electronic engineers.

A RESPONSE TO A NEED

PCC's software/hardware technician program has its roots in a manpower study that Test and Measurement Business Analysis conducted in the fall of 1977. This study analyzed the mix of technical skills within Tektronix and forecasted needs for the next five years. An out-growth of this study identified the need for a large number of software technicians. Interviews with 15 software/firmware designers and managers produced a list of skills required for software technicians. PCC used this list of skills to design a curriculum for software technicians. Classes began in September 1978.

PCC's software technician program is the first of its kind in the country and has received a lot of attention. David M. Hata, department head of Electronic Engineering Technology at PCC, presented a paper to the Curriculum Committee of the IEEE Computer Society at COMPCON this spring. The PCC administration has received inquiries from prospective students and employees from as far away as southern California.

Beaverton area electronic firms have also responded favorably to this new program. At a recent local American

TERM 1
Software Programming I
Computer Oriented Mathematics I
Business Communications I
Basic Electric Circuits

TERM 2
Software Programming II
Computer Oriented Mathematics II
Business Communications II
Fundamentals of Semiconductors

TERM 3
Software Programming III
Introduction to Numerical Computation
Technical Report Writing
Digital Logic Fundamentals I

TERM 4
Introduction to Microprocessors
Low Level Languages
Basic Communication
Digital Logic Fundamentals II

TERM 5
Language Processors
I/O & Data Communication Programming
Psychology & Human Relations
Peripheral Circuits

TERM 6
Project Management
Operating Systems
Field Project
Advanced Micro Systems

Figure 1. The two-year (six-semester) Portland Community College Software Technician program includes 24 courses with a total of 101 credit hours. Of the 101 total, 66 are for lab work and 35 for lecture.

SOFTWARE PROGRAMMING
This series of three courses teaches software programming concepts and techniques using the PASCAL language. It emphasizes problem solving using top-down design and structured programming. Control techniques include tables, control blocks, transition matrices and recursive procedures. Data structures include arrays, queues, trees, stacks, graphs, and degraphs.

ELECTRONICS AND LOGIC
This series of four courses begins with basic electronic circuits, semiconductor device theory, followed by digital logic theory. The first two courses emphasize fundamental circuit network theory in conjunction with the operational characteristics of bipolar and mos transistors. The last two courses cover Boolean Algebra, combinational and sequential logic design and various state machine design techniques.

INTRODUCTION TO MICROPROCESSORS
This course introduces the student to microprocessors from the hardware side. It includes hands-on experience with a microprocessor kit. It is taught at the same time as the Low Level Languages course which gives the student hands-on experience with a software development system. Both courses include a joint project which emphasizes in-circuit emulation.

I/O & DATACOM PROGRAMMING
This course covers i/o modules for synchronous and asynchronous communications including error detection and correction. It is taught at the same time as Peripheral Circuits which includes the design of interrupt driven i/o, dma and other topics such as a-to-d and d-to-a conversion.

Figure 2. Most of the technical courses in the Software Technician Program fall into one or the other of four major categories shown here.

Electronics Association meeting, Norm Winningstad, chairman of Floating Point Systems praised PCC for developing this program. ESI asked PCC to teach a special section of the complete curriculum at ESI's Scientific Park plant for 17 of its employees. Intel has added the software technician program to a select list of programs Intel has approved for its employee work-study program.

THE CURRICULUM

The two-year Software Technician Program consists of 101 credit hours applied to an Associate of Applied Science Degree. In the first year, students learn basic problem-solving and programming skills and acquire a solid foundation in electronic and basic computer circuitry.

In the second year, the student acquires more hardware and software skills and studies the hardware/software relationship. During the last of the six quarterly terms, the students participate in either a part-time job with a company like Tektronix or in a team project which teaches project management techniques.

Figure 1 lists the courses that make up the software technician program. Figure 2 describes a few of the courses in the program.

PCC is looking for qualified part-time instructors to cover the growing demand for this program. If you are interested, please contact Mike Connell by calling ext. 5123 or writing 39-327. ☐

Continued from page 11

policy, but a year seems a reasonable period provided the nominee's qualifications have changed significantly.

Does the nominee get any feedback from the Committee on where the nominee's apparent weaknesses are?

The Committee's output is a yes-or-no decision. The Committee does not give performance reviews. If the nominee's manager would be interested in discussing reasons with the Committee, or any of its members individually, they would be happy to do so.

Could a level IV or V engineer/scientist who has knowledge in the nominee's field be a part of the Approval Committee?

The nominee's manager is basically the sponsoring person for the nomination. If the manager wishes to bring another individual along as a resource for making a case, the manager is welcome to do so.

A level IV engineer/scientist is in the same pay range as a level I manager, however, the engineer/scientist must go through a much more rigorous evaluation. Does this tend to discourage the engineer/scientist from pursuing a technical career in favor a management career?

At this point, the criteria for selecting engineer IV's and V's are probably more visible than the criteria for selecting level I managers. That doesn't necessarily imply that, in all cases, the criteria are more difficult. ☐

Wim Velsink (chairperson)	**vice president, director, Tektronix Laboratories**
John Bowne	**general manager, T&D Business Unit (IDD)**
Gene Chao	**director, Applied Research, Tektronix Laboratories**
Oliver Dalton	**business unit manager, Portable Oscilloscopes & Accessories (SID)**
Dale DeVries	**Integrated Circuits Manufacturing manager**
Tom Long	**general manager, Communications Division**
Jack Piercy	**senior compensation analyst**
George Rhine	**engineering / scientific manager, Graphic Computing Systems (IDD)**
Aris Silzars	**director, Component Development, Tektronix Laboratories**
Jim Cavoretto	**business unit general manager, SPS / TM 500**

Table 2. In December 1978, Wim Velsink (vice president, director of Tektronix Laboratories) asked these managers to become members of the Engineering/Scientific Approval Committee.

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Volume. 6, No. 7, August-September 1979. Managing editor: Burgess Laughlin, ext. 6795, d. s. 19-313. Assistant Editor: Laura Lane. Cover and graphic design: Joan Metcalf, Joe Yoder. Graphic assistance: Jackie Miner. Typesetting: Jean Bunker. Published by the Technical Publications Department for the benefit of the Tektronix engineering and scientific community in the Beaverton, Grass Valley, and Wilsonville areas.

Why EN?

Engineering News serves two purposes. Long-range, it promotes the flow of technical information among the diverse segments of the Tektronix engineering and scientific community. Short-range, it publicizes current events (new services available and notice of achievements by members of the technical community).

Contributing to EN

Do you have an article or paper to contribute or an announcement to make? Contact the editor on ext. 6795 or write to 19-313.

How long does it take to see an article appear in print? That is a function of many things (the completeness of the input, the review cycle and the timeliness of the content). But the *minimum* is six weeks for simple announcements and about ten weeks for major articles.

The most important step for the contributor is to put the message on paper so that the editor will have something with which to work. Don't worry about organization, spelling and grammar. The editor will take care of those when he puts the article into shape for you.

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