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Random Sampling Oscilloscope for the Observation of Mercury Switch Closure Transition Times

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Abstract—**With the advent of new miniaturized mercury (Hg) switches with reputed transition times of the order of 10 ps, interest has been rekindled in their use in high-speed pulse measurements. Since there is no pretrigger signal available from a Hg switch, normal sequential sampling techniques are not useable to measure the fast Hg switch transition time. For this reason, a new random sampling time base unit was designed to perform these measurements at the low repetition rate of Hg switches. The time base may be used with commercial sampling oscilloscope systems through suitable interconnection terminals or possible interface equipment. It features three selectable time windows of 1 μs, 100 ns, and 10 ns. Using its time magnifier, the fastest sweep rate is 10 ps/cm. A variable trigger lead time control is provided. The trigger sensitivity is 5 mV.**

INTRODUCTION

WITH THE advent of new miniaturized mercury (Hg) switches with reputed transition times of the order of 10 ps [1], interest has arisen in their use in high-speed pulse measurements. It is not possible to directly observe the electrical closure of these miniature switches with the widest bandwidth (dc-18 GHz) sampling oscilloscope available. The problem is that due to the mechanical nature of the mercury switch there is no pretrigger information available to initiate the oscilloscope timing circuits. A signal delay line would not provide an acceptable solution as it would distort the closure waveform. Normal sequential sampling techniques are not usable to observe the small transition time of these mercury switches. For this reason a new random sampling time base was designed to perform these measurements at the low repetition rate of mercury switches (<100 Hz). The time base may be used with commercial sampling oscilloscope systems through suitable interconnection terminals or possible interface equipment. It features three selectable time windows of 1 μs, 100 ns, and 10 ns. Using its time magnifier, the fastest sweep rate is 10 ps/cm. A variable lead time control is provided. The trigger sensitivity is 5 mV. It also includes a phase-locked oscillator to predict the point in time at which the next signal will occur.

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INITIAL MEASUREMENTS USING DELAY LINES

To observe signals that can not be triggered with precision or that do not furnish a pretrigger, the classical technique [2] is to introduce a coaxial cable delay line in the oscilloscope vertical channel to obtain the necessary (35-70 ns) pretrigger lead time (Fig. 1).

A microminiature mercury switch [3] is available which is capable of producing extremely fast transition times [1] upon closure. To observe this fast transition, a system such as shown in Fig. 1 was used. The oscilloscope was a 28-ps nominal transition time sampling oscilloscope. The delay line consisted of a commercial 60-ns large diameter semisolid dielectric coaxial cable. An additional 10 ns of RG-8A/U was also used to give the total 70-ns delay required by the oscilloscope. The response of Fig. 2 was obtained when this system was pulsed by the mercury switch.

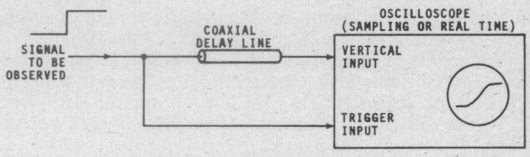

Fig. 1. Classical technique to measure signals that do not furnish pretrigger.

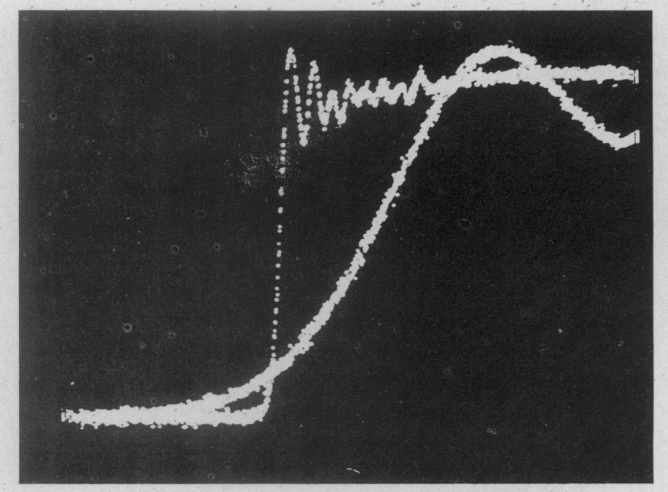

Fig. 2. Observed pulse output from microminiature mercury switch. Horizontal scales are 500 ps/div and 50 ps/div. Measurement system consisted of commercial 60-ns delay line, 10 ns of RG-8A/U, and a 28-ps nominal transition time sampling oscilloscope.

The mercury switch was then replaced by a 20-ps nominal transition time tunnel diode pulse generator. Fig. 3 is the observed response of the measurement system when pulsed by the tunnel diode.

The responses of Fig. 2 and Fig. 3 are almost identical. The 10-percent–90-percent transition times are 0.16 ns. Both responses are completely dominated by the step response of the delay line. These figures show the characteristic response of a coaxial cable having a semisolid dielectric structure [4]. They are characterized by an initial ringing on the top which is caused by the inhomogeneous dielectric which introduces phase dispersion. Some skin effect losses are present also as evidenced by the slow "dribble-up" of the flat top.

The measurement system was also pulsed by a 46-ps transition time tunnel diode. In this case the system transition time was noticeable slower and the magnitude of the ringing was less. From these observations one can conclude that the mercury switch transition time is definitely less than 46 ps and is probably of the order of 20 ps or less.

Random Sampling Approach

An alternative measurement method is to use a different horizontal timing measurement method called random sampling [5]. Operation at a low repetition rate places stringent design requirements on the random sampling time base. Thus the desire to measure 60-Hz mercury switch closures of the order of 10 ps along with the unavailability of a low repetition rate commercial random sampling time base unit led the author to the decision to design a new time base unit. A workable prototype has been built. It is currently undergoing evaluation and minor modifications to improve its performance.

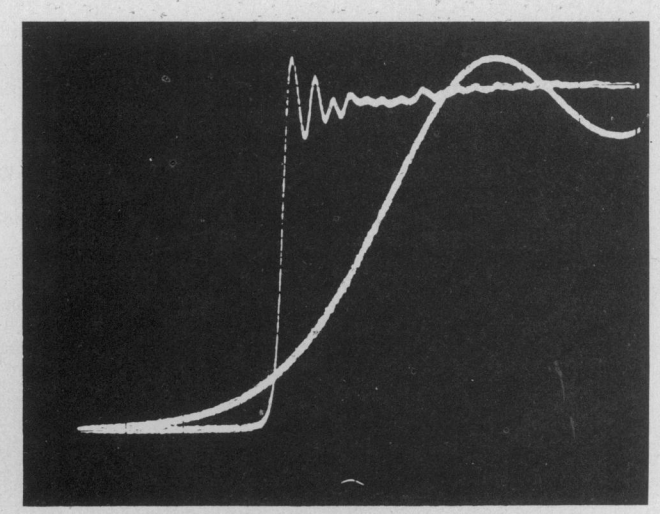

Fig. 3. Observed response of measurement system used in Fig. 2 when pulsed by 20-ps nominal transition time, tunnel diode, pulse generator. Horizontal scales are 500 ps/div and 50 ps/div.

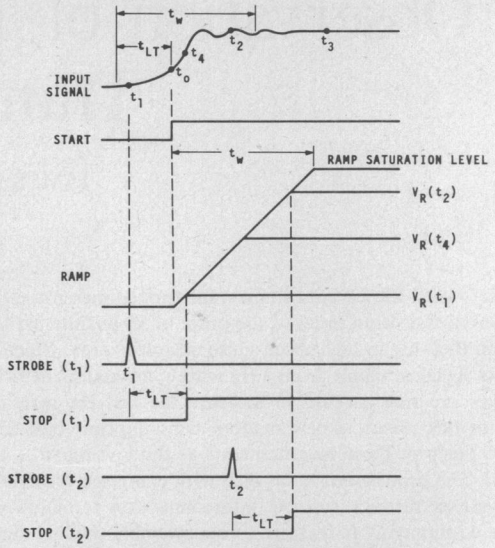

Fig. 4. Basic random sampling timing diagram.

Principles of Random Sampling

The basic principle of random sampling is demonstrated in Figs. 4 and 5. Consider that we are interested in observing a time window t_w framed around an input signal. The point in time at which the input signal is of sufficient amplitude to cause a trigger recognition is at $t = t_0$. However, we are interested in also observing the signal ahead of t_0 for a distance t_{LT}, the trigger lead time. The random sampling scheme provides a means of obtaining this lead time.

At the instant (t_0) a trigger is recognized, a step pulse called START is generated. The START pulse is applied to the linear timing ramp, and it allows the RAMP voltage to begin its run up. Meanwhile a free-running oscillator has been generating a train of STROBE pulses that are completely unsynchronized with the input signal repetition rate. Thus the occurrence of a STROBE pulse within the time window of interest (t_w) is a purely random coincidence. The STROBE pulse is the command to the vertical sampling gate to take a sample of the input signal. Assume now that indeed a STROBE has occurred at

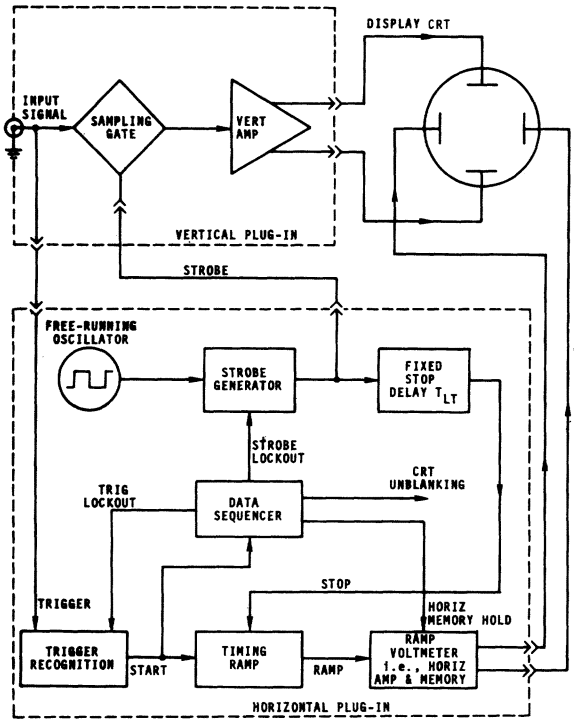

Fig. 5. Basic random sampling block diagram.

time t_1 within the time window and before the trigger recognition. The vertical channel now has a valid data point in the region of interest. Now introduce a fixed delay of length t_{LT} between the occurrence of the STROBE pulse and the generation of a STOP pulse. This delay is chosen to be sufficient to allow the STOP (t_1) pulse, associated with the STROBE at t_1, to arrive at the timing RAMP after it has started its run up at t_0. The STOP pulse terminates the RAMP run up at whatever level it has achieved at the time of the occurrence of the STOP pulse. The stopped RAMP voltage level $V_R(t_i)$ is thus proportional to the instant in time (t_i) at which a vertical sample was taken. The timing ramp is thus a time to amplitude converter. The only item necessary after the ramp is a voltmeter to measure $V_R(t_i)$ and apply it after suitable low-frequency amplification to the horizontal deflection plates of the display CRT. The cycle may now be repeated with another randomly occurring coincidence between the signal and the STROBE, say at t_2, again within the time window but after t_0. If for this event $t_2 > t_1$, the STOP (t_2) occurs later in time, but still a fixed delay t_{LT} after STROBE-signal coincidence at t_2. Thus the RAMP is allowed to run-up to a much larger voltage $V_R(t_2)$. The process is allowed to repeat many times until sufficient data are obtained to permit a relatively complete representation of the input signal. Due to the randomness of the STROBE-signal coincidence, many data points will not be within the window of interest (such as t_3).

The major difference between the classical technique Fig. 1 and the random sampling technique Fig. 5 is the location of the time delay element. In the classical technique, the time delay element is inserted in the input signal channel. It was shown earlier that this disperses the signal and restricts the system bandwidth.

With random sampling the delay element has been moved into the horizontal timing circuit (see fixed stop delay t_{LT}). This eliminates the signal distortion due to the delay line in the vertical channel and allows the full bandwidth capabilities of the sampling head to be utilized. The requirements on the delay element in the time base are much less stringent. The signals within the time base unit are digital logic signals. It is not necessary to preserve with fidelity their waveshape during transmission through the delay element. The only requirement is that the time delay introduced by the delay element be stable and free from any jitter. A coaxial delay line could be used. An electronic circuit is used instead as this allows easy variation of the time delay (t_{LT}) with a dc control voltage.

There are some disadvantages. Random sampling is like everything else in actual practice, i.e., compromises and tradeoffs must be made. The major disadvantage of random sampling as compared to sequential sampling is the longer data acquisition time to obtain sufficient samples to adequately represent the input signal. The probability of a coincidence within the time window of the free-running STROBE and the input signal is quite low particularly if the time window is narrow (for example, 100 ps) and the signal repetition rate is low (for example, 50 Hz). For this reason a prediction circuit is included in the time base. The function of this circuit is to measure the incoming signal frequency and then program the STROBE to occur within the time window (t_w) when the next input signal is predicted to occur.

For mercury switches, which have very large period jitters of typically 0.2 ms, random sampling data acquisition runs of several hours are not uncommon. This thus imposes very stringent long-term stability requirements on the time base.

Design of Instrument

An actual instrument has been constructed to implement the random sampling scheme as shown in the block diagram of Fig. 5. While it was necessary to design many specialized circuits, it was also possible to take advantage of integrated circuits, both digital and linear, to perform many of the more common signal processing tasks.

The resulting instrument is a compact plug-in designed to operate directly as the horizontal time base in a commercially available oscilloscope. The instrument features three switch selectable time windows of 1 μs, 100 ns, and 10 ns with resultant sweep rates of 100 ns/cm, 10 ns/cm, and 1 ns/cm, respectively. Any region within the basic time window may be magnified by factors of X1, X2, X5, X10, X20, X50, or X100. The fastest equivalent sweep rate possible with the 10-ns window and X100 magnification is 10 ps/cm. A variable lead time control is provided to allow positioning of the basic time window to the region of interest relative to the trigger recognition. Lead times that are positive or negative (i.e., simple delay) are included in the control range. The strobe oscillator is a voltage-controlled oscillator that may be zero degree phase locked with the incoming signal. It has a frequency range of 10 Hz–100 kHz. The basic instrument can process data at a maximum rate of 60 kHz. Signals at higher repetition rates are simply counted down to frequencies below 60 kHz. The trigger circuit has an input sensitivity of 5 mV. Trigger controls are provided to optimize the triggering.

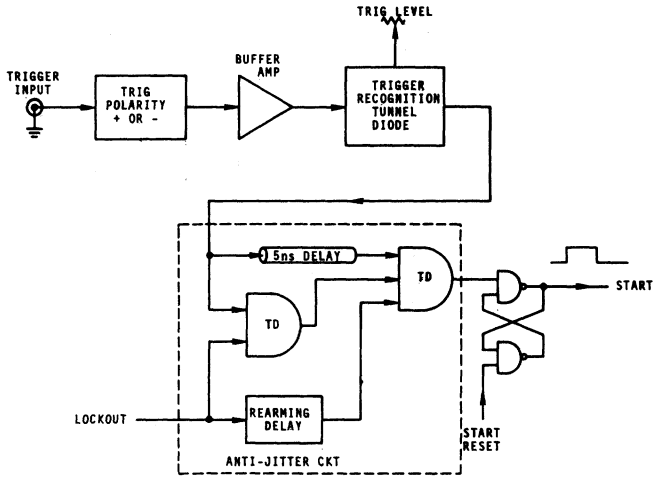

Fig. 6. Trigger recognition block diagram.

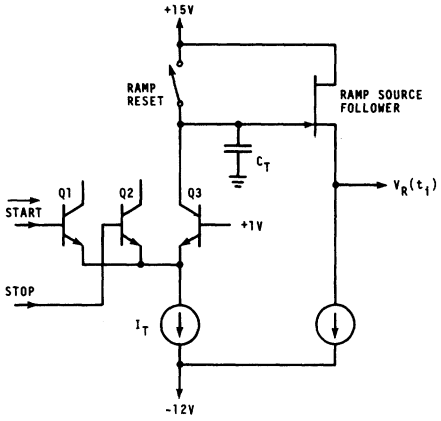

Fig. 7. Timing ramp block diagram.

The resultant data from this instrument and its companion unit, the vertical sampling plug-in, are stored on a bistable storage oscilloscope screen. The operator is thus able to permanently retain the previously measured data and monitor the data gathering until a sufficient amount is obtained to accurately represent the input signal. This is a necessary feature for low repetition rate signals. For these signals several hours may be required to fill the CRT screen.

The salient features of the instrument's circuits are discussed next in the following order: trigger, timing ramp, horizontal amplifiers, strobe, stop delay, and data sequencer.

Trigger

A more detailed block diagram for the trigger recognition circuit is presented in Fig. 6. The basic trigger recognition function is performed by a high speed (70-ps) tunnel diode. The adjustable bias voltage for this tunnel diode is furnished from a well-regulated differential amplifier bias supply [6]. The importance of a highly stable low noise bias for this tunnel diode to insure low jitter operation cannot be ignored. The bias level can be adjusted for monostable operation with low-frequency signals or astable operation to synchronize and count down high-frequency signals. A buffer amplifier is used to provide isolation between external circuits and the very fast trigger recognition pulse.

Following the trigger recognition tunnel diode is the trigger lockout and anti-jitter circuit. The anti-jitter circuit [7] uses tunnel diode logic to prevent false triggering during the rearming of the trigger circuit at the end of the trigger lockout period. A similar idea has been proposed by Nahman and Wigington [8] using coincidence circuits to detect the simultaneous presence of trigger and arming signals and then another gate to inhibit the passage of the delayed trigger. A modification of this has been proposed most recently by Bertolaccini and Cova [9].

A fast transistor-transistor logic (TTL) flip-flop follows the trigger lockout circuit. The output of this flip-flop is the START pulse which is used to start the timing ramp and activate the data sequencer.

Timing Ramp

Fig. 7 is a detailed block diagram of the timing ramp. The basic mechanism used to obtain a linear timing ramp is a constant current source I_T discharging a capacitor C_T. The START-STOP switching action is performed by the emitter coupled logic (ECL) gate. TTL logic signals drive $Q1$ and $Q2$. A fixed potential of 1 V is applied to the base of $Q3$. When the inputs to $Q1$ and $Q2$ are both "0"s, $Q3$ is on and the timing current I_T passes through it discharging C_T. When the input to either $Q1$ or $Q2$ is a "1" then that transistor is on and $Q3$ is off, thus stopping the rundown of the ramp voltage on C_T. The voltage on C_T is read by a JFET source follower. The ramp voltage is reset to + 15 V by a JFET switch.

HORIZONTAL AMPLIFIER

The block diagram for the horizontal amplifier is shown in Fig. 8. The gain and voltage level distribution is also included. With the exception of the discrete transistor final amplifier, fast slewing rate, integrated circuit, operational amplifiers are used throughout. The two memories use MOSFET sampling gates and JFET source followers.

The decay time of the stopped RAMP voltage $V_R(t_i)$ on the 39-pF timing capacitor C_T is quite rapid. Therefore it is necessary to quickly transfer $V_R(t_i)$ to a larger ramp storage capacitor. This function is performed by a X1 follower amplifier and the ramp memory.

The valid data region of the RAMP voltage from 10 V to 5 V is inverted and level shifted by a X(-1) summing amplifier to a -2.5 to +2.5 V signal. In addition this amplifier also introduces an adjustable dc offset when the time magnifier is used in the X2 to the X100 positions. This offset allows the operator to select a particular time position within the basic time window around which he will use the time magnifier.

Following the summing amplifier is a variable attenuator. That is used for the time magnifier function. The total gain in the amplifier chain is 2×10^3. The CRT requires $\Delta V = 100$ V for full-scale deflection. With the time magnifier in the X1 position, an attenuation of 100 is inserted into the chain. For this case a change in the ramp voltage from 10 V to 5 V corresponds to a ΔV of 100 V at the CRT (i.e., full-scale deflection). With the time magnifier in the X100 position, there is

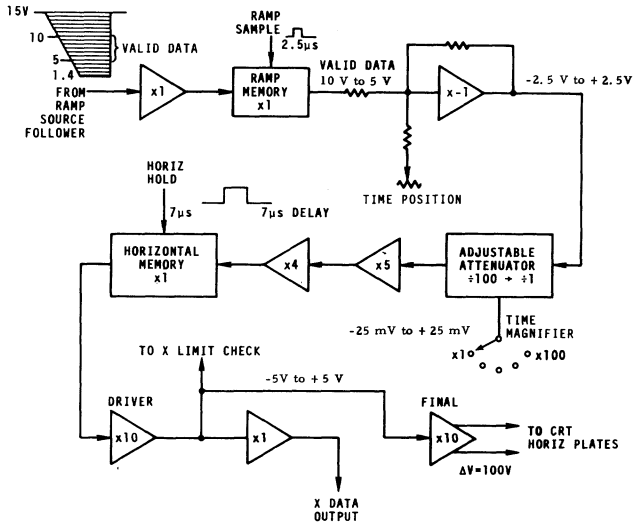

Fig. 8. Horizontal amplifier block diagram.

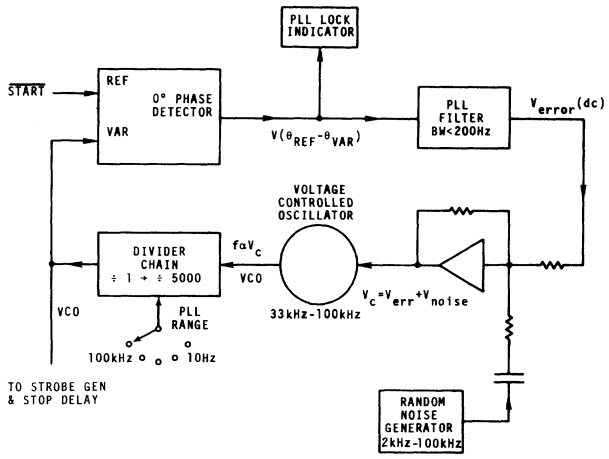

Fig. 9. Strobe predictor block diagram.

no attenuation inserted. In this situation, the ΔV of 5 V in the ramp voltage corresponds to a ΔV of 10^4 at the output of the final amplifier. In actual practice an output of 10^4 V does not occur due to limiting within the amplifier chain. A particular small portion of the ramp voltage is actually linearly amplified by 2×10^3 to give an output ΔV of 100 V. This portion is chosen by adjustment of the time position control.

A horizontal memory is also included in the amplifier chain. Its purpose is to stabilize the data applied to the CRT during the 7-μs unblanking period when a data point dot is being written on the bistable storage oscilloscope screen. There is a 7-μs delay after trigger recognition to allow for the horizontal and vertical amplifiers' settling time. At the end of this 7-μs delay this memory goes to a hold condition for the 7-μs unblanking period.

For proper data handling transient response and long-term stability it is imperative that the amplifiers never be allowed to limit or saturate. Separate fast diode limiters are included with each amplifier to carefully control the maximum signal levels.

Strobe Predictor

In the actual instrument the free-running oscillator, Fig. 5, is replaced by a strobe predictor. Fig. 9 is the block diagram for this circuit. Its function was described earlier in the random sampling theory section. It is basically a phase-locked oscillator [10]. The reference signal into the phase-locked loop (PLL) is the START pulse from the trigger recognition circuit. Thus the PLL attempts to lock in frequency and phase with the incoming trigger signal.

The phase/frequency detector is a TTL integrated circuit [11]. The inputs to this detector are TTL logic pulses. This detector attempts to lock the loop with zero degree phase error between the negative going transitions of the reference and variable inputs.

The voltage controlled oscillator used is also a TTL integrated circuit and is a companion unit to the phase detector. Its basic operating frequency range is 33 kHz–100 kHz. This is compatible with the maximum data rate of 60 kHz of the instrument. For operation at lower frequencies, TTL frequency dividers are inserted to count down the voltage controlled oscillator's basic frequency. The output of this divider chain is the variable input to the phase detector and also the VCO drive signal for the strobe generator and the stop delay circuit.

A low-pass filter is also in the loop. It is used to improve the PLL performance. A second-order active filter is used [10]. The PLL natural frequency is 100 Hz or less depending upon the range in use. A damping factor of 0.7 is used to provide optimum damping.

With the PLL locked to an incoming signal, whose repetition rate is extremely stable (such as that derived from a quartz oscillator), no random sampling occurs. The PLL output occurs precisely at t_0 (i.e., trigger recognition). The visual result on the CRT screen is the continuous display of a single dot in the center of the CRT. Thus it is necessary to randomize the occurrence of the predicted STROBE on either side of t_0 in a controlled manner. The technique used to accomplish this is the injection of a controlled amount of random noise onto the dc control voltage that is applied to the voltage controlled oscillator. The mean value of the noise voltage is zero and its lowest frequency component is at least 10X greater than the PLL bandwidth. Thus the injection of this noise into the PLL does not affect the lock characteristics of the PLL. The net result is a random phase jitter of the STROBE centered on t_0. The amount of phase jitter introduced is adjusted to coincide with the width of the time window used. The net result is a greatly increased probability of coincidence of the STROBE with the input signal in the time window as compared to the simple free-running oscillator.

The noise generator consists of the base-emitter junction of a transistor biased into its reverse breakdown region. The low level breakdown noise is amplified 80 dB by a low noise audio amplifier. The passband of the audio amplifier is from 2 kHz–100 kHz.

One other addition is a simple circuit to turn on a LED on the front panel when the PLL is locked.

Strobe and Stop Delay

The strobe and stop delay block diagram is shown in Fig. 10. The TTL input to these circuits is the VCO signal from the

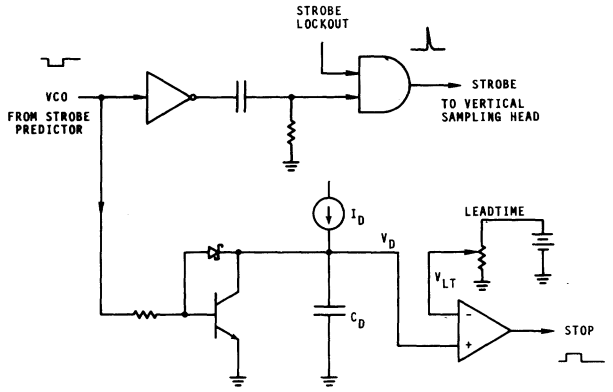

Fig. 10. Strobe and stop delay block diagram.

strobe predicter circuit. To generate the STROBE signal, the VCO signal is simply differentiated and passed through a high-speed TTL gate and routed to the vertical plug-in. A strobe lockout gate is included to prevent the strobing of the vertical channel during the data display cycle.

The strobe delay circuit consists of a linear time ramp generator and a differential comparator. The ramp generator consists of a constant current source I_D charging the delay capacitor C_D. Initially the VCO signal is in the "1" state. Thus the clamp transitor is turned on, clamping the delay ramp voltage V_D near zero volts. The clamp transistor is held just above saturation by the Schottky diode connected between the base and collector. When the VCO signal goes to the "0" state the clamp transistor is cutoff allowing C_D to be charged by I_D. $V_D(t)$ is thus a positive going ramp. When $V_D(t)$ reaches the voltage level V_{LT} set by the lead time control, the differential comparator changes states and produces the STOP pulse. The differential comparator consists of two high-speed differential amplifiers constructed of discrete fast n-p-n and p-n-p transistors.

For minimum timing jitter and excellent long-term stability, it is imperative that the delay current I_D and the lead time voltage V_{LT} be extremely well regulated and filtered from external transients (such as the START signal in particular). These filtering requirements also hold for the strobe generator. There must be a very precisely held time delay between the STROBE and STOP signals. Any jitter between these two signals will be seen as jitter on the CRT. Any crosstalk between the START pulse (and its other related data sequencing pulses) and the STOP and STROBE pulses must be avoided as this will also be a source of timing jitter. Thus proper component and wiring layout and power supply filtering is absolutely essential to minimizing timing jitter.

Data Sequencer

The last block diagram (Fig. 11) to complete the instrument is the data sequencer. The sequencer is composed entirely of TTL integrated circuits. Its purpose is to provide the proper time sequencing of the various data handling functions in the instrument after receipt of a START pulse (i.e., trigger recognition).

When the START pulse goes to the "1" state it triggers a 2.5-μs monostable ($M1$). This 2.5-μs pulse is the RAMP SAMPLE command for the ramp memory. Simultaneous with the leading edge of the 2.5-μs pulse, a 7-μs monostable ($M2$) is triggered. The purpose of this monostable ($M2$) is to allow sufficient data settling time in the vertical and horizontal amplifiers. At the end of this 7-μs delay another 7-μs monostable ($M3$) is triggered. The output of $M3$ is the HORIZ HOLD pulse for the horizontal memory. This 7-μs pulse is also used as the CRT UNBLANKING pulse if the X data is valid, i.e., if the X voltage from the driver amplifier is between -5 V and +5 V. This check is performed by a dual comparator.

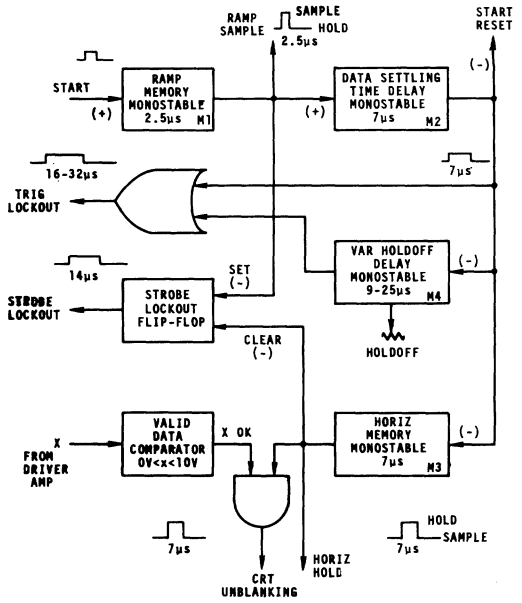

Fig. 11. Data sequencer block diagram where "+" denotes positive going edge triggering and "–" denotes negative going edge triggering.

One additional monostable ($M4$) is used. It is a 9-25-μs variable holdoff delay. It is triggered at the end of the 7-μs data delay. The outputs of $M2$ and $M4$ are combined in an OR gate to give a variable width (16-32-μs) TRIG LOCKOUT pulse.

The STROBE LOCKOUT pulse is provided by a flip-flop. The flip-flop is set to the "1" state at the end of the 2.5-μs RAMP SAMPLE pulse. It is then reset to "0" at the end of the data display period (CRT UNBLANKING).

The START flip-flop is reset to "0" at the end of the 7-μs data delay pulse ($M2$). The resetting of START in turn resets the timing ramp.

Performance

The working prototype of this instrument is shown in Fig. 12. The complete schematics, circuit descriptions, operating and calibration instructions are included in [12]. This prototype has just been completed. It is presently undergoing evaluation tests and some minor circuit changes. It is possible to present at this time the results of some preliminary measurements made with this instrument.

Fig. 13 is a random sampling measurement of the system response of a very fast tunnel diode pulse generator and sampling head combination. The random sampling timing jitter is shown to be of the order of 20 ps.

Fig. 14 is the result of a random sampling measurement of the pulse transition from a very fast mercury switch. This is the same pulse that was measured earlier with the 60-ns commercial delay line, Fig. 2. Fig. 14 was obtained using a 30-ps

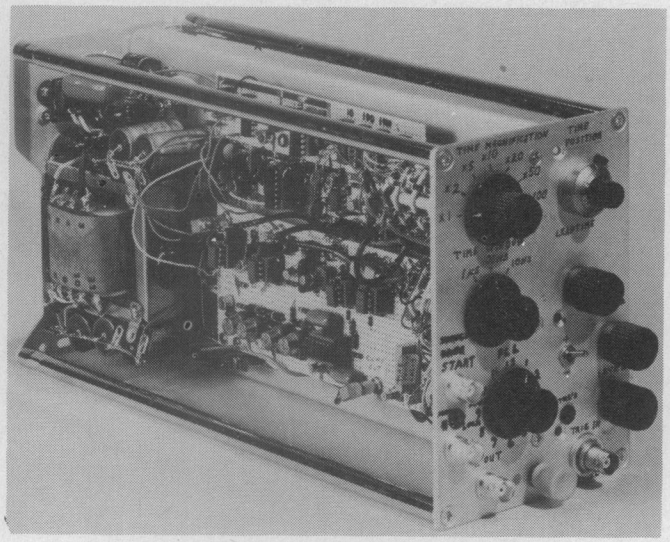

Fig. 12. Prototype of random sampling time base.

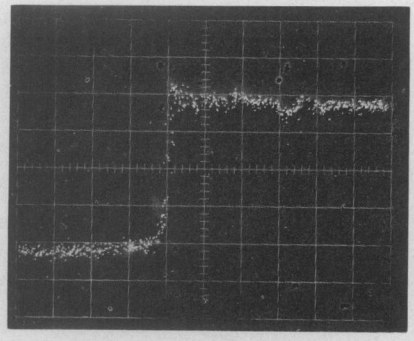

Fig. 13. Random sampling measurement of the system response of a 20-ps transition time tunnel diode, 7-mm 10-dB attenuator, and a 20-ps transition time sampling head. Vertical scale is 20 mV/div. Horizontal scale is 100 ps/div.

(10 percent–90 percent) transition time feed-through sampling head. The pulse was first passed through the sampling head and then into the trigger input of the time base. The pulse to pulse period jitter of this mercury switch was of the order of 0.2 ms. With this excessive jitter, the PLL strobe predictor circuit did not increase the valid data acquisition rate. For this measurement the PLL lock was broken and the VCO was allowed to free-run at 33 kHz. To obtain the data shown in this photograph required a data acquisition run of 2 h. The transition is very nearly a straight vertical line in this photograph. The horizontal time scale is 0.6 ns/div. Thus the transition time is definitely less than 100 ps and probably less than 50 ps. The results of more exhaustive testing of these mercury switches using random sampling and also pulse autocorrelation [13] will be reported in a later communication.

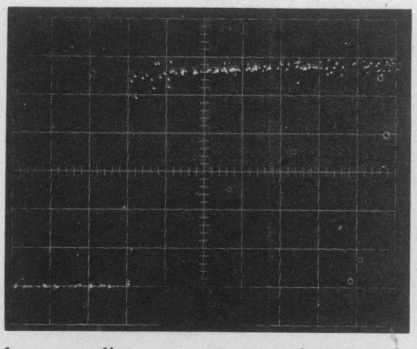

Fig. 14. Random sampling measurement of the pulse output from microminiature mercury switch step generator. Measured with 30-ps transition time sampling head. Vertical scale is 50 mV/div. Horizontal scale is 0.6 ns/div. Data acquisition time of 120 min.

Conclusion

This paper has discussed a particular measurement problem: namely, the determination of the transition time of a microminiature mercury switch closure. Random sampling was proposed as a possible instrumentation technique. The basic theory of random sampling was discussed. The design of an actual random sampling time base was presented. Finally, the preliminary results of a mercury switch transition time measurement were presented. The transition time was found to be definitely less than 100 ps and probably less than 50 ps.

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