TEKTRONIX®

DPO INTERFACE CONCEPTS using the DPO/CP BUS INTERFACE

INSTRUCTION MANUAL

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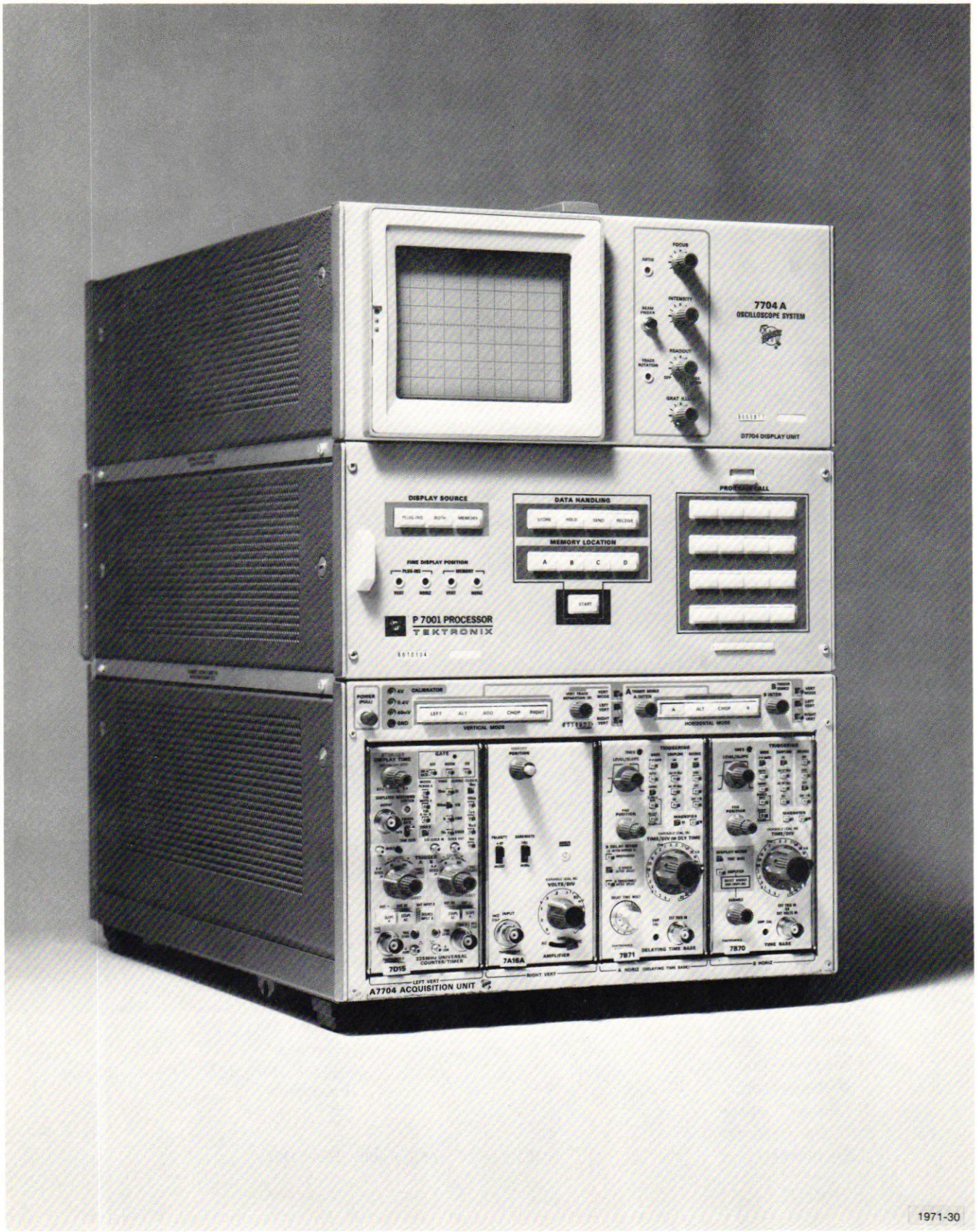


Section 1

INTRODUCTION

This manual has been prepared to assist the programmer in developing a versatile software operating system that fully utilizes the capability of the computer-controlled Digital Processing Oscilloscope (DPO).

Section 2 is somewhat hardware oriented and describes in general the operation of the P7001 Processor. For more detailed information refer to the P7001 Processor Service manual (070-1882-00).

Section 3 contains a general description of the DPO/CP Bus Interface. Refer to the DPO/CP Bus Interface manual (070-1654-00) for more detailed information.

Section 4 lists the controllable functions of the DPO. It contains programming information that will enable the programmer to use the DPO with any type of computer system.

Section 5 provides examples and flow charts that illustrate the procedures for programming your computer to utilize the full potential of the DPO. To fully apply the information in this section, you will need to understand the command structure of your computer.

Two appendices have been included to provide a summary of Device Addresses and Status Word Formats and information on a typical computer/CP Bus Interface. A removable shirt-pocket aid containing a summary of the information is also provided.

Digital Processing Oscilloscope

The Digital Processing Oscilloscope provides a fast, efficient, interactive waveform processing capability when interfaced with a computer. Waveforms are acquired by the 7704A Oscilloscope and then stored in digital format in the internal memory of the P7001 Processor. The DPO's versatility is shown in its multiple waveform storage and message transfer capabilities. PROGRAM CALL buttons on the P7001 Processor front panel provide convenient access to prepared waveform analysis routines in an external computer. By simply pressing a few buttons, the DPO operator can initiate such complex waveform analyses as Fast Fourier Transforms, Integration, or Differentiation. Any specialized processing routines that may be required are easily accessed. Waveform processing results can be returned to the DPO for display on the Oscilloscope CRT. Simultaneous display of scale factors or messages relevant to the processed data keeps the operator aware of important parameters. Fig. 1-1 is a block diagram of a typical DPO/Computer system.

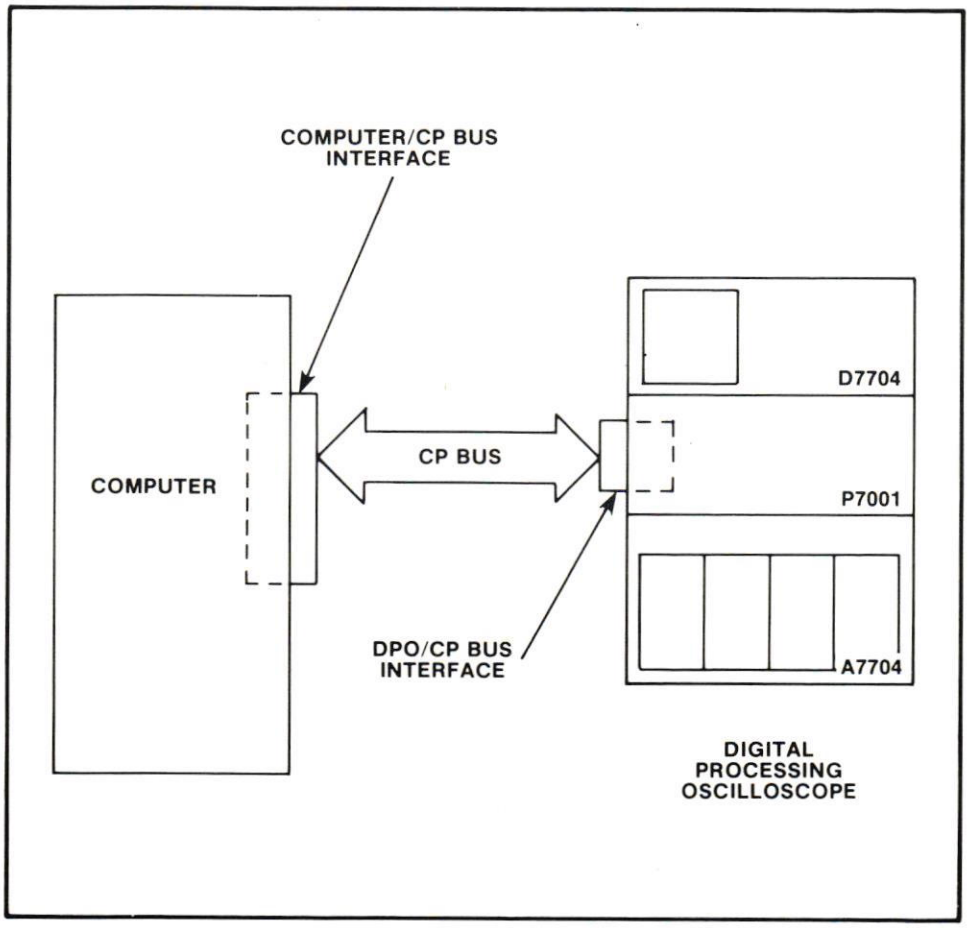


Fig. 1-1. DPO/Computer System.

Section 2

THE P7001 PROCESSOR

The P7001 Processor, sandwiched between the acquisition portion (the plug-ins and their compartment) and the display portion (the CRT and associated drive circuitry) of a 7704A Oscilloscope, makes the 7704A a Digital Processing Oscilloscope. Since the P7001 Processor is the most significant portion of the DPO (in terms of programming), the following discussion is centered on it. The discussion assumes that you are familiar with the DPO front panel. If not, you should read the DPO Operator's manual (070-1599-00) before continuing.

The P7001 Processor consists of a number of circuit cards arranged along an asynchronous communications bus. Fig. 2-1 is a functional block diagram of the P7001.

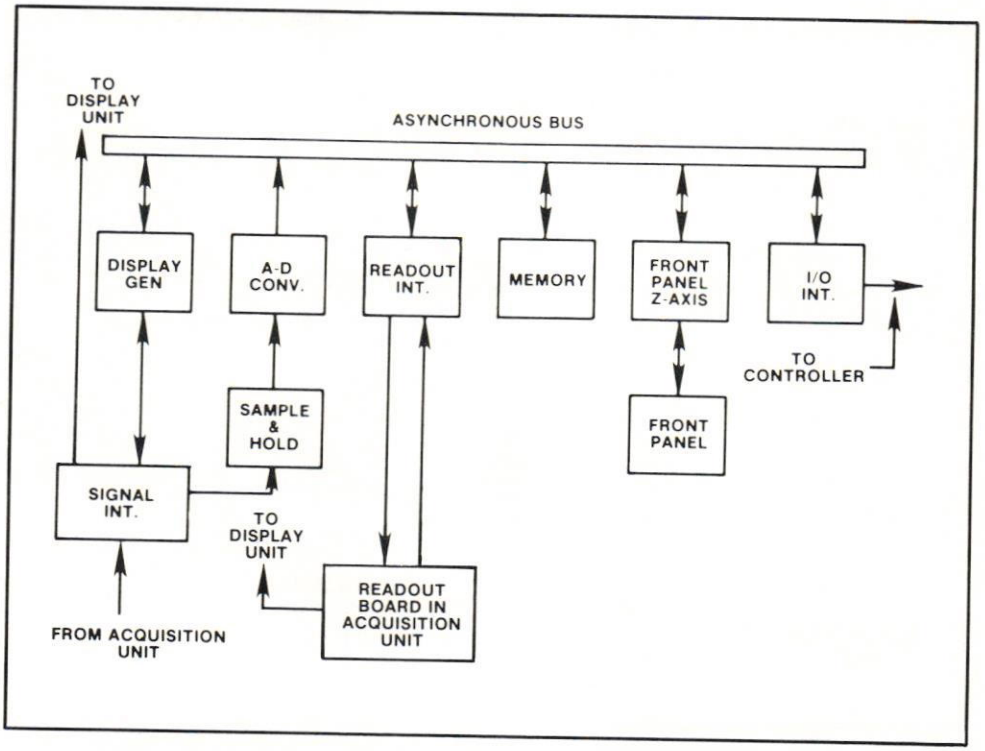


Fig. 2-1. Block Diagram of the P7001.

Signal Interface. The Signal Interface functions like a selector switch. It accepts analog signals from either the plug-ins or the Display Generator, and directs them to the CRT for display. Real-time signals at the plug-ins, or stored signals in the P7001 memory can be displayed. Both can be displayed simultaneously if desired. Three pushbuttons on the P7001 Front Panel (Display Source) allow operator control, and internal circuitry provides for computer control of the Signal Interface.

Sample and Hold. The Sample and Hold circuit continuously samples the analog signals from both horizontal and vertical plug-ins. The samples are taken asynchronously every 6.5 microseconds, regardless of sweep speed. The repetition rate will change for non-valid samples determined by the A-D Converter. The pseudo-random sampling reduces Nyquist sampling errors for repetitive waveforms. A sample of the instantaneous value of the analog vertical signal and of the instantaneous amplitude of the horizontal sweep ramp are taken simultaneously. (Horizontal delayed by about 80 nanoseconds from the vertical sample.) Fig. 2-2 illustrates the process. Both samples are sent to the Analog-to-Digital Converter.

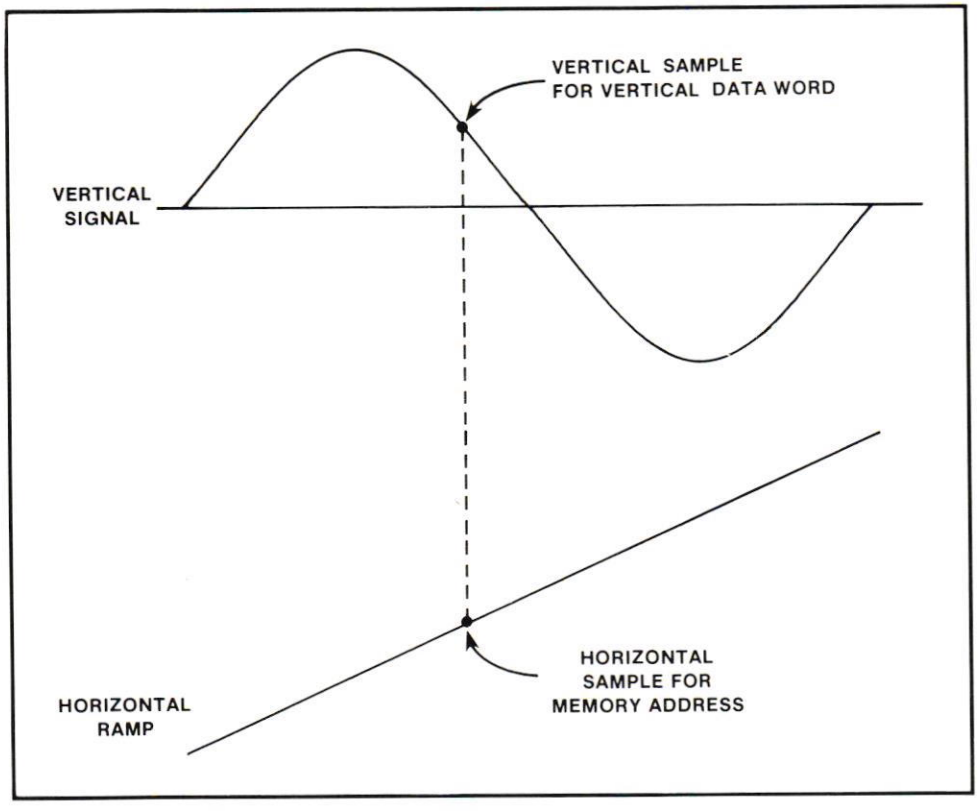


Fig. 2-2. Simultaneous Sampling.

Analog-to-Digital Converter. The A-D Converter accepts the multiplexed analog horizontal and vertical samples from the Sample and Hold circuits, and converts them to binary values. Horizontal samples are converted to 9-bit values corresponding to 512 integer horizontal addresses across the display. Vertical samples are converted to 10-bit values corresponding to 1024 integer values on the display. The reference zero point for vertical values occurs one division below the bottom graticule line, and the 1024th value occurs one division above the top graticule line. The horizontal zero address occurs at the leftmost graticule line, and the 511th at the rightmost graticule line.

If the waveform being sampled is swept at sweep speeds slower then 0.5 milliseconds/division, all 512 possible samples are taken in one sweep. If the sweep rate is faster than 0.5 milliseconds/division, successive sweeps randomly fill in any areas not sampled in the first sweep.

Memory. The information from the A-D Converter is stored in the P7001 memory when a STORE command is received. The command can be issued from the P7001 Front Panel by pressing the STORE and START buttons, or when addressed under program control. The memory usually consists of 4096 10-bit words, divided into sections. Four 512-word blocks are available for waveform storage (waveforms A, B, C, and D). One 512-word block is dedicated to scale factor storage. The scale factor information is in ASCII format. Three other 512-word blocks are available for computer-generated messages. Messages are limited to a maximum of 80 characters displayed at any one time, due to space limitations on the CRT screen.

Readout Interface. The Readout Interface converts analog scale-factor information from the plug-ins to ASCII format for storage in the P7001 Memory. It also performs the opposite function, providing analog information for display from the ASCII information stored in memory. Computer-generated messages stored in the P7001 memory are routed to the Readout Interface on command for display on the CRT. Messages and scale-factor information are displayed on a time-shared basis simultaneously with the stored waveform. Optionally, the readout from the Acquisition Unit can be internally switched to provide a display after a horizontal sweep is completed. This feature is valuable when viewing single-shot events, since it prevents readout time-sharing during the sweep.

Display Generator. The Display Generator functions as a digital-to-analog converter, providing analog information for the display circuitry of the DPO from the digital waveform information stored in Memory. The Display Generator does not use ASCII information. It accesses only those portions of Memory containing waveform data, whether generated by the plug-ins (through the A-D Converter) or by the computer.

The Display Generator can operate in two modes. The normal mode plots the vertical values across the screen as a function of time. The familiar Y-T (Y = amplitude vs T = time) oscilloscope display results. The circuit will also operate in the X-Y mode under program control. With software continually refreshing the display and directing the readout sequence, multivalued functions may be displayed (spirals, for instance). The display generator can also provide a dot pattern rather than the normal vector display. The dot mode is selected with a strap option on the Display Generator circuit card (refer to the DPO Operators manual for specific information).

Front Panel. The Front Panel circuitry of the P7001 allows operator control of some of the P7001 functions. Lighted buttons allow the status of the processor to be determined easily. Pressing many of the buttons causes a status word to be sent to all circuit cards in the P7001. The cards addressed respond by changing their status to correspond to the pressed pushbutton. In addition, the button lights to indicate the change of status.

The Front Panel operates somewhat differently under program control. When the Front Panel is addressed and changed by the computer, most operations affect only the lights at the selected buttons. In order to perform the desired operation, the computer must address both the Front Panel and the affected P7001 circuit cards. For example, if a change from memory location A to memory location B is desired, the Front Panel would be addressed and changed (to change the lights) and then the Display Generator and the Readout Interface would be addressed. The Display Generator and Readout Interface actually perform the mode change, while the Front Panel lights keep the operator aware of the P7001 status.

Section 3

DPO/CP BUS INTERFACE

The DPO/CP Bus Interface provides two-way communication between the P7001 and the Computer Interface via a passive multiwire data cable called the CP Bus. Control and data signals are transferred through the interface on an interrupt basis. Actually, the DPO/CP Bus Interface appears "transparent" to the programmer. It is designed to allow rapid data flow to and from the P7001 Processor with a minimum of software overhead.

Address Strap Options. The DPO/CP Bus is designed to allow up to eight DPO's to be controlled by one computer, via strap options. Each DPO connected to the computer must have a unique address. The address of a particular DPO is user definable, and is selected by exercising a strap option on the DPO/CP Bus Interface card. Located in a plug-in housing at the rear of the DPO (see Fig. 3-1), the Interface card has a "harmonica" plug for address selection. This connector is plugged onto a row of pins that protrude from the board near the aluminum end plate (see Fig. 3-2). The device number is selected by moving the harmonica along the row of pins. For example, a device number of zero would be selected by positioning the harmonica at the leftmost end of the row of pins. A device number of one would require that the harmonica be moved one position to the right (toward the aluminum end plate), exposing one pin to the left of the harmonica. The last DPO on the line must leave the termination resistors connected.

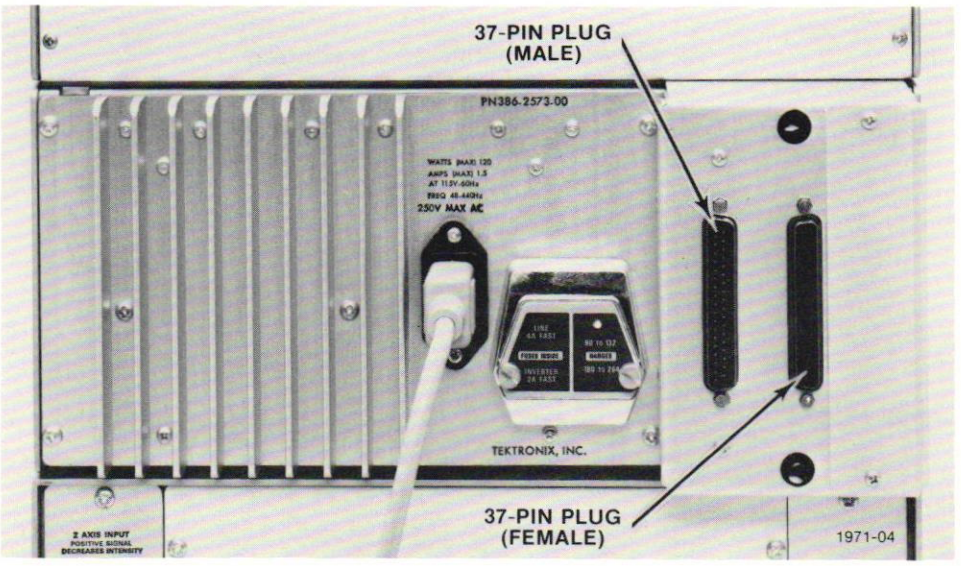


Fig. 3-1. Location of DPO/CP Bus Interface.

Selecting an address for a particular DPO also establishes its priority. If two DPO's request service simultaneously, the instrument strapped to the highest number is serviced first. For example, if instruments number 5 and 7 request service, number seven will be recognized. The binary representation of the selected device number is used both to address the DPO and to identify an interrupting DPO.

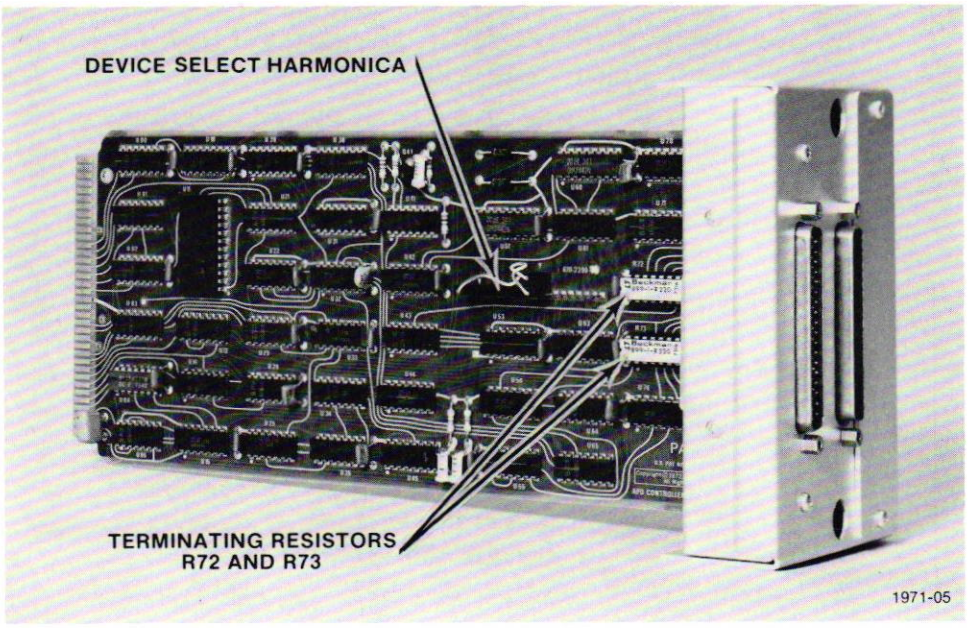


Fig. 3-2. Side View of DPO/CP Bus Interface.

Signal Names

A brief description of the signals required on each pin of the 37-pin connector is listed in Table 3-1.

TABLE 3-1

Signal Names at the Computer Connector J02 & J03 of DPO/CP Bus Interface

Pin No.	Signal Name	Function
1	$\overline{CB0}$	These are bidirectional lines on the common bus that are used to communicate between the DPO and the computer. They are used for both addressing and data.
2	$\overline{CB1}$	
3	$\overline{CB2}$	
4	$\overline{CB3}$	
5	$\overline{CB4}$	
6	$\overline{CB5}$	
7	$\overline{CB6}$	
8	$\overline{CB7}$	
9	$\overline{CB8}$	
10	$\overline{CB9}$	
11	$\overline{CB10}$	
12	$\overline{CB11}$	
13	$\overline{CB12}$	
14	$\overline{CB13}$	
15	$\overline{CB14}$	
16	$\overline{CB15}$	
17	Gnd	
18	Gnd	
19	$\overline{CLR}$	Clear. Sets the interface to an idle state. Sent by computer.
20	$\overline{CLI}$	Clear Interrupt. Indicates the interrupt request has been acknowledged. Sent by computer.
21	$\overline{DRCV}$	Data Received. Indicates data has been received by the DPO or computer. Bidirectional. This signal is in response to Data Sent ($\overline{DSNT}$).
22	$\overline{BQ1}$	Control lines which indicate action to be taken on the bus (set by computer).
23	$\overline{BQ2}$	$\overline{BQ1}$ $\overline{BQ2}$ Action H L Indicates a transfer of data to the DPO. H H Indicates a transfer of data from the DPO. L H Indicates a transfer of address to the DPO. L L Start Read Cycle.
24	$\overline{CBBZY}$	Common Bus Busy. Set by DPO or computer to indicate that some device (DPO and/or computer) is active.
25	$\overline{BS1}$	Bus Select. Indicates the unit number (0 through 7) of the DPO being addressed (set by computer).
26	$\overline{BS2}$	
27	$\overline{BS3}$	
28	$\overline{DSNT}$	Data Sent. Indicates the presence of valid data on the common bus. Bidirectional. Sent by device that is asserting $\overline{CB0}$—$\overline{CB15}$.
29 ↓ 37	$\overline{Gnd}$	

DATA TRANSFER BETWEEN THE COMPUTER AND THE DPO

The sequence of events for sending the address to the DPO from the computer, sending data to the DPO from the computer, the computer reading data from the DPO, and the interrupt sequence are given below. The timing sequences are ideal design parameters for the DPO/CP Bus Interface. Actual timing sequence may vary with type of Computer used.

Sequence for Sending the Address to the DPO from the Computer (Fig. 3-3):

1. The computer puts the address on $\overline{CB0}$ through $\overline{CB15}$, the device number on $\overline{BS1}$ through $\overline{BS3}$, and sets $\overline{CBBZY}$ and $\overline{BQ1}$.

2. The computer waits 0.3 μs for data settling time and sets $\overline{DSNT}$.

3. When the computer sees $\overline{DRCV}$, it releases all lines.

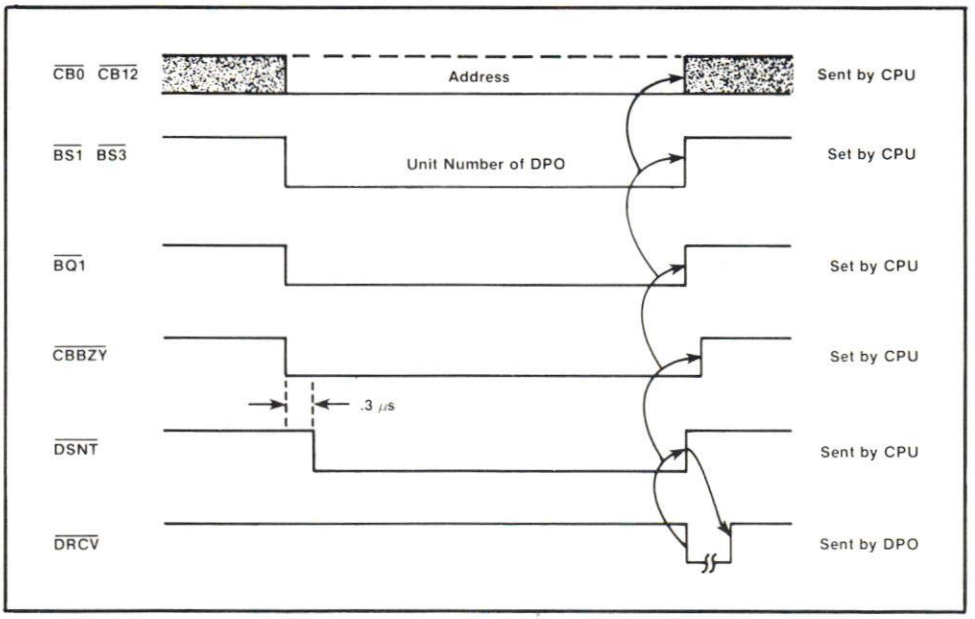


Fig. 3-3. Sending the Address to the DPO from the Computer.

Sequence for Sending Data to the DPO from the Computer (Fig. 3-4):

1. The computer puts the data on $\overline{CB0}$ through $\overline{CB15}$, the device number on $\overline{BS1}$ through $\overline{BS3}$, and sets $\overline{CBBZY}$ and $\overline{BQ2}$.

2. The computer waits 0.3 μs for data settling time and sets $\overline{DSNT}$.

3. When the computer sees $\overline{DRCV}$, it releases all lines.

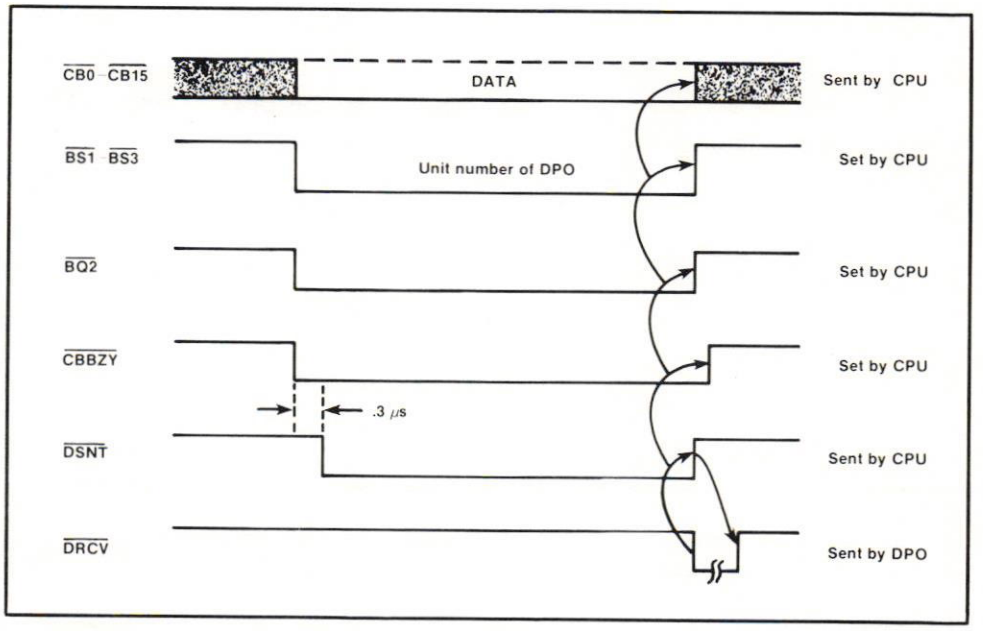


Fig. 3-4. Sending Data to the DPO from the Computer.

Sequence for the Computer to Read Data from the DPO (Fig. 3-5):

1. The computer puts the device number on $\overline{BS1}$ through $\overline{BS3}$, sets $\overline{CBBZY}$, $\overline{BQ1}$, and $\overline{BQ2}$. NOTE: This is a start read cycle.

2. The computer waits 0.3 μs for data settling time and sets $\overline{DSNT}$.

3. When the computer sees $\overline{DRCV}$, it releases $\overline{BQ1}$ and $\overline{BQ2}$ but continues to assert $\overline{CBBZY}$, and $\overline{BS1}$ through $\overline{BS3}$. NOTE: When the DPO sees $\overline{BQ1}$ and $\overline{BQ2}$ released, it will put data on the common bus. The time that DATA is present on the Bus is variable. The signals $\overline{DSNT}$ and $\overline{DRCV}$ are used for keying.

4. The computer waits for $\overline{DSNT}$ from the DPO.

5. When the computer sees $\overline{DSNT}$, it latches the data and sends $\overline{DRCV}$ to the DPO.

6. When the computer sees $\overline{DSNT}$ released by the DPO, it releases $\overline{DRCV}$, $\overline{CBBZY}$, and $\overline{BS1}$ through $\overline{BS3}$.

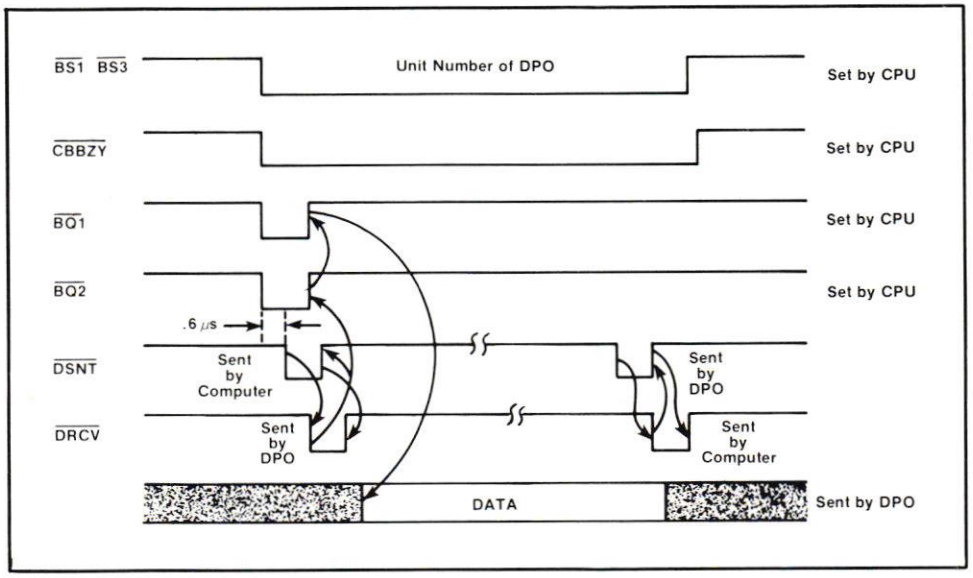


Fig. 3-5. Sequence for the Computer to Read Data from the DPO.

Interrupt Sequence:

1. If $\overline{\text{CBBZY}}$ is not being asserted by any device and the computer detects that one of the $\overline{\text{CB0}}$ through $\overline{\text{CB7}}$ lines is asserted, it encodes the decimal representation of that line ($\overline{\text{CB0}}$ through $\overline{\text{CB7}}$) in the range of 0 through 7. This represents the device number of the interrupting DPO, i.e., Device number 5 will interrupt on $\overline{\text{CB5}}$.

2. The computer is interrupted and the encoded device number is latched.

3. When the computer acknowledges the interrupt, the device code of the interrupting device is placed on $\overline{\text{BS1}}$ through $\overline{\text{BS3}}$ and $\overline{\text{CLI}}$ is asserted for approximately 1 μs.

Section 4

CONTROLLABLE FUNCTIONS OF THE DPO

Introduction

The P7001 Processor in the DPO allows computer control of many DPO functions. As discussed in Sections 1 and 2, the P7001 consists of five functional circuit cards arranged along an asynchronous bus. Four of the cards have specific addresses and related status words that allow their operational mode to be changed by a computer. The fifth card (actually two cards in most cases) is the P7001 Memory. The memory usually consists of 4096 10-bit words, but smaller memories are available. This discussion assumes that your DPO is equipped with the 4K memory. If you have a smaller memory, refer to the DPO Operator's Manual for strapping information.

P7001 Memory

The P7001 Memory is organized in several sections, providing storage for four waveforms, related scale factors, and messages. Fig. 4-1 is a "map" of the memory, with the starting and ending address of each section given in octal.

Waveforms A through D are stored in consecutive memory locations in 512-word blocks. In addition, each waveform has four "fields" associated with it.

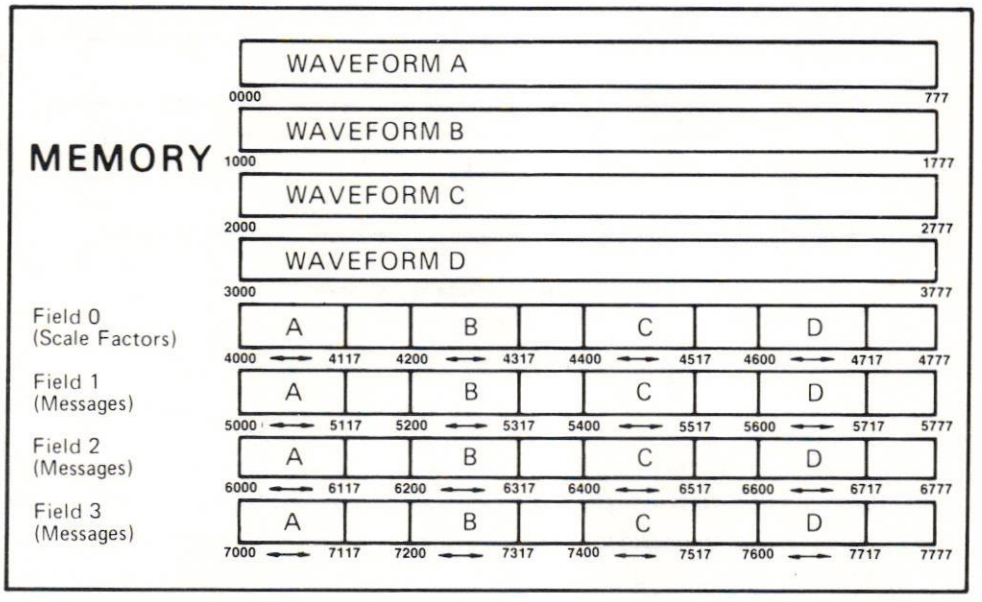


Fig. 4-1. Memory map.

Fields. The field areas of memory are used to store-scale factor information from the plug-ins (Field Ø only) and computer generated messages relevant to each waveform. The Readout Interface circuit card in the P7001 has access to all field locations in memory. Messages stored in the fields are converted from ASCII to analog row and column currents, similar to that generated by the Plug-ins. These currents are then converted to an analog drive signal for the CRT by the Acquisition Unit Readout Board and displayed on the DPO screen.

The display is limited to 80 characters, 40 across the top of the screen, and 40 across the bottom. The 80 character limit results in some extra memory. For example, notice on the memory map that Field 1 includes 512 addresses. An 80-character message for each of the four waveforms requires only 320 memory locations. The extra locations form 50-character "blocks" between displayable fields. These memory locations are available for use by the computer, but the information in them cannot be displayed on the CRT.

More information concerning message display and storage is given in the Readout Interface discussion in this section.

Storing Data. The P7001 Memory is directly accessible for both reading and writing. No status setting or reading is necessary. Once the desired memory address is sent to the DPO, a Read or Write Data operation transfers information from or to that address. The format of the memory data is shown in Fig. 4-2.

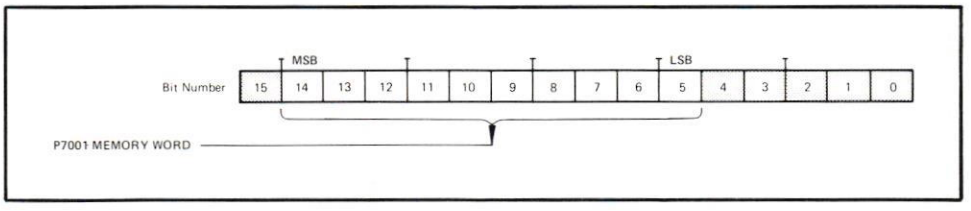


Fig. 4-2. Memory Data Word format.

The P7001 uses a 16-bit data bus. The memory data word includes 10 of those bits, shifted left 5 bits. The data word is used to store either vertical (Y) waveform information (data points) or alphanumeric information for scale factors or messages. The range of the vertical data points is from Ø through 1023, with the LSB in bit 5 of the data word. ASCII information is in the low-order 7 bits of the same data word. In both cases the LSB must be in bit 5 of the data word.

Setting the P7001 Status

The P7001 front-panel pushbutton operations — selecting display sources, storing waveforms, sending waveforms, etc. — all have the effect of setting the status of one or more of the P7001 circuit cards. These manual operations (and some additional ones) can be performed under program control.

There are four P7001 circuit cards that can have their status set. They are:

1. Analog-to-Digital Converter.
2. Readout Interface.
3. Display Generator.
4. Front Panel.

To set the status of a particular card, the DPO is first addressed through the Computer/CP Bus Interface. Then the P7001 Card address is then loaded into the DPO/CP Bus Interface Address Register. The Status Word is then sent to the Addressed Card. The Addressed Card responds to the status word, when received, by changing its operational mode and acknowledging the exchange on the bus.

Fig. 4-3 is a map of the device addressed (in octal) in the P7001 Processor. Notice that a range of addresses is available for every device. This range is located above the 4K memory addresses. The area in between is available for future use. Although the circuit cards will respond to any address within their range, it is recommended that the lowest address be used.

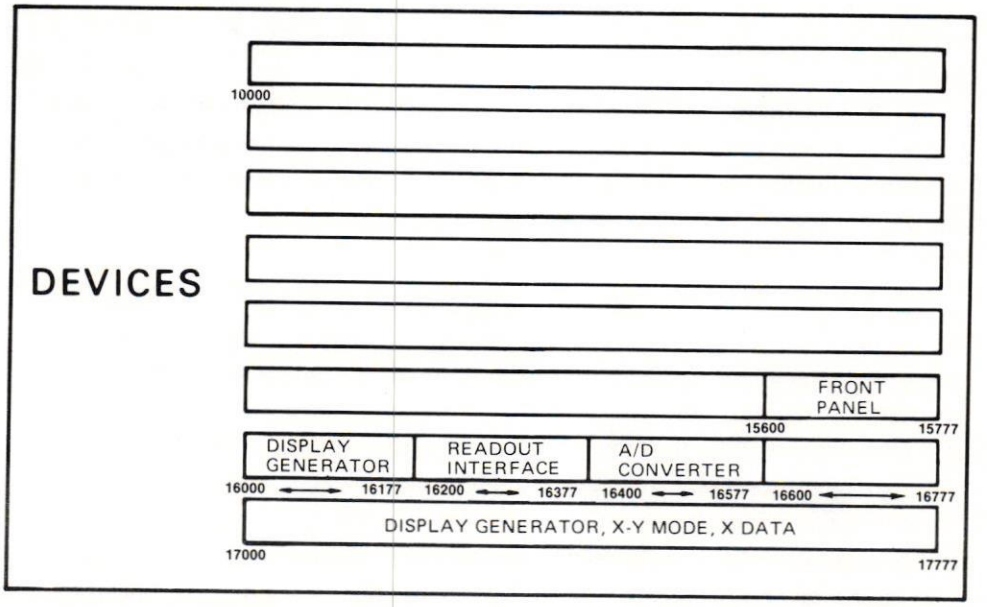


Fig. 4-3. Device address map.

Status Word Formats

Analog-to-Digital Converter. The analog-to-digital converter converts the analog signals from the plug-ins to digital information. The digitized waveforms are stored in one or more of the four memory locations (A, B, C, or D) as determined by the A-D Converter status word. Fig. 4-4 illustrates the format of the A-D Converter status word, and lists the bit combinations required.

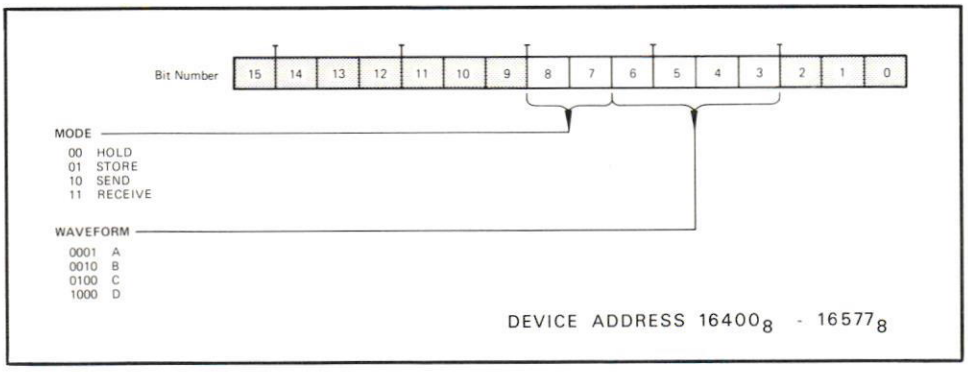


Fig. 4-4. Analog-to-Digital Converter Status Word.

The MODE bits of the A-D Converter status word determine whether or not the converted samples are stored in memory. Turning only bit 7 on initiates the STORE operation, with storage occurring in the memory array(s) specified by the WAVEFORM bits. The WAVEFORM bits are not mutually exclusive, allowing any combination of waveform locations to be selected. If a single waveform is to be stored in more than one memory array however, the destination array is restricted to A and B if the input is from the left vertical plug-in, or to C and D if the input is from the right vertical plug-in. Storing multiple waveforms requires some additional precautions. For more information, refer to the DPO Operator's manual (070-1599-00). Turning bits 7 and 8 off returns the A-D Converter to the HOLD mode, stopping the STORE operation. The SEND and RECEIVE bit combinations are decoded as HOLD. They have no other effect on the A-D Converter.

The A-D Converter through the Sample & Hold card simultaneously samples the horizontal sweep ramp and the vertical input signal. The horizontal sample determines the memory address, while the vertical sample determines the value to be stored. The dynamic range of the sampling circuitry exceeds the 512 horizontal addresses and the 1024 vertical values that can be produced by the A-D Converter. Any waveform values that exceed the limits of the A-D Converter are converted as end point values (see Fig. 4-5). For example, any vertical data values greater than 1023 are converted to a 1023 value. The horizontal end points are subject to the same compression. In summary, the end points of the converted waveforms may not correspond to the end points of the sampled waveforms, and should be considered invalid. Software can easily extrapolate the

horizontal end points during processing. If vertical compression occurs, the vertical sensitivity of the plug-in producing the signal should be reduced, or the positioning corrected. Remember that the vertical Ø point occurs one division below the bottom graticule line. The 1023 point occurs one division above the top graticule line.

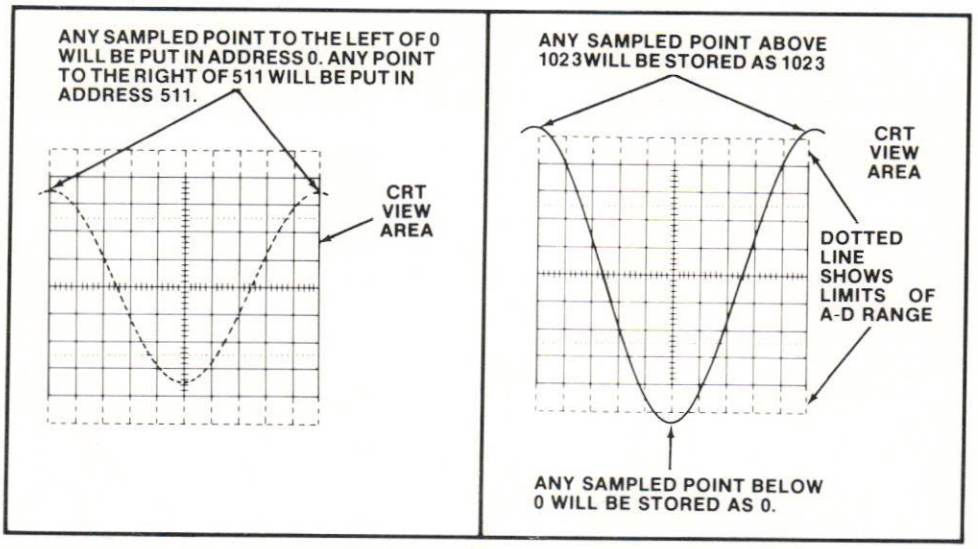


Fig. 4-5. End point value conversion.

The A-D Converter through the Sample & Hold card asynchronously samples the horizontal and vertical data every 6.5 microseconds/division. With this sampling rate, all memory locations can be filled in a single sweep at sweep speeds slower than 0.5 millisecond/div. Single sweeps at faster sweep speeds will not fill all memory locations, and the resolution of the stored waveform may be reduced.

Repetitive waveforms need not fill all memory locations in one sweep. Successive sweeps fill any missing locations until the memory is full. The memory is then repeatedly updated during each sweep until the storing operation is stopped.

As the sweep speed increases, however, the number of samples taken per sweep is reduced. It takes more sweeps to fill the memory, and more time, too. If the repetition rate of the signal is low, the time required is increased even more. The time required to fill the memory at a given sweep speed and signal repetition rate is given in Fig. 4-6. Software should detect the sweep speed and determine an appropriate STORE interval whenever initiating a STORE operation.

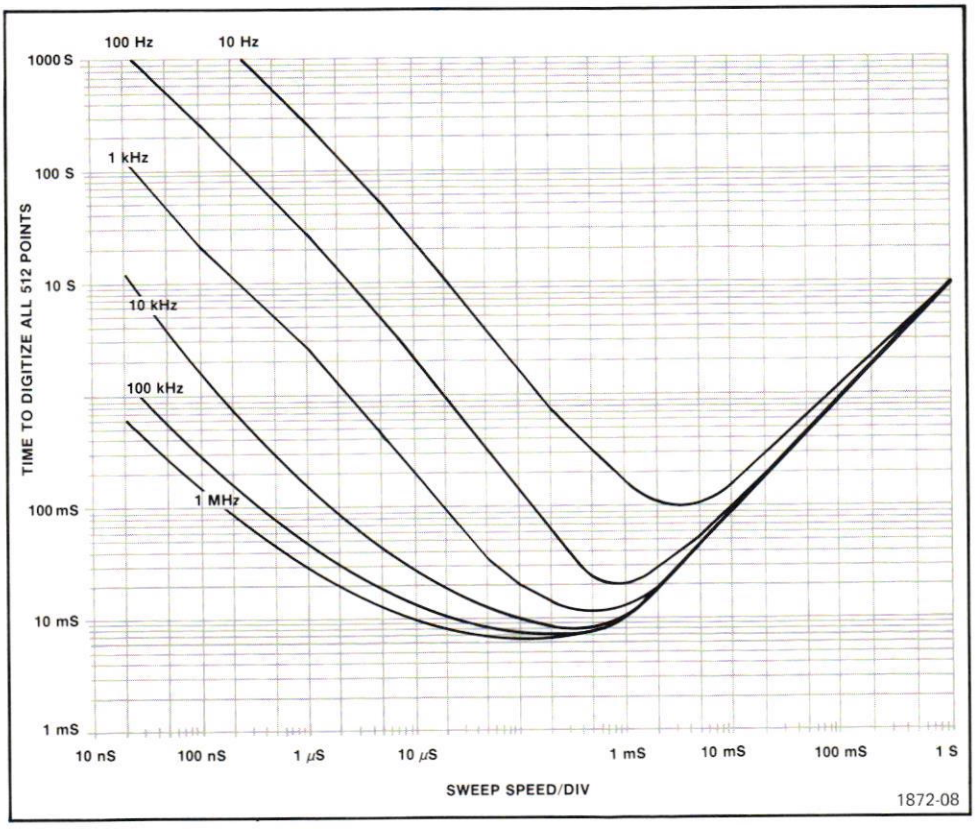


Fig. 4-6. Time required to digitize 512 data points.

Readout Interface. The Readout Interface converts analog scale-factor information from the plug-ins to ASCII format for storage in the P7001 Memory. It also performs the opposite function, providing a CRT display of stored scale factors or messages. The Readout Interface does not generate the actual displayed signal. It converts the ASCII data to row and column currents that are identical to those generated by the plug-in. These currents are sent to the Readout board in the DPO Acquisition unit. This board generates the analog signal for display of the readout characters.

Each waveform memory location has associated with it four fields, each containing storage for up to 80 characters. Field Ø contains the scale-factor readout from each plug-in, stored automatically when waveform storage occurs.

The remaining three fields are used for computer-generated messages. The messages are stored by addressing the desired field and waveform locations (see Fig. 4-1), and then writing ASCII data into the addressed locations. The ASCII data is set in the lower seven bits (Bits 5—11) of the P7001 Memory Data Word (see Fig. 4-2). The stored message can be selected for display by writing a status word to the Readout Interface. The format of the status word is shown in Fig. 4-7.

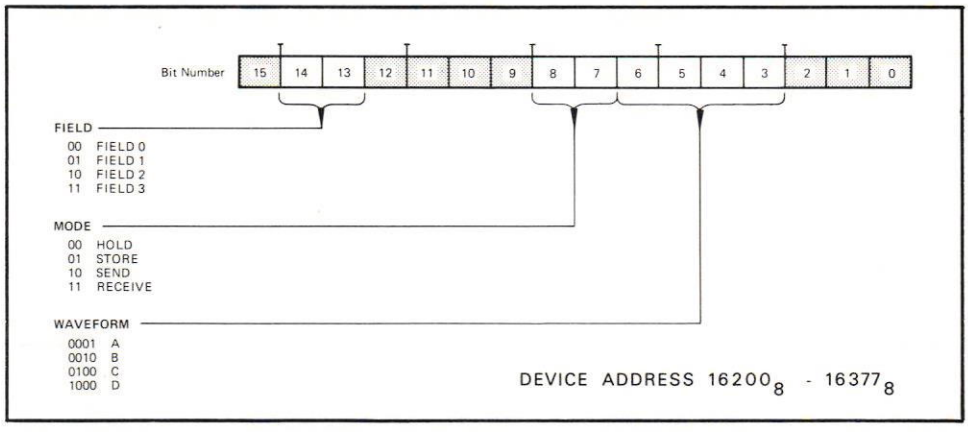


Fig. 4-7. Readout Interface Status Word.

The FIELD bits determine which message field is to be displayed. The displayed field will be the one associated with the waveform selected by the WAVEFORM bits. If more than one waveform is selected, the Readout Interface automatically selects the message field alphabetically nearest A. The front panel DISPLAY SOURCE switch must be set to BOTH or MEMORY and the Readout Interface Card's status set to HOLD before the Readout Interface will display messages.

The MODE bits determine whether the Readout Interface is to store converted scale-factor information, or read memory and display its contents. When in STORE mode, the Interface stores scale-factor data from the plug-ins for the waveform selected with the WAVEFORM bits. Field Ø is automatically selected. The characters displayed on the CRT during STORE come from the Plug-ins. When in HOLD, SEND, or RECEIVE mode, the Readout Interface scans the field indicated by the FIELD and WAVEFORM bits, displaying the information it finds there.

Display Generator. The Display Generator functions as a Digital-to-Analog Converter, providing drive signals to the CRT from digital information stored in the waveform portions of memory. Alternately, the computer can supply information to the Display Generator on a real-time basis, resulting in a refreshed display. Since information stored in memory is displayed in a Y-T mode, multivalued functions cannot be displayed (one memory location can't hold more than a single value). The computer-refreshed information is not stored in memory, however. In this X-Y mode, each point is plotted on the DPO screen as soon as its coordinates are received, allowing a refreshed display of spirals, circles, etc.

The Y-T or X-Y mode is selected by writing a status word to the Display Generator. The Display Generator status word format is shown in Fig. 4-8.

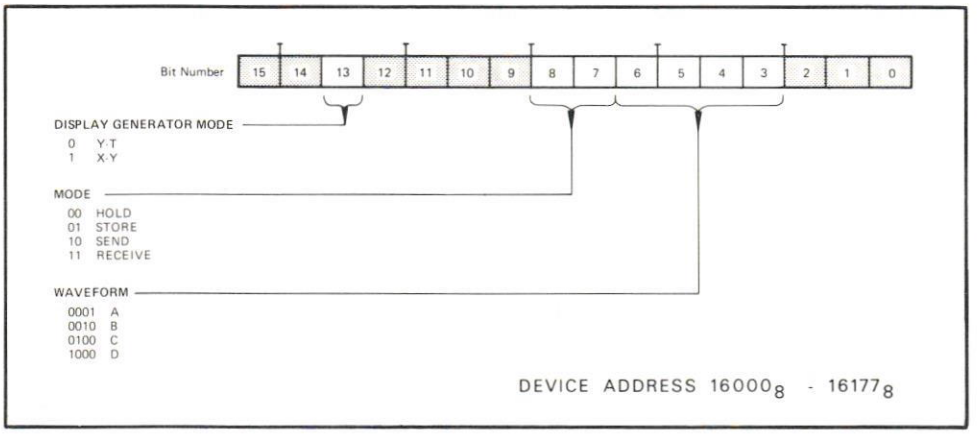


Fig. 4-8. Display Generator Status Word Format.

The DISPLAY GENERATOR MODE bits select the X-Y or Y-T mode, as just discussed. Remember that the Display Generator must be set to the Y-T mode to display waveforms stored in memory. The waveform to be displayed is selected by the WAVEFORM bits. In the Y-T mode, any combination of waveforms may be displayed simultaneously. Note that the Display Generator may be set to display one waveform while another is being stored by the A-D Converter. Multiple operations such as this often save time and result in a more meaningful display for the DPO operator.

The MODE bits determine the operating sequence of the Display Generator. Although four bit patterns are indicated, only two distinct states are recognized: HOLD, and STORE. The SEND and RECEIVE bit patterns are decoded as HOLD. HOLD mode results in a normal display of the waveform(s) selected by the WAVEFORM bits. STORE mode causes the Display Generator to clear the selected memory location(s) and begin to display new information placed there by the A-D Converter. This operation amounts to a Clear and Hold sequence.

Approximately 40 milliseconds are required for the Display Generator to perform the clearing operation and return to the HOLD mode. Any information placed in memory by the A-D Converter or the computer during this time may be lost. A convenient solution is to not use the Display Generator in the STORE mode. Writing new information directly into the selected waveform memory location results in an overwrite of the old data, effectively performing the clear operation without concern for the 40-millisecond delay.

When the Display Generator is operating in the X-Y mode, the X and Y coordinates must be provided by the computer. To make the transfer as simple as possible, the horizontal data word is contained in a special Display Generator X-Y mode address. The format of the address is shown in Fig. 4-9.

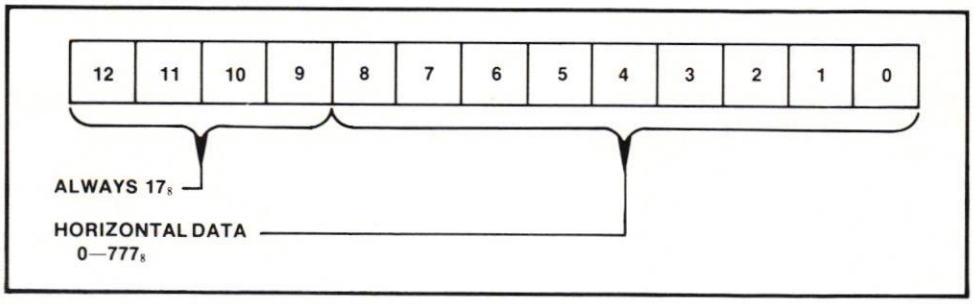


Fig. 4-9. X-Y Mode Address Format.

Sending the desired X-Y mode address to the Display Generator also prepares it to accept vertical data. The vertical data is simply written to that address. The vertical data word format is shown in Fig. 4-10. A minimum delay of 8 microseconds is required between X-Y coordinate pairs, to allow the points to be plotted.

Notice in Fig. 4-10 that you can also control the intensity of the electron beam as it plots the data. The Display Generator automatically plots a vector between successive points. The brightness of the vector can be changed from DARK (no display) to DIM, NORMAL, or BRIGHT by appropriately setting the INTENSITY bits. This intensity control is a tremendous advantage when displaying complex functions in the X-Y mode.

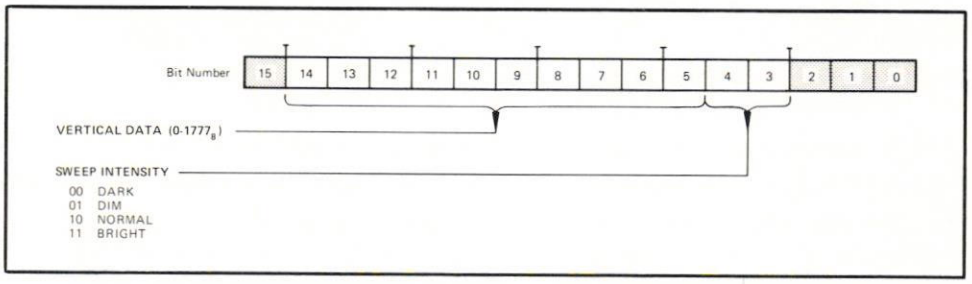


Fig. 4-10. X-Y Vertical Data Word Format.

Front Panel. The Front Panel performs a dual function. First, it controls the P7001 Processor functions when certain buttons are pressed. Lights behind most pushbuttons indicate the current status of the Front Panel circuitry. The lights can be operated under program control.

Second, the P7001 generates interrupt signals to allow the computer to respond to pushbutton requests from the Front Panel. When an interrupt is received, the computer reads the Front Panel status word to determine the interrupt source. The computer interrupt handler then initiates the appropriate action.

Some portions of the Front Panel status word are read/write, some write only. The format of the Front Panel status word is shown in Fig. 4-11.

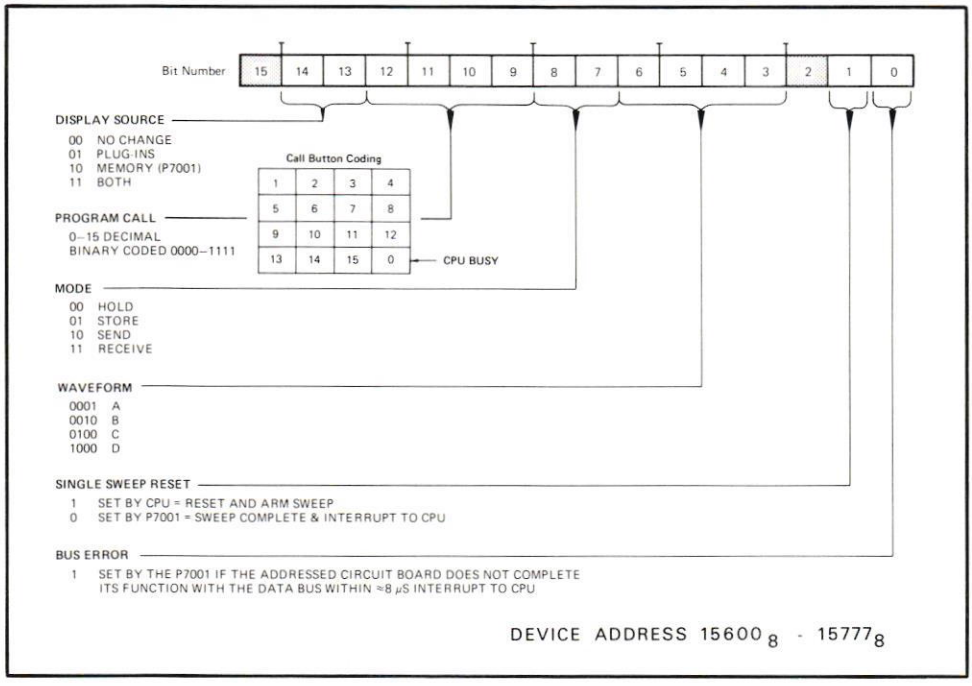


Fig. 4-11. Front Panel Status Word Format.

The DISPLAY SOURCE bits control the source of signal to the CRT. Writing the desired bit combination into the Front Panel status register switches the display source and lights the corresponding pushbutton on the P7001. Pressing the Display Source pushbuttons does not cause interrupts to occur, and the status of the lights cannot be read from the Front Panel status word.

The PROGRAM CALL bits can be read only after one of the Program Call buttons has been pressed, causing an interrupt. The binary code that becomes available after the interrupt indicates which button was pressed. The information is usually used to

begin the execution of a specific program in the computer. In this way, as many as fifteen different waveform processing programs can be executed by the DPO operator with the press of a button.

Writing a "1" into any of the PROGRAM CALL bits of the status word causes button 16 to light. This light is commonly used to inform the DPO operator that the computer is busy. Writing zeroes into all bits turns off the light.

The MODE bits control only the lights under the Data Handling pushbuttons. Writing the desired bit combination into the status register turns on the selected light. The MODE bits are write-only, and one of the lights will always be on.

Pressing a Data Handling pushbutton does not cause an interrupt, but it does set a flip-flop that allows the START button to cause one when pressed. If an interrupt is generated this way (i.e., by pressing SEND, or RECEIVE, or STORE, and then START), any one of the DATA HANDLING or WAVEFORM buttons will generate another interrupt when pressed, changing the mode to HOLD.

The WAVEFORM bits control the lights under the Memory Location pushbuttons. Any combination of lights may be turned on by combining the individual bit patterns. Writing "Ø into all bit positions extinguishes all of the lights.

If a Memory Location button is pressed on the Front Panel, an interrupt is generated, but no action need be taken by the computer if the MODE bits of the Front Panel status word indicate the HOLD mode. The Front Panel logic is constructed so that if HOLD and any other Data Handling buttons are lighted, the Front Panel status word indicates only the HOLD pattern. If SEND (for example) and HOLD are both on, and START is pressed, HOLD is cleared. The Front Panel status word now indicates the SEND operation, and the interrupt handler can transfer to a routine that reads the waveform data indicated by the WAVEFORM bits, transferring it to the computer.

The SINGLE SWEEP RESET bit affects the sweep circuits of the horizontal time-base plug-in. If the plug-in is set to Single Sweep mode, the sweep can be reset (armed) by writing a "1" into the status register. A flag should be set in the computer whenever the sweep is armed this way. After the sweep is triggered and has completed its sweep, the SINGLE SWEEP RESET bit is cleared from the status register and an interrupt is generated. When the interrupt handler interrogates the Front Panel status word, the bit will be off, and the flag set, indicating that sweep completion caused the interrupt.

The BUS ERROR bit is read only. It is set by the P7001 whenever an addressed circuit fails to complete its operation in approximately 3.5 microseconds. An interrupt is generated when the bit is set. A bus error can be caused by a circuit malfunction, or by the absence of an addressed card.

Section 5

THE DPO UNDER PROGRAM CONTROL

Any operation that can be done from the Front Panel of the DPO can be done by computer. Storing waveforms, sending and receiving waveforms to and from the computer, and any processing desired can be carried out by pressing a button to start the computer program.

This section presents methods of acquiring repetitive and single sweep waveforms, zero references, and waveform transfers to and from the computer. Generalized flowcharts of the procedures are offered for ease in understanding the steps necessary for different operations. The programmer, however, is by no means limited to these procedures.

A good understanding of setting and reading the DPO status words (see Appendix A) is necessary for efficient DPO/computer communication. In these examples, communications through interfaces are not shown. It is assumed that routines to handle interface communications will precede any transfers between the computer and the DPO address and Data registers. The computer operation also must be understood for efficient program design.

Setting Up the Environment

Before any of these status words can be put to use, an operating environment must exist inside the computer to handle the different functions assigned to the Front Panel pushbuttons.

Each waveform requires several words and buffers to hold the necessary information. Listed below are suggested labels for these values, and an explanation of what they will contain.

ARRAYA:	A 512-word buffer to hold the waveform.
ZEROA:	Word to hold the Zero Reference Value of the array.
VERTA: or VA:	Word to hold the vertical scale factor of the array (i.e., Volts per division).
HORZA or HA:	Word to hold the horizontal scale factor (i.e., Time per division).

VA$: Ten-byte buffer to hold vertical units (i.e., V for Volts, A for Amps, etc.).

HA$: Ten-byte buffer to hold horizontal units (i.e., S for seconds, H for hours, etc.).

These labels will be used in the following flowcharts to reference P7001 array A. When referencing other arrays, B for example, the labels will be ARRAYB, ZEROB, VB$, etc.

Also, labels will be used to refer to the different DPO status words. These labels (with corresponding address in octal) are:

AD: =16400, address of the Analog-to-Digital status word.

RO: =16200, address of the Readout Interface status word.

DG: =16000, address of the Display Generator status word.

FP: =15600, address of the Front Panel status word.

Another nomenclature used in these flowcharts refers to addressing and reading data from the DPO. These are:

xx → DPO To move the address xx (FP, DG, etc. or memory address) to the DPO Address Register.

DATA → xx Read Data and place the results in location xx.

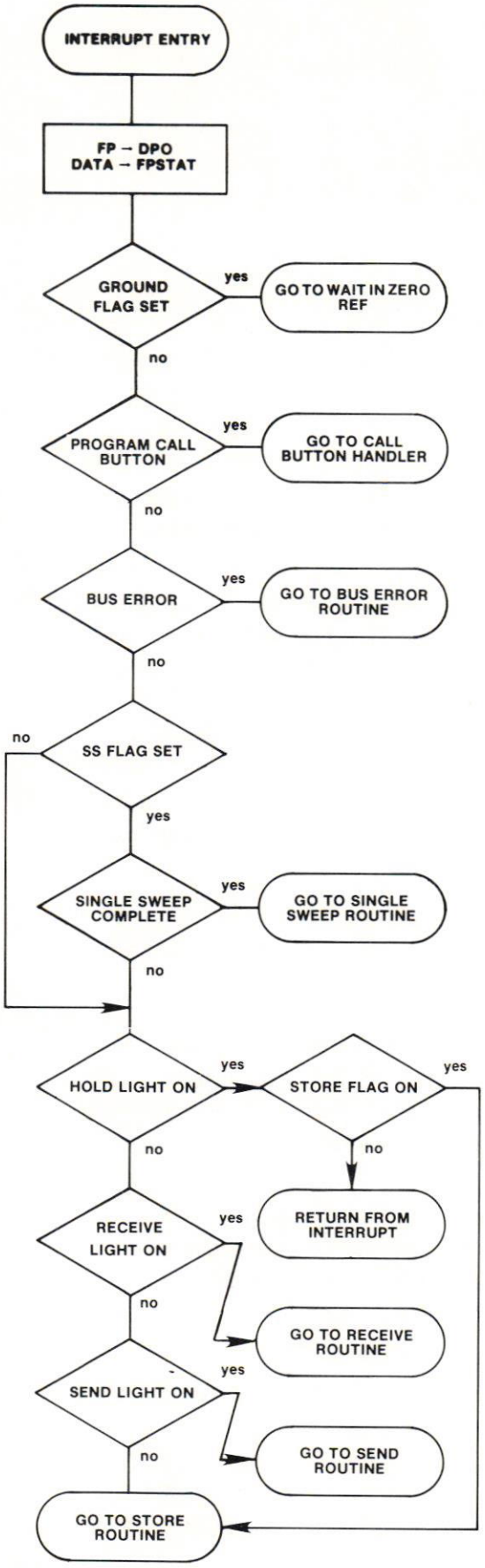
When information is sent to a subroutine, the labels ARG1, ARG2, etc. are used.

Data Handling Buttons

None of the Data Handling buttons (STORE, HOLD, SEND, and RECEIVE) cause interrupts to the computer by themselves. However, when START is pressed, an interrupt is generated, and the software can examine the Mode bits in the Front Panel status word and determine what action is to be taken. After START has been pressed, pressing any of the DATA HANDLING or WAVEFORM LOCATION buttons will be the same as pressing HOLD.

Let's go through the steps necessary for the computer to recognize a Front Panel Interrupt. Assume that the Interrupt Enable circuitry in interfaces is not set to enable interrupts. The computer can be processing a foreground program, be interrupted to examine the Front Panel, determine if any action is to be taken, and then either perform the desired operation, or continue with the foreground program, depending on priority.

The following flow chart is a generalized routine to handle interrupts from the DPO. It is assumed that the coding to determine what particular instrument caused the interrupt has preceded the interrupt handler.



Enter the Interrupt Handler.

Put Front Panel Status into FPSTAT.

Test GROUND FLAG. If set, go to instruction after WAIT in Zero Reference Routine.

If any Program Call bits are set, branch to Special Handler Routine.

If Bus Error bit is set, print DPO Timeout message.

If Single Sweep bit off and Flag is set, go to single sweep routine.

If HOLD light is on, and STORE FLAG set, then this is completion of a STORE operation. If STORE FLAG is not set, then Interrupt was a Memory location change, so ignore.

If RECEIVE or SEND lights are on, then branch to appropriate routine.

If nothing else, must be a STORE operation.

Storing Waveforms

The Store routine must determine if the operation is the start or end of the STORE sequence. (The sequence is STORE — waveform location(s) — START — HOLD.) If it is the start, then all it need do is set a flag and return from the interrupt. When HOLD is pressed, stopping the STORE operation, an interrupt is again generated. The interrupt handling routine checks if the store flag has been set, and if so, goes to the Store routine.

Zero Reference. At this time, the Store routine should request a zero reference from the DPO operator. (This step may be deleted if desired, or used only if another flag has been set previously, possibly by a Program Call button. This allows use of previous zero references with the new waveform.)

The request for a zero reference may be done (as in this example) by displaying a message on the DPO CRT, or sending a message to the computer terminal.

The message is sent in ASCII to Field 1 of the selected Memory Location. (Sending to Field 1 will not destroy scale factor information in Field Ø of the waveform.) The Readout Interface is then selected to display that message.

After the message has been displayed, the routine should wait for the operator to ground the probe and signal the computer to read several samples of the A-D output. These samples can then be averaged, and a ground reference established. Our sample routine will accept a ground reference input only if Program Call button 14 has been pushed. It ignores all other interrupts.

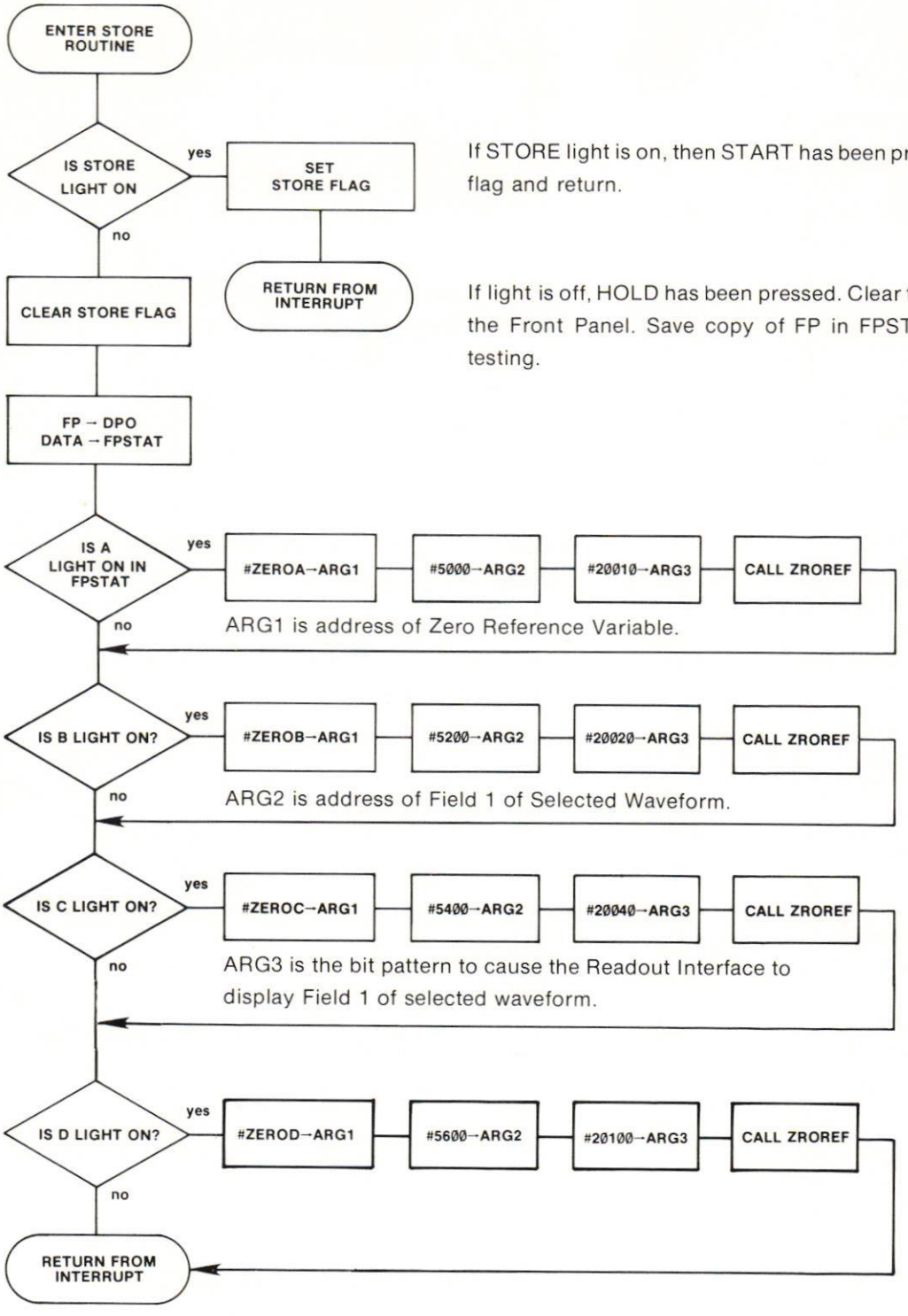
Since the waveform still resides in the P7001 Processor Memory, scale factors can be ignored for now.

In the flowchart example, the Memory Location bits are tested sequentially. Those found to be on represent a newly acquired signal. The ZROREF routine displays the "ground probe" message, waits for button 14 to be pressed, acquires 32 samples of the A-D output, and stores the average in the location pointed to by ARG1.

ARG2 points at the DPO Memory Location at which the message is to start (the first word of Field 1 for the selected waveform). If, in your particular operation, any field other than Field Ø is unused, it would be possible to put ground reference messages in the field at program load time, and then just display that field when needed.

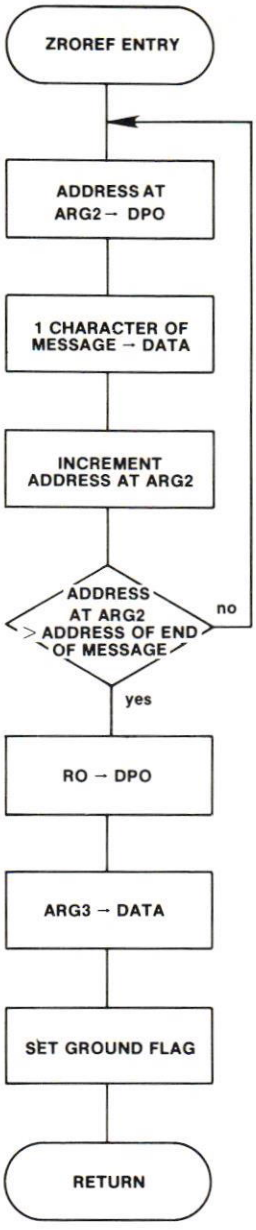
ARG3 is used to address the proper field for message display.

The Front Panel status is saved in a location labeled FPSTAT, and this word is then used when testing the Memory Location bits. This ensures that any bit which was on when HOLD was pressed (to stop the store operation) will not be lost if the Front Panel status is changed later by pressing other buttons.



If STORE light is on, then START has been pressed, so set flag and return.

If light is off, HOLD has been pressed. Clear flag and read the Front Panel. Save copy of FP in FPSTAT for later testing.



Enter the Zero Reference Routine.

Move address of Field 1 of selected waveform to DPO address register.

Send first character of Message to address in DPO Address register.

Increment the address.

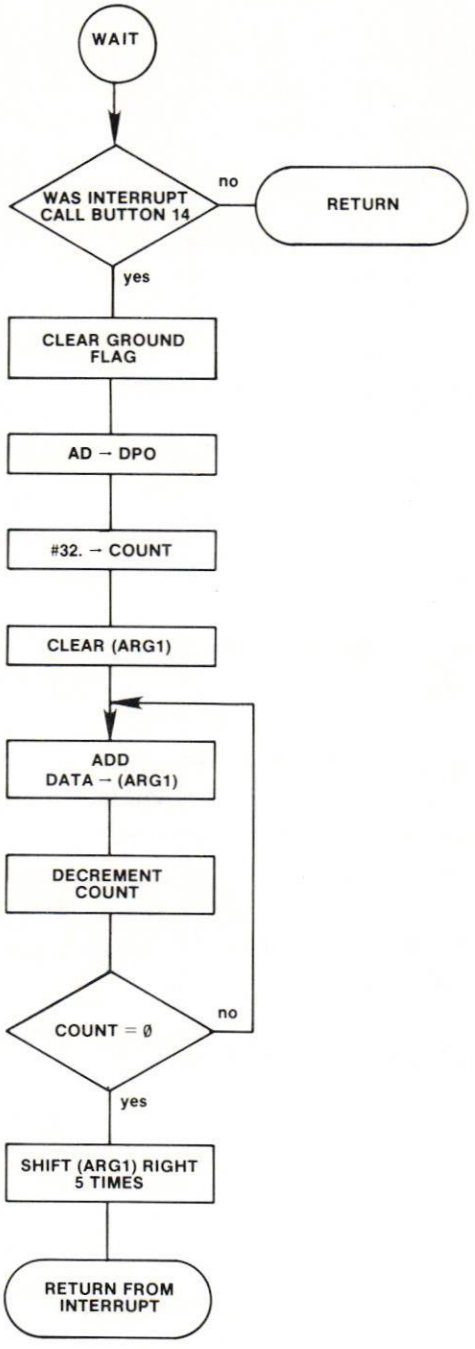
Address greater than address of end of Message? No, move next character.

Address the Readout Interface board.

Display Field 1 of selected waveform.

Set flag so Interrupt Handler can branch here next interrupt.

Return from the interrupt.



Here is where Interrupt handler branches if GROUND FLAG has been set. See if button 14 was pressed (FP→DPO, test bits 12-9 of DATA).

Clear the GROUND FLAG.

Address the DPO Address register.

Prepare to COUNT 32 times.

Clear the location pointed to by ARG1.

Add the current value of the A-D output.

Count it.

All done? If not, do again.

Divide sum by 32 for average.

Return from the interrupt.

Program Controlled Storage

The preceding store routine was used only to ask the operator to ground the probe so a proper zero reference could be obtained. The actual storage operation was done automatically by the P7001 Processor when the START button was pressed.

However, it is possible for the entire operation (except the grounding of the probe) to be initiated by the computer itself (a buttonless procedure).

The programming sequence to store a waveform into Memory Location A would be as follows:

1. Set the A-D Converter status to STORE, A.

2. Set the Readout Status to STORE, Field Ø, A.

3. If desired, the Display Generator and Front Panel Status can be set to STORE, A so the DPO operator can see the operation take place.

4. Initiate a timing loop to keep the STORE operation on long enough to ensure all data points in the array have been filled. Fig. 4-6 is a graph of sweep speed versus time to store a waveform. (You can get the horizontal scale factor from an array first and create a timing loop for optimum storage through computation, if desirable.)

5. When the STORE operation is complete, reset the A-D and Readout status words to HOLD (also the Display Generator and Front Panel, if used).

6. If desired, a message may be sent to the DPO operator to request a ground signal for a zero reference.

Storing Single Sweeps By Computer Control

To capture single sweeps with the DPO under computer control, the following steps must be performed before the event:

1. The DPO time base plug-in must be set to SINGLE SWEEP.

2. The A-D Converter and Display Generator status word must be in the STORE mode, and the Memory Location bits set to indicate which array to store into.

3. The Readout Interface status must be in the STORE mode, the correct Field set (usually Field Ø), and the proper array indicated in the Memory Location bits.

4. Bit 1 of the Front Panel status word must be turned on. (This is the same as pressing SWEEP READY on the time base.)

Step 2 clears the array that will contain the waveform and step 3 will store readout information. Step 4 arms the single sweep. After the trigger occurs and the sweep is complete, the P7001 Processor turns off bit 1 of the Front Panel status word and interrupts to the computer. The interrupt handler must determine if the interrupt was caused by the bit being turned off. This can be accomplished by setting a flag during set up. If the flag is set, and the Single Sweep Reset bit is off, then it can be assumed that the interrupt did indeed result from a sweep complete.

Sending Waveforms To The Computer

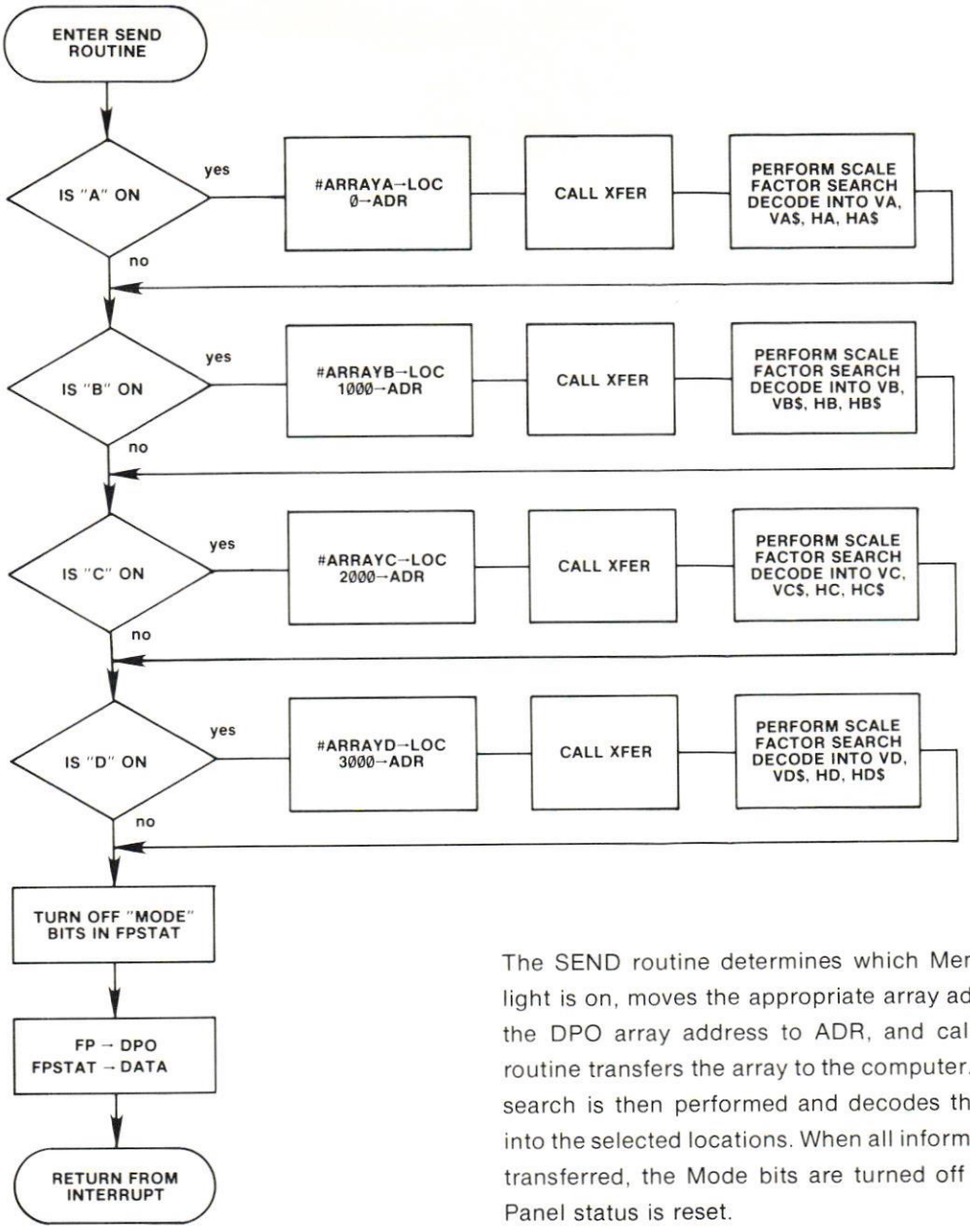
After a storing sequence is complete, the DPO operator (or computer program) may want to SEND the array to the computer for processing. This is done by the pushbutton sequence SEND — waveform button — START. The computer can automatically reset the Front Panel to the HOLD mode after the transfer is complete.

The SEND routine must determine which of the Memory Location buttons has been pressed, send the specified P7001 arrays to matching computer arrays, and find the appropriate scale-factors for the waveform.

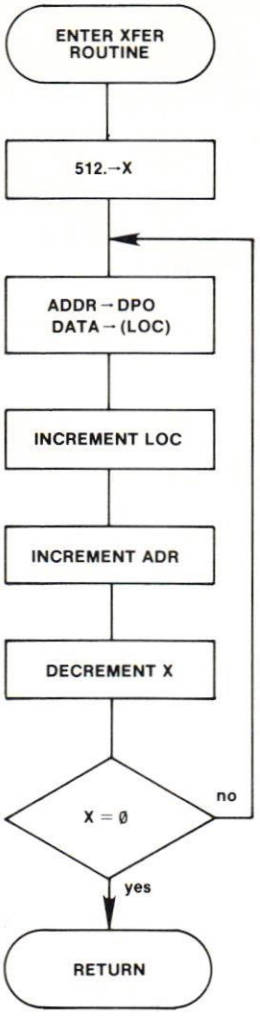
When the SEND button is pressed, an interrupt is not generated. HOLD is still illuminated. When a Memory Location button is pressed, an interrupt is sent to the computer. The interrupt handling routine must check to see what the status of the Front Panel is to determine the cause of the interrupt. The possibilities are a bus error, a single sweep complete, program call button, or status change. In this example, the interrupt is a status change, but no action need be taken. (The computer cannot "see" the SEND button, since HOLD is still on.)

Now, when START is pressed, the HOLD light goes out, and the interrupt handler can see that the SEND operation has been requested. The Memory Location bits are examined, and depending on which bits are on, the correct DPO address can be generated and the transfer can start.

The transfer operation simply moves a block of words from the DPO to the computer (512 words for a DPO array, 20 for scale-factors, both horizontal and vertical). The address of the DPO word to be moved is sent to the DPO Address Register, and that word is read from the DPO Data Word. The 10-bit data word from the DPO is located in bits 5—14 of the Data Word, so the sending routine should shift the Data Word 5 bits to the right to be compatible for computer processing.



The SEND routine determines which Memory Location light is on, moves the appropriate array address to LOC, the DPO array address to ADR, and calls XFER. This routine transfers the array to the computer. A scale factor search is then performed and decodes this information into the selected locations. When all information has been transferred, the Mode bits are turned off and the Front Panel status is reset.



Enter the waveform transfer routine.

Set counter to 512.

Put address to move into DPO Address Register. Move data word to location pointed to by LOC.

Increment the receiving address

and the sending address.

Count the move.

512 words moved yet?

Return to the calling routine.

Scale-Factor Decoding

The 80 readout characters are divided into eight channels of 10 time slots each as shown in Fig. 5-1. Channels Ø, 1, 4, and 5 hold vertical scale-factor information, and channels 2, 3, 6, and 7 contain the horizontal (time/div) information.

In order to get the correct readout for a specified waveform (i.e., if more than one channel contains information), a specific search algorithm is used. The first channel found to contain readout information is the desired channel.

The search sequence for vertical data is:

Waveform INPUT	CHANNEL SEARCH ORDER
A	Ø, 4, 1, 5
B	4, Ø, 5, 1
C	1, 5, Ø, 4
D	5, 1, 4, Ø

When getting horizontal readout, the search sequence is:

Waveform INPUT	CHANNEL SEARCH ORDER
A or B	3, 7, 2, 6
C or D	2, 6, 3, 7

A "find" is determined by a scale-factor indicator in time slot 1 of the correct channel followed by non-blank characters. The scale-factor indicator produced by analog plug-ins is a ":" in ASCII.

For example, to find the vertical scale factor for waveform B, the following search sequence would be used:

Channel No.	Addresses to search
4	4250 — 4261
Ø	42ØØ — 4211
5	4262 — 4273
1	4212 — 4211

When decoding scale-factor information, the following characters after time slow 1 can be ignored:

Space, delete or null.

: (the scale factor indicator)

; (digital measurement indicator)

Decimal point logic is used in digital plug-ins, and determines the position of the decimal point in the channel. These characters may be placed by the computer at any position within the channel. They are:

CHARACTER	DECIMAL POINT POSITION
$	Decimal placed after 3rd "non-delete" character in channel.
%	Decimal placed after 4th "non-delete" character in channel.
&	Decimal placed after 5th "non-delete" character in channel.
'	Decimal placed after 6th "non-delete" character in channel.
(	Decimal placed after 7th "non-delete" character in channel.

A minus sign (−) indicates that the numerical portion which follows is negative.

The following characters, if they occur, must appear in the order listed. Unless otherwise indicated, each item may appear only once.

Uncal units: ! (appears as down-arrow on readout, means input is inverted)

>, <, or X (uncal indicators)

No more than two uncal units should appear, the first signifying that the waveform is inverted, the second that it is uncalibrated.

Number: 0—9 (up to 10 digits may be present)

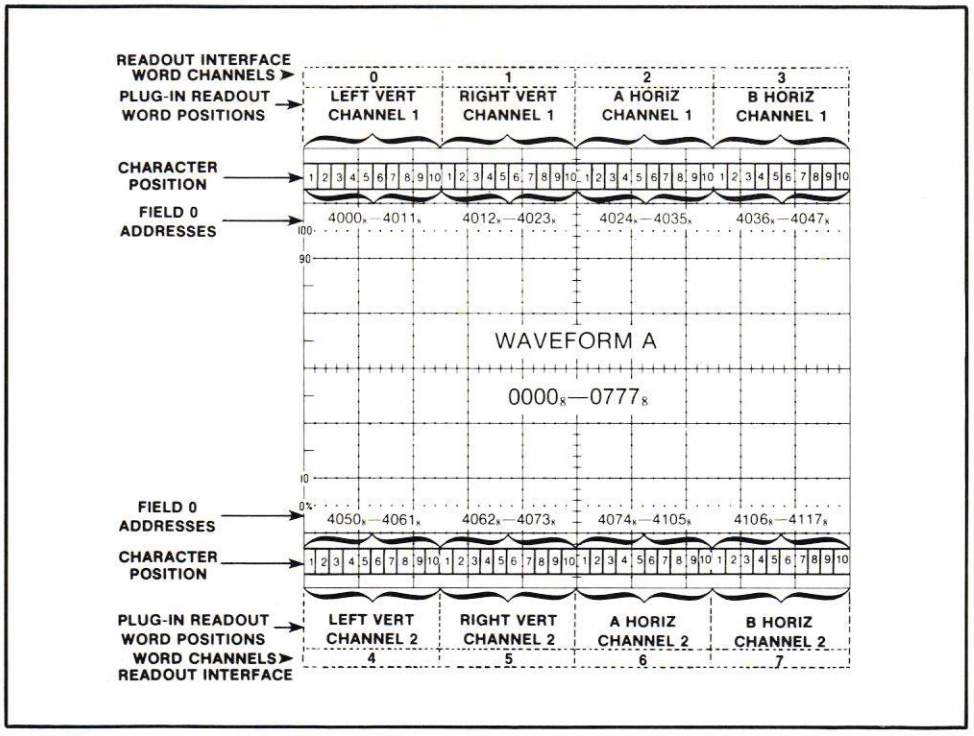
Exponent: F, p, n, μ, m, K, M, G, T, (prefix to units)

Only one prefix may occur.

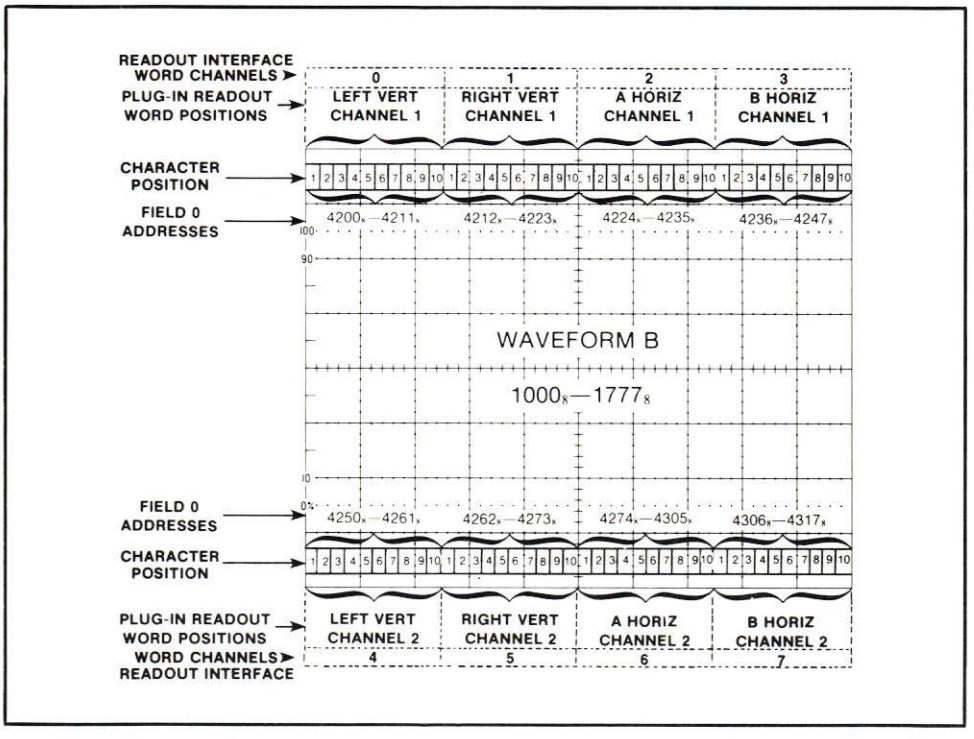
Units: Any other characters.

The contents of any time slots remaining after the above items have been found are treated as units.

Once the proper scale factor has been found and transferred to the computer, it is necessary to decode the ASCII information to a computer-usable binary number. Also, the "units" (i.e., V for volts, S for seconds, etc.) should be saved for future display.

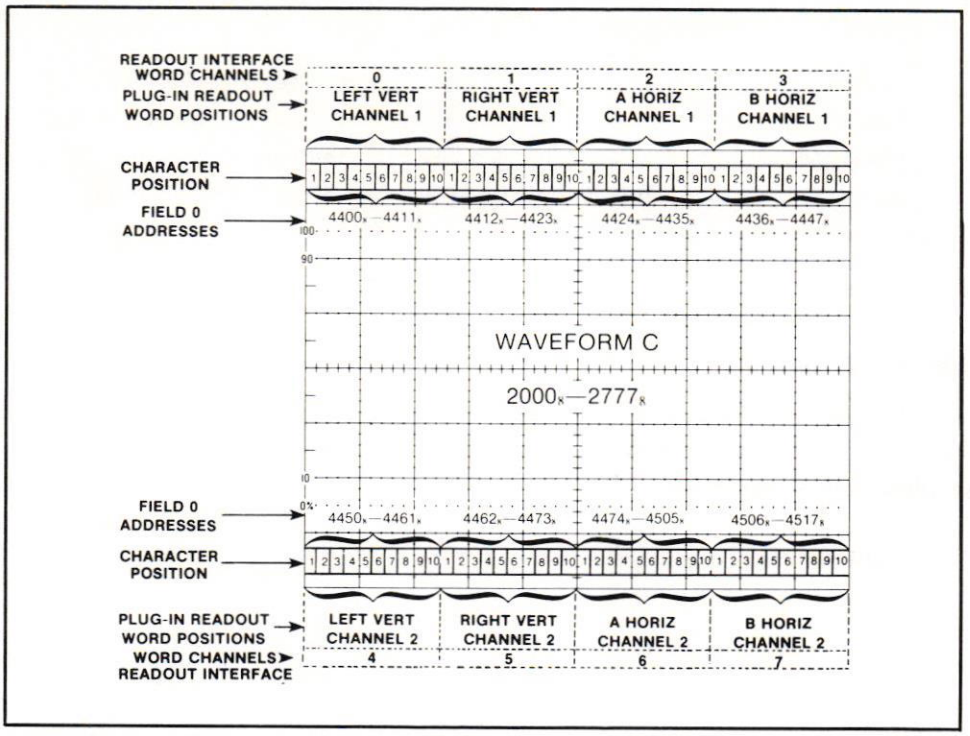


(A)

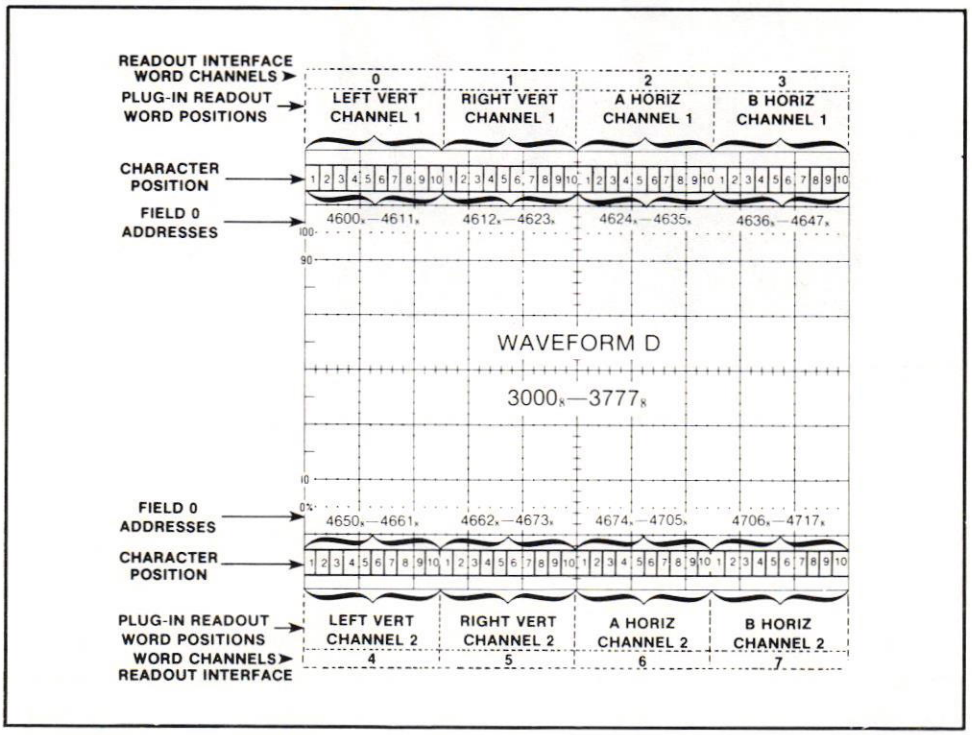


(B)

Fig. 5-1. Addresses of Waveform Readout Locations.



(C)



(D)

Fig. 5-1 (cont). Addresses of Waveform Readout Locations.

NOTE

The P7001 Readout Interface Card has a strap option which will allow you to store the ASCII code for DELETE or uppercase "O" (underline). This will allow those computer systems using the DELETE command for a significant operation to use the underline for P7001 Readout Storage. See the P7001 Readout Interface Service Manual (070-1609-00).

Scaling Waveforms

With the waveform residing in the computer, processing can begin. One very useful operation is converting the 10-bit array value to a value representing the true amplitude of the waveform.

Consider the acquired waveform as shown in Fig. 5-2.

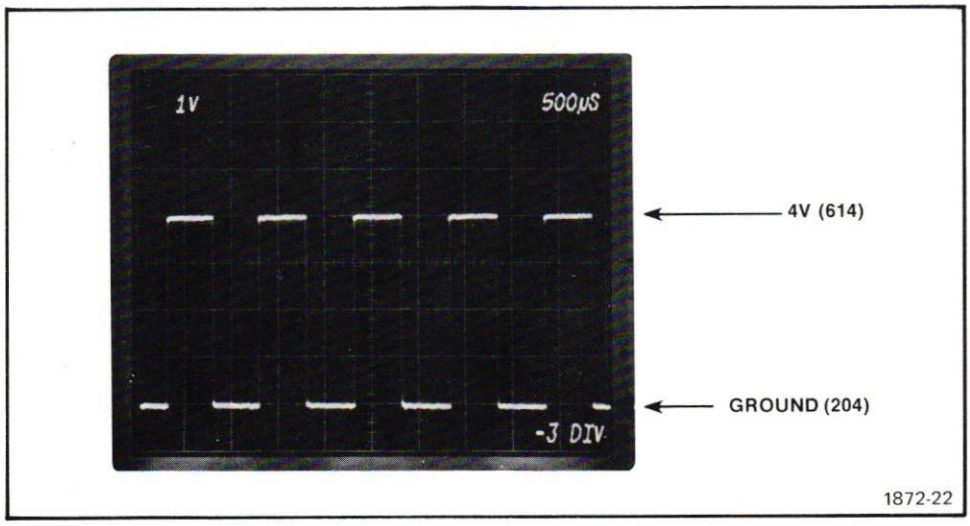


Fig. 5-2. Actual amplitude of signal in P7001 Memory.

A ground reference has been acquired, with a value of decimal 204. This represents 2 divisions up from the bottom of the array (the bottom line of the graticule is one division above the bottom of the array). The vertical scale factor reads 1 volt/division. With this information, you can see that the waveform has an amplitude of 4 volts peak-to-peak. However, if the computer were to print out the values of the array, they would be in the range of decimal 614, or the peak vertical amplitude of the P7001 array.

A simple formula can be used to convert the processor values to true amplitude:

A_i is the true amplitude where:

$$A_i \text{ (true amplitude)} = \frac{(A_i\text{-ZEROA}) * \text{VERTA}}{102.4} \qquad (\text{for } i = 0, 1, 2 \ldots 511)$$

where ZEROA is the zero reference value, and VERTA is the vertical scale factor. A_i is the waveform element.

Rescaling Waveforms. After waveform processing is complete, and sometimes at intermediate stages of processing, it is often desirable to send the waveform back to the DPO for display.

If the waveform is scaled to true amplitude, it is necessary to "un-scale" the waveform to allow DPO display. This is simply the reverse of the scaling processes. Also, it is possible to expand or contract the waveform vertically by changing the VERTA variable. The formula for rescaling the waveform is:

$$A_i \text{ (DPO amplitude)} = \frac{A_i * 102.4}{\text{VERTA}} + \text{ZEROA} \qquad (\text{for } i = 0, 1, 2, 3 \ldots 511)$$

Remember that as waveforms are sent back to the DPO, each word of the array must be shifted 5 bits to the left before transmission to the DPO Data Register.

To present as much information as possible at the display, a message indicating the ground level should also be displayed. For easy interpretation, this value should be presented in terms of screen graticule lines. If the center line is used to represent 0 division, the following formula can be used to write the ground level on the screen:

$$\text{Ground level} = \text{ZEROA}/102.4 - 5$$

When this formula is used, the ground reference in Fig. 5-2 would be −3 divisions from center screen.

X-Y Displays on the DPO CRT

The DPO has the capability of displaying vectors plotted between sequential X-Y coordinate pairs provided on a realtime basis by a computer. Vectors can be drawn between points in any of four intensity modes; dark, dim, normal, or bright.

To set the DPO to the X-Y mode of operation, the Display Generator must be addressed and bit 13 of the Display Generator Status word turned on. The MODE bits (7 and 8) should be set to HOLD.

Coordinates are sent as X and Y pairs, the X data going to the DPO Address Register, and the Y data (with intensity information included) to the DPO Data Register.

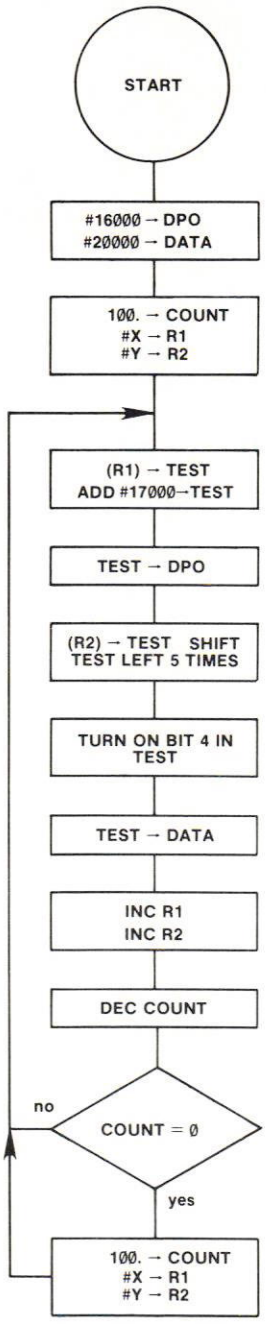
Each data pair sent causes the DPO to draw a vector from the last position selected to the new coordinate. Since the DPO CRT is not a storage type, visibility of the vector is dependent on the intensity selected and the computer's data refresh time.

X Data Format. When the X data is sent to the DPO, it is sent as a modified address. The lower 9 bits (0—8) contain the horizontal address (0—511) of the data point. This is added to octal address 17000 to create a DPO address. The X data word format is shown in Fig. 4-9.

The X data is presented to the DPO Address Register. The DPO interprets information sent to locations 17000_8 to 17777_8 as a horizontal beam position. Vectoring does not occur, however, until the Y coordinate data has been sent.

Y Data Format. The vertical coordinate data is sent to the DPO Data Register. Bits 5—14 contain the vertical value (0—1023), and bits 3 and 4 control the beam intensity. Fig. 4-10 shows the format for the Y data word.

The following flowchart shows a simple program for displaying 100 X-Y data pairs with normal intensity on the DPO CRT. Buffers X and Y each contain 100 values, corresponding to each X-Y coordinate pair.



Address Display Generator X-Y Mode.

Establish a Counter.

Set Registers 1 and 2 to point to beginning of X and Y buffers.

Get first X value.

Add in 17000 to create DPO Address.

SEND the X address to the DPO Address Register.

Put Y value into test.

Shift left 5 times.

Make intensity NORMAL.

Send Y value to DPO DATA word.

Point registers to next data pair.

Count the vector.

If last data pair sent, restore counter and pointers and start over.

APPENDIX A

ASCII* (OCTAL)	CRT DISPLAY	ASCII* (OCTAL)	CRT DISPLAY	ASCII* (OCTAL)	CRT DISPLAY	ASCII* (OCTAL)	CRT DISPLAY
040	SPACE	067	7	107	G	124	T
041(!)*	↓	070	8	110	H	125	U
053	+	071	9	111	I	126	V
055	–	074	<	112	J	127	W
056	.	075(=)*	△	113	K	130	X
057	/	076	>	114	L	131	Y
060	0	100(@)*	Ω	115	M	132	Z
061	1	101	A	116	N	143	c
062	2	102	B	117	O	144	d
063	3	103	C	120	P	155	m
064	4	104	D	121	Q	156	n
065	5	105	E	122	R	160	p
066	6	106	F	123	S	165(u)*	μ

*ASCII character is different from displayed character.

1609-11

ASCII Codes for CRT Character Display.

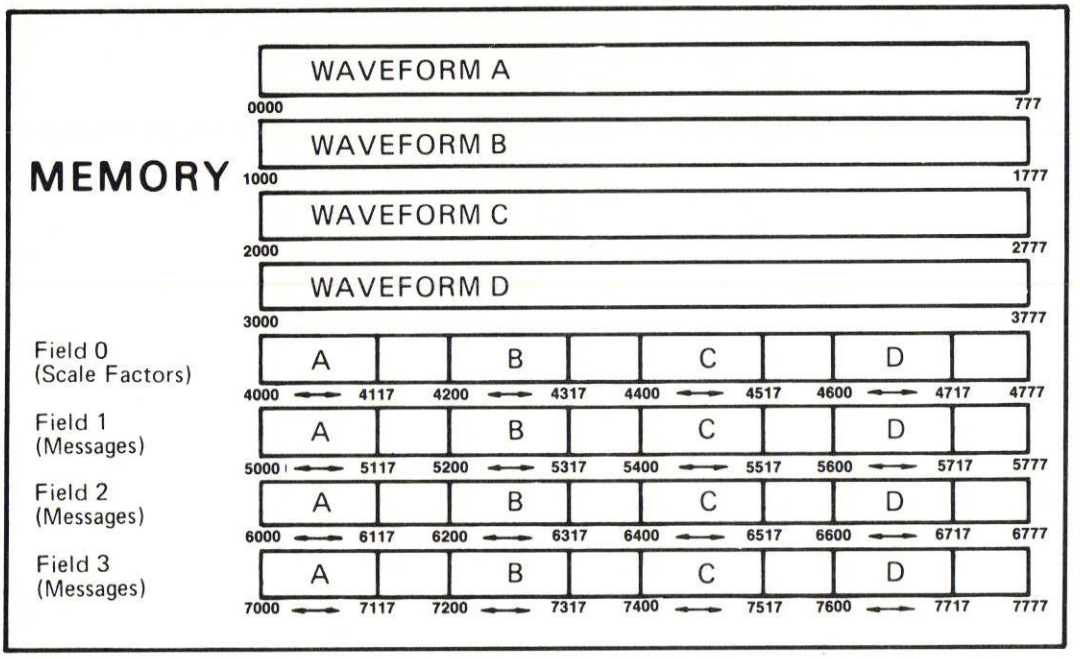
ASCII		Notes
OCTAL CODE	Char.[1]	(Refer to 7704A Manual for details)
044	$	Decimal placed after 3rd "non-DEL" character in this channel.
045	%	Decimal placed after 4th "non-DEL" character in this channel.
046	&	Decimal placed after 5th "non-DEL" character in this channel.
047	'	Decimal placed after 6th "non-DEL" character in this channel.
050	(	Decimal placed after 7th "non-DEL" character in this channel.
072	:	Indicates a "Scale factor" channel.[2]
073	;	Indicates a "Digital" channel.[2] A "Digital" type channel is indicated if the first ASCII character in the channel is any of the following: !;</+–=>$%&'(
077	?	This channel is not displayed (ignore).[2]
137	_	Do not leave a space; wait for next character or next channel.
177	DEL	Do not leave a space; wait for next character or next channel.

[1]These ASCII characters are not displayed on the CRT.
[2]The :; and ? ASCII characters are used only as the first character in a channel.

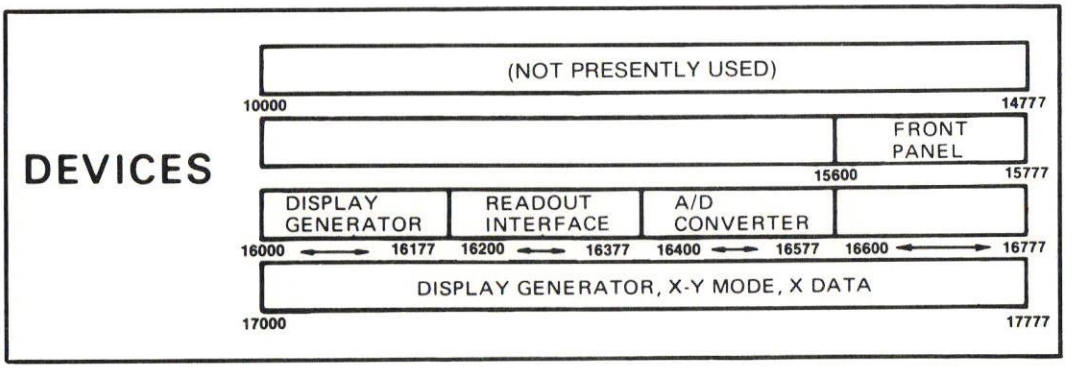
1609-10

Code for Reading Operational Commands (generated by plug-ins).

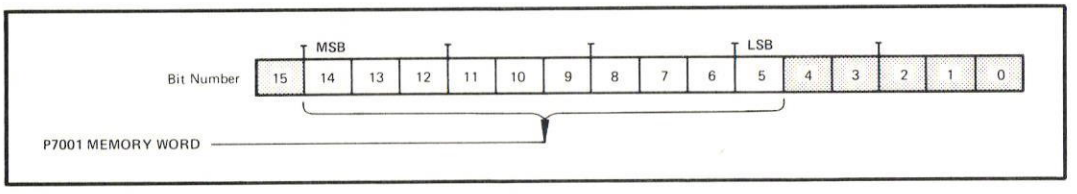
DPO Interface Concepts



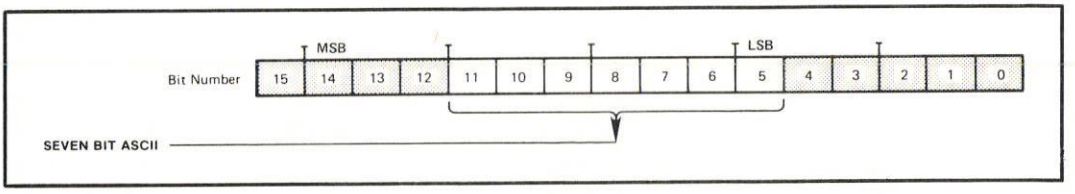
4K Memory Map.



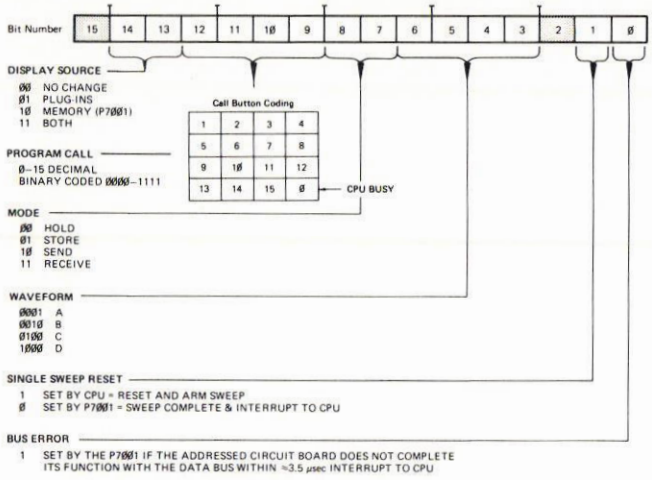
Device Address Map.



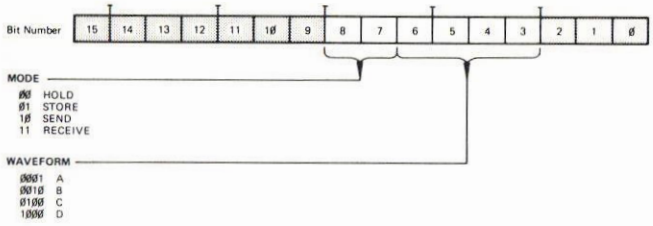
P7001 Memory Word.



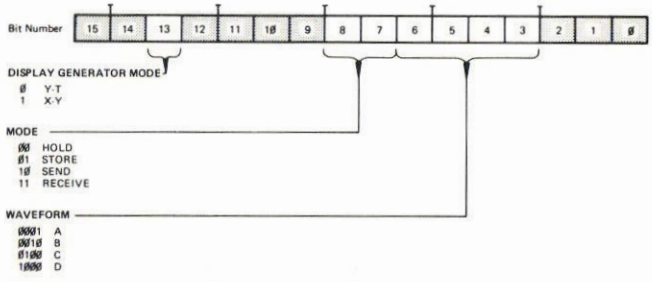
Readout ASCII Data.



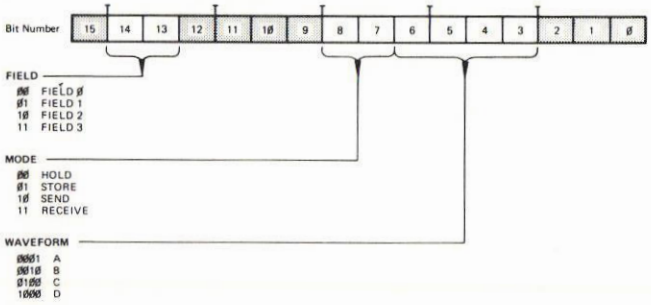
(a). FRONT PANEL STATUS WORD FORMAT.



(b). A/D CONVERTER STATUS WORD FORMAT.



(c). DISPLAY GENERATOR STATUS WORD FORMAT.



(d). READOUT INTERFACE STATUS WORD FORMAT. 1603-27

P7001 Status Words.

APPENDIX B

TYPICAL COMPUTER/CP BUS INTERFACE

The following describes a typical computer/CP Bus Interface for use with the DPO/CP Bus Interface. It is not intended to be applicable to any one computer but to aid in the design of an interface that will meet the requirements of interfacing a specific computer to the DPO/CP Bus Interface.

In the lower right hand corner of the diagram is a typical data latch for one data bit (bit 0 is shown). Sixteen of these data latches are required to transfer data between the DPO/CP Bus Interface and the computer.

The signals shown on the pins of J02 are connected to the DPO/CP Bus Interface, the remainder of the signals are connected to the computer or between the interface and the data latches. The signal levels are TTL and positive logic.

Sending the Address to the DPO from the Computer

First, the address of the circuit card in the DPO or the DPO memory location must be loaded into the Data Latches (see typical data latch) 0 through 12 by asserting the bit pattern of the desired address and a LOAD command from the CPU. Next, the following lines must be asserted: AAR, DPO Address Register; WRITE, to indicate the data is going to the DPO; and START. Since AAR, START, and WRITE are asserted the Q outputs of flip-flops U20, U26, and U29 will be high. The high on the Q output of U20 generates $\overline{\text{CBBZY}}$ (Common Bus Busy) at pin 24 of J02; the Q outputs of U26 and U29 are gated through U28 and generates $\overline{\text{BQ1}}$, which indicates a transfer of address to the DPO; the Q output of U29 generates a LOAD DATA signal which goes to the Typical Data Latch and gates the data onto the CP Bus (in the typical data latch shown, only data bit 0 is shown and it is gated through U53). The Q output of U29 also fires monostable U30, U31 is clocked on the trailing edge of the pulse from U30. The Q output of U31 goes high and is gated through U34, generating $\overline{\text{DSNT}}$ (Data Sent) at pin 28 of J02. The $\overline{\text{DSNT}}$ signal indicates that data is valid on CP Bus bits 0 through 16. The pulse width of U30 is sufficient to allow the data on the CP Bus to be sufficiently settled and deskewed before the $\overline{\text{DSNT}}$ line is driven. The network consisting of U32, U33, the 180 ohm resistor and the 0.001 microfarad capacitors are to ensure that U35, which is the receiver for the $\overline{\text{DSNT}}$ line, will not be activated during the time either immediately before or immediately after the $\overline{\text{DSNT}}$ line is being driven.

The DPO/CP Bus Interface will acknowledge the fact that it has latched the address or the data on the CP Bus bit lines 0 through 12 into the DPO Address Register by asserting $\overline{\text{DRCV}}$ (Data Received) pin 21 of J02. $\overline{\text{DRCV}}$ is gated through U38 and fires monostable, U39. The pulse width of U39 must be fairly long as it is going to be used to clear several flip-flops. Since WRITE is still asserted both inputs to U48 are now high and this generates the DONE signal. The DONE signal indicates to the computer that the action is complete. The Q output of U39 is also gated through U50 and clears flip-flops U31, U29, U26, and U25.

The computer acknowledges the receipt of the DONE signal by issuing a ACTION COMPLETE signal. This signal is gated through U44 and resets the DONE flip-flop consisting of U45 and U46. Also the output of U44 resets U20 which is the $\overline{\text{CBBZY}}$ flip-flop. This completes the transfer of data to the DPO Address Register.

Sending Data to the DPO from the Computer

Data is transferred to the DPO Data Register in much the same way as the address was transferred to the DPO Address Register except ADR is asserted in place of AAR; START and WRITE are both asserted. Since ADR is asserted the Q output of U25 will be high and the Q output of U26 will be low. The Q output of U25 and U29 are gated through U27, generating $\overline{\text{BQ2}}$ at pin 23 of J02. $\overline{\text{BQ2}}$ indicates a transfer of data to the DPO. The remainder of the circuitry functions in the same manner as was previously described when transferring the address to the DPO.

Sequence for the Computer to Read Data from the DPO

When data is to be read from the DPO, the computer interface must go through two bus cycles. The first bus cycle is very similar to the previously described bus cycle; ADR, START, and READ are now asserted. Since WRITE is not asserted, U24 will not clock U25 or U26 but U23 will preset U25 and U26 causing their Q outputs to be high. The Q outputs of U25, U26, and U29 are gated through U27 and U28, asserting $\overline{\text{BQ1}}$ and $\overline{\text{BQ2}}$, indicating that this is a read cycle. $\overline{\text{CBBZY}}$ and $\overline{\text{DSNT}}$ will be asserted in the previously described manner.

When the DPO/CP Bus Interface receives $\overline{\text{BQ1}}$, $\overline{\text{BQ2}}$, and $\overline{\text{DSNT}}$, it will respond by sending $\overline{\text{DRCV}}$, which will fire monostable U39. Since WRITE is not asserted, DONE will not be generated but the output of U39 will be gated through U50 clearing U31, U29, U26, and U25 (note that $\overline{\text{CBBZY}}$ is still asserted). This places the CPU interface in a state to receive data from the DPO/CP Bus Interface.

When the DPO/CP Bus Interface has acquired the data from the DPO and placed it on the CP Bus, it will assert $\overline{\text{DSNT}}$. $\overline{\text{DSNT}}$ will be gated through U35 and U51 and generate $\overline{\text{CLOCK DATA}}$. $\overline{\text{CLOCK DATA}}$ goes to the Data Latch and is shown, in the Typical Data Latch, clocking $\overline{\text{CB0}}$ (Common Bus bit 0) from the DPO/CP Bus Interface through U56 to the CPU. In addition to asserting $\overline{\text{CLOCK DATA}}$, $\overline{\text{DSNT}}$ is gated through U47 and sets the DONE flip-flop. When DONE is set, the computer will indicate that the data has been accepted by asserting ACTION COMPLETE. ACTION COMPLETE will be gated through U37 and assert $\overline{\text{DRCV}}$ to the DPO/CP Bus Interface; also it is gated through U44 and clears the DONE flip-flop and $\overline{\text{CBBZY}}$ flip-flop.

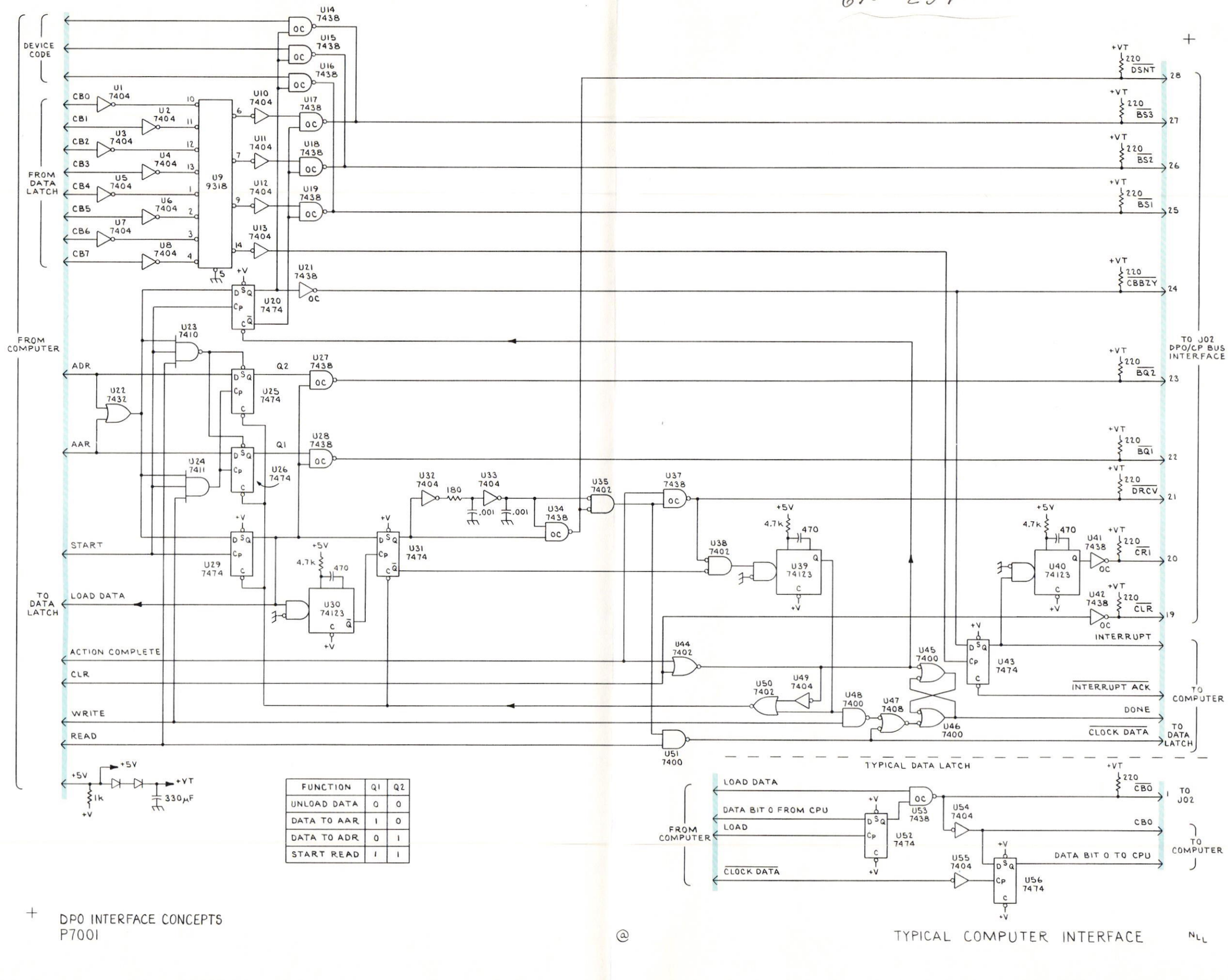
In the previously described sequences, if there is more than one DPO on the line, the CPU may put the device code of the addressed DPO on the line when $\overline{\text{CBBSY}}$ is asserted. The device code will be gated through U14, U15, and U16 and set $\overline{\text{BS1}}$ through $\overline{\text{BS3}}$.

Interrupts

The DPO interrupts the CPU by asserting one of the CP Bus bits $\overline{CB0}$ through $\overline{CB7}$, if $\overline{CBBZY}$ is not asserted. The interrupting device will interrupt on the CP Bus line that is the decimal representation of its device number, e.g., device number 5 will interrupt on $\overline{CB5}$. The received interrupt is inverted through the Data Latch (U54 of Typical Data Latch) and then goes through inverters U1—U8 to the inputs of U9, a Priority Encoder, which encodes the binary representation of the interrupting device and asserts $\overline{BS1}$ through $\overline{BS3}$. When any one or combination of the inputs to U9 are low, pin 14 on the output will be low. This low is inverted through U13 and clocks U43. Since $\overline{CBBZY}$ is not asserted, the Q output of U43 goes high and generates the signal INTERRUPT to the CPU. Also the Q output of U43 fires the monostable U40, which will issue the signal $\overline{CRI}$ (Clear Interrupt) acknowledging the interrupt from the DPO. The DPO will respond by releasing the CP Bus line ($\overline{CB0}$—$\overline{CB7}$).

Notice that a CLR (clear) signal, developed at the computer, is coupled through U42 to pin 19 of J02. This signal, when asserted, sets the DPO to the idle state. It is recommended that this signal be available from the front panel of the computer and/or a programmable function within the computer software.

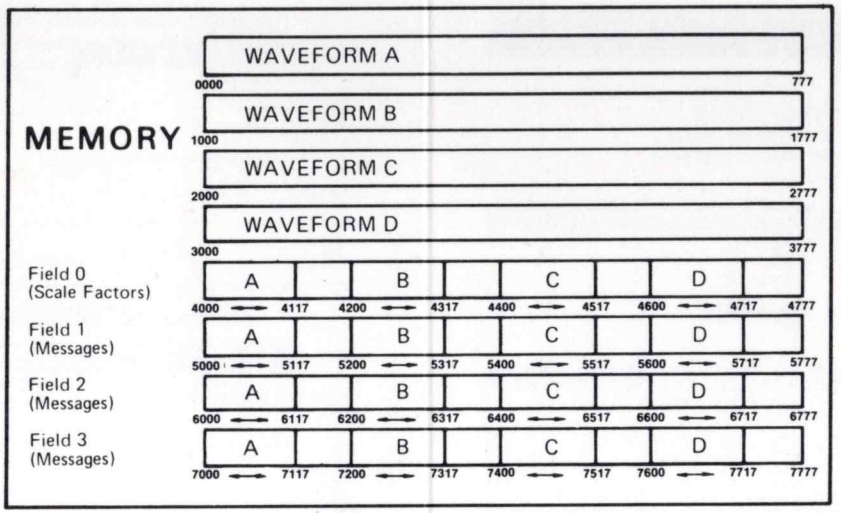
670-2390-01

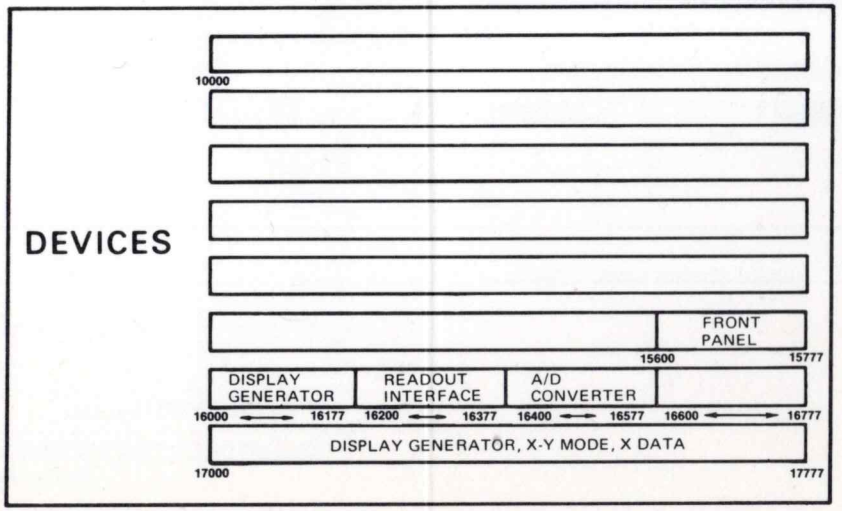


FUNCTION	Q1	Q2
UNLOAD DATA	0	0
DATA TO AAR	1	0
DATA TO ADR	0	1
START READ	1	1

+ DPO INTERFACE CONCEPTS
P7001

@ TYPICAL COMPUTER INTERFACE NLL





DPO INTERFACE CONCEPTS

PROGRAMMING AID

TEKTRONIX®

PA-1971

Remove programming aid at perforation. Fold along crease as shown:

FOLD

FOLD

For additional copies of this programing aid, contact your local Tektronix Digital Applications Engineer.

PA-1971

ASCII* (OCTAL)	CRT DISPLAY	ASCII* (OCTAL)	CRT DISPLAY	ASCII* (OCTAL)	CRT DISPLAY	ASCII* (OCTAL)	CRT DISPLAY
040	SPACE	067	7	107	G	124	T
041(!)*	↓	070	8	110	H	125	U
053	+	071	9	111	I	126	V
055	–	074	<	112	J	127	W
056	.	075(=)*	^	113	K	130	X
057	/	076	>	114	L	131	Y
060	0	100(@)*	Ω	115	M	132	Z
061	1	101	A	116	N	143	c
062	2	102	B	117	O	144	d
063	3	103	C	120	P	155	m
064	4	104	D	121	Q	156	n
065	5	105	E	122	R	160	p
066	6	106	F	123	S	165(u)*	μ

*ASCII character is different from displayed character.

ASCII Codes for CRT Character Display.

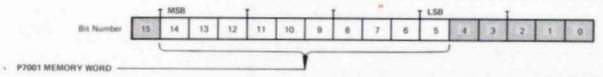
ASCII OCTAL CODE	ASCII Char.[1]	Notes (Refer to 7704A Manual for details)
044	$	Decimal placed after 3rd "non-DEL" character in this channel.
045	%	Decimal placed after 4th "non-DEL" character in this channel.
046	&	Decimal placed after 5th "non-DEL" character in this channel.
047	'	Decimal placed after 6th "non-DEL" character in this channel.
050	(	Decimal placed after 7th "non-DEL" character in this channel.
072	:	Indicates a "Scale factor" channel.[2]
073	;	Indicates a "Digital" channel.[2] A "Digital" type channel is indicated if the first ASCII character in the channel is any of the following: !;<-/+=>$%&'(
077	?	This channel is not displayed (ignore).[2]
137	_	Do not leave a space; wait for next character or next channel.
177	DEL	Do not leave a space; wait for next character or next channel.

[1]These ASCII characters are not displayed on the CRT.
[2]The ; and ? ASCII characters are used only as the first character in a channel.

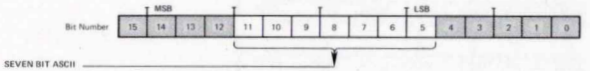
Code for Reading Operational Commands. (Generated by Plug-Ins)

MEMORY DATA WORDS

AD Converter Output:
Display Generator Input:
Computer Input/Output:

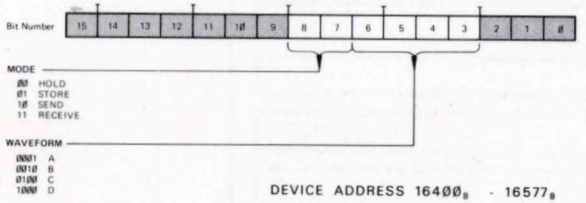


Readout ASCII Data:



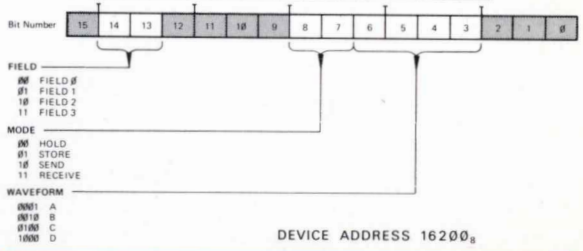
STATUS WORDS

ANALOG-TO-DIGITAL CONVERTER STATUS WORD FORMAT



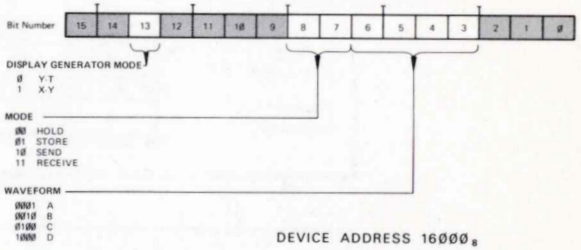
DEVICE ADDRESS $1640\emptyset_8$ - $1657\emptyset_8$

READOUT INTERFACE STATUS WORD FORMAT



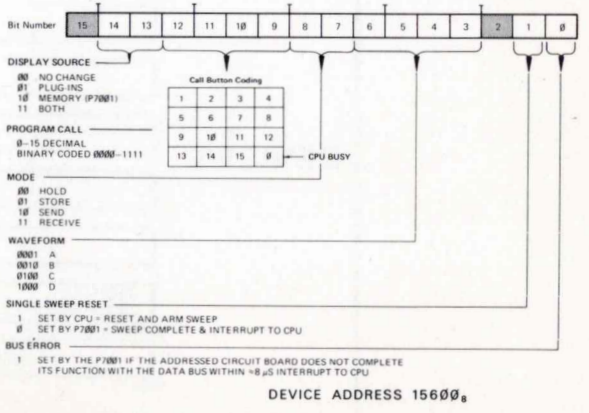
DEVICE ADDRESS $1620\emptyset_8$

DISPLAY GENERATOR STATUS WORD FORMAT



DEVICE ADDRESS $1600\emptyset_8$

FRONT PANEL STATUS WORD FORMAT



DEVICE ADDRESS $1560\emptyset_8$