Tektronix®

PM 108

PERSONALITY MODULE FOR Z8002 MICROPROCESSOR

INSTRUCTION MANUAL

Tektronix®
COMMITTED TO EXCELLENCE

PM 108
PERSONALITY MODULE FOR Z8002 MICROPROCESSOR

INSTRUCTION MANUAL

Tektronix, Inc.
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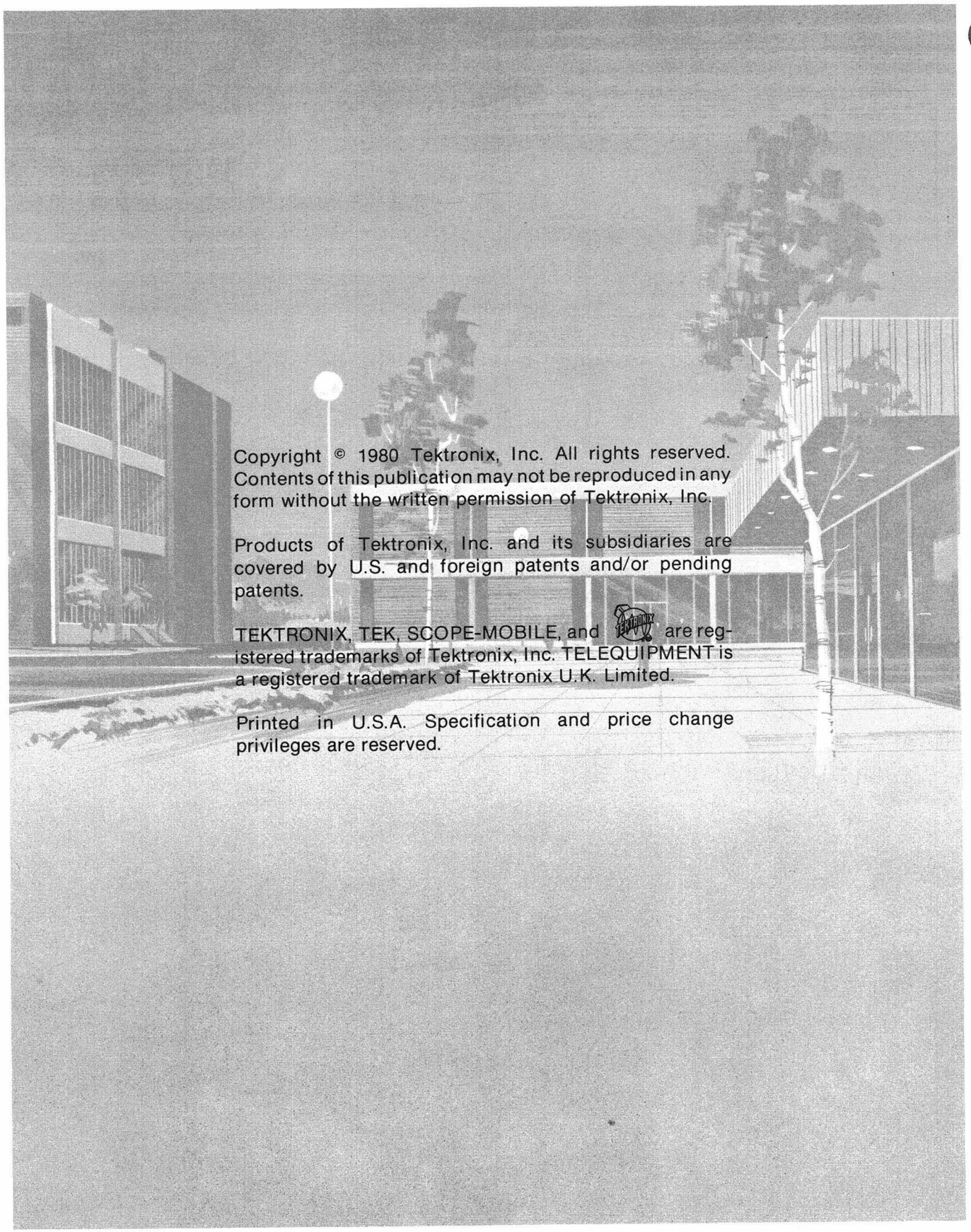

ABOUT THIS MANUAL

This manual describes operation and service of the PM 108 Personality Module. The first part of the manual, the operator's part, describes connection of the personality module to the logic analyzer, connection of the personality module to the system under test (S.U.T.) and other information necessary for operation. The second part, the service part, is found after the colored divider page. That information is intended for use by qualified personnel in servicing the personality module. It contains circuit descriptions, diagnostic techniques, schematic diagrams, and parts lists. Refer to the Table of Contents for the specific location of information.

The PM 108 supports the Z8002 microprocessor.

Since the PM 108 is a tool to aid design of Z8002-based products, Tektronix assumes that the reader has access to a manual relating to this microprocessor.

This manual often refers to a "logic analyzer". This means the 7D02 Logic Analyzer. It is assumed that the reader has access to a Tektronix 7D02 Operator's Manual and 7D02 Service Manual.

Throughout this manual, references are made to signals. The following conventions should be kept in mind:

1. The slash (/) preceding a signal name indicates the signal is active or asserted in the low state. For example /AS is an active low signal. If a portion of a signal name is preceeded by a slash, that portion of the signal is an active low signal, for example R/W implies 1 = read, 0 = write.

2. The components are numbered with assembly number, then component number. For example, A1U3XXX is a component on assembly A1, the top board in the personality module pod. (A2 is the bottom board.) In Section 8, on the schematic for Board 1, component A1U3XXX is shown without the assembly number, e.g., U3XXX.

3. For more information about signal lines, consult the Signal Glossary in Section 10.

TABLE OF CONTENTS

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

TABLE OF CONTENTS (cont)

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LIST OF ILLUSTRATIONS

OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

Terms In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols In This Manual

This symbol indicates where applicable cautionary or other information is to be found.

Symbols As Marked on Equipment

ATTENTION—refer to manual.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Operate Without Covers

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.

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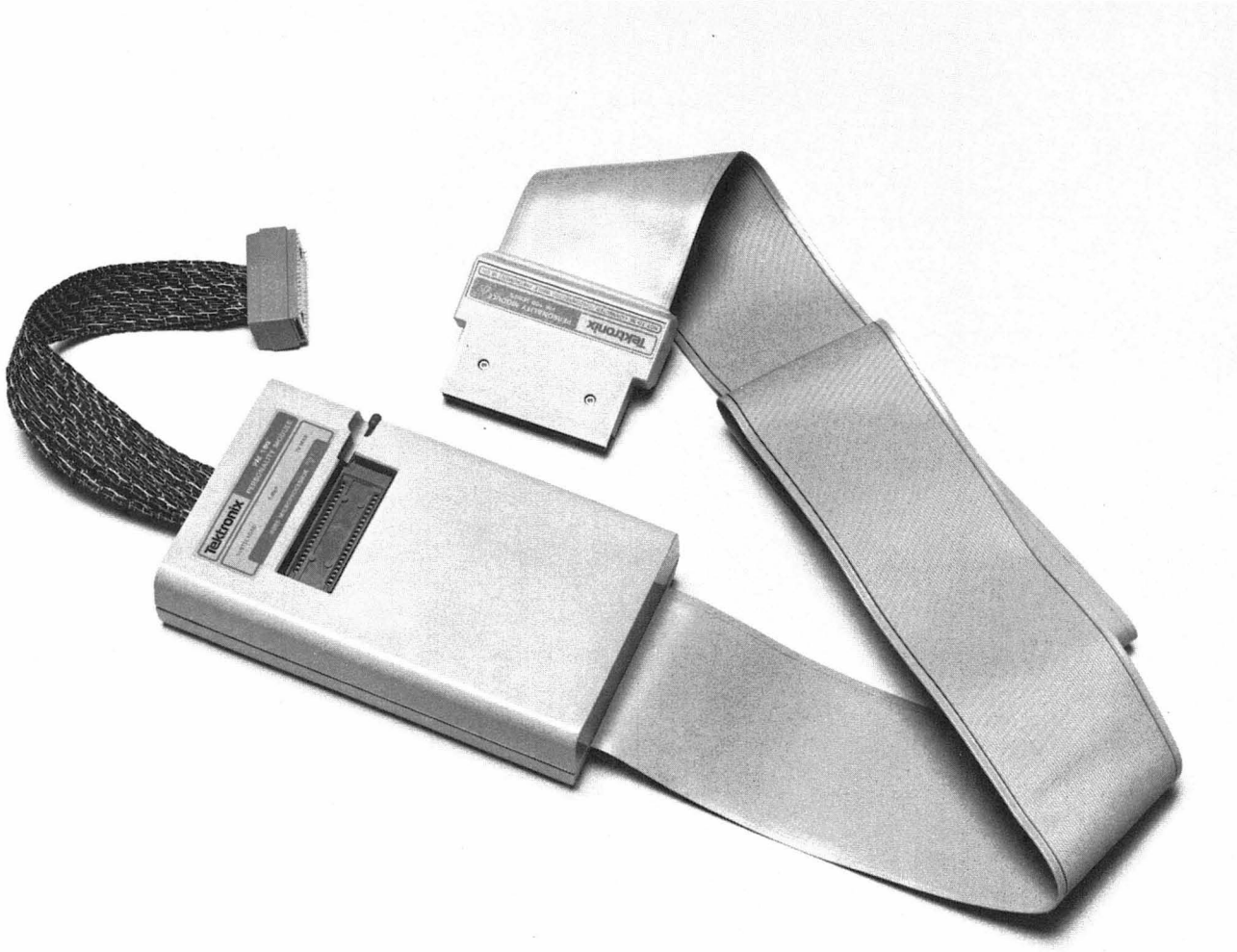
SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Disconnect power before removing protective panels, soldering, or replacing components.



3472-23

The PM 108 Personality Module.

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INTRODUCTION TO THE PM 108

The PM 108 Personality Module collects data from a Z8002-based system-under-test (S.U.T.) and transfers it to a Tektronix logic analyzer in a format that the logic analyzer can interpret.

The microprocessor in the S.U.T. is removed and plugged into the personality module. The microprocessor plug on the personality module is then inserted into the S.U.T., replacing the microprocessor. The microprocessor then drives the S.U.T. as before, through the personality module. This allows the logic analyzer to acquire data by monitoring the address, control, data, and clock lines. The personality module also generates additional information needed by the logic analyzer.

Physically, the PM 108 personality module consists of a circuitry pod with a ribbon cable and logic analyzer plug on one end, and a twisted-pair woven cable and microprocessor plug on the other end.

To operate with the PM 108, the 7D02 requires the expansion option.

The personality module pod is an interface assembly that "personalizes" the logic analyzer to work with the Z8002 microprocessor.

a. A zero-insertion-force (ZIF) socket on the pod for the Z8002 microprocessor from the system under test.

b. Firmware that allows the logic analyzer to disassemble the information it receives into the mnemonics of the Z8002 and set up displays.

c. Circuitry to generate the state clock, and other inputs to the logic analyzer.

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3472-14

Fig. 1-1. The PM 108 Personality Module.

OPERATING INSTRUCTIONS FOR THE PM 108 PERSONALITY MODULE

STORAGE AND INSTALLATION OF PERSONALITY MODULE

Storing the Personality Module

When storing the Personality Module (P.M.), protect the P.M. microprocessor plug with the plastic protector. This prevents damage to the pins during storage and protects the Personality Module from static electricity.

Connecting Personality Module to Logic Analyzer

CAUTION

Always turn the mainframe power switch OFF before connecting the Personality Module to the logic analyzer mainframe. Before removing the microprocessor from your system under test and installing the microprocessor plug, turn off your system power switch. Failure to take this precaution may cause permanent damage to the logic analyzer, the personality module, and the system under test.

1. Turn mainframe power switch to the OFF position.

2. Insert the PM 108 logic analyer plug, label side up, into the socket on the front of the Logic Analyzer.

Connecting Personality Module to the System Under Test (S.U.T.)

1. Turn OFF the power to your S.U.T. and the logic analyzer.

2. Ground yourself to drain static electricity.

3. Remove the microprocessor from your S.U.T. and insert it into the ZIF socket in the Personality Module Pod. Be sure to insert it correctly, with pin 1 of your microprocessor next to the lever on the ZIF socket.

4. Plug the PM microprocessor plug into the empty microprocessor socket on your S.U.T. Again, make sure to insert the plug correctly. Pin 1 of the microprocessor plug is marked with a notch and an arrow.

5. Turn on the logic analyzer mainframe power switch and power up your S.U.T.

NOTE

To save wear to the microprocessor socket on your S.U.T., you may insert another socket into your S.U.T. socket.

A socket appropriate for this purpose is available through your Tektronix Field Office.

USING PERSONALITY MODULE

The 7D02 Operator's Manual provides general operating information for use with all personality modules. The 7D02 operates slightly differently with each different personality module.

This sub-section is devoted to operating the 7D02 with a PM 108 Personality Module.

7D02 Displays

The following 7D02 screen displays contain PM 108-specific elements. For more information about signal lines, consult Section 4, Theory of Operation, and Section 10, Signal Glossary.

- **WD RECOGNIZER Event Format**

  When the PM 108 is attached to the 7D02, the 7D02 WD RECOGNIZER key produces the following display. The radices of the data bus and address bus may be changed with the 7D02 FORMAT key.

```
  TEST 1
1 IF
1   WORD RECOGNIZER #1
1   DATA=XXXX
1   ADDRESS=XXXX
1   IO/M=X IRQ=X FETCH=X R/W=X
1   /BUSAK=X /MREQ=X EXT TRIG IN=X
1   TIMING WR=X
1   THEN DO
1
```

DATA—The 16-bit data bus, normally in hexadecimal, unless changed with the FORMAT key. The logic analyzer stores information from the data bus when a program is run.

ADDRESS—The 16-bit address bus, normally in hexadecimal, unless changed with the FORMAT key. The 7D02 stores information from the address bus when a program is run.

IO/M—The Input-Output/Memory line from the PM 108 to the logic analyzer. If IO/M is in a "1" state, the operation is IO. If in a "0" state, the READ or WRITE is to memory. The logic analyer stores information on this line when a program is run.

IRQ—The Interrupt Request line from the PM 108 to the logic analyzer. When in a high state, IRQ indicates an interrupt request by one or more of the Z8002 interrupts. The logic analyzer stores information on this line when a program is run.

FETCH—The FETCH line from the PM 108 to the logic analyzer. When the FETCH line is high, the first byte of a Z8002 instruction is on the data bus. For the 7D02 to recognize an instruction fetch, the FETCH element requires a 1. The radix for this element is always binary. The logic analyzer stores information on this line when a program is run.

R/W—The buffered read/write line from the Z8002 microprocessor in the ZIF socket. The line tells the user that the microprocessor is in a Read (1) or Write (0) state. The logic analyzer stores information on this line when a program is run.

/BUSAK—The buffered bus request acknowledge line from the Z8002 microprocessor in the ZIF socket. A low on this line indicates that the Z8002 CPU has relinguished the bus in response to a bus request.

/MREQ—The buffered memory request line from the Z8002 in the ZIF socket. A low on this output indicates that a Z8002 CPU transaction with memory is taking place.

- **TRIGGER command format**

```
1   TRIGGER 0-MAIN
1           0-MAIN
1           1-TIMING
1     0-BEFORE DATA
1     0-SYSTEM UNDER TEST CONT.
1     0-STANDARD CLOCK QUAL.
```

The only field of specific interest to the PM 108 user is the "0-STANDARD CLOCK QUAL."

When the cursor is placed on this element, this display appears:

```
0-STANDARD CLOCK QUAL.
  0 STANDARD CLOCK QUAL.
  1 USER CLOCK QUAL.
```

If "1 USER CLOCK QUAL." is selected, the following display appears:

```
1-FALLING EDGE OF CLOCK
  0 RISING EDGE OF CLOCK
  1 FALLING EDGE OF CLOCK
C9-C4 (ANDED CLOCKS)=XXXXXX
0-STANDARD CLK. SYNTHESIS
```

C9-C4, shown in the above example, are PM 108 control lines that may be used to re-define the state clock through clock qualification.

Clock qualification allows the user to select the edge of the S.U.T. master clock on which data is considered to be valid and should be sampled. This qualified S.U.T. clock is used by the logic analyzer to generate the State Clock.

The control lines are as follows:

C9/TWAIT—The output of the Wait State Generator in the personality module.

C8/AS—The buffered address strobe line from the Z8002 microprocessor in the ZIF socket. This line may be used to define ESYNC.

C7/HALT—The halt line generated by the PM 108 in response to halt requests from the system under test or logic analyzer.

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C6/RESET—The buffered line from the Z8002 in the ZIF socket.

C5/MREQ—The buffered line from the Z8002 in the ZIF socket.

C4/BUSAK—The buffered line from the Z8002 in the ZIF socket.

An S.U.T. master clock edge is selected only when the values on all six control lines (C9-C4) simultaneously match the values entered by the user. See Fig. 2-1.

Note the default values of X ("Don't Care") in C9-C4. All S.U.T. master clock edges are selected.

For example, if the display is

1 1-FALLING EDGE OF CLOCK
1 C9-C4 (ANDED CLOCKS)=XXX1XX

then the 7D02 clocks when

1. the Z8002 clock is on the falling edge, and
2. C6 (/RESET) is in its high state.

Notice also the "0-STANDARD CLK. SYNTHESIS" line. When the cursor is moved to this line in the display, the following display occurs:

0 STANDARD CLK. SYNTHESIS
1 USER CLOCK SYNTHESIS

If "USER CLOCK SYNTHESIS" is selected, the following display appears:

0 STANDARD CLK. SYNTHESIS
1 USER CLOCK SYNTHESIS
1—DIVIDE CLOCK BY 1
ESYNC: C6=X OR C8=0
WAIT: C7=X OR C9=0

ESYNC allows synchronization of the logic analyzer clock synthesizer to the timebase of the S.U.T. The ESYNC signal is the reference for both the DIVIDE BY N mode and the DELAY BY N mode.

If USER CLOCK SYNTHESIS is selected in the 7D02 program, the user has a choice of DELAY CLOCK BY N, where N equals 0—4; and DIVIDE CLOCK BY N, where N is 1—4. If the user selects DELAY CLOCK BY N, one state clock will occur for every ESYNC, delayed by N input clock pulses. Refer to Fig. 2-2. If the user selects DIVIDE CLOCK BY N, the state clock will occur on the N-1th input clock pulse after the end of the ESYNC signal, and at one Nth of the frequency of the input clock. The clock continues at that frequency without further ESYNC signals. Refer to Fig. 2-3.

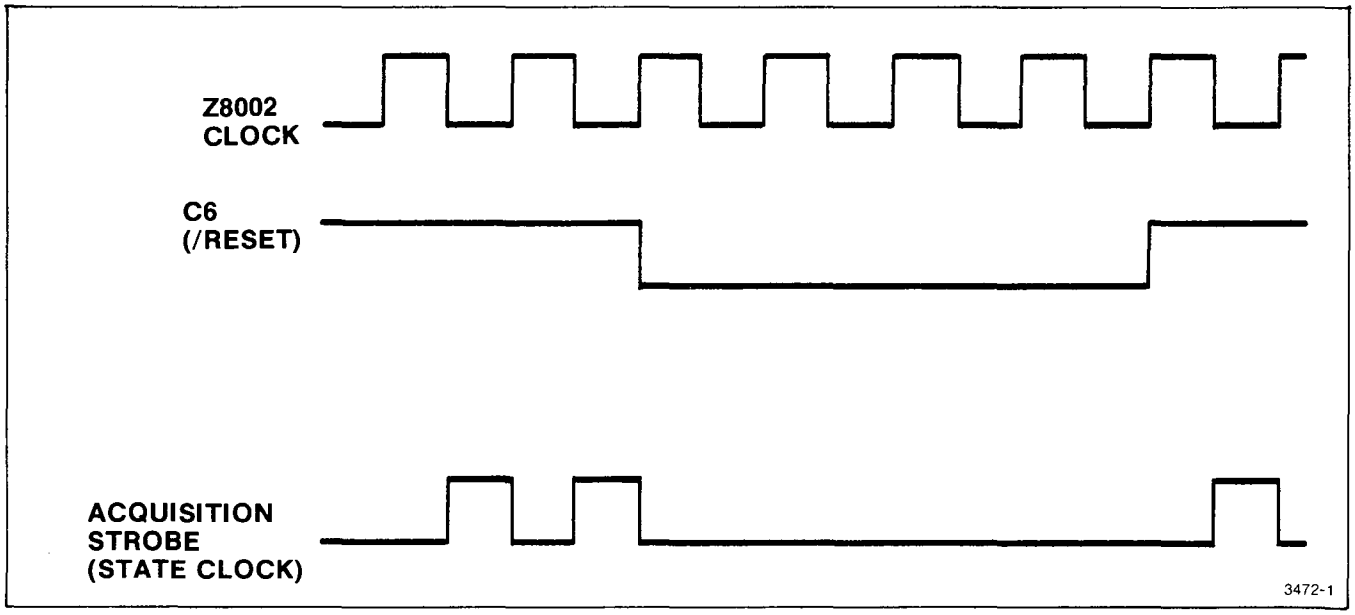

Fig 2-1. State Clock Generation.

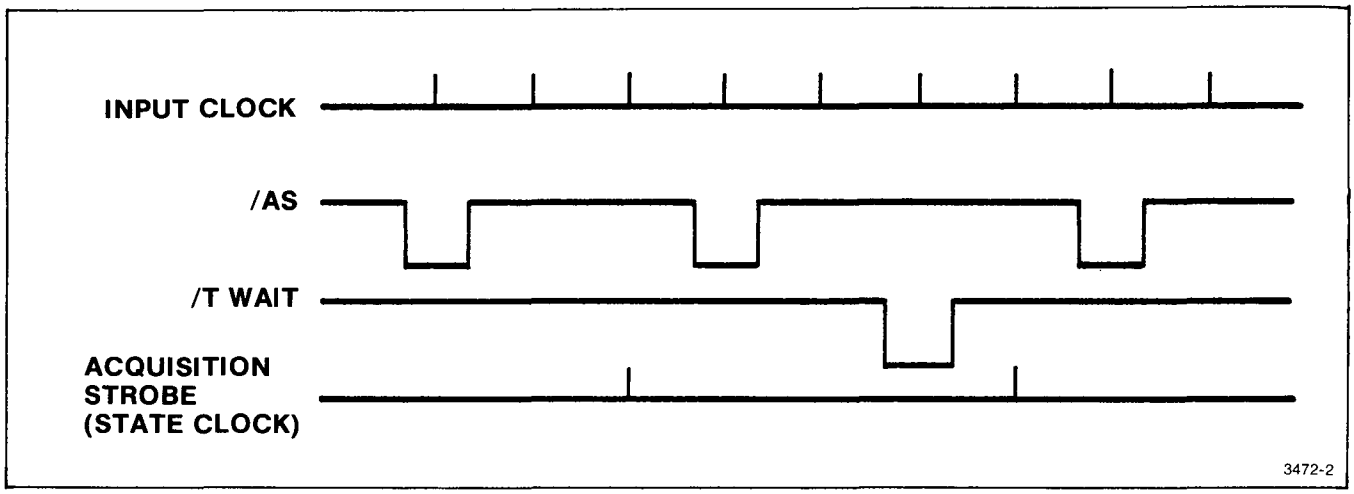

Fig 2-2. User Clock Synthesis—Delay by 2.

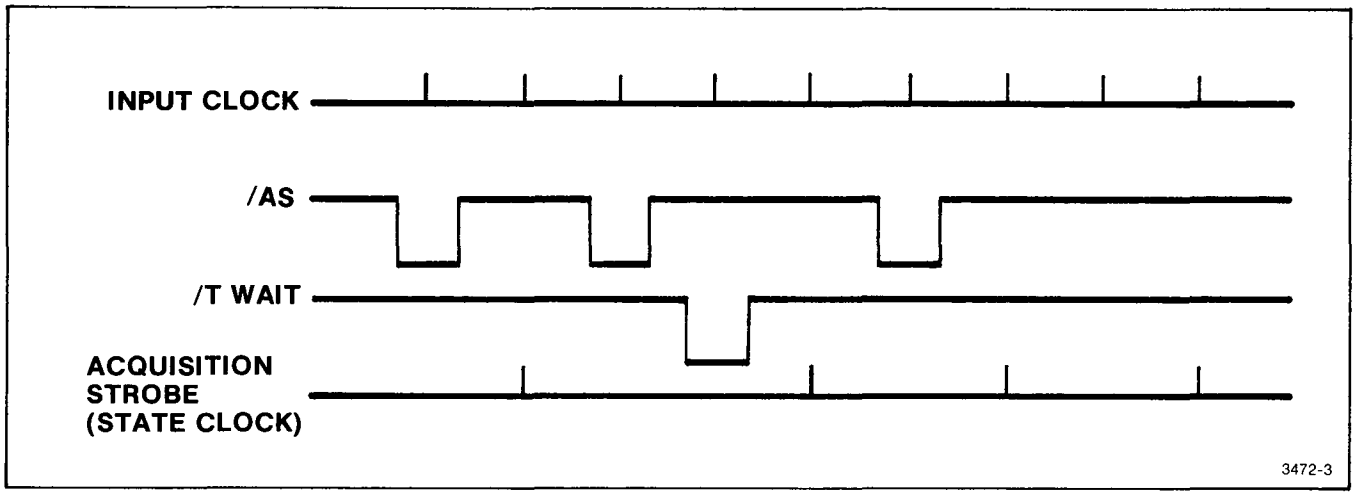

Fig 2-3. User Clock Synthesis—Divide by 2.

ESYNC may be defined as any ORed combination of C6 and C8. The default is C8=0.

WAIT delays the next state clock by one input clock pulse. See Fig. 2-2 and 2-3. The WAIT may be defined as any ORed combination of C7 and C9. The default is C9=0.

For example, here is a portion of a program to synchronize the state clock generator with the beginning of each Z8002 machine cycle and to provide a strobe at T3, allowing for WAIT states.

1—USER CLOCK QUAL.
1—FALLING EDGE OF CLOCK
C9—C4 (ANDED CLOCKS)=00XXXX
1—USER CLOCK SYNTHESIS
0—DELAY CLOCK BY 2

C9 corresponds to the WAIT state at the microprocessor and is generated by a low signal on the /WAIT line. C8 corresponds to the /AS (Address Strobe) pulse that starts each machine cycle. Using these clock qualifiers, the logic analyzer stores once for each machine cycle. See Fig. 2-4.

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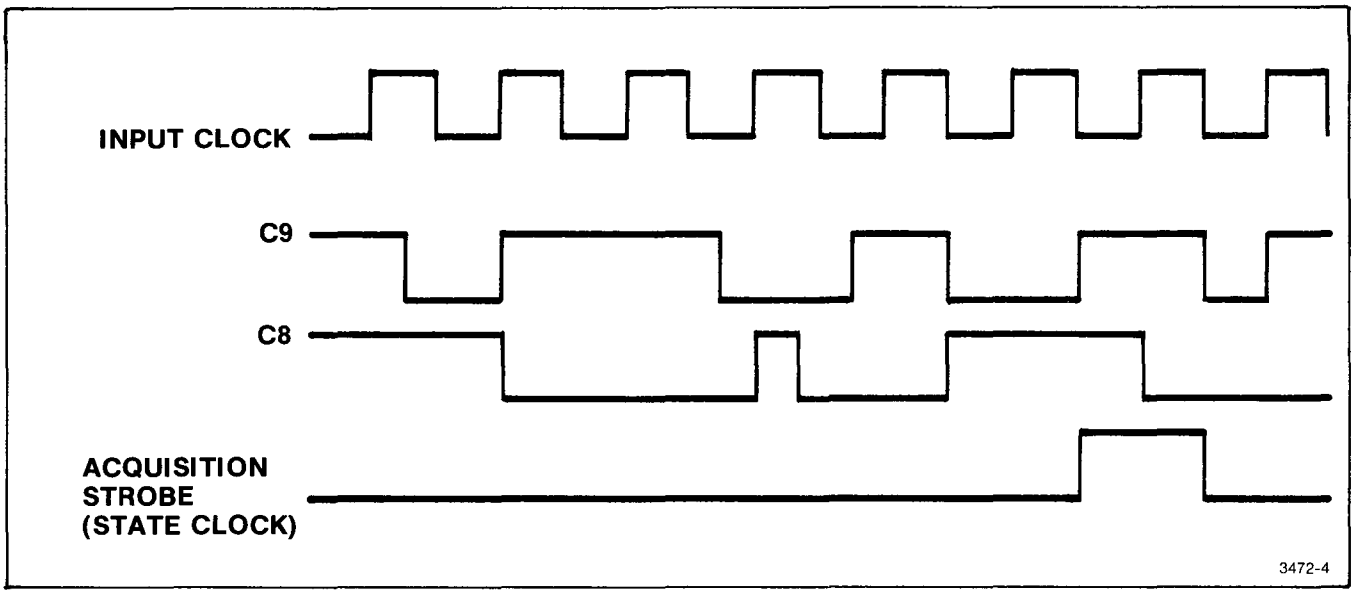

Fig 2-4. User Clock Synthesis, C9=0, C8=0, Delay by 2.

If you change the program to

0—DELAY CLOCK BY 0

you may observe what happens on a bus during each "T State". A state clock is produced for each "T State" and causes each line of the display to be repeated several times. See Fig. 2-5.

NOTE

Redefining the state clock is not a normally recommended procedure, and may produce unpredictable results. If the TRIGGER—MAIN command is deleted from the 7D02 program, the values last entered in the USER CLOCK QUAL. are retained. The default state of STANDARD CLOCK QUAL. is restored after logic analyzer power-up or reselection of 0-STANDARD CLOCK QUAL.

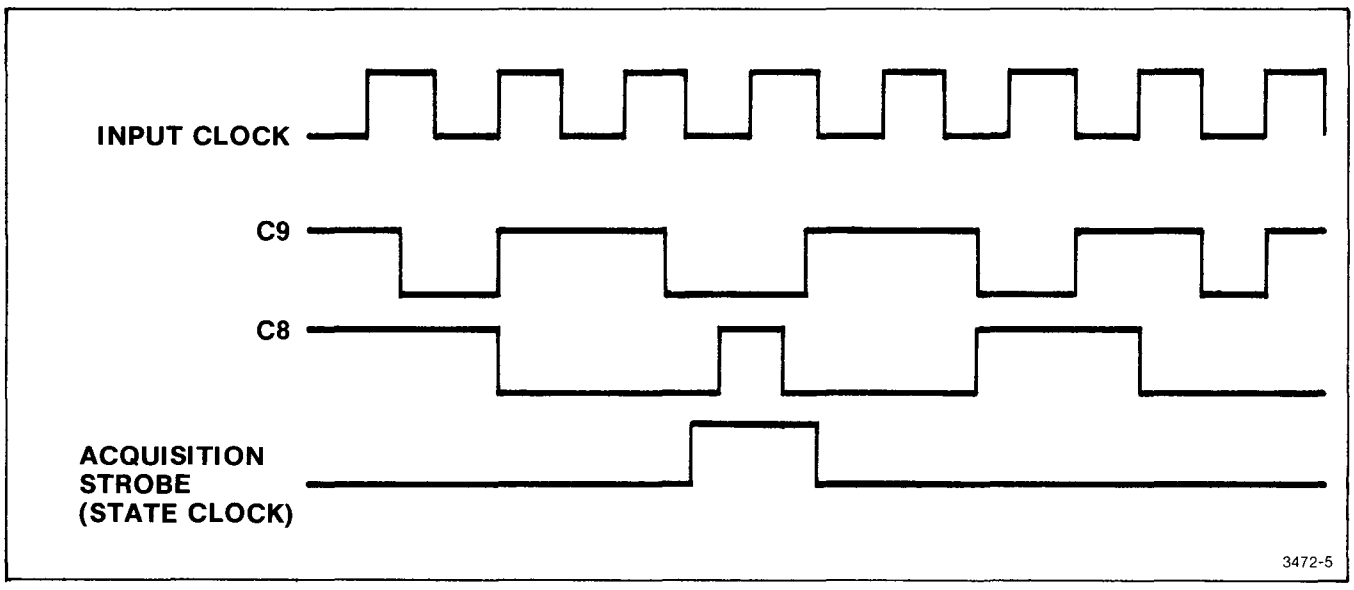

Fig 2-5. User Clock Synthesis, C9=0, C8=0, Delay by 0.

- **FORMAT mode display**

When the PM 108 is installed in a 7D02 logic analyzer with a timing option, the 7D02 FORMAT key produces the following default display.

```
TIMING OPTION WORD RECOGNIZER
    0—BINARY
WORD RECOGNIZER ADDRESS FIELD
    2—HEX
WORD RECOGNIZER DATA FIELD
    2—HEX
TIMING OPTION DATA DISPLAY
    0—BINARY
ADDRESS FIELD DISPLAY
    2—HEX
DATA FIELD DISPLAY
    2—HEX
HIGHLIGHT MEMORY DIFFERENCES?
    1—NO
DISPLAY GLITCHES?
    0—YES
TIMING OPTION DATA INVERSION
    DATA=00000000
```

The WORD RECOGNIZER ADDRESS FIELD menu sets the radix for the ADDRESS field in the WD RECOGNIZER display. Its default state is hexadecimal. It does not affect the display of acquired data.

The WORD RECOGNIZER DATA FIELD menu sets the radix for the DATA field in the WD RECOGNIZER display. Its default state is hexadecimal. It does not affect the acquired data display.

The ADDRESS FIELD DISPLAY sets the radix for the acquired address bus values when displayed in Absolute display mode. Its default radix is hexadecimal.

The DATA FIELD DISPLAY sets the radix for the acquired data bus values when displayed in Absolute display mode. Its default radix is hexadecimal.

- **Absolute Display of Acquired Data**

The 7D02 with the PM 108 produces an Absolute display format like the one below unless the 7D02 FORMAT key has been used to change the radices:

LOC	ADDRESS	DATA	STATUS	IRQ
012	0764	43C4	FETCH N	0
013	43C4	0000	DAT MEM R	0
014	0766	E6FB	FETCH 1	0
015T	075E	6100	FETCH 1	0
016	0760	43C6	FETCH N	0
017	43C6	0000	DAT MEM R	0
018	0762	4B00	FETCH 1	0
019	0764	43C4	FETCH N	0
020	43C4	0000	DAT MEM R	0
021	0766	E6FB	FETCH 1	0
022	06BE	06BE	REFRESH R	0
023	075E	6100	FETCH 1	0
024	0760	43C6	FETCH N	0
025	43C6	0000	DAT MEM R	0
026	0762	4B00	FETCH 1	0
027	0764	43C4	FETCH N	0
028	43C4	0000	DAT MEM R	0
029	0766	E6FB	FETCH 1	0
030	075E	6100	FETCH 1	0

LOC is a decimal number, 0-255, indicating the location in 7D02 acquisition memory. In order of acquisition, 000 is the oldest acquired data, and 255 is the newest.

ADDRESS is a value in the Z8002 address bus. Its default radix is hexadecimal unless changed with 7D02 FORMAT key.

DATA is value on the Z8002 data bus. Its default radix is hexadecimal unless changed with 7D02 FORMAT key.

STATUS is the execution status. The status bits are decoded for each acquisition memory location and displayed along with an "R" for "READ" or a "W" for "WRITE".

Status Definitions

Display	Remarks
- - - - - - -	Invalid or Reserved Status
EPU XFR	Transfer to/from External Processing Unit
FETCH 1	Instruction Fetch 1st Word
FETCH N	Instruction space access
EPU STK	Stack Memory Request (EPU)
EPU DAT	Data Memory Request (EPU)
STK MEM	Stack Memory Request
DAT MEM	Data Memory Request
VI ACK	Vectored Interrupt Acknowledge
NVI ACK	Non-vectored Interrupt Ack.
NMI ACK	Non-maskable Interrupt Ack.
SPL I/O	Special I/O Reference
I/O	Input/Output Reference
REFRESH	Memory Refresh
INT OPR	Internal Operation

IRQ is the value on the interrupt request line.

Selecting binary format with the 7D02 FORMAT key, changes the absolute display format to the following:

```
LOC:001
  ADDR:A009              IRQ:0
  DATA:010111100001001   NVI ACK W
```

Notice the DATA and STATUS information is moved to the second line.

- **Mnemonic Disassembly Display of Acquired Data**

The 7D02 when used with the PM 108 produces a mnemonic disassembly display like the one below. The Mnemonic Disassembly Display cannot be changed with the 7D02 FORMAT key.

LOC	ADDR	OPERATION	IRQ
012	0764	43C4 FETCH N	0
013	43C4	0000 DAT MEM R	0
014	0766	JR Z, 075E	0
015T- - - -	075E - - -	LD RO, 43C6 - - - - - - - -	0
016	0760	43C6 FETCH N	0
017	43C6	0000 DATA MEM R	0
018	0762	CP RO, 43C4	0
019	0764	43C4 FETCH N	0
020	43C4	0000 DAT MEM R	0
021	0766	JR Z, 075E	0
022	06BE	06BE REFRESH R	0
023	075E	LD RO, 43C6	0
024	0760	43C6 FETCH N	0
025	43C6	0000 DAT MEM R	0
026	0762	CP RO, 43C4	0
027	0764	43C4 FETCH N	0
028	43C4	0000 DAT MEM R	0
029	0766	JR Z, 075E	0
030	075E	LD RO, 43C6	0

LOC is a decimal number, 0-255, indicating the location in 7D02 acquisition memory. In order of acquisition, 000 is the oldest acquired data, and 255 is the newest.

ADDR is a value in the Z8002 address bus. Its radix is hexadecimal.

OPERATION—on FETCH 1 Cycles is either

The opcode mnemonic and disassembled operands of the Z8002 instruction whose opcode was fetched on that cycle.

or

Three asterisks and a hexadecimal value in parentheses like this:

LOC	ADDR	OPERATION	IRQ
010	6282 ***	(9D82)	0

Three asterisks following the ADDR column indicate an invalid opcode. The value on the data bus is shown in hexadecimal in parentheses on the same line.

or

Asterisks in the OPERATION column of a mnemonic display indicate no FETCH N data was stored at that location. The PM 108 decodes and displays information by first checking for the mnemonic type, then displaying it. If the mnemonic requires more data, the program advances to the next word of stored information and tests to determine whether it is a FETCH N cycle or a READ/WRITE cycle. If the word is a READ/WRITE cycle, asterisks are displayed to indicate that no data has been stored for the second part of the opcode. If it is a FETCH N cycle, then the operand decoding and display is continued. This display may appear on any cycle.

OPERATION—on all other cycles

The value (in hex) that was on the data bus on that cycle. The cycle type is also identified with the status mode, and a READ or WRITE statement.

IRQ is the value on the Interrupt Request line.

Qualifiers

If you choose to change the qualifiers for the state clock or condense the data stored in memory by using data qualification in a program, you must be careful to interpret the displayed information correctly. As an example, assume a portion of an assembly level program is made up of the following steps:

```
        LABEL1 EQU 43C6
        LABEL2 EQU 43C4
START   LD RO, LABEL1
        CP RO, LABEL2
        JR Z,START
```

The normal disassembly would be as follows (LOC, ADDR, and IRQ were chosen at random):

LOC	ADDR	OPERATION	IRQ
056	075E	LD RO, 43C6	0
057	0760	43C6 FETCHN	0
058	43C6	000D DATA MEM R	0
059	0762	CP RO, 43C4	0
060	0764	43C4 FETCHN	0
061	43C4	000D DATA MEM R	0
062	0766	JR Z, 075E	0

If you choose to qualify on FETCH cycles only, for example, the disassembly would look like this:

LOC	ADDR	OPERATION	IRQ
025	075E	LD RO, 43C6	0
026	0760	43C6 FETCHN	0
027	0762	CP RO, 43C4	0
028	0764	43C4 FETCHN	0
029	0766	JR Z, 075E	0

Note that the Data Memory Reads are missing.

NOTE

Correct mnemonic disassembly of acquired data is guaranteed only if 1) data qualification is not used at all (so that all cycles are stored) or 2) if data qualification is used, all Fetch Cycles are stored.

This may be accomplished by using the QUALIFY block. Store only on Word Recognizer N, where the Word Recognizer is set to all "Don't Care", except FETCH = 1. This guarantees that all instruction fetches are stored.

Z8002 Instruction Set

The table below provides a detailed description of the Z8002 instruction set. This information is useful in comparing actual with expected results during debug of both software and hardware.

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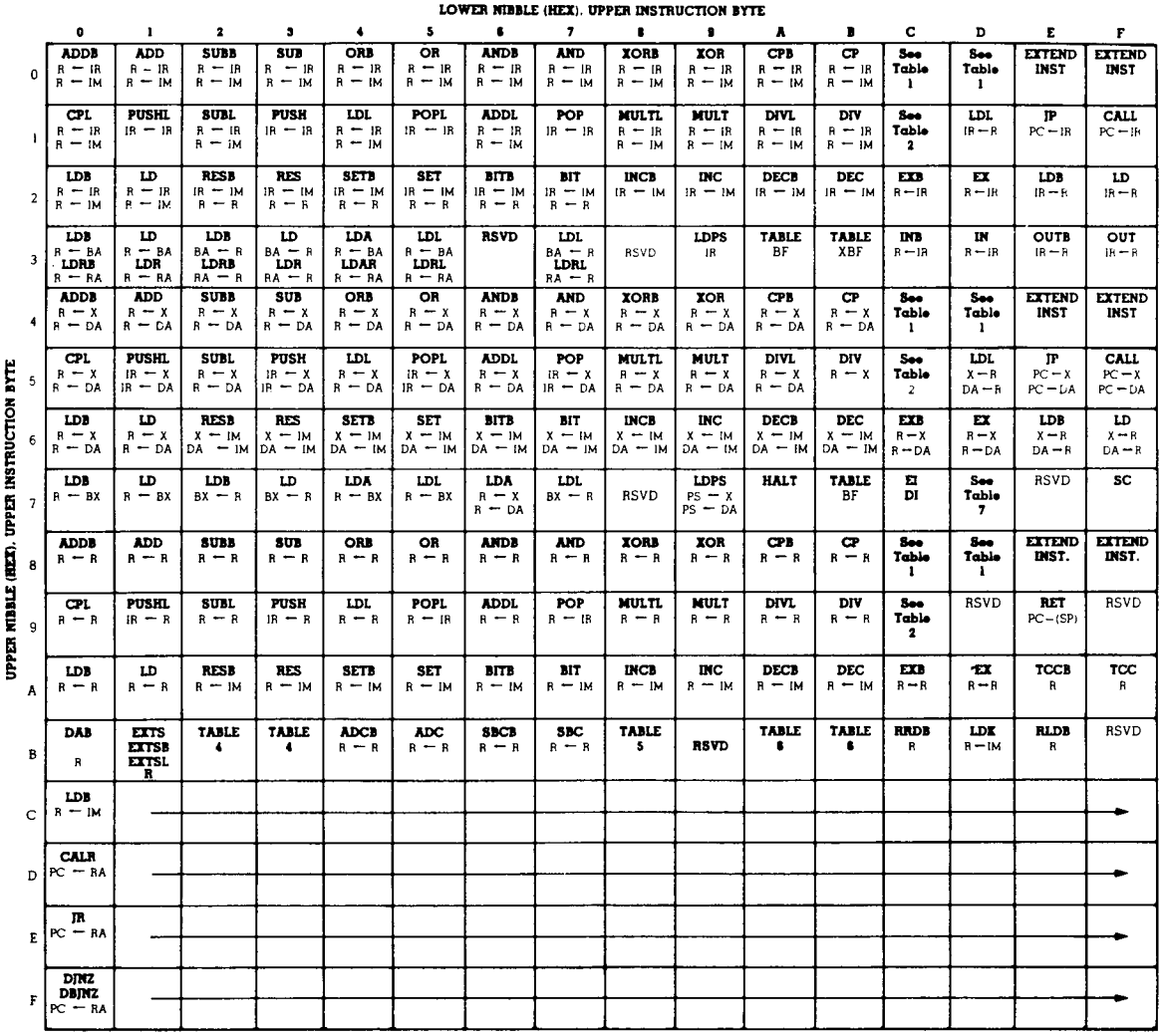


UPPER NIBBLE (HEX), UPPER INSTRUCTION BYTE	LOWER NIBBLE (HEX), UPPER INSTRUCTION BYTE															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	**ADDB** R ← IR R ← IM	**ADD** R ← IR R ← IM	**SUBB** R ← IR R ← IM	**SUB** R ← IR R ← IM	**ORB** R ← IR R ← IM	**OR** R ← IR R ← IM	**ANDB** R ← IR R ← IM	**AND** R ← IR R ← IM	**XORB** R ← IR R ← IM	**XOR** R ← IR R ← IM	**CPB** R ← IR R ← IM	**CP** R ← IR R ← IM	**See Table 1**	**See Table 1**	**EXTEND INST**	**EXTEND INST**
1	**CPL** R ← IR R ← IM	**PUSHL** IR ← IR	**SUBL** R ← IR R ← IM	**PUSH** IR ← IR	**LDL** R ← IR R ← IM	**POPL** IR ← IR	**ADDL** R ← IR R ← IM	**POP** IR ← IR	**MULTL** R ← IR R ← IM	**MULT** R ← IR R ← IM	**DIVL** R ← IR R ← IM	**DIV** R ← IR R ← IM	**See Table 2**	**LDL** IR ← R	**JP** PC ← IR	**CALL** PC ← IR
2	**LDB** R ← IR R ← IM	**LD** R ← IR R ← IM	**RESB** IR ← IM R ← R	**RES** IR ← IM R ← R	**SETB** IR ← IM R ← R	**SET** IR ← IM R ← R	**BITB** IR ← IM R ← R	**BIT** IR ← IM R ← R	**INCB** IR ← IM	**INC** IR ← IM	**DECB** IR ← IM	**DEC** IR ← IM	**EXB** R ← IR	**EX** R ← IR	**LDB** IR ← R	**LD** IR ← R
3	**LDB** R ← BA **LDRB** R ← RA	**LD** R ← BA **LDR** R ← RA	**LDB** BA ← R **LDRB** RA ← R	**LD** BA ← R **LDR** RA ← R	**LDA** R ← BA **LDAR** R ← RA	**LDL** R ← BA **LDRL** R ← RA	**RSVD**	**LDL** BA ← R **LDRL** RA ← R	RSVD	**LDPS** IR	**TABLE** BF	**TABLE** XBF	**INB** R ← IR	**IN** R ← IR	**OUTB** IR ← R	**OUT** IR ← R
4	**ADDB** R ← X R ← DA	**ADD** R ← X R ← DA	**SUBB** R ← X R ← DA	**SUB** R ← X R ← DA	**ORB** R ← X R ← DA	**OR** R ← X R ← DA	**ANDB** R ← X R ← DA	**AND** R ← X R ← DA	**XORB** R ← X R ← DA	**XOR** R ← X R ← DA	**CPB** R ← X R ← DA	**CP** R ← X R ← DA	**See Table 1**	**See Table 1**	**EXTEND INST**	**EXTEND INST**
5	**CPL** R ← X R ← DA	**PUSHL** IR ← X IR ← DA	**SUBL** R ← X R ← DA	**PUSH** IR ← X IR ← DA	**LDL** R ← X R ← DA	**POPL** IR ← X IR ← DA	**ADDL** R ← X R ← DA	**POP** IR ← X IR ← DA	**MULTL** R ← X R ← DA	**MULT** R ← X R ← DA	**DIVL** R ← X R ← DA	**DIV** R ← X	**See Table 2**	**LDL** X ← R DA ← R	**JP** PC ← X PC ← DA	**CALL** PC ← X PC ← DA
6	**LDB** R ← X R ← DA	**LD** R ← X R ← DA	**RESB** X ← IM DA ← IM	**RES** X ← IM DA ← IM	**SETB** X ← IM DA ← IM	**SET** X ← IM DA ← IM	**BITB** X ← IM DA ← IM	**BIT** X ← IM DA ← IM	**INCB** X ← IM DA ← IM	**INC** X ← IM DA ← IM	**DECB** X ← IM DA ← IM	**DEC** X ← IM DA ← IM	**EXB** R ← X R ← DA	**EX** R ← X R ← DA	**LDB** X ← R DA ← R	**LD** X ← R DA ← R
7	**LDB** R ← BX	**LD** R ← BX	**LDB** BX ← R	**LD** BX ← R	**LDA** R ← BX	**LDL** R ← BX	**LDA** R ← X R ← DA	**LDL** BX ← R	RSVD	**LDPS** PS ← X PS ← DA	**HALT**	**TABLE** BF	**EI** **DI**	**See Table 7**	RSVD	**SC**
8	**ADDB** R ← R	**ADD** R ← R	**SUBB** R ← R	**SUB** R ← R	**ORB** R ← R	**OR** R ← R	**ANDB** R ← R	**AND** R ← R	**XORB** R ← R	**XOR** R ← R	**CPB** R ← R	**CP** R ← R	**See Table 1**	**See Table 1**	**EXTEND INST.**	**EXTEND INST.**
9	**CPL** R ← R	**PUSHL** IR ← R	**SUBL** R ← R	**PUSH** IR ← R	**LDL** R ← R	**POPL** R ← IR	**ADDL** R ← R	**POP** R ← IR	**MULTL** R ← R	**MULT** R ← R	**DIVL** R ← R	**DIV** R ← R	**See Table 2**	RSVD	**RET** PC ← (SP)	RSVD
A	**LDB** R ← R	**LD** R ← R	**RESB** R ← IM	**RES** R ← IM	**SETB** R ← IM	**SET** R ← IM	**BITB** R ← IM	**BIT** R ← IM	**INCB** R ← IM	**INC** R ← IM	**DECB** R ← IM	**DEC** R ← IM	**EXB** R ← R	**EX** R ← R	**TCCB** R	**TCC** R
B	**DAB** R	**EXTS** **EXTSB** **EXTSL** R	**TABLE 4**	**TABLE 4**	**ADCB** R ← R	**ADC** R ← R	**SBCB** R ← R	**SBC** R ← R	**TABLE 5**	**RSVD**	**TABLE 6**	**TABLE 6**	**RRDB** R	**LDK** R ← IM	**RLDB** R	RSVD
C	**LDB** R ← IM	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→
D	**CALR** PC ← RA	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→
E	**JR** PC ← RA	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→
F	**DJNZ** **DBJNZ** PC ← RA	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→

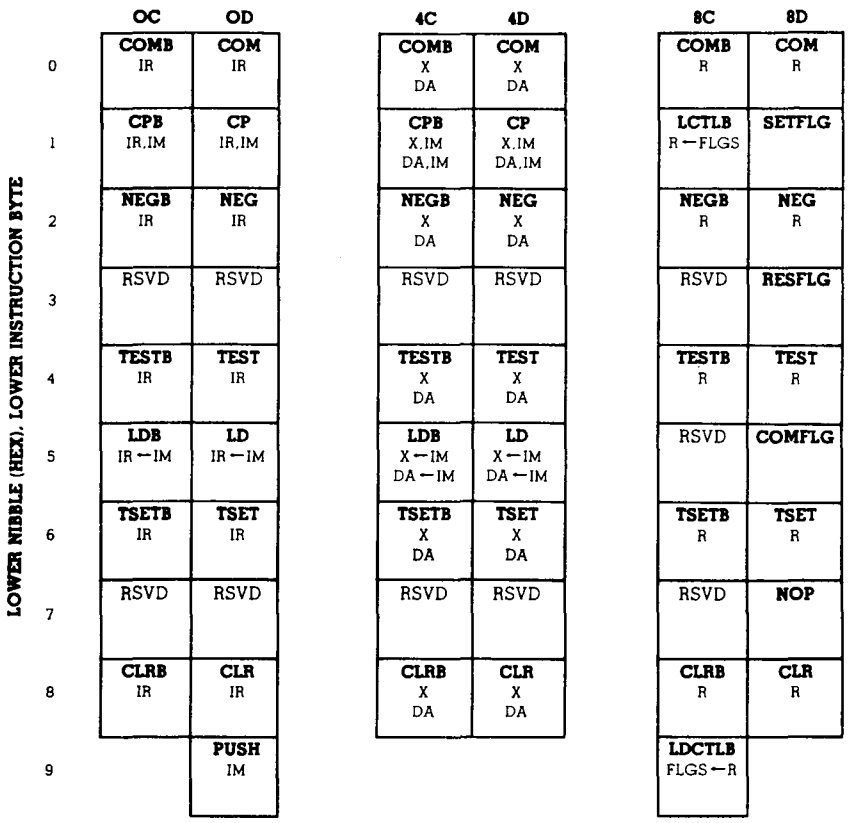
Op Code Map

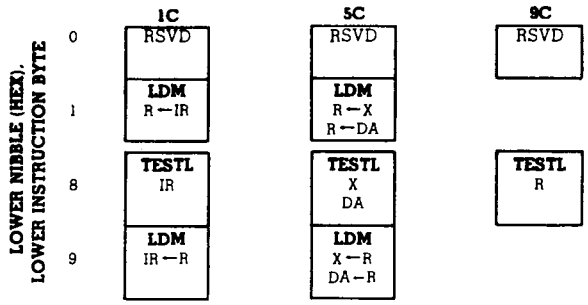
Notes:

1) Reserved Instructions (RSVD) should not be used. The result of their execution is not defined.

2.) The execution of an extended instruction will result in an Extended Instruction Trap if the EPA bit in the FCW is a zero. If the flag is a one the Extended Instruction will be executed by the EPU function.

Fig 2-6. Z8002 Instruction Set.



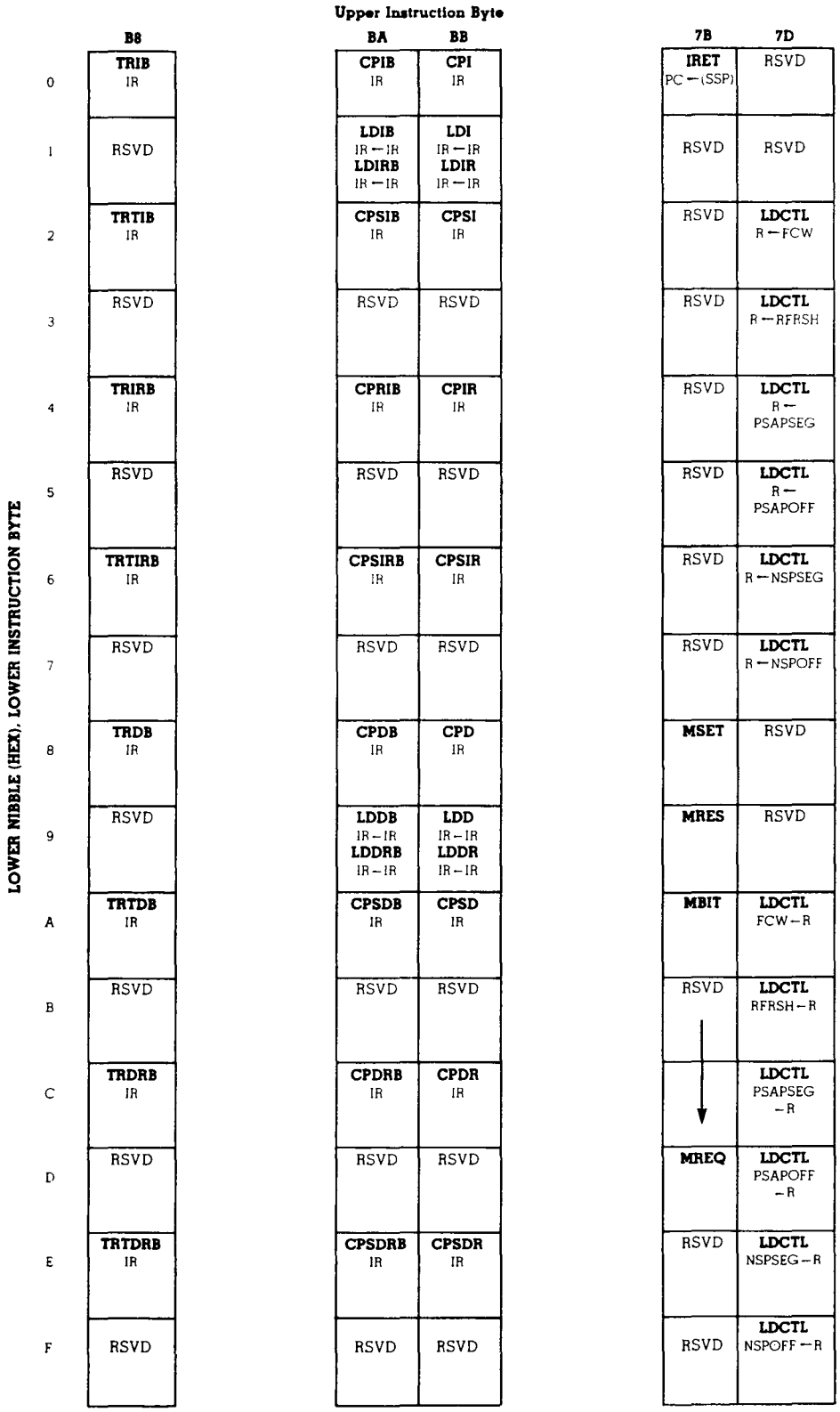


LOWER NIBBLE (HEX), LOWER INSTRUCTION BYTE	3A	3B
0	**INIB** IR←IR **INIRB** IR←IR	**INI** IR←IR **INIR** IR←IR
1	**SINIB** IR←IR **SINIRB** IR←IR	**SINI** IR←IR **SINIR** IR←IR
2	**OUTIB** IR←IR **OTIRB** IR←IR	**OUTI** IR←IR **OUTIR** IR←IR
3	**SOUTIB** IR←IR **SOTIRB** IR←IR	**SOUTI** IR←IR **SOTIR** IR←IR
4	**INB** R←DA	**IN** R←DA
5	**SINB** R←DA	**SIN** R←DA
6	**OUTB** DA←R	**OUT** DA←R
7	**SOUTB** DA←R	**SOUT** DA←R
8	**INDB** IR←IR **INDRB** IR←IR	**IND** IR←IR **INDR** IR←IR
9	**SINDB** IR←IR **SINDRB** IR←IR	**SIND** IR←IR **SINDR** IR←IR
A	**OUTDB** IR←IR **OTDRB** IR←IR	**OUTD** IR←IR **OTDR** IR←IR
B	**SOUTDB** IR←IR **SOTDRB** IR←IR	**SOUTD** IR←IR **SOTDR** IR←IR

Upper Instruction Byte

LOWER NIBBLE (HEX), LOWER INSTRUCTION BYTE	B2	B3
0	**RLB** (1 bit) R	**RL** (1 bit) R
1	**SLLB** R **SRLB** R	**SLL** R **SRL** R
2	**RLB** (2 bits) R	**RL** (2 bits) R
3	**SDLB** R	**SDL** R
4	**RRB** (1 bit) R	**RR** (1 bit) R
5	RSVD	**SLLL** R **SRLL**
6	**RRB** (2 bits) R	**RR** (2 bits) R
7	RSVD	**SDLL** R
8	**RLCB** (1 bit) R	**RLC** (1 bit) R
9	**SLAB** R **SRAB** R	**SLA** R **SRA** R
A	**RLCB** (2 bits) R	**RLC** (2 bits) R
B	**SDAB** R	**SDA** R
C	**RRCB** (1 bit) R	**RRC** (1 bit) R
D	RSVD	**SLAL** R **SRAL**
E	**RRCB** (2 bits) R	**RRC** (2 bits) R
F	RSVD	**SDAL** R

Upper Instruction Byte



Assembly listing differences between ZILOG, AMD, and PM 108:

Address Mode	ZILOG	AMD	PM 108
Immediate Data (IM)	#%FF2D	#FF2D	#FF2D
Indirect Register (IR)	@R11	R11↑	@R11
Direct Address (DA)	%1234	#1234↑	1234
Indexed Address (X)	%1234(R7)	1234(R7)	1234(R7)
Relative Address (RA)	$+12	label(12)	absolute address
Based Address (BA)	R7(#%1234)	R7↑(1234)	R7(#1234)
Based Indexed Address (BX)	R7(R4)	R7↑(R1)	R7(R4)

Zilog uses the percent sign only to indicate that the following number is in hex. The PM 108 displays data and addresses always in HEX in mnemonic mode so Base indicator is not used in the display.

The PM 108 displays decimal for register numbers, shift instructions, and bit numbers.

SPECIFICATIONS

This section of the manual lists the electrical, mechanical, and environmental characteristics of the PM 108 Personality Module. Since the PM 108 operates only as part of a logic analyzer system, all operating voltages and currents are furnished by the logic analyzer to which the PM 108 is connected.

If verification of these listed electrical characteristics is required for customer incoming inspection or other purposes, Section 5, Performance Verification, lists the necessary test equipment and procedures.

Items listed in the Supplemental Information column are either explanatory notes or performance characteristics for which no limits are specified. They may not be verified.

INTERFACE TO 7D02

PIN	SIGNAL		DESCRIPTION
1	GND		CONNECT TO GROUND PLANE
2	CLOCK	>	ECL LEVEL CLOCK DIFFERENTIALLY TERMINATED INTO 124 OHM
3	/CLOCK	>	ECL LEVEL CLOCK DIFFERENTIALLY TERMINATED INTO 124 OHM
4	GND		POWER SUPPLY COMMON GROUND
5	A0	<>	TTL, ADDRESS 0, TERMINATED INTO 68 OHMS
6	A1	<>	TTL, ADDRESS 1, TERMINATED INTO 68 OHMS
7	A2	<>	TTL, ADDRESS 2, TERMINATED INTO 68 OHMS
8	A3	<>	TTL, ADDRESS 3, TERMINATED INTO 68 OHMS
9	A4	<>	TTL, ADDRESS 4, TERMINATED INTO 68 OHMS
10	A5	<>	TTL, ADDRESS 5, TERMINATED INTO 68 OHMS
11	A6	<>	TTL, ADDRESS 6, TERMINATED INTO 68 OHMS
12	A7	<>	TTL, ADDRESS 7, TERMINATED INTO 68 OHMS
13	A8	<>	TTL, ADDRESS 8, TERMINATED INTO 68 OHMS
14	A9	<>	TTL, ADDRESS 9, TERMINATED INTO 68 OHMS
15	A10	<>	TTL, ADDRESS 10, TERMINATED INTO 68 OHMS
16	A11	<>	TTL, ADDRESS 11, TERMINATED INTO 68 OHMS
17	A12	>	TTL, ADDRESS 12, TERMINATED INTO 68 OHMS
18	A13	>	TTL, ADDRESS 13, TERMINATED INTO 68 OHMS
19	A14	>	TTL, ADDRESS 14, TERMINATED INTO 68 OHMS
20	A15	>	TTL, ADDRESS 15, TERMINATED INTO 68 OHMS
21	ST0		TTL, STATUS 0, TERMINATED INTO 68 OHMS
22	ST1		TTL, STATUS 1, TERMINATED INTO 68 OHMS
23	ST2		TTL, STATUS 2, TERMINATED INTO 68 OHMS
24	ST3		TTL, STATUS 3, TERMINATED INTO 68 OHMS
25	N/S		TTL, NORMAL/SYSTEM, TERMINATED INTO 68 OHMS
26	GND		NOT USED — GROUNDED
27	GND		NOT USED — GROUNDED
28	GND		NOT USED — GROUNDED
29	D0	>	TTL, DATA 0, BACK TERMINATED INTO 68 OHMS
30	D1	>	TTL, DATA 1, BACK TERMINATED INTO 68 OHMS
31	D2	>	TTL, DATA 2, BACK TERMINATED INTO 68 OHMS
32	D3	>	TTL, DATA 3, BACK TERMINATED INTO 68 OHMS
33	D4	>	TTL, DATA 4, BACK TERMINATED INTO 68 OHMS

INTERFACE TO 7D02 (cont.)

PIN	SIGNAL		DESCRIPTION
34	D5	>	TTL, DATA 5, BACK TERMINATED INTO 68 OHMS
35	D6	>	TTL, DATA 6, BACK TERMINATED INTO 68 OHMS
36	D7	>	TTL, DATA 7, BACK TERMINATED INTO 68 OHMS
37	D8	>	TTL, DATA 8, BACK TERMINATED INTO 68 OHMS
38	D9	>	TTL, DATA 9, BACK TERMINATED INTO 68 OHMS
39	D10	>	TTL, DATA 10, BACK TERMINATED INTO 68 OHMS
40	D11	>	TTL, DATA 11, BACK TERMINATED INTO 68 OHMS
41	D12	>	TTL, DATA 12, BACK TERMINATED INTO 68 OHMS
42	D13	>	TTL, DATA 13, BACK TERMINATED INTO 68 OHMS
43	D14	>	TTL, DATA 14, BACK TERMINATED INTO 68 OHMS
44	D15	>	TTL, DATA 15, BACK TERMINATED INTO 68 OHMS
45	+5 V		
46	C0	>	READ-/WRITE, TTL, BACK TERMINATED INTO 68 OHMS
47	C1	>	IO-/MEM, TTL, BACK TERMINATED INTO 68 OHMS
48	C2	>	INTERRUPT REQUEST, TTL, BACK TERMINATED INTO 68 OHMS
49	C3	>	INSTRUCTION FETCH, TTL, BACK TERMINATED INTO 68 OHMS
50	C4	>	/BUSAK, TTL, BACK TERMINATED INTO 68 OHMS
51	C5	>	/MREQ, TTL, BACK TERMINATED INTO 68 OHMS
52	C6	>	/RESET, TTL, BACK TERMINATED INTO 68 OHMS
53	C7	>	/HALT, TTL, BACK TERMINATED INTO 68 OHMS
54	C8	>	/AS, TTL, BACK TERMINATED INTO 68 OHMS
55	C9	>	/TWAIT, TTL, BACK TERMINATED INTO 68 OHMS
56	+5 V		+5 VOLTS SUPPLY
57	+5 V		+5 VOLTS SUPPLY
58	+15 V		+15 VOLTS SUPPLY
59	−15 V		−15 VOLTS SUPPLY
60	GND		TTL GND
61	STOP P.U.T.	<	STTL, INPUT: HALTS P.U.T.
62	INPUT LOOK	<	STTL, INPUT: DISABLES P.U.T. INPUT BUFFER
63	/SEL P	<	STTL, INPUT: SELECTS PROM
64	GND		GROUND PLANE

SYSTEM DESCRIPTION

CONTROL LINES

(Names the definitions grouped by function. For example, word recognizer events, clock qualifiers, and halt lines have been used in previous probe specifications.)

These four control lines are stored and used as primary events for the word recognizer:

C0 — READ-/WRITE — Memory read or write
C1 — IO-/MEM — Memory or IO transaction
C2 — INT REQ — Interrupt Request
C3 — IFC — Instruction Fetch

These two control lines are primary events for the word recognizer and are used as clock qualifiers, but are not stored:

C4 — /BUSAK — Signifies that a DMD device has requested the bus and has been granted it.

C5 — /MREQ — Memory Request line

The next four are clock qualifiers only. C7 is the /STOP input to the CPU and also the response to the STOP PUT from the 7D02. C8 and C9 are clock qualifiers generated by the probe to qualify clocks at the time there are valid bus transactions on the P.U.T.

C6 — /BRESET — Reset the CPU from the system under test.

C7 — /B HALT — The SUT as the 7D02 stops the processor.

C8 — /BAS — Buffered Address Strobe.

C9 — /TWAIT — "T" state wait signal generated by internal oper, memory refresh or /WAIT.

ELECTRICAL SPECIFICATIONS

Replacement Plug Pin Designation

CONNECTOR	ZIF PIN NO.	INPUT PROTECT	SIGNAL NAME
J6020-1	40	YES	AD0
J6020-17	32	YES	AD1
J6020-15	33	YES	AD2
J6020-13	34	YES	AD3
J6020-9	36	YES	AD4
J6020-11	35	YES	AD5
J6020-7	37	YES	AD6
J6020-5	38	YES	AD7
J6020-3	39	YES	AD8
J7020-1	1	YES	AD9
J7020-3	2	YES	AD10
J7020-5	3	YES	AD11
J7020-7	4	YES	AD12
J7020-9	5	YES	AD13
J7020-17	9	YES	AD14
J7020-15	8	YES	AD15
J6020-23	29	YES	/AS
J7020-23	12	YES	/NVI
J7020-21	11	YES	/VI
J7020-25	13	YES	/NMI
J6020-39	21	YES	ST0
J7020-39	20	YES	ST1
J7020-37	19	YES	ST2
J7020-35	18	YES	ST3
J7020-31	16	YES	/MREQ
J7020-33	17	YES	/DS
J7020-27	14	YES	/RESET
J7020-11	6	YES	/STOP changes to /HALT in MODULE
J6020-31	25	YES	R-/W
J6020-33	24	YES	/BUSAK
J6020-35	23	YES	/WAIT
J6020-27	27	NO	B-/W
J6020-29	26	YES	N-/S
J6020-25	28	NO	DCPL
J6020-37	22	NO	/BUSREQ
J7020-13	7	NO	/MI
J7020-29	15	NO	/MO
J7020-19	10	NO	Vcc
J6020-21	30	YES	CLOCK
J6020-19	31	NO	GND
J7020 2, 4, 6..	40		All even-numbered lines are ground
J6020 2, 4, 6..	40		All even-numbered lines are ground

Table 3-1

SIGNAL INPUTS

CHARACTERISTICS	DESCRIPTION
Maximum number of channels w/option 03	47

DATA	16	
ADDRESS	16	
STATUS	4	Status of μp Z8002 - Pins 18, 19, 20, 21
N/S	1	Normal/System Bit - Pin 26
CONTROL	10	

Control Line	Stored	Word Recognizer Input	Clock Qualifier	Description
C0	X	X		Read/Write
C1	X	X		IO/MEM
C2	X	X		INTREQ
C3	X	X		IFC
C4		X	X	/BUSAK
C5		X	X	/MREQ
C6			X	/RESET
C7			X	PHALTED
C8			X	/AS
C9			X	/TWAIT

Table 3-2

ELECTRICAL SPECIFICATIONS

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Z8002 Personality Module		
Data Input Channels		
TTL Input Levels		0-7 V Signal swings 1/2 LSTTL LOAD with 37 pF nominal.
Voltage in, low limits (operating)	Min. 0.0 V, max. 0.5 V	
Voltage in, high limits (operating)	Min. 2.4 V, max. 7.0 V	
Current in low limits (V. in low = 0.4 V)		−0.2 mA max.
Current in high limits (V. in high = +2.7 V)		+0.02 mA max.
Hysterisis		0.2 V min.
Maximum voltage in, non-operating, non-destructive		−7 V to +15 V continuous limited to any five inputs pulled high simultaneously.
Threshold Voltage V_t		Fixed 1.4 V, nominal. TTL compatible.

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Table 3-2 (cont)

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
/STOP P.U.T.		
/STOP Output Drive		
V_{oh}		2.4 V, I_{oh} = 1 mA
V_{ol}		.5 V, I_{ol} = −1 mA
Clock Input		
Input Impedance		50 KΩ at 37 pF — nominal
Clock Period	250 ns min.	
Clock Pulse Width (min)	105 ns HI, 105 ns, LOW	
Data Acquisition Rate	625 ns (min)	
Voltage in Low Limits (operating)	Min. 0.0 V, max. 0.6 V	
Voltage in High Limits (operating)	Min. 2.0 V, max. 7.0 V	
Hystersis		0.4 V nominal
Threshold Votlage		Fixed 1.4 V, nominal
Maximum Voltage in, non-operating non-destructive		−15 V to +15 V
Propagation Delays through Personality Module		
Delay through ECL Clock		10.5 ns min., 14.5 ns max.
Delay added to STOP Line (from microprocessor plug to μP)	35 ns max.	
Data Channel Delay		
Channels D0-D15		20 ns min., 35 ns max.
Control Channel Delays C0, C1, C3, C4, C5, C6 and C8		20 ns min., 35 ns max.
Test Clock		
Clock Period		230 ns min., ±20 ns
Clock Pulse Width (high or low)		105 ns
System Specifications		System is 7D02 with Z8002 (PM 108)
Data	Set up time = 40 ns Hold time = Ø ns	Referenced to falling edge of T_3
Control Channels C0, C1, C3, C4, C5, C6 and C8		Set up time = 40 ns Referenced to the rising edge of /AS. Hold time = Ø ns After the falling edge of T_3

Table 3-2 (cont)

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
C2 (IRQ)	160 ns min setup Latched at falling edge of T_2. Held until cleared by Interrupt Acknowledge cycle.	
Address A0-A15		Set up time = 34 ns Hold time = 0
/AS (Address Strobe)		24 ns typical
Delay		35 ns max
Mechanical Specifications		
Size		4.7 in. X 8 in. X 1.7 in. (12 X 20.3 X 4.3 cm)
Weight		Approximately 2 lbs with cables (1 kg. with cables).
Cable Length (7D02 to Pod)		122 cm, ±2.5 cm (4 ft. ±1 inch)
Cable Length (Replacement Plug to Personality Module Conductor in Module Pod)		13 in. ±1/2 in.
Environmental Specifications		
Operating		−15° C to +55° C
Non-operating		−62° C to +85° C
Relative Humidity		95 to 97% 5-24 hour cycles @30° C to 60° C
Altitude		
Operating		4.5 km (15,000 ft)
Non-operating		15 km (50,000 ft.)
Vibration		.64 mm peak-to-peak, 10-55 Hz sinewave 75 min. total.

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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

THEORY OF OPERATION

OVERVIEW

The primary function of a Personality Module is to collect data from a system under test (S.U.T.) and transfer it to the logic analyzer in a format that the logic analyzer can interpret.

The PM 108 Personality Module achieves this result by performing the following separate functions:

1. The PM 108 allows the logic analyzer to monitor almost all communication between the processor-under-test in the ZIF socket (P.U.T.) and the system under test (S.U.T.) as the system operates.

2. The personality module generates additional control signals needed by the logic analyzer, that are not provided by the processor under test.

3. Before data acquisition the personality module PROM

   - sets up the acquisition hardware.
   - personalizes the logic analyzer program display into a format for Z8002-based systems.

   After data acquisition the PROM allows the logic analyzer to

   - display the acquired data in a usable format.
   - disassemble the acquired data into Z8002 mnemonics, if desired.

4. The personality module lets the user halt his S.U.T. after the logic analyzer acquires the requested data.

5. In self test mode, the personality module outputs a predictable set of test signals, designed to simulate a subset of Z8002 instructions and special modes. The signals may be used to test the personality module and the logic analyzer.

Refer to Fig. 4-1, the Block Diagram, and the schematics in Section 8. Components are outlined on the schematic in grey.

CIRCUIT DESCRIPTION

T States

The Z8002 microprocessor can be driven by an external clock signal. Each clock cycle at pin 30 is described as a "T State". The personality module operates in synchronism with T States in all its functions, and throughout this description reference is made to each major occurrence as it relates to some part of a T State.

Address and Data Line Operations

Sixteen addresses and data (multiplexed) lines are taken from the Z8002 in the ZIF socket and applied to buffers and address latches in the personality module. Address latches are A1U2060 and A1U3060. Addresses 0 through 16 are latched by the rising edge of /AS (address strobe).

During the falling edge of T3, /INPUT LOOK is low and Data (D0-D15) is read from buffers A1U2050 and A1U3050. At the same time the output enable pins of the address latches are low, allowing the address lines (AD0-AD15) to be read by the 7D02.

/AS

The /AS (Address Strobe) signal is buffered by A1U3030 and sent directly to the 7D02 where it appears on control line C8 as ESYNC. ESYNC synchronizes the front end board of the 7D02. /BAS is also used to latch the address into A1U3060 and A1U2060. It is also used by the lower board to initialize the WAIT State Generator. Any pending Interrupt Acknowledge I/O status will be latched into their respective latches (A2U3020A and A2U3020B). These status signals are used to generate WAIT states to the 7D02 in order to latch data into the 7D02 at proper times. /BAS also starts T2 generator A2U4018 which determines the proper time to generate WAIT states.

Interrupts

There are three types of interrupts used by the Z8002 microprocessor. Non-vectored (NVI), Vectored (VI) and Non-Maskable (NMI). These interrupts are buffered by A1U3030, ORed in U4010 B and C, and sent to the lower board as /INT. /INT is latched in A2U1020A where, during the falling edge of T2, it is sent to the 7D02 on control line C2, Interrupt Request (IRQ). It is then displayed at the proper time on the right side of the screen. Interrupt

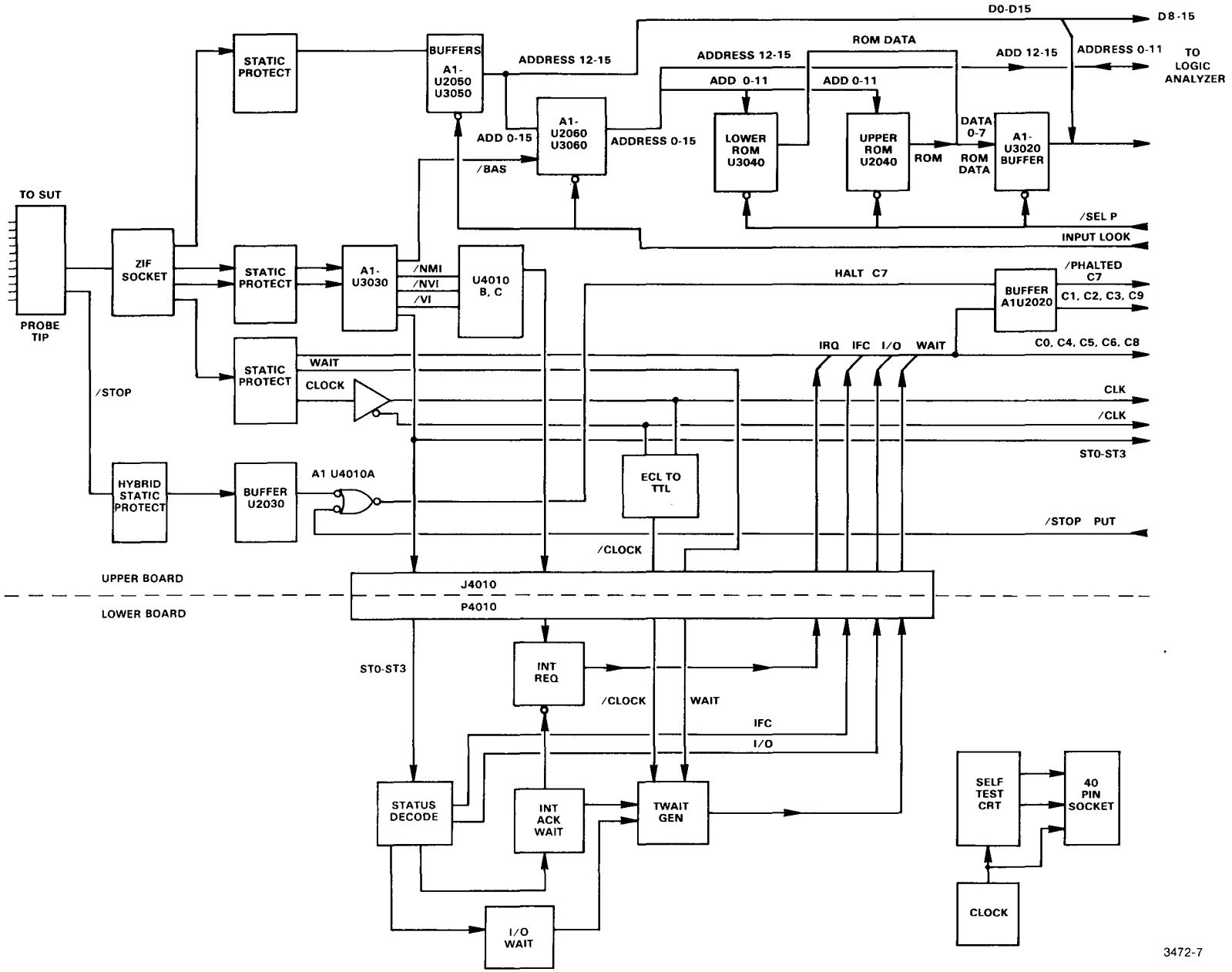

Fig. 4-1. PM 108 Block Diagram.

Acknowledge status generated by the Z8002 ANDed with /BDS (Data Strobe) clears A2U1020, removing IRQ on line C2. The status encoded by the Z8002, in this case one of the interrupt acknowledge statuses, removes the Wait states from C9 and also be displayed on the 7D02 screen. This should happen at the same time that IRQ (C2) goes low.

The ECL Comparator

Pin 30 of the ZIF Socket monitors the clock output of the Z8002. This signal is sent to A1U3070, a very fast ECL comparator, which outputs CLK and /CLK signals to the 7D02. The fast comparator is needed to get the clock signal to the logic analyzer as quickly as possible. (The ECL comparator also provides a constant 50 KΩ input impedance to the Z8002 clock output, preventing excessive loading from the personality module circuits.) A1Q3070, A1Q3072 and A1Q2070 with their associated circuits form an ECL to TTL converter, which generate the TTL clock to the WAIT state generator on the lower board.

Memory

Two sockets are provided for personality module firmware storage. One socket is 28 pins and performs two functions. It allows two types of ROMs to be installed, a single 8K EROM or mask ROM, or a single 4K EROM or 4K mask ROM containing the lower half of the firmware program. The other socket is for a 4K EROM or 4K mask ROM which contains the upper half of the firmware. The single 8K EROM or 8K mask ROM contains the entire firmware. A1P3020 selects 1 each 8K ROM or 2 each 4K ROMs.

PM 108 Self Test Information

The Self Test Circuitry in the PM 108 comprises an 8.4 MHz oscillator, a binary counter, additional logic gates that provide clock, /AS, /DS, status lines ST0-ST3, R-/W, /RESET, /BUSAK, and /NMI.

The counter is a 16-bit binary counter which counts 0 to 65535, then repeats. /AS is generated every T1 cycle and only three T States are generated. /DS is generated during T3. The upper 8 bits of the address are the complemented version of the data bits. For example, Data = 0057H and address = FF57H; or Data = 5A01H and address = A501H.

R/W changes states with every 16 counts (AD4).

NMI is generated when AD 15 goes high or at Data = 8000.

The Self Test circuit has been designed into the personality module for the purpose of testing the operation of the module itself. This allows any apparent difficulties in the system to be localized to the PM 108 or the Z8002 processor under test. It generates a simulated program which exercises most of the functioning circuits of the personality module. Self Test also provides the stimulus for Signature Analysis.

DETAILED CIRCUIT DESCRIPTION

Upper Board

The upper circuit board (A1) in the PM 108 contains the buffers for the various processor lines from the ZIF Socket, as well as circuitry that accepts and processes address and data information from the system under test so that the disassembled information can be displayed on the logic analyzer. The ECL Comparator, which processes the incoming clock signal from the processor, is also located on the upper board.

Timing and Synchronizing Signals

Clock is the signal from the processor pin 30 of the ZIF Socket. Clock is input to pin 2 of ECL Comparator A1U3070, and emerges as two signal outputs; CLK at J1010 pin 2, and /CLK at J1010 pin 3. A1U3070 is a fast ECL Comparator, ensuring that Clock signals are transferred to the logic analyzer in the shortest possible time. The CLK output from pin 7 and /CLK on pin 8 are also applied to the ECL-to-TTL converter circuit, A1Q3070, A1Q3072 and A1Q2070, where the clock TTL signal is generated for use on the lower board.

The other major timing signal from the Z8002 processor is /AS (Address Strobe). /AS is on pin 29 of the ZIF socket and is buffered in A1U3030 (shown on the schematic as /BAS or buffered /AS) and presents it to the logic analyzer as ESYNC on Control Line C8. /AS acts to synchronize the front-end board of the 7D02. The /BAS signal from the output of A1U3030 is used to latch AØ through A15 at Latch A1U3060 and A1U2060. It is also sent to the lower board for use in synchronizing the state machines via pin 4 of J4010.

Address and Data Lines

The Z8002 bus lines, AD0 through AD15, are multiplexed; each of these lines contain address and data at different times in the machine cycle.

During T1 of the machine cycle, address information enters the personality module from the ZIF socket to buffers A1U2050 and A1U3050. Each line to the buffers contains a static protection hybrid H1023 which contains a spark gap with a breakdown voltage of about 400 V, a clamp diode to +15 V protected by a 720 Ω current limiting resistor. From the output of the buffers the

address information is latched by A1U2060 and A1U3060. Latching takes place during T1 on the rising edge of /AS. During succeeding T states of the processor's machine cycle, the address is removed and changed to data by the processor (WRITE) or external device such as memory (READ). The address information is then "read" by the logic analyzer from A1U2060 and A1U3060 and the data is "read" from the buffers A1U2050 and A1U3050 during T3 state.

After the 7D02 Acquisition Memory has been filled, the 7D02 pulls the INPUT LOOK (J1010, pin 62) high. This causes A1U2050, A1U3050, A1U2060 and A1U3060 to go to a high impedance state. The 7D02 can then use the address and data lines on J1010 to access the personality module ROM to decode information stored in the acquisition memory. /SEL P (J1010 pin 63) turns on the PROMs and buffer A1U3020 to read the data from the PROMs.

Lower Board

The Circuits on the lower board include four state machines—the WAIT generator, Interrupt Latch, Interrupt Acknowledge WAIT generator, and I/O WAIT generator. Also included in a status decode circuit and a self-test circuit.

Interrupt Latch

The interrupt latch circuit (A2U4028 A/B, A2U1020 A/B, A2U3030D) latches any interrupt (VI, NVI or NMI) and holds it until cleared by the next interrupt acknowledge cycle. The status displayed on the 7D02 screen indicates the type of interrupt (VI, NVI or NMI).

Status Decode Circuit

BST0 through BST3 are buffered signals ST0 through ST3 coming from the Z8002 processor in the ZIF socket. These signals are buffered by A1U3030 and sent to the logic analyzer and the lower board. The components A2U4038, A2U2020A, A2U2010A, and A2U3040 comprise the decode circuits. Only four of the logic analyzer status codes are decoded. They are I/O, Interrupt Ack, Instruction Fetch, and Refresh.

- I/O is buffered by A2U4038 and A1U2020 and placed on A1J1010 as C1, IO/MEM. I/O is also used on the lower board to generate one WAIT state after T2 to keep the 7D02 synchronized during Z8002 I/O cycles.

- Interrupt Acknowledge is used to clear the Interrupt Request latch as well as generate WAIT states to the logic analyzer until cleared by /BDS. The Z8002 generates five automatic WAIT states during an acknowledge cycle by asserting WAIT law for 5 clock cycles until T3. The 7D02 then strobes in the data for vector information.

- Instruction Fetch is decoded and used by the logic analyzer as control line C3. Notice that FETCH 1 and FETCH N both generate IFC at line C3.

- Refresh—During Z8002 memory refresh cycles the Z8002 ignores WAIT signals from the memory. The WAIT input monitored by the personality module causes the WAIT state generator to inhibit clocks in the logic analyzer. To prevent this, the Refresh status is decoded and sent to A2U2020 Pin 9 to prevent /TWAIT being generated.

WAIT State Generator

The WAIT state generator comprises A2U4018 A and B, A2U3030 A and B, A2U3007A and A2U2020C. A2U4018 A and B are set by /BAS and at the next rising edge of the clock T2 is generated at pin 8 of A2U4018B. When a /WAIT signal is present on pin 5 of A2U2020, a pulse of one clock cycle is allowed to pass through to A2P4010 pin 10, which becomes control line C9. This pulse inhibits clock cycles at the 7D02 for one clock period. The circuit will continue generating WAIT (C9) as long as pin 1 of A2U3030 is held low. There are three signals that can hold this line low; the /WAIT from the Z8002 ZIF socket on the top board, Interrupt Acknowledge from the INT ACK WAIT generator A2U3020A, or I/O WAIT from the I/O WAIT generator A2U3020B.

A2U2020C inhibits WAIT states when pin 9 or pin 10 is low. Pin 9 is the refresh signal noted previously and during self test. When the module is plugged into the self-test socket, pin 31 is grounded, this prevents signals passing thru A2U2020 during self test.

Self-Test

The self-test circuit in the PM 108 comprises A2Q3010, A2U3007B, A2U2010 B, C, D, A2U1010, A2U1030, A2U2030, A2U1040, A2U2040, A2U3085 and A2U4028E.

A2Q3010 and associated circuits functions as an 8.4 MHz oscillator to provide a self test 4.2 MHz clock. A2U3007B provides Clock and /Clock. Clock is sent to pin 30 of the 40-pin test socket (J2065). /Clock is used to generate /AS and /DS via A2U1010. /AS drives 8-bit counter A2U1030 producing AD0-AD7. AD7 of A2U1030 drives A2U1040 producing AD8-AD15. AD8-AD15 are inverted during the time /DS is high and non-inverted during /DS low. This produces a different display for address and data on the logic analyzer screen. For example: ADDR = FF02, DATA = 0002.

@

Status lines ST0-ST3 are inverted by A2U3085 to produce an inverse status display. This allows the mnemonic decode to receive a Fetch N after a Fetch 1 for more realistic decoded display.

Data line D15 is inverted and used to generate an interrupt NMI for testing the interrupt circuits. This produces an interrupt when the data changes from 7FFF to 8000.

AD0-AD7 are presented at J3075 for use in testing the timing option.

AD15 is also present on J3075, pin 2 and 3 for signature analysis start and stop pulses.

PERFORMANCE VERIFICATION

INTRODUCTION

The procedures that follow provide a method of checking the operation and performance requirements of the PM 108. The procedure can be used for incoming inspection, familiarization, or system troubleshooting.

There are two parts to the Performance Verification. Part 1 describes a procedure that allows you to verify that the personality module circuitry and the connections to the logic analyzer are functional and operating as expected. The personality module self test circuit produces the necessary signals on all address, data, control, and clock lines to provide a preliminary check of the PM 108 circuits.

Part 2 describes a procedure to test the more specific performance requirements such as input impedance, actual threshold voltages, propagation delays within the module, etc. This procedure requires some physical disassembly of the personality module.

TEST EQUIPMENT REQUIRED

1. An oscilloscope with vertical frequency response DC to 100 MHz, minimum vertical deflection factor 50 mV to 5 V/Div, and dual trace. An example is the Tektronix 465.
2. A pulse generator with variable pulse width and amplitude. The Tektronix PG 508, for example.
3. A digital multimeter. Example: the Tektronix DM 501A.
4. A 40-pin dual in-line package socket, wire wrap pins. Example: Tektronix Part No. 136-0622-00.
5. A small flat blade screwdriver.
6. A Phillips screwdriver.
7. A 3/32" Allen wrench.

PERFORMANCE VERIFICATION PART I

Preliminary setup

With the 7D02 Logic Analyzer properly installed in a 7000-series mainframe and the power switch in the OFF position, plug in the PM 108.

Plug the microprocessor plug into the self-test socket. See Section 6, How to Use the Self-Test Circuitry.

After checking that all connectors are secure, turn on the mainframe power switch and observe the display. The screen should show the "Powerup Diagnostics Completed" message. If it does not, see Section 6, Diagnostics and Troubleshooting.

Set the Channel 1 vertical input of the test oscilloscope to 1V/div. and the horizontal sweep rate to 0.19/div. Select Channel 1 for vertical mode. Then carry out the following steps.

1. Attach the oscilloscope probe ground lead to pin 31 of the ZIF socket on the personality module. Place the probe tip at pin 30 of the ZIF socket to see a TTL pulse train with a period of 250 nS and minimum low time greater than 105 nS. This check verifies that the test clock on the lower board is running.
2. Turn off the mainframe power switch.

3. While holding down any one of the 7D02 input keys, turn the mainframe power switch back on, and wait for the display to appear. The display should indicate that the Keyboard test failed due to a key being held down. This allows access to the more detailed diagnostics in the 7D02 firmware.

4. Press the X (Don't Care) key on the 7D02 keypad to enter the Diagnostic Monitor. A diagnostic menu will appear on the display.

5. Press 9 on the keypad to enter the Personality Module diagnostics. Notice that the display asks for "Self Test Stimulus", even though it is connected already.

6. Press the 7D02 START/STOP key to begin Self Test diagnostics. These tests check most of the PM 108, as well as the connections to the 7D02 for all address, data, and clock lines, and most of the control lines. If everything is functioning properly, the display will indicate that all tests "PASS."

Timing Option Checks

The personality module self test circuit generates signals to check the timing option of the 7D02. If a timing option is installed, test these signals by following this procedure.

1. Connect a P6451 Data Acquisition Probe to the 7D02 Timing P6451 socket.

2. Attach the P6451 input leads to J3075 (to the right of the test socket) as follows: GND to pin 1 (marked by an arrow in the board). Channels 0 to 7 to J3075 pins 4 to 11, respectively. (Pins 2 and 3 are used for signature analysis only.)

3. Press X to return to the Diagnostic menu.

4. Press B on the keypad to enter Timing Option diagnostics.

5. Press START/STOP to begin the tests.

6. The display should show "PASS" for all three tests.

7. The remaining checks will be accomplished by putting the 7D02 in its normal operating mode and setting up various conditions via the keypad.

Test Circuit Data

Press the START/STOP key twice to trigger the 7D02 and acquire the test circuit data. The information displayed is produced by the self-test circuit. It does not represent a functioning program, but stimulates various Fetch, Read, and Write machine cycles, by providing the necessary signals on the bus and control lines. This simulated program starts at address 0000 and repeats every 65,535 machine cycles. During each program cycle, all of the address, data, and control lines are pulled high and then low at least once to test for stuck lines. If any line contains wrong information, a failure will have occurred in the previously-described diagnostic tests.

Obtain a display of the program by pressing

IMMEDIATE
DISPLAY
PROGRAM

on the 7D02 keypad. Move the cursor to "0-SYSTEM UNDER TEST CONT." enter a "1". The display will change to "1-SYSTEM UNDER TEST HALT".

Press the START/STOP key several times while watching for the "Z8002 HALTED" message, which will appear briefly in the upper right corner of the display screen before the display is shown. Since the Word Recognizer is set to trigger on all "Don't Cares", the display will show new information each time the START/STOP key is pressed.

Press

IMMEDIATE
DISPLAY
PROGRAM

and change 1-SYSTEM UNDER TEST HALT back to 0-SYSTEM UNDER TEST CONT. Move the cursor the DATA = XXXX and change it to DATA = 8002. Press START/STOP. Use the scrolling keys to find the display of address 7F00 and data 8000. Notice when the data changed from 7FFF to 8000, the IRQ changed from 0 to 1. The IRQ will change back when "VI ACK" is received for status.

This concludes Part I of the Performance Verification. Turn the 7D02 power switch off and remove the P6451 plug and microprocessor plug from the personality module test socket. Move jumper J1065 back to the NORM position. Replace the access door.

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PERFORMANCE VERIFICATION PART II

Introduction

The tests described in this part of the performance verification test PM 108 specifications that are not checked by the self test function. Equipment used in this part of the procedure is the same as that listed at the beginning of the section. These tests will be easier to complete if a 40-pin DIP socket is plugged on the PM 108 microprocessor plug. The pulse generator can then be connected via short leads from a female BNC connector to the designated pins on the DIP socket.

1. Check personality module input impedance for microprocessor clock signal 50 KΩ or less, within ± 5%, by following this procedure: turn off 7D02 power, connect the digital multimeter between microprocessor plug pins 31 (GND) and 30. Check for an impedance of 50 KΩ, ± 2.5 K.

2. Check maximum voltage inputs for low limit, minimum input for voltage high limit, data setup time and hold time for address and data lines.

   a. Set the oscilloscope as follows:

Vertical Mode	Channel 1
Vertical Deflection Factor	1 V/Div
Time/Div or Delay Time	0.5 μ/div.
Ground	Channel 1 input

   Center the trace with the vertical position control and set for DC input. Connect the channel 1 oscilloscope probe to the BNC plug from the pulse generator.

   b. Power up the oscilloscope and the pulse generator and set the pulse generator controls as follows:

Period	1 microsecond
Duration	50 ns
Back Terminated	
high level	2.0 V
low level	0.6 V
rise/fall time	5 ns

   c. Adjust the pulse generator to form a pulse 2 cm high, with a width of 1 cm, (500 ns) on the test oscilloscope CRT.

   d. Turn on the 7D02 power switch.

NOTE

Most of the performance tests in this section involving the pulse generator require that connection be made to pin 30 (the clock signal), in parallel with some other pin on which the test signal is read.

   e. To check the setup and hold times on the data lines, leave the pulse generator connections across pins 30 (clock) and 31 (ground) of ZIF socket. Press the Format key on the 7D02. Change the data field display from hex to binary, as follows:

```
    0-BINARY
WORD RECOGNIZER ADDRESS FIELD
  2-HEX
WORD RECOGNIZER DATA FIELD
  2-HEX
TIMING OPTION DATA DISPLAY
  0-BINARY
ADDRESS FIELD DISPLAY
  2-HEX
DATA FIELD DISPLAY
  0-BINARY
    0 BINARY
    1 OCTAL
    2 HEX
    3 ASCII
HIGHLIGHT MEMORY DIFFERENCES?
  1-NO
DISPLAY GLITCHES?
  0-YES
TIMING OPTION DATA INVERSION
  DATA=00000000
```

   Press Format again to exit format mode. Program the 7D02 as follows:

```
ELSE
TRIGGER
  User Clock Qual.
  Rising Edge of Clock
  User Clock Synthesis
  Delay by 0
```

Your program should look like this:

```
TEST 1
   1ELSE DO
   1      TRIGGER 0-MAIN
   1      0-BEFORE DATA
   1      0-SYSTEM UNDER TEST CONT.
   1      1-USER CLOCK QUAL.
   1      0-RISING EDGE OF CLOCK
   1      C9-C4 (ANDED CLOCKS)=XXXXXX
   1      1-USER CLOCK SYNTHESIS
   1      0-DELAY CLOCK BY 0
   1      ESYNC: C6=X OR C8=0
   1      WAIT: C7=X OR C9=0
   1
```

f. Using a jumper, apply the signal from the pulse generator going to pin 30 to each of the address/data lines on the ZIF socket in sequence. The ZIF socket is laid out as follows:

Address line	ZIF Pin Number
AD0	40
AD1	32
AD2	33
AD3	34
AD4	36
AD5	35
AD6	37
AD7	38
AD8	39
AD9	1
AD10	2
AD11	3
AD12	4
AD13	5
AD14	9
AD15	8

Press the START/STOP key each time you move the pulse generator to a different address/data line.

g. Observe the 7D02 display. Note that the least significant bit of the data display (indicating the state of multiplexed line AD0) is 0. (All other displayed bits show as 1's in the figure, but since all other bits are floating in this display, they can be either 1 or 0 without affecting anything. We are only concerned with the state of Data 0.) The address may be any value, depending on the power-up state of the latch A1U2060 and A1U3060. The display should look like this:

```
LOC: 00T          TRIGGER
  ADDR:00E9                    IRQ:0
  DATA:1111111111111110-VI     ACK-R
LOC:001
  ADDR:00E9
  DATA:1111111111111110 VI     ACK R
LOC:002
  ADDR:00E9
  DATA:1111111111111110 VI     ACK R
LOC:003
  ADDR:00E9
  DATA:1111111111111110 VI     ACK R
LOC:004
  ADDR:00E9
  DATA:1111111111111110 VI     ACK R
LOC:005
  ADDR:00E9
  DATA:1111111111111110 VI     ACK R
```

h. Change the 7D02 program to observe the display triggered on the falling edge of the clock. To do this press the following 7D02 keys in sequence:

IMMEDIATE
DISPLAY
PROGRAM

Move cursor to RISING EDGE OF CLOCK and change it to FALLING EDGE OF CLOCK. Press the START/STOP key. Note now that all data lines are displayed as 1's, regardless of which Address pin the signal is applied to.

3. Check /AS Setup and Hold.

a. Turn the 7D02 power off.

b. Set the pulse generator duration to 500 ns.

c. Connect the pulse generator to ZIF socket pins 31 (GND), and 30 (clock). Connect pin 30 (clock) to pin 29 (/AS).

d. Turn 7D02 power on.

e. Program the 7D02 as follows:

```
ELSE
TRIGGER
   User Clock Qual.
   User Clock Synthesis
   Delay by 1
   ESYNC: C6=X OR C8=1
   WAIT:C7=X OR C9=X
```


@

The program should look like this:

```
TEST 1
     1ELSE D0
     1  TRIGGER 0-MAIN
     1       0-BEFORE DATA
     1       0-SYSTEM UNDER TEST CONT.
     1       1-USER CLOCK QUAL.
     1       1-FALLING EDGE OF CLOCK
     1       C9-C4 (ANDED CLOCKS)-XXXXXX
     1       1-USER CLOCK SYNTHESIS
     1       0-DELAY CLOCK BY 1
     1       ESYNC: C6=X or C8=1
     1       WAIT: C7=X OR C9=X
     1
```

Then press the START/STOP key.

f. The logic analyzer display should show SLOW CLOCK.

g. Press the following 7D02 keys:

STOP
IMMEDIATE
DISPLAY
PROGRAM

h. Change the program from RISING EDGE OF CLOCK TO FALLING EDGE OF CLOCK. Press the Start/Stop key.

i. The 7D02 should now trigger and give a display.

4. Check Delay added to /WAIT less than or equal to 35 ns.

a. With channel 3 of the oscilloscope still connected to the pulse generator output, connect the pulse generator signal lead to the personality module microprocessor plug pin 6, and ground to pin 31.

b. Connect test oscilloscope channel 2 to pin 6 of the ZIF socket on the personality module, and ground to pin 31. (Use matched probes for these connections.)

c. Set the vertical deflection factor on the oscilloscope to 1 V/Div.

d. Set the test oscilloscope vertical mode to Alt.

e. Ground both test oscilloscope channels and position both traces to the center horizontal graticule line.

f. Set both channels to DC.

g. Determine the delay at 1.4 V (it must be less than 35 ns).

5. Check remaining inputs for maximum voltage in, low limits and minimum voltage in, high limits.

a. Remove the top cover of the PM 108 as described under How to Disassembly Personality Module Pod in Section 6.

b. Set the pulse generator controls as follows:

Duration	500 ns
High level	2.0 V
Low level	0.6 V
Rise/Fall Time	5 ns

c. Connect the pulse generator ground lead to pin 31 of the ZIF socket.

d. Connect the pulse generator signal lead to the ZIF socket pin indicated by the following table.

e. Connect the test oscilloscope to the pin of U3030 or U2030 as shown in the following table to check that the buffer is gating the signal through. Repeat this procedure for signals at all ZIF socket pins in the table.

Signal	ZIF Pin	U3030 Pin	U2030 Pin
St0	21	16	
St1	20	7	
St2	19	18	
St3	18	9	
/MREQ	16		12
/RESET	14		14
R/W	25		16
N/S	26		9

f. To check maximum voltage in limits, change the pulse generator amplitude to produce a pulse of 0-7 volts. Then connect the oscilloscope probe in turn to each address and data line, to the clock signal at pin 30, and to the lines mentioned in the table above to check their respective outputs.

MAINTENANCE AND TROUBLESHOOTING

MAINTENANCE AND CLEANING

Repair

Tektronix, Inc., provides complete instrument service at local Field Service Centers and at the Factory Service Center. Contact your local Tektronix Field office or representative for further information.

Obtaining Replacement Parts

Most electrical and mechanical parts can be ordered through your local Tektronix Field Office or representative. However, you should be able to obtain many of the standard electronic components from a local commercial source in your area. Before you purchase or order a part from a source other than Tektronix, Inc., please check the Replaceable Electrical Parts List, Section 7, and the Replaceable Mechanical Parts List, Section 9, for the proper value, rating, tolerance, and description.

Ordering Parts

When ordering replacement parts from Tektronix, Inc., it is important that all of the following information be included to ensure receiving the proper parts.

1. Instrument type (include modification or option numbers).
2. Instrument serial number.
3. A description of the part (if electrical, include component and number from the Electrical Parts List.)
4. The Tektronix part number.

Cleaning Instructions

This instrument should be cleaned as often as operating conditions require. Accumulation of dirt on components acts as an insulating blanket and prevents efficient heat dissipation, which can cause overheating and component breakdown.

Exterior

Loose dust on the personality module pod can be brushed off. Dirt that remains can be removed with a soft cloth dampened with a mild detergent and water solution. Abrasive cleaners should not be used.

CAUTION

Use only enough water to dampen the cloth or swab. Prevent water from getting inside the pod. Don't get the microprocessor plug or logic analyzer plug wet. DO NOT use chemical cleaning agents. They may damage the plastics used in the instrument. In particular, avoid chemicals that contain benzene, toluene, xylene, acetone or similar solvents.

Interior

Dust in the interior should be removed with a jet of dry, low pressure air and a soft brush.

After major repairs flush the board well with clean isopropyl alcohol. Make certain soldering resin and dirt are removed from the board.

How to Disassemble Personality Module Pod

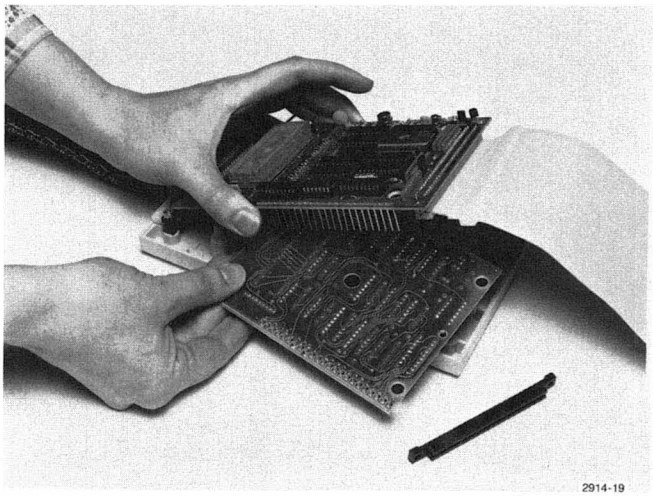
1. To remove the top cover, unscrew the four middle screws on the bottom of the Personality Module.
2. Lift the top cover off. The top board, A1, is now accessible.
3. To access the bottom board, A2, loosen the two end screws on the twisted pair woven cable end so that the cable can move inside the strain relief.
4. Remove the two end screws on the other end of the pod.
5. Lift up gently on the top board. It will remain attached on the twisted pair woven cable end.

6. Lift the bottom board out and turn it face down.

7. Plug J4010 into P4010.

8. The pod may now be operated, with both boards accessible for signature analysis.

To reassemble the instrument, reverse the above procedure.



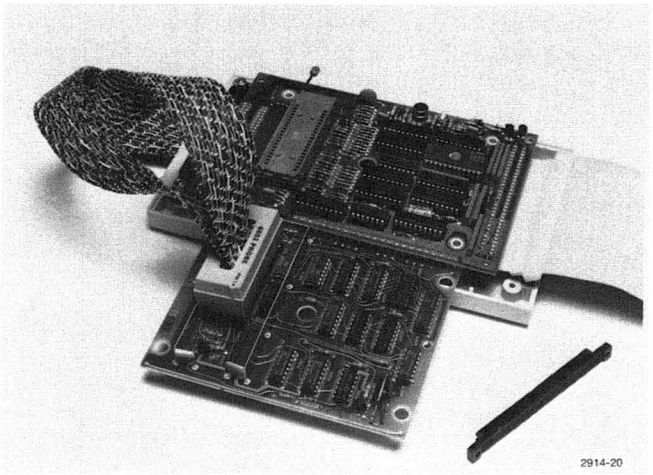


Fig. 6-1. How to Disassemble Personality Module Pod.

How to Disassemble Microprocessor Plug

If the pins on the microprocessor plug bend or break, the pin assembly is replaceable. Simply remove the two screws on the front of the plug and lift off the front. Replace the pin assembly (Tektronix part number 352-0536-00). Replace the plug front and the two screws.

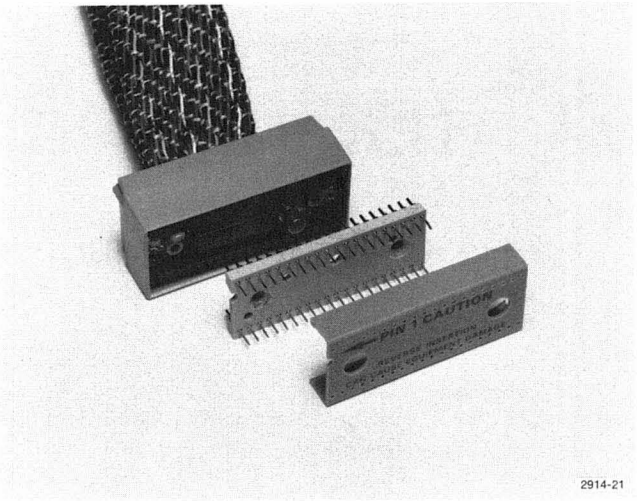


Fig. 6-2. How to Disassemble Personality Module Microprocessor Plug.

TROUBLESHOOTING -- where to find:

- Performance Check—Section 5
- Troubleshooting Procedure—Section 6
- Circuit Descriptions—Section 4
- Schematics—Section 8
- Signature Analysis Tables—Section 6
- Signal Glossary—Section 10

Several methods of verifying performance are available to the service technician for localizing and identifying problems in the PM 108. The Performance Check in Section 5 tests many of the functions of the Personality Module. The 7D02 Diagnostics also test the Personality Module. The Troubleshooting Procedure in this section is designed 1) to verify that the fault lies with the personality module, and not the logic analyzer; and 2) to aid the user in isolating the problem in the personality module. The procedure makes use of the personality module self-test circuitry, 7D02 Diagnostics, and signature analysis.

How to Use the Self Test Circuitry

On the bottom side of the PM 108 Personality Module is a plastic door covering the self-test stimulus generator outputs. Some 7D02 diagnostic tests will run only if the self-test plug is inserted into the test socket. The 7D02 indicates when this is necessary with the message "PLEASE CONNECT SELF TEST STIMULUS."

The self test should only be used in a service situation. For a better understanding of self test circuitry, see Section 4, Theory of Operation.

Before starting the Self Test procedure, the mainframe power switch is turned off, the 7D02 is installed in the mainframe, PM 108 is installed in the 7D02.

1. If a microprocessor is in the personality module ZIF socket, remove it. Never operate the self test with the microprocessor in the ZIF socket.

2. Open the plastic cover on the bottom of the pod by inserting a small screw driver into the latch slot and gently prying up the cover.

3. Switch jumper J1065 from NORM to TEST.

4. Insert the P6451 Timing Option plug into the self test as follows: connect the P6451 ground to the ground pin of J3070 in the self test socket, connect P6451 0-7 to J3075 pins 1-8.

5. Insert the P.M. microprocessor plug into test socket J2065. Make sure the microprocessor plug is inserted correctly, with pin 1 in the proper position. The cable should not be twisted. (See Fig. 6-3)

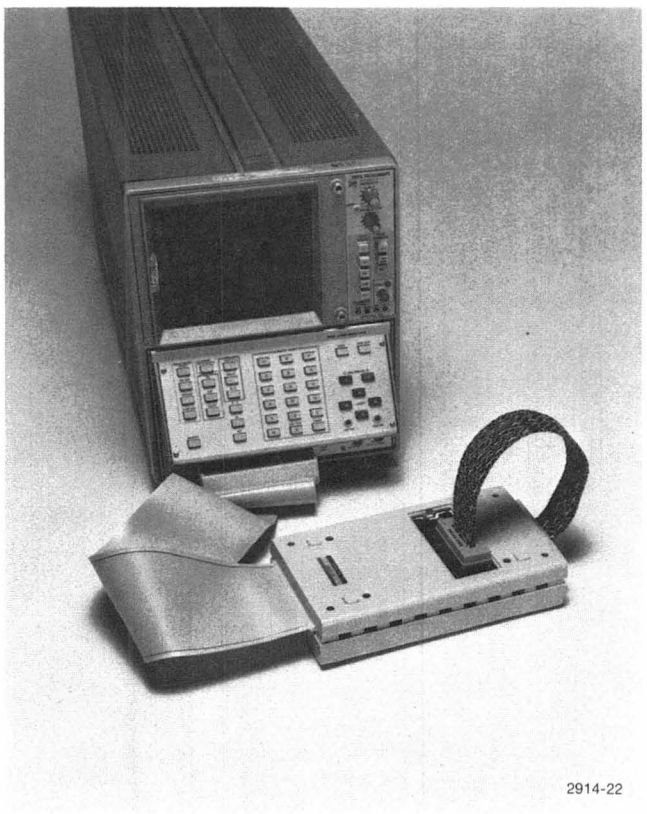


Fig. 6-3. PM 108 with microprocessor plug inserted into Self-Test socket.

6. While holding down any 7D02 key to force the 7D02 into diagnostic mode, turn the mainframe power switch on.

7. Select and execute the desired 7D02 diagnostic tests. The only 7D02 diagnostic tests that require the microprocessor plug in the self test socket are 0 - TEST ALL, 9 - PER. MOD. - SYSTEM, and B - TIMING OPTION.

8. For more information about the diagnostic tests for the PM 108, see Troubleshooting Procedure, below.

9. When testing is completed, turn off the mainframe power switch.

10. Remove the microprocessor plug and P6451 plug from self test socket.

11. Return P1065 to NORM.

12. Replace the plastic cover.

CAUTION

Always protect the self test socket by replacing the plastic cover when through testing.

How to Use the 7D02 Diagnostic Module 9 - PER. MOD. - SYSTEM

Connect the PM 108 personality module microprocessor plug to the self test socket. (See "How to Use the Self Test Circuitry.") Hold down any 7D02 key to force the 7D02 into diagnostic mode.

Press the X (Don't Care) key on the 7D02 keypad. Press 9 on the 7D02 keypad. Press the START/STOP key to begin the following tests.

TEST 1

The first test in the Diagnostic Monitor checks the Data line from the 7D02 to the Personality Module ROM for high and low data, checks the Logic Analyzer's ability to read the ROM, and checks the functioning of the SEL P and LOOK lines from the 7D02 to the PM 108. The test reads a byte (ØFFH) in the Personality Module to determine the length of the ROM. Using this data, it locates the ROM Trailer and reads the value at location 3FFFC. This value is compared with the value at 3FFFD, which should be its

complement. If the two bytes are not complementary, the displayed error message for 8K ROM is:

1 FAIL 3FFFD - X

If an incorrect value is found at 3EØ1Ø, the error message is:

1 FAIL 3YYFD - X

The X signifies the first non-complementary data bit when the two bytes are compared on a bit-by-bit basis from least significant to most significant bit. The most significant part of the address implies the ROM lengths, as indicated by the value at 3EØ1Ø. If the ROM cannot be read correctly, this byte may be any random value (as indicated by YY in the second error message display). If the ROM is not present in the circuit, or cannot be read at all, the value will usually be 3FFH.

If the part of the test just described passes, it is assumed that the ROM can be read correctly and the ROM location is checked. The value at 3FFF9 should be equal to ØFFH. If the Location Byte is correct, the test will print "PASS" followed by the ROM part number. If incorrect, the test will print "FAIL" followed by the part number—for example, 1 PASS 1023-00 or 1 FAIL 1023-00. This is the only place in the tests where any data follows the word "PASS". It is not a failure, but actually a way of verifying that the correct ROM is present. The part number prefix is 160-, so the complete ROM part number in this case is 160-1023-00.

TEST 2

This test ensures that all ROM addresses are read correctly, and that the ROM functions properly. A failure in Test 2 may imply a bad address line, or a faulty ROM. If a failure occurs, the information on the address lines may be checked with a test oscilloscope, or by Signature Analysis as described later in this section.

Test 2 calculates a 16-bit checksum on the Personality Module ROM in accordance with standard Tektronix practice. In the test, the ROM Trailer is located using the value read from 3EØ1Ø in Test 1. The starting address of the checksum is determined. All bytes in the ROM except the two highest bytes are checksummed. When this calculation is complete, the result is compared to the sum of the values in the two remaining locations. If the values do not match exactly, the test fails and the calculated checksum value is displayed as 2 FAIL XXXX, where XXXX is the calculated checksum. If the first part of Test 1 failed, this test will probably also fail. However, if the second part of Test 1 failed, this test may still pass, since the checksum is location-independent.

TEST 3

Test 3 checks the clock circuitry and the /AS line from the Personality Module to the 7D02. Failure of the system to trigger, if caused by the Personality Module, probably means that an address or data line or one of Control lines CØ-C5 has faulty information.

Prior to running this test, the four Word Recognizers are programmed according to data stored in the Personality Module ROM. The Word Recognizers will remain programmed to these values throughout the remainder of the Personality Module Diagnostic Tests. The state machine is programmed as follows:

```
1    IF WR1 THEN TRIGGER MAIN AND TIMING
1    IF WR2 or WR3 or WR4, THEN DON'T
TRIGGER
1    GOTO 1
```

and the Acquisition Memory Board is set for Ø Delay. The Front End Qualifiers and Clock Shifter/Divider are programmed according to data stored in the Personality Module ROM. After all setups are complete a DISPLAY command is sent and the slow clock detector is checked. A Slow Clock indication will result in the following error:

3 FAIL ØFF6Ø1; SLOW, OR NO CLOCK

If the clock appears to be running, the Personality Module ROM is read to determine how long the 7D02 should wait for a trigger to occur, then a STORE command is sent. After waiting the specified length of time, the Activity Monitor on the Acquisition Memory Board is examined to see if the main section has triggered and returned to Display Mode. If the Main Section is still in Store Mode, the following error is generated:

3 FAIL 2E8Ø3-7 ; MAIN SECTION FAILED TO TRIGGER

Failure to trigger can be caused by failure of the Personality Module to generate the WR1 value, failure of the Word Recognizer, the State Machine, or the Acquisition Memory to respond, or lack of State Clocks from the Front End board. A faulty Activity Monitor may also be responsible.

If the Main Section has triggered, a DISPLAY command is sent before proceeding further. This makes certain that the Timing Option will not remain in Store Mode and interfere with reading the Personality Module ROM. The next step is to read the "Last Address +1" Buffer and calculate the trigger location. The trigger location in the Acquisition Memory is examined and the data stored there is compared with the data in the Personality Module ROM that was used to program WR1. Any values that were set to "Don't Care" in WR1 are not compared. If the acquired data does not match the expected data, the following error is reported:

3 FAIL 2YYZZ-X; TRIGGER VALUE INCORRECT

YYZZ is the Acquisition Memory address which holds the data that does not match. The X is the first bit that did not match when comparison was made from least significant

@

bit through most significant bit. The data is compared one byte at a time in the following order:

AØ-A7
A8-A15
DØ-D7
CØ-C5

The FAIL data is interpreted as follows:

YY =	ZZ =	X =	7	6	5	4	3	2	1	Ø	
E0, E1, E2, E3	X0, X4, X8, XC		A7	A6	A5	A4	A3	A2	A1	A0	
E0, E1, E2, E3	X1, X5, X9, XD		A15	A14	A13	A12	A11	A10	A9	A8	
E0, E1, E2, E3	X2, X6, XA, XE		D7	D6	D5	D4	D3	D2	D1	D0	
E0, E1, E2, E3	X3, X7, XB, XF		-	-	C5	C4	C3	C2	C1	C0	C0
E4, E5, E6, E7	XØ, X4, X8, XC		D15	D14	D13	D12	D11	D1Ø	D9	D8	
E4, E5, E6, E7	X1, X5, X9, XD		A23	A22	A21	A20	A19	A18	A17	A16	

This type of failure may be caused by a faulty part in the Acquisition Memory, a bad Memory Address counter, or a faulty "Last Address +1" Buffer. If the Word Recognizer has triggered on the wrong word, or if the state machine has sent Stop Trace prematurely, this failure might result. Still another possibility is that the Main Section failed to acquire data at all.

TEST 4

This test checks all four Word Recognizers, the two counters, the State Machine, and the Acquisition Memory. The four Word Recognizers are programmed as described in Test 3. The State Machine is programmed as follows:

```
1  QUALIFY ALL
1  IF WR2 OR WR3 OR WR4 THEN GOTO 1
1  IF WR1 THEN RESET CTR1 and CTR2, GOTO 2

2  QUALIFY ALL
2  IF WR1 or WR3 or WR4 THEN GOTO 2
2  IF WR2 THEN GOTO 3
2  ELSE INC CTR1

3  QUALIFY ALL
3  IF WR1 OR WR2 OR WR4 THEN GOTO 3
3  IF WR3 THEN GOTO 4
3  ELSE INC CTR2

4  IF WR1 OR WR2 OR WR3 then GOTO 4
4  IF WR4 THEN (DON'T QUALIFY) AND
TRIGGER BOTH
4  ELSE, QUALIFY
```

Starting in State 1, as each of the four Word Recognizers occurs in order, the State Machine advances to the next state. While in State 1, the two counters are reset. While in State 2, Counter is incremented, and while in State 3, Counter 2 is incremented. As this takes place, the Acquisition Memory is acquiring data. When Word Recognizer 4 occurs, that one data sample is not stored, and both the Main Section and the Timing Option are triggered. At this point, the Acquisition Memory Delay Counter begins counting down 240 State Clocks. At the completion of the countdown, it ceases to acquire data. The Acquisition Memory contains the last 16 words generated immediately after Word Recognizer 4. If the Qualify RAM has worked properly, the Word Recognizer 4 value has not been stored. Counter 1 contains the number of clocks that occurred between Word Recognizers 1 and 2, and Counter 2 contains the number of clocks that occurred between Word Recognizer 2 and Word Recognizer 3. The Acquisition Memory Board is set for a delay of 240 clocks, and the Memory Address Counter is preset to ØFDH. The Front End Qualifiers and Clock Shifter/Divider are programmed according to data stored in the Personality Module ROM. After all setups are complete, a DISPLAY command is sent, and the Slow Clock Detector is checked. A Slow Clock indication will result in the following error message:

```
4 FAIL ØFF6Ø-1 ; SLOW, OR NO CLOCK
```

If the clock appears to be running, the Personality Module ROM is read to determine how long the 7D02 should wait for a trigger to occur, then a STORE command is sent. After waiting the specified length of time, the Activity Monitor on the Acquisition Memory Board is examined to see if the Main Section has triggered and returned to Display Mode. If the Main Section is still in Store Mode, the following error message is generated:

```
4 FAIL 2EØ3-7 ; MAIN SECTION FAILED TO
TRIGGER
```

Failure to trigger can be caused by failure of the Personality Module to generate any one of the four Word Recognizer values. Failure of the Word Recognizer, the State Machine, or the Acquisition Memory to respond, or lack of State Clocks from the Front End Board could cause this failure, as could a faulty Activity Monitor.

If the Main Section has triggered, a DISPLAY command is sent before proceeding further. This ensures that the

Timing Option will not remain in Store Mode and interfere with the reading of the Personality Module ROM. The Memory Full bit of the Activity Monitor is examined next. As long as there are at least 16 clocks between the occurrence of Word Recognizer 1 and Word Recognizer 4, the Acquisition Memory must be full. If the Memory Full bit indicates otherwise, the following error message will result:

4 FAIL 2E8Ø3-5 ; MEM FULL BIT NOT SET

The next part of the test is a check of the counters. First the most significant bit of Counter 1 is read and compared with the expected value stored in the Personality Module ROM. If it matches, the least significant bit is compared, then Counter 2 is checked. If any byte fails to match exactly, the following error message will be printed:

4 FAIL 1E2Ø2-X ; CTR1 MSB BIT X IS WRONG
4 FAIL 1E2Ø3-X ; CTR1 LSB BIT X IS WRONG
4 FAIL 1E3Ø2-X ; CTR2 MSB BIT X IS WRONG
4 FAIL 1E3Ø3-X ; CTR2 LSB BIT X IS WRONG

If the counters function properly, the next step is to checksum the Acquisition Memory. All bytes between 2EØØØ and 2E3FF are added together and the result is saved. The expansion option Acquisition Memory is then checksummed by adding together all bytes between 2E400 and 2E7FF. The results of the checksums are compared with the expected data in the PM 108 ROM. Failure of the comparison will result in the following error message:

4 FAIL 3EØ35-X ; MAIN ACQ. MEM. FAILS CHECKSUM
4 FAIL 3E036-X ; EXP. OPT. MEM. FAILS CHECKSUM

Since this RAM is checked separately in the Acquisition Memory and Expansion Option test, this test is primarily of the ability of the RAM to acquire data at high speed. This one checksum could point up an error in any of several areas, such as the Memory Address Counter, the Qualify RAM, or the PM 108 Data Buffers on the Word Recognizer Board. The PM 108 itself, the Front End Qualifiers, or the Acquisition Memory could also be faulty.

TEST 5

This test checks the ability of the State Machine time base to generate ms clocks, and the ability of CTR1 to count those clocks while operating in Control Mode. In Control Mode, the State Machine is programmed as follows:

1 RESET AND START CTR1 50 MS
1 STOP CTR2
1 GOTO 2

2 CONTINUE CTR1
2 STOP CTR2
2 GOTO 2
2 IF CTR1 = Ø THEN TRIGGER

The counters are both loaded with 48 (Desired count-2) and placed in Control Mode (Decrement). The CTR1 time base is set to MS. A DISPLAY Command is sent, and the Acquisition Memory is set for zero delay. The Slow Clock Detector is checked for the presence of a clock from the PM 108. If none is present, the following error message appears:

5 FAIL ØFF6Ø-1 ; SLOW OR NO CLOCK FROM PER. MOD.

If a clock is present, a STORE Command is sent and the processor enters a delay loop for 46 ms. At the end of the delay, the Acquisition Memory Activity Monitor is checked to see whether the State Machine has timed out and returned to Display Mode. If this has occurred, the following error is displayed:

5 FAIL 2E803-2; CTR1 TIMED OUT PREMATURELY

If the Main Section remains in Store Mode, the processor delays another 8 ms, then checks the Activity Monitor again. If the Main Section has not returned to Display Mode, this error message appears in the display:

5 FAIL 2E8Ø3-7 ; CTR1 DIDNT TIME OUT IN 50 MS

Since the processor and Counter Time Base are both derived from the same 6 MHz crystal, this is not intended as a check of absolute time base accuracy.

This type of error might be caused by failure of the Time Base Divider on the State Machine Board; by failure of the counter to count clock pulses correctly, or by failure of the State Machine to respond to the Counter reaching zero.

TEST 6

Test 6 checks the ability of the State Machine Time Base to generate μs clocks, and the ability of Counter 2 to count those clocks while operating in Control Mode. The State Machine is programmed as follows:

1 RESET AND START CTR2 50000 US
1 STOP CTR1
1 GOTO 2

2 CONTINUE CTR2
2 STOP CTR1
2 GOTO 2
2 IF CTR2 = Ø THEN TRIGGER

@

The counters are both loaded with 49998 (Desired count -2), and placed in Control Mode (Decrement). The CTR2 Time Base is set to μs. A DISPLAY Command is sent and the Acquisition Memory is set for zero delay. The Slow Clock Detector is checked for the presence of a clock from the PM 108. If none is present, the following error is displayed:

6 FAIL ØFF6Ø-1 ; SLOW OR NO CLOCK FROM PER. MOD.

If a clock is present, a STORE Command is sent and the processor enters a delay loop for 46 ms. At the end of the delay, the Acquisition Memory Activity Monitor is checked to see if the State Machine has timed out and returned to Display Mode. If this has occurred, an error message is displayed:

6 FAIL 2E8Ø3-2 ; CTR2 TIMED OUT PREMATURELY

If the Main Section remains in Store Mode, the processor delays another 8 ms, then checks the Activity Monitor again. If the Main Section has not returned to Display Mode, the error message is:

6 FAIL 2E8Ø3-7 ; CTR2 DIDNT TIME OUT IN 50000 US.

The processor and Counter Time Base are derived from the same 6 MHz crystal, so this is not intended as a check of absolute Time Base accuracy.

Errors of this type may result from failure of the Time Base Divider on the State Machine Board, by failure of the counter to count the clock pulses correctly, or by failure of the State Machine to respond as the counter reaches zero.

TEST 7

This test checks the Control (Qualifier) lines C4-C9 on the Front End Board. The State Machine is programmed as follows:

```
1  IF WR1 THEN TRIGGER MAIN
1  GOTO 1
```

Word Recognizer 1 was programmed earlier to a value specified by the Personality Module. This test uses each of the Control Lines in turn to qualify out the value to which WR1 has been programmed. If the Control Line operates correctly, the State Clock that occurs with WR1 will be inhibited, and the State Machine will not see the Word Recognizer output. Thus, a PASS condition is indicated by the failure of the Main Section to trigger. A byte in the PM 108 ROM specifies how long the processor should wait for the trigger to occur.

The Clock Shifter/Divider, /ESYNC, and /WAIT are set up in the normal manner as specified by the PM 108 ROM. Six additional bytes in the Personality Module ROM specify the value to write to the Front End Board for each of the six Control Lines to inhibit State Clocks at the occurrence of WR1. The following sequence is repeated six times, once for each Control Line (or until a failure occurs).

```
READ VALUE FROM PER. MOD. ROM
WRITE VALUE TO FRONT END LATCH
SEND STORE COMMAND
WAIT SPECIFIED LENGTH OF TIME
CHECK ACTIVITY MONITOR ON ACQ. MEM. BOARD
IF IN DISPLAY MODE PRINT FAIL AND STOP
```

Because of the way this test operates, a PASS indication may be caused by anything that prevents the Store/Display flipflop on the Acquisition Memory Board from returning to Display Mode. For example, lack of a Clock from the PM 108 may produce a PASS. However, if Tests 3 and 4 pass, it can be assumed that TEST 7 is operating correctly. Test failures on the respective Control Lines are indicated by the following error displays:

7 FAIL 3EØ39 ; C4 DIDNT INHIBIT TRIGGER
7 FAIL 3EØ3A ; C5 DIDNT INHIBIT TRIGGER
7 FAIL 3EØ3B ; C6 DIDNT INHIBIT TRIGGER
7 FAIL 3EØ3C ; C7 DIDNT INHIBIT TRIGGER
7 FAIL 3EØ3D ; C8 DIDNT INHIBIT TRIGGER
7 FAIL 3EØ3E ; C9 DIDNT INHIBIT TRIGGER

Summary of Module Test Failures

Failures in the tests just described which result from SLOW or NO CLOCK may indicate one of the following defects:

1. J1065 is not in the Test position.
2. /AS is not functioning correctly, so there is no ESYNC pulse.
3. WAIT is held high.
4. The Clock circuit of the PM 108 is inoperative.

Failure to read the Personality Module ROM correctly may be caused by a failing address or data line, or a failure on the LOOK or /SEL-P lines from the 7D02.

How to Check Timing Option

Enter the following program and press the 7D02 START/STOP key.

```
1  WORD RECOGNIZER #1
1  DATA=XXXX
1  ADDRESS=XXXX
1  IO/M=X     IRQ=X     FETCH=X     R/W=X
1  /BUSAK=X /MREQ=X EXT     TRIG IN=X
1  TIMING WR=1
1          THRESHOLD V. = Ø—PLUS 1.40
1       Ø—SYNC
1       WORD RECOGNIZER ØØØØØØØØ
1THEN DO
1  COUNTER # 1 Ø —EVENTS
1       Ø—INCREMENT
1OR IF
1  COUNTER # 1 = ØØ25Ø Ø —EVENTS
1THEN DO
1  TRIGGER 1—TIMING
1       1—CENTERED
1       THRESHOLD V. = Ø—PLUS 1. 40
1       Ø—SYNC, TRIGGER IMMEDIATE
  END TEST 1
       DISPLAY ← PROGRAM
```

The display should look like the one in Fig. 6-4.

If the timing display does not look like the one in Fig. 6-4, and the data/address lines are operating correctly, suspect an error in the P6451 probe or the 7D02.

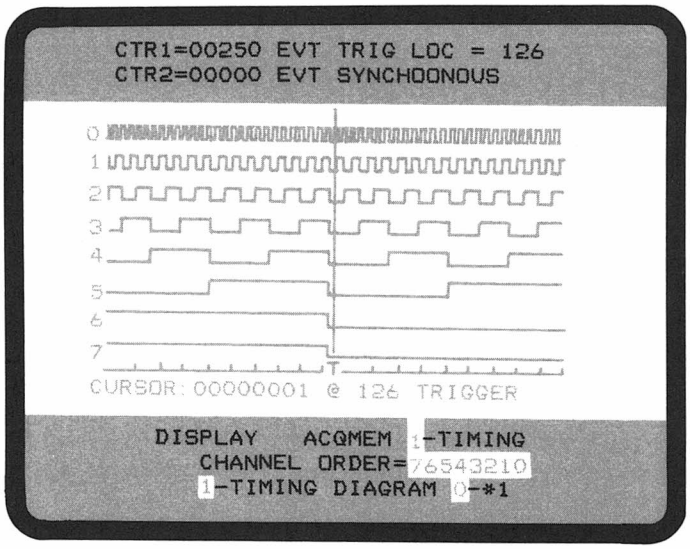


Fig. 6-4. Timing Option Display.

TROUBLESHOOTING BY SIGNATURE ANALYSIS

General Discussion

The recent trend in digital system design is toward bus-structured machines that make use of Large Scale Integration (LSI) components such as microprocessors, ROMs, RAMs, etc. By controlling communication and algorithmic interaction between bus devices, much of the dedicated hardware logic formerly used to handle complex signal and data processing is now replaced by data bit streams in a microprocessor system, for example, functional characteristics of the circuit are difficult to associate with a particular part of the circuitry—and when a fault occurs, its location is extremely hard to pin down.

Board exchange and transition counting are two methods of troubleshooting that have been used widely in LSI systems, but both have severe limitations. A new troubleshooting technique that promises faster, more accurate results is Signature Analysis.

The Concept of Signature Analysis

The basic ingredients of Signature Analysis (SA) are "Data Compression" and "Circuit-generated Stimulus."

Data compression is accomplished in the signature analyzer by probing a logic test node from which data is input for each circuit clock cycle occurring within a circuit-controlled time window. Within the signature analyzer is a 16-bit feedback shift register into which the data is entered in either true or complement logic state, according to previous data-dependent register feedback conditions. There are 65,536 (2^{16}) possible states to which the shift register can be set during a measurement window. These states are encoded and displayed as four hexadecimal characters known as a "signature." This four-character signature is a characteristic number representing time-dependent logic activity during a specified measurement interval for a given circuit node. Any change in the behavior of this node (even a transition that occurs one clock cycle late) will produce a different signature, indicating a probably malfunction in the circuit. A single logic state change on a node is all that's needed to produce a useful signature.

The signal that causes the node to produce a signature is the "stimulus." In SA, the stimulus is supplied by the product itself. In this way, a controlled environment is created wherein selected portions of the circuit are tested independently, while maintaining full dynamic operation. Synchronization and measurement intervals for the signature analyzer are controlled by the system under test. In microprocessor systems, the stimulus is a special program—which in the PM 108 is called Self Test.

Signature Analysis Operation

In operation, signals supplied to the signature analyzer start and stop a measurement time period (called a window or a gate). A clock input synchronizes and controls the data sample rate of the signature analyzer probe input so that data is input to the analyzer and processed every clock cycle within a start/stop interval. The start and stop inputs are individually selectable for logic "1" or "Ø" levels. The clock input is edge triggered, and can be selected for either rising or falling edges. In signature analysis for the PM 108, both start and stop are triggered on negative edges of the clock for all tests. Figure 6-7 illustrates the timing relationships and data generated in a typical measurement window.

PM 108 Signature Analysis

The Signature Tables which follow show the signatures displayed when circuits function properly at each functionally important pin of each component and connector in the PM 108.

PM 108 Signature Tables

Signature Analyzer: Sony/Tektronix Type 308 With P6451 Probe

Disassemble and lay out the personality module boards as described in Fig. 6-1B. Set A2J1065 to the TEST position, and A2J1067 to the RUN position. Connect the signature analyzer probe clock lead to A2TP2020, and the ground lead to pin 1 of A2J3070, the Start lead to pin 2, and the Stop lead to pin 3. Connect the microprocessor plug into the Self Test Socket A2J2065. Power up the 7D02, and enter a program that triggers on ADDRESS=0000, DATA=0000. Press the START/STOP button on the 7D02.

NOTE

Table entries with "- - - -" indicate a normal FAULT caused by "floating" on unused signal lines. The buffer A1U2040 and A1U3040 are examples. The data output lines are floating lines.

Set the Sony/Tektronix type 308 to "Signature" with the following:

Clock ↓
START ↓
STOP ↑

A1	J5020
1	0870
2	C245
3	FCP8
4	2PFA
5	U686
6	PACU
7	0000
8	9F7U
9	2A38
10	PACU
11	PACU
12	PACU
13	0000
14	F5FØ
15	0000
16	F5FØ
17	76FØ
18	1A21
19	9293
20	U9A6
21	616A
22	0000
23	----
24	58ØA
25	PØ4F
26	8Ø46
27	5FU8
28	0000
29	A48Ø
30	PACU
31	0000
32	1319
33	182F
34	UØ9P
35	F5FØ
36	PØ4F
37	A8P1
38	U97H
39	5U7F
40	8CH5

A1	U4010
1	PACU
2	PACU
3	PACU
4	PACU
5	PACU
6	PACU
7	0000
8	0000
9	PACU
10	0000
11	PACU
12	----
13	----
14	PACU

A1	U2020
1	0000
2	----
3	PACU
4	PACU
5	69F7
6	C2C5
7	96PØ
8	----
9	PACU
10	0000
11	0000
12	----
13	7F5U
14	58ØA
15	8378
16	0000
17	0000
18	0000
19	0000
20	PACU

TP 4062
TP 4060-ØØØØ

P3020 1. C2C5
2. C2C5 } **jumper**
3. PACU

A1	U2030
1	0000
2	----
3	76FØ
4	PØ4F
5	PACU
6	F5FØ
7	58ØA
8	F5FØ
9	8Ø46
10	0000
11	8046
12	F5FØ
13	58ØA
14	F5FØ
15	----
16	PØ4F
17	76FØ
18	PACU
19	0000
20	PACU

A1	U3020
1	PACU
2	----
3	8CH5
4	----
5	1319
6	----
7	182F
8	----
9	UØ9P
10	0000
11	PØ4F
12	----
13	F5FØ
14	----
15	----
16	----
17	----
18	----
19	PACU
20	PACU

A1	U3030
1	0000
2	U293
3	PACU
4	616A
5	0000
6	PACU
7	U9A6
8	A480
9	1A21
10	0000
11	1A21
12	A48Ø
13	U9A6
14	PACU
15	0000
16	616A
17	PACU
18	U293
19	0000
20	PACU

A1	U2050
1	0000
2	A8P1
3	1319
4	PØ4F
5	UØ9P
6	182F
7	F5FØ
8	8CH5
9	----
10	0000
11	U97H
12	8CH5
13	F5FØ
14	182F
15	UØ98
16	PØ4F
17	1319
18	----
19	0000
20	PACU

A1	U2060
1	0000
2	F5PA
3	8CH5
4	1319
5	898F
6	8F16
7	182F
8	UØ9P
9	784U
10	0000
11	A480
12	7026
13	PØ4F
14	F5FØ
15	P2PØ
16	547Ø
17	----
18	----
19	7FCP
20	PACU

A1	U3050
1	0000
2	2A38
3	Ø87Ø
4	2PFA
5	FCP8
6	C245
7	U686
8	P21P
9	9F7U
10	0000
11	9F7U
12	P21P
13	U686
14	C245
15	FCP8
16	2PFA
17	0870
18	2A38
19	0000
20	PACU

A1	U3060
1	0000
2	7P61
3	P21P
4	Ø87Ø
5	94ØU
6	2P3A
7	C245
8	FCP8
9	5797
10	0000
11	A480
12	C2C5
13	2PFA
14	U686
15	6AU9
16	C647
17	2A38
18	9F7U
19	0000
20	PACU

A1	U2040
1	7FCP
2	547Ø
3	P2PØ
4	7Ø26
5	784U
6	8F16
7	898F
8	F5PA
9	----
10	----
11	----
12	0000
13	----
14	----
15	----
16	----
17	----
18	580A
19	2P3A
20	PACU
21	5797
22	94ØU
23	7P61
24	PACU

A1	U3040
1	0000
2	C2C5
3	7FCP
4	547Ø
5	P2PØ
6	7Ø26
7	784U
8	8F16
9	898F
10	F5PA
11	----
12	----
13	----
14	0000
15	----
16	----
17	----
18	----
19	----
20	C2C5
21	2P3A
22	PACU
23	5797
24	94ØU
25	7P61
26	PACU
27	PACU
28	PACU

A2 Pin	U1010 Sign
1	ØØØØ
2	PACU
3	PACU
4	PACU
5	0000
6	PACU
7	9F7U
8	A48Ø
9	4P3U
10	PACU
11	0000
12	9F7U
13	76FØ
14	A48Ø

A2 Pin	U1020 Sign
1	AHAU
2	PACU
3	PACU
4	PACU
5	Ø9ØØ
6	P3CU
7	0000
8	7F5U
9	96PØ
10	PACU
11	9F7U
12	0900
13	AHAU
14	PACU

A2 Pin	U4018 Sign
1	76FØ
2	PACU
3	A48Ø
4	PACU
5	38UU
6	H24Ø
7	0000
8	76FØ
9	9F7U
10	PACU
11	0000
12	38UU
13	PACU
14	PACU

A2	U2010
1	U35A
2	616A
3	UCFC
4	PACU
5	PACU
6	0000
7	0000
8	76FØ
9	9F7U
10	9F7U
11	PACU
12	----
13	----
14	PACU

A2	U2020
1	UØ9P
2	182F
3	H37Ø
4	649P
5	PACU
6	5H51
7	0000
8	0000
9	UCFC
10	0000
11	C7PP
12	U35A
13	1319
14	PACU

A2	U4028
1	0000
2	PACU
3	76FØ
4	9F7U
5	76FØ
6	9F7U
7	0000
8	0000
9	0000
10	0000
11	PACU
12	0000
13	0000
14	PACU

A2	U3007
1	PACU
2	H370
3	0000
4	PACU
5	7658
6	9FP7
7	0000
8	PACU
9	PACU
10	PACU
11	PACU
12	PACU
13	PACU
14	PACU

A2	U3020
1	76FØ
2	H573
3	A480
4	PACU
5	8P21
6	649P
7	0000
8	H370
9	39FM
10	PACU
11	A480
12	H6C7
13	76FØ
14	PACU

A2	U4038
1	U9A6
2	1319
3	U293
4	182F
5	1A21
6	UØ9P
7	0000
8	8378
9	69F7
10	PACU
11	0000
12	1P79
13	H6C7
14	PACU

@

A2 Pin	U1030 Sign
1	A480
2	0000
3	8CH5
4	1319
5	182F
6	U09P
7	0000
8	U97H
9	A8P1
10	F5F0
11	P04F
12	0000
13	U09P
14	PACU

A2 Pin	U1040 Sign
1	29CF
2	76F0
3	5U7F
4	UH61
5	76F0
6	0870
7	0000
8	C245
9	890C
10	76F0
11	FCP8
12	924P
13	76F0
14	PACU

A2	U3085
1	PACU
2	8CH5
3	616A
4	PACU
5	1319
6	U9A6
7	0000
8	U293
9	PACU
10	182F
11	1A21
12	PACU
13	U09P
14	PACU

A2	U2030
1	U97H
2	0000
3	29CF
4	UH61
5	890C
6	924P
7	0000
8	PACU
9	5FU8
10	8046
11	580A
12	0000
13	924P
14	PACU

A2	U2040
1	580A
2	76F0
3	2PFA
4	8046
5	76F0
6	U686
7	0000
8	2A38
9	5FU8
10	76F0
11	9F7U
12	PACU
13	76F0
14	PACU

TP	Sign
A2TP1028	A480
A2TP2020	PACU
A2TP2048	76F0
A2TP2007	0000

A2 Pin	U3030 Sign
1	5H51
2	PACU
3	C7PP
4	76F0
5	9FP7
6	PACU
7	0000
8	H370
9	C7PP
10	649P
11	AHAU
12	H573
13	9F7U
14	PACU

A2 Pin	U3040 Sign
1	82F
2	U09P
3	U09P
4	U09P
5	U293
6	H573
7	0000
8	69F7
9	1319
10	U293
11	1A21
12	H6C7
13	U9A6
14	PACU

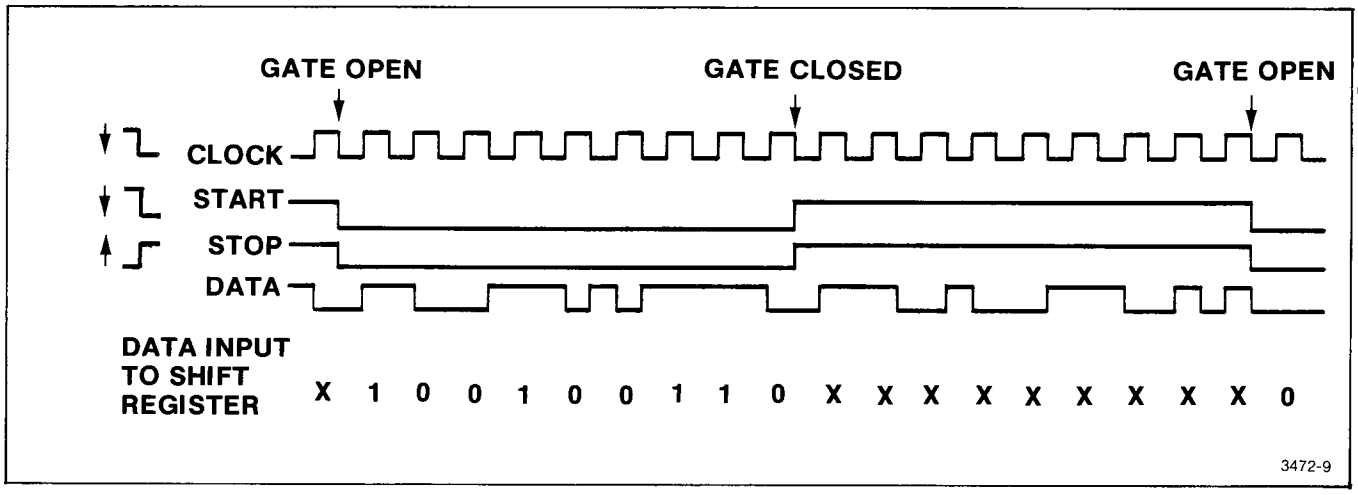
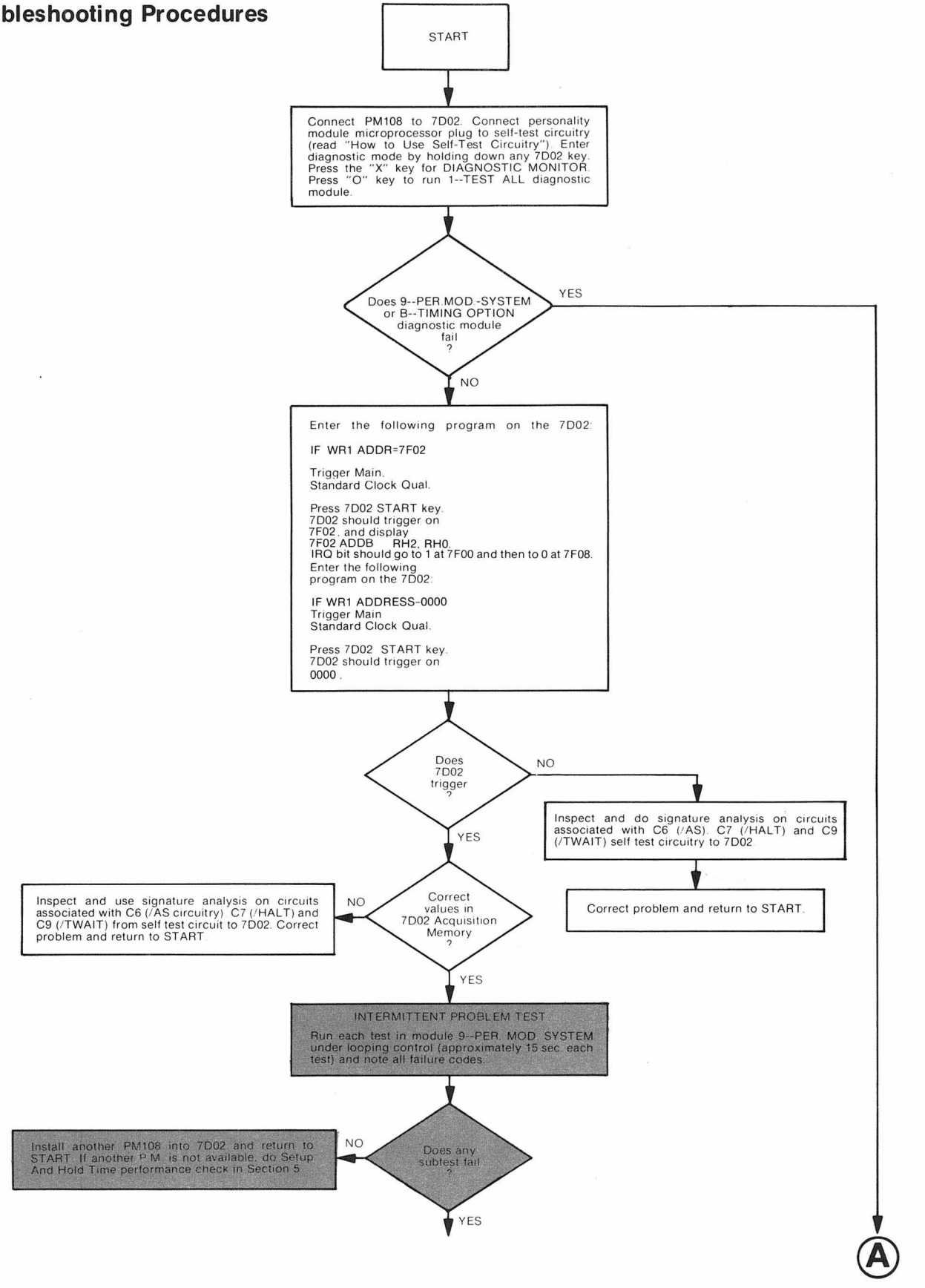


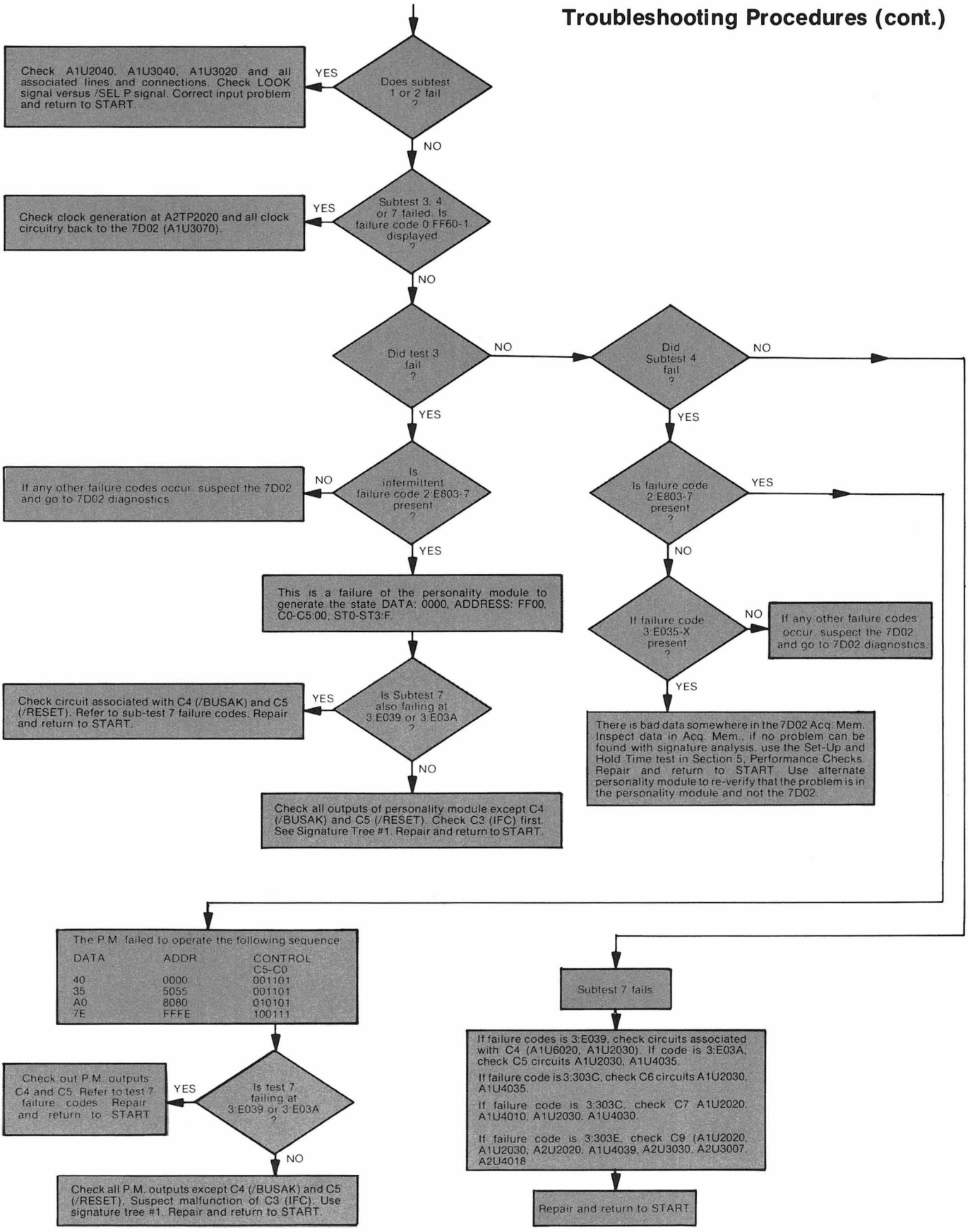
Fig. 6-5. Signature Analysis Timing Diagram.

Troubleshooting Procedures



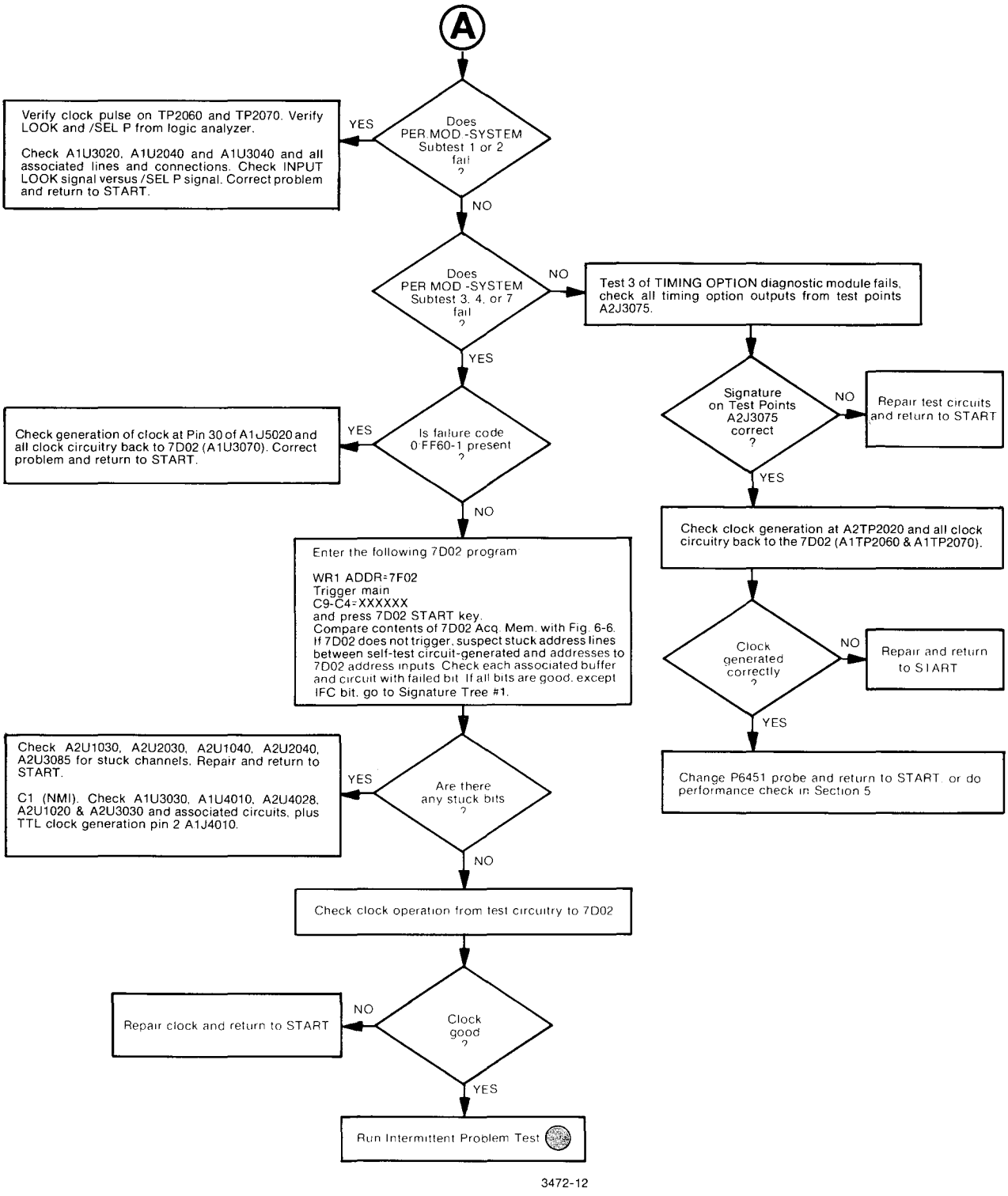
3472-10

Troubleshooting Procedures (cont.)



3472-11

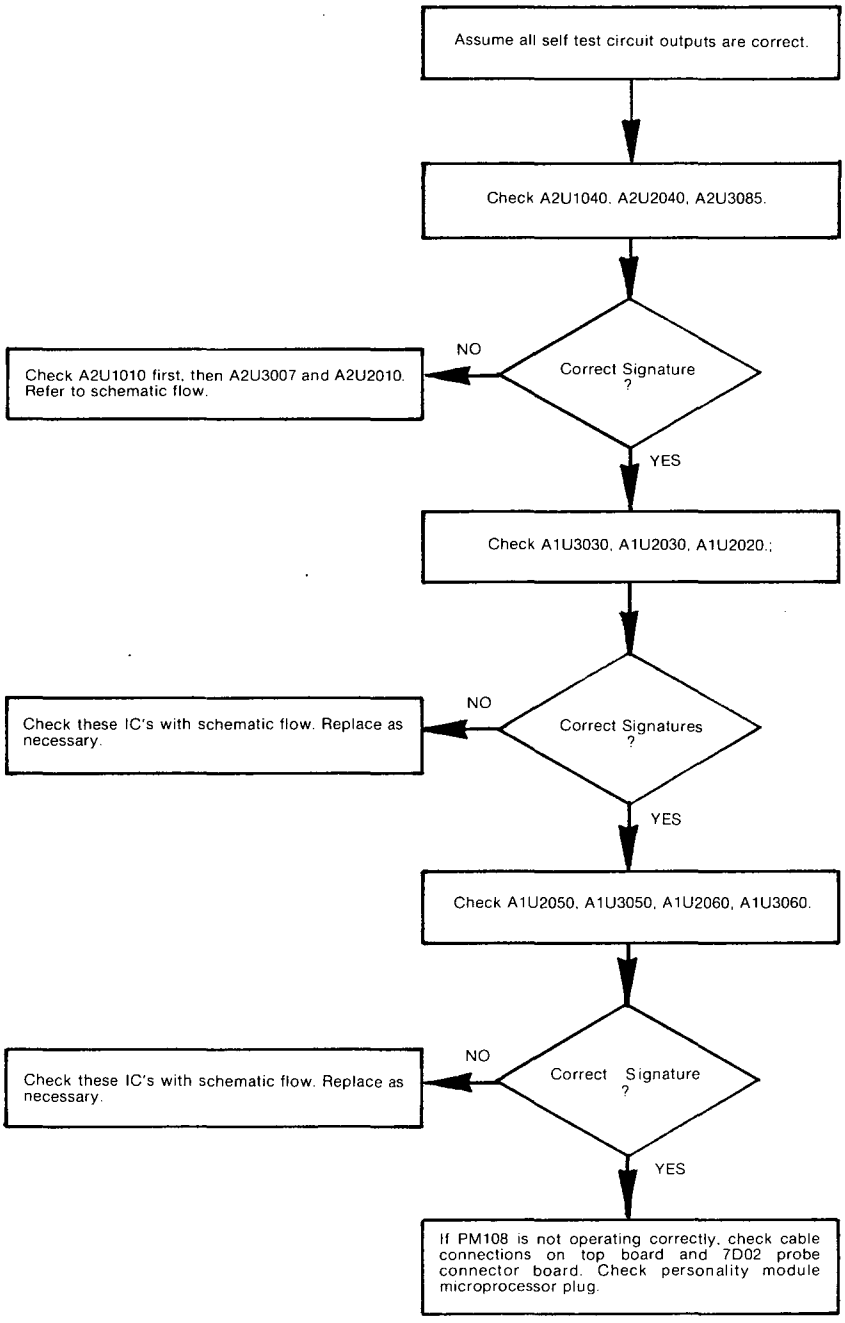
Troubleshooting Procedures (cont.)



3472-12

Troubleshooting Procedures (cont.)

Signature Tree #1



3472-13

LOC	ADDR	OPERATION	IRQ
Ø09	8ØFC	7FFC SPL I/O R	Ø
Ø1Ø	8ØFD	7FFD I/O R	Ø
Ø11	8ØFE	7FFE REFRESH R	Ø
Ø12	8ØFF	7FFF INT OPR R	Ø
Ø13	7FØØ	8ØØØ ------- W	1
Ø14	7FØ1	8ØØ1 EPU XFR W	1
Ø15T	7FØ2—ADD	B—RH2,RHØ--------	1
Ø16	7FØ3	8ØØ3 FETCH N	1
Ø17	7FØ4	8ØØ4 EPU STK W	1
Ø18	7FØ5	8ØØ5 EPU DAT W	1
Ø19	7FØ6	8ØØ6 STK MEM W	1
Ø20	7FØ7	8ØØ7 DAT MEM W	1
Ø21	7FØ8	8ØØ8 VI ACK W	Ø
Ø22	7FØ9	8ØØ9 NVI ACK W	Ø
Ø23	7FØA	8ØØA NMI ACK W	Ø
Ø24	7FØB	8ØØB ------- W	Ø
Ø25	7FØC	8ØØC SPL I/O W	Ø
Ø26	7FØD	8ØØD I/O W	Ø
Ø27	7FØE	8ØØE REFRESH W	Ø

DISPLAY ← ACQMEM Ø—MAIN
1 — MNEMONIC

Fig. 6-6. 7D02 Acquisition Memory.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

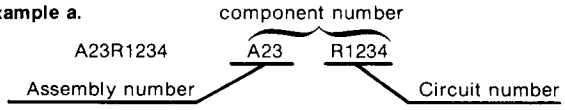
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

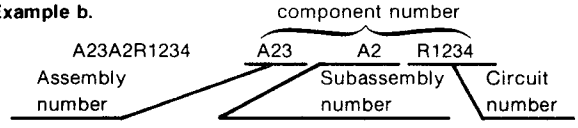
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P O BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
14433	ITT SEMICONDUCTORS	3301 ELECTRONICS WAY P O BOX 3049	WEST PALM BEACH, FL 33402
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
52648	PLESSEY SEMICONDUCTORS	1641 KAISER	IRVINE, CA 92714
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-6896-00			CKT BOARD ASSY:PM108/8002/TOP	80009	670-6896-00
A2	670-6897-00			CKT BOARD ASSY:PM108/8002/BOTTOM	80009	670-6897-00
A3	670-6149-00			CKT BOARD ASSY:PROBE CONNECTOR	80009	670-6149-00
	----- -----			(NO ELECTRICAL PARTS)		
A4	670-6948-00			CKT BOARD ASSY: Z8002 PROBE	80009	670-6948-00
	----- -----			(NOT REPL,ORDER 175-3330-00. NO ELEC PARTS)		
A1	670-6896-00			CKT BOARD ASSY:PM108/8002/TOP	80009	670-6896-00
A1C1010	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A1C1020	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A1C1030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C1050	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C1060	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2050	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2060	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2062	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A1C4020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C4060	281-0765-00			CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710100X5P101J
A1C4070	281-0757-00			CAP.,FXD,CER DI:10PF,20%,100V	72982	8035-D-COG-100G
A1C5060	281-0810-00			CAP.,FXD,CER DI:5.6PF,0.5%,100V	72982	1035D2ADC0G569D
A1C5070	281-0810-00			CAP.,FXD,CER DI:5.6PF,0.5%,100V	72982	1035D2ADC0G569D
A1C6060	281-0757-00			CAP.,FXD,CER DI:10PF,20%,100V	72982	8035-D-COG-100G
A1C6062	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A1CR2062	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A1CR2070	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A1CR3060	152-0071-00			SEMICOND DEVICE:GERMANIUM,15V,40MA	14433	G865
A1CR6060	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR6062	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1Q2070	151-0282-00			TRANSISTOR:SILICON,NPN	80009	151-0282-00
A1Q3070	151-0427-00			TRANSISTOR:SILICON,NPN	80009	151-0427-00
A1Q3072	151-0427-00			TRANSISTOR:SILICON,NPN	80009	151-0427-00
A1R1010	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210B680
A1R1025	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210B680
A1R1035	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210B680
A1R1045	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210B680
A1R1066	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210B680
A1R1074	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210B680
A1R1665	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210B680
A1R2010	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210B680
A1R2015	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210B680
A1R2060	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R2070	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	01121	CB1625
A1R3010	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210B680
A1R3070	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A1R4060	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A1R4070	321-0208-00			RES.,FXD,FILM:1.43K OHM,1%,0.125W	91637	MFF1816G14300F
A1R5060	321-0344-00			RES.,FXD,FILM:37.4K OHM,1%,0.125W	91637	MFF1816G37401F
A1R5062	321-0286-00			RES.,FXD,FILM:9.31K OHM,1%,0.125W	91637	MFF1816G93100F
A1R5070	321-0274-00			RES.,FXD,FILM:6.98K OHM,1%,0.125W	91637	MFF1816G69800F
A1R6060	321-0631-00			RES.,FXD,FILM:12.5K OHM,1%,0.125W	91637	MFF1816G12501F
A1U2020	156-0914-00			MICROCIRCUIT,DI:OCT ST BFR W/3-STATE OUT	01295	SN74LS240
A1U2030	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	04713	SN74LS244N OR J
A1U2040	160-1023-00			MICROCIRCUIT,DI:4096 X 8 EPROM,PRGM,HI INT	80009	160-1023-00
A1U2050	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	04713	SN74LS244N OR J

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1U2060	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
A1U3020	156-0916-02			MICROCIRCUIT,DI:8-2 INP 3-STATE BFR,BURN	27014	DM81LS97
A1U3030	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	04713	SN74LS244N OR J
A1U3040	160-1086-00			MICROCIRCUIT,DI:4096 X 8 EPROM,PRGM	80009	160-1086-00
A1U3050	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	04713	SN74LS244N OR J
A1U3060	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
A1U3070	156-1344-00			MICROCIRCUIT,LI:COMPARATOR ECL	52648	SP9685CM
A1U4010	156-0480-00			MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	01295	SN74LS08(N OR J)
A1U4030	155-0230-00			MICROCIRCUIT,DI:INPUT PROTECTION	80009	155-0230-00
A1U4035	155-0230-00			MICROCIRCUIT,DI:INPUT PROTECTION	80009	155-0230-00
A1U4039	155-0230-00			MICROCIRCUIT,DI:INPUT PROTECTION	80009	155-0230-00
A1U4050	155-0230-00			MICROCIRCUIT,DI:INPUT PROTECTION	80009	155-0230-00
A1U4055	155-0230-00			MICROCIRCUIT,DI:INPUT PROTECTION	80009	155-0230-00
A1U4059	155-0230-00			MICROCIRCUIT,DI:INPUT PROTECTION	80009	155-0230-00
A1U6020	155-0230-00			MICROCIRCUIT,DI:INPUT PROTECTION	80009	155-0230-00
A1U6060	155-0230-00			MICROCIRCUIT,DI:INPUT PROTECTION	80009	155-0230-00
A1U6065	155-0230-00			MICROCIRCUIT,DI:INPUT PROTECTION	80009	155-0230-00
A1VR2060	152-0611-00			SEMICOND DEVICE:ZENER,0.4W,9V,2%	80009	152-0611-00

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2	670-6897-00			CKT BOARD ASSY:PM108/8002/BOTTOM	80009	670-6897-00
A2C1018	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C1028	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C1038	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2008	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2018	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2038	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2080	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2085	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A2C3028	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C3038	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C4007	283-0645-00			CAP.,FXD,MICA D:790PF,1%,100V	00853	D151E791F0
A2C4010	283-0645-00			CAP.,FXD,MICA D:790PF,1%,100V	00853	D151E791F0
A2C4022	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C4030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C4040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2L3018	108-0666-00			COIL,RF:900NH	80009	108-0666-00
A2Q3010	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A2R2007	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A2R2028	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R4015	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2U1010	156-0387-02			MICROCIRCUIT,DI:DUAL J-K FLIP-FLOP	01295	SN74LS73NP3
A2U1020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A2U1030	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR,BURN IN	80009	156-1172-01
A2U1040	156-0381-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATES	80009	156-0381-00
A2U2010	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A2U2020	156-0481-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT AND GATE	07263	74LS11(PC OR DC)
A2U2030	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR,BURN IN	80009	156-1172-01
A2U2040	156-0381-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATES	80009	156-0381-00
A2U3007	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A2U3020	156-0331-00			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74S74PC
A2U3030	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A2U3040	156-0481-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT AND GATE	07263	74LS11(PC OR DC)
A2U3085	156-0381-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATES	80009	156-0381-00
A2U4018	156-0331-00			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74S74PC
A2U4028	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0385-00
A2U4038	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0385-00
A3	670-6149-00			CKT BOARD ASSY:PROBE CONNECTOR	80009	670-6149-00
	----- -----			(NO ELECTRICAL PARTS)		
A4	670-6948-00			CKT BOARD ASSY: Z8002 PROBE	80009	670-6948-00
	----- -----			(NOT REPL,ORDER 175-3330-00. NO ELEC PARTS)		

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966 Drafting Practices.
Y14.2, 1973 Line Conventions and Lettering.
Y10.5, 1968 Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

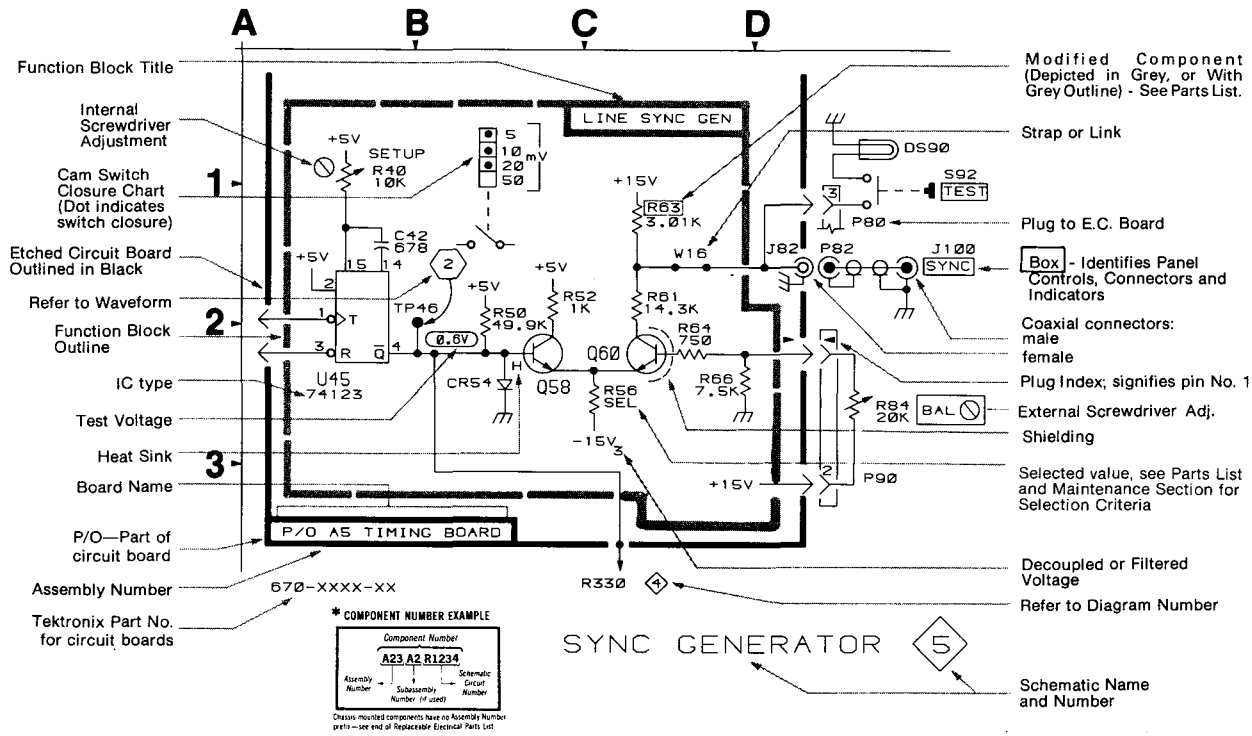
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



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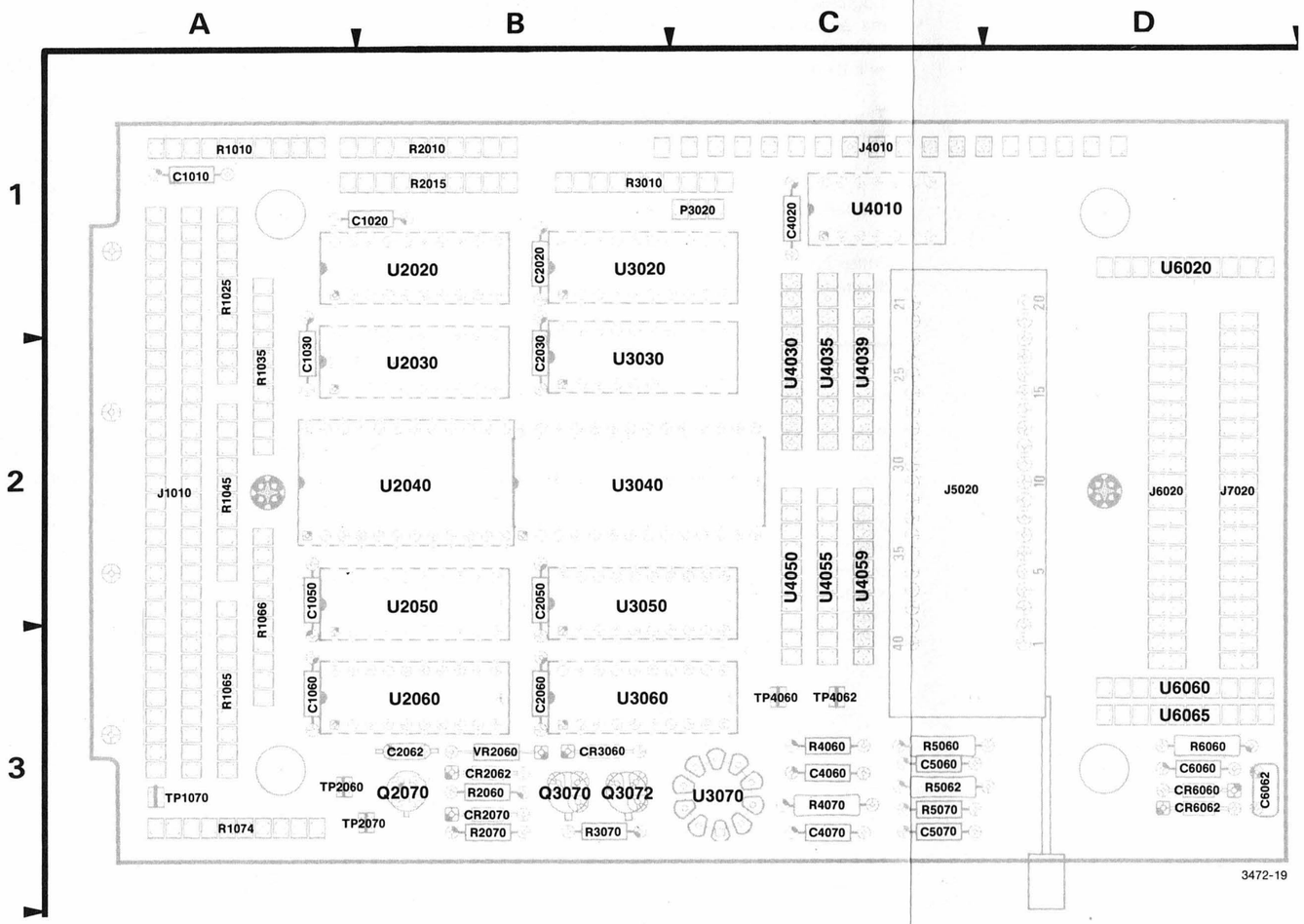
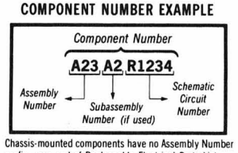


Figure 8-1. A1 Upper Board Component Locations.

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

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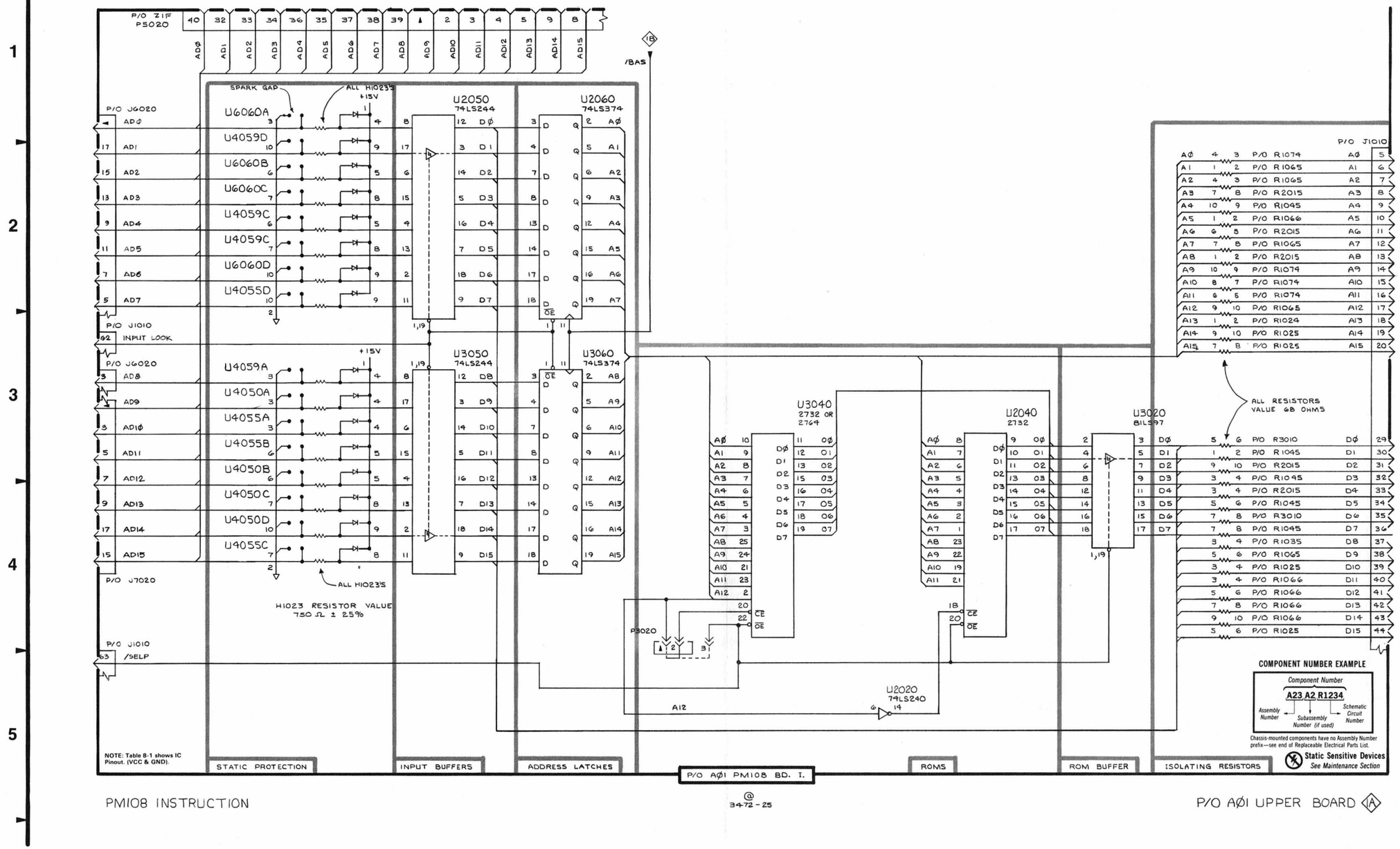
Table 8-1

IC Pin Information

Device Type	VCC	GND
2732	24	12
2764	24	12
74LS00	14	7
74LS04	14	7
74LS08	14	7
74LS11	14	7
74LS73	14	7
74LS74	14	7
74LS86	14	7
74LS240	20	10
74LS244	20	10
74LS374	20	10
74LS393	14	7
81LS97	20	10

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1010	A3	A1	U2020C	D5	B1
J1010	A5	A1	U2040	E3	B2
J1010	F2	A1	U2050	B2	B2
J5020	A1	C2	U2060	C2	B3
J6020	A1	D2	U3020	E3	B1
J6020	A3	D2	U3040	D3	B2
J7020	A4	D2	U3050	B3	B2
			U3060	C3	B3
P3020	C4	C1	U4050A	A3	C2
			U4050B	A3	C2
R1025	F3	A1	U4050C	A4	C2
R1025	F4	A1	U4050D	A4	C2
R1045	F2	A2	U4055A	A3	C2
R1045	F3	A2	U4055B	A3	C2
R1045	F4	A2	U4055C	A4	C2
R1065	F2	A3	U4055D	A2	C2
R1065	F4	A3	U4059A	A3	C2
R1066	F2	A2			
R1074	F2	A3	U4059B	A2	C2
R1074	F3	A3	U4059C	A2	C2
R2015	F2	B1	U4059D	A1	C2
R2015	F3	B1	U6060A	A1	D3
R2015	F4	B1	U6060B	A2	D3
R3010	F3	B1	U6060C	A2	D3
R3010	F4	B1	U6060D	A2	D3



PM108 INSTRUCTION

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P/O AØ1 UPPER BOARD 1A

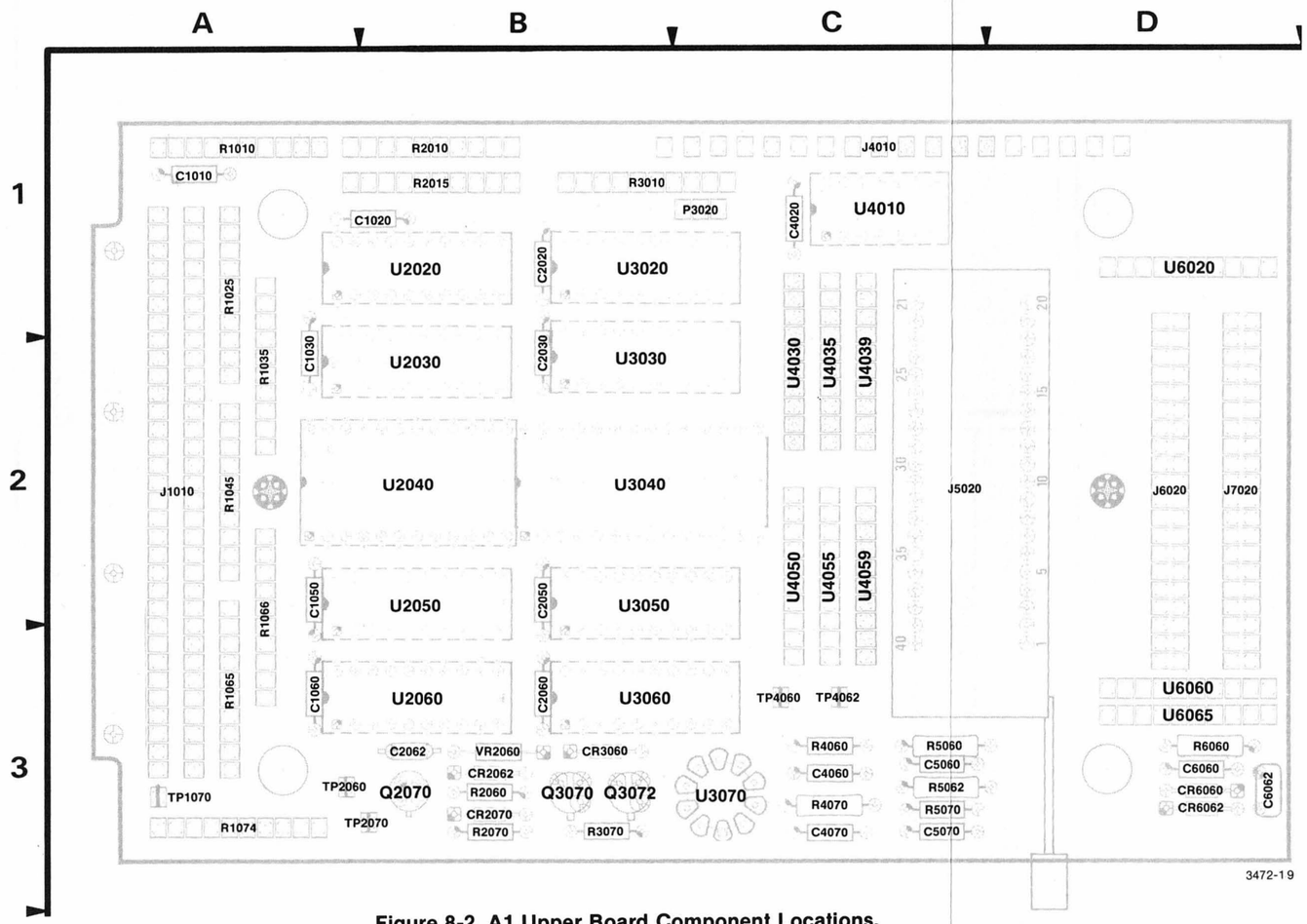
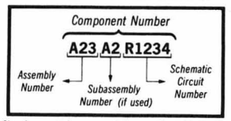


Figure 8-2. A1 Upper Board Component Locations.

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

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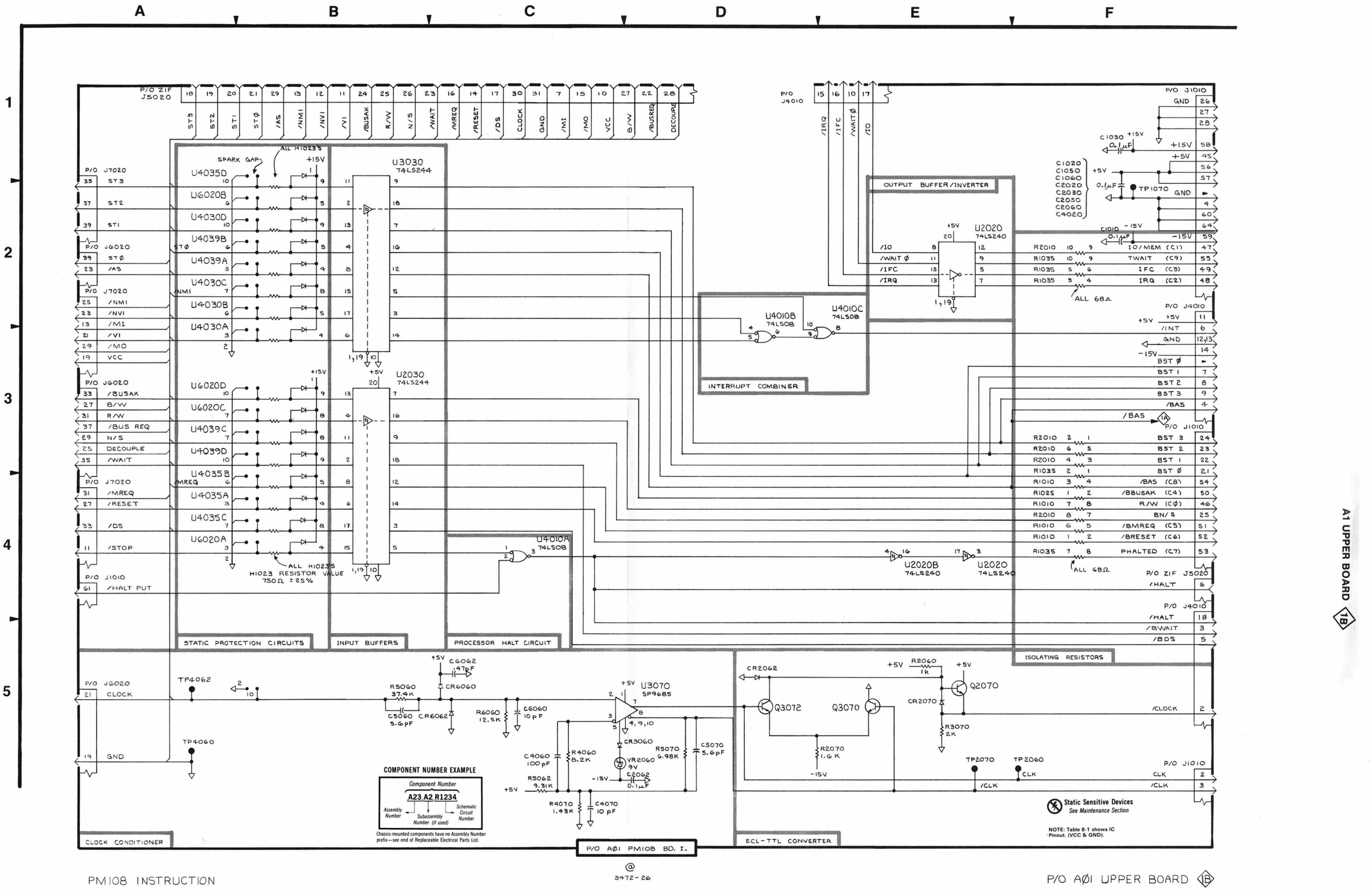
ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1010	F2	A1
C1020	F1	B1
C1030	F1	A2
C1050	F1	A2
C1060	F1	A3
C2020	F1	B1
C2030	F1	B2
C2050	F1	B2
C2060	F1	B3
C2062	D5	B3
C4020	F1	C1
C4060	C5	C3
C4070	C5	C3
C5060	B5	C3
C5070	D5	C3
C6060	C5	D3
C6062	C5	D3
CR2062	D5	B3
CR2070	E5	B3
CR3060	D5	B3
CR6060	C5	D3
CR6062	C5	D3
J1010	A4	A1
J1010	F1	A1
J1010	F3	A1
J1010	F5	A1
J4010	E1	C1
J4010	F2	C1
J4010	F5	C1
J5020	A1	A2
J6020	A2	D2
J6020	A3	D2
J6020	A5	D2
J7020	A2	D2
J7020	A4	D2
Q2070	E5	B3
Q3070	E5	B3
Q3072	D5	B3
R1010	F4	A1
R1025	F4	A1
R1035	F2	A2
R1035	F3	A2
R1035	F4	A2
R2010	F2	B1
R2010	F3	B1
R2010	F4	B1
R2060	E5	B3
R2070	E5	B3
R3070	E5	B3
R4060	C5	C3
R4070	C5	C3
R5060	B5	C3
R5062	C5	C3
R5070	B5	C3
R6060	C5	D3
TP1070	F1	A3
TP2060	F5	A3
TP2070	E5	B3
TP4060	A5	C3
TP4062	A5	C3
U2020	E2	B1
U2020B	E4	B1
U2020H	E4	B1
U2030	B3	B2
U3030	B2	B2
U3070	D5	C3
U4010A	C4	C1
U4010B	D3	C1
U4010C	E2	C1
U4030A	A2	C2
U4030B	A2	C2
U4030C	A2	C2
U4030D	A2	C2
U4035A	A4	C2
U4035B	A4	C2
U4035C	A4	C2
U4035D	A1	C2
U4039A	A2	C2
U4039B	A2	C2
U4039C	A3	C2
U4039D	A3	C2
U6020A	A4	D1
U6020B	A2	D1
U6020C	A3	D1
U6020D	A3	D1
U6065D	B5	D3
VR2060	D5	B3



PM108 INSTRUCTION

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P/O AØ1 UPPER BOARD 1B

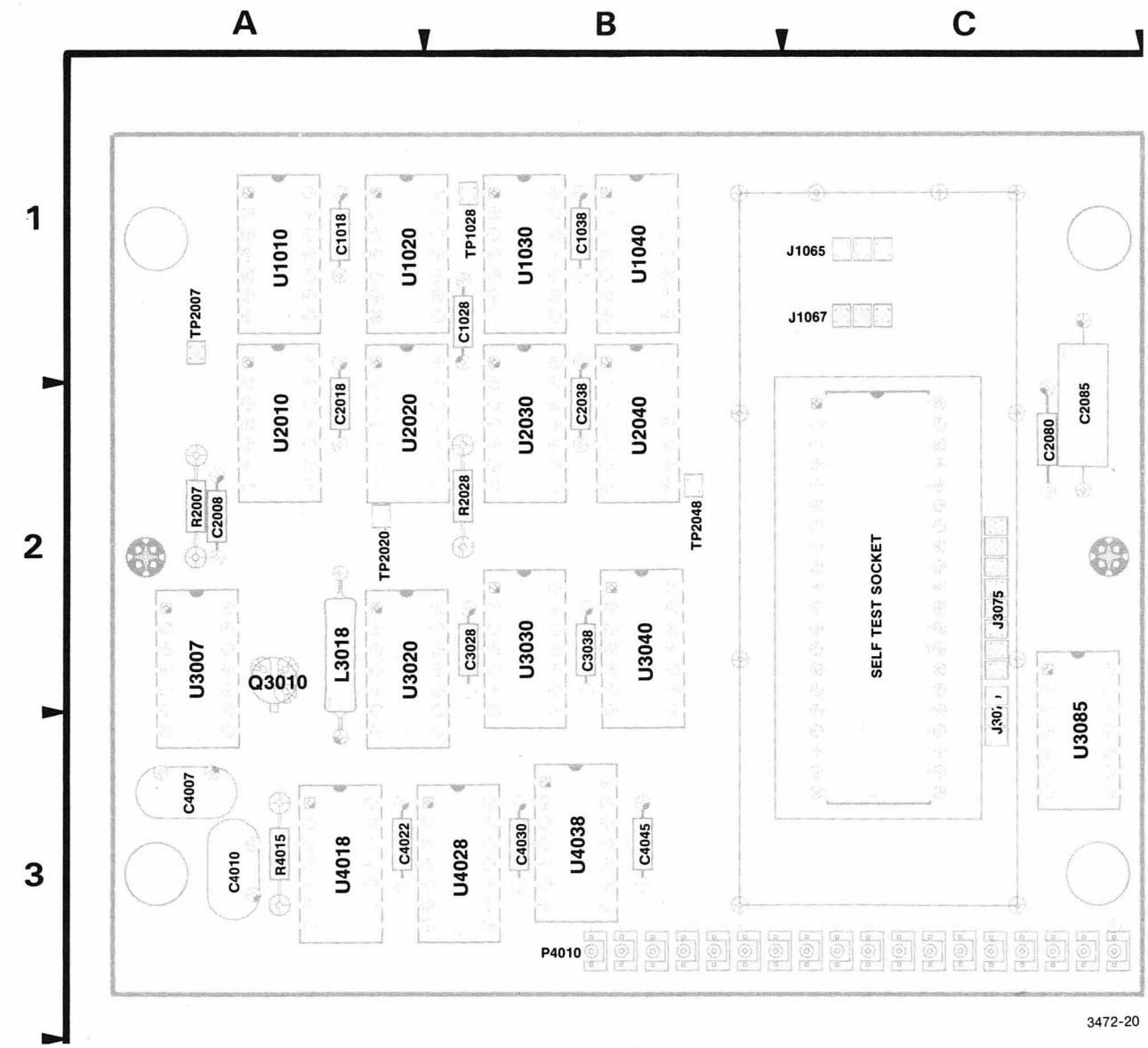
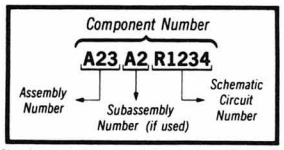


Figure 8-3. A2 Lower Board Component Locations.

A2 LOWER BOARD

COMPONENT NUMBER EXAMPLE

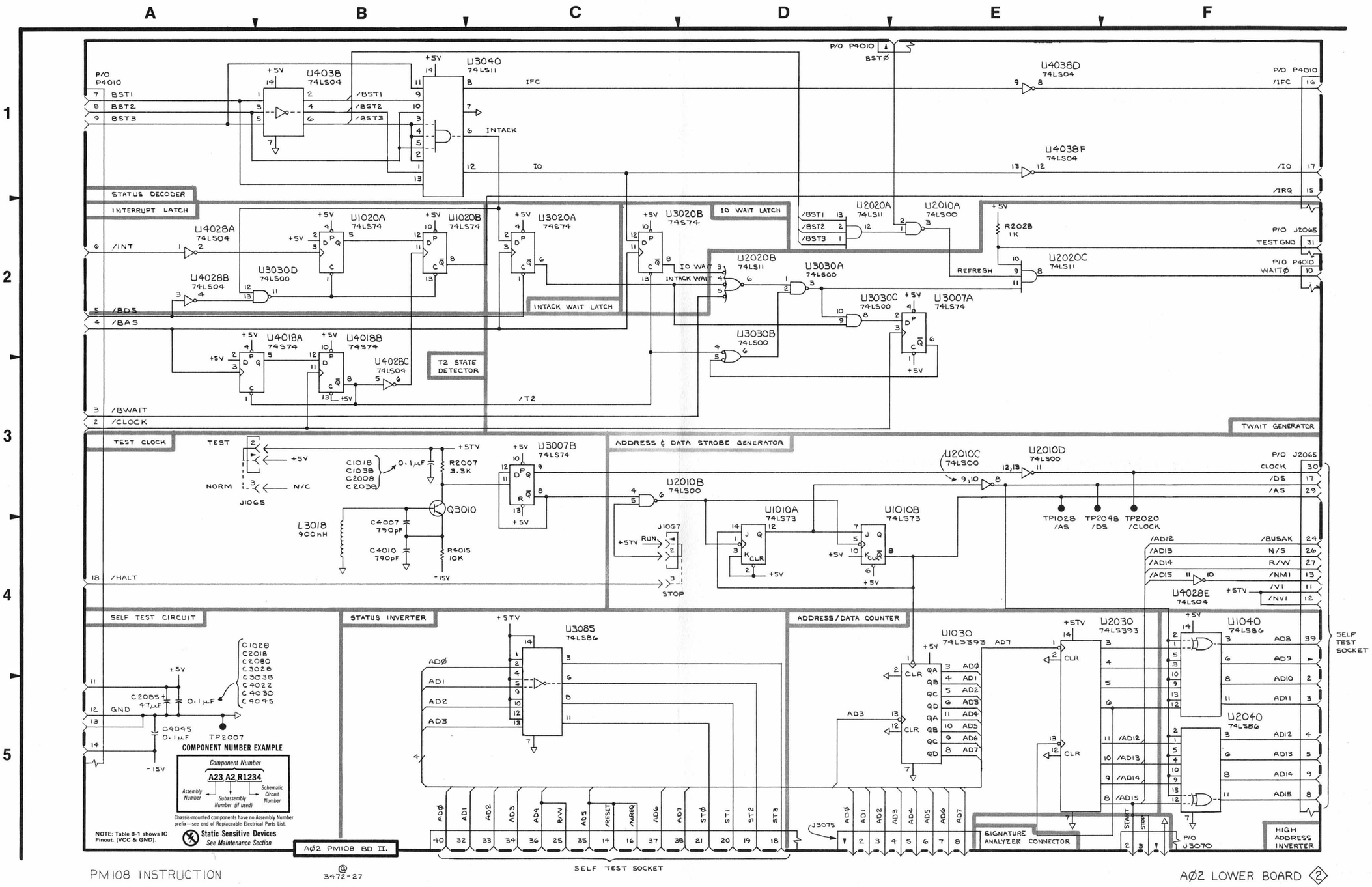


Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1018	B3	A1
C1028	A5	B1
C1038	B3	B1
C2008	B3	A2
C2018	A5	A2
C2038	B3	B2
C2080	A3	C2
C2085	A5	C2
C3028	A5	B2
C3038	A5	B2
C4007	B4	A3
C4010	B4	A3
C4022	A5	A3
C4030	A5	B3
C4045	A5	B3
J1065	A3	C1
J1067	C4	C1
J3070	F5	C3
J3075	E5	C2
L3018	B4	A2
P4010	A1	B3
P4010	D1	B3
P4010	F1	B3
Q3010	B3	A2
R2007	B3	A2
R2028	E2	B2
R4015	B4	A3
SELF TEST SOCKET	C5	B1
SELF TEST SOCKET	F4	B1
TP1028I	E3	B1
TP2007	A3	A1
TP2048	E3	B2
TP2020	F3	A2
U1010A	D4	A1
U1010B	D4	A1
U1020A	B2	A1
U1020B	B2	A1
U1030	E5	B1
U1040	F4	B1
U2010A	E2	A2
U2010B	C3	A2
U2010C	E3	A2
U2010D	E3	A2
U2020A	D2	A2
U2020B	D2	A2
U2020C	E2	A2
U2030	E5	B2
U2040	F5	B2
U3007A	E2	A2
U3007B	C3	A2
U3020A	C2	A2
U3020B	C2	A2
U3030A	D2	B2
U3030B	D2	B2
U3030C	D2	B2
U3030D	B2	B2
U3040	B1	B2
U3085	C4	C3
U4018A	B3	A3
U4018B	B3	A3
U4028A	A2	B3
U4028B	A2	B3
U4028C	B3	B3
U4028D	F4	B3
U4038	B1	B3
U4038D	E1	B3
U4038F	E1	B3



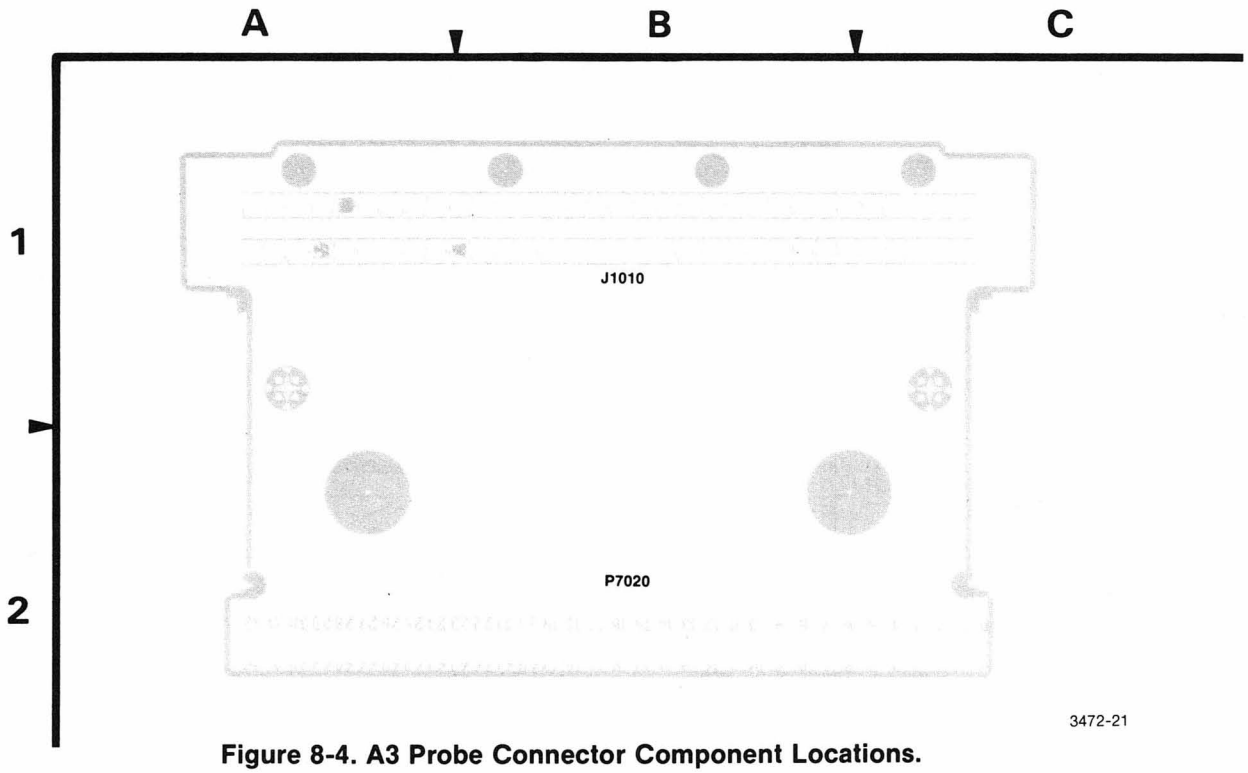
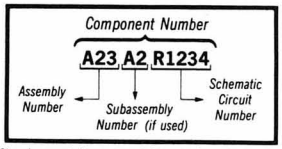


Figure 8-4. A3 Probe Connector Component Locations.

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

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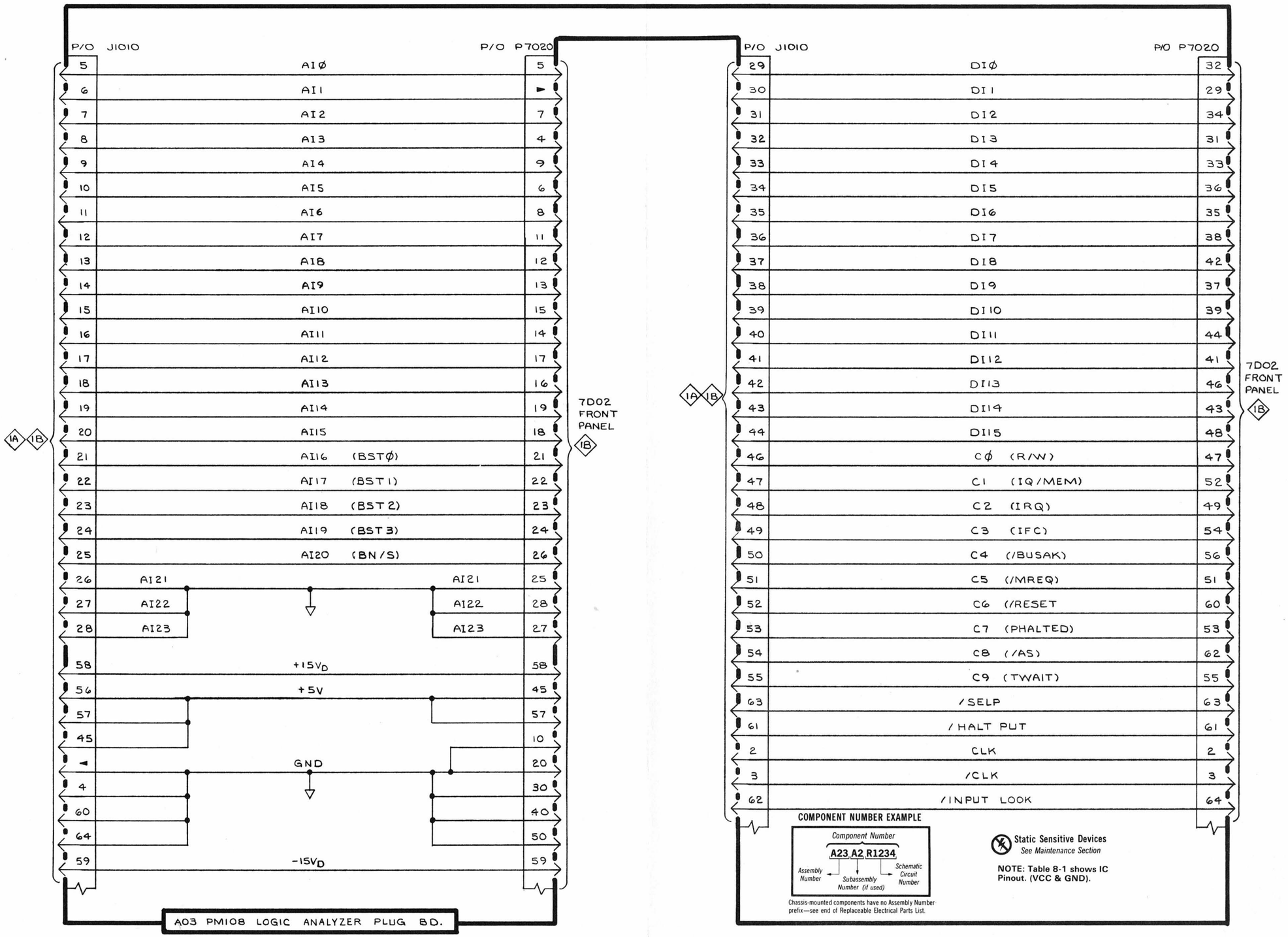

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PM108 SERIES INSTRUCTION

A03 PM108 LOGIC ANALYZER PLUG ◇3

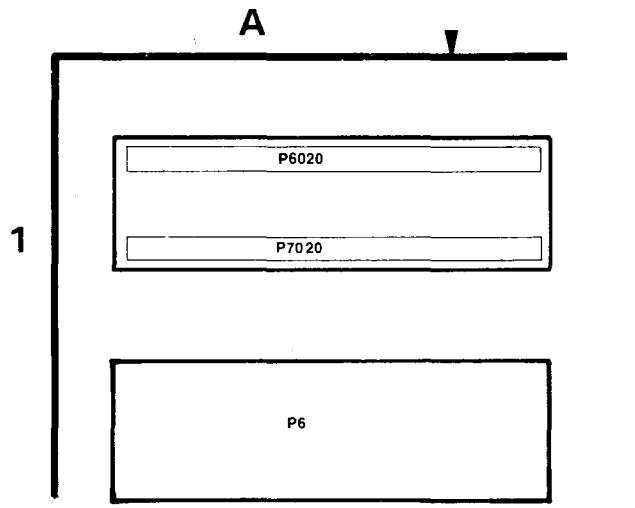
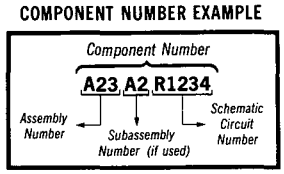


Figure 8-5. A4 Probe Board Component Locations.

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

```
1 2 3 4 5                    Name & Description
Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
  Detail Part of Assembly and/or Component
  Attaching parts for Detail Part
  - - - * - - -
    Parts of Detail Part
    Attaching parts for Parts of Detail Part
    - - - * - - -
```

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000AH	STANDARD PRESSED STEEL CO., UNBRAKO DIV.	8535 DICE ROAD	SANTA FE SPRINGS, CA 90670
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
19613	TEXTOOL PRODUCTS, INC.	1410 W PIONEER DRIVE	IRVING, TX 75061
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
23880	STANFORD APPLIED ENGINEERING, INC.	340 MARTIN AVE.	SANTA CLARA, CA 95050
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153

@

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	334-4066-00			1		PLATE,IDENT:MKD Z8002	80009	334-4066-00
-2	380-0593-01			1		HSG HALF,CKT BD:TOP	80009	380-0593-01
						(ATTACHING PARTS)		
-3	211-0093-00			4		SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
						- - - * - - -		
-4	380-0594-01			1		HSG HALF,CKT BD:BOTTOM	80009	380-0594-01
						(ATTACHING PARTS)		
-5	211-0093-00			4		SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
-6	210-0586-00			4		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	211-041800-00
						- - - * - - -		
-7	343-0836-00			4		CLAMP,CABLE:3.72 L,ALUM	80009	343-0836-00
-8	200-2415-00			1		DOOR,ACCESS:PLASTIC	80009	200-2415-00
	175-3330-00			1		CABLE ASSY,SP,ELEC:40,28 AWG,13.0 L,RIBBON	80009	175-3330-00
	200-2445-00			1		. COVER,PROBE:PIN PROTECTOR,PLASTIC	80009	200-2445-00
-9	386-3814-00			1		. PLATE,CONN BODY:	80009	386-3814-00
-10	352-0536-00			1		. HOLDER,CONTACT:40 PIN,NYLON	80009	352-0536-00
						(ATTACHING PARTS)		
-11	211-0102-00			2		. SCREW,MACHINE:4-40 X 0.500",FLH,STL	83385	OBD
						- - - * - - -		
-12	334-3754-00			1		. MARKER,IDENT:MKD P7020	80009	334-3754-00
-13	334-3753-00			1		. MARKER,IDENT:MKD	80009	334-3753-00
-14	----- -----			1		. CKT BOARD ASSY:**Z8002 PROBE(SEE A4 REPL)**		
-15	131-2093-00			2		. . SKT,PL-IN ELEK:MICROCKT,20 CONT,LOW PF	23880	CSA-3200-208
-16	200-2429-00			1		. . CABLE NIP,ELEC:CABLE,32/64 MALE	80009	200-2429-00
	131-2443-00			1		CONN,RCPT,ELEC:CABLE,32/64 MALE	80009	131-2443-00
-17	334-3722-00			1		. PLATE,IDENT:MKD P6460 MICROPROCESSOR PROBE	80009	334-3722-00
-18	380-0591-00			1		. HSG HALF,CKT BD:TOP	80009	380-0591-00
						(ATTACHING PARTS)		
-19	211-0225-00			2		. SCR,CAP,SOC HD:4-40 X 0.312 INCH,STL	000AH	OBD
-20	211-0093-00			2		. SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
-21	210-0551-00			4		. NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	83385	OBD
						- - - * - - -		
-22	380-0590-01			1		. HSG HALF,CKT BD:BOTTOM	80009	380-0590-01
-23	343-0836-00			2		. CLAMP,CABLE:3.72 LONG,ALUM	80009	343-0836-00
-24	200-2412-00			2		. CABLE NIP,ELEC:3.45 L X 0.05 ID,PLASTIC	80009	200-2412-00
	175-2683-00			1		. CA ASSY,SP,ELEC:64,28 AWG,48.0 L	80009	175-2683-00
-26	----- -----			1		. CKT BOARD ASSY:PROBE CONNECTOR(SEE A3 REPL)		
-27	131-0608-00			64		. . TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-28	361-0998-00			4		SPACER,CKT BD:0.245 ID X 0.38 OD X 0.23 H	80009	361-0998-00
-29	----- -----			1		CKT BOARD ASSY:PM108/8002/TOP(SEE A1 REPL)		
-30	131-0590-00			18		. CONTACT,ELEC:0.71 INCH LONG	22526	47351
-31	131-0993-00			1		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
	136-0537-00			1		. SOCKET,PLUG-IN:40 PIN,W/LOCKING LEVER	19613	240-0333-00-0602
-33	136-0578-00			1		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-34	136-0694-00			1		. SKT,PL-IN ELEK:MICROCIRCUIT,28 CONTACT	73803	CS9002-28
-35	131-0787-00			40		. CONTACT,ELEC:0.64 INCH LONG	22526	47359
-36	136-0252-07			10		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-37	131-0608-00			112		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-38	----- -----			1		CKT BOARD ASSY:PM108/8002/BOTTOM(SEE A2 REPL)		
-39	136-0263-04			18		. SOCKET,PIN TERM:FOR 0.025 INCH SQUARE PIN	22526	75377-001
-40	131-0993-00			2		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-41	131-0608-00			21		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-42	136-0623-00			1		. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
-43	337-2722-00			1		. SHIELD,ELEC:ACCESS DOOR	80009	337-2722-00

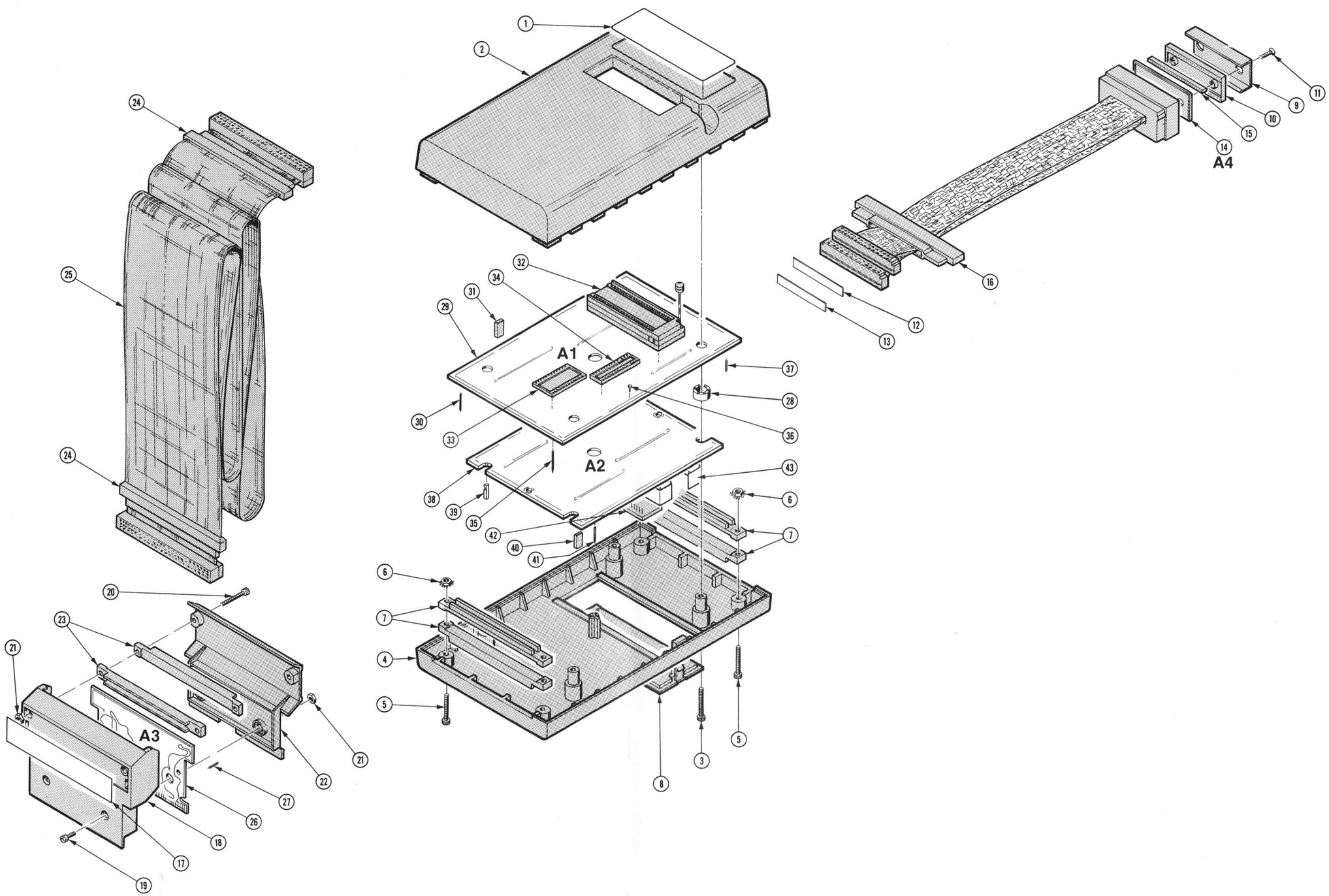


FIG. 1 EXPLODED

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
	070-3472-00			1		MANUAL,TECH:INSTRUCTION PM 108, PERSONALITY MODULE	80009	070-3472-00

PM 108 SIGNAL GLOSSARY

Introduction

The listings which follow describe each signal line within the PM 108 as it appears at each pin of every connector in the Personality Module. Some line titles appear more than once, and the active state and line definition may differ at one pin as compared to another because of the different purposes served by some signals at different locations within the Personality Module. For additional information, refer to Section 4, Theory of Operation.

PM 108 SIGNAL DESCRIPTION

Module Input Pin #	Signal Name	Description
J6020 - 1	ADØ	
" 17	AD1	
" 15	AD2	
" 13	AD3	
" 9	AD4	
" 11	AD5	**AD_0-AD_{15}.** *Address/Data* (inputs/outputs, active High, 3-state). These multiplexed address and data lines are used both for I/O and to address memory.
" 7	AD6	
" 5	AD7	
" 3	AD8	
J7020 - 1	AD9	
" 3	AD1Ø	
" 5	AD11	
" 7	AD12	
" 9	AD13	
" 17	AD14	
" 15	AD15	
J6020 - 23	/AS	**/AS.** *Address Strobe* (output, active Low, 3-state). The rising edge of /AS indicates addresses are valid. /AS occurs at the beginning of every machine cycle.
J7020 - 33	/DS	**/DS.** *Date Strobe* (output, active Low, 3-state. This line times the data in and out of the CPU. Indicates that data is valid.
J7020 - 25	/NMI	**/NMI.** *Non-Maskable Interrupt* (edge triggered, Input, active Low). A high-to-low transition on NMI requests a non-maskable interrupt. The NMI interrupt has the highest priority of the three types of interrupts.
J7020 - 23	/NVI	**/NVI.** *Non-Vectored Interrupt* (input, active Low). A low on this line requests a non-vectored interrupt.

PM 108 SIGNAL DESCRIPTION (cont)

Module Input Pin #	Signal Name	Description
J7020 - 21	/VI	**/VI.** *Vectored Interrupt* (input, active Low). A Low on this line requests a vectored interrupt.
J7020 - 31	/MREQ	**/MREQ.** *Memory Request* (output, active Low, 3-state). A Low on this line indicates that the address/data bus hold a memory address.
J6020 - 39 J7020 - 39 J7020 - 37 J7020 - 35	STØ ST1 ST2 ST3	**ST_0-ST_3.** *Status* (outputs, active High, 3-state). These lines specify the CPU status (see table). **ST_3-ST_0 Definition** 0 0 0 0 Internal operation 0 0 0 1 Memory refresh 0 0 1 0 I/O reference 0 0 1 1 Special I/O reference 0 1 0 0 Segment trap acknowledge 0 1 0 1 Non-maskable interrupt acknowledge 0 1 1 0 Non-vectored interrupt acknowledge 0 1 1 1 Vectored interrupt acknowledge 1 0 0 0 Data memory request 1 0 0 1 Stack memory request 1 0 1 0 Data memory request (EPU) 1 0 1 1 Stack memory request (EPU) 1 1 0 0 Instruction space access 1 1 0 1 Instruction fetch, first word 1 1 1 0 EPU Transfer 1 1 1 1 Reserved
J7020 - 27	/RESET	**/RESET.** *Reset* (input, active Low). A Low on this line resets the CPU.
J6020 - 31	R/W	**R/W.** *Read/Write* (output, Low = Write, 3-state). R/W indicates that the CPU is reading from or writing to memory or I/O.
J6020 - 33	/BUSAK	**/BUSAK.** *Bus Acknowledge* (output, active Low). A Low on this line indicates the CPU has reliquished control of the bus.
J6020 - 37	/BUSRQ	**/BUSRQ.** *Bus Request* (input, active Low). This line must be driven Low to request the bus from the CPU. (Not used by PM 108)
J6020 - 27	B/W	**B/W.** *Byte/Word* (output, Low = Word, 3-state). This signal defines the type of memory reference on the 16-bit address/data bus. (Not used by PM 108)
J6020 - 29	N/S	**N/S.** *Normal/System Mode* (output, Low = System Mode, 3-state). N/S indicates the CPU is in the normal or system mode. (Not used by PM 108)

PM 108 SIGNAL DESCRIPTION (cont)

Module Input Pin #	Signal Name	Description
J6020 - 28	DCPLE	**Decouple.** Output from on-chip negative substrate-bias generator. Presently not connected. (Not used by PM 108)
J7020 - 13 J7020 - 29	/MI /MO	**M_i, M_o.** *Multi-Micro In, Multi-Micro Out* (input and output, active Low). These two lines form a resource-request daisy chain that allows one CPU in a multi-microprocessor system to access a shared resource. (Not used by PM 108)
J6020 - 35	/WAIT	**/WAIT.** *Wait* (input, active Low). This line indicates to the CPU that the memory or I/O device is not ready for data transfer. When this signal is asserted the PM 108 will generate /TWAIT to the 7D02.
J7020 - 11	/STOP	**/STOP.** *Stop* (input, active Low). This input can be used to single-step instruction execution. The PM 108 monitors this line and will display "Z8002 HALTED" when asserted and the 7D02 is running. It also is "ORED" with a "STOP PUT" signal from the 7D02 to enable the user program to halt the Z8002 Processor on conditions.
J6020 - 21	CLK	**CLK.** *System Clock* (input). CLK is a 5 V single-phase time-base input. CLK is monitored by the PM 108, converted to ECL and sent to the 7D02.

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

SERVICE NOTE

Because of the universal parts procurement problem, some electrical parts in your instrument may be different from those described in the Replaceable Electrical Parts List. The parts used will in no way alter or compromise the performance or reliability of this instrument. They are installed when necessary to ensure prompt delivery to the customer. Order replacement parts from the Replaceable Electrical Parts List.

CALIBRATION TEST EQUIPMENT REPLACEMENT

Calibration Test Equipment Chart

This chart compares TM 500 product performance to that of older Tektronix equipment. Only those characteristics where significant specification differences occur, are listed. In some cases the new instrument may not be a total functional replacement. Additional support instrumentation may be needed or a change in calibration procedure may be necessary.

Comparison of Main Characteristics

DM 501 replaces 7D13		
PG 501 replaces 107	PG 501 - Risetime less than 3.5 ns into 50 Ω.	107 - Risetime less than 3.0 ns into 50 Ω.
108	PG 501 - 5 V output pulse; 3.5 ns Risetime	108 - 10 V output pulse 1 ns Risetime
PG 502 replaces 107		
108	PG 502 - 5 V output	108 - 10 V output
111	PG 502 - Risetime less than 1 ns; 10 ns Pretrigger pulse delay	111 - Risetime 0.5 ns; 30 to 250 ns Pretrigger pulse delay
PG 508 replaces 114	Performance of replacement equipment is the same or better than equipment being replaced.	
115		
2101		
PG 506 replaces 106	PG 506 - Positive-going trigger output signal at least 1 V; High Amplitude output, 60 V.	106 - Positive and Negative-going trigger output signal, 50 ns and 1 V; High Amplitude output, 100 V.
067-0502-01	PG 506 - Does not have chopped feature.	0502-01 - Comparator output can be alternately chopped to a reference voltage.
SG 503 replaces 190, 190A, 190B	SG 503 - Amplitude range 5 mV to 5.5 V p-p.	190B - Amplitude range 40 mV to 10 V p-p.
191		
067-0532-01	SG 503 - Frequency range 250 kHz to 250 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
SG 504 replaces 067-0532-01	SG 504 - Frequency range 245 MHz to 1050 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
067-0650-00		
TG 501 replaces 180, 180A	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	180A - Trigger pulses 1, 10, 100 Hz; 1, 10, and 100 kHz. Multiple time-marks can be generated simultaneously.
181		181 - Multiple time-marks
184	TG 501 - Trigger output-slaved to market output from 5 sec through 100 ns. One time-mark can be generated at a time.	184 - Separate trigger pulses of 1 and 0.1 sec; 10, 1, and 0.1 ms; 10 and 1 μs.
2901	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	2901 - Separate trigger pulses, from 5 sec to 0.1 μs. Multiple time-marks can be generated simultaneously.

NOTE: All TM 500 generator outputs are short-proof. All TM 500 plug-in instruments require TM 500-Series Power Module.

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MANUAL CHANGE INFORMATION

Date: 6-8-81 Change Reference: M43586

Product: PM 108 Personality Module for Z8002 Manual Part No.: 070-3472-00

DESCRIPTION

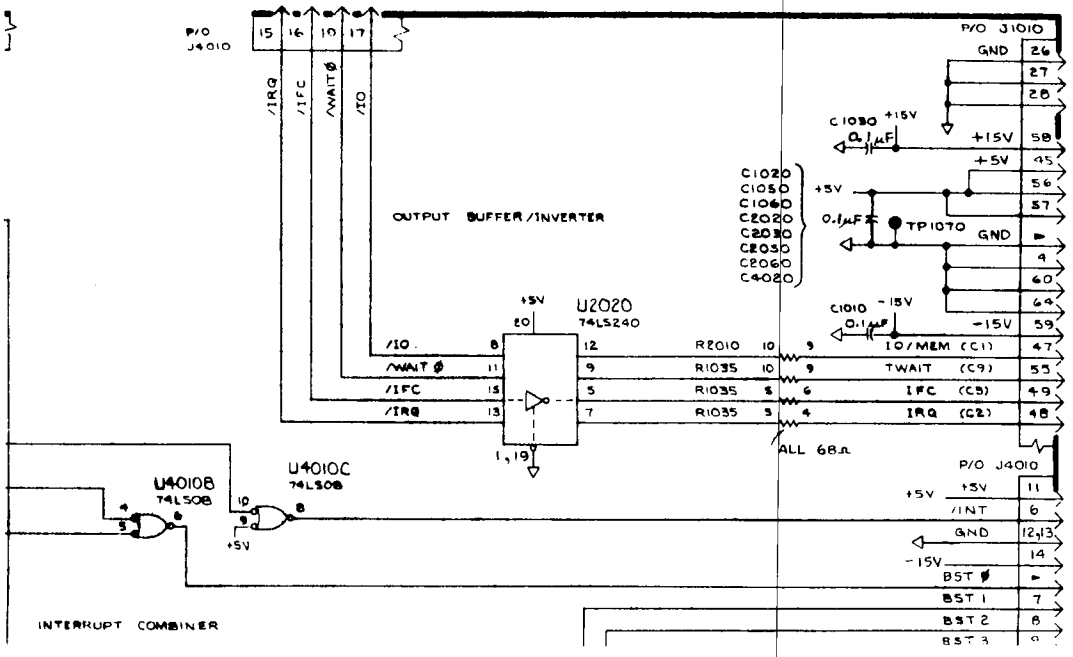
EFF SN B010100

REPLACEABLE ELECTRICAL PARTS LIST AND SCHEMATIC CHANGES

CHANGE TO:

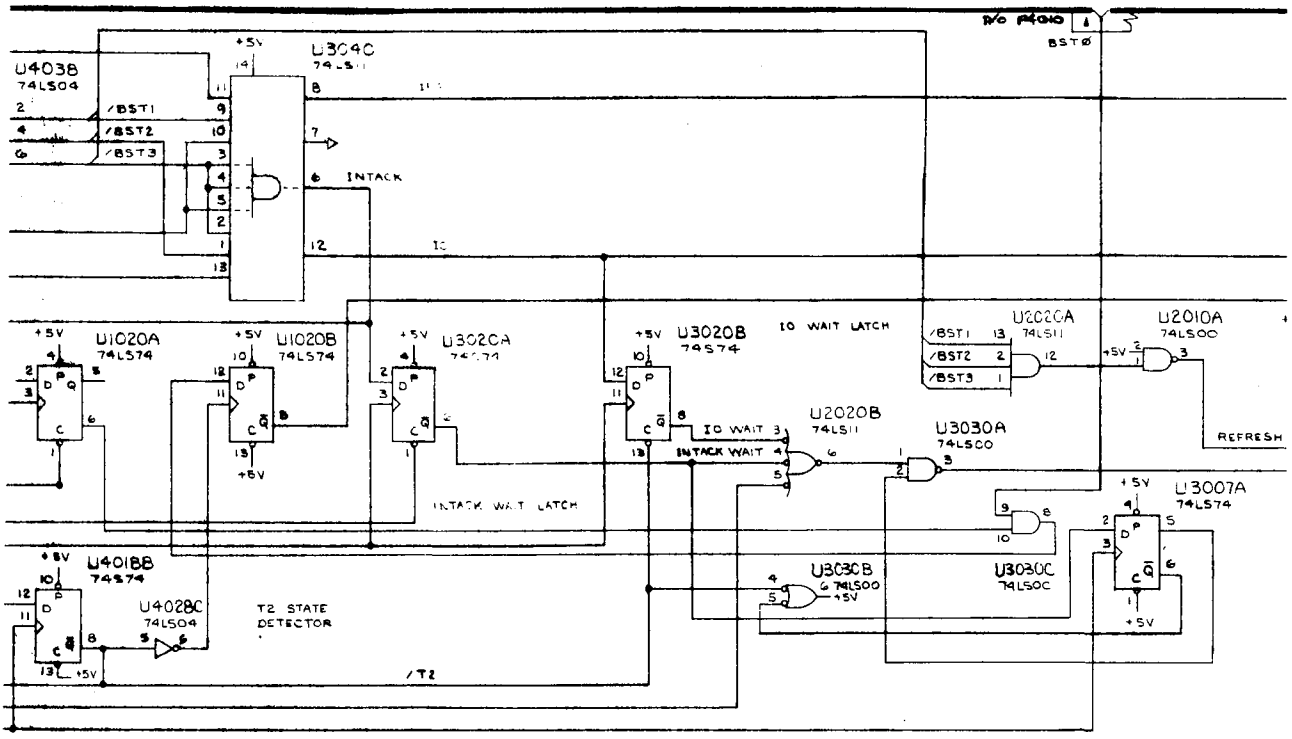
A1	670-6896-01	CKT BOARD ASSY:PM 108/8002/TOP
A2	670-6897-01	CKT BOARD ASSY:PM 108/8002/BOTTOM
A1U2040	160-1023-02	MICROCIRCUIT,DI:4096 X 8 EPROM,PRGM,HI INT
A1U3040	160-1086-02	MICROCITCUIT,DI:4096 X 8 EPROM,PRGM

Partical DIAGRAM 1B



DESCRIPTION

Partical DIAGRAM 2



Tektronix®
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MANUAL CHANGE INFORMATION

Date: 9-22-81 Change Reference: C2/981

Product: PM 108 PERSONALITY MODULE FOR Z8002 Manual Part No.: 070-3472-00

DESCRIPTION

TEXT CHANGES

SECTION 3 SPECIFICATIONS

Table 3-2 page 3-5

Propagation Delays	SUPPLEMENTAL INFORMATION
through Personality Module	
Control Channel Delays	20 ns min., 35 ns max.
C0, C1, C3, C4, C5,	
C6 and C8	

CHANGE TO:

Control Channel Delays	
C0, C4, C5, C6, & C8	20 ns min., 35 ns max.
C1, C3	50 ns min., 85 ns max.

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MANUAL CHANGE INFORMATION

Date: 1-22-81 Change Reference: C1/181

Product: PM 108 INSTRUCTION MANUAL Manual Part No.: 070-3472-00

DESCRIPTION

PAGE	CHANGE
4-4	Paragraph 13, line 7, "drives A2U1040 producing AD8-AD15. AD8-AD15 are" to "drives A2U1040 producing AD8-AD15. AD12-AD15 are".
4-4	Paragraph 13, line 11, "example: ADDR=FF02, DATA=0002." to "example: ADDR=F002, DATA=0002."
4-5	Paragraph 2, lines 3-4, "produces an interrupt when the data changes from 7FFF to 8000." to "produces an interrupt when the data changes from 70FF to 8F00."
6-15	The fourth figure from the top, line 8, "7F02 ADDB RH2, RH0." to "7F02 LP R15, EPU 2, #4."
6-16	The square with the text "This is a failure of the personality module to generate the state DATA: 0000, ADDRESS: FF00..." Change "FF00" to "F000".
6-19	Change the OPERATION column as follows: 70FC SPL I/O R 70FD I/O R 70FE REFRESH R 70FF INT OPR R 8F00 ------- W 8F01 EPU XFR W --LD R15, EPU 2, #4----- 8F03 FETCH N 8F04 EPU STK W 8F05 EPU DAT W 8F06 STK MEM W 8F07 DAT MEM W 8F08 VI ACK W 8F09 NMI ACK W 8F0A NMI ACK W 8F0B ------- W 8F0C SPL I/O W 8F0D I/O W 8F0E REFRESH W

PAGE	CHANGE
6-9	Column 2, first paragraph, the last sentence "Figure 6-7 illustrates timing relationships and data . . ." Replace with "Figure 6-5 illustrates timing relationships and data . . ."
6-9	Column 2, beginning with the paragraph with the heading "PM 108 Signature Tables" replace all information from that point through page 6-13 with the following information:

Use a Sony/Tektronix 308 Signature Analyzer with a P6451 Probe, and a P6107 signature/signal data input probe. Connect PM 108 to 7D02, with power off.

Disassemble and lay out the personality module boards as described in Fig. 6-1B. Set A2J1065 to the TEST position, and A2J1067 to the RUN position. Connect the microprocessor plug into the Self Test Socket A2J2065. Connect the P6451 probe clock lead to A2TP2020, and the ground lead to pin 1 of A2J3070. Connect the Start lead to pin 2, and the Stop lead to pin 3. Connect the ground lead of signature/signal data input probe to TP2007. Power up the 7D02, and enter a program that triggers on ADDRESS=0000, DATA=0000. Press the START/STOP button on the 7D02.

The 7D02 should indicate RUNNING, and not trigger on any data.

Set the Sony/Tektronix 308 to "Signature" with the following:

Clock↓
START↓
STOP ↑

Touch the signature/signal data input probe tip to each pin in the following tables and verify that the signature for each pin matches the one in the table.

NOTE
Table entries with "----" indicate a normal FAULT caused by "floating" on unused signal lines. The buffer A1U2040 and A1U3040 are examples. The data output lines are floating lines.

Pin	Signature	Pin	Signature	Pin	Signature	Pin	Signature
A1J5020		A1U4010		A1U2030		A1U3030	
1	17HP	1	PACU	1	0000	1	0000
2	2P3A	2	PACU	2	----	2	U293
3	5797	3	PACU	3	76F0	3	PACU
4	2PFA	4	PACU	4	P04F	4	616A
5	U686	5	PACU	5	PACU	5	0000
6	PACU	6	PACU	6	F5F0	6	PACU
7	0000	7	0000	7	580A	7	U9A6
8	9F7U	8	0000	8	F5F0	8	A480
9	2A38	9	PACU	9	0000	9	1A21
10	PACU	10	0000	10	0000	10	0000
11	PACU	11	PACU	11	0000	11	1A21
12	PACU	12	----	12	F5F0	12	A480
13	0000	13	----	13	580A	13	U9A6
14	F5F0	14	PACU	14	F5F0	14	PACU
15	0000			15	----	15	0000

16	F5F0
17	76F0
18	1A21
19	U293
20	U9A6
21	616A
22	0000
23	----
24	580A
25	P04F
26	0000
27	5FU8
28	0000
29	A480
30	PACU
31	0000
32	1319
33	182F
34	U09P
35	F5F0
36	P04F
37	A8P1
38	U97H
39	F303
40	8CH5

A1U2020

1	0000
2	----
3	PACU
4	PACU
5	69F7
6	C2C5
7	96P0
8	----
9	PACU
10	0000
11	0000
12	----
13	7F5U
14	58DA
15	8378
16	0000
17	0000
18	0000
19	0000
20	PACU

16	P04F
17	76F0
18	PACU
19	0000
20	PACU

A1U3020

1	PACU
2	----
3	8CH5
4	----
5	1319
6	----
7	182F
8	----
9	U09P
10	0000
11	P04F
12	----
13	F5F0
14	----
15	A851
16	----
17	497H
18	----
19	PACU
20	PACU

16	616A
17	PACU
18	U293
19	0000
20	PACU

A1U2050

1	0000
2	A8P1
3	1319
4	P04F
5	U09P
6	182F
7	F5F0
8	8CH5
9	U97H
10	0000
11	U97H
12	8CH5
13	F5F0
14	182F
15	U09P
16	P04F
17	1319
18	A8P1
19	0000
20	PACU

TP 4062	PACU
TP 4060	0000
P3020	
pin 1	C2C5 } jumper
pin 2	C2C5 }
pin 3	PACU

Pin	Signature
A1U2060	
1	0000
2	F5PA
3	8CH5
4	1319
5	898F
6	8F16
7	182F
8	U09P
9	784U
10	0000
11	A480
12	7026
13	P04F
14	F5F0
15	P2P0
16	5470
17	A8P1
18	U97H
19	7FCP
20	PACU

Pin	Signature
A1U3050	
1	0000
2	2A38
3	940U
4	2PFA
5	5797
6	2P3A
7	U686
8	F303
9	9F7U
10	0000
11	9F7U
12	----
13	U686
14	2P3A
15	5797
16	2PFA
17	940U
18	2A38
19	0000
20	PACU

Pin	Signature
A1U3060	
1	0000
2	7P61
3	----
4	940U
5	940U
6	2P3A
7	2P3A
8	5797
9	5797
10	0000
11	A480
12	C2C5
13	2PFA
14	U686
15	6AU9
16	C647
17	2A38
18	9F7U
19	0000
20	PACU

Pin	Signature
A1U2040	
1	7FCP
2	5470
3	P2P0
4	7026
5	784U
6	8F16
7	898F
8	F5PA
9	----
10	----
11	----
12	0000
13	----
14	----
15	----
16	----
17	----
18	580A
19	2P3A
20	PACU
21	5797
22	940U
23	7P61
24	PACU

Pin	Signature
A1U3040	
1	0000
2	C2C5
3	7FCP
4	5470
5	P2P0
6	7026
7	784U
8	8F16
9	898F
10	F5PA
11	----
12	----
13	----
14	0000
15	----
16	----
17	----
18	----
19	----
20	C2C5
21	2P3A
22	PACU
23	5797
24	940U
25	7P61
26	PACU
27	PACU
28	PACU

A2U1010

Pin	Signature
1	PACU
2	PACU
3	PACU
4	PACU
5	PACU
6	PACU
7	9F7U
8	A480
9	0000
10	PACU
11	0000
12	9F7U
13	76F0
14	A480

A2U1020

Pin	Signature
1	AHAU
2	PACU
3	PACU
4	PACU
5	0900
6	P3CU
7	0000
8	7F5U
9	96P0
10	PACU
11	9F7U
12	0900
13	AHAU
14	PACU

A2U4018

Pin	Signature
1	76F0
2	PACU
3	A480
4	PACU
5	38UU
6	H240
7	0000
8	76F0
9	9F7U
10	PACU
11	0000
12	38UU
13	PACU
14	PACU

A2U2010

Pin	Signature
1	U35A
2	616A
3	UCFC
4	0000
5	PACU
6	PACU
7	0000
8	76F0
9	9F7U
10	9F7U
11	PACU
12	PACU
13	PACU
14	PACU

A2U2020

Pin	Signature
1	U09P
2	182F
3	H370
4	649P
5	PACU
6	5H51
7	0000
8	0000
9	UCFC
10	0000
11	C7PP
12	U35A
13	1319
14	PACU

A2U4028

Pin	Signature
1	0000
2	PACU
3	76F0
4	9F7U
5	76F0
6	9F7U
7	0000
8	0000
9	0000
10	0000
11	PACU
12	0000
13	0000
14	PACU

A2U3007

Pin	Signature
1	PACU
2	H370
3	0000
4	PACU
5	7658
6	9FP7
7	0000
8	0000
9	PACU
10	PACU
11	PACU
12	0000
13	PACU
14	PACU

A2U3020

Pin	Signature
1	76F0
2	H573
3	A480
4	PACU
5	8P21
6	649P
7	0000
8	H370
9	39FU
10	PACU
11	A480
12	H6C7
13	76F0
14	PACU

A2U4038

Pin	Signature
1	U9A6
2	1319
3	U293
4	182F
5	1A21
6	U09P
7	0000
8	8378
9	69F7
10	PACU
11	0000
12	----
13	H6C7
14	PACU

A2U1030

Pin	Signature
1	A480
2	0000
3	8CH5
4	1319
5	182F
6	U09P
7	0000
8	U97H
9	A8P1
10	F5F0
11	P04F
12	0000
13	U09P
14	PACU

A2U1040

Pin	Signature
1	29CF
2	PACU
3	F303
4	UH61
5	PACU
6	17HP
7	0000
8	2P3A
9	890C
10	PACU
11	5797
12	924P
13	PACU
14	PACU

A2U3085

Pin	Signature
1	PACU
2	8CH5
3	616A
4	PACU
5	1319
6	U9A6
7	0000
8	U293
9	PACU
10	182F
11	1A21
12	PACU
13	U09P
14	PACU

A2U2030

1	U97H
2	0000
3	29CF
4	UH61
5	890C
6	924P
7	0000
8	PACU
9	5FU8
10	8046
11	580A
12	0000
13	924P
14	PACU

A2U2040

1	580A
2	76F0
3	2PFA
4	8046
5	76F0
6	U686
7	0000
8	2A38
9	5FU8
10	76F0
11	9F7U
12	PACU
13	76F0
14	PACU

TP	Signature
A2TP1028	A480
A2TP2020	PACU
A2TP2048	76F0
A2TP2007	0000

A2U3030

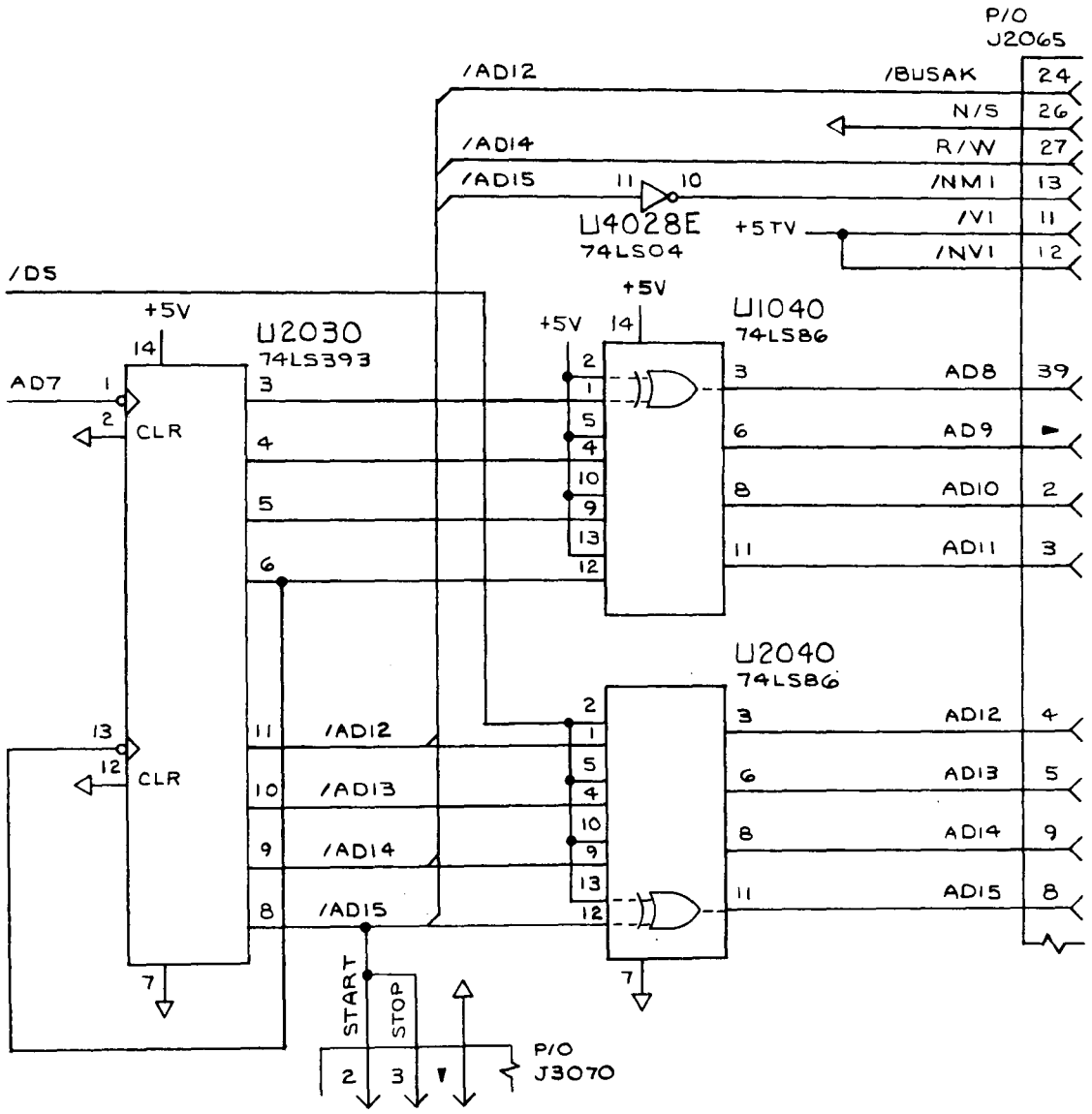
1	5H51
2	PACU
3	C7PP
4	76F0
5	9FP7
6	PACU
7	0000
8	H370
9	C7PP
10	649P
11	AHAU
12	H573
13	9F7U
14	PACU

A2U3040

1	182F
2	U09P
3	U09P
4	U09P
5	U293
6	H573
7	0000
8	69F7
9	1319
10	U293
11	1A21
12	H6C7
13	U9A6
14	PACU

PAGE	CHANGE
7-3	The second part number from the bottom of the page, number A1U2040, should have a Tektronix Part No. of 160-1023-01. The Mfr Part Number should also be 160-1023-01.
7-4	The fourth part number from the top, number A1U3040, should have A Tektronix Part No. and Mfr Part Number of 160-1086-01.
7-5	The ninth part number from the bottom, number A2U3020, should have a Tektronix Part No. 156-0331-01, and a Mfr Part Number of 74S74.
7-5	The fifth part number from the bottom, number A2U4018, should have a Tektronix Part No. of 156-0331-01, and a Mfr Part Number of 74S74.

A2 Lower Board Schematic -- Change the lower right-hand corner of the schematic to match the following illustration:



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MANUAL CHANGE INFORMATION

Date: 7-15-83 Change Reference: M50150 REV.

Product: PM 108 PERSONALITY MODULE Manual Part No.: 070-3472-00

DESCRIPTION

SN B020000 & UP

DIAGRAM AND PARTS LIST ADDITIONS

SECTION 7 REPLACEABLE ELCTRICAL PARTS

670-6897-01, A2U4018, and A2R2028

CHANGE TO:

670-6897-02		
A2U4018	136-0728-00	MICROCIRCUIT,SKT.
A2R2028	315-0271-00	RES,270 OHM

ADD:

670-8230-00	WAIT FUNCTION CKT BD. ASSY	
A2U2000	156-0331-03	MICROCIRCUIT,74S74
A2U2100	156-1059-01	MICROCIRCUIT,74LS109
A2U2300	156-0467-02	MICROCIRCUIT,74LS38
A2C2300	281-0775-00	CAP,1 UF
A2R2000	315-0271-00	RES,270 OHM,.25W,5%
A2R2100	315-0271-00	RES,270 OHM,.25W,5%

000-2775-00D

DESCRIPTION

SECTION 8 DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

ADD:

partial schematic
of bottom board.

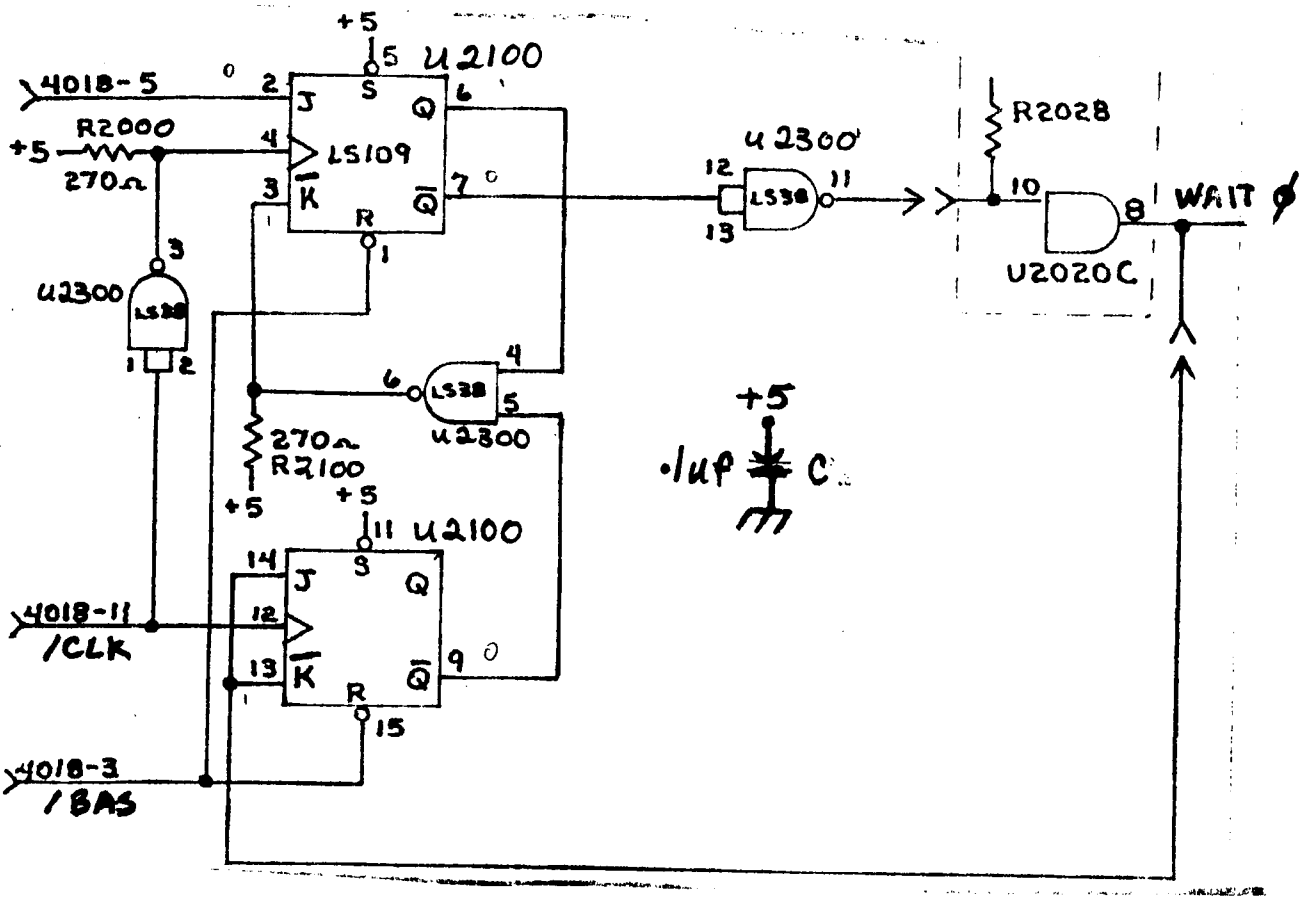

Diagram for 670-8230-00 WAIT FUNCTION CKT BD.