DESCRIPTION

The H710 is designed for use with the M177 in a parallel-serial system. It is also possible to construct a 10-Bit DAC using two H710's. The hybrid contains Nichrome resistors with a sheet resistance of 50 Ω/sq. R_R sets the reference current and is trimmed to 480 Ω/Sq. R_A is a pull-up load resistor trimmed to be 0.25 R_R. Binarily-scaled emitter resistors are functionally trimmed to set-up precision current sources. These are trimmed while measuring the output current at Pin #5. Two unswitched current sources approximately equal to ILSB are provided. One is connected to the output, the other is available as an open collector. The emitters of these two current sources are brought out so that they can be adjusted or disabled.

The part is designed to operate with a reference of +3.072 volts or ± 1.536 volts. Full scale output current is then 25.6 mA. A -5.2 volt digital supply is needed to set-up the reference current. Digital inputs are ECL compatible and sink 1 mA each.

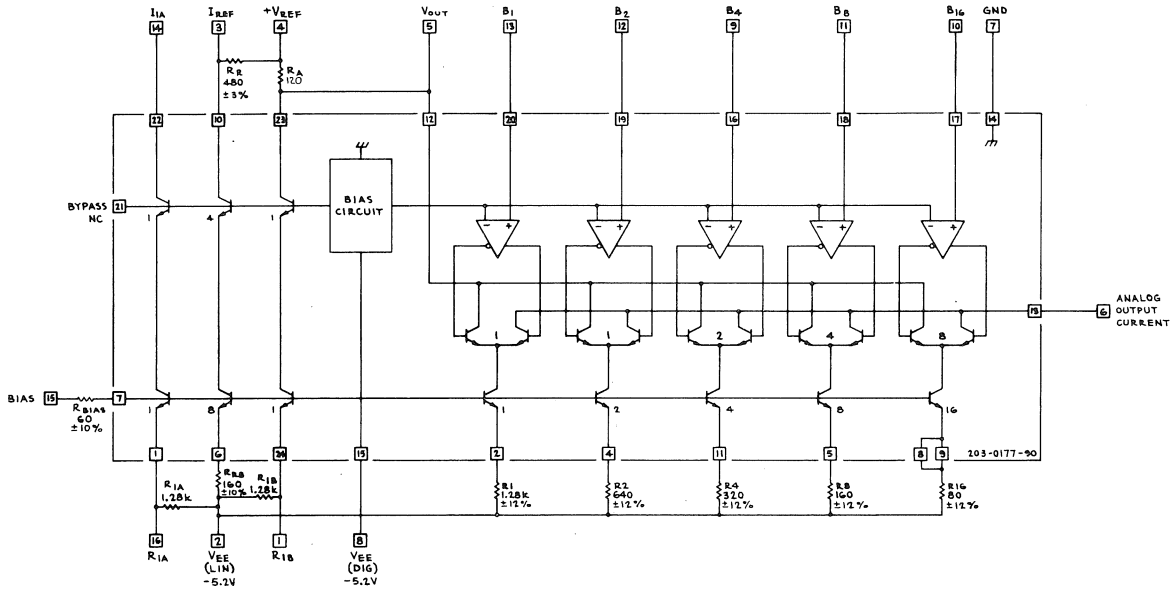
The H710 is tested to have linearity between ± 0.05% (± 1/2 LSB at 10 bits). More specifically, the four LSB currents ratio binarily to the MSB current within ± 0.05% of full scale where full scale is defined to be twice the MSB current. Differential non-linearity is also tested so that each 1-bit transition causes an output change of 1/32 of full scale ± 0.05% full scale. A final check of overall linearity is made by testing that the sum of the absolute values of each bit current error is less than 0.1% of full scale. This guarantees an overall non-linearity of less than ± 0.05%.

The trimming and testing of the hybrid is done with the output at a constant potential in order to minimize non-linearity due to variable DAC output conductance. Theory and some testing indicate than an output compliance of 3 volts will affect linearity in a "smooth" fashion by less than 0.05% of full scale.

Settling time to ± 1/2 LSB with 10 pF load capacitance is typically 15 nS for 8-bits.

Refer to 203-0177-90 M177

PROCESS	Thin-Film
POWER SUPPLY.	
PACKAGE	TO-8
DESIGNER	Bob Nordstrom
INSTRUMENT USAGE	ADC 820



NOTES:

1. R_R IS TRIMMED SO THAT V(PIN 10) = −750mV ± 50mV.
2. R_A IS TRIMMED TO RATIO TO R_R.
3. R_{1A}, R_{1B}, R8 AND R16 ARE TRIMMED SO THAT THEIR RESPECTIVE OUTPUT CURRENTS SCALE APPROXIMATELY TO THE REFERENCE CURRENT.
4. R1, R2 AND R4 ARE TRIMMED SO THAT THEIR RESPECTIVE OUTPUT CURRENTS SCALE ACCURATELY TO THE CURRENT THROUGH R8.
5. FOR RATIO AND SCALING TOLERANCE SEE LASER TRIM SPECIFICATION.

ENGR	[signature]	4-29-77	PROCESS
DWN BY	Ron Hankins	4-21-77	PACKAGE 16 PIN TO-8 LG.
CHK BY	[signature]	5-26-77	SUB SIZE .3" X .3"
TYPE	HYBRID	5 BIT D/A CONVERTER	H710
INTEGRATED CIRCUIT ENG/MFG. TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0167-01	

OUTLINE DRAWING NOT AVAILABLE AT THIS TIME