PULSE INSTRUMENTS COMPANY

USER'S REFERENCE MANUAL

MODEL PI-458

PROGRAMMABLE PULSE DRIVER

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SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

The PI-458 Programmable Pulse Driver is a plug-in unit designed to operate in Tektronix TM-500 Series Power Modules. It is compatible with other plug-in units manufactured by Pulse Instruments Company, and with Tektronix TM-500 Series plug-in units, operating in standard (not custom-wired) Power Modules.

The PI-458 is a programmable level shifter which may also be used as a triggered pulse generator. As a level shifter, it converts a TTL-level input signal into a high-power, 50-ohm signal having other upper and lower voltage levels such as those used with MOS nd MOS/CCD devices. Output high and low levels are independently adjustable from +20V to -10V and from -20V to +10V, respectively, either manually or under external voltage control or, if the unit includes Option-002, by digital programming.

A voltage-programming feature provides overvoltage protection when testing CMOS devices, using the Vcc supply to limit and track the output amplitude.

The digital programming feature included in the PI-458-002 permits interfacing the unit, through a suitable controller, in a computer-centered automatic testing system. The digital interface and programming principles are described in Section 5 of this manual. Refer also to the PI document Digital Programming for PI-Series Plug-in Instruments, which contains information pertinent to special TM-506 wiring and rear panel connectors.

Other valuable features of the PI-458 include manually variable pulse delay, output pulse width, and output inversion.

The compact and versatile PI-458 can be used in a wide range of applications: Applications including device characterization in the development laboratory and automatic production testing.

COMPATIBILITY REQUIREMENTS

The PI-458, or the PI-458-002/003, may be installed in any standard Tektronix TM-500 Series Power Module, if use of the digital programming feature, or the rear input/output feature, is not required. To use the digital programming capabilities or the rear input/output feature of the PI-458-002/003, however the unit must be installed in a TM-506 Power Module containing Tektronix Option 02, which has also been modified by Pulse Instruments Company to provide required additional wiring and connectors (designated MOD-DP, or designated MOD-451, MOD-451A, MOD-454, or MOD-454A in earlier units).

PERFORMANCE SPECIFICATIONS

Table 1-1 gives the principal performance capabilities and input requirements of the basic PI-458 Programmable Pulse Driver; that is, the unit not including the Digital Programming feature (Option -002). All measurements should by made using 3-foot length, low loss 50-ohm coaxial cables.

Performance specifications and input requirements for the Model PI-458-002 (which includes the Digital Programming feature) are given in Section 5 of this manual.

Table 1-1. Performance Specifications, Basic PI-458

Specification	Characterisitcs
OUTPUT HIGH LEVEL	+20V to -10V into 1 Meg ohm; +10V to -5V into 50 ohms. Full range controlled either manually, or by external voltage program. Control selected with front panel switch.
Manual	Continuously variable over full range by front panel control.
Voltage Program	Continuously variable over full range with input through front panel jack. Offset voltage with 1 Meg ohm is <75mV.
OUTPUT LOW LEVEL	-20V to +10V into 1 Meg ohm; -10V to +5V into 50 ohms. Full range controlled either manually, or by external voltage program. Control selected with front panel switch.
Manual	Continuously variable over full range by front panel control.
Voltage Program	Continuously variable over full range with input through front panel jack. Offset voltage with 1 Meg ohm is <75mV.
OUTPUT AMPLITUDE	1V minimum to 25V maximum into 1 Meg ohm. Minimum 0.5V to 12.5V maximum into 50 ohms.

Table 1-1. Performance Specifications, Basic PI-458 (cont'd)

Specifications	Characteristics
OUTPUT RISE AND FALL TIMES	<5ns for output amplitude <10V into 50 ohms <6ns for output amplitude <20V into 1 megohm // 15pf.
MAX OUTPUT REPETITION RATES	>50MHz for output amplitude <10V into 50 ohms. >40MHz for output amplitude <20V into 1 megohm // 15pf.
OUTPUT SETTLING TIME	Approx 750 usec to 0.1% of full scale.
OUTPUT ABERRATIONS	5% plus 350mV peak-to-peak with output amplitude >3V, driving a 3-foot-long, 50-ohm cable terminated with 15pf in parallel with 1 megohm.
OUTPUT POLARITY	Either normal or inverted, selected with front panel switch.
OUTPUT PULSE DELAY	10 nsec max with respect to trigger output, or adjustable from <10 nsec to >10 msec in 6-decade steps, plus continuously adjustable (10:1) control. Pulse of at least 2.5V, 10-nsec duration is required to trigger delay circuit. Delay jitter <0.1% of setting +200ps.
OUTPUT PULSE WIDTH	Determined by input, or adjustable from <10 nsec to >10 msec in 6-decade steps plus continuously adjustable (10:1) control. Pulse of at least 2.5V, 10-nsec duration is required to trigger pulse width circuit. Width jitter <0.1% of setting +200ps.
TRIGGER OUTPUT	TTL-compatible. Propagation delay from input is 40nsec max. Output pulse width determined by input.
TTL INPUT SIGNAL	2.5V to 5V into 1000 ohms, through front panel BNC connector.
VOLTAGE PROGRAM INPUTS HIGH LEVEL	+20V max to -10V min across 100k ohms.
LOW LEVEL	-20V min to +10V max across 100k ohms.

INPUT AND OUTPUT SIGNALS

Table 1-2 lists and defines input and output signals and their interconnections on the basic PI-458, including the rear input/output option.

For digital signal interconnections to and from the Model PI-458-002 (having the digital programming feature), refer to Section 5 of this manual.

Table 1-2. Input and Output Signals, Basic PI-458 (including Rear I/O Option -003)

Signal	Connector
TTL (clock) input	Front panel BNC TTL INPUT connector, and rear edge connector finger 27A, connected as ORed inputs.
Driver output	Front panel BNC DRIVER OUTPUT connector, and rear edge connector finger 24A. In units with Option -002 or -003, front panel push button switch connects output to either front panel connector only, or to the rear.
Trigger output (buffered input)	Front panel BNC TRIGGER OUTPUT connector.
Monitoring points for selected high and low levels	Banana jacks present selected high and low level reference voltages at front panel except when MODE switch selects voltage program mode.
Analog (voltage) program inputs (high and low levels)	Banana jacks accept externally generated voltage program levels when MODE switch selects voltage program mode.
Ground connections	Front panel banana jack marked with schematic Ground symbol. Rear edge connector fingers 26A (input return), and 23A (output return).

OPERATING CONTROLS AND INDICATORS

Table 1-3 lists and describes operating controls and indicators on the front panel of the instrument.

Table 1-3. Operating Controls and Indicators

Control/Indicator	Description
HIGH LEVEL/LOW LEVEL controls	
LOW LEVEL potentiometer	Inner knob of concentric LOW LEVEL/ HIGH LEVEL controls. Controls output low level in Manual mode of operation. Note that output low level must be set to a value more negative than that of high level. If set more positive, no output will appear.
HIGH LEVEL potentiometer	Outer knob of concentric LOW LEVEL/ HIGH LEVEL controls. Controls output high level in Manual mode of operation. Note that output high level must be set to a value more positive than that of low level. If set more negative, no output will appear.
INVERT/NORM switch	A push-push switch which causes inversion of pulse output. Output is normal when switch has been pressed towards the front panel, inverted when switch is out from the front panel.
MODE switch	Selects source of level control input, as follows: MAN -- manual controls DIGITAL PROGRAM -- digital signal interface (Option -002 only) Vprogram -- External voltages (analog program). The three switch positions within the Vprogram area permit selecting control inputs for either low (LO), or high (HI) level; or both (HI & LO). When

Control/Indicator	Description
Vprogram (cont'd)	the switch is in either the HI or the LO position, the unselected level is controlled manually.
INT DLY/WIDTH EXT WIDTH switch	A lighted push-push switch, which, when turned on in the EXT WIDTH mode, causes buffered input signal to bypass delay and width control circuits and appear directly at high- and low-level control circuits. Delay and width controls are effective when switch light is turned off, in which case the selected delay and width range indicating lights are on.
DELAY RANGE SELECTOR switches	A pair of momentary pushbutton switches which select range of input-to-output pulse delay. Ranges are 10 to 100 ns, 100 nsec to 1 usec, 1 to 10 usec, 10 to 100 usec, and 100 usec to 1 msec. Upper switch decreases range setting, and lower switch increases it.
DELAY potentiometer	Outer knob of concentric DELAY/WIDTH controls. Permits continuously variable adjustment of delay over the range selected with DELAY range selector switch.
WIDTH RANGE SELECTOR switches	A pair of momentary pushbutton switches which select range of pulse width adjustment. Ranges are 10 to 100 nsec, 100 nsec to 1 usec, 1 to 10 usec, 10 to 100 usec, and 100 usec to 1 msec. Upper switch decreases range setting, and lower switch increases it.
WIDTH potentiometer	Inner knob of concentric DELAY/WIDTH controls. Permits continuously variable adjustment of pulse width over the range selected with WIDTH range selector switch.
FR/REAR OUTPUT SELECTOR switch	A push-push switch which selects either front panel output or rear edge connector output. Rear output is operable with Options -002 and -003 only.

Fig 1-1 shows fr. panel controls + indicators on the PI-458-002.

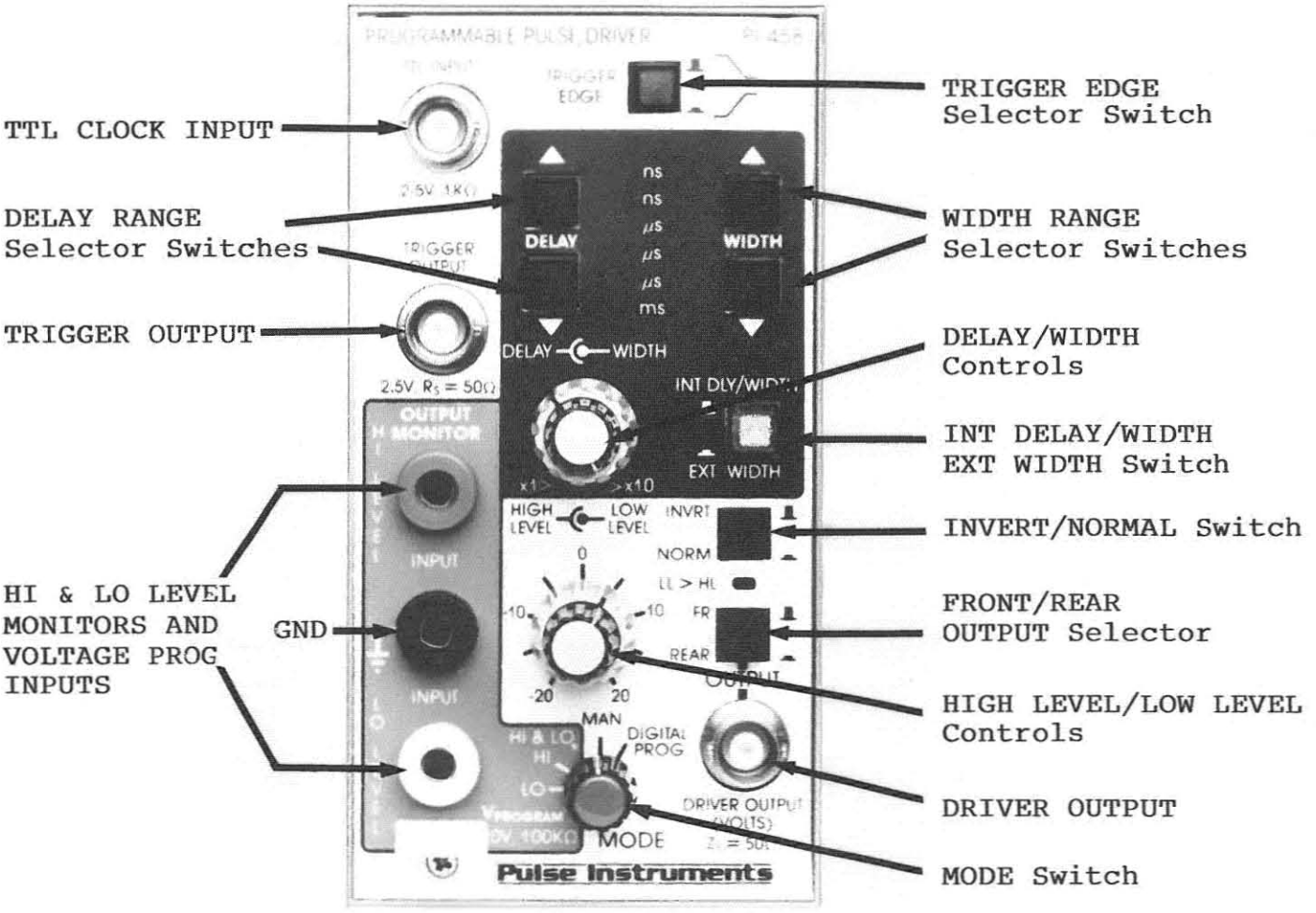

Figure 1-1. PI-458-002/003 Programmable Pulse Driver, Front Panel

SECTION 2

INSTALLATION

INSTALLATION AND CABLING

Install the PI-458 in any slot of a standard Tektronix TM-500 Series Power Module if use of the digital programming feature, or the rear input/output feature, is not required.

If the digital programming or rear input/output feature is to be used, install the unit in a compatibly keyed slot in a TM-506, Option 02, Power Module having PI MOD-DP custom interplug-in wiring. (In earlier units, this wiring has been designated MOD-451, MOD-451A, MOD-454, or MOD-454A.)

Connect interconnection cables as follows:

a. Connect coaxial input cable from test clock source to either the front panel TTL INPUT connector, or to the rear panel INPUT connector (see Figure 2-1).

b. Connect coaxial output cable from DRIVER OUTPUT connector on either the front panel, or the rear panel, to the item under test.

c. If the buffered input signal (TTL) is to be used externally, connect a coaxial cable from the front panel TRIGGER OUTPUT connector to the external equipment.

d. If digital programming is to be used, connect the digital interface cable connector to the 50-pin D-type connector on the rear panel.

e. If the rear output monitor function is to be used, connect the rear 25-pin D-type connector to the external equipment.

This completes installation procedures.

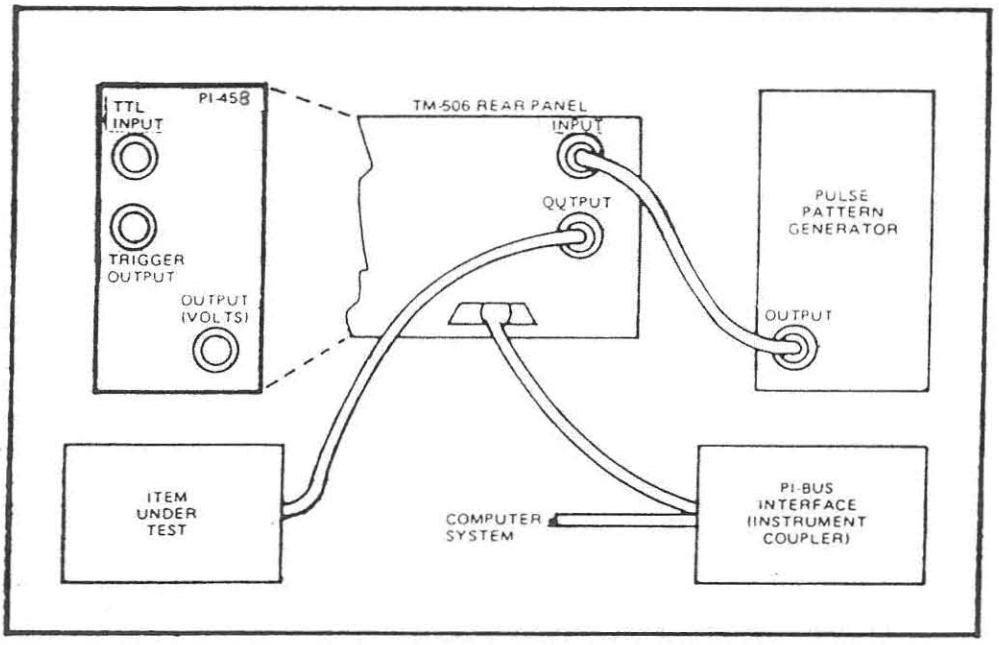

Figure 2-1 Typical Interconnections

SECTION 3

PERFORMANCE CHECKS AND CALIBRATION PROCEDURES

GENERAL

To verify correct operation of the PI-458, perform procedures in the following paragraphs. Refer to Section 5 of this manual for performance checks and calibration procedures applicable to the digitally programmable Model PI-458-002.

Because the PI-458 is carefully calibrated at the factory, subsequent recalibration should not be required and the following procedures need, generally, to be performed only to verify correct performance. If recalibration is required, readjust internal potentiometers and trimmer capacitors in accordance with instructions in these procedures.

TEST EQUIPMENT REQUIRED

The following equipment is required to perform the performance checks:

- Oscilloscope, dc to 300 MHz, 15 pf input capacitance (Tektronix Model 2465 preferred)
- DVM, 4.5 digit (5.5 digits required for PI-458-002)
- Pulse Generator
- Adjustable Power Supply, 0 to 20V dc.
- Feed-through Termination, 50 ohms, 2 watts
- Coaxial Cable, 3 feet long RG-58C/U (50 ohm). Quantity three.
- Adapter, BNC to banana jack
- Tee Connector, BNC.

WARM-UP PERIOD

Allow the plug-in unit to operate in a TM-500 Series mainframe for at least 15 minutes before attempting performance check procedures.

CHECKING OUTPUT VOLTAGE LEVELS

Checking Maximum Output High Level

To check the upper limit of the output high level, perform the following steps.

a. Set MODE switch to MAN position.

b. Push out INVRT/NORM switch to invert the output.

c. Connect negative terminal of DVM to the front panel banana jack marked as ground, and connect positive terminal of DVM to the DRIVER OUTPUT BNC connector, using the BNC-banana jack adapter.

d. Turn OUTPUT-HIGH LEVEL control fully clockwise (+20V, nominal), and set OUTPUT LOW-LEVEL control to the position marked 0 (high-level setting minus low-level setting must be less than 25V).

e. Read output voltage at DVM. DVM should indicate +20V minimum.

f. Connect a 50-ohm, 2-watt resistor between the DVM lead banana plugs at the front panel. DVM should indicate +10V minimum.

g. Remove the 50-ohm resistor connected in the previous step f.

Checking Minimum Output High Level

With the DVM connected as in the preceding steps, perform the following procedure to check the lower limit of the output high level.

a. Set both concentric OUTPUT knobs fully counterclockwise (-20V and -10V, respectively).

b. Read output voltage at DVM. DVM should indicate -10V or more negative.

c. Connect a 50-ohm, 2-watt resistor between the DVM lead banana plugs at the front panel. DVM should indicate -5V or more negative.

d. Remove the 50-ohm resistor connected in the previous step c.

Checking Minimum Output Low Level

With the DVM connected, and with controls set, as in the preceding steps, perform the following procedure to check the lower limit of the output low level.

a. Set OUTPUT-HIGH LEVEL control (outer concentric knob) to the position marked 0.

b. Push in INVRT/NORM switch (output not inverted).

c. Read output voltage at DVM. DVM should indicate -20V or more negative.

d. Connect a 50-ohm, 2-watt resistor between the DVM lead banana plugs at the front panel. DVM should indicate -10V or more negative.

e. Remove the 50-ohm resistor connected in the preceding step d.

Checking Maximum Output Low Level

With the DVM connected, and with controls set, as in the preceding steps, perform the following procedure to check the upper limit of the output low level.

a. Set both concentric OUTPUT knobs fully clockwise (+20V and +10V, respectively).

b. Read output voltage at DVM. DVM should indicate +10V minimum.

c. Connect a 50-ohm, 2-watt resistor between the DVM lead banana plugs at the front panel. DVM should indicate +5V minimum.

d. Remove the 50-ohm resistor connected in the preceding step c.

CHECKING AND ADJUSTING OUTPUT OFFSET VOLTAGE AND CHECKING VOLTAGE PROGRAMMING

Perform the following steps to check the output offset voltage, and voltage programming ranges.

a. Set MODE switch to the HI and LO position.

b. Remove DVM leads from the PI-458 front panel.

CHECKING AND ADJUSTING OUTPUT OFFSET VOLTAGE AND CHECKING VOLTAGE PROGRAMMING (cont'd)

c. Connect Power Supply negative output lead to LOW LEVEL-INPUT banana jack, and connect Power Supply positive output lead to Ground banana jack.

d. Adjust Power Supply output voltage to -20V dc.

e. Connect positive lead of DVM to the -20V Power Supply output, and connect negative lead of DVM to the PI-458 output (at BNC/banana jack adapter).

f. Adjust low level offset potentiometer R152 to obtain DVM reading of 0V$\pm$10mV (output low level offset).

g. At the Power Supply, slowly adjust the Power Supply output voltage from -20V to -1V, observing DVM. DVM should indicate no voltage greater than $\pm$35mV.

h. Disconnect Power Supply output leads, and the positive DVM lead, from the PI-458.

i. Push out INVRT/NORM switch (to invert output).

j. Connect Power Supply positive output lead to HIGH LEVEL-INPUT banana jack, and connect Power Supply negative output lead to Ground banana jack.

k. Connect positive lead of DVM to the Power Supply positive output.

l. Adjust Power Supply output voltage to +20V.

m. Adjust high level offset potentiometer R153 to obtain DVM reading of 0V$\pm$10mV (output high level offset).

n. At the Power Supply, slowly adjust the Power Supply output voltage from +20V to +1V, observing DVM. DVM should indicate no voltage greater than $\pm$35mV.

o. Disconnect Power Supply output leads, and DVM leads, from the PI-458.

CHECKING OUTPUT RISE AND FALL TIMES

Perform the following steps to check output rise and fall times.

a. Set MODE switch to MAN position.

b. Push in INVRT/NORM switch to obtain normal (uninverted) signal.

c. Set up Pulse Generator to obtain a 3-volt, positive-going pulse, having a pulse width of 10ns at the 1.5V level.

d. Connect Pulse Generator output to the PI-458 TTL INPUT connector, using a 3-foot-long, 50-ohm coaxial cable.

e. Using a 3-foot-long, 50-ohm coaxial cable, connect PI-458 DRIVER OUTPUT connector to a 300-MHz Oscilloscope, and set oscilloscope input to 1M-ohm DC.

f. Push out INT DLY/WIDTH/EXT WIDTH switch to enable Delay and Width Control functions, and set PI-458 output pulse width to approximately 50ns.

g. Set Oscilloscope vertical display to 5V/division.

h. Adjust concentric OUTPUT HIGH LEVEL and LOW LEVEL controls to obtain a pulse height on the Oscilloscope of exactly 4 centimeters (20V peak-to-peak).

i. Change oscilloscope vertical display to 2V/division and adjust vertical gain control knob to obtain a 5-centimeter display.

j. Check rise and fall times between 10 per cent and 90 per cent level points. Rise and fall times should be less than 6ns.

k. Set oscilloscope input to 50 ohm DC and set vertical gain control knob to the fully CW position (calibrated).

l. Readjust the HIGH and LOW LEVEL controls, if necessary, to obtain a 5 centimeter display.

m. Check rise and fall times between 10 per cent and 90 per cent level points. Rise and fall times should be less than 5ns.

CHECKING VARIABLE OUTPUT PULSE DELAY

To check correct operation of pulse delay controls, perform the following steps, with the Pulse Generator connected to the PI-458 as in the preceding procedure.

a. Connect 3-foot-long, 50-ohm coaxial cables as follows:

1. Between TRIGGER OUTPUT connector on PI-458A and Vertical input of Oscilloscope Channel 1, set to 1M ohm DC.

2. Between DRIVER OUTPUT connector on PI-458A and Vertical input of Oscilloscope Channel 2, set to 50 ohm DC.

b. At PI-458, set DELAY range to 10 ns.

c. Push out INT DLY/WIDTH/EXT WIDTH switch to enable Delay and Width control functions.

d. Set DELAY control (outer knob of the concentric controls) fully counterclockwise.

e. At Pulse Generator, set pulse amplitude to 3V, and pulse width to 10 nsec at the 1.5V level (seen on Oscilloscope).

f. Oscilloscope should show no more than 10 nsec delay between the 1.5V amplitude point of the leading edge of the TRIGGER OUTPUT signal, and the 50-per cent point (0V) of the leading edge of the DRIVER OUTPUT signal.

g. Set PI-458A DELAY control fully clockwise. Oscilloscope should show at least 100 ns delay between points defined in preceding step f.

h. Set DELAY control fully counterclockwise, and set DELAY range to 100 ns. Oscilloscope should show no more than 100 ns delay between the 1.5V amplitude point of the leading edge of the TRIGGER OUTPUT signal, and the 50-per cent point of the leading edge of the DRIVER OUTPUT signal.

i. Set DELAY control fully clockwise. Oscilloscope should show at least 1 usec delay between points defined in preceding step h.

j. Set DELAY control fully counterclockwise, and set DELAY range switch to 1 us position. Oscilloscope should show no more than 1 usec delay between the 1.5V amplitude point of the leading edge of the TRIGGER OUTPUT signal, and the 50-per cent point of the leading edge of the DRIVER OUTPUT signal.

CHECKING VARIABLE OUTPUT PULSE DELAY (cont'd)

k. Set DELAY control fully clockwise. Oscilloscope should show at least 10 usec delay between points defined in preceding step j.

l. Set DELAY control fully counterclockwise, and set DELAY range to 10 us. Oscilloscope should show no more than 10 usec delay between the 1.5V amplitude point of the leading edge of the TRIGGER OUTPUT signal, and the 50-per cent point of the leading edge of the DRIVER OUTPUT signal.

m. Set DELAY control fully clockwise. Oscilloscope should show at least 100 usec delay between points defined in preceding step 1.

n. Set DELAY control fully counterclockwise, and set DELAY range switch to 100 us position. Oscilloscope should show no more than 100 usec delay between the 1.5V amplitude point of the leading edge of the TRIGGER OUTPUT signal, and the 50-per cent point of the leading edge of the DRIVER OUTPUT signal.

o. Set DELAY control fully clockwise. Oscilloscope should show at least 1 ms delay between points defined in preceding step n.

p. Set DELAY control fully counterclockwise, and set DELAY range to 1 ms. Oscilloscope should show no more than 1 msec delay between the 1.5V amplitude point of the leading edge of the TRIGGER OUTPUT signal, and the 50-per cent point of the leading edge of the DRIVER OUTPUT signal.

q. Set DELAY control fully clockwise. Oscilloscope should show at least 10 msec delay between points defined in preceding step p.

CHECKING VARIABLE OUTPUT PULSE WIDTH

Leaving Pulse Generator and Oscilloscope leads connected, and the Pulse Generator and Oscilloscope set up, as in the preceding steps, check operation of PI-458 pulse width controls by performing the following procedure.

a. Set WIDTH range to 10 ns, and set WIDTH control knob (inner knob of concentric DELAY and WIDTH controls) fully counterclockwise.

b. Adjust C until oscilloscope shows a pulse width between 8 and 9nsec at 50-per cent amplitude (OV).

c. Set WIDTH control fully clockwise. Oscilloscope should show a pulse no narrower than 100 ns at 50-per cent amplitude.

d. Set WIDTH range to 100 ns.

e. Set WIDTH control fully counterclockwise. Oscilloscope should show a pulse no wider than 100 ns at 50-per cent amplitude.

f. Set WIDTH control fully clockwise. Oscilloscope should show a pulse no narrower than 1 usec at 50-per cent amplitude.

g. Set WIDTH range switch to 1 usec.

h. Set WIDTH control fully counterclockwise. Oscilloscope should show a pulse no wider than 1 usec at 50-per cent amplitude.

i. Set WIDTH control fully clockwise. Oscilloscope should show a pulse no narrower than 10 usec at 50-per cent amplitude.

j. Set WIDTH range to 10 us.

k. Set WIDTH control fully counterclockwise. Oscilloscope should show a pulse no wider than 10 usec at 50-per cent amplitude.

1. Set WIDTH control fully clockwise. Oscilloscope should show a pulse no narrower than 100 usec at 50-per cent amplitude.

m. Set WIDTH range to 100 us.

n. Set WIDTH control fully counterclockwise. Oscilloscope should show a pulse no wider than 100 usec at 50-per cent amplitude.

o. Set WIDTH control fully clockwise. Oscilloscope should show a pulse no narrower than 1 ms at 50-per cent amplitude.

p. Set WIDTH range to 1 ms.

CHECKING VARIABLE OUTPUT PULSE WIDTH (cont'd)

q. Set WIDTH control fully counterclockwise. Oscilloscope should show a pulse no wider than 1 msec at 50-per cent amplitude.

r. Set WIDTH control fully clockwise. Oscilloscope should show a pulse no narrower than 10 msec at 50-per cent amplitude.

CHECKING MAXIMUM OUTPUT REPETITION RATE, AND MINIMUM EXT WIDTH

With Pulse Generator and Oscilloscope connected as in the preceding steps, perform the following procedure to check the upper limit of the output pulse repetition rate, and the lower limit of output pulse width.

a. Set OUTPUT HIGH and LOW LEVELS to +5V and -5V into 50 ohms, respectively, and INT DLY/WIDTH/EXT WIDTH switch to EXT WIDTH.

b. Adjust Oscilloscope to obtain a displayed pulse height of exactly 5 centimeters.

c. At Pulse Generator, adjust pulse repetition rate to approximately 10 MHz, and adjust pulse width to obtain a 10-volt pulse of minimum width.

d. Slowly increase pulse repetition rate, observing Oscilloscope. Pulse height must remain at 5cm until pulse rate rises to at least 50 MHz. (Readjust pulse width at the Pulse Generator, if necessary, to maintain 5-cm pulses to the maximum pulse repetition rate.)

e. Push INVRT/NORM switch to invert the output signal.

f. Perform preceding steps c. and d. for the inverted output signal.

g. Set Oscilloscope input to 1 M ohm DC and 5V/division. Readjust HIGH and LOW LEVEL controls, if necessary, to obtain a 4-centimeter display.

h. Repeat steps d., e., and f. for 40 MHz minimum pulse repetition rate.

i. Adjust Pulse Generator output repetition rate to approximately 10 MHz. Oscilloscope should display pulse width of 10nsec and 12ns maximum, at the point of 50-per cent amplitude, when its input is set to 50 ohms DC and 1 M ohm DC, respectively.

j. Push INT DLY/WIDTH/EXT WIDTH switch to enable DELAY and WIDTH functions.

k. Set DELAY range and WIDTH range to 10 ns.

l. Set DELAY and WIDTH controls to fully counterclockwise.

m. Repeat steps d., e., f., g. and h.

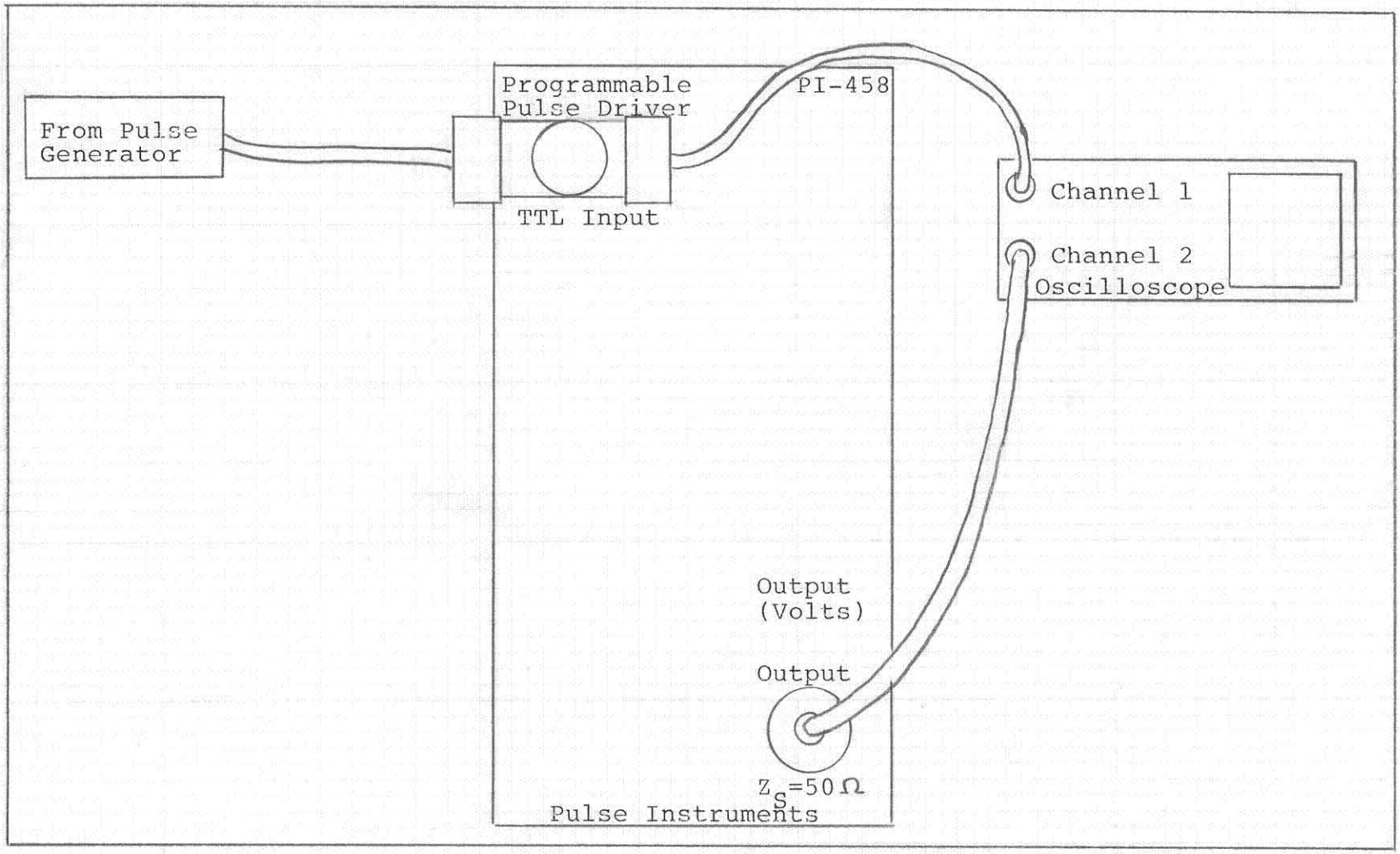

Figure 3-1. Interconnections for Insertion Pulse Delay Measurement (Input to Output)

CHECKING INSERTION PULSE DELAYS

With the Pulse Generator and Oscilloscope connected and set up as in the preceding steps, check insertion pulse delays as follows.

a. Push in INT DLY/WIDTH/EXT WIDTH switch to disable Width and Delay control functions.

b. Connect Oscilloscope Channel 1 input cable to TRIGGER OUTPUT connector on PI-458A front panel.

c. At Pulse Generator, adjust output pulse width to 50 nsec (seen on Oscilloscope). Delay between leading and trailing edges of the TRIGGER OUTPUT pulse at 1.5V amplitude, and those of the DRIVER OUTPUT pulse at 50-per cent points, should be no greater than 15 nsec.

d. Disconnect Oscilloscope Channel 1 input cable from TRIGGER OUTPUT connector.

e. Disconnect Pulse Generator signal output cable from the PI-458A INPUT connector, and connect a BNC Tee connector at the INPUT connector (see Figure 3-1).

f. Connect Pulse Generator signal output cable, and Oscilloscope Channel 1 input cable, to the Tee connector.

g. Set Channel 1 input to 50 ohms DC.

h. At Pulse Generator, adjust pulse amplitude to 3V (seen on Oscilloscope). Delay between leading and trailing edges of the input pulse at 1.5V amplitude, and those of the DRIVER OUTPUT pulse at 50-per cent points, should be no greater than 50nsec.

CHECKING OUTPUT ABERRATIONS

With Pulse Generator and Oscilloscope connected and set up as in the preceding steps, check output aberration amplitude as follows:

a. Set Channel 2 input to 1 M ohm DC.

b. Set concentric HIGH LEVEL and LOW LEVEL controls to obtain a pulse (seen on Oscilloscope) between +1.5V (high level) and -1.5V (low level).

c. Adjust Pulse Generator to obtain a pulse width of 1 usec (seen on Oscilloscope).

d. Oscilloscope should show aberration no greater than 0.5V peak-to-peak.

CHECKING MAXIMUM OUTPUT AMPLITUDE

With Pulse Generator and Oscilloscope connected and set up as in the preceding steps, check maximum output amplitude by performing the following procedure.

a. Set concentric HIGH LEVEL and LOW LEVEL controls to approximate +10, and -10 positions, respectively. Slowly rotate HIGH LEVEL control clockwise until a change is observed in the output low level (base line). Oscilloscope should show a pulse of at least 25V peak-to-peak.

b. Set Channel 2 input to 50 ohms DC. Oscilloscope should show pulse of at least 12.5V peak-to-peak.

CHECKING DIGITAL PROGRAMMING OPTION (-002)

If the plug-in unit is Model PI-458-002, perform Check and Calibration procedures outlined in Section 5 of this manual.

SECTION 4

THEORY OF OPERATION

GENERAL

This section describes the theory of operation of the PI-458 in terms of the block diagram (Figure 4-1), and with reference to the schematic diagrams included at the back part of this manual.

INPUT, AND DELAY AND PULSE WIDTH CONTROL CIRCUITS

(Refer to schematic diagram, Sheet 1.) These circuits receive the input clock pulse, and perform the following functions:

a. Buffer the received clock pulse to the TRIGGER OUTPUT connector.

b. Permit adjusting the delay and width of the pulse triggered by either the rising or the falling edge of the input pulse. The delay and width of the triggered pulse become characteristics of the PI-458 output pulse.

c. Permit selecting the polarity of the output pulse.

Note that, except for the input buffer and the trigger output circuit which operate at TTL logic levels, all circuits shown on sheet 1 of the schedmatic diagram operate at ECL logic levels.

The input clock pulse is received through either the front panel TTL INPUT connector, or through the rear panel CLOCK connector. The applied input is ORed to a buffer which puts the received trigger signal at the front panel TRIGGER OUTPUT connector, at one input of multiplexer (U33-6) and at the differentiating circuit (U32-11) which subsequently triggers the delay one-shot (Q6).

The delay control circuit delays the received pulse transition by a period adjustable from 10 nanoseconds to 10 miliseconds. The circuit comprises the one-shot whose delay period is continually adjustable over a selected range by means of potentiometer R199, acting through (U11-14). The delay range is selected by two push-button switches which connect the appropriate timing capacitor to the delay one-shot circuit through a FET switch. The delay ranges are 10 ns, 100 ns, 1 us, 10 us, 100 us and 1 ms.

INPUT, AND DELAY AND PULSE WIDTH CONTROL CIRCUITS (cont'd)

The delay one-shot presents the delayed trigger pulse at the input of the width one-shot. The pulse width control circuit produces a pulse which falls with the delayed trigger pulse, and rises at a time determined by the setting of the WIDTH potentiometer and range switch. Pulse width may be adjusted from 10 nanoseconds to 10 miliseconds.

The pulse width circuit is similar to the delay circuit, with pulse width within a selected range determined by the setting of potentiometer R200, acting through (U12-17). The width range is selected by two push-button switches which connect the appropriate timing capacitor to the width one-shot circuit through a FET switch. The width ranges are 10 ns, 100 ns, 1 us, 10 us, 100 us and 1 ms.

The pulse, delayed and of the selected width, appears at the second input of muliplex U33-5. This delayed pulse becomes the selected output when the INT DLY/WIDTH-EXT WIDTH switch is out, enabling the display of the selected delay and width ranges. When the switch is pushed in, thus illuminated, the buffered trigger pulse is selected.

When the INVRT/NORM switch is pushed in, (NORM), the input and output pulses are in phase. When the switch is pushed out (INVRT), the output pulse is inverted with respect to the input pulse.

LEVEL CONTROL CIRCUITS

(Refer to schematic diagram, sheet 2.) These circuits receive inputs from manual level controls, or from an external voltage program, or from the internal Digital Programming Option (-002); and deliver level-control voltages to High Level and Low Level channels in pulse generator circuits (schematic diagram, sheet 2).

The control signal sources are selected by means of the MODE switch, as follows:

a. In the MAN (Manual) position, the switch selects voltages from the HIGH LEVEL and LOW LEVEL control potentiometers (R156, and R157, respectively). The voltage at the wipers of these potentiometers are in the ranges between -10V and +20V, and between -20V and +10V, respectively. These reference voltages are derived from the regulated ±26V supply lines by additional

regulator circuits U16/U18, and U17/U19, respectively.

b. In the DIGITAL PROGRAM position, the switch selects control voltages from the high-level and low-level DACs in the Digital Programming option (refer to Section 5 of this manual for a description of Option -002 circuits).

c. In the HI and LO position, the switch selects external control voltages present at both the HIGH LEVEL jack, and the LOW LEVEL jack, on the front panel.

d. In the HI position, the switch selects the external control voltage present at the HIGH LEVEL jack on the front panel, and the voltage at the wiper of the manual LOW LEVEL potentiometer.

e. In the LO position, the switch selects the external control voltage present at the LOW LEVEL jack on the front panel, and the voltage at the wiper of the manual HIGH LEVEL potentiometer.

The selected high-level control signal, and the selected low-level control signal, are each applied to an amplifier circuit (high level U22, low level U36). Each amplifier circuit drives the related pulse level switch circuit (sheet 2).

PULSE DRIVE CIRCUITS

(Refer to schematic diagram, sheet). These circuits consist of a high level drive amplifier, a low level drive amplifier, a pair of complimentary switches, and a complimentary output emitter follower stage. The signal input to these circuits is derived either from the buffered input clock or a delayed pulse of a selected width, triggered by the input clock.

Additionally, a high level and a low level control (reference) voltages are connected to these circuits for setting the upper and lower voltage levels of the output pulse.

The buffered input clock and the delayed pulse of selected width are multiplexed through U33, using the front panel EXT WIDTH/INT DLY/WIDTH switch, respectively. Output of U33 is level shifted through U20, and the resultant differential signals are used for driving the complimentary switch Q5 and Q11, one of which is ON while the other is OFF, or visa versa. The outputs of Q5 and Q11 are then connected to complimentary output emmitter follower stage U27 which has an effective output impedance of 50 ohms.

Output short circuit protection is accomplished through voltage drops across sense resistors R77, R78, R129 and R130 which in turn turn on either Q7 or Q18 or both, resulting in reduced output voltages.

POWER SUPPLY

(Refer to schematic diagram, sheet 4.) The PI-458 receives both ac and dc voltages from the mainframe power supply. Rectifier/filter circuits receive ac voltages and produce regulated $\pm$26V, and unregulated $\pm$11V. Dc voltages from the

mainframe are regulated to obtain supplies of $\pm$5V and $\pm$15V.

SECTION 5

DIGITAL PROGRAMMING OPTION

GENERAL

The Digital Programming option (-002) is a factory-installed feature which adds digitally programmable high level and low level control to the other capabilities of the PI-458. The digital interface permits using the PI-458-002, in conjunction with a suitable controller, in a computer-controlled automatic testing system.

If the digital programming option is not required in a given application, the PI-458-002 may be used in any standard TM-500 Series Power Module. In order to use the digital programming option, however, it is necessary that the unit be installed in a TM-506 Power Module with Option 02, and incorporating Pulse Instruments special wiring MOD-DP.

The modified Power Module includes additional rear-panel TTL Clock Input, and Pulse Driver Output connectors (BNC), and a 25-pin, D-type output monitor connector. Digital inputs are through a 50-pin, D-type connector at the rear of the Power Module. Digital inputs are compatible with low-power Schottky TTL devices.

The 21 digital input signals are as follows:

- D1 — Selects output polarity (negative/positive).
- D2-D12 — Encode output level magnitude.
- PS1-PS6 — Selects the plug-in.
- MS — Selects the mainframe.
- LS — Selects high level, or low level, channel (high/low).
- DS — Data strobe loads data on lines D1-D12 into the plug-in.

For detailed timing and general digital interface information, refer to the Pulse Instrument Company document Digital Programming for PI-Series Plug-In Instruments.

FRONT PANEL CONTROLS

Controls and other facilities on the front panel are the same as those on the PI-458 except that the MODE switch may select the added DIGITAL PROGRAM position. This position of the MODE switch disables all manual high level and low level controls, and connects digital inputs to high level and low level circuits.

The front panel banana jacks retain their monitoring function in digital program operation.

REAR INPUT AND OUTPUT CONNECTIONS

The -002 or -003 option provides rear input and output connections which are accessed through BNC connectors on the appropriately modified mainframe. The rear TTL Clock Input is ORed with the INPUT connector on the front panel, and is furnished for cabling convenience.

The rear Pulse Driver Output is connected to the output circuit only when the front panel FR/REAR switch is pushed in. Because of the added cable length to the rear output connector and of the discontinuity introduced by the edge connector, it is recommended that the rear output be used with a 50 ohm load termination whenever possible.

SPECIFICATIONS

Except for specifications given in Table 5-1, performance specifications for the PI-458-002 are identical to those given for the basic PI-458 (refer to Section 1 of this manual).

Table 5-1. Performance Specifications

Specification	Characteristics
OUTPUT LEVELS	Same as for PI-458 but programmable by means of digital program, as well as manually or by voltage program.
DIGITAL PROGRAM	
Resolution	11 bits (10 mV typical) plus sign bit.
Accuracy	±100mV of programmed value.
RISE AND FALL TIMES (at rear connectors)	<5.5ns with 50 ohm termination at the end of a 3-foot-length RG58C/U cable.
MAX OUTPUT REPETITION RATE (at rear connectors)	> 45 MHz with 50 ohm termination at the end of a 3-foot-length RG58C/U cable.

DIGITAL INTERFACE

Option -002 provides control logic and storage registers within the plug-in instrument which interface with the custom wiring in the mainframe. This wiring provides 21 lines connected from the backplane to a 50-pin D-type connector at the rear of the mainframe. The 21 lines have the following functions:

a. Data (D1 through D12). Each of these 12 lines is wired, in daisy-chain fashion, to the connector for each plug-in module. D1 is the sign bit for the data, with a "0" bit (low) specifying a positive output, and a "1" bit (high) specifying a negative output.

Bit D2 is the most-significant data bit, with bit D 12 the least-significant bit. All 12 bits are loaded, simultaneously, by the DS (Data Strobe) pulse.

b. Mainframe Select (MS). This line is used to select the specific mainframe, among others, to receive programmed information. That is, when the MS line is low, any plug-in instrument in the selected mainframe is enabled to receive data if its related PS line is also low.

c. Plug-in Select (PS1 through PS6). One of six PS lines is wired to each plug-in position in the TM-506 mainframe. When the PS line at the position in which the PI-458-002 is installed goes low, that plug-in is enabled to receive data, if the MS line is also low.

d. Level Select (LS). This line is wired in common to all plug-in instruments in the mainframe. When the line is high, data will be loaded into the high level channel. When the line is low, data will be loaded into the low level channel.

Once the mainframe, plug-in, and the high or low level have been selected, the MS, PS, and LS lines must remain at the select levels for as long as data is to be transferred to the instrument.

No special enabling sequence is required when communicating with the plug-in, and either low level, or high level data may be loaded first. The Data Strobe (DS) should not rise until data has been on the bus for at least 14 microseconds, and DS must persist for at least 1 microsecond.

Note that the programmed high level must always be more positive than the programmed low level. If it is not, no output will appear.

Figure 5-1 shows the general timing required to perform a select-and-transfer cycle to set up the instrument to receive data, and to load the word into its internal registers.

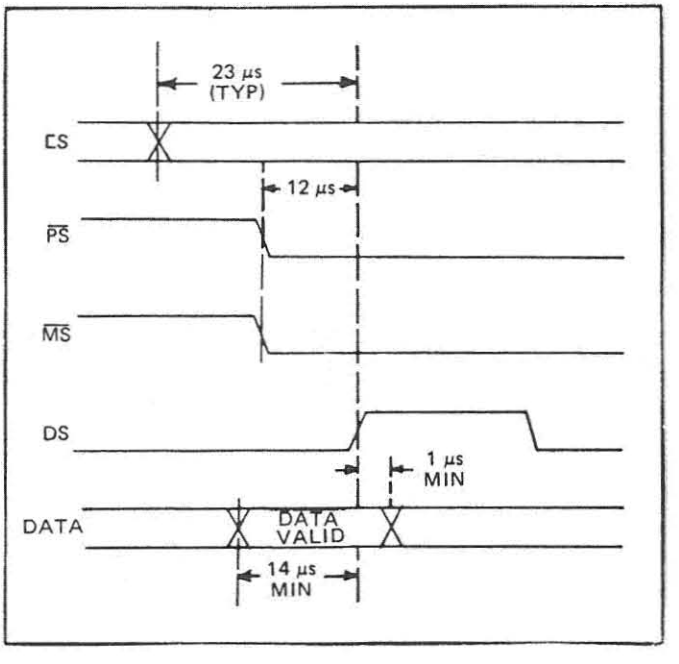

Figure 5-1. Digital Interface Timing

DATA CODING

The 12-bit data code is complementary offset binary. This code is obtained by complementing the straight binary code, and then subtracting from the midscale value of the straight binary code.

000000000000 = positive full scale
111111111111 = negative full scale
011111111111 = midscale value, or zero

Table 5-2 gives codes for typical output level values.

The binary word required to generate a positive output level VO+ may be obtained using the equation:

$$VO+ = a1 + a2D2 + \ldots a12D12 = a1 + \sum aiDi$$

where Di is the weight of a given bit (see Table 5-2) and ai is the binary coefficient. The term a1 = 0 for positive or zero output levels, and a1 = 1 for negative output levels.

Coding is best illustrated by an example. Referring to Table 5-2, note that bit D1 specifies polarity, and bits D2 through D12 specify voltages in binary-weighted increments.

With resolution of 11 bits (1/2048), the nominal voltage of 20.48 may be resolved to 20.48V/2048, or 0.0100V, the value of bit 12. The digital code corresponding to any positive voltage between zero and the maximum voltage is found by adding together bit weights whose sum is the requird voltage. For example:

Encode the voltage +8.2000V:

First, identify the required terms in the equation. These are identified and then added together as follows:

	Value	Term
	5.12	D3
	2.560	D4
	.320	D7
	.160	D8
	.040	D10
Sum	8.2000	

Then, set the corresponding coefficients (a1, a3, a4, a7, and a10) equal to "0", and set the remaining coefficients equal to "1". The resulting binary word is:

W = 010011001011

When this binary word is loaded into either the high level channel, or the low level channel, of the PI-458-002 digital logic, the selected output will be at a level of +8.2000V ±100 mV max.

A negative voltage may be expressed as W - 1, where W is the code for the corresponding positive voltage. For example:

If W = +8.20000 = 010011001011, then
W -1 = -8.2000 = 101100110100 - 000000000001 = 101100110011.

That is, to find the binary code for a negative output level, first determine the input for the corresponding positive output, complement that code, and then subtract 1.

Output Level	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12
	+ −	10.24V	5.120V	2.560V	1.280V	640mV	320mV	160.0mV	80.0mV	40.0mV	20.0mV	10.0mV
20.470V	0	0	0	0	0	0	0	0	0	0	0	0
20.000V	0	0	0	0	0	0	1	0	1	1	1	1
18.000V	0	0	0	0	1	1	1	1	0	1	1	1
15.000V	0	0	1	0	0	0	1	0	0	0	1	1
12.000V	0	0	1	1	0	1	0	0	1	1	1	1
10.000V	0	1	0	0	0	0	0	1	0	1	1	1
7.500V	0	1	0	1	0	0	0	1	0	0	0	1
5.000V	0	1	1	0	0	0	0	0	1	0	1	1
2.000V	0	1	1	1	0	0	1	1	0	1	1	1
1.000V	0	1	1	1	1	0	0	1	1	0	1	1
0.000V	0	1	1	1	1	1	1	1	1	1	1	1
-1.000V	1	0	0	0	0	1	1	0	0	0	1	1
-2.000V	1	0	0	0	1	1	0	0	0	1	1	1
-5.000V	1	0	0	1	1	1	1	1	0	0	1	1
-7.500V	1	0	1	0	1	1	1	0	1	1	0	1
-10.000V	1	0	1	1	1	1	1	0	0	1	1	1
-12.000V	1	1	0	0	1	0	1	0	1	1	1	1
-15.000V	1	1	0	1	1	1	0	1	1	0	1	1
-18.000V	1	1	1	1	0	0	0	0	0	1	1	1
-20.000V	1	1	1	1	1	1	0	0	1	1	1	1
-20.480V	1	1	1	1	1	1	1	1	1	1	1	1

Table 5-2. Typical Output Level Codes

PERFORMANCE CHECK AND CALIBRATION PROCEDURES

Before performing the following procedures, complete Performance Checks and Calibration Procedures in Section 3 of this manual.

Because the PI-458-002 is carefully calibrated at the factory, subsequent recalibration should not be required and the following procedures need, generally, to be performed only to verify correct performance. If recalibration is required, readjust internal potentiometers in accordance with instructions in these procedures.

Set-up and Test Equipment

These procedures require the same test equipment as procedures for the basic PI-458 (refer to Section 3), as well as the PI-810 Manual Programming Box (Pulse Instrument Company P/N 99000160), if a suitable controller is not available.

Note that the PI-458-002 can be checked and calibrated only when it is installed in a TM-506 Power Module (mainframe) which has been specially wired (Pulse Instruments MOD-DP). Note that equivalent modifications, made prior to 1982, are designated MOD-451, MOD-451A, MOD-454, and MOD-454A.

To speed checking and calibration, three PI-458-002 units may be installed in slots 1, 3, and 5 of the mainframe and checked and recalibrated at the same time.

Connect the Manual Programming Box (PI-810) to the rear panel 50-pin connector. The PI-810 is used to control plug-in and level selection, and to load the binary word into the selected plug-in. Table 5-2 gives the binary codes which select typical output levels. For operating instructions for the PI-810, refer to the instructions furnished with the PI-810.

When performing the following procedures, be sure that there is no signal connection to the front or rear panel BNC INPUT connector. Measure output voltage using a 5 1/2-digit DVM, using a coaxial cable and a BNC-to-banana jack adapter.

Warm-up Period

Allow the PI-458-002 to operate in the mainframe for at least 25 minutes before attempting to perform the following procedures. During warm up, verify that the digital program mode is operating by loading binary codes for a number of selected high and low levels, and checking corresponding outputs at the DVM.

NOTE

> In the following procedures, the MODE switch on the PI-458-002 is first set to the MANUAL position, and the High and Low Level DAC outputs, without the driver circuits, are calibrated. The driver output offset voltage is then checked, and finally the programmed output High and Low Levels are checked.

Checking and Adjusting DAC Output Voltage Offset

The DAC bipolar offsets are adjusted (if necessary) using potentiometers accessible at the right-hand side of the plug-in unit (see Figure 5-2). The high level offset adjustment is designated R37, and the low level offset adjustment is designated R21. A small flashlight will help in locating screw slots in adjustment potentiometers.

Proceed as follows:

a. At the PI-810, set-up and load codes for -20.480V for both High and Low Levels (refer to Table 5-2).

b. Connect DVM leads to the DAC output test points as shown in Figure 5-2.

c. Adjust High and Low Level offset potentiometers R37 and R21 to obtain DVM readings of -20.480V$\pm$2mV.

Checking and Adjusting Gain

High level and low level channel gains are adjusted (if necessary) using potentiometers accessible at the right-hand side of the plug-in unit (Figure 5-2). The high level gain potentiometer is designated R38, and the low level gain potentiometer is designated R20.

Proceed as follows:

a. At the PI-810, set-up and load codes for +20.470V for both high and low levels (refer to Table 5-2).

b. Adjust high and low level gain potentiometers R38 and R21 to obtain DVM readings of +20.470V ±2mV.

c. Repeat DAC offset voltage adjustments, and gain adjustments, as necessary until low level and high level channels are calibrated to end points within ±5mV.

d. Recheck output offset voltages as outlined in Section 3, if desired. Recalibrate if output offset voltages are greater than ±35mV.

e. Connect output to DVM with a 3-foot length coaxial cable and a BNC to banana jack adapter. Verify all voltages listed in Table 5-2, if that is desired. Any voltage selected should be accurate to within ±100mV.

Checking Rear Panel Input and Minimum Output Transition Time

Perform the following procedures to check performance using rear panel input and output connectors.

a. Set front panel FR/REAR switch to REAR.

b. Connect Pulse Generator output cable to rear panel BNC connector marked TTL CLOCK INPUT.

c. Adjust Pulse Generator to obtain a pulse of 3V amplitude at the rear panel TTL CLOCK INPUT connector.

d. Connect rear panel BNC connector marked CCD CLK AND POWER SUPPLY OUTPUT to Vertical input of Oscilloscope, and set Oscilloscope input 50-ohms.

e. At PI-810, load codes to obtain a pulse between -10V (low level), and +10V (high level). The Oscilloscope display is actually ±5V, due to the 50-ohm load. Adjust pulse height on

Oscilloscope to exactly 5 cm.

f. Neither rise time nor fall time should exceed 5.5 nsec at points that are 10 percent, and 90 percent, of pulse height.

g. If rear panel output is not to be used, restore front panel FR-REAR switch to the FR position.

h. Disconnect all test equipment cables from the rear of the mainframe.