component news

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Designers' guide to CMOS RAMS

The last year or so has seen CMOS RAMs decreasing in price and increasing in density. Compared to NMOS RAMs, the cost per bit is still higher, but in some applications the lower power requirements are worth the extra cost.

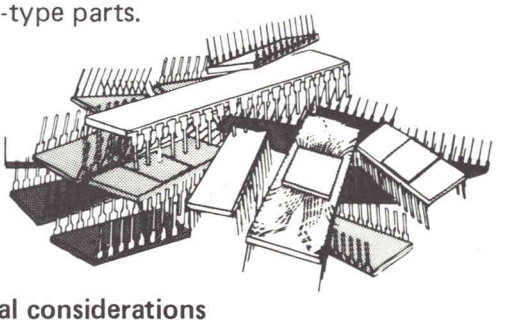
These parts are usually found in portable or battery-operated equipment. They are also used in plug-ins to cut the total power required so that old mainframes can use the newer plug-ins without any redesign of the power supply.

CMOS RAM vendors usually specify their parts by the maximum power supply current required in the battery backup or standby mode. The normal standby voltage is three volts, but some vendors specify their parts down to two volts. The current in the standby mode for the 4K RAMs varies from 5μA to 15μA depending on the vendor.

Tektronix has recently part-numbered the HMI-6514-9, a 1K X 4 CMOS RAM by Harris. This part has a 300 nS maximum access time and a current spec of 5μA at three volts for standby. The operating current spec is 6 mA at five volts and 1 MHz. This part has the same pinout as the industry standard 2114. It will fit directly into some, but not all, 2114 boards. The part requires a high to low transition on the Enable line to latch the addresses for every Read or Write cycle. Many systems do this already and some can be modified easily. The 6800 systems that use either VmA or Phase 2 as an input to the chip select circuitry will run these parts without modification.

There are several second sources for the Harris part that will be in full production later this year. RCA and NEC have parts which do not require the latched addresses. The RCA part is the MWS 5114. This part has a 650 nS access time and a 15μA current spec at two volts. The operating current is 5μA at five volts. The part is a direct replacement for the 2114 except for the slower access time. RCA will have a faster part later this year.

The NEC part is the UPD 444. This part has a 300 nS access time and 10μA current spec at three volts. The operating current is 100μA at five volts. This part will directly replace all but the fastest 2114-type parts.



Special considerations

There are several special considerations when designing with CMOS RAMs. The first problem engineers have is excessive battery drain. This is usually caused by not properly terminating all inputs to the RAM in the power down mode. The inputs must be pulled up to V_{CC} or down to ground to keep the input buffers from drawing current. If the inputs are driven by TTL they will be pulled to ground when the TTL power goes away. Other systems use pull-up or pull-down resistors to control these lines.

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The second problem is a latch-up mode which some RAMs have. The CMOS RAMs require that the input voltages are always less than the supply. This includes noise on the V_{CC} pin. A negative spike of only a few hundred nanoseconds is sufficient to latch some parts, and the power supply must be removed to get out of this mode. The parts are not usually damaged if the condition is corrected in a few minutes. The Harris HMI-6514-9 is especially sensitive to negative V_{CC} spikes.

The third problem is random writes into the RAM array. This is caused by negative spikes on the address or control inputs. The parts should be buffered from the system bus unless some other negative spike protection is provided.

Battery backup circuits

When designing battery backup systems, you should be aware that:

1. As RAM V_{CC} drops, the input logical one should follow so as not to exceed V_{CC} + 0.3 volts.

2. The Enable must be held high at CMOS V_{CC}. Write, Address and data inputs should be held at either GND or CMOS V_{CC} to minimize power dissipation.

3. When exiting from the battery backup mode, V_{CC} should ramp without ringing or discontinuities.

The most common battery backup circuit is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS RAMs. When the system power goes down, diode D1 is reverse biased and only the CMOS RAMs use the battery power. A disadvantage of this method is the diode voltage drop causing the RAM V_{CC} to be lower than the system V_{CC}. There is a possibility that an input to the RAM may be pulled higher than the CMOS V_{CC} and cause latch-up. This problem can be reduced by using a Germanium diode which has a forward drop of about 0.2 volts instead of 0.7 volts.

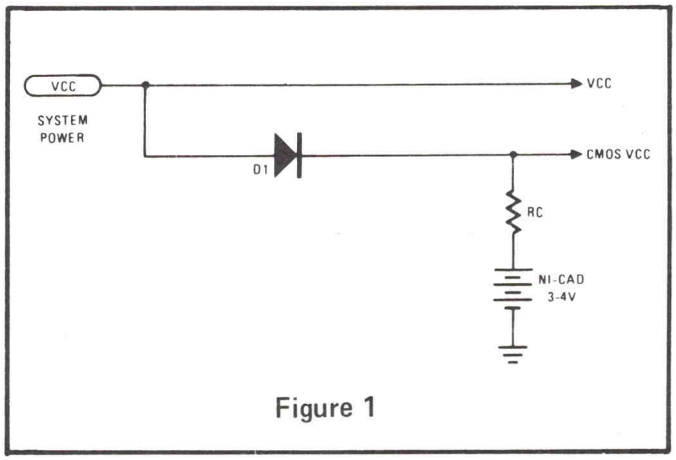

Figure 1

Another circuit is shown in Figure 2. This circuit is recommended by Harris for their parts. A PNP transistor is substituted for the diode in Figure 1. The saturation drop of the transistor (0.2V) is less than the 0.7V drop of the diode, giving more margin against latch-up. A power fail output signal is available to disable the R/W circuitry. Open collector TTL with pullups to CMOS V_{CC} or LS-type TTL should be used as memory drivers. This will ensure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NiCd battery pack is trickle-charged through R_C.

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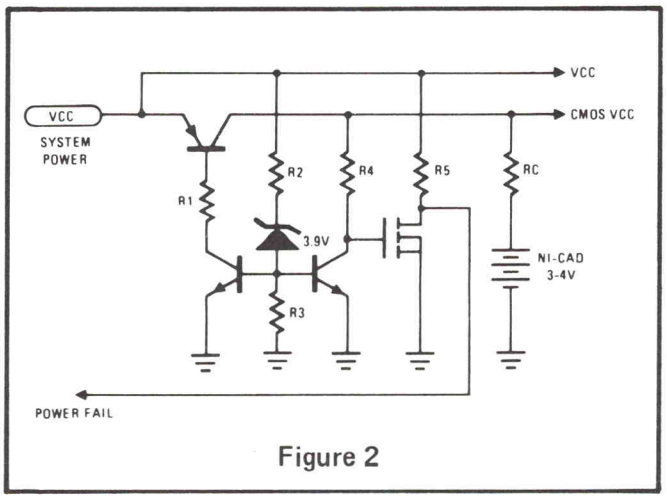

Figure 2

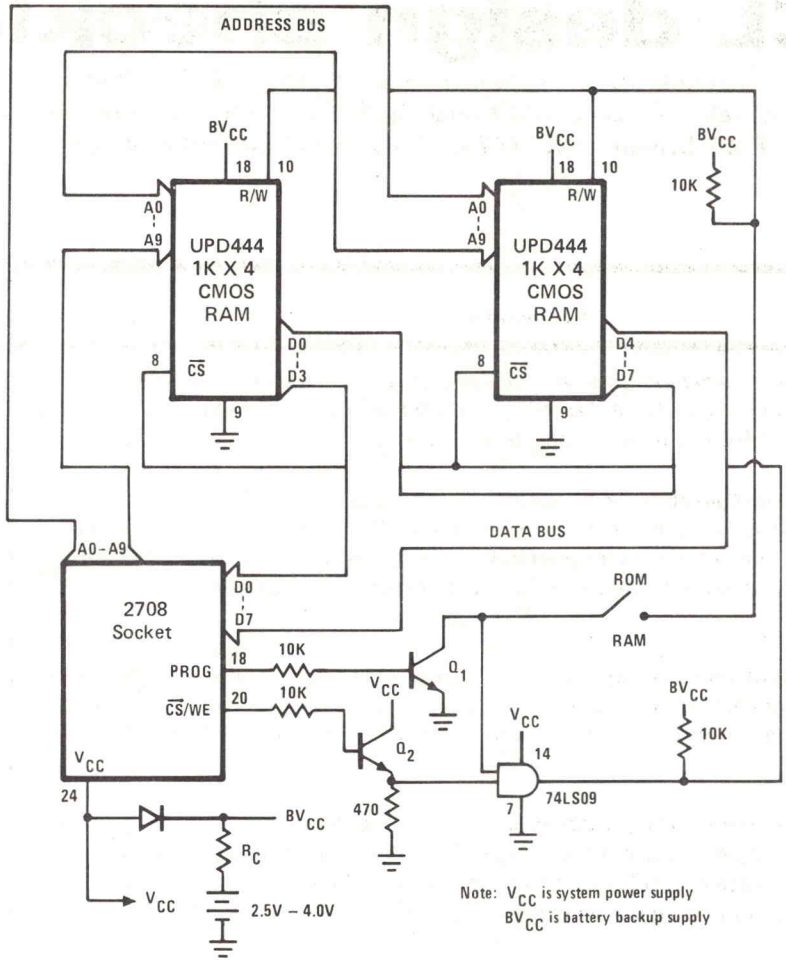

Figure 3 – CMOS replacement for the 2708

A possible use for these RAMs is shown in Figure 3. The circuit is a functional replacement for the industry standard 2708 EPROM. A 2708 replacement can be made by using two UPD 444 1K X 4 RAMs on a small circuit board with a battery and interface circuitry.

The advantage of this replacement is the erase time. The 2708 needs 10 to 20 minutes under an ultraviolet light for erasure. The CMOS RAMs can be immediately rewritten. This can create a considerable time savings in debugging a system.

The circuit is designed to be programmed by any 2708 programmer. Transistors Q_1 and Q_2 are level translators. The programming pulse is 26 volts and the CS/WR is 12 volts. The two 10K pullup resistors are used to deactivate the RAMs in the battery backup mode. The ROM/RAM switch is used to protect against random writes during power down. The simple battery isolation circuit was used here but the other circuit shown in Figure 2 could have been used just as well. R_C sets the charge rate of the battery.

2708 programmers make many passes to complete one full programming cycle. For this circuit the cycles can be reduced to one. There is one precaution that needs to be mentioned, though. The circuit is CMOS and must be treated as a static-sensitive device. This also includes plugging the circuit into a powered-up board or a programmer which does not shut off the power supplies. Four of these parts could be used to replace a 2716 but the Chip Enable and Read/Write circuit would need to be redesigned.

If you have any questions about CMOS design and application, please contact me at 58-125, ext. 7607.

Wilton Hart
Digital Component Engineering

ECL design checklist

The following design checklist for ECL devices is taken from the Government/Industry Data Exchange Program (GIDEP) files at Tek. To access additional GIDEP information (more than 35,000 reports are currently on file), contact **Fred Schade, ext. 7974.** If you have questions about ECL devices, contact **Don VanBeek, ext. 5414.**

Requirement	Yes	No	N/A
1. *Has the fanout been checked?* Both AC limitations and current needed in the transmission line termination can be expected to restrict the system fanout to a smaller number than expected from simplistic considerations.			
2. *Has the wired-OR configuration been used?* When several circuits are connected with wired-OR outputs, a noise spike may be generated on the output if all gates are at a 1 output, and all gates but one are simultaneously changed to a logic 0. The noise spike is due to the one gate suddenly having to source the output current previously supplied by the other circuits.			
3. *Has the correct interconnect wiring been used between devices?* Incorrect selection of conventional interconnect wiring could result in false system operation due to a high percentage of incident pulse reflections and subsequent lowering of the AC noise immunity.			
4. *Is a low-noise power supply being used?* High frequency noise and ripple from the power supply should be avoided because they produce, in effect, differences in voltage levels among sections of a system, and lead to loss of noise margin. It is recommended that high-frequency power supply noise be held below 50 mV.			
5. *Have V_{CC1} and V_{CC2} pins been connected directly to the ground plane as close as possible to the package?* V_{CC1} should equal V_{CC2} for best operation. If V_{CC1} drops below V_{CC2} by more than 200mV, the output devices could saturate and cause propagation delays.			
6. *Are only a few ECL devices used in a predominantly TTL system?* Care must be exercised with both logic families when using this technique to be certain of proper bypassing of the power supply. This prevents coupling of noise between circuit families. The safest method is to use a 0.01μF ceramic capacitor across each ECL device. When larger systems are operated on a common power supply, separate power buses to each logic family help to prevent problems.			
7. *Are double-sided boards used?* A ground plane is recommended on one side of the board. If a ground plane is not possible, a ground bus must be used as part of the layout on the board to provide a low inductance V_{CC} line.			
8. *Have high current devices such as relays, lamps, core drivers been incorporated on the same board as the logic circuits?* These high current circuits should be connected to a separate ground bus on the board and in the backplane.			
9. *Are flip-flops used in the design?* A damping resistor or a combination of series/parallel terminations with microstrip lines is required when driving flip-flops whenever fanouts exceed four and whenever line lengths are greater than three inches.			
10. *Have worst case combinations of driver output and load input characteristics been computed?* A 35% overshoot limit ensures that system speed is not compromised either by saturating an input on overshoot or extending into the threshold region on the following undershoot.			

Has your can kicked the bucket?

Re-forming capacitors extends shelf life

Aluminum electrolytic capacitors (most 290-XXXX-XX P/Ns) are electrochemical devices whose characteristics change with time; both when in use and when sitting on the shelf. This gradual change in the dielectric-electrolyte system gives the capacitor a finite operating life, and a finite (and usually shorter) shelf life.

construction

An electrolytic capacitor is composed of: the metal anode (usually aluminum or tantalum) with an electrochemically-formed oxide layer (Al_2O_3) around it; the absorbent paper spacer and electrolyte; and the metal cathode (see Figure 1). The metal anode is one plate of the capacitor, the aluminum oxide is the dielectric, and the electrolyte is the second plate of the cap. The only function of the metal cathode plate is to serve as a low resistance contact to the electrolyte (which is the actual cathode).

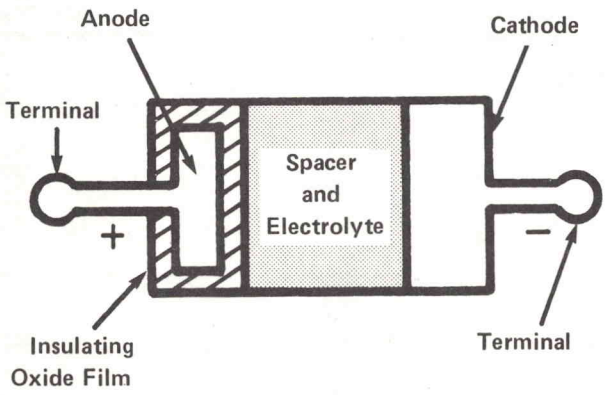

Figure 1 — Polarized electrolytic capacitor

The common method of producing aluminum electrolytic caps is to roll two long strips of thin, very pure aluminum foil into a cylinder, with the absorbent paper separator layer between (see Figure 2). The anode foil has been previously anodized to form the required thickness of aluminum oxide. This assembly is then impregnated with the conductive electrolyte, and assembled in a can with an insulated header to close the can and, hopefully, prevent electrolyte leakage.

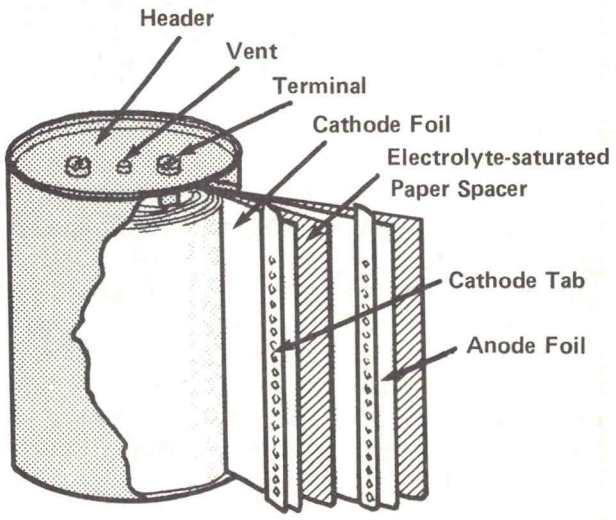

Figure 2 — Construction of electrolytic capacitor

operating life

The operating life of a capacitor is directly influenced by the quality of the header and its seal. This is because the cap is usually considered dead when 50% of its electrolyte is lost due to permeation through the seal, and through disassociation from DC leakage current.

As the capacitor sits on the shelf with no voltage applied, the dielectric slowly degrades. This degradation is exhibited as increased DC leakage current and increased capacitance. The rate of degradation is proportional to time, ambient temperature and the amount of impurities in the aluminum foil and the electrolyte. When voltage is applied to the cap, hydrogen is generated by the reaction:

$$2Al + 3H_2O \xrightarrow{6e^-} Al_2O_3 + 6H^+$$

$$6H \xrightarrow{6e^-} 3H_2 \text{ (gas)}$$

If there has been excessive degradation of the dielectric, the H_2 gas and the temperature rise due to ohmic heating by the excessive leakage current will cause a large internal pressure rise. If this pressure rise is too large, the capacitor will vent its

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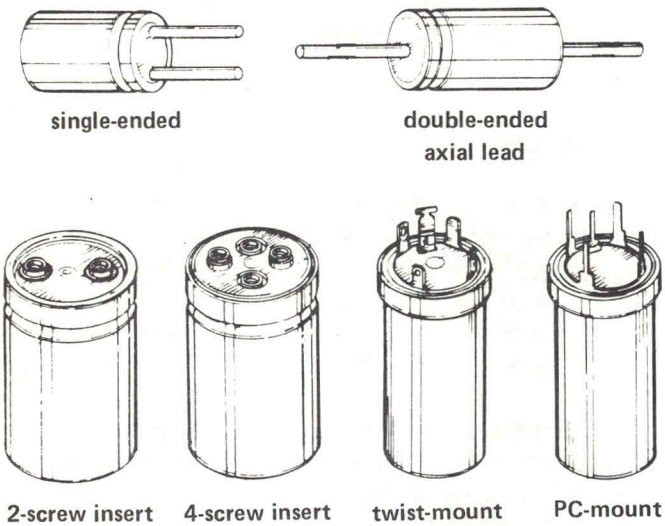
contents, or explode if there is no safety vent. The electrolyte vented by the overpressured capacitor is very conductive and has, on some occasions, shorted-out circuits and caused small fires.

shelf life

The shelf life of aluminum electrolytic capacitors varies from type to type and from manufacturer to manufacturer. A safe rule of thumb to follow is: axial leaded and printed circuit mount caps can be used within two years of the date of manufacture (if stored below 35°C). Computer grade capacitors (screw terminal) should be used within three years. For more specific information, consult the manufacturer's data sheets or contact Component Engineering.



single-ended

double-ended axial lead

2-screw insert

4-screw insert

twist-mount

PC-mount

Most capacitors have a lot date printed on their side or top. For American-made parts this is usually represented by the last two digits of the year followed by the number of the week it was manufactured. Thus, **7914** represents the fourteenth week of 1979.

Some manufacturers use this system: **49(1)**, where "4" is the last digit of the year (1974), "9" is the month (Sept.) and "(1)" is the plant code number. In other cases, **7A** represents the year (1977) and "A" indicates the two-week period (last two weeks in Jan.) in which it was manufactured.

DC leakage check

If a capacitor has been stored without voltage applied for longer than the recommended shelf life, the DC leakage should be checked. If the leakage is within spec it can be used; if not, the capacitor should be re-formed.

To check DC leakage use a variable voltage power supply with a milliammeter and a current-limiting resistor in series with it. Slowly increase the voltage up to full rated working voltage and do not let the current exceed 5mA during charging. If the leakage does not drop below the stated specification within five minutes, the capacitor should be re-formed. The DC leakage specification is usually listed in the Tektronix spec, or it can be obtained from the manufacturer or Component Engineering. The following chart can be used to find an upper limit on leakage, although many cap families have lower leakage limits than those listed.

CV Product	Leakage Current in μA (after 5 minutes)
To 1000	0.05 CV or 5μA whichever is greater
1001 to 250,000	$6\sqrt{CV}\ \mu A$
above 250,000	$6\sqrt{CV}\ \mu A$

C = rated capacitance
V = rated working voltage

re-forming capacitors

Re-forming a capacitor is very similar to performing a leakage check. Slowly raise the voltage to full rated working voltage while ensuring that the current does not exceed 5mA per axial lead or small PC-mount capacitor, or 10mA per large PC-mount or computer grade (threaded terminal) cap.

If the leakage current has not dropped below specification within one hour the capacitor should be discarded.

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Be sure that the capacitor is at room temperature (25°C) before the leakage is checked. If a cap is checked every two or three years it can be left on the shelf for up to ten years. After ten years it should be discarded.

for more information

If you have any questions about this procedure, or for more details about aluminum electrolytic caps in general, please contact me at 58-299, ext. 5415.

Don Anderson
Optoelectronic & Passive Component Engineering

Fuse voltage drop evaluated

Since the announcement in last month's **Component News** that I will be handling the evaluation of fuses, several new problems have come my way. I am giving attention to the problem of fuse voltage drop at rated load, and fuse wearout under repeated starting surges.

For example, on the 1/16 ampere 159-0024-00, units from Littelfuse have exhibited a 0.35 to 0.50 volt drop at 90% of rated current, whereas fuses from Bussman are showing a 3.0 to 3.4 volt drop. The Bussman fuse, though, is more sturdy and has shown a significantly lower failure rate than Littelfuse units. We currently show Littelfuse as the main source, with Bussman as the emergency source for these fuses.

We believe that reduced field failure rates are possible if we reverse this policy, making Bussman the primary source. But, would the increased voltage drop cause trouble for some instrument lines? Also, should we begin specifying voltage drop on our fuses?

In trying to answer these questions, we've found that one type of fuse has a symmetrical distribution of voltage drops about the mean value, but with a distinct hole in the center of the distribution. We are considering the significance of this, as well.

If you have an interest in this situation, we have a surge tester in our area which is very convenient for recording the starting surge current on an instrument. The surge tester can also be used as a preliminary tool for fuse selection. If you would like to borrow the tester, call me on ext. 5953.

Also, please contact me if you have comments about the source designation on these fuses (159-0024-00), or about specifying voltage drops on fuses.

Dennis Johnson

Product Safety/Standards relocates

To relieve the pressure for increased manufacturing space in Building 58, part of the Product Safety/Standards group has moved to Town Center. Pete Perkins and the Safety/Standards staff are located at delivery station 41-400. The Product Safety Technical Support group, under Dick Griffin, and Rich Nute (Corporate Product Safety Engineer) are also located at 41-400. The Technical Standards group, managed by Chuck Sullivan, can be reached at delivery station 41-260.

Here's a list of new phone extensions for these groups:

- Pete Perkins (Product Safety/Standards manager) ext. 256
- Dick Griffin (Technical Support group) ext. 253
- Rich Nute (Corporate Product Safety Engineer) ext. 255
- Chuck Sullivan (Technical Standards group) ext. 241

Product Safety activities are continuing at each Tek operating site. Wally House (58-123, ext. 7192) is leading Product Safety Engineering in Beaverton; Bob Crawford (60-222, ext. 2269) is responsible for activities in Wilsonville; and George Clark (92-835, ext. 1563) is leading Walker Road Product Safety Engineering.

Pete Perkins

New style resistor available

Do you need a low-cost resistor to replace the 1/8-watt carbon composition part? You might consider using 1/8-watt carbon film resistors; tests have shown they are superior to most carbon composition part specifications.

Here's a comparison of the two part types:

Parameter	Carbon Film	Carbon composition
Wattage	1/8W	1/8W
Voltage rating	150V	150V
Overload	300V	300V
Resistance range	1 Ω to 220 KΩ	1 Ω to 100 MΩ
Temperature coefficient		(+55°C) (+105°C)
under 10Ω	+300,0	+267,–200 +375,–75
10Ω to 1KΩ	0, –300	+333,–267 +500,–100
1.1KΩ to 100KΩ	0, –500	+433,–333 +625,–125
110KΩ to 220KΩ	0, –700	+600,–467 +888,–467
Short time overload (2.5 X rated voltage; 5 sec.)	±1.0%	±2.5%
Terminal strength (pull 1 Kg; 10 sec.)	±1.0%	±1.0%
Temperature cycle	±1.0%	±2.0%
(5 cycles)	(–55°C to 130°C)	(–55°C to 85°C)
Dielectric withstand (V-block test; 1 min.)	300V	300V
Insulation resistance (100V; 1 min.)	10^4 MΩ	10^4 MΩ
Pulse rating (4 X rated voltage, 1 sec; 10,000 times)	±0.75%	not rated
Solder effect	±1.0%	±2.0%
	(270°C, 10 sec; 350°C, 3 sec.)	(250°C, 10 sec.)
Load life (1000 hrs. at 70°C; 90 min. on, 30 min. off)	±5%	+4%, –6%
Moisture	±5%	+8% average, 11% max.
Moisture load life	±5%	not specified
(40°C, 95% RH, 1000 hrs; plus load life)		
Storage (25°C for 24 months)	±1.0%	not specified
Voltage coefficient	–25 ppm / V	10 KΩ –200 ppm / V
		100 KΩ –300 ppm / V
		1 MΩ –450 ppm / V
Low temperature operation	±1%	±2%
Noise –		
under 56 KΩ	0.5 μV / V	
56K to 470 KΩ	1.0 μV / V	not specified
above 470 KΩ	1.5 μV / V	

The dimensions of the body diameter and length, and the lead diameter and length, are the same for both part types.

The carbon film resistor will not be used as an alternate for any 317-series parts. Also, if you plan to use any carbon film parts for production, a new part number must be assigned.

For more information on these resistors, or if you'd like some samples for testing, contact **Ray Powell (58-299), ext. 6520.** For information on the carbon composition supply situation, reference **Component News 270,** page 11.

Part II in a series

Using the 9914 as a controller

Editor's note: This is the second in a series of articles on the 9914 GPIB chip. In the last issue, the 9914 interrupt structure was analyzed; this article covers the 9914 controller functions.

The 9914 may function either as System Controller or non-System Controller. The System Controller Active state is resident entirely in firmware. A System Controller instrument may use the 'sic' (Send Interface Clear) or 'sre' (Send Remote Enable); others may not. In addition, the companion transceiver will have the direction control for REN and IFC provided from off-chip, so an erroneous use of one of the commands will not adversely affect the GPIB.

System controllers

When the 'sic' command is used, the 9914 asserts IFC true, and on finding ATN false as an input, sets CONTROLLER, ATN, and Talk Enable true. Firmware must assure that IFC is held true for greater than 100 μS before the use of 'sicf' (send Interface Clear false).

When Talk Enable becomes true, the chip is effectively in CACS (Controller Active State); the Source Handshake function is active and the 'BO' interrupt is set true. Remote Messages are simply written to the data-out register.

System and non-system controllers

To release ATN, the 'gts' (go to standby) command is used. ATN will become false immediately. There are three possibilities here: go to standby as a talker, a non-participant, or as a listener. To become a non-participant, the 'gts' command is used alone. To become a talker, the instrument should first source to the GPIB its own primary talk address in order to ensure that other talkers are off the bus. Then the 'ton' (talk only) command is used, and finally the 'gts' command. The device immediately enters CSBS and TACS and generates a 'BO' interrupt.

The controller may address itself to listen by use of the 'lon' (listen only) command before using 'gts,' and it may participate in the Acceptor Handshake by either inputting bytes through the data-in register or via a shadow handshake. In both cases, the 'hlde' (hold on END) command may be used, with the END interrupt being generated at the termination of the process; control may be regained synchronously via 'tcs' because the handshake is held in ANRS due to the 'hlde' command.

To grab the bus while a process is in progress, the 'tcs' (take control synchronously) command may be used. The 9914 will wait until the AH function reaches ANRS before asserting ATN; TE will delay for eight clock cycles before going active in order to allow the bus time to recognize ATN true before DAV is allowed to go true. On the other hand, 'tca' (take control asynchronously) may be used, in which case ATN is asserted independent of the AH function, with TE being delayed as in the case of 'tcs.'

Passing control

From the Controller Active State, the 9914 will source the Talk address of the new controller and the TCT message, and upon receipt of 'BO' will have the 'rlc' command issued to it by the microprocessor. Talk Enable, CONTROLLER and ATN will go false immediately upon receipt of 'rlc.'

To have control passed to the 9914, the UACG function must be enabled. The receipt of MTA followed by TCT (Take Control) will raise the UACG interrupt. The microprocessor should respond by issuing the 'rqc' command, then the 'dacr' (Data Accepted Release) command. When ATN is detected false as an input, the 9914 will set CONTROLLER and ATN true as outputs, with TE going true immediately as in the case of taking control via sending IFC.

General comments on the 9914 as a controller

The 'BO' interrupt is set true on entry into CACS. It is cleared only by reading the interrupt status register or by writing to the data out register. Thus, the chip gives 'BO' as a response to 'sic,' which moves the device from CIDS or CSBS to CACS; 'tca' and 'tcs,' which move the chip from CSBS to CACS; and 'rppf' (Set Request Parallel Poll False), which moves the interface from CPPS to CACS.

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The 'BO' interrupt is also set while in CACS on output of data, and therefore is the mechanism by which the firmware knows that each procedure is finished. DMA requests are not issued while in CACS, so all remote messages are transferred out via software.

Once set, the $\overline{\text{DMARQ}}$ line remains asserted until the data out register is written to or read from. This means that the DMA controller's disable bit must be used to shut off DMA. It is also conceivable that a situation could arise in which $\overline{\text{DMARQ}}$ would be asserted following the last data byte out and would remain asserted through the first 'BI' interrupt. A DMAC which is edge sensitive on $\overline{\text{DMARQ}}$ may not be able to function with the 9914.

There is a final note about using the 9914 as a controller. Because the Talk Enable pin is high while sourcing Device Dependent data while in CSBS, there is no way for the 9914 to freeze the bus Acceptor Handshake in ANRS in order to execute a 'take-control-synchronously' operation.

In general, the ATN line will be asserted true while the bus AH function is in ACRS, which is an asynchronous take-control operation. However, this should have no ill effect because ATN will be asserted while DAV is false. It is necessary to use the 'tca' command, rather than 'tcs,' following the 'BO' interrupt for the last byte in order to take control after sourcing device dependent data.

Initialization procedures

Neither the $\overline{\text{RESET}}$ (pin 19) input nor the 'srst' command is able to completely initialize the device. It seems that the hardware reset will clear each c/s bit of each software command but will not enable the device to come alive after power up. The 'srst' command, on the other hand, will not affect the state of the c/s bit for most (any?) of the auxiliary commands, but will make the device responsive.

A complete initialization should include a provision for having the software set or clear the c/s bits for **interface clear, parallel poll,** and **remote enable** (i.e. use: 'sic,' 'sre,' 'rpp') in addition to using the software reset and to writing the bus address into the chip. A careful initialization procedure will be helpful during system debug to ensure that a talker/listener doesn't turn itself into a controller.

Problem areas

Polled software If a Read Int Reg occurs during a four clock cycle window following DAV, it is possible that the read pulse will be narrower

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9914 Read Registers

Address			Register	Contents							
RS2	RS1	RS0	Name	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	INT STATUS 0	INT0	INT1	B1	B0	END	SPAS	RLC	MAC*
0	0	1	INT STATUS 1	GET	UUCG	UACG	APT	DCAS	MA*	SRQ	IFC
0	1	0	ADDRESS STATUS	REM	LLO	ATN	LPAS	TPAS	LADS	TADS	ulpa
0	1	1	BUS STATUS	ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN
1	0	0	ADDRESS SWITCH 1)	edpa	dal	dat	A5	A4	A3	A2	A1
1	1	0	CMD PASS THRGH	D108	D107	D106	D105	D104	D103	D102	D101
1	1	1	DATA IN	D108	D107	D106	D105	D104	D103	D102	D101

* Disabled on APT

Note: This register is external to the TMS 9914 and will consist of a DIL switch at the rear of the instrument.

9914 Write Registers

Address			Register	Contents							
RS2	RS1	RS0	Name	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	INT MASK 0	X	X	BI	BO	END	SPAS	RLC	MAC
0	0	1	INT MASK 1	GET	UUCG	UACG	APT	DCAS	MA	SRQ	IFC
0	1	1	AUXILIARY CMMD	c/s	x	x	f4	f3	f2	f1	f0
1	0	0	ADDRESS REG	edpa	dal	dat	A5	A4	A3	A2	A1
1	0	1	SERIAL POLL	S8	RSV	S6	S5	S4	S3	S2	S1
1	1	0	PARALLEL POLL	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1
1	1	1	DATA OUT	D108	D107	D106	D105	D104	D103	D102	D101

than the internal pulse used to set the interrupt bit; therefore, the Read will not clear the register as it should. Five of the interrupt bits known to be affected are interrupts for functions which **freeze** the AH function in **ACDS**; therefore, the microprocessor may re-read the Int Reg upon finding one of these five bits set, which will guarantee that the bit will be cleared. There is no risk in this operation because the bus is stopped and no new interrupts can arise. However, the 'MAC' bit will not cause hold-off in ACDS, which means that a second read of the register may contain new information which instrument firmware must take into account.

When using minimum Data-In Times, which may occur when interfacing to 6800 systems, 'rsv' may be written to the wrong state during the front end of the write cycle. Other write bits and commands are strobed-in at the back end of the write cycle and will most likely not exhibit this problem. The prognosis for this problem is that an additional latch could be added into which 'rsv' could be strobed at the end of the write cycle, and that the chip layout involved will not be excessively difficult to modify.

The problem will exhibit itself to the user when the user is attempting to write to the other bits in the Serial Poll Register (i.e. 'busy' or 'error'), but is **not** attempting to **change** the present state of 'rsv.' Two cases are possible: (1) if 'rsv' is 'zero' and is being written to 'zero,' it may be erroneously pulsed to 'one' before being left at zero, which may pulse the SRQ line momentarily true; (2) if 'rsv' is one and is being written to 'one,' 'rsv' may be momentarily set to zero before being left at one; the effect of this has already been shown on the tester to cause a movement through the SR function which would cause SRQ to be left true. This second case may be avoided through proper software; i.e., don't change the status byte while 'rsv' is true. The first case may cause a glitch on the SRQ line, the effects of which would depend upon the controller involved.

In addition, the 9914 does not correctly implement the R-L function when secondary addressing is enabled. The 9914 is in accord with the 1975 version but not the 1978 version of IEEE-488.

When secondary addressing is enabled, the transition from LOCS to REMS is on $\overline{\text{rtl}} \wedge \textcircled{\text{ACDS}} \wedge \text{MSA} \wedge \textcircled{\text{LPAS}} \wedge \text{REN}$. The 9914 makes the transition on $\overline{\text{rtl}} \wedge \text{MLA} \wedge \textcircled{\text{ACDS}} \wedge \text{REN}$.

Because the REN line is brought to the microprocessor interface, it should be possible to handle the R-L function in software, when secondary addressing is enabled, in the following manner: (1) initialize with RLC masked; (2) on APT interrupt, check the state of REN; if MSA and REN are true, set software REM bit and enable RLC interrupt; (3) on RLC interrupt, clear REM status bit and mask RLC interrupt.

Two other problems have recently been uncovered with the T.I. 9914 GPIB chip. Carl Hovey of TM500 found that it is possible to change the GPIB bus data in Serial Poll Active State (SPAS) and Source Transfer State (STRS) by writing to the serial poll register. Bus data is not supposed to change during STRS. There is no way to detect the fact that the chip is in SPAS or to prevent its entry into SPAS in order to guarantee that a write to register 5 will not occur during a Serial Poll.

An even more serious variation of this problem is the case where the 'rsv' message is taken from false to true during SPAS. Whenever 'rsv' is used, the firmware should immediately check the state of the SRQ line to ensure as much as is possible that the device entered SRQS. The problems associated with using the Serial Poll register must be corrected if we are to use the 9914.

Dennis Smith and the AICE group have revealed a problem with the 9914 while listening to a fast talker in 'hdfa' mode. This is a mode where the AH function holds in ANRS after each byte. If the talker is ready to source a new byte and its 'T2' time has already passed, then when the 9914 allows NRFD to go false by using the 'rfdr' command, DAV may go true immediately. If DAV goes true within two clock (pin 18 of 9914) periods of NRFD going false, the next byte put on the bus is lost. This problem may be **minimized**, but not in principle eliminated, by using a 5 MHz clock.

continued on page 12

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It can, however, be eliminated by replacing in software the 'rfdr' command with the following sequence of events:

a) clear 'hdfa' (or 'hdfe') mode
b) read Data-In register (Reg. 7)
c) set 'hdfa' (or 'hdfe') mode

Even with a slow clock (6800 Φ2) and a fast talker, this sequence will cure the byte loss problem. The sequence should also be used for the 'hdfe' mode or at any time the 'rfdr' would have been used.

A final application note is to use the microprocessor data bus in the reverse bit order relative to TI's nomenclature so that the least significant processor data bit corresponds to the least significant GPIB data bit.

Conclusion

This device appears to be the most completely functional GPIB chip available today. I am confident that the simplicity of the design will greatly ease the firmware design task.

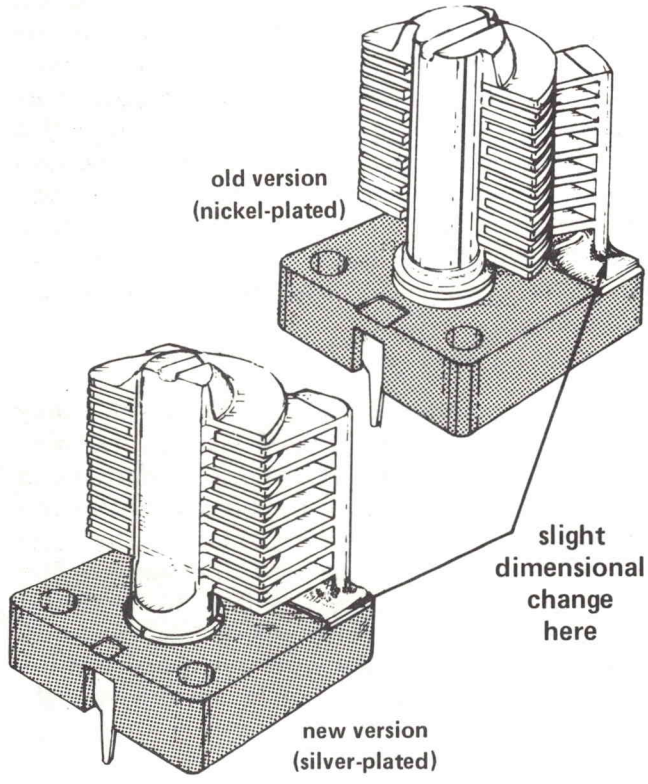
Jim Howe, ext. 6303
Digital Component Engineering

Air variable caps single-sourced

We have recently become single-sourced on all miniature air variable capacitors. To compound this situation, most of our part numbers call for nickel plating, and our only source can no longer produce nickel-plated parts.

Therefore, the parts we receive in the future will be standard, machine-built silver-plated parts. The silver-plated capacitors will be electrically equivalent to the nickel-plated parts, but some part numbers will have a slight dimensional change. This is because the machine-built part has a wider radius than the hand-built nickel-plated parts (see illustration).

Please note that the wide radius parts will still be within our specifications; the ceramic base and the lead dimensions will *not* be affected, only the rotor and stator dimensions may change.



Part numbers 281-0081-00 and 281-0153-00 were changed to the machine-built silver-plated parts some time ago, and the rest of the part-numbered capacitors will be changed when the supply of nickel-plated parts is depleted.

Below is a list of the part numbers affected by this change:

281-0076-00	281-0116-00
281-0098-00	281-0079-00
281-0159-00	281-0101-00
281-0168-00	281-0080-00
281-0114-00	281-0102-00
281-0077-00	281-0117-00
281-0099-00	281-0198-00
281-0209-00	281-0103-00
281-0078-00	281-0166-00
281-0100-00	281-0131-00
281-0115-00	281-0111-00

If you have any questions about these parts, contact **Alan LaValle (58-299), ext. 5415.**

COMPONENT CHECKLIST

The "Component Checklist" is intended to draw attention to problems or changes that affect circuit design. This listing includes: catalog and spec changes or discrepancies; availability and price changes; production problems; design recommendations; and notification of when and how problems were solved. For those problems of a continuing nature, periodic reminders with additional details will be included as needed.

	Tek P/N	Vendor	Description of Part	Who to Contact, ext.
✓	156-1246-00	Motorola	MC68488 GPIB	Jim Howe, 6303

When the 68488 is in SPAS and STRS, it is possible to change the contents of the GPIB Data Bus by simply writing to the Serial Poll register, R-5-W.

The GPIB Data Bus is required to remain unchanged during STRS. Because it is not possible to guarantee from the microprocessor side that the chip is not in SPAS, there is a possibility that updating the Serial Poll status byte will disturb a status byte transfer which is simultaneously taking place.

✓	151-0292-00 151-0367-00	Texas Instruments	Transistor	Matt Porter, 7461

Texas Instruments is temporarily unable to deliver these parts without relaxation of H_{fe}. The following relaxations are in effect:

156-0292-00 $H_{fe} \geq 10$, relaxed to $H_{fe} \geq 6$ (at 25V, 5mA)
$H_{fe} \geq 35$, relaxed to $H_{fe} \geq 30$ (at 25V, 100mA)
The relaxed parts will be marked "X-292"

156-0367-00 H_{fe} 100-300, relaxed to $H_{fe} \geq 75$ (at 6V, 5mA)
The relaxed parts will be marked "KX-367"

Z-80 instructions clarified

The following information pertains to the Z-80 microprocessor (Tek P/N 156-0983-XX).

The instructions LR A,I and LR A,R should copy the status of IFF2 into the parity bit of status register F. The status is copied correctly except when an interrupt occurs simultaneously with the execution of those instructions. In this case, a zero is always copied into the parity status of IFF2.

If interrupts are spaced properly this problem can be overcome by performing the load and test twice; then, if either test is positive, assume IFF2 was a one.

There is also a minor problem with the block transfer instructions INI, INIR, IND, INDR, OUTI, OTIR, OUTD and OTDR. According to all documentation, these instructions are not supposed to affect the carry flag. However, the carry flag will be set or reset according to the contents of the L register, C register, and the memory location pointed to by the HL register pair.

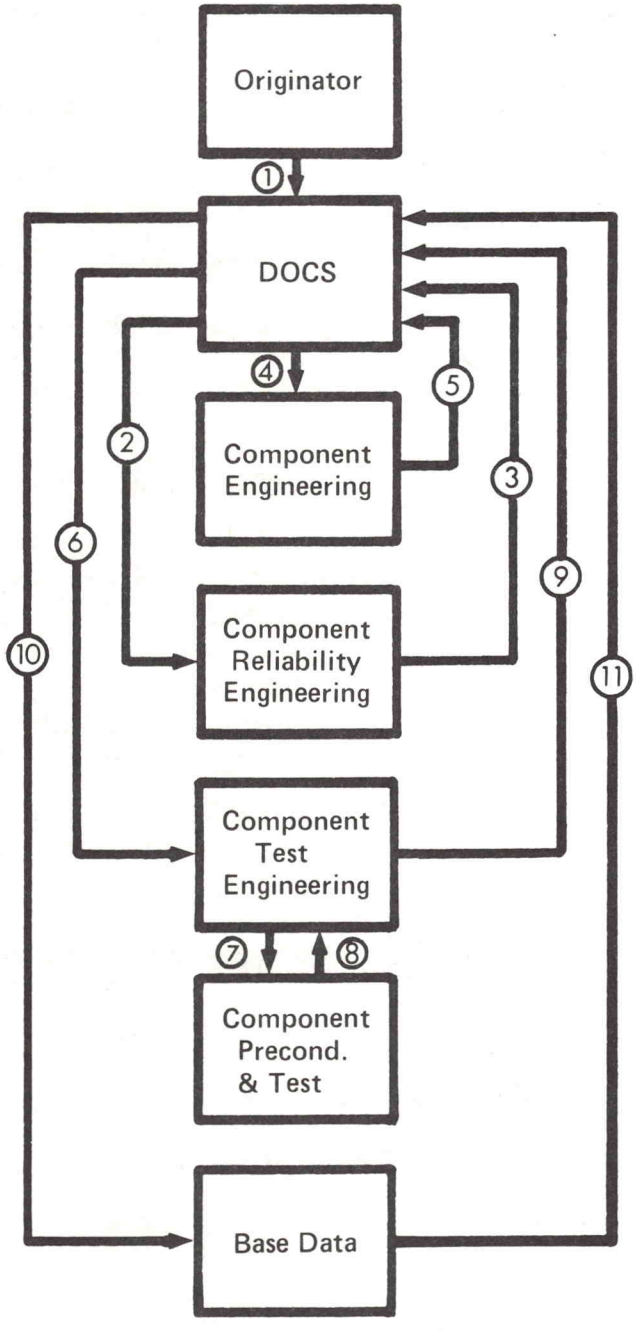
For the OUT instructions, the carry bit will be set if the L register plus the contents of memory location pointed to by HL, exceeds $\emptyset FF_H$ and reset otherwise. For the IN instructions, the carry bit will be set if the contents of the C register exceeds $5\emptyset_H$ and reset otherwise.

Don Kirkpatrick
58-098, ext. 6959

DOCS initiates "Processing Request" form

To aid in processing requests for burn-in/screened components, the DOCS (documentation coordination) group has initiated a "Processing Request" form. This form must be completed before any testing procedures can be implemented.

Here is the documentation flow for this new procedure:



① PPIF to DOCS

② PPIF from DOCS to Reliability Engineering. (Reliability Engineering will aid the originator in filling out a processing request form)

③ PPIF, with Processing Request form attached, returned to DOCS

④ PPIF and Processing Request form logged to Component Engineering (CE)

⑤ PPIF and Processing Request form returned from CE to DOCS

⑥ PPIF and Processing Request form logged to Component Test Engineering (CTE)

⑦ CTE will furnish test program to Component Preconditioning and Test

⑧ Component Preconditioning and Test will notify CTE when test is implemented

⑨ Completed PPIF and Processing Request returned to DOCS when procedure is implemented (Note: If request cannot be implemented within ten working days, a photocopy of the request will be returned to DOCS with the date the request will be implemented. DOCS will copy originator and Prototype Support. The PPIF and completed form will be held by CTE until the process is complete.)

⑩ DOCS will log and deliver to Base Data completed PPIF and copy of request form

⑪ DOCS will distribute completed request form after a part number has been assigned by Base Data.

If you have any questions about this new procedure, please contact **Dorothy Peterson, (58-299), ext. 6336.**

ComponentNewsNewComponents

This column is designed to provide timely information regarding new components, vendors, availability and price. "New Components" can also be used as an informal update to the Common Design Parts Catalogs. Samples may or may not be available in Engineering Stock.

Vendor	No.	Description	When available	Tek P/N	Approx. cost	Engineer to contact
		analog devices				
National	LF3520	Amplifier, FET input, instrumentation	now	no P/N	$ 2.50	John Hereford, 6700
Intersil	ICL760X	Amplifier, commutating auto-zero, 2μV offset, low drift, CMOS	now	no P/N	5.00 to 15.00	John Hereford, 6700
Intersil	ICL761X	Op amp, low power (10μW), low voltage (1V), CMOS	now	no P/N	0.75	John Hereford, 6700
National	LM359	Op amp, current mode (Norton), 300 MHz, G.B.W. product at A_V = 10, dual	now	no P/N	1.00	John Hereford, 6700
Plessey	SP9865	Comparator, 3 nS delay, compatible with AM685	now	156-1344-00	5.00	John Hereford, 6700
National	92PU01A	Transistor, NPN, TO-92+ high-current (2A), medium power, amplifier/switch	now	no P/N	0.40	Matt Porter, 7461
CTC	CTC3921	Transistor chip, RF, similar to 151-0494-00	now	151-0709-00	5.50	Matt Porter, 7461
RCA	CA3096AF	Transistor, NPN/PNP array, two PNP transistors and 3 NPN transistors, all individually connected, general purpose, 300 MHz NPNs, 2 MHz PNPs	now	no P/N	100.00	Matt Porter, 7461
		digital devices				
Motorola	MC14555	Decoder/demultiplexer, dual binary to 1 - of - 4	now	156-1368-00	--	Wilton Hart, 7607
		memory and I/O devices				
T.I.	74S472	PROM, 512 X 8, tri-state TTL, 20-pin cer.	--	156-1352-00	--	Gene Stout, 6003
Signetics	2632	ROM, 32768 bit static MOS ROM, 24-pin	--	062-4172-00	--	Gene Stout, 6003
		optoelectronic and passive devices				
Monsanto	MV53124	LED, discrete, yellow rectangular	--	150-1073-00		Betty Anderson, 6389
H-P	5082-7616	LED display, overflow, universal polarity, high efficiency, red	--	no P/N	1.85	Betty Anderson, 6389
TRW	X363UW	Capacitor, dielectric, 4μF ±10%, 200V metallized polypropylene, 3 A RMS ripple current	now	285-1203-00	--	Don Anderson, 5415
Mallory	CGR262U-035R2C3P	Capacitor, 2600 μF,35V, aluminum electrolytic, 5.8 A RMS ripple current, replacement for 290-0754-00 stacked foil capacitor	--	290-0898-00	--	Don Anderson, 5415
Dale	CMF110-216G485ROD	Resistor, metal film, – 485Ω 0.5% to 1/8W	July 1	321-0708-01	0.03	Ray Powell, 6520
TRW-IRC	CFA1.05M-Ω1% to 1/8W	Resistor, metal film,	July 1	321-0483-00	0.12	Ray Powell, 6520
Dale	CMF110-216G52302F	Resistor, metal film, – 523K Ω1% to 1/8W	July 1	321-0454-00	0.03	Ray Powell, 6520
Dale,AB Bourns	MSPO8A-01560	Resistor network, SIP, 8-pin, 4–56Ω ±2%	July 1	307-0677-00	0.25	Ray Powell, 6520
Allen Bradley	--	Panel Control, 75 KΩ Lin. Pot, Cermet, w/2 Rot. Sw., both DPST, 1-open/1-closed contacts, lug term.	--	311-2070-00	3.50	Gene Single, 5302

announcements

responsibilities in Opto/Passive group

The following responsibility changes have been instituted in the Optoelectronic and Passive Component Engineering group:

Ray Powell (ext. 6520) is now responsible for ceramic capacitor evaluation and support, in addition to evaluating resistors;

Alan LaValle (ext. 5415) is responsible for all variable capacitor and mica capacitor evaluation and support activities, including resistive trimmers;

Harry Ford (ext. 6520) will devote full time to developing test and evaluation capabilities for purchased monitors, CRTs and related components.

Please direct your inquiries to Ray, Alan or Harry if you have questions regarding these components.

Paul Curley, manager
Optoelectronic & Passive CE group

vendor P/N suffix list compiled

A table showing manufacturer part number suffixes for major suppliers of digital microcircuits is now available. The table also reflects Tek's current marking requirements for reliability-screened digital microcircuits in both plastic and ceramic packages.

An up-to-date copy of this listing is available from **Yvonne Brinck (58-125).**

new data books received

We have received a large shipment of AMI's *Winter 1979 MOS Products Catalog.* These books will be distributed on a first-come, first-served basis – if you want a copy, drop by 58-299 as soon as possible. If you're at Walker Road, Wilsonville, Vancouver, or other locations outside Beaverton, you may order this book by writing to Lola Janes, 58-299. No phone calls, please!

CRE moves to Walker Road

Component Reliability Engineering has moved from Building 58 to Walker Road (92). The new delivery station is 92-336. New phone extensions are: Ron Schwartz (manager), ext. 1991; Art Fraser and Steve Hui, ext. 1995; Barbara Hutchens and Lynn Kung, ext. 1993; Larry Meneghin, ext. 1994; Norm Sanneman, ext. 1996; Gunhild Feuchert, ext. 1992.

Bill Snell
Reliability Engineering and Modified Products

correction

Component News 270 (page 5) reported on some sealed rocker switches which were recently part-numbered. Unfortunately, the part numbers we listed were juxtaposed. Here are the correct part numbers: 260-1827-00, 5-wide; 260-1589-00, 6-wide; 260-1721-00, 8-wide.

Please contact Joe Joncas (ext. 6365) if you have any questions.

component news

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