Conditioning an External Clock For Use With The 92SX109 and 92SX118

The 92SX109 and 92SX118 are 100 MHz pattern generation subsystems available for the 9200 Series Digital Analysis System (DAS9200). These subsystems can be operated from either an internal timebase or external, user supplied clock. An external clock must be accurately controlled and meet very specific requirements. This Application Note has been written to reduce the potential restriction imposed by these requirements when using a signal from the system under test (SUT) as the source of this clock. If you are using a pulse generator as the external clock, the issues discussed in this Application Note will offer useful but less applicable information.

DESCRIPTION

The 92SX109 and 92SX118 are based on enhanced, re-calibrated 92S16 and 92S32 pattern generator cards respectively. The 92S16/S32 operate to a maximum of 50 MHz. Each 92SX109/SX118 subsystem is composed of a pattern generator card, output data multiplexer(s), and P6464 output data probe(s). The 92SX109/SX118 provide twice the operating speed and double the memory depth of the 92S16/S32 in part by reducing the number of channels by half.

EXTERNAL CLOCK REQUIREMENTS

The 92SX109/SX118 require a well controlled source when operated from an external clock. This waveform must exhibit the following characteristics:

- One half the desired output clock rate
- 50% duty cycle[1]
- Edge jitter less than 100 ps
- 600 mV or greater amplitude[2]
- 0.20 V/ns or greater Slew Rate

The 92SX109 and 92SX118 are clocked on both edges of the clock source. This is the reason for the half speed and 50% duty cycle requirements.

[1] The maximum high time of the clock waveform is typically: (clock period/2 + 1.0 ns). The maximum low time of the clock waveform is typically: (clock period/2 – 2.0 ns).

[2] The 92SX109 offers a fixed TTL, fixed ECL, and variable threshold for the external clock input. The 92SX118 provides a fixed TTL input only.

THE TECHNIQUE

We will be using a divide-by-two flip-flop to generate an external clock to meet the requirements stated previously. The output waveform of the Clock Conditioning Circuit will have a 50% duty cycle and be half the rate of the input signal because we are using a flip-flop.

THE PROCEDURE

The selection of an external clock source is critical to your success in using the 100 MHz pattern generators. Any period jitter on the clock source will generate period jitter on the pattern generator's output clock and data. Therefore you need to select a clock source with good rise/fall times, amplitude, and minimum jitter. If possible select a clock driver from the SUT as the source. This will reduce any additional loading that the clock source might see. Better yet would be an unused clock driver output.

For this Application Note we "piggy-backed" a flip-flop appropriate for the logic family of our system (TTL, ECL, CMOS, etc). Alternatively, you could build the circuit on a section of vector board. This would make the clock conditioning circuit more of a universal adaptor. If you are going to "piggy-back" ICs, be sure to leave an air gap between them so they won't overheat. This is especially important with ECL logic.

There are special considerations if you are using a 92SX118 rather than a 92SX109. Review the section *Sourcing The External Clock For The 92SX118* before proceeding.

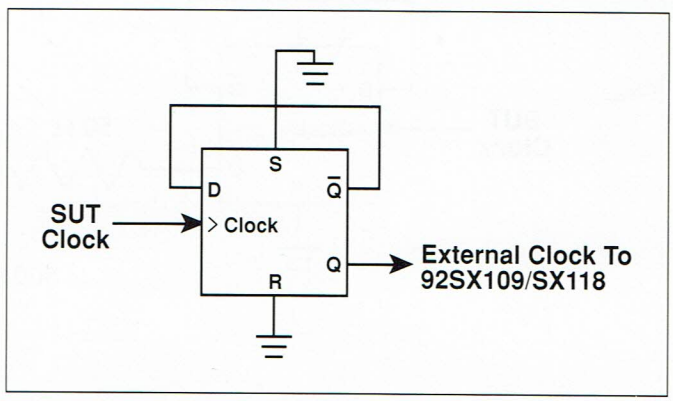

Figure 1 — Divide-by-Two Flip-Flop; The Clock Conditioning Circuit.

Tektronix®
COMMITTED TO EXCELLENCE

Wire the flip-flop's clock input pin to the selected clock source of the SUT. Connect the device's Q-bar (Q/) output to it's D-input. Then wire the Set & Reset inputs inactive; pulled high or low depending on the technology and specific device you are using. The Q-output of the flip-flop will drive the external clock input of the 92SX109/SX118. The output of the Clock Conditioning Circuit will produce a waveform suitable for driving the pattern generator subsystems.

Note that TTL parts have unequal rising vs. falling delays. This will cause some pulse shaving. The 92SX109 and 92SX118 can accept an external clock that has a rising pulse width 1 ns greater than the required 50% duty cycle and the falling pulse width can be 2 ns greater than 50%. If the positive pulse width from the divider is too big, the polarity of the external clock can be inverted by reprogramming the 92SX109/SX118 clock input in the pattern generator's Config menu. If this is not sufficient, a 300 Ω pull-down resistor can be added as outlined in the section *Sourcing The External Clock For The 92SX118*.

SOURCING THE EXTERNAL CLOCK FOR THE 92SX109

The external clock input of the 92SX109 is located on the P6460 External Control probe. This input offers fixed TTL and ECL as well as a variable threshold. Connect the external clock input lead of the P6460 to the output of the Clock Conditioning Circuit. For input frequencies greater than 25 MHz, the 5" leadset and both grounds should be used. In especially noisy environments, it may help to twist the clock and ground wires together.

SOURCING THE EXTERNAL CLOCK FOR THE 92SX118

The 92SX118 requires an external clock that is TTL compatible and capable of driving a 50 Ω, unterminated environment. This source can be provided by placing a 50 Ω resistor in series between the Q output of the divide-by-two flip-flop and a length of 50 Ω coax connected to the 92SX118 external clock input.[3] This represents a back, or series termination (Figure 2). Note that most TTL flip-flops can drive a 50 Ω, unterminated line. Under worst case conditions, however, an additional line driver or a parallel driver[4] may be required. The coax is not terminated at the 92SXS118's clock input. To reduce pulse shaving at 1.4 V (the 92SX118's external clock input threshold), a 300 Ω pull-down is added as shown in Figure 2.

The Clock Conditioning Circuit for the 92SX118 should use a 74F74 or 74AS74 TTL flip-flop (even if the SUT signal is CMOS) in order to maintain the required TTL input levels.

If the signal chosen as the external clock is ECL, then the flip-flop used in the Clock Conditioning Circuit must be ECL. In this case, however, a second device, an ECL-to-TTL translator (such as a 10H350 or 10H125) will need to be wired into the Clock Conditioning Circuit. Keep in mind that negative ECL and positive ECL have different power supply requirements. Your Clock Conditioning Circuit will need to take this into consideration. Wire the translator input to the Q-output of the divide-by-two flip-flop. The translators output will drive the resistor network and coax as mentioned above.

[3] The optional P6041 External Clock Cable is available specifically for this purpose.

[4] A parallel driver can be created by wiring two flip-flops from the same package in parallel. This doubles the current drive capability. The Q output of the primary flip-flop, however, must be used for the D inputs of both devices.

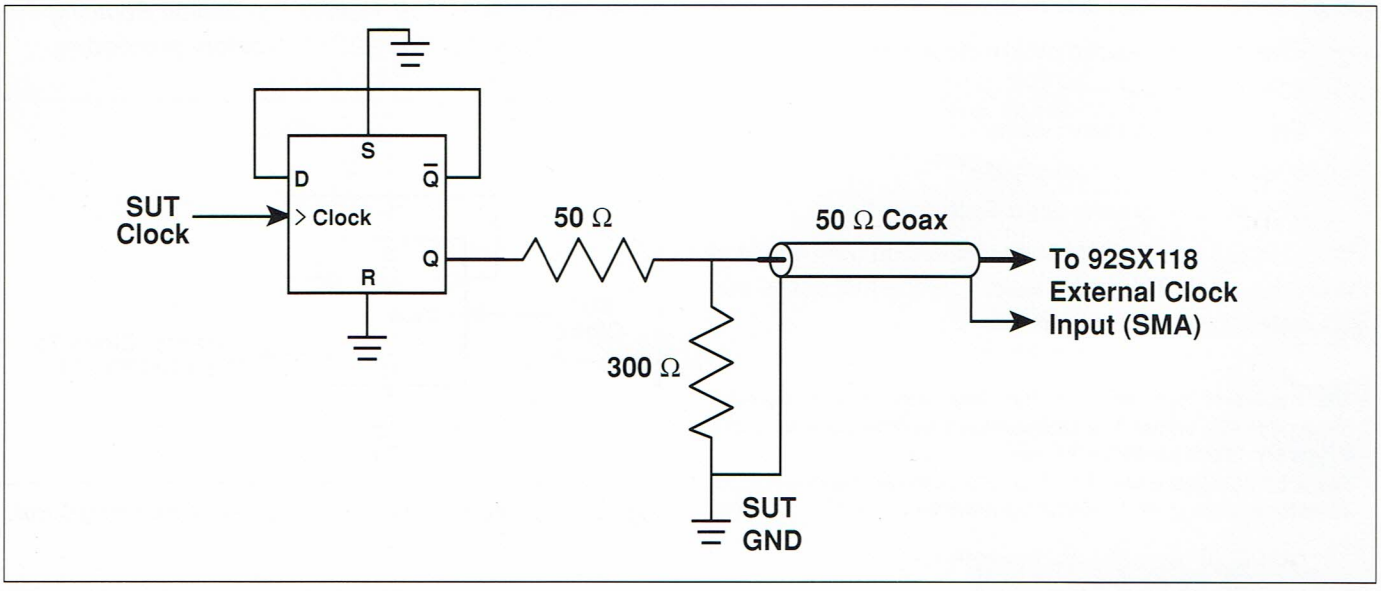

Figure 2 — Back termination example schematic.

PHASE DELAY CONSIDERATIONS

The 92SX109/SX118 have approximately a 100 ns external clock propagation delay measured from the External Clock input lead to the clock output of a P6464 output data probe. This may be an issue when these subsystem's are interfaced to the SUT. The following discussion outlines two techniques which can be used to minimize the effects of this delay. The first technique is frequency dependent and requires measurements and adjustments when ever you change the operating speed. Also there is a phase delay between the first clock applied to the 92SX109/SX118 clock inputs and the first clock output by the pattern generators. Although the second technique doesn't exhibit either of these anomalies, it is more intrusive on the SUT. It requires modifications to the SUT not required in the first technique. The decision about how and where an external clock is provided is very dependent on the actual device/system being tested. The hope is that these concepts will help you in your decision.

1. Add Delay to Align 92SX109 Data

Consider an application where the P6464 data outputs are to be synchronized to the SUT clock. There will be set/hold requirements and the P6464 data must have the proper timing relationship with the SUT clock at the circuit where the data is being applied.

To set this timing relationship, program the 92SX109 to run in a loop and then measure the time between the SUT clock and pattern generator's output data with an oscilloscope. This measurement needs to be made right at the pins of the device where the pattern generator data is being applied. When the 92SX109 is operating at 100 MHz, the maximum difference between SUT clock and pattern generator data will be ± 5 ns (1 cycle). The programmable data edge placement of the 92SX109 (± 2 ns range) can be used to minimize this difference if it is ≤ 2 ns. If the difference is near 5 ns, the 92SX109's programmable clock delay provides a ± 5 ns range that can be used along with the edge placement to minimize this difference. The combination of both delays provide a maximum 7 ns adjustment range. If you are trying to align the pattern generator output clock with the SUT clock, the data edge positioning does not effect the clock timing.

At lower speeds where data delay compensation greater than 7 ns may be required, you will need to externally delay the SUT clock prior to the external clock input of the 92SX109. Be sure that the method you use does not substantially degrade the integrity of the clock signal.

With this technique, the data edges can be aligned, but there will be a delay of several clock cycles between the External Clock input and P6464 clock output. With a free-running clock source, this is of no concern.

2. Run the SUT Using The Pattern Generator Clock

Each P6464 output data probe has nine data outputs and one clock output. If you are not using one of these output clocks, it can be used to drive the SUT. Choose a point in the SUT clock path where you can disconnect the normal clock source. Replace this source with the clock output from the 92SX109/SX118.

As an example, the SUT clock could be disconnect between the clock oscillator and clock buffers. The Clock Conditioning Circuit's input would connect to the oscillator's output. The selected pattern generator's output clock would be connected to the SUT clock's buffer. This technique assures that the pattern generator output data is in phase with the clock with NO delay. The SUT clock however, should be free running. Beware, there may be undesirable results if the SUT clock should stop/start on the wrong phase of the Clock Conditioning circuit.

CONCLUSIONS

This document has covered the basics of converting a non-symmetrical clock source at a frequency higher than the 92SX109/SX118 can accept into a compatible waveform. The techniques discussed are provided as guidelines and suggestions. The hope is that, with knowledge about your design, you will be able to adapt these techniques with success for your specific needs.

Written by Mike Nelson, Tektronix, Inc.

To place your order or to obtain more information, please contact your local Tektronix Sales Representative, or call or write to these locations:

U.S.A.
Call the Tektronix National Marketing Center
at (800) 426-2200.

Central & South America, Japan, Asia and Australia
Tektronix, Inc.
P.O. Box 500, M/S 50-439
Beaverton, Oregon 97077, USA
Phone: (800) 835-9433 Ext. 1916
Telex: 192825 TEKTRONIX
FAX: (503) 627-6905

France and Africa
Tektronix S.A.
ZAC Courtaboeuf, 4 Av. du Canada
BP. 13
91941 Les Ulis Cedex
France
Phone: 33 (1) 69 86 81 81
Telex: (842) 690332 TEKOR A
FAX: 33 (1) 69 07 09 37

Federal Republic of Germany
Tektronix GmbH
Colonia Allee 11
D-5000 Cologne 1
Phone: 49 (221) 96969-0
Telex: (841) 8885417 ATEK D
FAX: 49 (221) 96969-362

United Kingdom
Tektronix U.K. Limited
Fourth Avenue
Globe Park
Marlow
Bucks SL7 1YD
Phone: 44 (628) 486000
Telex: (851) 847277, 847378
FAX: 44 (628) 474799

Italy
Tektronix S.p. A.
Via Lampedusa 13
20141 Milan
Phone: 39 (2) 84441
Telex: (843) 315217 TEKMIL I
FAX: 39 (2) 8950-0665

Austria, Eastern Europe and the Middle East
Tektronix Ges.m.b.H.
Doerenkampgasse 7
A-1100 Vienna
Austria
Phone: 43 (222) 68 66 02 0
Telex: (847) 111481 TEK A
FAX: 43 (222) 68 66 00

Rest of Europe
c/Condessa de Venadito, 1-5.planta
28027 Madrid
Spain
Phone: 34 (1) 404.1011
Telex: (831) 46014 TKME E
FAX: 34 (1) 404.0997

Canada
Tektronix Canada Inc.
P.O. Box 6500
Barrie, Ontario L4M 4V3
Phone: (705) 737 2700
Telex: 06875672 TEKTRONIX BAR
FAX: (705) 737-5588

For further information, contact Tektronix, Inc., Corporate Offices: P.O. Box 500, Beaverton, OR 97077.
Phone: (503) 627-7111; TLX: 192825 TEKTRONIX.
Subsidiaries and distributors worldwide.

Tektronix®
COMMITTED TO EXCELLENCE

05/89 57W-7167