Tektronix®
COMMITTED TO EXCELLENCE

7D01
LOGIC ANALYZER

(Serial No. B020000 to B086084)

WITH OPTIONS

OPERATORS

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

Serial Number _____

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WARRANTY

Tektronix warrants that this product is free from defects in materials and workmanship. The warranty period is one (1) year from the date of shipment. Tektronix will, at its option, repair or replace the product if Tektronix determines it is defective within the warranty period and if it is returned, freight prepaid, to a service center designated by Tektronix.

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SAFETY SUMMARY

The following safety information is provided to ensure safe operation of this instrument. WARNING information is intended to protect the operator; CAUTION information is intended to protect the instrument. The following are general safety precautions that must be observed during all phases of operation and maintenance.

WARNING

Ground the Instrument

To reduce electrical-shock hazard, the mainframe (oscilloscope) chassis must be properly grounded. Refer to the mainframe manual for grounding information.

Do Not Operate in Explosive Atmosphere

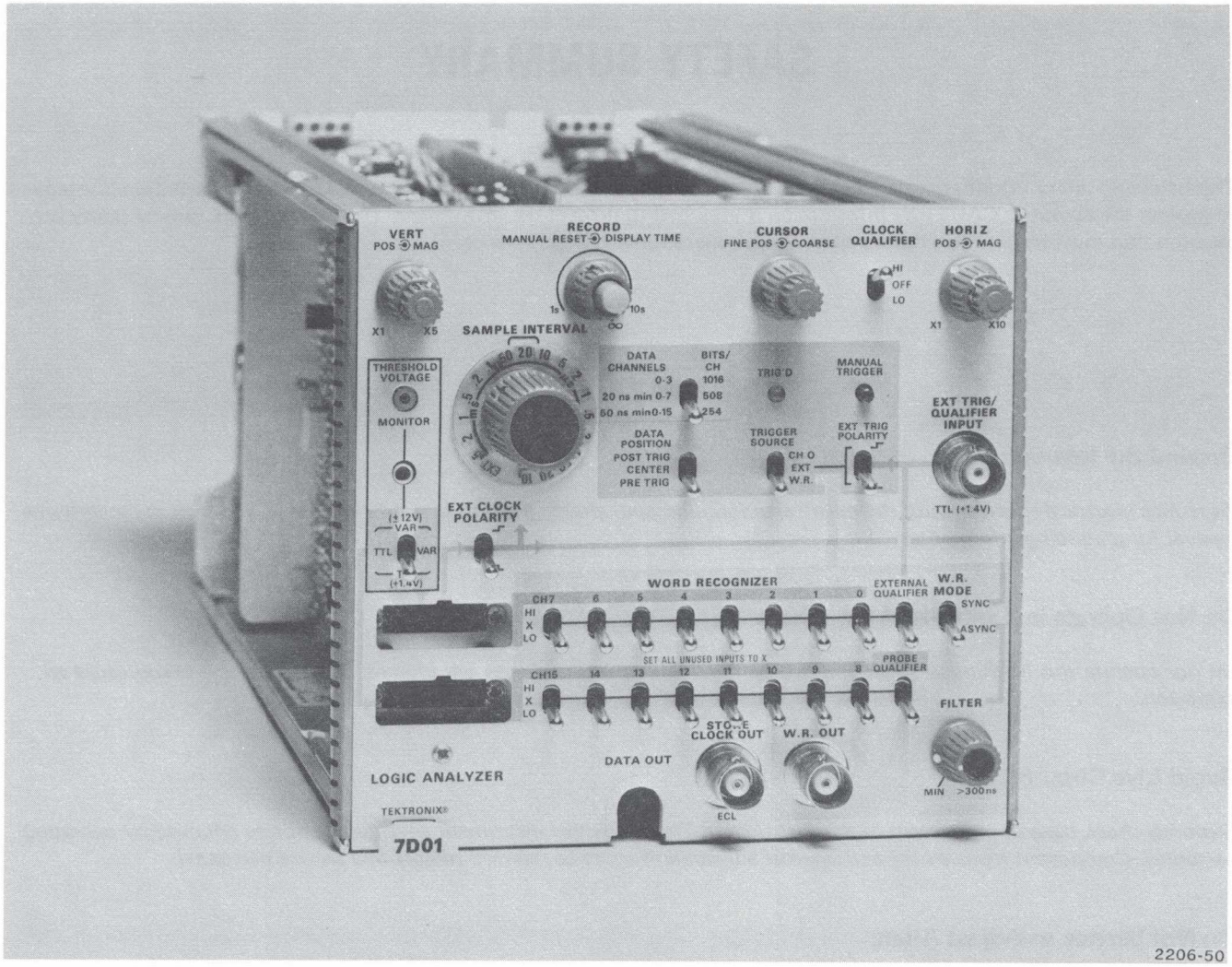
Do not operate this instrument in an area where flammable gases or fumes are present. Such operation could cause an explosion.

Avoid Live Circuits

Electrical-shock hazards are present in this instrument. The protective instrument covers must not be removed by operating personnel. Component replacement and internal adjustments must be referred to qualified service personnel.

Do Not Service or Adjust Alone

Do not service or make internal adjustments to this instrument unless another person, capable of giving first aid and resuscitation, is present.



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7D01 FEATURES

The 7D01 Logic Analyzer will store and display up to 16 channels of digital data when installed in a 7000-series mainframe. The cursor function provides an intensified zone on the data display, and a corresponding numerical readout display shows the logic state (1 or 0) for each displayed channel of data. The position of the cursor, relative to the trigger, is also displayed on the crt readout. Cursor readout is displayed in either 3-bit or 4-bit bytes.

Digital data can be stored in 3 formats: 4 channels at 1016 bits/channel, 8 channels at 508 bits/channel, or 16 channels at 254 bits/channel. The sample rate is selectable from 10 nanoseconds to 5 milliseconds/sample (in a 5-2-1 sequence) when using the internal time base, or can be used with an external clock signal (up to 50 megahertz).

The 7D01 can be triggered from 4 sources: channel 0 data, an external signal, a built-in 16-channel word recognizer, or manually. The triggered data can be produced following the trigger (POST TRIG), centered around the trigger (CENTER), or preceeding the trigger (PRE TRIG). The input threshold can be varied from minus 12 volts to plus 12 volts, or set to plus 1.4 volts for TTL logic levels.

The Word Recognizer produces an output when the logic states of the 16 input data channels match the states of the corresponding Word Recognizer switches. Two qualifier inputs are also provided to enable the Word Recognizer output. The Word Recognizer operates in either the synchronous or asynchronous mode. A variable filter (to at least 300 nanoseconds) allows rejection of brief false-trigger signals.

GENERAL INFORMATION

INTRODUCTION

7D01 Operator's Manual

The Operator's manual contains the information necessary to operate the 7D01 Logic Analyzer. The manual is divided into three sections, each covering a specific topic of the instrument. Section 1 provides a basic description of the 7D01, a glossary of logic terms, installation instructions, and specifications. Section 2 contains operating information for the instrument. Information concerning available options for the 7D01 is on a tabbed page in Section 3.

7D01 Instruction Manual

The Instruction manual provides operating and servicing information for the 7D01 Logic Analyzer. The manual is divided into ten sections. Operating information is covered in the first two sections; servicing information is contained in the remaining eight sections of the manual. Schematics are located at the rear of the manual and can be unfolded and used for reference while reading other parts of the manual. The reference designators and symbols used on the schematics are defined on the first page of the Diagrams section. Abbreviations used in the manuals, except in the parts list and schematics, comply with the American National Standards Institute Y1.1-1972 publication. The parts lists are computer printouts and use computer-supplied abbreviations.

GLOSSARY

The terms listed in this glossary are used throughout this manual.

Asynchronous—Multiple digital information transferred at non-common clock rates.

Bit—The smallest increment of digital information.

CPU—Central Processing Unit.

ECL—Emitter-Coupled Logic.

Jitter—A form of distortion in asynchronous systems that is due to timing variations of the received data.

Multiplexing—The combining of multiple inputs into a single output.

Parallel-to-Serial Conversion—The technique of storing a digital pattern from a parallel bus, then transferring that pattern out to a serial bus.

Parity Bits—Bits added to the data stream which enable the receiver to verify whether the data is correctly or incorrectly received.

PROM—Programmable Read Only Memory.

RAM—Random Access Memory.

Serial Data—Data transferred on a single line. Serial data logic is derived in a sequential mode.

Store Clock—The clock used to store information into the 7D01 memory.

Synchronous—Digital information transferred with the same clock reference.

Threshold Voltage—The comparator input voltage on the inverting input, which is used as a reference. Thus, if the signal on the non-inverting input is above the threshold voltage, the output is HI; if the signal is below the threshold voltage, the output is LO.

TTL—Transistor-Transistor Logic.

"Wired-OR"—ECL gate outputs that are connected together to yield the equivalent output of an OR gate.

INSTALLATION

The 7D01 is calibrated and ready to use when received. It is designed to occupy a vertical and horizontal plug-in compartment in all 7000-series mainframes with readout except the Digital Processing Oscilloscope (DPO), which will not digitize the 7D01 outputs. There are some operating modes, however, that will not provide proper operation. These modes are discussed under Displaying Data in section 2.

Install the 7D01 in the two compartments on the right side of a three-compartment mainframe, or in the right vertical and A horizontal compartments in the center of a four-compartment mainframe.

NOTE

Some rackmounted mainframes have vertically mounted rods in front of the plug-in compartments that interfere with the installation of the 7D01. Detach these rods by removing the mounting screws at each end before installing the 7D01.

To install the 7D01 in the mainframe, align the 7D01 tracks with the rails of a vertical and horizontal plug-in compartment. Gently slide the 7D01 into the mainframe and push firmly to lock the 7D01 front panel flush with the mainframe.

To remove the 7D01, grasp the release latch in the lower left corner and pull the 7D01 out of the mainframe.

PACKAGING FOR SHIPMENT

If this instrument is to be shipped for long distances by commercial transportation, it is recommended that the instrument be packaged in the original manner for maximum protection. The carton and packing material in which your instrument was shipped should be saved and used for this purpose.

If the original packaging is unfit for use or not available, package the instrument as follows:

1. Obtain a carton of corrugated cardboard with at least a 200 pound test strength and inside dimensions of no less than six inches more than the instrument dimensions; this will allow for cushioning.

2. Surround the instrument with polyethylene sheeting to protect the finish of the instrument.

3. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between the carton and the instrument, allowing three inches on all sides.

4. Seal the carton with shipping tape or an industrial stapler.

Also, if this instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag to the instrument showing the following: Owner of the instrument (with address), the name of an individual at your firm that can be contacted, complete instrument type and serial number, and a description of the service required. Mark the address of the Tektronix Service Center, and your return address, on the carton in one or more prominent locations.

SPECIFICATION

The electrical specifications listed in Table 1-1 apply when the following conditions are met: (1) The instrument must have been adjusted at an ambient temperature between +20° and +30° C (+68° and +86° F), (2) the instrument must be operating in an ambient temperature between 0° and +40° C (+32° and +104° F), and (3) the instrument must have been operating for at least 20 minutes.

TABLE 1-1
Electrical Characteristics

Characteristic	Performance Requirement	
CLOCK AND DATA INPUTS		
Probe Inputs (Clock, Qualifier, and Data)		
Input R and C	1 MΩ within 5%, paralleled by approx. 5 pF.	
Threshold Voltage		
VAR (at Monitor Jack)	−12 V or less, to at least +12 V.	
TTL	+1.4 V within 0.2 V.	
Minimum Logic Swing	500 mV plus 2% of threshold voltage p-p or less, centered on threshold voltage.	
Maximum Logic Swing	−60 V or less, to at least threshold voltage plus 10 V.	
Maximum Non-Destructive Input Voltage	−60 V or less, to at least +60 V.	
External Clock		
Minimum Clock Period		
CH 0-3	20 ns or less.	
CH 0-7	20 ns or less.	
CH 0-15	40 ns or less.	
Minimum Clock Pulse Width	**HI Level**	**LO Level**
CH 0-3	10 ns or less	10 ns or less
CH 0-7	10 ns or less	10 ns or less
CH 0-15	20 ns or less	20 ns or less
Minimum Data Setup Time		
CH 0-3	20 ns or less.	
CH 0-7	20 ns or less.	
CH 0-15	23 ns or less.	
Minimum Data Hold Time	0 ns or less.	

TABLE 1-1 (CONT.)
Electrical Characteristics

Characteristic	Performance Requirement
CLOCK AND DATA INPUTS (CONT.)	
Internal Clock	
Minimum Sample Interval	
CH 0-3	10 ns or less.
CH 0-7	20 ns or less.
CH 0-15	50 ns or less.
Minimum Data Pulse Width (to Ensure Recording)	1 sample interval plus 5 ns.
INTERNAL CLOCK	
Crystal Oscillator Frequency	100 MHz within 0.005 MHz.
Sample Intervals	10 ns to 5 ms/sample in 1-2-5 sequence.
TRIGGER	
Trigger Sources	
CH 0	Triggers on rising edge of CH 0 data.
External Trig/Qualifier Input	
Threshold	+1.4 V within 0.2 V (TTL Level).
Minimum Pulse Width	15 ns or less.
Max Safe Input Voltage	−5 V or less, to at least +10 V.
Word Recognizer	16 Data inputs, Probe Qualifier, and External Qualifier. Output is true when input conditions match switch settings (HI, X, LO).
Minimum Input Pulse Width (Asynchronous Mode)	
Any Single Channel	10 ns or less.
Channels 0-3	15 ns or less.
Any Other Combination	20 ns or less.
Filter	Continuously variable to at least 300 ns.
Synchronous Mode	Coincidence of matching combination and an external clock edge must occur for recognition.
Minimum Setup Time	12.5 ns or less.
Minimum Hold Time	8.5 ns or less.

TABLE 1-1 (CONT.)
Electrical Characteristics

Characteristic	Performance Requirement
TRIGGER (CONT.)	
Word Recognizer Output	
Voltage	
HI	At least +1.9 V (0.95 V into 50-Ω load).
LO	+0.1 V or less (50 mV into 50-Ω load).
Output Impedance (Rising Edge)	50 Ω, within 10%.
Full Display/First Trigger Mode Selection	Selectable by internal jumper, P617.
Full Display Mode	Produces a full horizontal display.
First Trigger Mode	Accepts the first trigger after reset.
DISPLAY	
Vertical	
Magnify	X1 to at least X5.
Position	Positions magnified display within graticule area.
Horizontal	
Magnify	X1 to at least X9.
Position	Positions magnified display within graticule area.
Display Length in X1 Mag (With Full Data)	7.5 div to 10 div.
Raster Shift With Format Change	1 div or less at X1 mag.
Display Time Range	Approximately 1 sec to 10 sec, followed by reset; or infinite hold.
Manual Reset	Resets to store mode when button is pushed.
Display Format	Selectable by DATA CHANNELS switch:
Ch 0-3 x 1016 Bits/Ch	1 group of 4 traces.
Ch 0-7 x 508 Bits/Ch	2 groups of 4 traces each.
Ch 0-15 x 254 Bits/Ch	4 groups of 4 traces each.
Blanking Time	
Ch 0-3	8 bits.
Ch 0-7	4 bits.
Ch 0-15	2 bits.

TABLE 1-1 (CONT.)
Electrical Characteristics

Characteristic	Performance Requirement
DISPLAY (CONT.)	
Cursor	
Cursor Position Control	Positions intensified zone to any displayed bit, in increments of 1 bit or 16 bits.
Readout	
Cursor Position	Top right-hand readout shows cursor position (in sample intervals) relative to trigger (e.g., TRIG ± xxx).
Data	Bottom readout shows the logic state of each displayed channel at the cursor (Hi = 1; Lo = 0).
Byte Switch	Breaks data readout into 3-bit or 4-bit bytes. In 16 channels and 3-bit bytes, the left hand group remains 4 bits.
Trigger Intensified Zone	Intensifies trigger point selected by data position switch.
Position (Relative to Displayed Trigger Event)	
10 ns/Sample	Typically 0 to 4 bits.
20 ns/Sample	Typically 0 to 3 bits.
50 ns to 5 ms/Sample	Within 1 bit.
DATA OUT	
Data Out Connector J120*	
Parallel Data Out	Parallel data from Memory, non-inverted.
Serial Data Out	Pin 4—Serial data from memory, non-inverted.
Channel Sequence:	
CH 0-3	2-3-0-1-2, etc.
CH 0-7	2-3-4-5-6-7-0-1-2, etc.
CH 0-15	2-3-12-13-14-15-8-9-10-11-4-5-6-7-0-1-2, etc.

Channel	Pin	Channel	Pin
0	13	8	9
1	25	9	21
2	12	10	8
3	24	11	20
4	11	12	7
5	23	13	19
6	10	14	6
7	22	15	18

***All logic levels are ECL levels unless otherwise specified.**

TABLE 1-1 (CONT.)
Electrical Characteristics

Characteristic	Performance Requirement
DATA OUT (CONT.)	
Data Out Connector J120* (Cont.)	
Frame Output	Pin 16—Falling edge indicates end of Ch 2; rising edge indicates end of Ch 3. Frame occurs every 16th sweep (independent of format).
Flag Output	Pin 14—Falling edge indicates beginning of channel; rising edge indicates end of channel.
Record Enable	Pin 15 Hi input forces reset. Hi output occurs when MANUAL RESET is pressed.
External Display Clock Input	Pin 3, terminated with 100 Ω to −2 V.
Frequency Range	Less than 1 Hz to at least 2 MHz.
Ground	Pin 17.
Signal Select Jumper P300	Pins 1, 2, and 5 of J120 are connected to pins 7, 8, and 6, respectively of the Signal Select Jumper. There are 5 signals available to the Signal Select Jumper.
Format Output	Pins 1 and 2 of Signal Select Jumper:

	Pin 1	Pin 2
Ch 0-3	Hi	Hi
Ch 0-7	Hi	Lo
Ch 0-15	Lo	Lo

Display/Store Output	Pin 3 of the Signal Select Jumper:
Store	Hi
Display	Lo
Trigger Intensify Output	Pin 4 of Signal Select Jumper, LO = intensified trigger point on display.
Master Reset Output	Pin 5 of Signal Select Jumper, HI during reset.
POWER SUPPLY	
Line Voltage Ranges	Refer to 7000-series oscilloscope performance requirements.
Internal Power Supplies	
−4.8 Volt	
Accuracy (+20° to +30° C)	Within −4.80 V to −4.925 V.
−2.0 Volt	
Accuracy (+20° to +30° C)	Within 0.2 V.

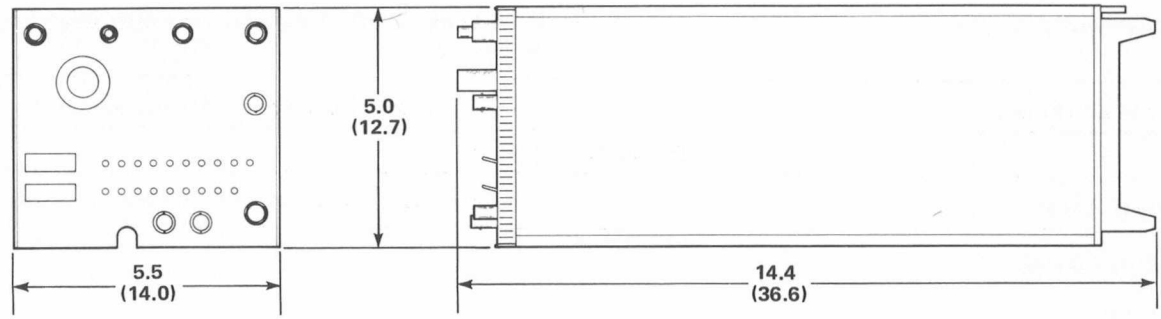
***All logic levels are ECL levels unless otherwise specified.**

TABLE 1-2
Environmental Characteristics

Characteristic	Performance Requirement
Temperature	
Operating	0° to +40° C.
Storage	−55° to +75° C.
Altitude	
Operating	To 15,000 feet.
Storage	To 50,000 feet.
Transportation	Qualified under National Safe Transit Committee Test Procedure 1A, Category II.

TABLE 1-3
Physical Characteristics

Characteristic	Description
Weight (Without Accessories)	Approximately 4.4 lbs (2.0 kg).
Dimensions	See Figure 1-1.



NOTE
DIMENSIONS ARE GIVEN WITH TOP FIGURE IN INCHES AND BOTTOM FIGURE IN CENTIMETERS.

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Figure 1-1. 7D01 Dimensional Drawing.

STANDARD ACCESSORIES

1 ea . . . . . Instruction Manual

1 ea . . . . . Operator's Manual

2 ea . . . . . P6451 Probe Package

For more information, refer to the tabbed Accessories page in the back of this manual.

OPERATING INSTRUCTIONS

This section includes a description of the 7D01 front-panel controls, connectors, and indicators. Also included is detailed operating information, some basic application procedures and a functional check procedure. Refer to Section 1, General Information, for a glossary of terms and installation instructions.

FRONT-PANEL CONTROLS, CONNECTORS, AND INDICATORS

The location and function of the front-panel controls, connectors, and indicators are illustrated in Figure 2-1.

Refer to Detailed Operating Information for a discussion of the auxiliary functions available with the internal selectors, and the input and output signals available through the Data Out connector.

DETAILED OPERATING INFORMATION

AUXILIARY FUNCTIONS

Several auxiliary functions can be selected by connectors and jumpers located inside the 7D01. A 25-pin Data Out connector is also located inside the 7D01 to provide various input and output signals for use with external equipment. The following information describes the auxiliary functions with procedures for making the appropriate internal connections.

Display Clock Source Selector (P835)

Two-pin jumper which determines whether the 7D01 is to be used for display only, or for display and data output (serial and parallel data at the Data Out connector).

When the 7D01 is used for data displays, P835 must be set to Internal Display Clock (see Fig. 2-2). When the 7D01 is to be used for display and data output (serial and parallel), P835 must be set to External Display Clock (see Fig. 2-2) and an external display clock signal must be applied to pin 3 of Data Out connector J120 to synchronize the data output. The rate per bit of the serial and parallel output data is determined by the rate of the external display clock signal applied to pin 3 of Data Out connector J120. If a display is desired, as well as serial and parallel data, the external display clock signal repetition rate must be approximately 2 microseconds. The internal display clock signal is not available as an output.

Full Display/First Trigger Selector (P617)

Two-pin jumper which determines whether data is displayed at the first acceptable trigger after the memory has addressed one full block of data, or whether data is displayed after the first acceptable trigger.

When P617 is set to Full Display (see Fig. 2-2), the memory stores one complete block of data and then accepts the next trigger. The Full Display position is recommended for most repetitive signal applications. If a trigger is expected soon after a reset pulse, or if the wait between displays at slow sample rates is objectionable, P617 can be set to the First Trigger position (see Fig. 2-2). Refer to Synchronous and Asynchronous Data Sampling for more information.

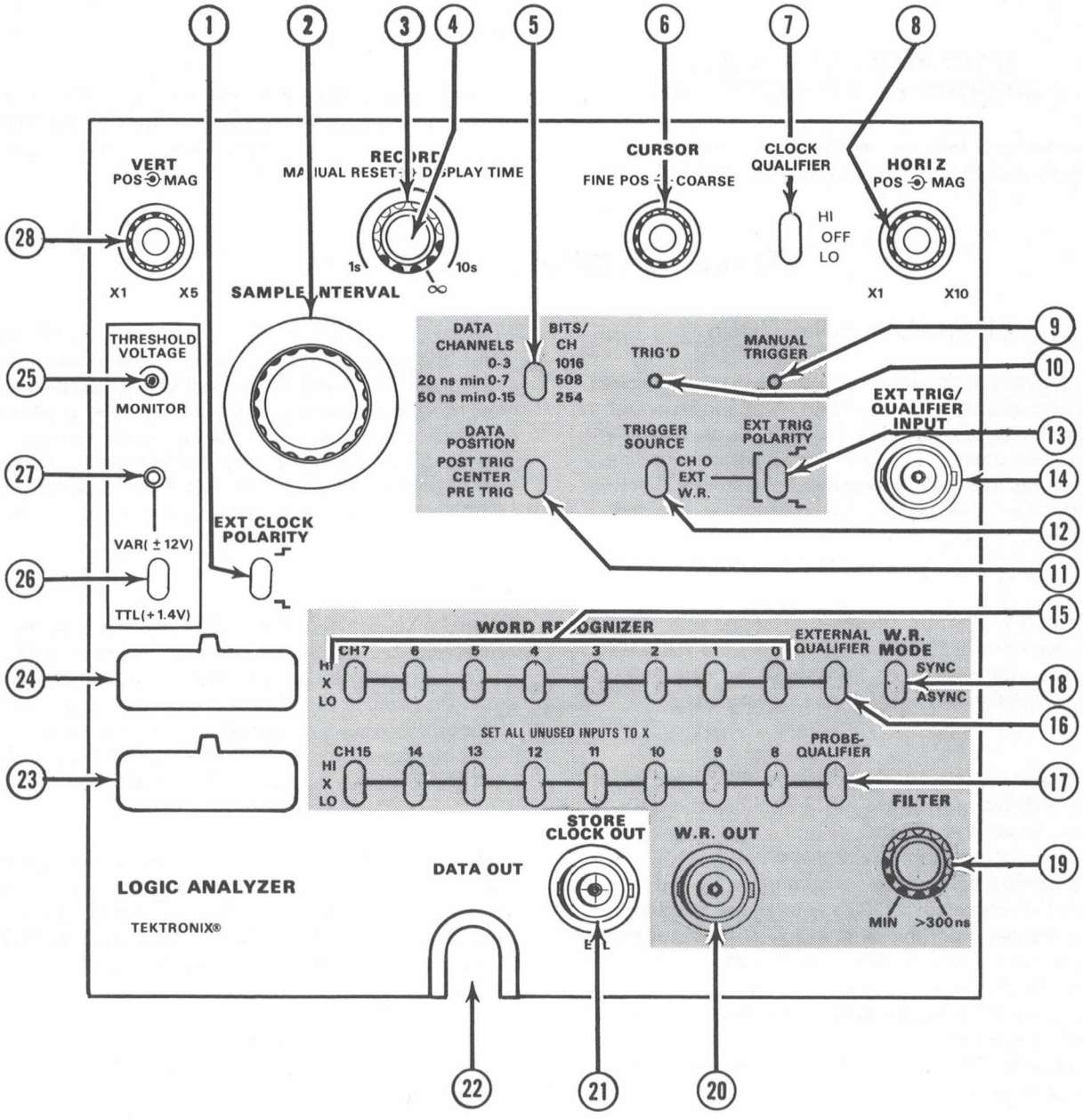
Signal Selector (P300)

Internal multi-pin connector P300 provides 5 signals for connection to 3 outputs on Data Out connector J120. Any 3 of the 5 signals can be used for external use. Figure 2-3 shows the location of P300, and identifies the pin assignments as they are connected when shipped from the factory. To change signal outputs at J120, move the jumper connections at P300 (refer to Fig's. 2-3 and 2-4).

FORMAT OUTPUT. Two outputs (P300 pins 1 and 2) provide ECL-level outputs which indicate the channel selected by the front-panel DATA CHANNELS switch. Table 2-1 shows the ECL levels at pins 1 and 2 of P300 for each position of the DATA CHANNELS switch.

TABLE 2-1
Format Output Levels

DATA CHANNELS	P300	
	Pin 1	Pin 2
0-3	HI	HI
0-7	HI	LO
0-15	LO	LO



(1) EXT CLOCK POLARITY Switch—Selects the active edge of the external clock signal applied to the C (clock) input of the Channel 0-7 Data Input connector.

(2) SAMPLE INTERVAL Switch—Selects the data input sample rate. Sample rates from 5 milliseconds to 10 nanoseconds are provided in a 5-2-1 sequence. A lamp behind the knob skirt blinks when the sample rate is too fast for 8-channel operation (10 nanosecond) or 16-channel (10 or 20 nanosecond) sample intervals. When set to the EXT position, the C (clock) input is selected. The SAMPLE INTERVAL lamp does not blink when operating in the EXT position.

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Figure 2-1. Front panel controls, connectors, and indicators.

(3) DISPLAY TIME Control—Sets the time that the stored data is displayed before a new store cycle begins. The display time is continuously variable from approximately 1 to 10 seconds, or can be held indefinitely by turning the control fully clockwise into the ∞ detent position.

(4) MANUAL RESET Pushbutton (concentric with DISPLAY TIME control)—Overrides the DISPLAY TIME control and starts a new store cycle.

(5) DATA CHANNELS and BITS/CH Switch—Selects data from channels 0 through 3 with 1016 bits of memory per channel (0-3/1016). Selects data from channels 0 through 7 with 508 bits of memory per channel (0-7/508). Selects data from channels 0 through 15 with 254 bits of memory per channel (0-15/254).

(6) FINE POS/COARSE Controls—Positions the cursor intensified zone to any bit on the data display in one-bit (FINE POS) or 16-bit increments (COARSE).

(7) CLOCK QUALIFIER—The Clock Qualifier allows you to selectively store data into the 7D01 memory, by inhibiting or enabling the Store Clock. The Clock Qualifier became a part of the 7D01 Logic Analyzer beginning with serial number B086085. The CLOCK QUALIFIER switch replaces the BYTE switch found on 7D01 units prior to B086085; byte selection is now accomplished through the use of an internal jumper.

(8) HORIZ POS/MAG Controls—Horizontally positions the display with the graticule area (POS) and provides continuously variable horizontal magnification (X1 to X10) of the display (MAG).

(9) MANUAL TRIGGER Switch—Activates the trigger circuit.

(10) TRIG'D Indicator—Lights on the first accepted trigger (after reset) and remains on until the store cycle is reset.

(11) DATA POSITION Switch—Three-position switch selects data for storage in the memory after the trigger (POST TRIG), before and after the trigger (CENTER), or before the trigger (PRE TRIG).

(12) TRIGGER SOURCE Switch—Three-position switch derives the trigger signal from the rising edge of the channel 0 data (CH 0), from an external signal applied to the EXT TRIG/QUALIFIER INPUT Connector (EXT), or from the Word Recognizer (W.R.).

(13) EXT TRIG POLARITY Switch—Selects either the rising or the falling slope as the active edge of the external triggering signal.

(14) EXT TRIG/QUALIFIER INPUT Connector—Provides input for an external signal (TTL level) to be used as an external trigger signal or as an external qualifier signal for the Word Recognizer.

(15) Channel Switches—Sixteen three-position switches (channels 0 through 15) select the active state for each channel of data input. The active state for each channel can be selected to be a high level (HI), a low level (LO), or to disregard the data level (X). The amplitude of the HI and LO states is determined by the THRESHOLD VOLTAGE controls.

(16) EXTERNAL QUALIFIER Switch—Three-position switch selects active state of the signal applied to the EXT TRIG/QUALIFIER INPUT connector. The active state can be selected to be a high level (HI), a low level (LO), or to disregard the data level (X).

(17) PROBE QUALIFIER Switch—Three-position switch selects the active state of the signal applied to pin Q of the channel 0-15 Data Input connector. The active state can be selected to be a high level (HI), a low level (LO), or to disregard the data level (X). The amplitude of the HI and LO states is determined by the THRESHOLD VOLTAGE controls.

(18) W.R. MODE Switch—Two-position switch determines the operating mode of the Word Recognizer system. In the SYNC position, the signal at the W.R. OUT connector goes HI on the active edge of the clock signal after all WORD RECOGNIZER conditions are met (Channels 0 through 15, EXTERNAL QUALIFIER, and PROBE QUALIFIER). The clock input is applied to the C (clock) input of the Digital Acquisition Probe connected to the Channel 0-7 and External Clock Data Input connector. In the ASYNC position, the signal at the W.R. OUT connector goes HI after all WORD RECOGNIZER conditions are met (Channels 0 through 15, EXTERNAL QUALIFIER, and PROBE QUALIFIER).

(19) FILTER Control—Inhibits the HI output at the W.R. OUT connector for about 300 nanoseconds. The FILTER control is functional only when operating in the ASYNC W.R. MODE and is used to prevent triggering from noise or bits that have no meaning at that time.

(20) W.R. OUT Connector—Provides a HI output level for external use when all WORD RECOGNIZER conditions have been satisfied.

(21) STORE CLOCK OUT Connector—Provides ECL level store-clock signal for use with external equipment. This output will drive an unterminated 50-ohm cable. (Do NOT terminate cable with 50-ohm load to ground.)

(22) DATA OUT Access—Provides access to the Data Output connector (J120) inside the instrument.

(23) Channel 8-15 and Probe Qualifier Data Input Connector—Provides probe inputs to Channels 8 through 15 and the Probe Qualifier.

(24) Channel 0-7 and External Clock Data Input Connector—Provides probe inputs for Channels 0 through 7 and the External Clock.

(25) THRESHOLD VOLTAGE MONITOR Pin Jack—Provides an output to monitor the dc threshold voltage of the data inputs.

(26) THRESHOLD VOLTAGE Selector Switch—Three-position switch selects a preset threshold voltage for TTL logic levels (TTL), or a + to − 12-volt variable threshold voltage (VAR) as determined by the screwdriver adjustment. Also selects in TTL-VAR position the variable threshold voltage (+ to − 12-volts) for the Channel 0-7 and External Clock Data Input connector and the preset TTL threshold voltage for the Channel 8-15 and Probe Qualifier Data Input connector.

(27) THRESHOLD VOLTAGE Adjustment—Provides variable threshold voltage (plus or minus 12 volts) when the THRESHOLD VOLTAGE selector is set to VAR.

(28) VERT POS/MAG—Vertically positions the display within the graticule area (POS). Provides continuously variable vertical magnification (X1 to X5) of the display (MAG).

Figure 2-1 (Continued). Front panel controls, connectors, and indicators.

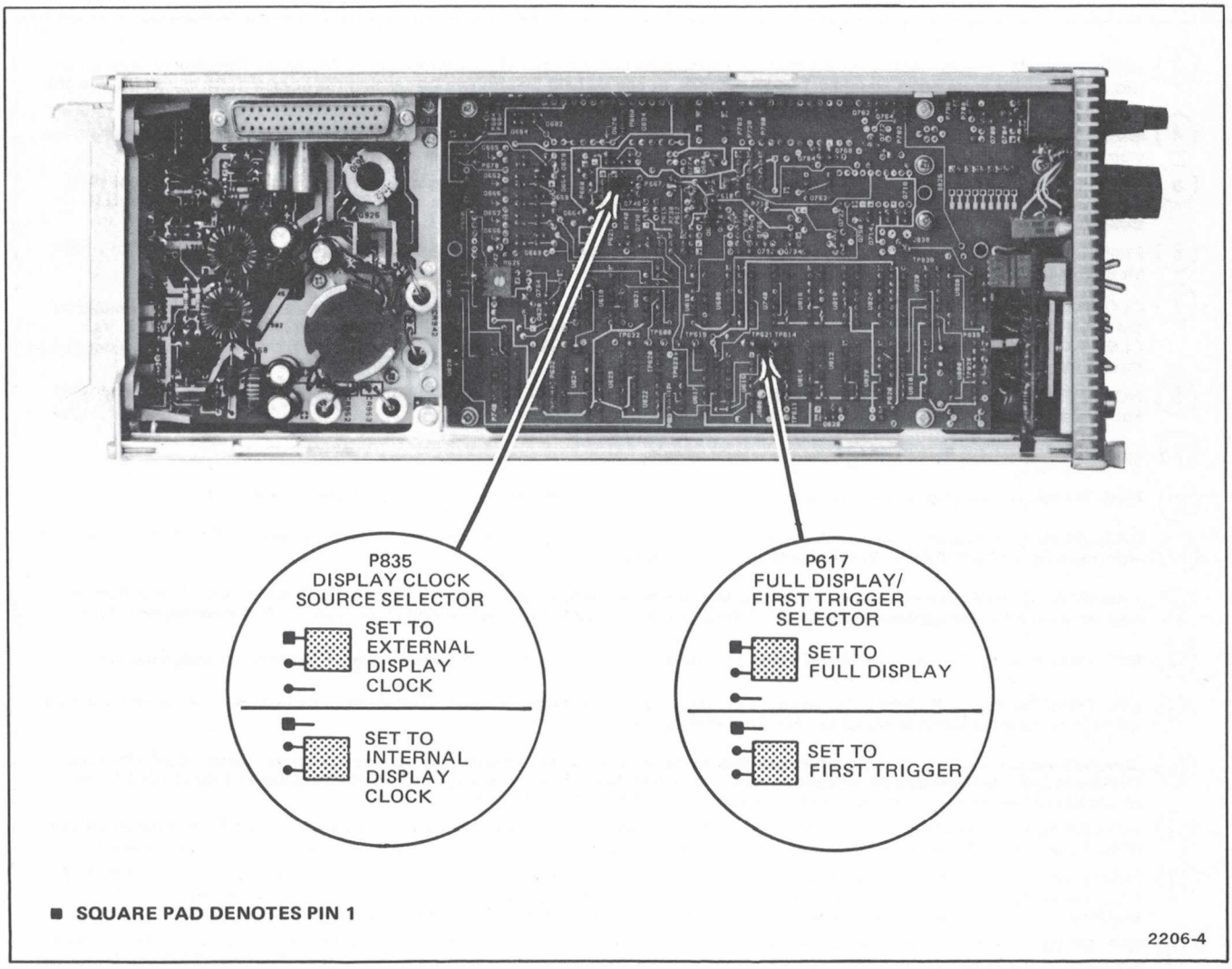


Figure 2-2. Internal Display Clock Source and Full Display/First Trigger Selectors.

DISPLAY-STORE OUTPUT (P300, pin 3). This output indicates whether the 7D01 memory is in the display or store mode. An ECL LO level indicates the memory is in the display mode. An ECL HI level indicates that the memory is in the store mode.

TRIGGER INTENSIFY OUTPUT (P300, pin 4). During the bit when the trigger point on the data display is intensified, an ECL LO level is present at pin 4 of P300.

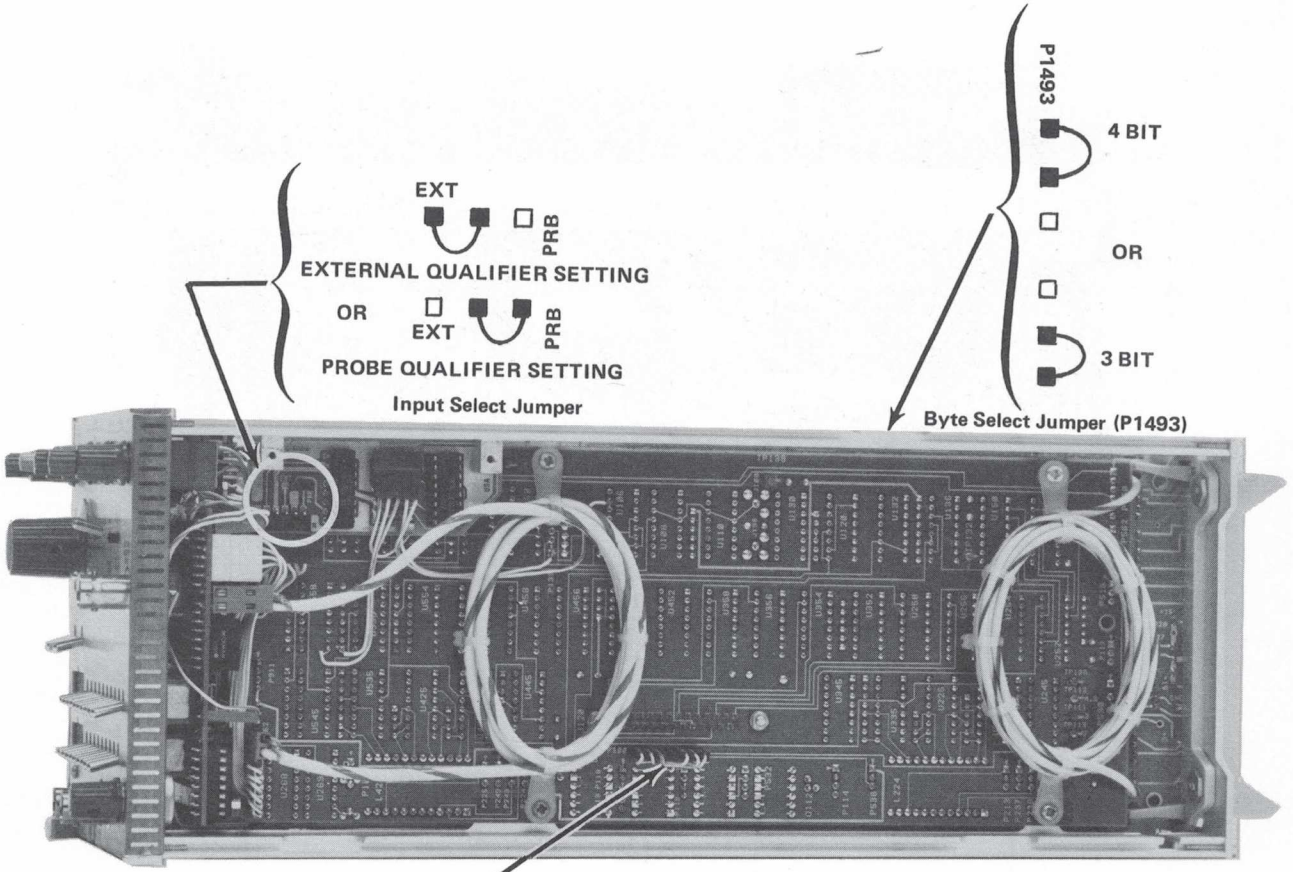
MASTER RESET OUTPUT (P300, pin 5). This output indicates whether the 7D01 is in the store and display or reset mode. An ECL HI level indicates that the memory is in a reset mode. An ECL LO level indicates that the memory is in either the store or display mode.

INTERNAL STRAP SELECTIONS

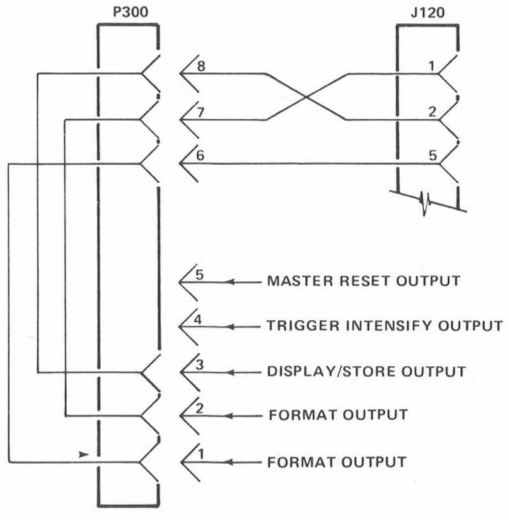
CLOCK QUALIFIER. Equipped 7D01 Logic Analyzers contain two additional internal strap selections. These are the Input Select jumper for the probe qualifier, and the Byte Select jumper that replaces the BYTE switch found on earlier 7D01 models. Set them as follows:

INPUT SELECT. This strap selects which input (External or Probe) will be used for the Clock Qualifier. There are three pins, allowing two possible settings (Fig. 2-3). Place the jumper between the center pin and the PRB pin for Probe Qualifier use. Place the jumper between the center pin and the EXT pin to use the External Qualifier input. The 7D01 is factory-set for Probe Qualifier.

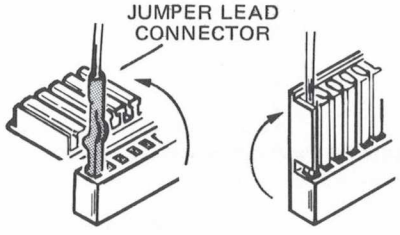
BYTE SELECT. This strap is located near the top center of the 7D01; it is labeled P1493 (Fig. 2-3). It sets the display format of the cursor readout (displayed on the crt of the mainframe) for either 3-bit bytes (0 100 101 010 001 100) or 4-bit bytes (0100 1010 1000 1100). Placing the strap between the top and center pins selects 4-bit bytes; placing the strap between the bottom and center pins selects 3-bit bytes. The 7D01 is factory-set at the 4-bit position.



P300 SIGNAL SELECTOR



P300 JUMPER PLACEMENT PROCEDURE



1. Remove P300 from instrument.
2. Bend grooved portion of holder away from the jumper lead connector in direction of its hinged side.
3. Insert the jumper lead connector into the selected hole in the holder. Crimped side of jumper lead connector faces toward hinged portion of holder.
4. Bend the grooved part of holder back to its vertical position so connector is inserted into groove.
5. Observe the connector polarity and install P300 back into the instrument.

2206-51

Figure 2-3. Internal Signal Selector.

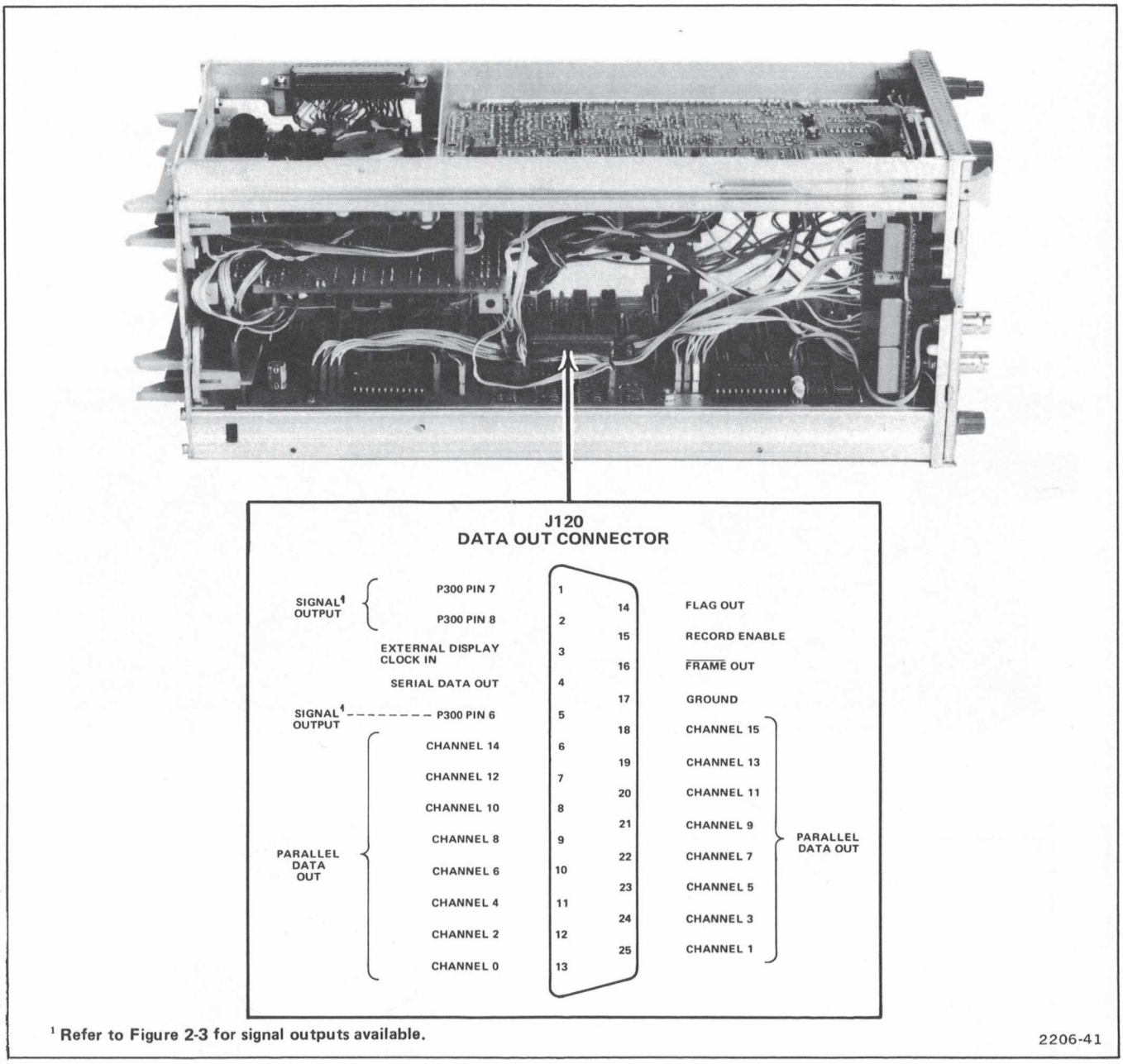


Figure 2-4. Pin assignments for Data Out connector J120.

SIGNAL CONNECTIONS

Data Acquisition

Data is acquired through two high input-impedance Tektronix P6451 Data Acquisition Probes supplied with the 7D01. One probe applies data inputs to channels 0 through 7 and the external clock; the other applies data inputs to channels 8 through 15 and the probe qualifier. The probe microhook connectors provide a convenient means of attaching the probe to the data source. A preset threshold voltage (+1.4 volts) for TTL logic levels or a variable threshold voltage (+12 to −12 volts) can be selected for either or both probes with the THRESHOLD VOLTAGE selector switch.

Data Output

The internal 25-pin Data Out connector (J120) provides access for various input and output signals that can be used with external equipment. See Figure 2-4 for the location of the Data Out connector and the pin assignments.

The outputs from the Data Out connector are unbuffered ECL levels; therefore, it is necessary to assemble a cable terminated to meet the test requirements of the external equipment. One end of the cable should be terminated with a connector that mates with the Data Out connector (J120). Use a type DB-25P, 25-pin male connector, such as Tektronix Part 131-0570-00. See Figure 2-5 for two suggested assembly methods. The external display clock and record

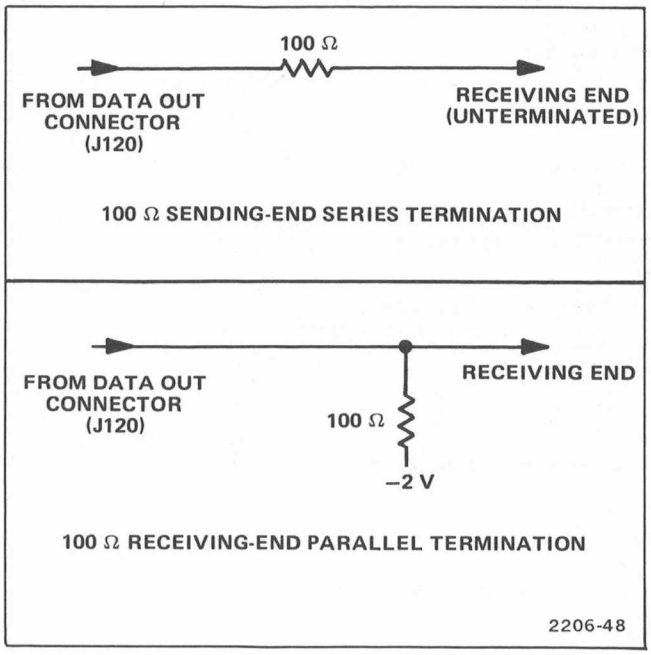


Figure 2-5. Suggested methods for terminating data outputs from Data Out connector J120.

enable inputs are terminated in 100 ohms to −2 volts in the 7D01. For further information, contact your Tektronix Field Office or representative.

In addition to the channel 0 through 15 parallel data outputs, the following input and output signals can be obtained through the Data Out connector (refer to Fig. 2-4 for the location of Data Out connector J120 and the pin assignments).

EXTERNAL DISPLAY CLOCK IN. Provides input for an ECL-level clock pulse and must be used to synchronize serial and parallel data. The internal Display Clock Source Selector, P835, must be set to the External Display Clock position (see procedure under Auxiliary Functions).

SERIAL DATA OUT. Provides serial data from channel 0 through 15. An external display clock must be applied to pin 3, and the Display Clock Source Selector, P835, must be set to the External Display Clock position for synchronized output (see procedure under Auxiliary Functions).

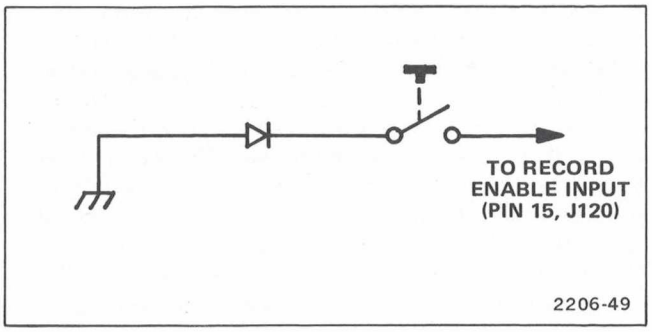


Figure 2-6. Suggested method for assembling a remote Manual Reset button.

PARALLEL DATA OUTPUT. Provides outputs from channels 0 through 15. An external display clock must be applied to pin 3, and the Display Clock Source Selector, P835, must be set to External Display Clock for synchronized output (see procedure under Auxiliary Functions).

FLAG OUT. Provides an output pulse which indicates the beginning of each data channel. A positive-going edge indicates the beginning of a data channel (channels 0 through 15). Data is not valid during a LO ECL level.

RECORD ENABLE. A HI ECL level input pulse forces reset of the memory. When the front-panel MANUAL RESET button is pushed, a HI output level is produced. A remote Manual Reset button can be assembled as shown in Figure 2-6.

FRAME OUT. Provides pulse to synchronize serial data. An ECL LO level occurs at every sixteenth flag pulse for the duration of channel 3. The Frame Out pulse occurs at every sixteenth flag pulse regardless of the setting of the DATA CHANNELS switch. For the sequence in 4, 8, and 16 data channel operation, see Serial Data Out Channel Sequence in Table 1-1, Electrical Characteristics.

DISPLAYING DATA

The 7D01 provides some convenient and unique display capabilities. Figure 2-7 shows a typical channel 0 to 15 display with a 254-bit window. One row of intensified dots are trigger markers that indicate whether the logic analyzer is operating in the pre, center, or post trigger mode as selected by the DATA POSITION switch. A second row of intensified dots are cursor markers that can be moved across the timing diagram with the CURSOR COARSE and FINE POS controls. The cursor function provides a simultaneous timing and logic state display by reading out the selected timing diagram word in 3-bit or 4-bit byte binary at the bottom of the crt. In addition, the number of sample intervals and direction (i.e., − or +) from the intensified trigger markers to the cursor markers appears at the top right side of the crt.

The X10 horizontal and X5 vertical POS and MAG controls expand any portion of the display for close examination. Further magnification can be obtained with a vertical amplifier and time-base plug-in unit, in addition to a 7D01, installed in a 4-compartment mainframe. Refer to Triggering for more information.

NOTE

If the 7D01 is used in a storage mainframe, it is recommended that the mainframe be operated in the non-store mode.

TRIGGERING

The built-in Word Recognizer provides a versatile trigger source. Logic states of parallel words up to 18 bits wide can be preselected by the front-panel channel switches. The Word Recognizer then triggers the 7D01 when the incoming parallel word matches the one preselected by the channel switches (HI, LO, or X-don't care). The intensified trigger markers on the data display indicate the trigger point selected by the Word Recognizer.

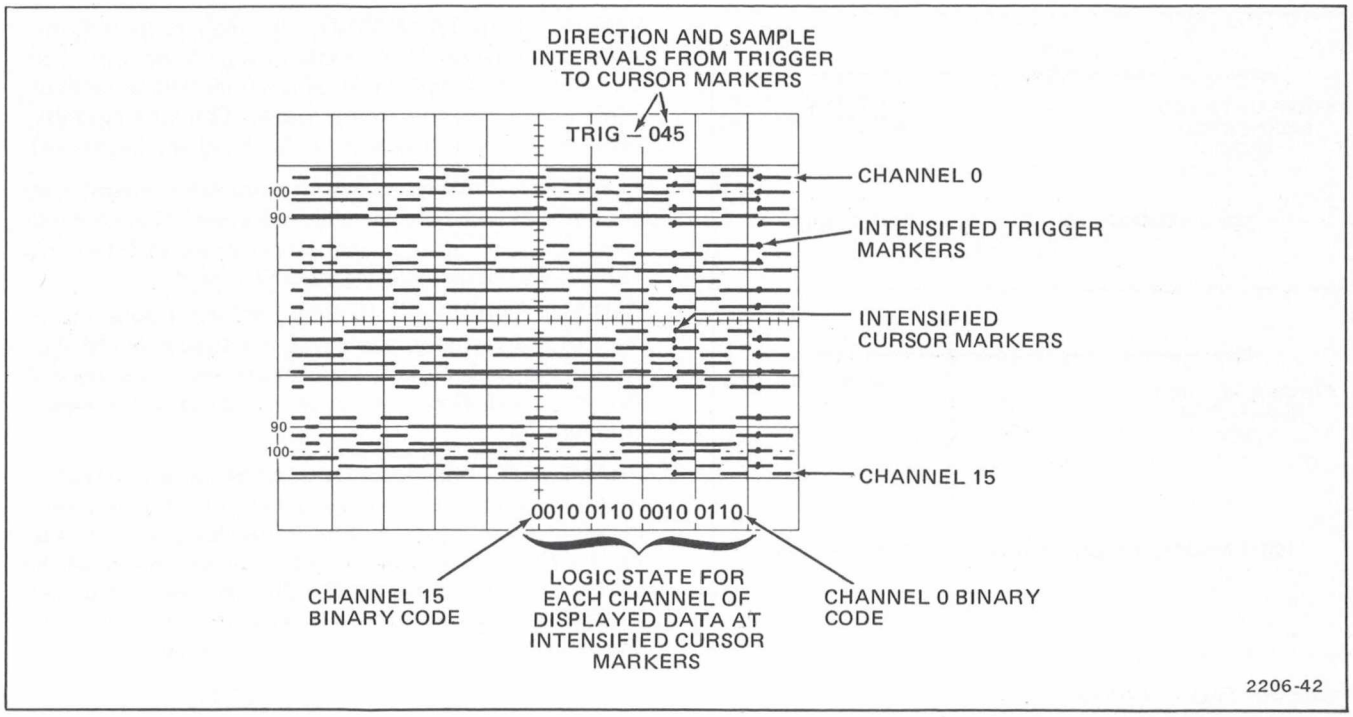


Figure 2-7. Typical channel 0 to 15 pre-trigger data display.

The Word Recognizer also provides a +2-volt (approximately) output pulse from a 50-ohm source at the front-panel W.R. OUT connector when the incoming parallel word matches the preselected word on the channel switches. This output pulse can be used to trigger a time-base plug-in to provide an analog display when the 7D01 is installed in a 4-compartment mainframe. By selecting the mainframe Alternate or Right Vertical Mode operation, analog and digital information can be displayed either simultaneously or separately.

The 7D01 is not designed to operate in the mainframe Horizontal Alternate mode. However, dual-trace displays (i.e. between the 7D01 and a pair of plug-in units installed in the Left Vertical and B Horizontal compartments) can be obtained by selecting the mainframe Vertical Alternate and Horizontal Chop modes. Refer to Fault Identification under Applications for an example of combined digital and analog display operation.

In addition to triggering the 7D01 on a preselected word or pattern, a trigger can be obtained from channel 0 of the input data or from an external qualifier signal such as an error flag, sector pulse, enable signal, or any unique single-channel event. For example, in the synchronous mode, a microprocessor loop can be checked by inputting from the external qualifier with all other channels set to X (don't care). Thus, the Word Recognizer triggers on the qualifier without recognizing the other channels, and displays an isolated window rather than the entire data train.

CLOCK QUALIFIER OPERATION

The Clock Qualifier allows you to make optimum use of the 4K memory present in the 7D01. In many test situations, continuous sampling fills the memory with data that isn't relevant to the problem at hand. When a properly timed qualifier signal is available, then entire memory space can be filled only with pertinent data.

The Clock Qualifier is used when the 7D01 is sampling in synchronous mode, using the clock of the system under test. During normal synchronous operation, data is stored in memory once during each clock cycle. When the Clock Qualifier is activated, new data is stored only when the clock cycle is qualified by an external signal.

The qualifying signal can come from the Probe Qualifier of the data probe (CH 8-15) or can come from a source external to the 7D01 through the unit's EXT TRIG/QUALIFIER INPUT. An internal jumper is used to select either the Probe Qualifier or the External Qualifier. If the Probe Qualifier is used, the PROBE QUALIFIER switch in the WORD RECOGNIZER section of the 7D01 should be set to the don't care (X) position. If an External Qualifier is used, the EXTERNAL QUALIFIER switch should be set to the don't care (X) position. If you use and External Qualifier signal, a word recognizer unit such as the WR 501 can be used to obtain multi-line qualifier capabilities.

The CLOCK QUALIFIER switch on the 7D01 is used to enable the Clock Qualifier, and also to select whether a high or low input signal will be used as the qualifier. This is true for External Qualifier signals and Probe Qualifier signals alike. You can also use the EXT CLOCK POLARITY switch to select whether the positive (⌐) or negative (¬) edge of the clock pulse will start the data sampling process. Different combinations of the CLOCK QUALIFIER switch and the EXT CLOCK POLARITY switch will cause variations in the sampling process.

CLOCK QUALIFIER SWITCH DESCRIPTION

The CLOCK QUALIFIER is a three-position front-panel switch. The switch positions control Clock Qualifier operations in the following ways:

HI — Data is clocked into memory in the active clock edge while the Qualifier input is high.

OFF — Clock Qualifier is disabled.

LO — Data is clocked into memory on the active clock edge while the Qualifier input is low.

The EXT CLOCK POLARITY switch selects either the positive (⌐) or negative (¬) clock edge as the active edge.

ADDITIONAL OPERATING INFORMATION

CLOCK QUALIFIER RULE NO. 1. The WORD RECOGNIZER is not automatically qualified by the clock qualifier. To qualify both the clock and WORD RECOGNIZER trigger, a WORD RECOGNIZER input and clock qualifier must be connected to the same signal. Therefore, whenever WORD RECOGNIZER triggering is employed with clock qualification, it is necessary to also qualify the WORD RECOGNIZER with the same signal which is qualifying the clock.

Example: Use the probe qualifier as WORD RECOGNIZER input, and use the external qualifier to qualify the clock.

CLOCK QUALIFIER RULE NO. 2. When the clock qualifier is utilized, the qualifying signal is input through either the EXT QUALIFIER connector or through the probe qualifier line on the CH 8-15 probe, by selecting the appropriate jumper position on the Clock Qualifier circuit board. Whichever qualifier input is used, the respective WORD RECOGNIZER qualification switch must be left in the "X" (don't care) position.

ASYNCHRONOUS AND SYNCHRONOUS DATA SAMPLING

ASYNCHRONOUS. When analyzing logic timing in a hardware system, it is desirable to sample data asynchronously. The 7D01 is then clocked internally (i.e., asynchronous to the system under test) to determine clock frequencies and make timing comparisons. Data is sampled asynchronously at a rate of up to 100 megahertz with a minimum data pulse width of 1 sample interval plus 5 nanoseconds. Asynchronous testing requires that data be sampled frequently for maximum timing resolution.

SYNCHRONOUS. For applications where the data is valid at qualified clock transitions is of interest and not the changes in between (e.g., when checking software), the program flow of clocked systems should be sampled externally or synchronously. The 7D01 is then synchronized with the measured system clock at a sampling rate of up to 50 megahertz.

When data is being recorded by the 7D01, there is a minimum number of external clock pulses necessary to produce a transition from record to display mode. The required number of clock pulses varies depending on the DATA POSITION switch and Full Display/First Trigger Selector (P617) settings. Refer to Figure 2-2 for the location of the Full Display/First Trigger Selector (P617).

When in Full Display mode after the MANUAL RESET button is pressed, the entire 4096 bits of memory must be filled with new data before the 7D01 will accept a trigger (4096 bits corresponds to 1024 clock pulses in 4 channel, 512 clock pulses in 8 channel, and 256 clock pulses in 16 channel). After the trigger is accepted, another block of data must be acquired before the 7D01 will switch from the record to the display mode. The size of this block of data depends on the DATA CHANNELS and DATA POSITION switch settings and contains all of the information stored from the trigger point to the end of the displayed trace. This block of data corresponds to the minimum number of clock pulses given in Table 2-2 for the First Trigger mode.

TABLE 2-2
Minimum Clock Pulses Required to Display Data (After the MANUAL RESET Button is Pressed)

DATA CHANNELS	First Trigger Mode DATA POSITION			Full Display Mode[1] DATA POSITION		
	POST TRIG	CENTER	PRE TRIG	POST TRIG	CENTER	PRE TRIG
0-3	958	510	62	1982	1534	1086
0-7	479	255	31	991	767	543
0-15	239	127	15	495	383	271

[1] **In Full Display mode, the 7D01 must have 1024 clock pulses with 0-3 data channels, 512 clock pulses with 0-7 data channels, and 256 clock pulses with 0-15 data channels before a trigger is accepted.**

In First Trigger mode, however, it is not necessary to fill the entire 4096-bit memory before a trigger is accepted. Instead, a trigger can be accepted at any time after the MANUAL RESET button is pressed and one clock pulse is accepted. Thus, the number of clock pulses needed to cause the 7D01 to switch from record to display mode (after the MANUAL RESET button is pressed) is always less in First Trigger mode than in Full Display mode (i.e., by 1024, 512, or 256 clock pulses).

When measuring a circuit with gated clock pulses and data, there may not be enough clock pulses, before the system is gated off, to cause the 7D01 to trigger or display data in the Full Display mode. If this condition occurs, the First Trigger mode will enable the 7D01 to accept a trigger and store the data. However, the data will not be displayed unless the minimum number of clock pulses specified in Table 2-2 is available. The additional clock pulses necessary to switch the 7D01 from record to display mode can be obtained by changing the SAMPLE INTERVAL switch from the EXT position to the 5 ms position after the data is recorded. However, the data recorded after the SAMPLE INTERVAL switch was changed to the 5 ms position is not valid since the system being measured is not functioning during that interval.

OPERATIONAL ANALYSIS

The following table lists some irregular operating symptoms with their probable causes and corrective procedures. Table 2-3 is intended to assist the operator in determining whether an irregular operating symptom is the result of a measurement technique problem or a malfunction in the 7D01. The probable causes for the symptoms listed in Table 2-3 assume that the 7D01 and associated equipment is operating properly. The corrective procedures can be performed by the operator without additional test equipment.

TABLE 2-3
Operational Analysis

Symptom	Probable Cause	Corrective Procedure
1. No data display.	Display positioned off screen.	Check HORIZ and VERT POS settings.
	Wrong threshold voltage.	Check THRESHOLD VOLTAGE selector and/or adjustment setting.
2. No data display with SAMPLE INTERVAL in EXT position.	No external clock signal.	Check that clock signal is applied through Data Acquisition Probe.
	Wrong threshold voltage.	Check THRESHOLD VOLTAGE selector and/or adjustment for proper setting.
3. No data display with: a. W.R. MODE in SYNC position. b. TRIGGER SOURCE in W.R. position. c. TRIG'D indicator not lit.	No external clock signal.	Check that clock signal is applied through Data Acquisition Probe.
	Word selected on WORD RECOGNIZER channel switches does not exist exist.	Check that WORD RECOGNIZER channel switches are set for an existing word.
4. No data display with: a. W.R. MODE in ASYNC position. b. TRIGGER SOURCE in W.R. position. c. TRIG'D indicator not lit.	Word selected on WORD RECOGNIZER channel switches does not exist.	Check that WORD RECOGNIZER channel switches are set for an existing word.
	Asynchronous filter is rejecting valid data.	Check that FILTER is not set too far clockwise.
5. When Testing Circuits with Gated Clocks a. No data display with: (1) SAMPLE INTERVAL in EXT position. (2) Full Display/First Trigger (P617) in First Trigger position. (3) TRIG'D indicator not lit.	Trigger word existed only during first clock pulse and is ignored by the 7D01.	See Asynchronous and Synchronous Data Sampling for minimum number of clock pulses required to obtain a display in First Trigger mode. — OR — Set SAMPLE INTERVAL to 5 ms position for at least 5 seconds. Then reset SAMPLE INTERVAL to EXT position and start data source.

TABLE 2-3 (CONT.)
Operational Analysis

Symptom	Probable Cause	Corrective Procedure
5. (Continued) b. No data display with: (1) SAMPLE INTERVAL in EXT position. (2) Full Display/First Trigger (P617) in First Trigger position. (3) TRIG'D indicator lit.	Insufficient number of clock pulses after trigger word to fill memory (display) from trigger markers to end of sweep.	See Asynchronous and Synchronous Data Sampling for minimum number of clock pulses required to obtain a display in First Trigger mode. —OR— Set SAMPLE INTERVAL to 5 ms position until display appears. Then reset SAMPLE INTERVAL to EXT position.
c. No data display with: (1) SAMPLE INTERVAL in EXT position. (2) Full Display/First Trigger (P617) in Full Display position. (3) TRIG'D indicator lit.	Insufficient number of clock pulses after trigger word to fill 7D01 memory (display) from trigger markers to end of sweep.	See Asynchronous and Synchronous Data Sampling for minimum number of clock pulses required to obtain a display in Full Display mode. —OR— Set SAMPLE INTERVAL to 5 ms position until display appears. Then reset SAMPLE INTERVAL to EXT position. **NOTE** *First Trigger mode may be preferred since fewer clock pulses are required to switch from record to display mode.*
d. No data display with: (1) SAMPLE INTERVAL in EXT position. (2) Full Display/First Trigger (P617) in Full Display position. (3) TRIG'D indicator not lit.	Insufficient number of clock pulses to fill 7D01 memory.	See Asynchronous and Synchronous Data Sampling for minimum number of clock pulses required to obtain a display in Full Display mode. Set SAMPLE INTERVAL to 5 ms position for at least 5 seconds. Then reset SAMPLE INTERVAL to EXT position. When data is present from Data Acquisition Probe, TRIG'D indicator should light and display should appear. But: (1) If there is no display and TRIG'D indicator is lit, set SAMPLE INTERVAL to 5 ms position until display appears. Then reset SAMPLE INTERVAL to EXT position. (2) If display does not appear and TRIG'D indicator is not lit, refer to Corrective Procedure for Symptom 3 and 4. **NOTE** *First Trigger mode may be preferred since fewer clock pulses are required to switch from record to display mode.*

TABLE 2-3 (CONT.)
Operational Analysis

Symptom	Probable Cause	Corrective Procedure
6. Incorrect data display when installed in a storage mainframe.	Mainframe set for store mode.	Set mainframe for non-store mode. **NOTE** *When the 7D01 is used in a storage mainframe, it is recommended that the mainframe be operated in the non-store mode.*
7. Incorrect data display.	Wrong mainframe Vertical and/or Horizontal Mode.	Check that proper mainframe Vertical and/or Horizontal Mode is selected.
	Wrong threshold voltage.	Check THRESHOLD VOLTAGE selector and/or adjustment for proper setting.
8. Incorrect data display after changing DATA CHANNEL or DATA POSITION setting.	MANUAL RESET was not pressed after changing DATA CHANNEL or DATA POSITION setting.	Press MANUAL RESET to store new data in memory in the correct format.
9. Incorrect or noisy data display on channels that are not connected to a Data Acquisition Probe.	Data input lines are not biased properly when a Data Acquisition Probe is not connected.	Connect a Data Acquisition Probe to unused channels. —OR— Use only channel 0-7 and set DATA CHANNELS to 0-3 or 0-7 position. Set all unused WORD RECOGNIZER channel switches (8-15) to X (don't care) position.
10. Random or incorrect triggering from WORD RECOGNIZER with only one Data Acquisition Probe connected.	WORD RECOGNIZER channel switches on unused channels are set to HI or LO positions which can cause some channels to oscillate.	Set WORD RECOGNIZER channel switches on unused channels to X (don't care) position.
11. Displayed data on left side of trigger marker is blanked out.	Full Display/First Trigger (P617) is in First Trigger position.	Set Full Display/First Trigger (P617) to Full Display position.
12. Portions of data input do not appear on display (aliasing) with internal clock pulses.	Data changes faster than the sampling rate.	Set SAMPLE INTERVAL for more than 1 sample interval for each data pulse (i.e., data pulse = shortest period of time that data remains in HI or LO state).

APPLICATIONS

INTRODUCTION

The 7D01 with its built-in Word Recognizer is a versatile measurement tool for detailed logic analysis. A choice of configurations are available to meet a variety of logic analysis and troubleshooting requirements. The following information includes some specific application procedures and examples of applications for the 7D01. Contact your local Tektronix Field Office or representative for assistance on applications that are not included here.

FAULT IDENTIFICATION

The following procedure describes a method for finding a fault, determining its location on a data train, and examining it on a real-time analog display. This method assumes that the fault occurs at a unique word. For this application, the 7D01 is used with a companion vertical amplifier and time-base plug-in unit in a 4-compartment mainframe with readout.

1. Connect test equipment as shown in Figure 2-8A.

2. Set the 7D01 W.R. MODE switch to ASYNC and the TRIGGER SOURCE switch to W.R.

3. Set the mainframe to display the right vertical and A horizontal compartments.

4. Obtain the desired data display (see example in Fig. 2-8B).

5. Set the CURSOR controls to position the intensified cursor markers to the leading edge of the displayed fault.

6. Note the binary word readout (bottom right side of graticule).

7. Set the Word Recognizer for the binary word code noted in step 6.

8. Connect a 10X probe from the vertical amplifier plug-in unit to the data channel that contains the fault as determined in step 5.

9. Set the mainframe to display the left vertical and B horizontal compartments.

10. Set the vertical amplifier deflection factor and time-base plug-in unit sweep rate and triggering for a stable analog display of the data channel selected in step 8 (see example in Fig. 2-8C).

NOTE

The 7D01 FILTER control can be used to provide some horizontal positioning of the display.

DELAY BY WORDS

The following describes a method for preselecting a binary word and positioning the data display window anywhere from the first to the 10 millionth time that the binary word occurs. For this application, the 7D01 is used with a companion digital events delay plug-in unit (e.g., Tektronix 7D10 Digital Events Delay) in a mainframe with readout.

1. Connect the test equipment as shown in Figure 2-9A.

2. Set the digital events delay plug-in unit for independent B sweep delay mode and external ac-coupled + slope triggering.

3. Set the 7D01 W.R. MODE switch to ASYNC and the TRIGGER SOURCE switch to W.R.

4. Set the WORD RECOGNIZER channel switches for the desired binary word code.

5. Set the mainframe to display the right vertical compartment.

6. Set the digital events delay plug-in unit for a stable display triggered on the + slope of the events start trigger input.

7. Set the digital events delay plug-in unit to indicate, on the events count readout, the desired number of times

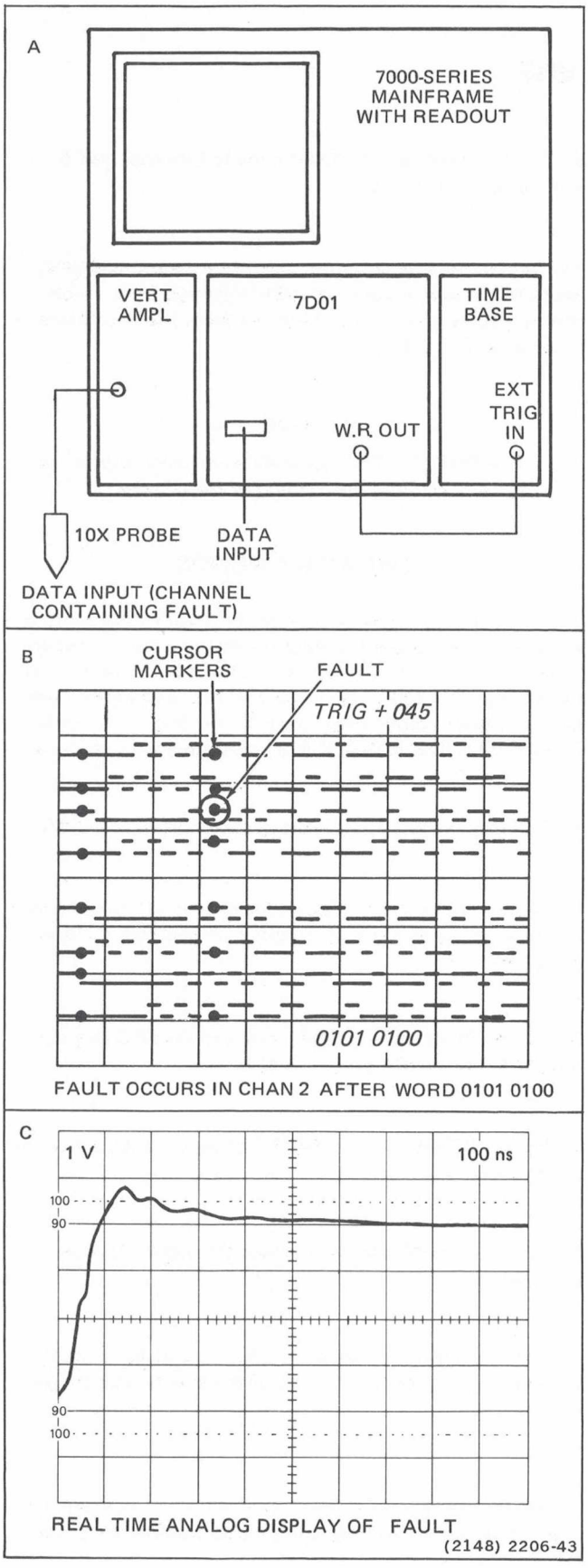


Figure 2-8. Equipment setup and displays for finding a data fault and examining it on an analog display.

that the preselected binary word is to occur before a data display is initiated. For example, if the digital events delay plug-in unit is set for an events count readout of 0000025, the word recognizer will initiate a display of the data before, after, or on both sides of the 25th time that the preselected binary word occurs (see example in Fig. 2-9B).

DELAY BY EVENTS

The following procedure describes a method for positioning the data display window to virtually anywhere along a data train. For this application, the 7D01 is used with a companion digital events delay plug-in unit (e.g., Tektronix 7D10 Digital Events Delay) in a mainframe with readout.

1. Connect the test equipment as shown in Figure 2-10A.

2. Set the digital events delay plug-in unit for external ac-coupled + slope triggering.

3. Set the 7D01 TRIGGER SOURCE switch to EXT and trigger from the external trigger input.

4. Set the mainframe to display the right vertical compartment.

5. Set the digital events delay plug-in unit for a stable display triggered on the + slope of the events start trigger input.

6. Set the digital events delay plug-in unit to indicate the desired number of clock pulses, on the events count readout, that the 7D01 bit-storage window is to be shifted down the data train. For example, if the digital events delay plug-in unit is set for an events count readout of 0010500, the 7D01 will initiate a display of the data before, after, or on both sides of the 10,500th clock pulse (see example in Fig. 2-10B).

STATE TABLE AND MAPPING DISPLAYS

The 7D01 in combination with a display formatter (e.g., Tektronix DF1 Display Formatter) adds state table and mapping displays to the timing diagram display normally available with the 7D01 alone.

The state table mode enables the data stored in the 7D01 memory to be displayed in a tabular format. The display formatter generates the cursor readout in the timing diagram mode, and the state table mode then generates a state display of 17 samples, starting at the cursor, in hexadecimal, octal, or binary code.

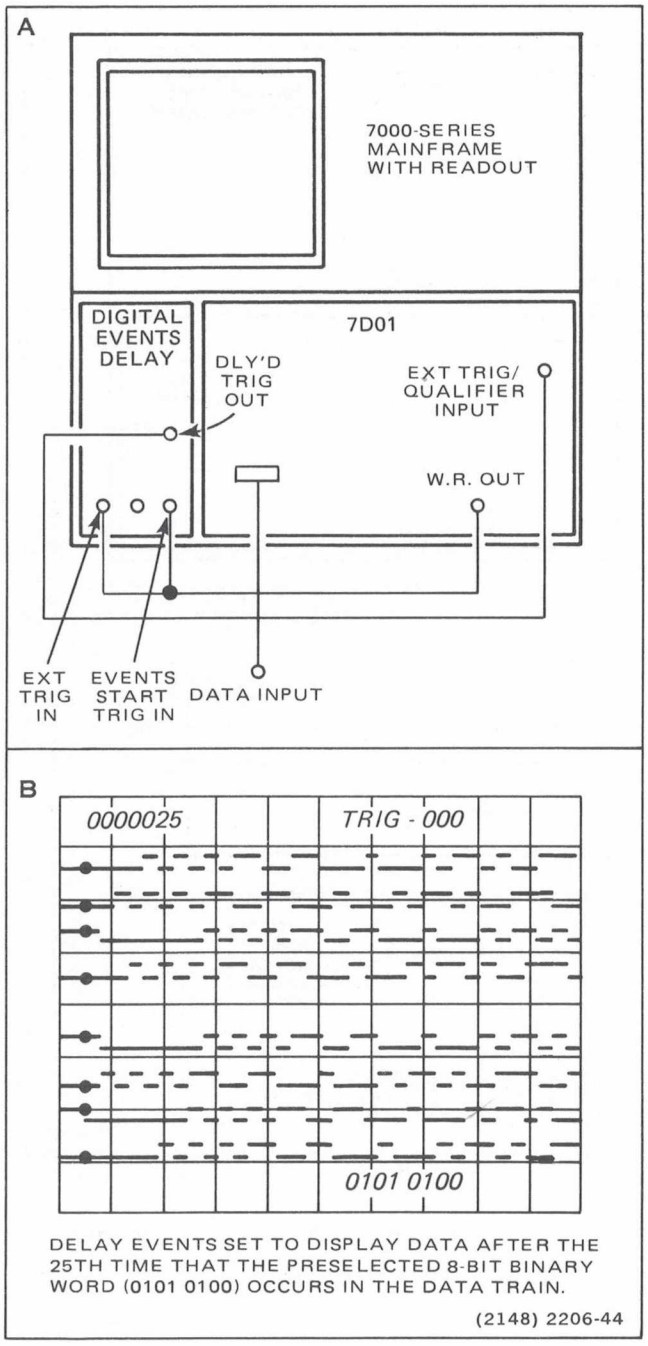


Figure 2-9. Equipment setup and data display window that has been positioned after a preselected word has occurred 25 times.

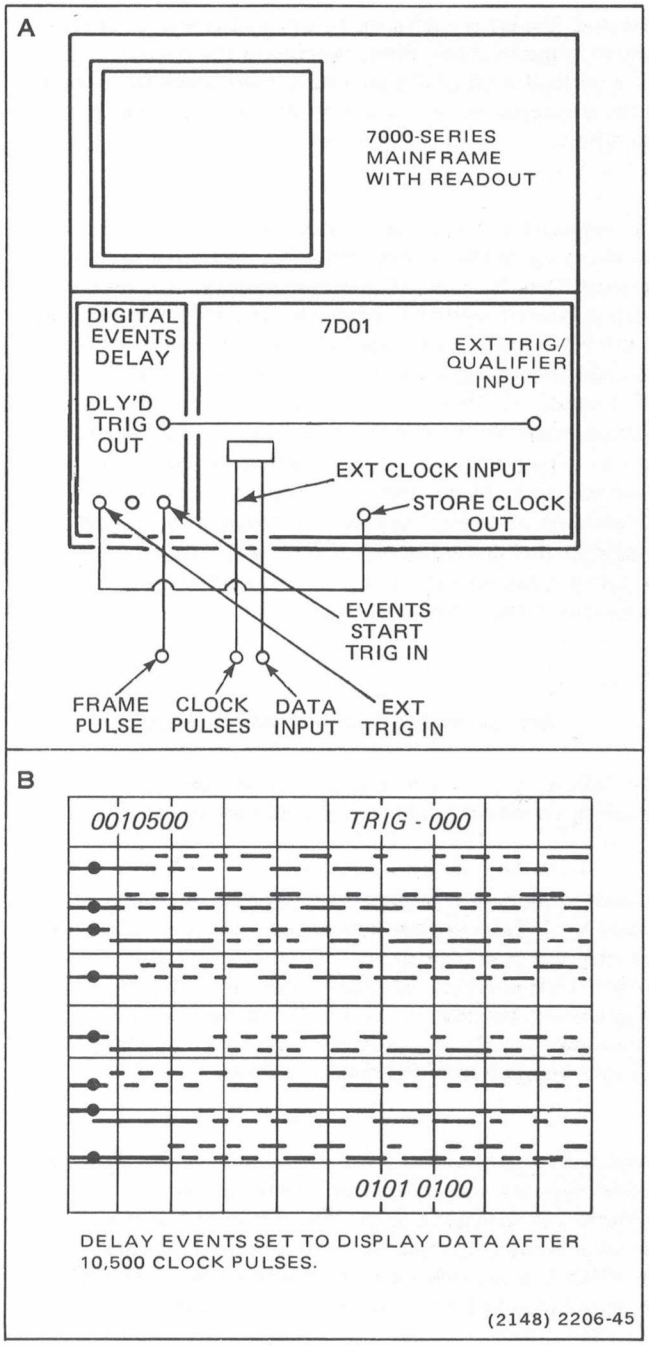


Figure 2-10. Equipment setup and display window that has been positioned after 10,500 clock pulses have occurred.

By using the EXCLUSIVE OR mode (featured with the Tektronix DF1 Display Formatter), the state table from the 7D01 and a reference state table can be displayed simultaneously and faulty bits can be quickly identified. For example, data from the 7D01 memory can be transferred to the display formatter memory for a reference and then incoming data stored in the 7D01 memory can be compared to the reference data. Any differences in the 7D01 data can be identified (each bit that does not agree with the reference data is intensified by the Tektronix DF1 Display Formatter) and the problem located by using the timing diagram display.

The map display is useful for fast overall checks of digital-system program flow. First, determine the pattern (map) for a particular set of digital inputs, then check for a change in the displayed pattern which might indicate abnormal operation.

The mapping and state table modes are particularly useful for checking faulty address lines. For example, evaluate program flow by examining a map display. If a problem word is located, switch to a hexadecimal state-table display in the EXCLUSIVE OR mode for more precise identification of the problem (refer to the preceding EXCLUSIVE OR discussion). Then switch to the binary state-table display to locate the incorrect address line. Further examination of the address line on a timing diagram display reveals a set up and hold problem between the clock and the address line. If desired, use the word recognizer output to trigger an analog display of the 7D01 data output for an even closer examination (refer to the previous Fault Identification discussion for more information).

MICROPROCESSOR ANALYSIS

The following is an example of a technique for troubleshooting a malfunctioning microprocessor system.

A malfunctioning microprocessor system is shown in Figure 2-11. Software had previously worked properly, but was still not free of suspicion. Data was stored in the RAM (random-access read/write memory). The system program was resident in the PROM (programmable read only memory). Restart vectors pointed to the address of the first instruction in the restart routine.

When the restart hardware was exercised, the CPU (central processing unit) should have performed certain initialization routines and then gone to the Wait for Interrupt mode. The terminal would then call up other operating software in the PROM, or provide access to a binary loader. The failure consisted of very erratic operation after restart.

The 7D01 was connected to the system as shown in Figure 2-11 to store and display a large data block from the 8 data lines. The display was obtained by triggering the 7D01 on the beginning of the restart cycle and using the system clock as an external data sampling strobe.

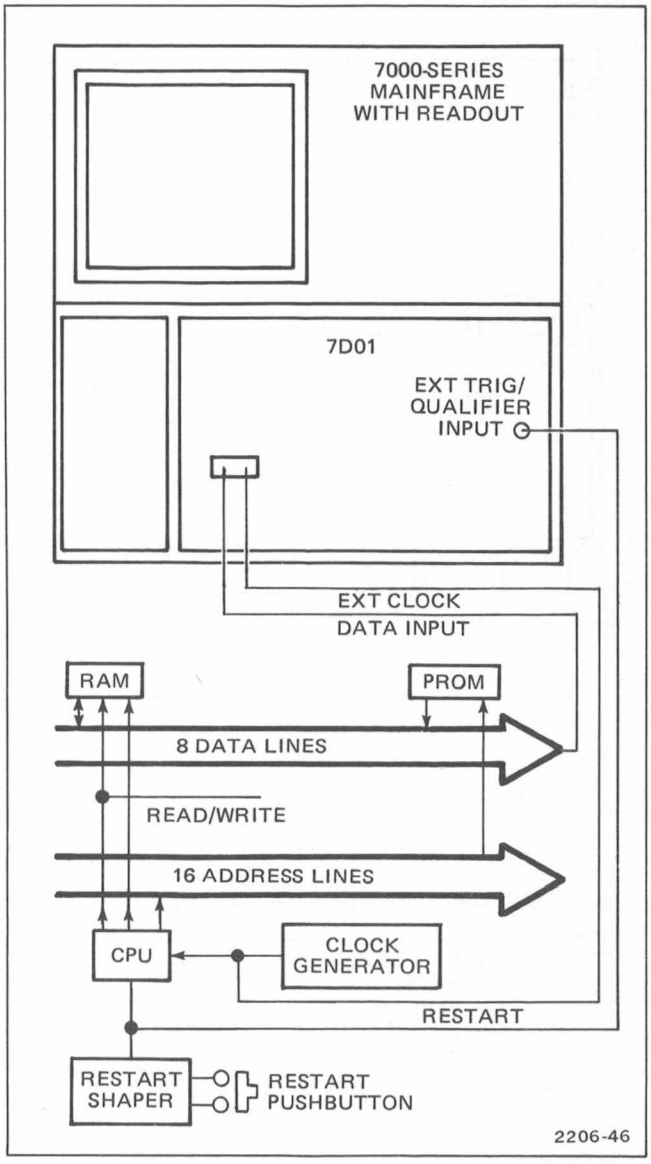


Figure 2-11. Typical setup for troubleshooting a microprocessor system.

Analysis of the data display showed the problem to be a dropped bit in the portion of the PROM providing the restart routine. The CPU fetched an invalid restart vector, causing data from the RAM to be executed as instructions.

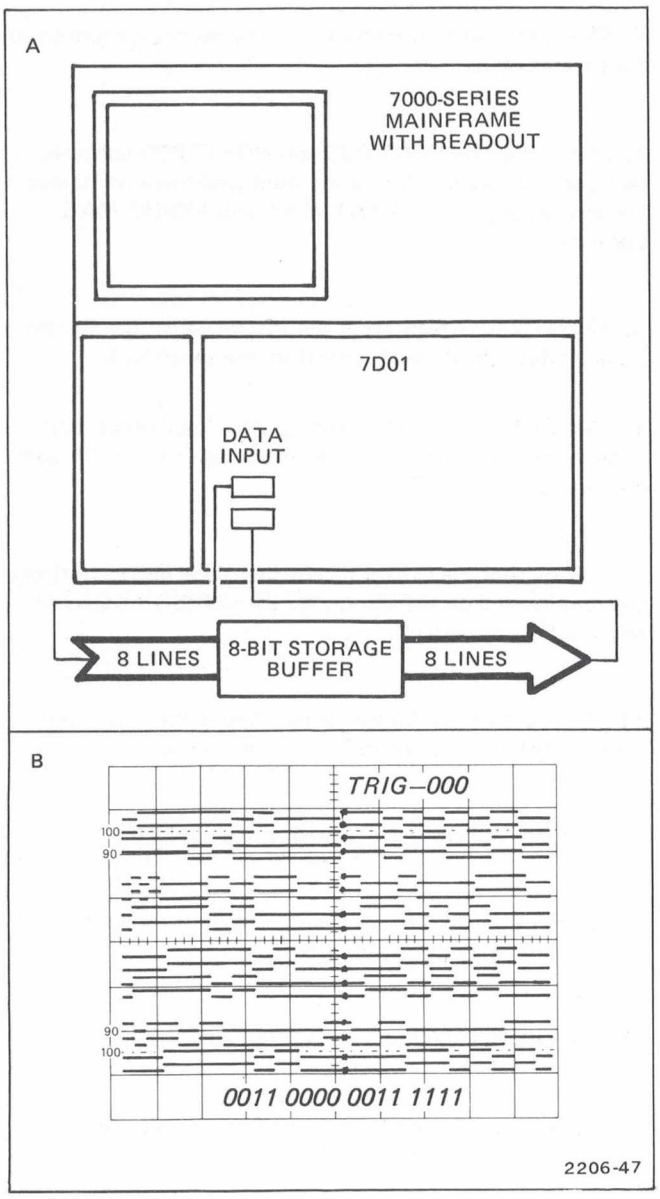


Figure 2-12. Typical setup and display for troubleshooting a storage buffer.

STORAGE BUFFER ANALYSIS

The following procedure describes a method for checking the performance of a storage buffer by monitoring the inputs and outputs simultaneously.

The non-synchronous buffer is a commonly used type, in which data flows continuously from input to output. A display of this data flow will show at a glance if all the memory cells are functioning properly.

The 7D01 can store 8 input and 8 output lines simultaneously and display all 16 data lines on a single display. By displaying an input line and the corresponding output line together, a quick comparison can be made. A typical setup and display is shown in Figure 2-12A and B. When the 7D01 is clocked asynchronously from the internal clock, a high-resolution timing diagram display will provide timing information as well as reveal malfunctions that would otherwise be difficult to detect with any other type of test equipment such as an oscilloscope or dvm.

FUNCTIONAL CHECK

The following procedure checks the basic operation of this instrument. The procedure can be used for incoming inspection to verify proper operation, or by the operator for system troubleshooting.

Functions only are checked in this procedure, therefore a minimum amount of test equipment is required. Measurement quantities and tolerances are not checked.

The Word Recognizer Filter and Output signal, and the Variable Threshold Voltage functions are not checked in this procedure because extra test equipment would be required. These functions, and their associated specifications are checked in the Performance Check and Adjustment section of the 7D01 Instruction manual. Refer these checks to a qualified service technician.

Preliminary Procedure

1. Install 7D01 in oscilloscope mainframe (see Installation instructions in General Information section).

2. Connect a P6451 Data Acquisition Probe to top data-input connector (Channel 0-7 and External Clock).

3. Set 7D01 front-panel controls as follows:

VERT
POS . . . . . .midrange
MAG. X1
RECORD
DISPLAY
TIME . . . . . .∞ (fully clockwise detent)
CURSOR
BYTE . . . . . .4 BIT

HORIZ
POS . . . . . .midrange
MAG. X1
THRESHOLD
VOLTAGE. . . . . .TTL
EXT CLOCK
POLARITY . . . . . ⌐
SAMPLE
INTERVAL . . . . . .1 μs
DATA
CHANNELS. 0-3
DATA
POSITION . . . . . .CENTER
TRIG SOURCE. . . .CH 0
EXT TRIG
POLARITY . . . . . ⌐
WORD
RECOGNIZER
W.R. MODE. . . .ASYNC
FILTER . . . . . .MIN
CH 0 through
15 . . . . . .X (center)
EXTERNAL
QUALIFIER . . .X (center)
PROBE
QUALIFIER . . .X (center)

4. Apply power to oscilloscope mainframe.

Functional Check Procedure

1. Press the RECORD MANUAL RESET and MANUAL TRIGGER pushbuttons (in that order) to obtain display.

2. Adjust Test Oscilloscope intensity and focus controls as desired.

3. Check that four traces are displayed on the crt.

4. Set DATA CHANNELS switch to 0-7.

5. Check that eight traces are displayed in two groups of four traces each.

6. Set DATA CHANNELS switch to 0-15.

7. Check that sixteen traces are displayed in four groups of four traces each.

8. Check that the VERT POS and HORIZ POS controls will position any portion of the displayed traces on screen for any setting of the VERT MAG and HORIZ MAG controls.

9. Check that sixteen zeros are displayed by the Cursor Data readout (bottom of screen) in groups of four.

10. Set CURSOR BYTE switch to 3 BIT and check that sixteen zeros are displayed in four groups of three bits each and one group of four bits.

11. Check that the Cursor Intensified Zone can be horizontally positioned on the display by the CURSOR COARSE and FINE POS controls.

12. Check that the Trigger Intensified Zone is approximately centered (horizontally) on the display.

13. Set DATA POSITION switch to POST TRIG.

14. Check that the Trigger Intensified Zone moves toward the left end of the displayed traces.

15. Set DATA POSITION switch to PRE TRIG.

16. Check that Trigger Intensified Zone moves toward the right end of the displayed traces.

17. Set DATA POSITION switch back to CENTER.

18. Set RECORD DISPLAY TIME control to 1 s position (fully counterclockwise).

19. Check that TRIG'D light goes out and that display disappears.

20. Connect channel 0 probe lead to 4-volt, 1-kilohertz output of oscilloscope calibrator.

21. Check that display reappears and that rising edge of channel 0 waveform is approximately centered (horizontally) on display. (Disregard any noise displayed on channels 7-15.)

22. Set TRIGGER SOURCE switch to W.R.

23. Set WORD RECOGNIZER channel 0 switch to HI.

24. Check that rising edge of channel 0 waveform is approximately centered on the display.

25. Connect channel 0 through 7 probe leads to oscilloscope calibrator output.

26. Set WORD RECOGNIZER channel 0 through 7 switches to HI.

27. Check that rising edges of channel 0 through 7 waveforms are approximately centered on the display.

28. Set WORD RECOGNIZER channel 0 through 7 switches to LO.

29. Check that falling edge of channel 0 through 7 waveforms are approximately centered on the display.

30. Set W.R. MODE switch to SYNC.

31. Check that the TRIG'D light goes out and that display disappears (with external clock probe lead disconnected).

32. Set W.R. MODE switch back to ASYNC.

33. Connect external clock probe lead to oscilloscope calibrator output.

34. Remove Data Acquisition Probe from top Data Input Connector (Channel 0-7 and External Clock) and connect to bottom Data Input Connector (Channel 8-15 and Probe Qualifier).

35. Set WORD RECOGNIZER channel 0 through 7 switches to X and channel 8 through 15 and PROBE QUALIFIER switches to HI.

36. Check that rising edges of channel 8 through 15 waveforms are approximately centered on the display.

37. Set WORD RECOGNIZER channel 8 through 15 and PROBE QUALIFIER switches to LO.

38. Check that falling edges of channel 8 through 15 waveforms are approximately centered on the display.

39. Set all WORD RECOGNIZER channel and qualifier switches to X.

40. Remove Data Acquisition Probe from botton Data Input Connector and connect to top Data Input Connector.

41. Disconnect all probe leads from oscilloscope calibrator.

42. Connect oscilloscope calibrator to EXT TRIG/QUALIFIER INPUT.

43. Set WORD RECOGNIZER EXTERNAL QUALIFIER switch to HI.

44. Check that TRIG'D light is on and display is present.

45. Set WORD RECOGNIZER EXTERNAL QUALIFIER switch to LO.

46. Check that TRIG'D light is on and display is present.

47. Set WORD RECOGNIZER EXTERNAL QUALIFIER switch to X.

48. Set TRIG SOURCE switch to EXT.

49. Check that TRIG'D light is on and display is present.

50. Set EXT TRIG POLARITY switch to ⌐.

51. Check that TRIG'D light is on and display is present.

52. Disconnect oscilloscope calibrator from EXT TRIG/QUALIFIER INPUT.

53. Set TRIGGER SOURCE switch to CH 0.

54. Connect channel 0 and external clock probe leads to 4-volt, 1-kilohertz signal from the oscilloscope calibrator.

55. Set DATA CHANNELS switch to 0-3.

56. Check that a display is present for each position of the SAMPLE INTERVAL switch.

57. Set SAMPLE INTERVAL switch to EXT.

58. Check that a display is present for both positions of the EXT CLOCK POLARITY switch.

59. Disconnect probe leads from oscilloscope calibrator output.

This completes the Functional Check Procedure.

INSTRUMENT OPTIONS

Your instrument may be equipped with one or more instrument options. A brief description of each available option is given in the following discussion. Option information is also incorporated into the appropriate sections of the manual. Refer to Table 3-1 and the Table of Contents for location of option information.

Conversion kits, for most options, are available and can be installed at a later time. For further information on instrument options, see your Tektronix Catalog or contact your Tektronix Field Office.

OPTION 49

Deletes one P6451 Data Acquisition Probe from the standard accessories furnished with the 7D01.

TABLE 3-1
Option Information Locator

Instrument Options	Manual Section	Location of Information
Option 49 (Delete One P6451 Probe)	3 Instrument Options	Instrument Options All information is contained in this section.

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

SERVICE NOTE

Because of the universal parts procurement problem, some electrical parts in your instrument may be different from those described in the Replaceable Electrical Parts List. The parts used will in no way alter or compromise the performance or reliability of this instrument. They are installed when necessary to ensure prompt delivery to the customer. Order replacement parts from the Replaceable Electrical Parts List.

CALIBRATION TEST EQUIPMENT REPLACEMENT

Calibration Test Equipment Chart

This chart compares TM 500 product performance to that of older Tektronix equipment. Only those characteristics where significant specification differences occur, are listed. In some cases the new instrument may not be a total functional replacement. Additional support instrumentation may be needed or a change in calibration procedure may be necessary.

Comparison of Main Characteristics

DM 501 replaces 7D13		
PG 501 replaces 107	PG 501 - Risetime less than 3.5 ns into 50 Ω.	107 - Risetime less than 3.0 ns into 50 Ω.
108	PG 501 - 5 V output pulse; 3.5 ns Risetime	108 - 10 V output pulse 1 ns Risetime
PG 502 replaces 107		
108	PG 502 - 5 V output	108 - 10 V output
111	PG 502 - Risetime less than 1 ns; 10 ns Pretrigger pulse delay	111 - Risetime 0.5 ns; 30 to 250 ns Pretrigger pulse delay
PG 508 replaces 114	Performance of replacement equipment is the same or better than equipment being replaced.	
115		
2101		
PG 506 replaces 106	PG 506 - Positive-going trigger output signal at least 1 V; High Amplitude output, 60 V.	106 - Positive and Negative-going trigger output signal, 50 ns and 1 V; High Amplitude output, 100 V.
067-0502-01	PG 506 - Does not have chopped feature.	0502-01 - Comparator output can be alternately chopped to a reference voltage.
SG 503 replaces 190, 190A, 190B	SG 503 - Amplitude range 5 mV to 5.5 V p-p.	190B - Amplitude range 40 mV to 10 V p-p.
191		
067-0532-01	SG 503 - Frequency range 250 kHz to 250 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
SG 504 replaces 067-0532-01	SG 504 - Frequency range 245 MHz to 1050 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
067-0650-00		
TG 501 replaces 180, 180A	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	180A - Trigger pulses 1, 10, 100 Hz; 1, 10, and 100 kHz. Multiple time-marks can be generated simultaneously.
181		181 - Multiple time-marks
184	TG 501 - Trigger output-slaved to market output from 5 sec through 100 ns. One time-mark can be generated at a time.	184 - Separate trigger pulses of 1 and 0.1 sec; 10, 1, and 0.1 ms; 10 and 1 μs.
2901	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	2901 - Separate trigger pulses, from 5 sec to 0.1 μs. Multiple time-marks can be generated simultaneously.

NOTE: All TM 500 generator outputs are short-proof. All TM 500 plug-in instruments require TM 500-Series Power Module.

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