Instructions

Tektronix®
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12RM05
80186 MNEMONICS ROM PACK
with Option 02

The 80186 Mnemonics ROM Pack configures a 1240 Logic Analyzer to acquire and disassemble data from an 80186 microprocessor. The PM202 Personality Module monitors the contents of the queue, provides fetch prediction, and arranges the address, data, and control lines for use with the setup supplied by the 80186 Mnemonics ROM Pack. (The PM202, which is ordered as Option 02 to the 12RM05, is required for successful use of the 80186 Mnemonics ROM Pack.)

NOTE

To use this ROM Pack and the PM202, your 1240 Logic Analyzer must be equipped with at least three 1240D2 cards and your 80186 must be mounted in an 68-pin JEDEC Type A Socket.

Insert this manual at the back of your *1240 Logic Analyzer Operator's Manual*, or in the 1240 Optional Accessories binder.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL

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OVERVIEW

THIS MANUAL

This manual describes how the 80186 Mnemonics ROM Pack configures the 1240 Logic Analyzer for use with 80186 microprocessors, how to connect the 1240 to the 80186 using the PM202 Personality Module, and how to acquire and display data. It also describes the four data display formats available when an 80186 Mnemonics ROM Pack is installed in your 1240 and how you can get a printout of these state table displays.

OTHER MANUALS

To use the 80186 Mnemonics ROM Pack, you should be familiar with the operation of the 1240 Logic Analyzer and the 80186 microprocessor. Refer to the *1240 Logic Analyzer Operator's Manual* and the operator's manuals for any communication packs that you may be using, as well as Intel's *iAPX 186 High Integration 16-bit Microprocessor* manual (preliminary, December 1982).

PM202 SERVICE

Servicing your own PM202 Personality Module is only recommended if you have a Digital Analysis System 9100 from Tektronix, since full service of the PM202 requires the use of a DAS 9100 equipped with a 91A24 module, a 91P16 module, and a 91P32 module. If you have such a DAS and want to service your own PM202 Personality Module, you will also need a copy of the *PM202 Service Manual*, a service interconnect fixture, and a service tape, all of which come as a kit.

CONFIGURING THE PERSONALITY MODULE

The PM202 Personality Module is designed to provide a convenient interface between the 1240 Logic Analyzer and your 80186 based system. (The 80186 Mnemonics ROM Pack cannot be used without a PM202.) The PM202 also monitors the contents of the 80186 queue and performs fetch prediction. (The PM202 is Option 02 to the 80186 Mnemonics ROM Pack; there is no Option 01.)

CAUTION

Only reconfigure your PM202 in a static-free environment and only after you have grounded yourself to drain static electricity.

Your PM202 was shipped to you configured for use with the 80186 Mnemonics ROM Pack (12RM05) in the normal ($\overline{\text{QSMD}}$) mode. If your 80186 is operating in the QSMD mode, you will have to open the PM202 covers and move the jumpers on J140, J141, and J240 to their QSMD positions.

The PM202 can also be used with an 80188 Mnemonics ROM Pack (12RM06) in either the NOT-QSMD mode or the QSMD mode. To reconfigure your PM202 for use with an 80188, remove the covers of the PM202 and move the jumpers on J500, J520, and J530 to the 80188 position. Refer to Figure 1.

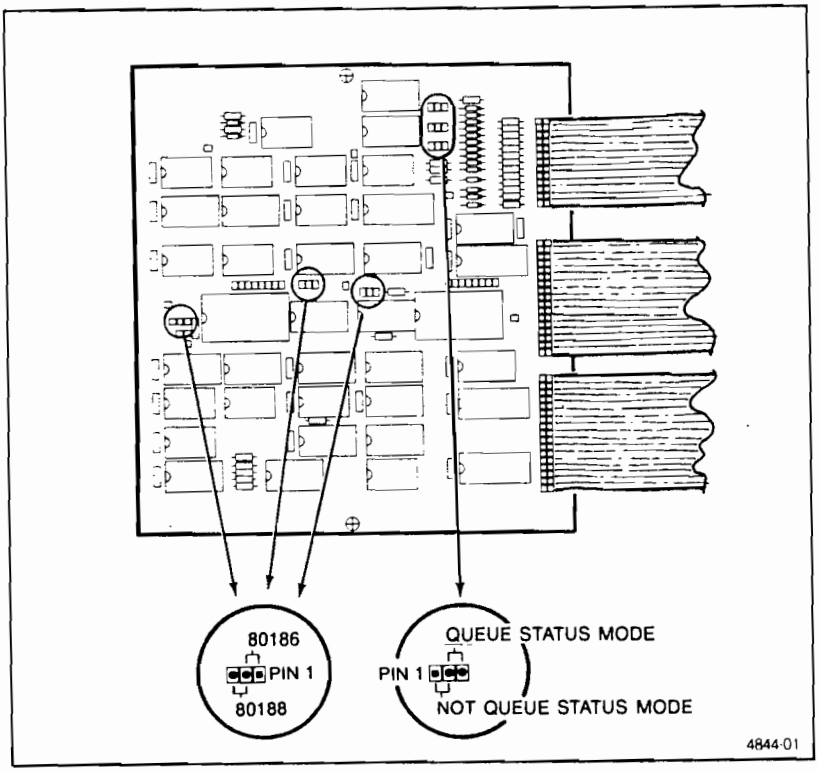


Figure 1. PM202 Configuration jumpers allow selection between normal and QS Mode, and between use with 80186s and 80188s.

CONNECTING TO THE 80186

CONNECTING THE PM202 TO THE 80186

To use the PM202 Personality Module, your 80186 system must be equipped with a Textool 68-pin JEDEC Type A Socket. Connect the PM202 Personality Module to your circuitry using Figure 2 and the following procedure:

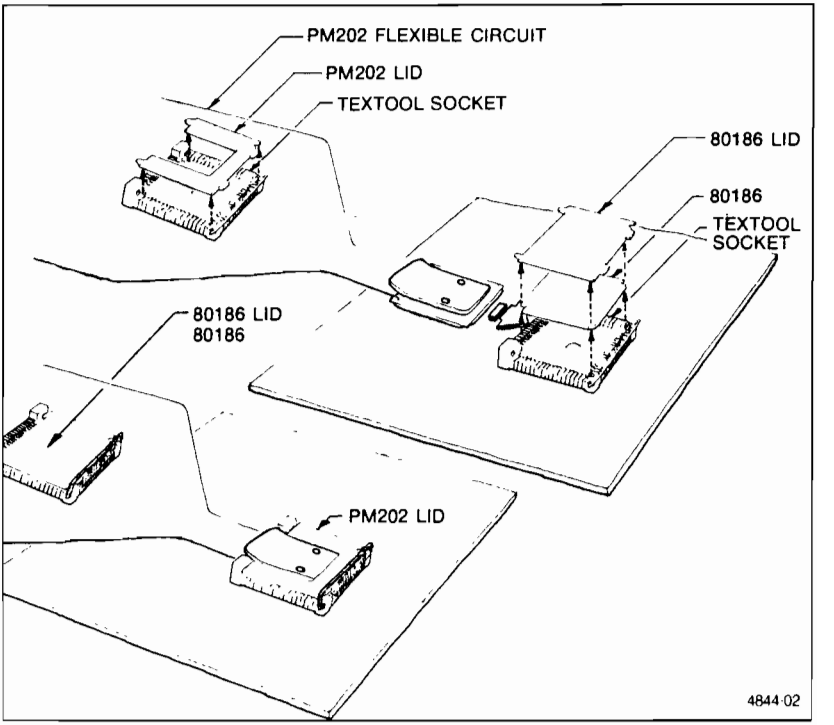


Figure 2. Connecting the PM202 to the 80186 circuit.

1. Turn off the power to your 80186 system and, if the PM202 is connected to it, the 1240.
2. Locate the chip carrier socket on the flexible circuit of the PM202. Remove the socket's U-shaped lid by slipping off the hold-down bail.

CAUTION

Only connect the PM202 to your 80186 system in a static-free environment and only after you have grounded yourself to drain static electricity.

3. Take the lid off of your 80186's carrier socket and remove the 80186.
4. Put the 80186 in the socket on the PM202 flexible circuit. Be sure it is oriented so that pin 1 connects to pin 1. The pin 1 corner of the chip is diagonal rather than notched like the other corners.
5. Put the lid from your 80186 system over the 80186 in the PM202 chip carrier. Fasten the lid with the hold-down bail.
6. Now, put the connector on the end of the PM202 flexible circuit into your 80186 system's chip carrier socket. Be sure it is oriented so that pin 1 connects to pin 1. (The four corners of the PM202 connector have the same registration scheme as the 80186.)

CAUTION

Make sure that the chip-carrier socket on the PM202 does not contact circuitry in your 80186 system. While the socket's lid is anodized and non-conductive, its wire hold-down bail could cause a short circuit.

7. Cover the PM202 connector using the U-shaped lid supplied with the PM202. Fasten the lid with the hold-down bail.

CAUTION

Always use care to avoid nicking the edge of the flexible circuit of the PM202. It is very resistant to stretching and bending, as long as its surface is intact. But, if its edge is nicked, its resistance to tearing is greatly lowered.

CONNECTING THE PM202 TO THE 1240

Remove any data acquisition probes from the three highest-numbered 1240D2 cards of the 1240. The six ribbon cables from the PM202 connect directly to the 1240D2 18-channel acquisition cards of the 1240; no data acquisition probes are required.

Connect the connectors on the six ribbon cables of the PM202 to the pods of the 1240 in accordance with the information in Table 1.

Table 1
PM202 TO 1240 CONNECTIONS

PM202 Connector		1240 Pod I.D. Number for:	
1240	(DAS)	3 Acq. Cards	4 Acq. Cards
0	(1A)	0	2
1	(1B)	1	3
2	(1C)	2	4
3	(2A)	3	5
4	(2B)	4	6
5	(2C)	5	7

CONNECTION OVERVIEW

Table 2 provides an overview of the connections between the 1240 Logic Analyzer equipped with an 80186 Mnemonics ROM Pack and your 80186 microprocessor through the PM202 Personality Module.

Table 2
1240 TO PM202 AND 80186 SIGNAL MAP

1240 SCREEN			CONNECTION		80186 (OR PM202)	
GROUP	BIT	C/Q	POD*	CHAN	SIGNAL	PIN
CNTL	3	-	5	7	INT	PM202
	2	-	5	6	C2	PM202
	1	-	5	5	C1	PM202
	0	-	5	4	C0	PM202
ADDR	19	-	5	3	A_{19}	65
	18	-	5	2	A_{18}	66
	17	-	5	1	A_{17}	67
	16	-	5	0	A_{16}	68
	15	-	3	7	AD_{15}	1
	14	-	3	6	AD_{14}	3
	13	-	3	5	AD_{13}	5
	12	-	3	4	AD_{12}	7
	11	-	3	3	AD_{11}	10
	10	-	3	2	AD_{10}	12
	9	-	3	1	AD_9	14
	8	-	3	0	AD_8	16
	7	-	0	7	AD_7	2
	6	-	0	6	AD_6	4
	5	-	0	5	AD_5	6
	4	-	0	4	AD_4	8
	3	-	0	3	AD_3	11
	2	-	0	2	AD_2	13
	1	-	0	1	AD_1	15
	0	-	0	0	AD_0	17
DATA	15	-	4	7	AD_{15}	1
	14	-	4	6	AD_{14}	3
	13	-	4	5	AD_{13}	5
	12	-	4	4	AD_{12}	7
	11	-	4	3	AD_{11}	10
	10	-	4	2	AD_{10}	12
	9	-	4	1	AD_9	14
	8	-	4	0	AD_8	16
	7	-	1	7	AD_7	2
	6	-	1	6	AD_6	4
	5	-	1	5	AD_5	6
	4	-	1	4	AD_4	8
	3	-	1	3	AD_3	11
	2	-	1	2	AD_2	13
	1	-	1	1	AD_1	15
	0	-	1	0	AD_0	17
(none)	-	P0	0	C/Q	$\overline{DEN}$	39
	-	P2	2	C/Q	ALE	61

* Pod numbers are shown for a 1240 with three 1240D2 acquisition cards installed. If your 1240 has four acquisition cards, add 2 to the pod numbers given.

ROM PACK INSTALLATION

1240 CONFIGURATION

In order to acquire data from an 80186 microprocessor using the 80186 Mnemonics ROM Pack, it is necessary to have a 1240 Logic Analyzer equipped with at least three 1240D2 18-channel Data Acquisition Cards.

NOTE

The 80186 Mnemonics ROM Pack will not set up the 1240 or disassemble data when it is installed in a 1240 with less than three 1240D2 acquisition cards.

INSTALLING THE ROM PACK

CAUTION

Static discharge can damage the semiconductor devices in a Mnemonics ROM Pack. Discharge static from a pack before installing it by momentarily laying the pack, label side up, on the top of the 1240.

To install the 80186 Mnemonics ROM Pack in your 1240 Logic Analyzer, locate the slot on the right side of the instrument, beneath the probe connectors. Insert the connector end of the ROM Pack, with the label up, past the hinged slot cover and into the memory pack connector. (The mechanical design of the pack ensures that it cannot be installed incorrectly.) Refer to Figure 3.

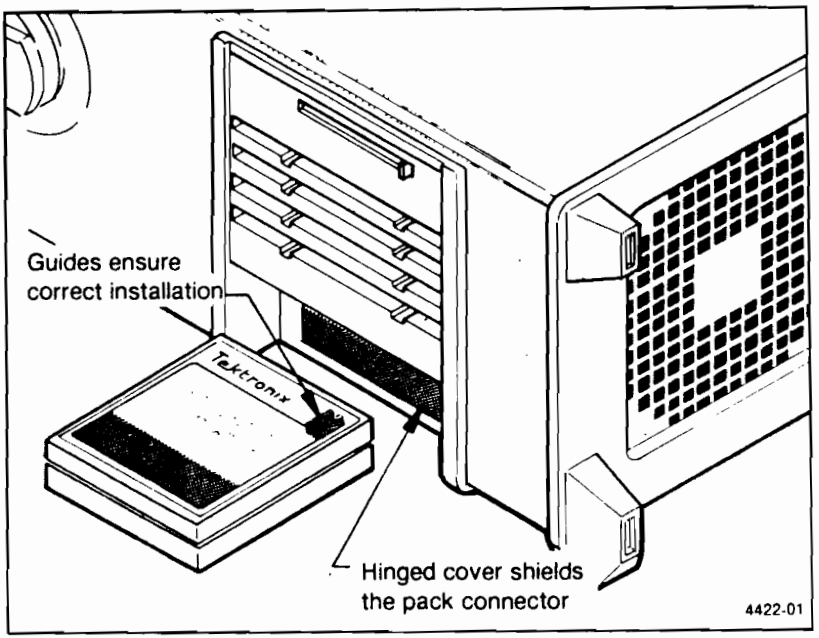


Figure 3. Installing the ROM Pack in a 1240.

Power up your 1240. The contents of the ROM Pack will be loaded automatically at powerup. If your 1240 was already on when the ROM Pack is installed, follow the next procedure, *Loading the ROM Pack Contents.*

NOTE

The 1240 should use the same power source as the system under test. Otherwise, differences between system grounds may cause inconsistent acquisition.

LOADING THE ROM PACK CONTENTS

Enter the Storage Memory Manager menu. Then press the LOAD NEW PACK soft key. The ROM Pack is now loaded.

CAUTION

Do not remove the ROM Pack while you are in any menu other than Storage Memory Manager. Removing it at any other time may cause complete disruption of the 1240's internal memory. To restore the 1240, turn it off and back on.

REMOVING THE ROM PACK

To unload the ROM Pack from the 1240, enter the Storage Memory Manager menu, pull the ROM Pack straight out of the 1240 (it is not necessary to power down), and press LOAD NEW PACK.

CAUTION

After removing the ROM Pack, do not leave the Storage Memory Manager menu without pressing the LOAD NEW PACK soft key. Doing so may cause complete disruption of the 1240's internal memory. To restore the 1240, turn it off and back on.

THE SETUP SUPPLIED BY THE ROM PACK

When the 80186 Mnemonics ROM Pack is loaded into a 1240 with three or more 1240D2 cards, several things happen:

- The 1240 enters Operation Level 2, ADVANCED STATE ANALYSIS. If you manually leave level 2 for levels 0 or 1, you will ruin the setup supplied by the ROM Pack. Using level 3 (after you load the Pack) will not cause a problem.
- All 1240D2 chaining is turned off.
- The thresholds are set to TTL on the three 1240D2s used by this ROM Pack.
- All polarities are set to 1 (positive - true) on the three 1240D2s used by this ROM Pack.
- T2 is redefined as DEMUX. See *Timebase Definitions* later in this manual.
- The first pod used by the ROM Pack is clocked by T2 F and used to acquire the low order bits of the ADDR group.
- The second pod used by the ROM Pack is clocked by T2 F and used to acquire the low order bits of the DATA group.
- The third pod used by the ROM Pack is clocked by T2 L and contains reserved channels used by the ROM Pack and the PM202 to accomplish postprocessing of acquired data. The channel 8 of the fourth pod used by the ROM Pack is also reserved for this purpose. Do not attempt to use any of these channels.
- The fourth pod used by the ROM Pack is clocked by T2 F and used to acquire bits 8 - 15 of the ADDR group.
- The fifth pod used by the ROM Pack is clocked by T2 F and used to acquire the high order bits of the DATA group.
- The sixth pod used by the ROM Pack is clocked by T2 L and used to acquire bits 16 - 19 of the ADDR group and the CNTL group.
- The radices of the CNTL group are set to BINary, while those of the ADDR and DATA groups are set to HEXadecimal.

NOTE

If you attempt to use the 80186 Mnemonics ROM Pack in a 1240 that does not have at least three 1240D2s, the 1240 setup will not be modified.

Table 3 summarizes the way the 80186 Mnemonics ROM Pack sets up the last three 18-channel cards in the 1240.

Table 3
HOW THE 80186 ROM PACK SETS UP THE 1240

GROUP	TIME BASE	INPUT RADIX	DISPLAY RADIX	THRESHOLD, POLARITY	POD*: CHANNELS
CNTL	T2 L	BIN	BIN	TTL, all +	**5**: 7-4
ADDR	T2 L	HEX	HEX	TTL, all +	**5**: 3-0
	T2 F	HEX	HEX	TTL, all +	**3**: 7-0
	T2 F	HEX	HEX	TTL, all +	**0**: 7-0
DATA	T2 F	HEX	HEX	TTL, all +	**4**: 7-0
	T2 F	HEX	HEX	TTL, all +	**1**: 7-0

* Pod numbers are shown for a 1240 with a total of three 1240D2 acquisition cards installed. If your 1240 has four acquisition cards, add 2 to the pod numbers given.

MENU AND DATA DISPLAY DIFFERENCES

- The Timebase, Memory Config, and Channel Grouping menus are set up as shown in Table 3. Do not change these settings except as described in the subsection, *What You May Change*.
- Every menu that uses groups contains the CNTL, ADDR, and DATA groups set up by the ROM Pack.
- If a 1200C01 RS232C or a 1200C11 Parallel Printer COMM Pack is installed, the COMM PORT CONTROL menu is replaced by the LINE PRINTER OUTPUT menu. Line printer operation is described later in this manual.
- The STATE TABLE soft key label changes to 80186 STATE TABLE while you are in the State Table menu.
- Also in the State Table display, GLITCHES ON/OFF is replaced by a FORMAT select field. This is where you choose a data display format. The choices are STATE, ABSOLUTE, HARDWARE, and SOFTWARE. The differences between these formats are discussed in detail later in this manual. You can still make the choice of GLITCHES ON or GLITCHES OFF in the Timing Diagram menu; the State Table display will reflect that choice.
- In the Timing Diagram display, the active cursor value at the bottom of the display is shown in STATE, ABSOLUTE, or HARDWARE format depending on the selection made in the State Table menu. (If you select SOFTWARE disassembly in the State Table menu, readouts in the Timing Diagram will appear in HARDWARE format.)

TIMEBASE DEFINITIONS

The 80186 Mnemonics ROM Pack sets up the 1240 to use Timebase 2 in the DEMUXed mode. T2 F is then used to store the DATA group and all of the ADDR group, except bits 16-19. T2 L is used to store the CNTL group and bits 16-19 of the ADDR group. Timebase T2 F is set up to be the *rising* edge of $\overline{\text{DEN}}$. Timebase T2 L is set up to be the *falling* edge of ALE. Refer to Table 4.

Table 4
DEFAULT SETUP OF CLOCK QUALIFIERS

Clock Qualifier	Pod Number		T2 F		T2 L	
	3 Acq. Cards	4 Acq. Cards	ORed Clock	ANDed Qual.	ORed Clock	ANDed Qual.
$\overline{\text{DEN}}$	0	2	rising			
ALE	2	4			falling	

CLKOUT. The CLKOUT signal from the 80186 is available on the clock/qualifier channel of pod 1. This allows acquisition of data on every internal cycle of the 80186. Obviously, disassembly will not work if you use this clock instead of those provided by default, but you may find that CLKOUT is most useful for detailed monitoring of the microprocessor.

Additional User Qualification. If your 1240 has four acquisition cards, you may use that extra clock/qualifier channel to further qualify Timebase 2. *HOWEVER*, correct disassembly is not guaranteed when you do this.

WHAT YOU MAY CHANGE

Much of the setup provided by the 80186 Mnemonics ROM Pack cannot be disturbed without seriously impairing the disassembly of your data, but you can safely make the following modifications:

- You may change radices anywhere, but your choices will be ignored in some display formats.
- You may reorganize the CNTL group; the ROM Pack will retain its own internal grouping for processing purposes.
- You may change anything having to do with timebase T1; the 80186 Mnemonics ROM Pack only uses T2.
- You may change the configuration or grouping of any acquisition card not used by the ROM Pack (as long as you do not chain the 1240D2s). The 80186 Mnemonics ROM Pack uses only the three highest-numbered 1240D2 (18-channel) acquisition cards.

NOTE

Do not chain your 18-channel cards. Doing so disrupts the setup supplied by the ROM Pack.

STORING AND USING A MODIFIED SETUP

When you have created and verified a modified setup for your 1240 that is compatible with the Mnemonics ROM Pack, you can store it and retrieve it using the following procedures:

Storing a Modified Setup

- Go to the Storage Memory Manager menu (UTILITY key).
- Remove the Mnemonics ROM Pack.
- Install a RAM Pack, press LOAD NEW PACK, and store your setup (FILETYPE: SETUP, STORED IN: PACK).

Using a Modified Setup

- Go to the Storage Memory Manager menu (UTILITY key).
- Install your RAM Pack, press LOAD NEW PACK, and load the file containing the modified setup.
- Store that setup in the 1240's internal RAM (FILETYPE: SETUP, STORED IN: RAM).
- Remove the RAM Pack, install the Mnemonics ROM Pack, and press LOAD NEW PACK.
- Retrieve your modified setup from the 1240's internal RAM and proceed.

DATA QUALIFICATION AND TRIGGERING

IDENTIFYING CYCLE TYPES

To use either the Global or Sequential Event Recognizers effectively, you need to be able to identify cycle types. Cycle types are decoded from the three low-order channels of the CNTL group according to the relationships shown in Table 5.

Table 5
IDENTIFYING CYCLE TYPES

CYCLE TYPE	CNTL GROUP 210	OCTAL
INT ACK	000	0
I/O READ	001	1
I/O WRITE	010	2
QUE DUMP	011	3
FETCH or FETCH N	100	4
MEM READ	101	5
MEM WRITE	110	6
DMA	111	7

SPECIFYING CYCLE TYPES

To specify a particular cycle type as a condition for data qualification or triggering, enter the values shown in Table 5 for that cycle type in the CNTL field of the event recognizer.

CNTL Group Modification. You may split up the CNTL group, or rearrange its channels, or change its radix, without affecting disassembly. The ROM Pack maintains for its internal use a version of the group as it originally set it up. This allows you to take individual channels out of the CNTL group or create your own sub-groups with names that suggest the sub-set of channels you include or the way you are using them. (Of course, reorganization of the CNTL group means that you can no longer use the values given in Table 5.)

INT (CNTL 3). This PM202 generated signal is the OR'ed sum of interrupts INT_0 and INT_1 from pins 44 and 45 of the 80186.

80186 CYCLE TYPE DEFINITIONS

DMA A direct memory access cycle. The 80186 is engaged in an internal DMA. (There is no way to clock in external DMAs; they are not acquired by the PM202.)

FETCH A memory read cycle in which the first byte of an instruction is fetched for execution (on either the high byte, low byte, or both).

FETCH N A memory read cycle in which neither the high byte nor the low byte is an opcode, but both bytes are part of an instruction.

I/O READ A cycle in which data is read from an I/O port.

I/O WRITE A cycle in which data is written to an I/O port.

MEM READ Any cycle, other than an opcode FETCH or FETCH N cycle, in which data is read from memory. An event recognizer set for MEM READ cycles can be modified to include fetch cycles by entering an X (don't care) in bit 0 of the default CNTL group. Byte size reads are displayed with the meaningless byte replaced by dashes, e.g. – –XX.

MEM WRITE Any cycle in which data is written to memory by the 80186. Byte size writes are displayed with the meaningless byte replaced by dashes, e.g. – –XX.

QUE DUMP Any cycle in which the instruction queue in the 80186 is emptied due to a change in the instruction stream. (Step B-2 and B-3 versions of the 80186 contain a bug which sometimes produces erroneous queue tracking information.)

TRIGGERING ON ODD ADDRESSES

Except when it jumps to odd addresses, the 80186 reads code by words from *even* address boundaries. If you attempt to trigger on an odd address value to find an instruction, you will only get a trigger if that address is accessed as the result of a program transfer (jump-like) instruction. To avoid this problem, use the even address below the odd address you are looking for as your trigger value. (HARDWARE and SOFTWARE disassembly formats will display the odd address for first fetches which are actually stored at odd addresses, even though you cannot trigger on that value.)

DISPLAYING DISASSEMBLED DATA

INSTRUCTION MNEMONICS

This ROM Pack disassembles in the Intel 80186 mnemonics syntax used in *iAPX 86/88,186/188 User's Manual Programmer's Reference* (1983) by Intel Corporation (Intel order number: 210911-001). Numeric operands in disassembled instructions are always displayed in hexadecimal.

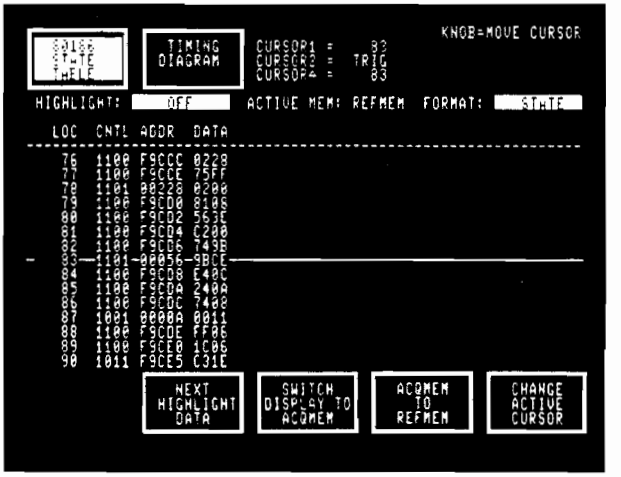
DISPLAY FORMATS

The mnemonics and cycle type information generated by the 80186 Mnemonics ROM Pack is available in the STATE TABLE display (accessed by pressing the DATA key). You have three choices of disassembly formats in addition to the standard state table display. You select the display format by placing the blinking field cursor in the FORMAT field and using the SELECT keys to indicate your choice.

NOTE

If you attempt to use the 80186 Mnemonics ROM Pack in a 1240 that does not have at least three 1240D2s, you will get an INSUFFICIENT 1240D2 CARDS TO SUPPORT DISASSEMBLY message in the State Table menu and only the (standard) STATE display format will be available.

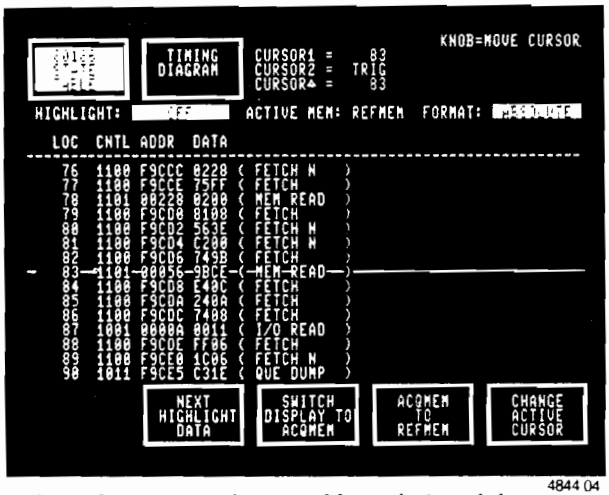
STATE. This is the standard 1240 State Table format that you get without the 80186 Mnemonics ROM Pack installed. This format is also the only one available in AUTO-RUN or when you have less than three 1240D2 cards installed (FORMAT field is not present). Look at Figure 4.



4844 03

Figure 4. STATE format is standard without the ROM Pack.

ABSOLUTE. This format is like the STATE format, but is enhanced by the addition of cycle type information. Look at Figure 5.



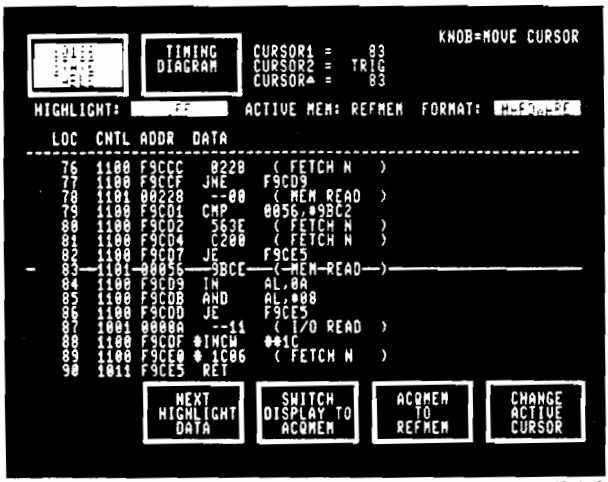
4844 04

Figure 5. ABSOLUTE format adds cycle type information.

HARDWARE. In this format, instruction mnemonics are displayed in the DATA group on FETCH cycles, and cycle type information is provided on all other cycles. Meaningless data bus values, such as the unused half of the bus during byte transfers, are replaced by dashes. The mnemonics for cycles which are discarded as the result of QUE DUMPS are shown preceeded by an asterisk. Look at Figure 6.

NOTE

User choices of display radix are overridden in the HARDWARE display format. The ADDR and DATA groups are always shown in HEX. To see the data in these groups in your choice of radix, use the FORMAT select field to switch back and forth between this format and ABSOLUTE or STATE.



4844 05

Figure 6. HARDWARE format shows instruction mnemonics.

SOFTWARE. This display format is designed to look like a source code listing and thus make analysis of the program flow easier. It is similar to HARDWARE except that DMAS, FETCH N, and flushed FETCH cycles are suppressed and only the CNTL, ADDR, and DATA groups are available. Also, meaningless data bus values, such as the unused half of the bus during byte transfers, are replaced by dashes. Look at Figure 7.

The suppression of cycles resulting from the transition from any other format to SOFTWARE may cause the data cursors to move.

NOTE

User choices of display radix are overridden in the SOFTWARE display format. The ADDR and DATA groups are always shown in HEX. To see the data in these groups in your choice of radix, use the FORMAT select field to switch back and forth between this format and ABSOLUTE or STATE.

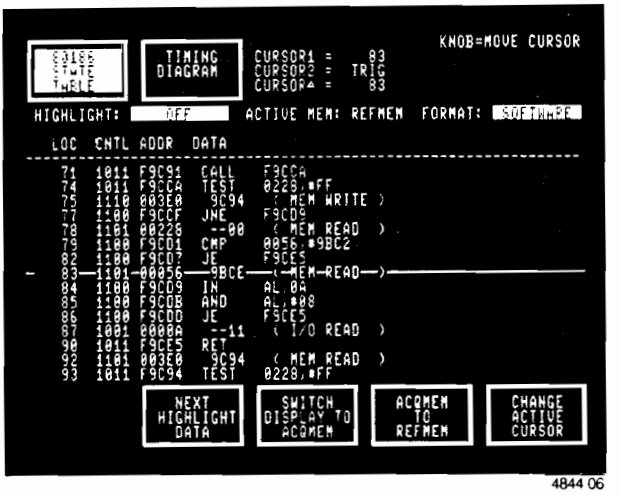


Figure 7. SOFTWARE format suppresses non-fetch instruction reads.

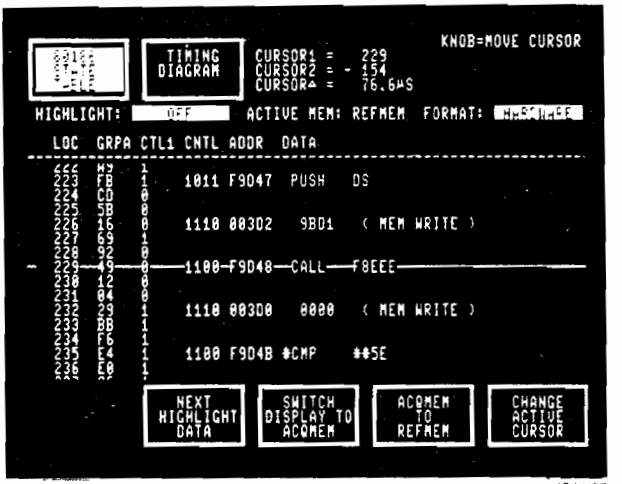
TIMING DISPLAYS

In the Timing Diagram menu, the active cursor value readout at the bottom of the data display reflects your choice of disassembly FORMAT in the State Table menu, with one exception: When you select SOFTWARE in the State Table menu, the readout in the Timing Diagram will be in HARDWARE format.

DUAL TIMEBASE DISPLAYS

You may use T1 with the fourth acquisition card in your 1240 if it has one. The ROM Pack only uses the three 18-channel cards with the highest pod numbers.

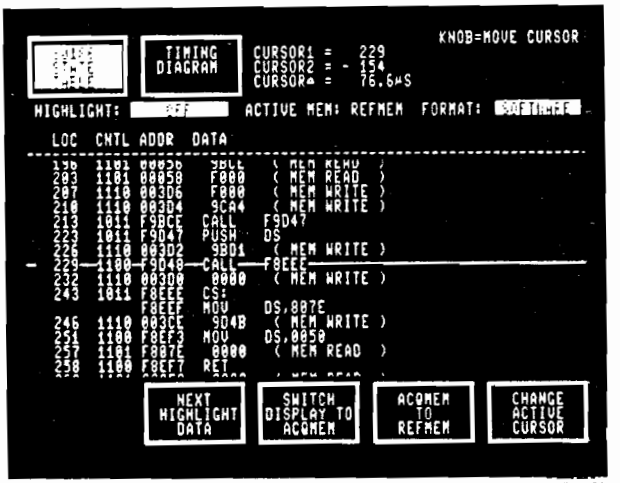
In the STATE, ABSOLUTE, and HARDWARE formats, the data acquired on T1 is correlated with the T2 data acquired from the 80186. Refer to Figure 8 to see T1 data correlated with 80186 data.



4844 07

Figure 8. T1 data correlated with 80186 data.

When you select SOFTWARE as the data display format, T1 data is suppressed in the interest of giving you the best possible overview of the 80186 program flow. Refer to Figure 9 and contrast it with Figure 8.



4844 08

Figure 9. T1 data is suppressed in SOFTWARE format.

EDITING THE REFERENCE MEMORY

If you edit a portion of your reference memory, you should also edit the reserved channels associated with that portion of memory to avoid disassembly anomalies. Ten channels are reserved by the ROM Pack for post-acquisition processing of data to determine when instructions are flushed from the queue of the 80186. Eight of these are used to store information from the PM202. Two of the channels are used to store the results of the post-processing and they must be edited as follows:

- POD 2, CHANNEL 8 should have a 1 placed in it when the *high byte was flushed* before it was executed.
- POD 3, CHANNEL 8 should have a 1 placed in it when the *low byte was flushed* before it was executed.

NOTE

Add 2 to the pod numbers shown if your 1240 has four acquisition cards.

You must also edit the four channels that contain fetch prediction information as shown is Table 8. These are channels 7 through 4 of the third pod used by the ROM Pack (pod 2 in a 1240 with three acquisition cards; pod 4 in a 1240 with four acquisition cards).

Table 8

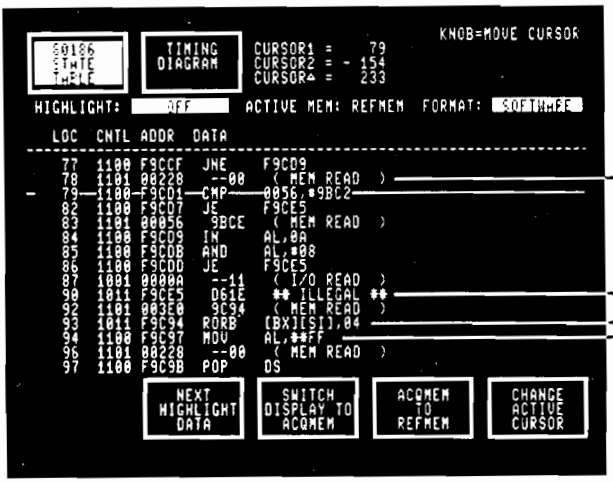
SIGNIFICANCE OF POD 2 CHANNELS*

HIGH BYTE	LOW BYTE	CH. 7-4
FETCH N	FETCH N	1010
FETCH N	FETCH	1011
FETCH	INVALID	1101
FETCH	FETCH N	1110
FETCH	FETCH	1111

* Pod numbers are shown for a 1240 with a total of three 1240D2 acquisition cards installed. If your 1240 has four acquisition cards, add 2 to the pod numbers given.

NON-STANDARD DISASSEMBLIES

When the 80186 Mnemonics ROM Pack encounters an unexpected combination of data, or when part of the data is missing, one of the indications shown in Figure 10 appears.



1 ***Byte size reads or writes*** are shown with dashes replacing the invalid data. Either byte may be invalid.

2 ***Illegal opcode*** indication. In the case of multibyte instructions, where the second or successive byte is either illegal or was not executed because of a queue flush, the first byte of the instruction is displayed. This indication can also occur when a problem in your software has caused an attempted execution at an erroneous address.

3 ***B or W suffix on opcode mnemonic*** is used to resolve an ambiguity about whether this instruction is performing its operation on a byte or a word. This is only done for those instructions and addressing modes where such an ambiguity occurs.

4 ***Missing data - operand not disassembled*** signals that part of the instruction was not stored in the acquisition memory. This can arise at the end of memory, or during a queue flush, or when some sort of data qualification has prevented the complete storage of an instruction. A single asterisk is displayed for each missing hexadecimal digit or register name.

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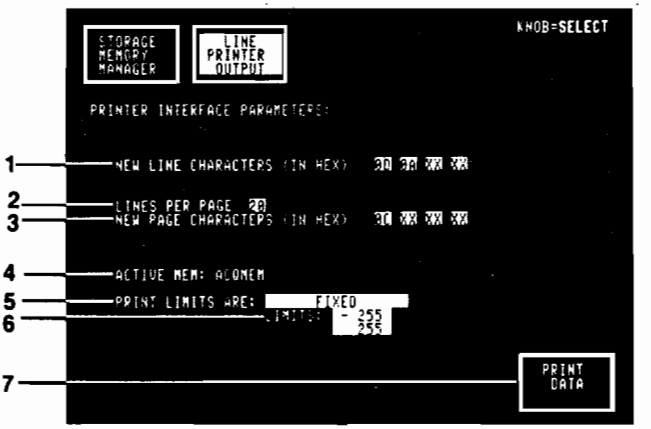
Figure 10. Non-standard disassemblies.

LINE PRINTER OUTPUT

When the 80186 Mnemonics ROM Pack is installed in a 1240 that also has a 1200C01 RS232C or 1200C11 Parallel Printer COMM Pack installed, the UTILITY menu presents a soft key labeled LINE PRINTER OUTPUT replacing the COMM PORT CONTROL key. The menu accessed by this key allows you to send your state data displays to a line printer in the current format. Refer to Figures 11 and 12.



1 NEW LINE CHARACTERS: Use these hexadecimal fields to define a string of from one to four characters that will be appended to each line. The first field must have an entry, but the last three fields can be filled with **X**s (don't cares).

2 LINES PER PAGE: Use this decimal field to specify the number of lines that will be printed on each page. Valid values range from 1 to 99.

3 NEW PAGE CHARACTERS: Use these hexadecimal fields to define a string of from one to four characters that will follow the end of every page. The first field must have an entry, but the last three fields can be filled with **X**s (don't cares).

4 ACTIVE MEM: This field is for information only. Change the active memory in the State Table or Timing Diagram menus.

5 PRINT LIMITS ARE: Use this field to indicate whether the area of active memory to be printed will be defined by FIXED LIMITS or BETWEEN CURSORS. When BETWEEN CURSORS is selected, the area of the active memory that will be printed is defined by the data cursors (inclusive).

6 LIMITS: This field becomes active when FIXED LIMITS is selected in the PRINT LIMITS ARE field. Entries here specify the first and last line of memory to be printed. When PRINT LIMITS ARE: BETWEEN CURSORS, this field displays the locations of the cursors.

7 PRINT DATA: Touch this soft key to start the transmission of data. It will remain lighted during the transfer. Use the STOP key to interrupt the transmission, if necessary.

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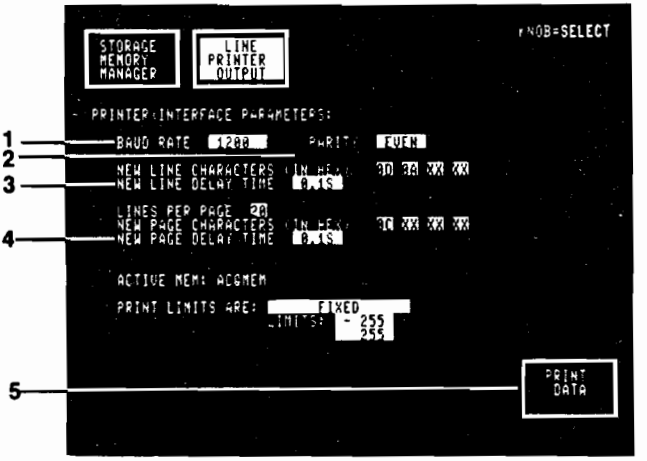
Figure 11. LINE PRINTER OUTPUT menu when 1200C11 is installed.

NOTE

Do not attempt to control the 1240 remotely using an RS232C COMM Pack while any Mnemonics ROM Pack is installed.



1 BAUD RATE: Use this field to specify the baud rate at which the 1240 will supply data to the printer. The available choices are: 110, 134.5, 150, 300, 600, 1200, 2400, 4800, and 9600.

2 PARITY: Use this field to make parity choices of ODD, EVEN, and NONE. If your printer uses the 8th (parity) bit for something other than parity, set this field to NONE.

3 NEW LINE DELAY TIME: Use this field to specify the minimum time delay between the transmission of successive lines by the 1240. The choices range from NONE to 9.9 SEC in 100 ms steps.

4 NEW PAGE DELAY TIME: Use this field to specify the minimum amount of time delay between the transmission of the last line of one page and the first line of the next page. The choices range from NONE to 9.9 SEC in 100 ms steps.

5 PRINT DATA: Touch this soft key to start the transmission of data. Use the STOP key to interrupt the transmission, if necessary. This key places the 1240 ONLINE when the 1200C01 RS232C COMM Pack is installed. If the device being transmitted to is capable of transmitting back, spurious remote commands can affect the operation of the 1240. Also, during a PRINT DATA operation, the 1200C01 parameters are modified. Therefore, do not attempt to control the 1240 remotely while any Mnemonics ROM Pack is installed.

4844 11

Figure 12. LINE PRINTER OUTPUT menu when 1200C01 is installed. Refer to Figure 11 for a description of those fields that are the same in both menus. Refer to the *RS232C COMM Pack 1200C01 Operator's Manual* for information on handshaking protocols and the use of null modems.

ERROR MESSAGES

When used with an 80186 Mnemonics ROM Pack, the 1240 Logic Analyzer uses some error messages that are different from those it normally displays. Also, some of the normal error messages have additional meanings when they are used with this ROM Pack.

APPLYING SEARCH PATTERN - PLEASE WAIT — This message occurs briefly twice during a data acquisition with the 80186 Mnemonics ROM Pack installed, unless PATTERN SEARCH DISABLED is selected.

CONFIG ERROR — This message always appears in the State Table display after power-up with an 80186 Mnemonics ROM Pack installed. It indicates that the setup used to acquire the current acquisition memory and the current setup from the 80186 Mnemonics ROM Pack are inconsistent. Acquiring new data should make this message go away. (Refer to the *Reference Information* section of the *1240 Logic Analyzer Operator's Manual* for a complete discussion of this message.) This message also appears in the LINE PRINTER OUTPUT menu if the current configuration does not permit a PRINT DATA operation to be performed.

INSUFFICIENT 1240D2 CARDS TO SUPPORT DISASSEMBLY — This message indicates that your instrument does not have enough 18-channel cards to support the use of this Mnemonics ROM Pack.

MEMORY TIMEBASE ASSIGNMENTS WILL NOT SUPPORT DISASSEMBLY — The memory being displayed cannot be disassembled because it was acquired with a setup that does not support disassembly. Go to the Storage Memory Manager menu and press LOAD NEW PACK to get a setup that will support disassembly. Then, acquire new data using that setup.

NO VALID DATA ACQUIRED — This message indicates that either no T2 data was acquired or that the acquired data was so heavily qualified that what was left of it disappeared during (SOFTWARE) disassembly.

PRESS "STOP" TO TERMINATE OPERATION — This message tells you the correct way to stop a PRINT DATA operation. Since letting the printing operation finish or stopping it are your only choices once a printout is in progress, the 1240 assumes that you want to stop printing if you touch any key.

PM202 SPECIFICATIONS

Table 6 contains the environmental specifications for the PM202. Note that the environmental specifications for the PM202 are more restrictive than those for the 1240 Logic Analyzer itself.

The specifications shown in Table 7 refer to a 1240 Logic Analyzer system which includes a PM202 Personality Module.

Table 6
PM202 ENVIRONMENTAL SPECS

Characteristic	Description
Temperature	
Operating	0°C - 50°C
Storage	−55°C - 75°C
Humidity	0% - 90%
Altitude (max.)	
Operating	15,000 feet
Storage	50,000 feet

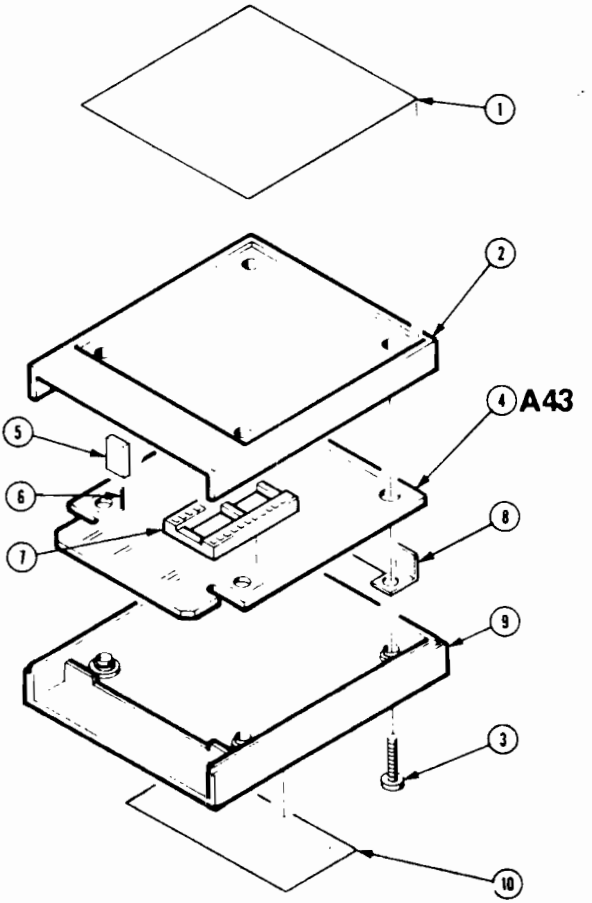
Table 7
PM202 - 1240 SYSTEM SPECS

Characteristic	Performance Requirement	Supplemental Information
CLK OUT Frequency	10 MHz max.	
Data Setup Time	30 ns min.	Measured from ⨍ $\overline{DEN}$
Data Hold Time	0 ns max.	Measured from ⨍ $\overline{DEN}$
Delays*		
ALE ⨍	32 ns min. 85 ns max.	Calculated from ⨍ CLKOUT prior to T1 (TCHLH)
ALE ⌊	39 ns max. 25 ns min.	Measured from ⨍ CLKOUT in T1 (TCHLL)
$\overline{WR}$ ⨍	55 ns max. 34 ns min.	Measured from ⌊ CLKOUT in T4 (TCVCTX)
$\overline{WR}$ ⌊	70 ns max. 27 ns min.	Measured from ⌊ CLKOUT in T2 (TCVCTV)
$\overline{RD}$ ⨍	55 ns max. 34 ns min.	Measured from ⌊ CLKOUT in T4 (TCLRH)
$\overline{RD}$ ⌊	70 ns max. 27 ns min.	Measured from ⌊ CLKOUT in T2 (TCLRL)
QS0	14 ns max.	Input to output transit time
QS1	36 ns max.	Input to output transit time
PM202 Output Levels Logical Lows Logical Highs	 0.8 V max. 2.4 V min.	
Input Capacitance		30 pF nominal
Max. Non-Destructive Input Voltage		−2 V to +7 V

* When the 80186 is installed in the PM202 flex-circuit, it always runs in the Queue Status mode. If the PM202 jumpers are configured for QSMD, the PM202 returns the 80186's queue status signals to the system under test. If the PM202 jumpers are configured for Not Queue Status Mode, the PM202 provides the system under test with synthesized ALE, $\overline{RD}$, and $\overline{WR}$ signals.

REPLACEABLE PARTS LIST
80186 MNEMONICS ROM PACK — 12RM05

NUMBER	TEK. P/N	DESCRIPTION
ELECTRICAL (REFER TO SCHEMATIC IN 1240 SERVICE MANUAL)		
A43	670-8172-00	CRT. BOARD ASSY: 32/64K MEMORY ROM PACK (U200, U300 EPROMs ARE NOT PART OF A43)
A43C100	281-0775-00	CAP, FIXED, CER, DI: 0.1 uF, 20%, 50V
A43C400	281-0775-00	CAP, FIXED, CER, DI: 0.1 uF, 20%, 50V
		CHASSIS PARTS
U200	160-2464-00	MICROCKT, DGTL: 16384 x 8 EPROM, PRGM
U300	160-2463-00	MICROCKT, DGTL: 16384 x 8 EPROM, PRGM
MECHANICAL (REFER TO EXPLODED VIEW DRAWING)		
1	334-0173-00	1 MARKER, IDENT: MKD 80186 ROM PACK
2	200-2503-01	1 COVER, ROM PACK: TOP
		(ATTACHING PARTS)
3	211-0012-00	4 SCREW, MACHINE: 4.40 x 0.375, PHD, STL
		— — * — —
4	- - - - -	CKT BOARD ASSY: 32/64K MEMORY ROM PACK (SEE A43 REPL)
5	131-0993-00	2 • BUS CONDUCTOR: 2 WIRE, BLACK
6	131-0608-00	6 • TERMINAL, PIN: 0.365 L x 0.025 PH BRZ GOLD
7	136-0755-00	2 • SKT, PL-IN ELEC: MICROCIRCUIT, 28 DIP
8	337-3122-00	1 SHIELD, ELEC: STATIC
9	200-2504-01	1 COVER, ROM PACK: BOTTOM
10	334-4727-00	1 MARKER, IDENT: MKD PROM PROGRAM IDENT
		STANDARD ACCESSORIES
	070-4844-00	MANUAL, TECH: INSTRUCTION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