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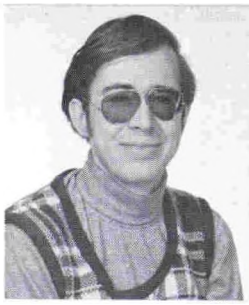
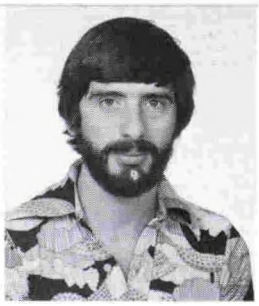
Cover: You can choose the display format best suited for your application, using the new DF1 Display Formatter, a companion plug-in for the TEKTRONIX 7D01 Logic Analyzer.



Dave Lowry



Jeff Bradford

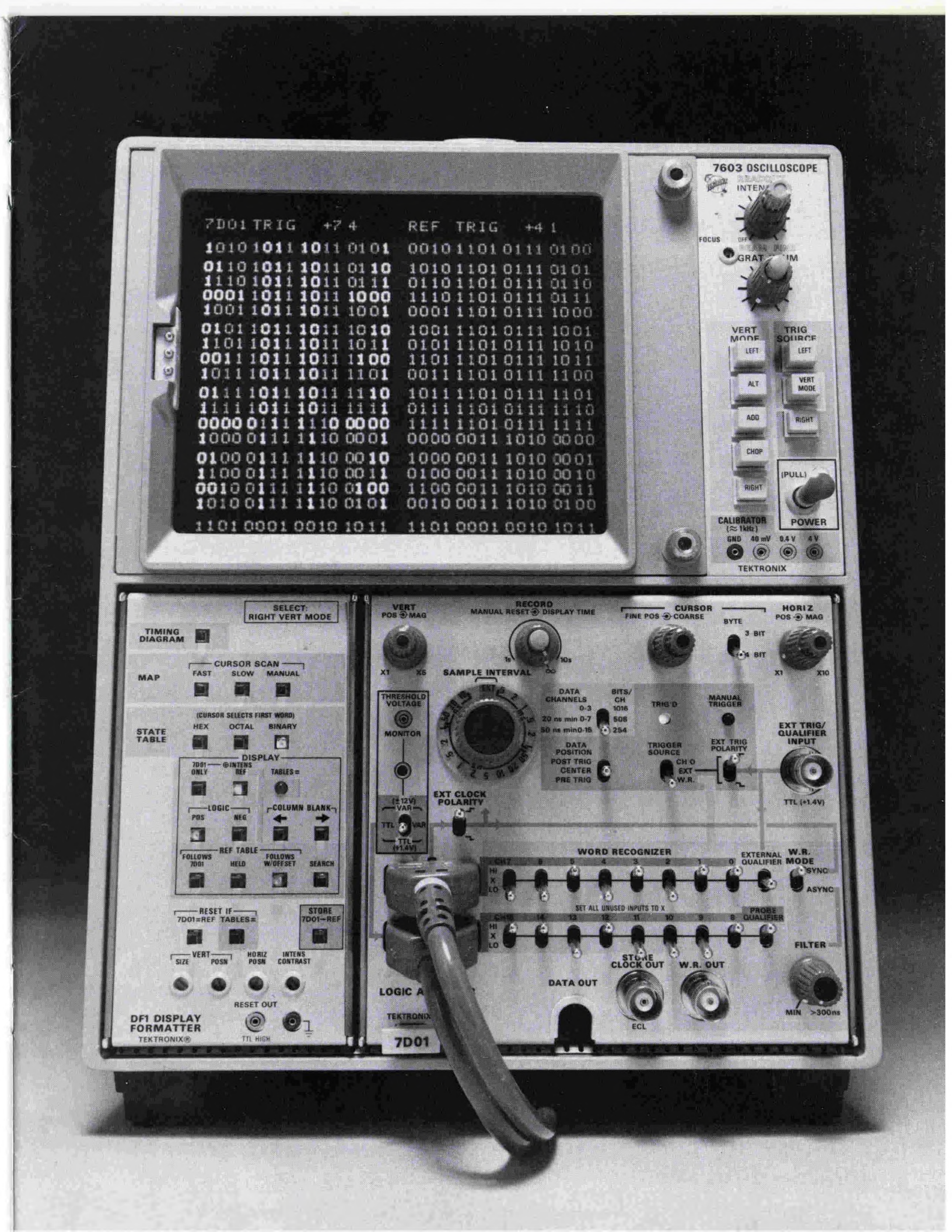
Rapid growth in the field of digital design and production—and especially the widespread use of microprocessors (μP) and minicomputers – has established the logic analyzer as an indispensible tool for the data domain. It has also created a need not just for a logic state or a logic timing analyzer, but for both capabilities. With the introduction of the new DF1 Display Formatter, Tektronix now offers both in one instrument.

A display formatter—the indispensable tool for the data domain

The DF1 is a dedicated, μP-based plug in for use only with the 7D01 7000-Series Logic Analyzer. The 7D01/DF1 combination (also called the 7D01F) constitutes the most versatile, as well as the most easily operated, logic analyzer available today, providing displays in mapping, state table, and timing diagram formats; state displays are available in hexidecimal, octal, or binary code. No other similar instrument offers such a wide range of display choices.

By itself, the 7D01 provides the type of display preferred by engineers who design and troubleshoot digital hardware—the standard timing diagram with simultaneous binary readout of the selected cursor word.

In combination with the DF1, the 7D01 now provides the state table formats and mapping displays favored by many. The state table format features an exclusive OR mode for ready comparisons of display and reference data. It also provides a reset function for automatic


7D01 TRIG +7 4
REF TRIG +4 1
7603 OSCILLOSCOPE
INTENS
FOCUS
VERT MODE
TRIG SOURCE
LEFT
ALT
ADD
CHOP
RIGHT
VERT MODE
RIGHT
(PULL)
POWER
CALIBRATOR
GND
40 mV
0.4 V
4 V
TEKTRONIX
SELECT: RIGHT VERT MODE
TIMING DIAGRAM
MAP
CURSOR SCAN
FAST
SLOW
MANUAL
(CURSOR SELECTS FIRST WORD)
STATE TABLE
HEX
OCTAL
BINARY
DISPLAY
7D01 ONLY
INTENS REF
TABLES=
LOGIC
POS
NEG
COLUMN BLANK
REF TABLE
FOLLOWS 7D01
HELD
FOLLOWS W/OFFSET
SEARCH
RESET IF 7D01=REF TABLES=
STORE 7D01=REF
VERT SIZE
VERT POSN
HORIZ POSN
INTENS CONTRAST
RESET OUT
TTL HIGH
DF1 DISPLAY FORMATTER
TEKTRONIX®
VERT POS MAG
X1
X5
RECORD
MANUAL RESET DISPLAY TIME
SAMPLE INTERVAL
CURSOR
FINE POS COARSE
BYTE
3 BIT
4 BIT
HORIZ POS MAG
X1
X10
THRESHOLD VOLTAGE
MONITOR
(±12V) VAR
TTL
VAR
TTL (+1.4V)
DATA CHANNELS
0-3
20 ns min 0-7
50 ns min 0-15
BITS/CH
1016
508
254
DATA POSITION
POST TRIG
CENTER
PRE TRIG
TRIG'D
MANUAL TRIGGER
TRIGGER SOURCE
CH 0
EXT
W.R.
EXT TRIG POLARITY
EXT TRIG/ QUALIFIER INPUT
TTL (+1.4V)
EXT CLOCK POLARITY
WORD RECOGNIZER
CH7 6 5 4 3 2 1 0
EXTERNAL QUALIFIER
W.R. MODE
SYNC
ASYNC
HI
X
LO
SET ALL UNUSED INPUTS TO X
CH15 14 13 12 11 10 9 8
PROBE QUALIFIER
FILTER
STORE CLOCK OUT
W.R. OUT
DATA OUT
ECL
MIN >300ns
LOGIC A
TEKTRONIX
7D01

comparisons with an output for triggering external equipment. For those who prefer a map mode for a quick look at program flow or patterns, the DF1 offers formattable mapping in 4, 8, or 16 channels.

Now let's take a closer look at each 7D01/DF1 display mode in turn.

State Display Modes

The STATE TABLE mode adds several unique features that enhance the power of the conventional state display. The standard 7D01/DF1 display consists of a table of up to 17 lines of 16-bit data words in hex, octal, or binary code. Negative or positive logic may be selected.

The state table is selected by the 7D01 cursor control. The table consists of the cursor word (the first word) and the 16 lines of data following the selected cursor word. In addition to the data, the trigger word is displayed at the bottom of the crt (as the 18th line).

When you're stepping forward through the memory 16 words at a time, the last word in the table becomes the cursor word in the next display, so that you can be sure you're paging through the data in the correct sequence. The trigger word remains the same until new data is acquired. When it also appears in the table, it flashes for identification.

The location of the cursor-selected word relative to the trigger word, measured in clock counts, is displayed in alphanumeric characters above the display.

The Exclusive OR Mode

In the exclusive OR mode, the 7D01/DF1 provides 4k-bit comparisons of new data and reference data. This is one of the most powerful analytical capabilities the 7D01/DF1 combination offers.

7D01 data from the circuit under test is displayed on the left-hand side of the crt, and reference data, transferred to the DF1 from an earlier 7D01 display, is displayed on the right. 7D01 data that differs from reference data is intensified for easy identification.

The RESET IF Mode

A unique RESET IF feature automatically resets the 7D01 to accept new data under two selectable conditions: (1) when the 7D01 table is identical to the reference table or (2) when the entire 4k memories of the 7D01 and reference are equal. (Any channel that has been column-blanked is not included in the comparison.) The 7D01 will continue to acquire new data until either the tables or the memories are no longer equal.

The first difference between 7D01 and reference is automatically positioned to the top of the display when the 7D01-REF button is activated. Then the display may be advanced table by table with the coarse 7D01 cursor control, or line by line with the fine control. A front-panel indicator will stay lit as long as both tables are equal.

Comparison Modes

Three comparison modes are available. In the FOLLOW mode, the cursor selects the data to be displayed from both memories with the same offset from the trigger. Line-by-line or table-by-table comparisons may now be made of new and reference data.

In the HELD mode, the selected reference table is retained, but the 7D01 data window may be advanced a line or table at a time, enabling a desired offset to be established between the two tables. Then the two sets of offset data may be compared in FOLLOWS W/OFFSET. This mode allows both tables to be advanced and compared while the desired offset is retained. This feature is quite useful in examining programs containing a repetitive series of instructions or operations.

In the SEARCH mode, the DF1 scans the 7D01 memory for a word identical to the reference cursor word (at the top of the reference table). When the first like word is encountered, it is displayed as the first word in the 7D01 table along with crt readout of its location relative to the trigger word. Repeated activation of the SEARCH button locates all other words in the memory that match the reference cursor word.

Mapping

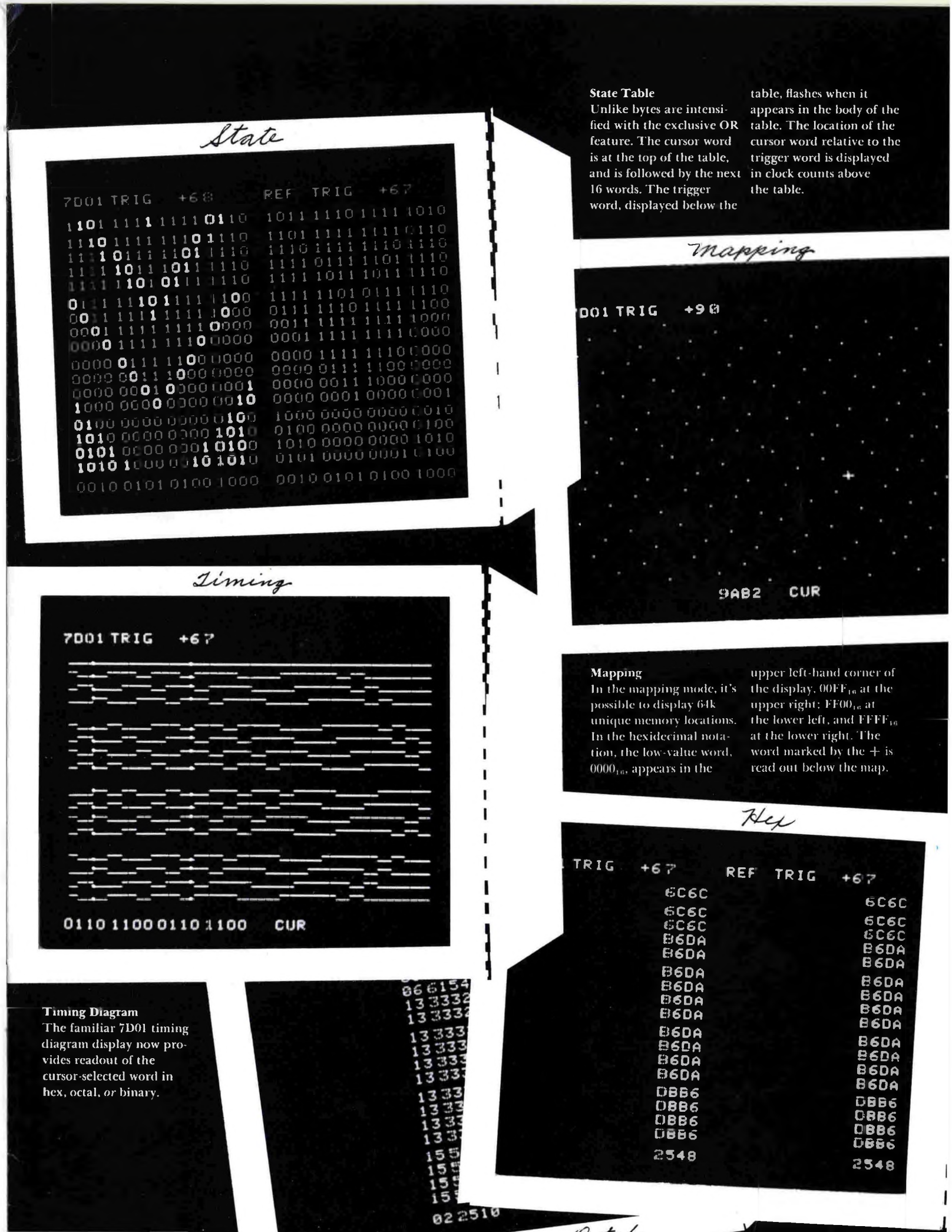
The DF1 also offers a mapping mode which enables an experienced user to get a quick overview of program flow or patterns.

Since the 7D01/DF1 memory is formattable in 4, 8, or 16 channels, acquired data may be formatted in a 4, 8, or 16-channel map. In other words, 8 or 4-channel data may be "spread out" over the map just as 16-channel data is.

In a 16-channel map, for example, 64k unique locations are possible. The most significant half of the characters of the word determines vertical location, while the least significant half determines horizontal location. 0000_{16} is located in the upper left of the display. As the last two characters increase from 0000_{16} to $00FF_{16}$, the word location moves across the top of the display from left to right; as the first two characters increase, the word location moves across the bottom from $FF00_{16}$ to $FFFF_{16}$.

In an 8-channel map, then, with 256 possible memory locations, the magnitude of the word ranges from 00_{16} (upper left) to $0F_{16}$ (upper right) from $F0_{16}$ (lower left) to FF_{16} (lower right). In a 4-channel map, there are 16 possible locations.

Mapped data is scanned manually or automatically with the + symbol in the same sequence that data is entered into the 7D01 memory. In the FAST or SLOW mode, the + is automatically positioned to each data word or location. In MANUAL operation, the + (controlled by clockwise or counterclockwise rotation of the 7D01 cursor control) steps forward or backward through



State Table
Unlike bytes are intensified with the exclusive OR feature. The cursor word is at the top of the table, and is followed by the next 16 words. The trigger word, displayed below the table, flashes when it appears in the body of the table. The location of the cursor word relative to the trigger word is displayed in clock counts above the table.

Mapping
In the mapping mode, it's possible to display 64k unique memory locations. In the hexidecimal notation, the low-value word, 0000_{16}, appears in the upper left-hand corner of the display, $00FF_{16}$ at the upper right; $FF00_{16}$ at the lower left, and $FFFF_{16}$ at the lower right. The word marked by the + is read out below the map.

Timing Diagram
The familiar 7D01 timing diagram display now provides readout of the cursor-selected word in hex, octal, *or* binary.

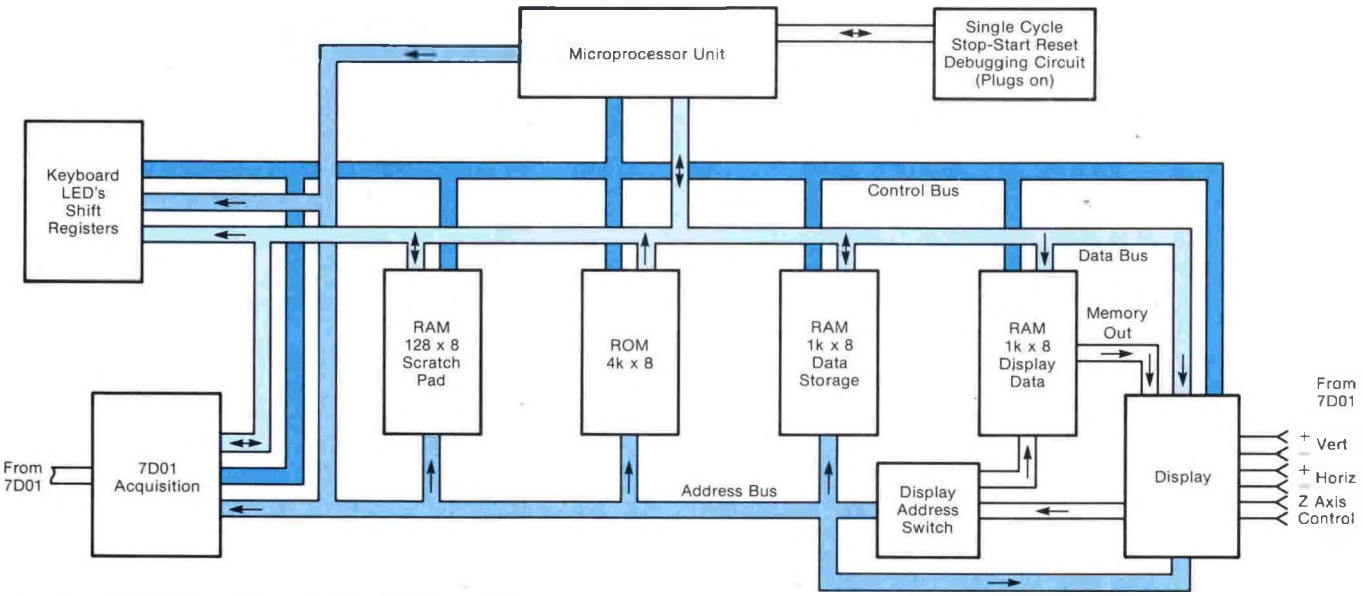


Fig. 1. Simplified block diagram of the DF1 Formatter.

memory. Crt readout in FAST, SLOW, or MANUAL tracking shows the word marked by the +, in hex, octal, or binary, as well as its location in memory relative to the trigger word.

The Timing Diagram Mode

In the TIMING DIAGRAM mode, the 7D01 provides its standard display, but now with a difference. Since the DF1 generates the crt readout, the cursor word may be read out in hex, octal, or binary. Furthermore, the 7D01/DF1 may now be operated in a 7000-Series mainframe without crt readout, which, in a dedicated logic analysis package, could amount to a substantial savings.

μP Base

The DF1's μP base gives the 7D01/DF1 combination its great versatility. Together, the μP and the 4k ROM containing its instructions constitute a small computer capable of performing a great many functions.

Data Acquired from the 7D01

Up to 16 channels of parallel data can be acquired simultaneously by the 7D01; the data must then be acquired by the DF1 to accomplish the type of display desired. Under instruction from the ROM, the μP acquires 7D01 data serially and stores it, in a known format, in the data storage RAM. At the same time, trigger position, number of channels being acquired, and bad data, are all stored in the scratch-pad RAM.

Data Formatted for Display

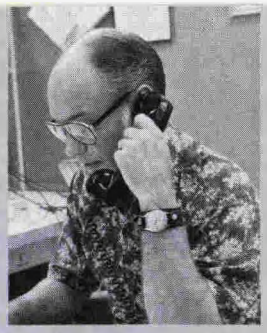
Under instruction from the ROM, the μP addresses the scratch-pad RAM for the selected display format. Data is loaded from the data storage RAM to the display data RAM, whose first 608 locations are the characters displayed. As each bit is transferred, it is coded into the appropriate ASCII character and loaded at the correct memory location. Other display data, such as whether the bit should be intensified or blinking, is also loaded. The display character generator then reads each character, decodes it, and positions it in the display.

Summary

The new DF1 Display Formatter makes it possible to obtain both logic state and logic timing displays with the same instrument. Dedicated to the 7D01 Logic Analyzer and operated in a 7000-Series mainframe, the DF1 provides mapping, at fast, slow, or manual speeds, with hex, octal, or binary readout; state tables in hex, octal, or binary, with an exclusive OR comparison mode; and the familiar 7D01 timing diagram, now with hex, octal or binary readout of the cursor-selected word. All DF1 modes are formattable.

Acknowledgements

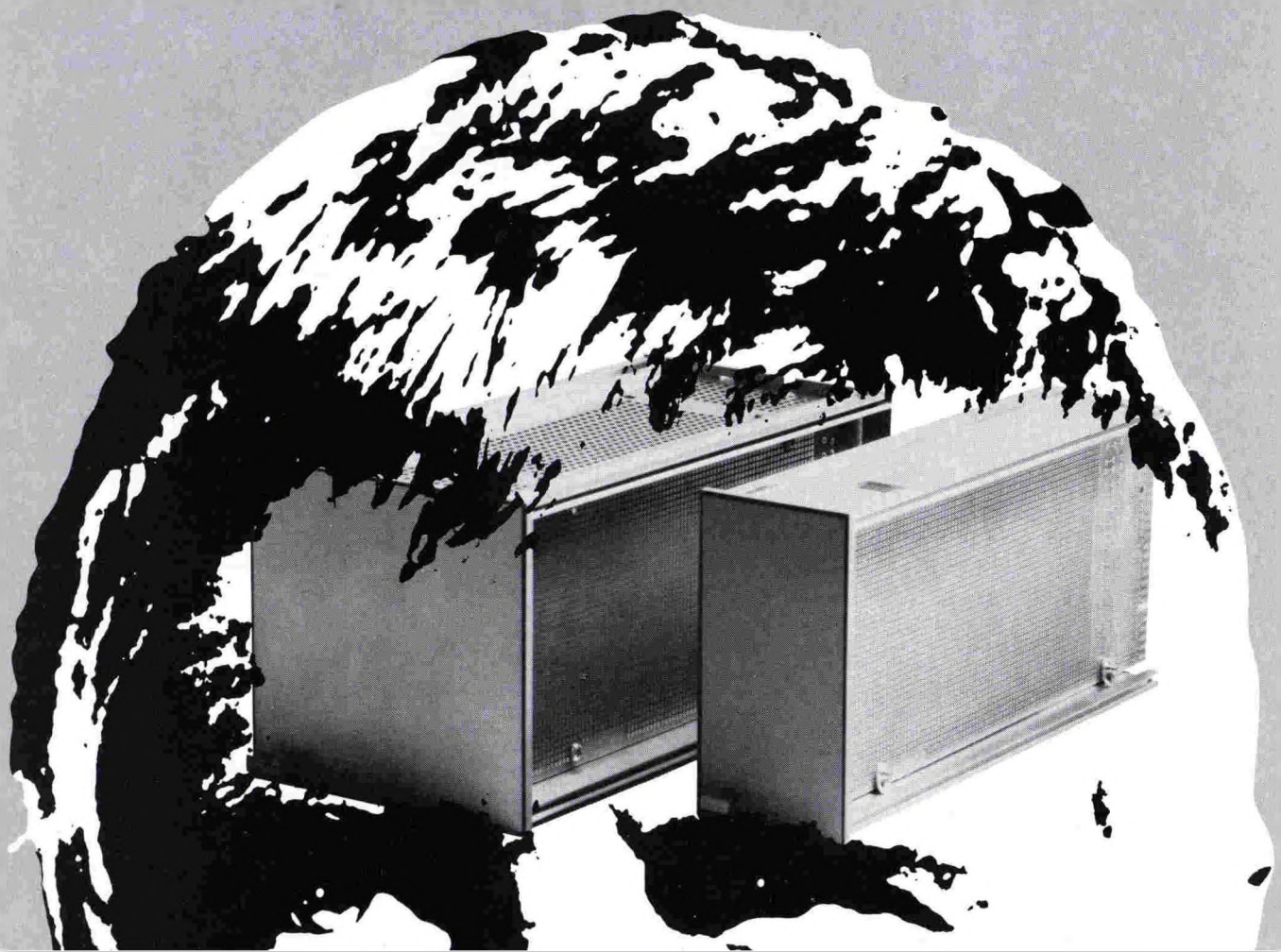
Project Manager Murlan Kaufman led the development of the DF1, with Dave Lowry and Jeff Bradford doing the electrical and software design, and Ed Wolfe doing mechanical design. Roy Kaufman and Joe Gaudio, Evaluation Engineers, and Dave McCullough, Marketing Program Manager, also made valuable contributions. Special thanks are due to Jack Lyngdal and Nick Colvin, Manufacturing; Betty Spohn, ECB; Jan Bowden, Prototypes; and to everyone else who contributed to a speedy, efficient completion of the project.



Warren Collier

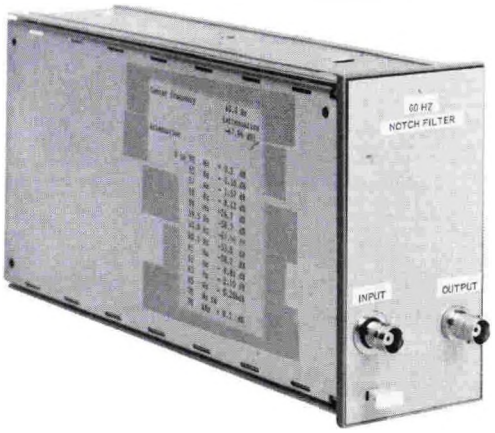
Plug-ins to reach the limits of your imagination

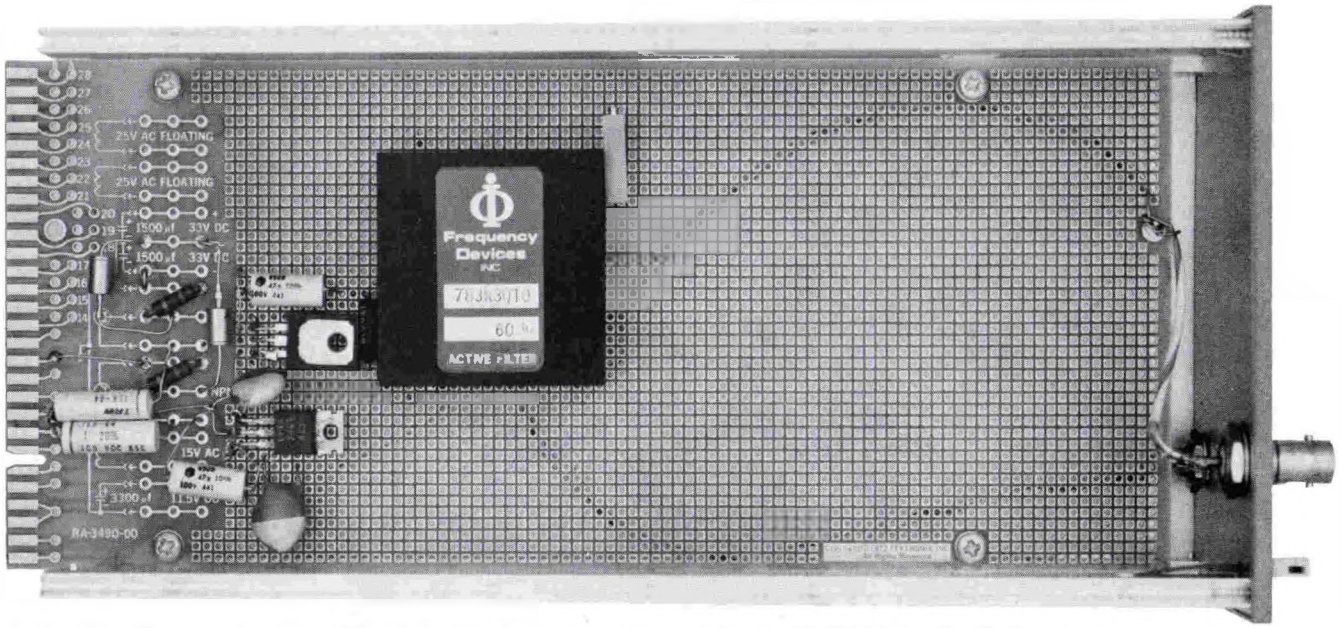
We are fortunate today in that we can turn to a catalog to find solutions to most measurement problems. Many of these problems once were unique and once required a build-it-yourself solution. But even with catalogs chock full of instruments there will be times when even the most thorough search does not turn up the precise item required. Then you are faced with the question "What do I do now?" The answer may be "Build it!"



A key concept of the TEKTRONIX TM 500 Series allows customers to select off-the-shelf modular products to fulfill the ordinary requirements of a job. But how about tailoring the series to complete a function unique to your job. How, for example, can you reduce the work in repetitive tests—or create exactly the specialized circuitry needed in a low-volume product that you are marketing, or how do you get that unique link in experimental apparatus up and running? Expectations of situations similar to those mentioned, not solvable with off-the-shelf products, led to the early development of the blank plug-in as the hardware base for another concept in the TM 500 modular approach—the custom plug-in kit that gives you the basis to do for yourself what can not be done by the instrument manufacturer.

A completed 60 Hz notch filter module





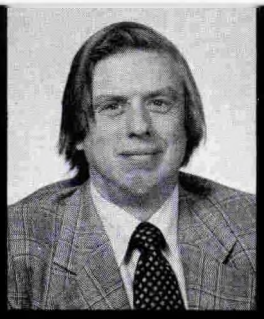
60 Hz notch filter circuitry installed on the perforated circuit board that is included in the plug-in kit.

A Custom Plug-in Kit* provides the basic mechanical parts to construct a plug-in for use in any TM 500 Series Power Module. The power module forms the exterior package (the mainframe), for a variety of instruments built in a standard plug-in format. It is helpful to consider the mainframe power supplies as a sort of "power supply kit" which can be reconfigured within the plug-in. The mainframe allows for custom interconnections between modules in the mainframe or to all TM 500 Series Option 2 Power Modules via rear-panel connectors. From the base of mainframe and kit you can build a special plug-in from your own design or from a construction note used as a guide.

The Construction Notes for the TM 500 Series suggest specific ways to build the units that you need. The Custom Plug-in Kits provide the mechanical hardware to build it on. Construction Notes do not have a rigid format. They are written to guide the customer in creating a special unit for his needs, assuming that he has reasonable resources to tackle the fabrication of what will be a unique unit. The 60-Hz Notch Filter Construction Note, AX3415, for example, does not give you a circuit layout. It does provide a circuit diagram, a suggested parts list and a list of sources of the filter module. The note also gives specifications and a performance test for the completed package. Other notes provide similar information. A very key note for most projects is "Suggested Power Supply Circuits for the TM 500 Blank Plug-in Kit AX3303."

*Both single (040-0652-01) and double (040-0754-00) compartment are available.

Two graphics technologies merged



Charles Ceranowski

The 4081 Interactive Graphics Display inaugurates a new era of sophisticated graphics terminals designed to work effectively as a terminal in a host computer environment, and with the aid of internal programming tools, makes a giant advance forward in operation as a highly flexible stand-alone graphics display.

Graphic displays in the past have used storage tube technology to offer high-resolution graphics of complex images and refresh-only tube technology to provide motion. Now, years ahead of its time, the two technologies are merged into one impressive system with the advantages of both refresh and storage in one tube. For the first time hardware and software have also merged to provide an integrated package—a powerful, interactive graphics display.

A low-cost storage terminal produces an excellent image presentation, even of complex pictures, but these images have proven to be static; using a refresh terminal for its dynamics provides excellent picture capabilities, but its extensive electronics have proven to be expensive. The 4081 gives a user the best of both—refresh and storage together, at a price much lower than a refresh-only display. The 4081 does this in four ways:

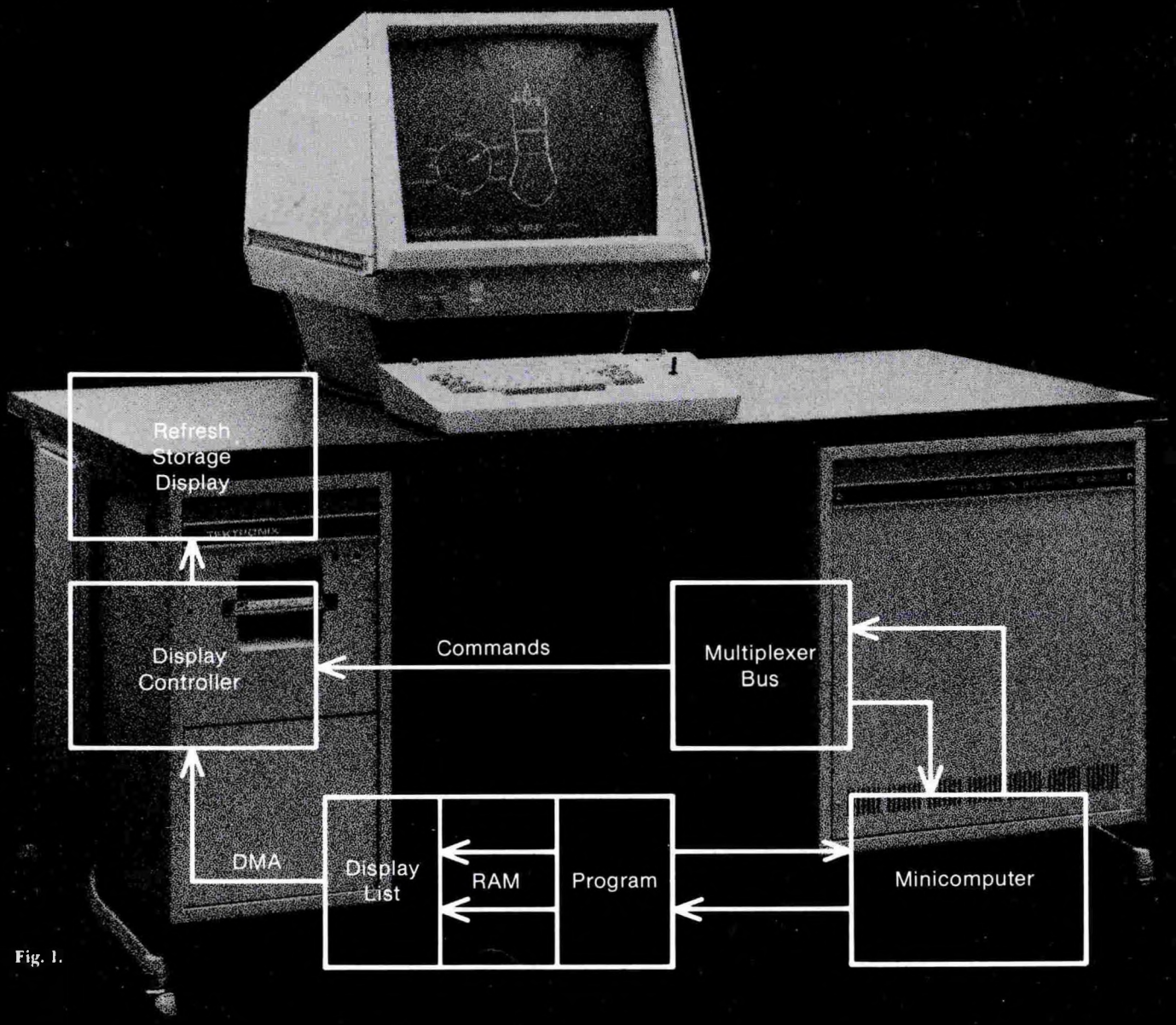


Fig. 1.

1. The standard tube technology combines storage and refresh capabilities.

2. In the 4081 this capability has been enhanced by the addition of local intelligence and a unique display controller that can *write* stored images and *maintain* refreshed images.

3. The 4081's picture processor and local storage capability also combine to lower communications overhead, timesharing costs, and host loading costs.

4. The same software that supports simultaneous refresh and storage operations also efficiently channels graphics data and commands to the proper system components.

In total, the 4081 adds up to better design capabilities and better business management.

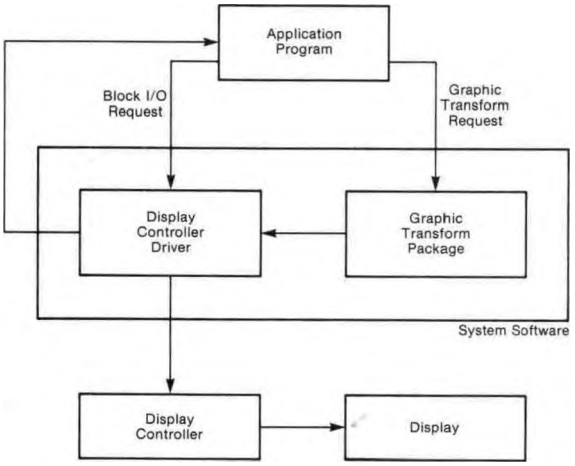


Fig. 2. Software overview. The software consists of two major areas —Application and System. The Application program makes requests to the System software for graphics output.

Hardware Operational Overview

The hardware for mixing refreshed and storage images is shown in Figure 1. It consists of a picture processor, a random access memory (RAM), a 19-inch refresh/storage display monitor, and a microcoded display controller. On command from the processor, the display controller accesses the display list in memory via the high-speed direct memory access (DMA) channel. This display list contains beam positioning and status information. The display controller directs the generation of vectors from which a picture is constructed.

The 4081 may function in three distinct modes: command, host, and program.

Command Mode: This is the mode of the 4081 when the Graphic Operating System (GOS), the interface between a program on the 4081 and the 4081 system hardware, is initially IPL'ed (loaded into memory). The 4081 is under operator control using the GOS command processor; GOS commands set various system parameters and invoke data files and programs to be executed.

Host Mode: Host mode instructs the 4081 to act like a full-ASCII alphanumeric terminal, similar to a teletype.

Program Mode: This mode is controlled by programs such as the 4014 Emulator, IGT, TECO, Assembler, and utilities. For programs that use the asynchronous communications interface, the communications parameters are usually set by the system COM command, and the communications interface must be connected to a modem or RS-232 computer communications line.

Software Functional Overview

The software can be divided into two major areas:

Application and System (Figure 2). The Application program makes requests to the Graphic Operating System software for graphic output. Before actual display,

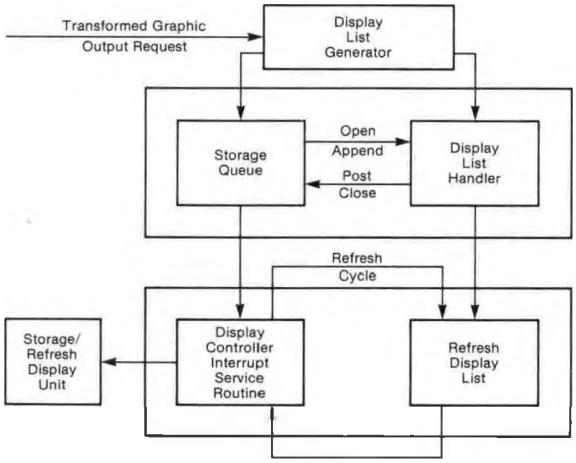


Fig. 3. Display controller driver. The display controller driver allows distinct graphic entities to be manipulated independently of one another.

the graphic output is manipulated by the Graphics Transform Package (GTP).

Graphics Transform Package. The GTP is responsible for Rotation, Scaling, Clipping, and Window/Viewport Mapping. The GTP also provides virtual graphics input and control, and support refreshed picture control. As an added feature it allows the operator to effect graphics input and output from, and to, a wide variety of graphic input devices without regard to the unique transformations required for each device. This feature is known as "device independence." Once transformed, the graphics data is passed to the Display Controller Driver (DCDVR), which builds display lists for the display controller.

Display Control Driver (DCD). The DCD (Figure 3) consists of three major modules: the Display List Generator which is responsible for taking transformed graphic output requests and generating display lists displayed as stored output or passed to the second module; the Display List Handler which manages the insertion, deletion, and modification of the refreshed

display list; and the Display Controller Interrupt Service routine which is responsible for starting up a display list and switching between storage and refresh output. Together, these modules manage the output of storage graphics while maintaining refresh display lists. The Display Controller Driver supports a transformed display file maintaining separate display code sequences for each individually identified refreshed picture. This allows distinct graphic entities or components to be manipulated independent of one another. Any graphic output request which is not identified with a refreshed object is directed between refresh cycles to the storage display.

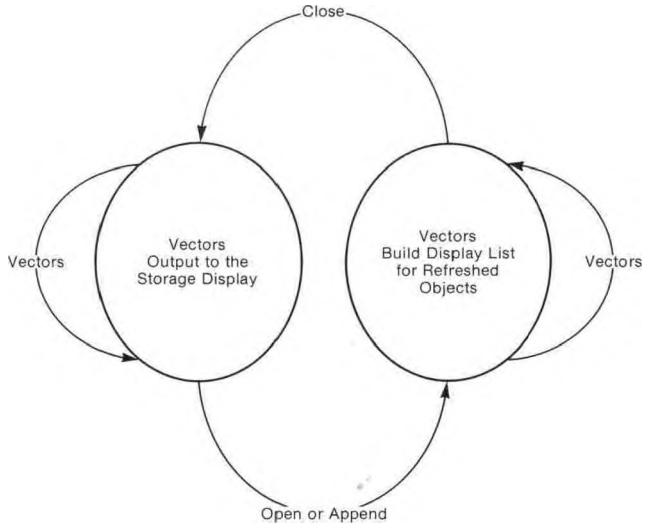


Fig. 4. State diagram depicting construction of an object.

Graphic output requests to the Graphic Operating System are made with a parameter block as outlined below:

The OP-CODE specifies the type of graphics (i.e., MOVE, DRAW, DASH, or POINT and ABSOLUTE or RELATIVE), while X and Y fields specify an X-Y coordinate pair to which the beam is to be positioned. For example, to draw a box in storage with sides of 100 units at (0,0) the following sequence of vector requests would be made:

OP-CODE	X	Y
MOVE ABSOLUTE	0	0
DRAW RELATIVE	100	0
DRAW RELATIVE	0	100
DRAW RELATIVE	−100	0
DRAW RELATIVE	0	−100

The display controller driver takes these requests and builds display code in fixed length blocks of memory. The interrupt service routine outputs the storage graphics between refresh cycles. When displayed, these blocks of memory are re-used for subsequent storage output requests.

A sequence of vector output requests, like the one given normally generates a stored image. The display code generated for the picture is traversed once and discarded. However, the user may conditionally save the display code generated by such a sequence as a refreshed object. This is done by preceding vector output requests with an OPEN command. This builds the display code generated by graphic output requests into dynamic memory areas. A CLOSE command stops the display code capturing process, and any further graphic output reverts to the storage display. The just-built 'refresh' object is not visible on the screen but is available for individual manipulation.

The process of object construction may be summarized by the state diagram in Figure 4.

An existing object may have vectors added to it by an APPEND command. A KILL command deletes the object from the system and returns the memory used to hold the display to the dynamic memory pool.

Plot 80: Graphics Operating System

The Plot 80: Graphics Operating System is the interface between a program on the 4081 and the 4081 system hardware.

If the user is a 4081 internal programmer, he may use GOS to simplify application program development. Many facilities, which must be coded by the users of other graphics systems, are provided as part of the GOS even in its very minimum configuration.

One of the more significant elements of the Graphics Operating System for use by the 4081 internal programmer is the Graphics Transform Package (GTP) that, as cited previously, does clipping, rotation, and scaling and allows the selection of window-to-viewport mapping. It also provides virtual graphics input and output and supports refreshed picture segment control. Using GTP the operator is able to perform graphics input and output operations from, and to a wide variety of graphic input/output devices without regard to the unique transformations required for each device (device independence). For example, data may be read from disc or tape; graphic input may be obtained from the joyswitch or the tablet; listings may be directed to the display, line printer, or to a disc or tape file. Device independence also allows the internal programmer to direct his effort toward his specific application, rather than being required to be cognizant of all the hardware details of a given graphics device.

Several window/viewport pairs may exist on a display and each may be referenced as separate logic units. This

capability enhances the graphic device independence of the system for a 4081 internal programmer.

GOS graphics input services are also device independent with transformations in three forms: screen coordinates, virtual coordinates relative to some window/viewport pair, and virtual coordinates relative to some input device window.

The Graphics Operating System also supports two different software character types: 1. Characters as elements of pictures. 2. Characters as elements of computer messages from, or to the human user within the monitor viewport. Character type 1 allows the continuous scaling, rotation, translation, and clipping required in a picture. Character type 2 circumvents the portions of Graphics Transform Package when displaying the character. A carriage return and line feed are automatically inserted at the right margin of the monitor viewport, so as to avoid loss of important display information.

Plot 80: Intelligent Graphics Terminal (IGT) Package. Plot 80: IGT resides in the 4081 and responds to commands from a host computer by initiating the execution of the specified capability within the 4081, such as the refreshed display of a picture. When used with a suitable host resident support package, the IGT package allows the 4081 to behave as a sophisticated "intelligent graphics terminal." Access to the IGT from the host computer is through a set of FORTRAN-callable routines which are resident in the host computer. Each routine performs a conceptually simple task, but when taken together provide the programmer with access to the full power of the 4081.

Uses of the 4081

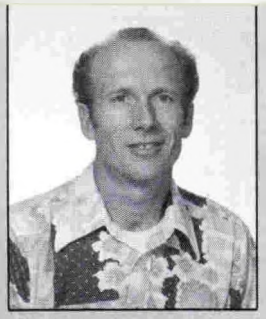
As of the date of this article the 4081 has been delivered to many sites throughout the continental United States and Europe. *Uses of the 4081 in performing interactive graphics have been varied* and include among others:

Design of automobile bodies
Electronic equipment design
Assembly plant layout
University course scheduling
Schematic drafting applications
Complex mathematical analyses
Design of oil drilling platforms
Military mapping applications
Sophisticated weapons planning
Grey scaling applications

For the majority of tasks that require interactive graphics, the 4081 has been designed to satisfy needs of the customer and to serve as a solution to his graphics applications. Future advances in the design of the 4081 will open many new thresholds for Tektronix to explore within interactive graphics. The highly effective graphics capabilities of the 4081 Interactive Graphics Display, its wealth of graphics software, its ease of programming, and its low cost all will contribute greatly to both the success of the 4081 for Tektronix as well as successes for the entire graphics industry in the United States and abroad.

Acknowledgments

Equipment of the complexity of the 4081 can only be a success with the contribution of a wide variety of personnel. Contributing to the hardware design of the 4081 were David Heinen, Roger Handy, and Donlan Jones. Software design and data were handled by Jon Meads, Gary Neher, and Ned Thanhouser. Data for inclusion in this article were mainly obtained from these individuals. In addition invaluable assistance and technical support for information included in this article was obtained from Richard Drew, Curt Coleman and Jeanne Judah in Marketing and George Rhine in Engineering.



Charles Phillips

Part I Wet-Washing

Have you ever noticed how much better your car seems to run when it has just been washed or polished? This is a psychological reaction of course, but the improved appearance does cause us to value our car more highly and take better care of it until the next rain storm messes it up again.

Servicescope

Tektronix products get dirty, too!

Not as rapidly as our car, perhaps, but with a more detrimental effect on its operation. Thorough cleaning of a dirty instrument not only improves its appearance, but improves its performance and reliability as well.

Many of you are aware that Tektronix people have, for many years, been washing instruments sent to our service centers for repair and calibration. Some customers with large numbers of instruments have installed their own wash facilities as an aid in keeping their instruments in top shape.

With the use of printed circuit boards and solid state devices in instruments comes the question, "Is it still necessary to wash instruments and, if so, what precautions do I need to observe?" While it is true that solid state instruments do not usually get dirty as quickly as their vacuum tube counterparts, they too, can benefit from a periodic cleaning. We find they are easy to wash and no particular precautions, other than those applying to vacuum-tube type instruments, need be observed.

Equipment Needed

There are several items you will need to do an effective job. They are as follows:

(a) Liquid silver cleaner used to remove tarnish from connectors.

(b) Brushes used to clean knobs and connectors.

(c) Paint brush used for dry method of cleaning, etc. Ajax cleaner, or equivalent, for wiping off front panel, etc.

(d) Sponge for applying cleaner to remove marks on aluminum.

(e) Non-sterile cotton-tip applicators used for miscellaneous cleaning chores.

(f) Piece of plastic light filter or graticule used to remove labels and adhesive after soaking them with solvent.

(g) WD-40 or furniture polish, applied sparingly to pots and switches as needed (before wash).

(h) Kimwipes, or equivalent, for wiping off front panel, etc.

(i) Spray paint used to touch up cabinets and side panels.

(j) Screwdriver for removing slotted screws.

(k) Screwdriver for removing Phillips screws.

(l) Glass and plastic cleaner.

The other items needed in the wash area are:

(a) A source of compressed air with approximately ten feet of hose.

(b) A spray gun with eight feet of hose (Devilbiss Type GDV Series 510 or equivalent).

(c) A rubber siphon hose three to four feet in length.

(d) Hot and cold water.

(e) Detergent (Kelite or equivalent, mixed approximately 1 part detergent to 20 parts water).

(f) A drying oven. There are a number of commercially available ovens suitable for this purpose. The primary considerations in selecting one are size and the capability of providing circulating air at a temperature of 125°F to 150°F.

Steps Prior to Cleaning (for wet washing only)

(1) Check for water-soluble lacquer. Some early Tektronix instruments used water soluble ink for chassis markings. The chassis have a shiny appearance as compared to those with permanent markings. If you suspect you are washing such an instrument use very little detergent and cold water.

(2) Paper covers on electrolytic capacitors should be replaced with plastic covers or sprayed with a water repellent such as WD-40.

(3) Leather handles should be sprayed with WD-40 or other type water repellent to prevent cracking.

(4) Capacitors leaking oil should be tagged for replacement.

(5) Labels and adhesive should be removed unless specified otherwise. If stubborn, soak with Flux Remover during wash.

(6) Use liquid silver cleaner (available at hardware and grocery stores) with a Q Tip or tooth brush to remove tarnish from silver anodized VHF-BNC and other connectors. After cleaning connectors be sure to protect them by washing with detergent and water or using WD-40—otherwise you will develop a small potential from the connector to ground and it will appear as grid or input leakage.

(7) Aluminum graticule covers and panels can be made to look like new by using a wet sponge and a little Ajax and rubbing the scratches or marks until clean.

(8) Knobs can be restored to like new by using a stiff bristle brush and detergent with water (from sprayer) and scrubbing them.

We no longer consider it necessary to remove the CRT, shields, vacuum tubes, etc. to do a thorough cleaning job. Experience has shown that warm water and detergent under pressure penetrates these areas adequately without completely exposing them.

The cabinet sides and bottom are removed and washed separately. They can be put back on the instrument before placing the instrument in the oven for drying, if desired. The 7000-Series plug-ins are washed with the side panels in place. This saves time and prevents a mix-up in panels.

Washing Procedure

After preparation, place the instrument in the wash booth and spray lightly with detergent and warm water. (Do not spray detergent directly on power transformers or paper items.)

Rinse thoroughly with warm water.

Remove excess water from the instrument (especially the front panel) with air.

Place the instrument (with washed plug-ins installed) in the oven and dry for at least 24 hours. (Oven makes good storage place until item is needed to be worked on. More drying time is o.k.)

The graticule and light filter are cleaned at the work bench using a glass or plastic cleaner.

After Washing and Drying

It is well to take a few minutes to apply lubricant to the switches, motors, etc., particularly on the older instruments. A lubrication kit designed specifically for this purpose is available under Tektronix Part No. 003-0342-01.

Switches—Lube detents with a light grease and contacts with No-noise.

Motors—Apply 1-2 drops of thin oil. (WD-40 is suitable).

Potentiometers—Apply 1-2 drops of No-noise or WD-40 to the shaft, contacts and open spots around the cover. Use a hypo and needle, or spray can with nozzle. Cover removal is neither necessary nor desirable. Rotate rapidly if necessary to eliminate noise.

Painting* Panels and Related Items

(a) Be sure panels are clean and dry.

(b) Use proper color paint. Available locally or from Tektronix.

(c) Use long sweeping strokes when spraying (short strokes will cause blotches) and stay several inches away from item to be sprayed.

*Local paint shops also do this type work for a moderate fee.

Waxing and Polishing

The appearance of the instrument can be enhanced by applying WD-40 or furniture polish.

Front panels—spray WD-40 on an absorbent towel, not directly on the panel, and wipe. Also use a soft 1" paint brush sprayed with WD-40 and get in around and on the knobs and switches.

Side panels and handles—treat the same as front panel, knobs and switches—combination of towel and brush.

Summary

You will find that the time spent in properly cleaning an instrument will result in fewer calibration problems, a longer period between calibrations and greater operator satisfaction with both the instrument and the service center.

Customer training classes

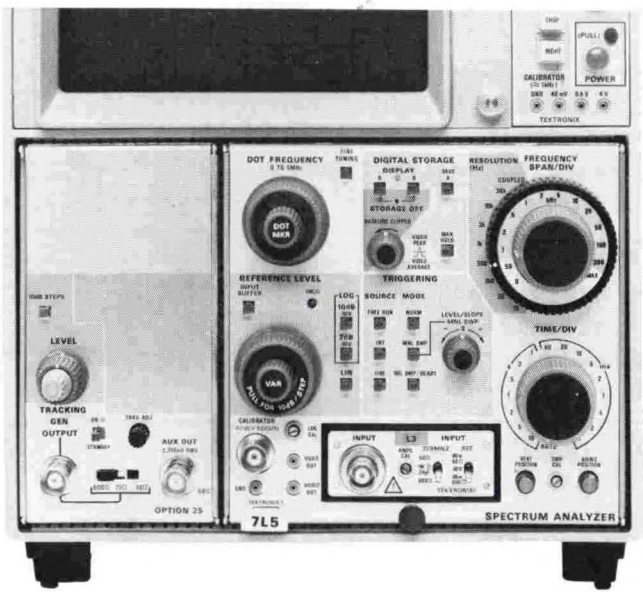
The following maintenance classes will be conducted at Tektronix, Inc. Beaverton, Oregon. There is no fee for these classes except as noted.

7704A/7A26/7B70/7B1	Feb. 7-11, 1977 April 18-22, 1977
7633/7A18/7B53A	Feb. 14-18, 1977
7904/7A19/7B92	Feb. 21-25, 1977
465/475	Jan. 31-Feb. 4, 1977
TM503/DC503/DM501 FG501/PG501/TG501	Jan. 17-21, 1977
SAMPLING 7S11/7T11	Mar. 7-11, 1977
IDG-4010/4012/4014 4610/4631/4623	Dec. 13-17, 1976 Apr. 4-8, 1977
WDI R7912/1350*	April 11-15, 1977
DPO P7001/CP1151*	Mar. 21-25, 1977

*Fee charged for this class

Contact your local Tektronix Field Office for registration information.

New Products



7L5 Options Expand Versatility

Two new options expand the versatility of the 7L5 Spectrum Analyzer. The new L3 plug-in module features a high impedance probe–compatible input (1 MΩ/28pF) with input termination selections of 50Ω and 600Ω. It is one of a series of modules used with the 7L5 to provide it with various front-end capabilities. The Option 25 Tracking Generator provides the 7L5 with selectable 50Ω, 75Ω, and 600Ω impedance source with calibrated frequency output for swept frequency tests from 10 Hz to 5 MHz.

The output of the Option 25 Tracking Generator can be adjusted so it tracks within 10 Hz of the spectrum analyzer frequency. The frequency span and rates are controlled with the spectrum analyzer. The output level is controlled from the tracking generator. Output level is calibrated and controlled in 10 dB and 1 dB steps over a 63 dB range. An Aux Output may be used to drive a frequency counter. The 7L5 with Option 25 is a three-wide unit for the 7000-Series Mainframe.

P6302 Current Probe and AM 503 Current Probe Amplifier

The P6302/AM 503 is particularly useful for evaluating currents from dc to 50 MHz and up to 20A, allowing the user to evaluate fast transients, low-frequency response and dc level. Especially useful where loading is critical, such as high impedance points, or in current dependent devices, the P6302 probe jaw slides open to be clipped around a conductor—no need to break the circuit under test. The current range of the P6302/AM 503 is from 1 mA/div to 5A/div. (Extended from 20 mA to 5,000 A/div (50,000 A peak) with the addition of the CT5 current probe). The AM 503 is a plug-in that operates in any TM 500 mainframe. It provides a convenient means of viewing current waveforms on most oscilloscopes.

1975-1976 Tekscope Index

*Domestic only

**International only

A-3452

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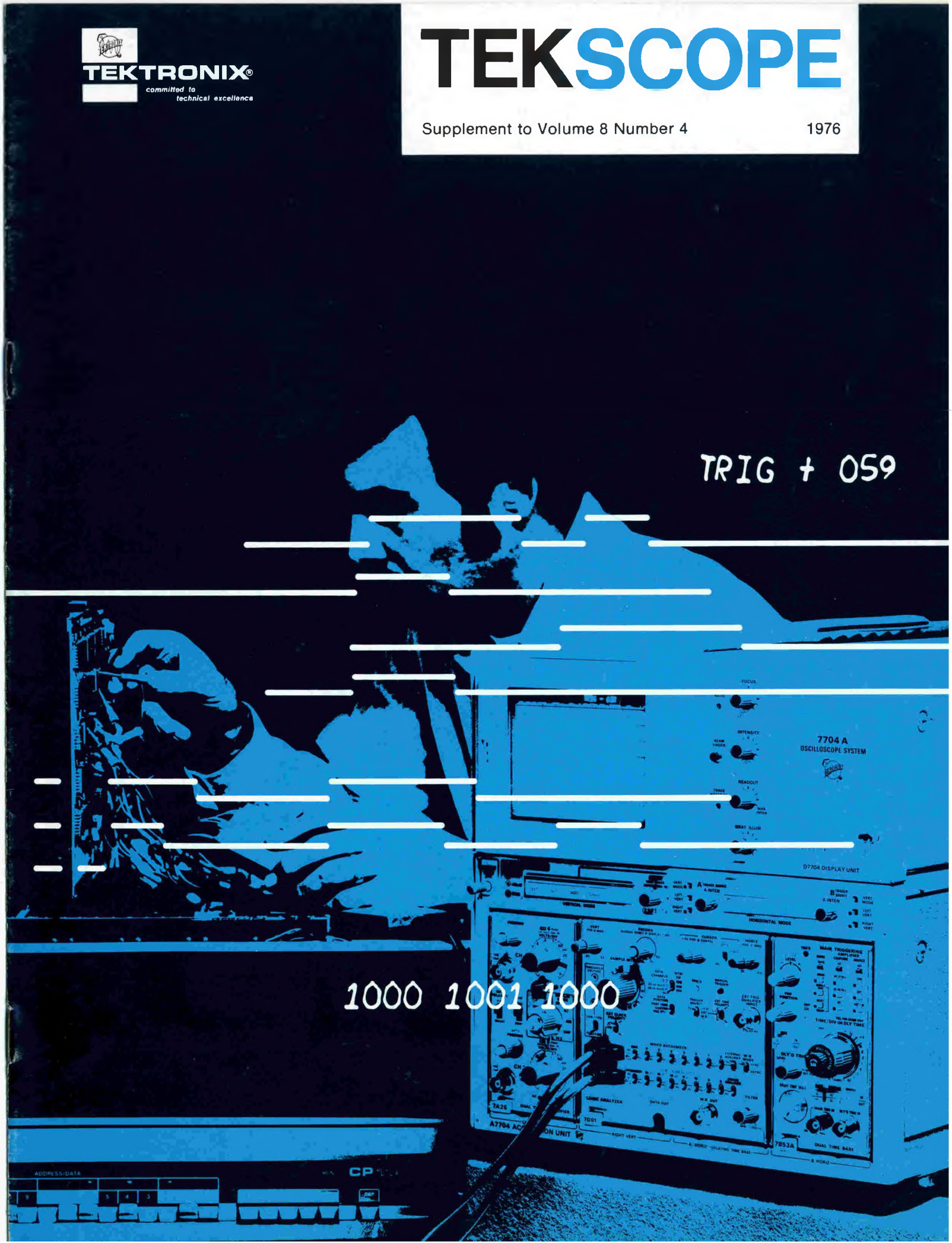
TEKSCOPE

Supplement to Volume 8 Number 4 1976



TEKSCOPE

TEKTRONIX
committed to technical excellence

Customer Information from Tektronix, Inc.,
Beaverton, Oregon 97077

Editor: Gordon Allison

Contents

Cover: Some of the unique features of the 7D01/7000 Series logic analyzer system are presented in this artistic treatment. The digital readout above the traces shows the number of clock pulses occurring between the trigger and cursor positions. The readout below the traces is the binary word present at the cursor position. (The trigger and cursor position are not shown in this display.)

Keith Taylor

A 16-channel logic analyzer for the 7000 Series

More than just an oscilloscope. This is the phrase often used to describe the 7000 Series. And for good reason. Plug-in versatility transforms 7000 Series Oscilloscopes into counters, digital multimeters, spectrum analyzers, time-domain reflectometers, curve tracers, rapid-scan spectrometers, etc. Now, with the introduction of the 7D01 plug-in, 7000 Series Oscilloscopes become state-of-the-art logic analyzers.

The 7D01 is a 16-channel, logic timing analyzer that presents data in the familiar oscilloscope-type, time-related diagram pictured in figure 1. But, as you can see, there's much more that meets the eye in figure 1 than just the usual multi-trace, logic timing diagram. Several features have been added to aid you in analyzing the displayed data.

Note the two vertical rows of bright dots. The row at the left indicates the triggering point. In this instance, we have selected the post-trigger position, which means that 90% of the data displayed occurs after the trigger. Pre-trigger and center-trigger positions are available at the flip of a switch, to give you a wide range of data to view.

The second row of bright dots in the display provides a reference point for making time comparisons between displayed channels. This row of dots can be positioned anywhere on the horizontal axis by means of the cursor

controls. The fine control moves the dots one bit at a time, and the coarse control in 16-bit increments. The readout at the top of the screen shows the number of bits occurring between the trigger and the cursor. In the asynchronous mode, this number multiplied by the sample interval equals the time difference between the trigger and the cursor position. When using an external clock, the readout shows the number of clock pulses occurring between these two points. The cursor is especially convenient for locating a particular bit or point in time relative to the trigger.

There has been much discussion as to whether the logic state or the logic timing display is the most useful in performing logic analysis. Each has advantages for specific applications. The 7D01 resolves this issue for many applications by providing both types of display.

You will note that the readout at the bottom of the screen in figure 1 is in the format usually displayed by logic state analyzers. The binary word displayed corresponds to the logic word present at the cursor position. This unique feature makes the 7D01 useful for many software and firmware applications. It is often a convenience also in hardware applications.

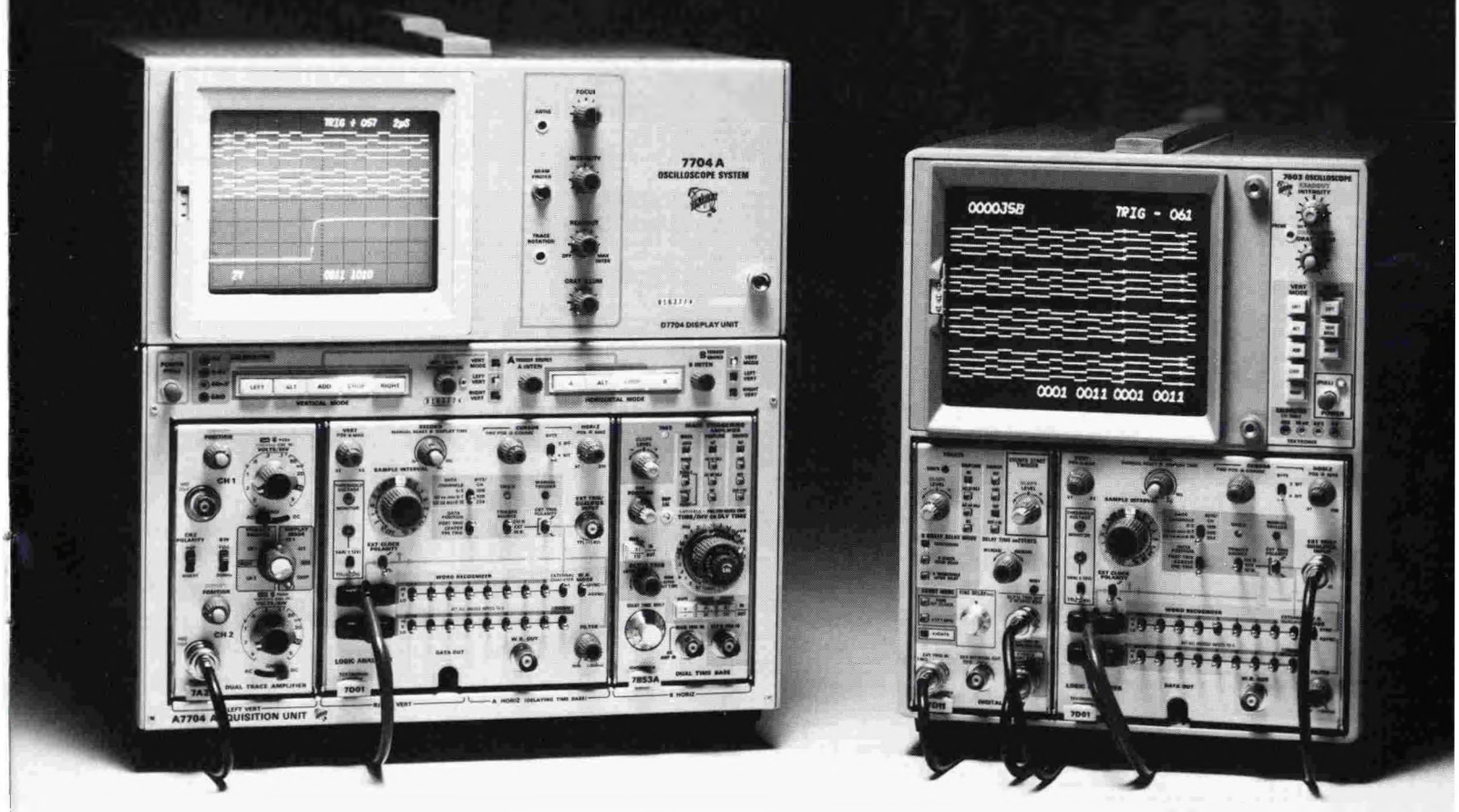
A versatile trigger

Trigger versatility is one of the most important characteristics of a logic analyzer. We have already discussed the ability to view data preceding the trigger, following the trigger, or both preceding and following the trigger. Now, let's consider the sources of trigger.

A choice of three sources is provided by a front-panel switch: channel 0 of the probe input, external via BNC input, or from the built-in, 16-bit Word Recognizer. A fourth choice is manual triggering by front-panel pushbutton.

The 16 data-input channels also serve as inputs for the Word Recognizer. Front-panel switches allow you to select any pattern of up to 16 parallel bits as the trigger word.

Two additional inputs, the Probe Qualifier and the External Qualifier, provide still further selection of the triggering point, giving us, in essence, an 18-bit Word Recognizer. The External Qualifier may be the output from another Word Recognizer, a time delay or digital delay generator, or another signal from the system under test. The signal should be TTL level and have a minimum duration of 15 ns.



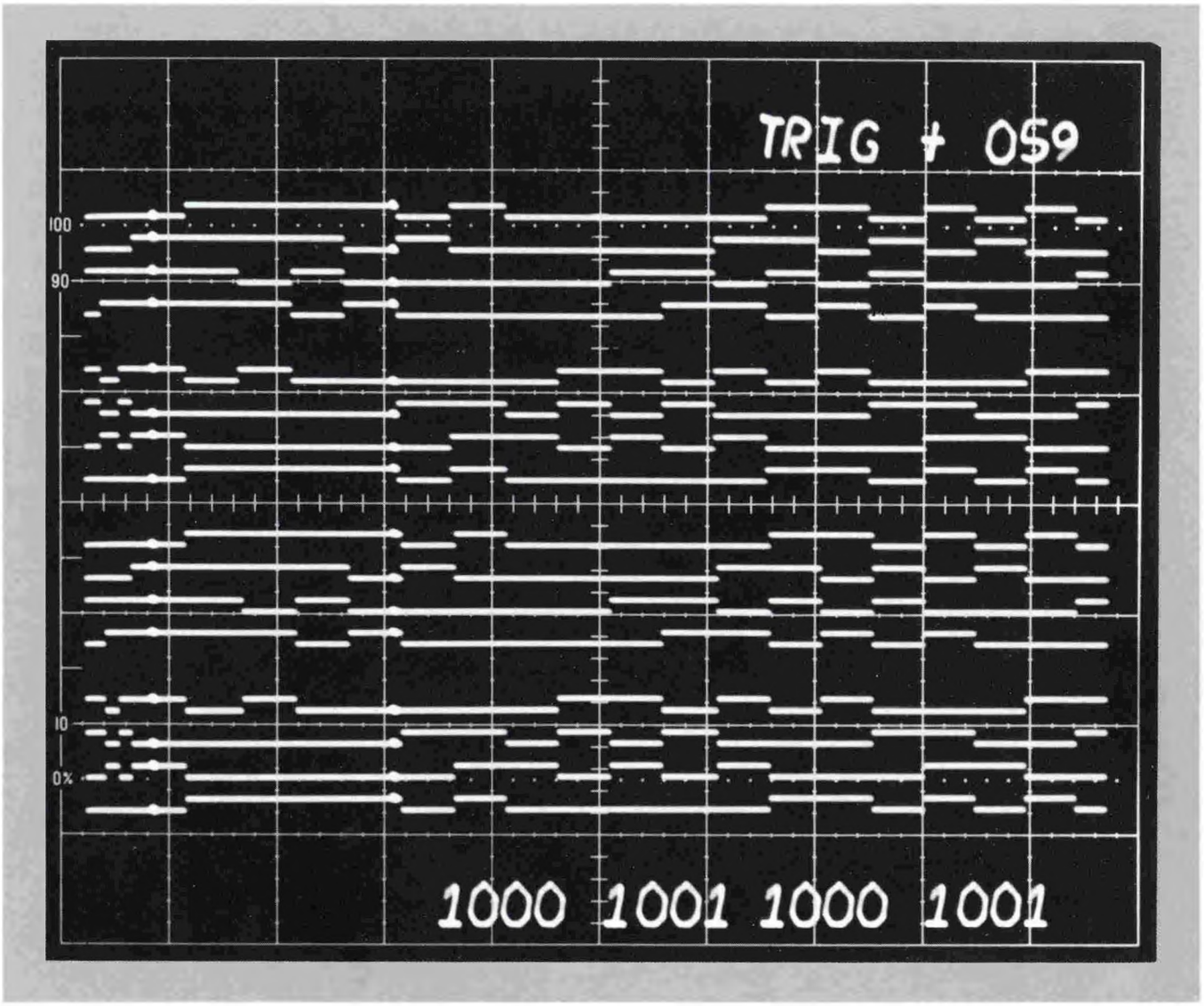


Fig. 1. A wealth of information is available from the display generated by the 7D01. The intensified dots at left show the trigger point. The dots about two divisions to the right are a movable cursor. The number of clock pulses occurring between the two bright dots is displayed at the top of the screen. The 16-bit binary word at the cursor position is displayed at the bottom of the screen. Right to left corresponds with top to bottom.

There are two paths through the Word Recognizer, synchronous and asynchronous, selectable by a front-panel switch. In the asynchronous mode, a variable filter is inserted in the trigger path that prevents glitches and other anomalies from causing false triggering. Word recognition of bit combinations of shorter duration than the filter setting is inhibited. Maximum filter width is at least 300 ns.

The trigger point indicated on the display is most accurate when operating the Word Recognizer in the asynchronous mode with the filter set at minimum, or when using an external sampling interval. The trigger position indication is less accurate when triggering from channel 0, or when the asynchronous filter is advanced clockwise.

The built-in Word Recognizer operates independent of the rest of the logic analyzer. When all of the conditions required for word recognition are met, the data acquisition circuits are enabled and a HI signal is supplied to a front-panel connector, for triggering an oscilloscope or other associated equipment. A Word Recognizer output occurs each time the conditions are met, whether the logic analyzer is operating in the store or display mode.

For applications where it is desirable to page through a long sequence of events, a companion plug-in, the 7D10, provides digital delay by up to 10^7 events. The delayed trigger output of the 7D10 serves as an external qualifier or trigger for the 7D01. The 7D10 counts events at rates up to 50 MHz.

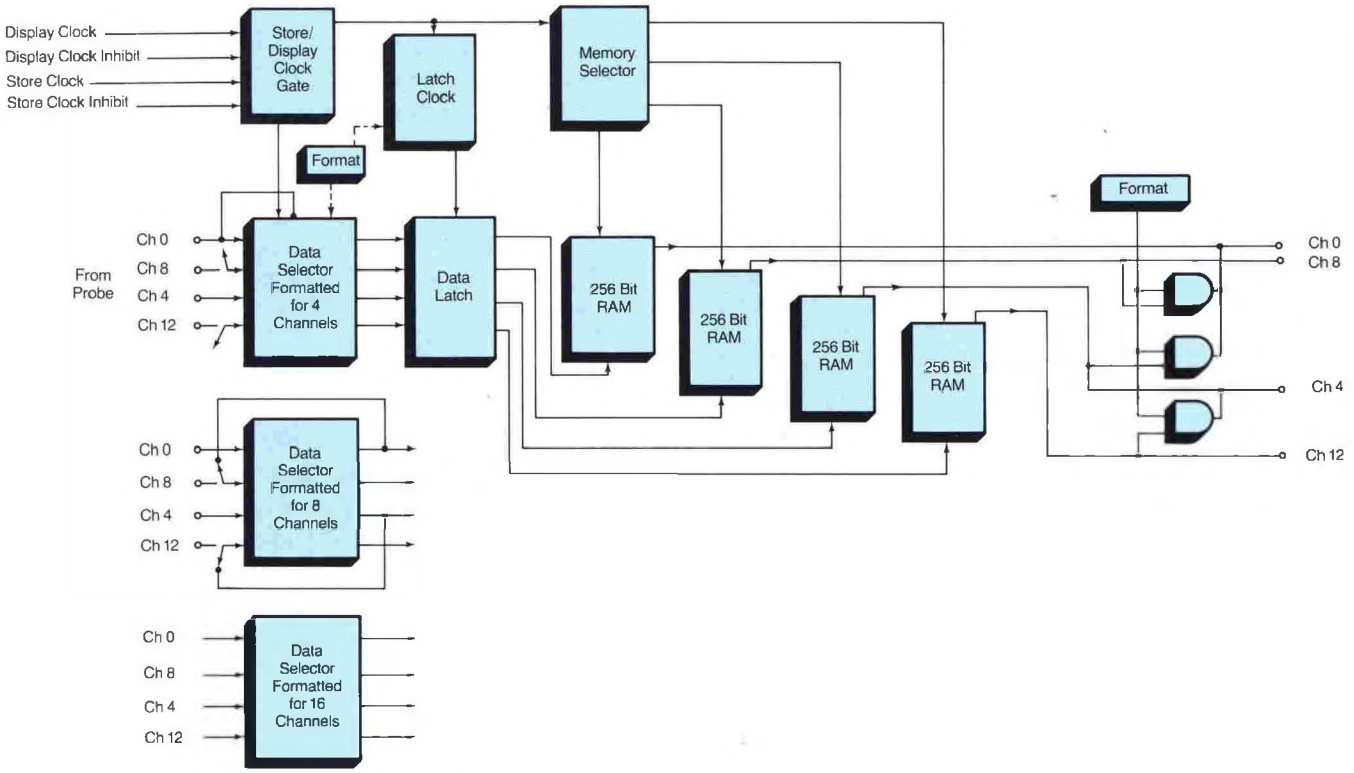


Fig. 2. The 4-k memory in the 7D01 is formattable. One of four 4 x 256-bit sections is shown. It can store 1024 bits from one channel, 512 from two, or 256 from four channels. In 4-channel operation the Data Selector functions as a 4-bit shift register, in 8- and 16-channel operation as 4-bit latches.

Data inputs

Up to 16 channels of parallel data can be acquired simultaneously by the 7D01. Minimum loading (1 MΩ, 5 pF) on the circuit under test is achieved by two active probes with multiple inputs. Probe qualifier and external clock inputs are also provided for in the active probes.

You have a choice of threshold levels for the probe inputs — a preset +1.4 volts for TTL applications, or selection over a range of ± 12 volts by a front-panel variable control.

Data can be clocked into the 7D01 in either a synchronous or asynchronous mode. In asynchronous, the clock may be either internal or external at rates up to 100 MHz depending upon the number of channels in use. To match the resolution of the measurement to your specific application, sample intervals derived from the internal clock may be selected over the range of 5 ms to 10 ns, in a 1-2-5 sequence.

A formattable memory

One of the most useful features of the 7D01 is the formattable memory. Consisting of sixteen 256-bit random access memories (RAMs), the memory can be formatted by a front-panel switch to store four channels with 1024 data bits per channel, eight channels with 512 bits per channel, or sixteen channels with 256 bits per channel.

Let's take a look at how this is accomplished (see figure 2). The 16 data inputs are arranged in groups of four, each group coupled to a corresponding 4 x 256-Bit RAM. In the 4-channel mode of operation, the Data Selector functions as a 4-bit shift register, acquiring four bits of data input from channel 0. The Data Latch transfers the data from the outputs of the Data Selector to the inputs of the four, 256-Bit RAMs. Through a three-gate arrangement controlled by the DATA CHANNELS switch, the outputs of the RAMs can be added to give us a single 1024-bit memory, two 512-bit memories, or four 256-bit memories. The function of the Data Selector is also controlled by the DATA CHANNELS switch to pass four bits of data from one channel, two bits from each of two channels, or one bit from each of four channels, to the Data Latch.

Data acquisition and display

Figure 4 is a simplified block diagram of the 7D01. Let's refer to it and go through a cycle of acquiring and displaying data. A good point to start is when reset occurs.

When display time ends, a reset signal is generated by the reset circuitry. This resets the trigger flip-flop, trigger and address counters, and the store/display flip-flop, switching the memory from the display mode to the store mode. Data, which is clocked into the Data Latch at the high-frequency clock rate, is transferred to the

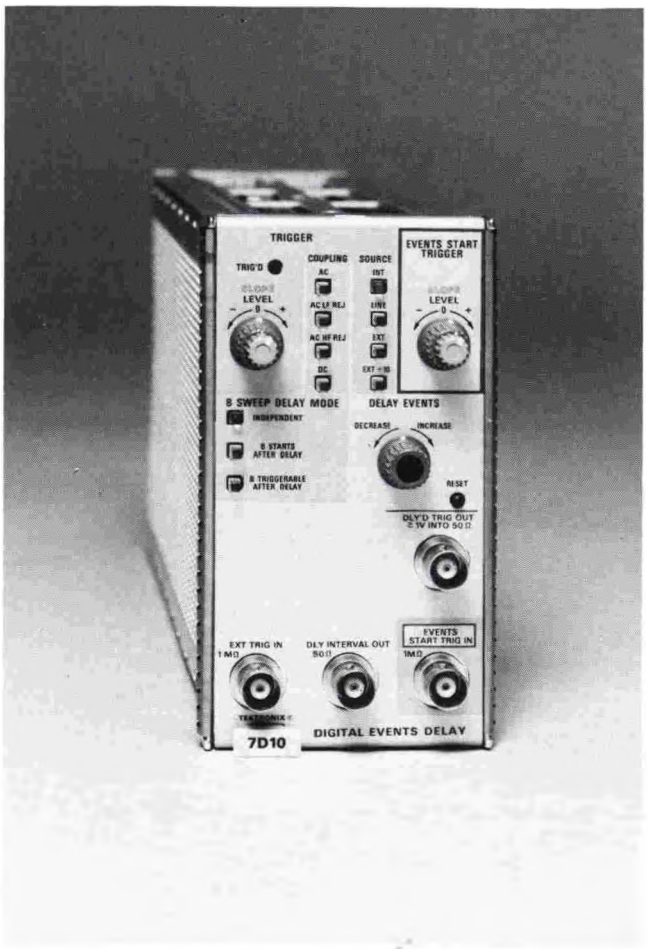


Fig. 3. The 7D10 Digital Delay plug-in is an ideal companion for the 7D01. It will count up to 10^7 arbitrary trigger events, periodic or aperiodic, and deliver an output after the preselected count has been reached.

memory at the memory low-frequency clock rate, starting with the end of reset. The high-frequency clock rate is determined by the SAMPLE INTERVAL switch setting, and is divided by 1, 2, or 4 times to establish the low-frequency clock. Data is clocked into the memory until a trigger occurs, and for a period following the trigger as determined by the DATA POSITION switch setting. For example, in the CENTER position, half of the memory fills after the trigger occurs.

The input steering and latch circuitry determines how data will be input to the memory. In the 4-channel mode, the data from channel 0 is clocked serially into one 4 x 256 section of the memory, as previously discussed. The data from channels 1, 2, and 3 are clocked into their respective memories simultaneously, in a similar manner.

Occurrence of the trigger, switches the trigger flip-flop, gating on the trigger low-frequency clock. The low-frequency clock is the store clock (high-frequency clock) divided by 1, 2, or 4 times, depending upon the setting of the DATA CHANNELS switch. A separate 1-, 2-, or 4-times divider is used for the trigger low-frequency clock because of phasing considerations related to the memory low-frequency clock.

The trigger counter counts 16, 128, or 240 counts (depending upon trigger position selected) and then generates the first flag. During this flag, the memory clock is summed with a gate derived from the trigger clock, to generate a gate that switches the Store/Display Flip-Flop to the display mode. Transition from store to display is thus made in phase with the memory low-frequency clock.

The display clock, which runs at 2 μs, now becomes the high-frequency clock. It, in turn, is divided by 1, 2, or 4 to become the memory and trigger low-frequency clocks. During display time, the outputs of the sixteen, 256-Bit RAMs are displayed in serial fashion, as determined by the Output Steering and Multiplexer circuitry.

In the display mode, the trigger counter counts through 256 counts of the display clock (equivalent to one display line) and generates a second flag. This flag resets the sweep, blanks the crt, and selects the next channel to be displayed. This flag also goes to a divide-by-16 counter that sets a flag when sixteen channels have been displayed. When the display time ends, a reset pulse is generated and the store/display cycle starts again.

To further enhance the flexibility of the 7D01, a choice of two display modes — Full Display or First Trigger — can be selected by positioning an internal jumper. In the Full Display mode, the trigger to the Trigger Flip-Flop is inhibited until the Address Counter has completely cycled. This assures that the memory is filled with valid data.

In the First-Trigger mode, it is conceivable that a trigger may occur before the memory is completely filled. If this occurs, the display is blanked during the time that invalid data would be presented.

Data outputs

Data from the memory is available in both parallel and serial format from an internal 25-pin connector. Also available are the display/store, flag, frame, trigger intensify, and master reset outputs.

Two inputs are made via the connector: record enable and external display clock input. An external display clock is required if the data are to be output to computer for further analysis.

Summary

The 7D01 is designed to offer high-performance, 16-channel logic analysis to 7000 Series users. Used with conventional oscilloscope plug-ins in a four-hole mainframe, you can have both an oscilloscope and a logic analyzer in a single package. The formattable memory offers unparalleled flexibility, and the high-speed data

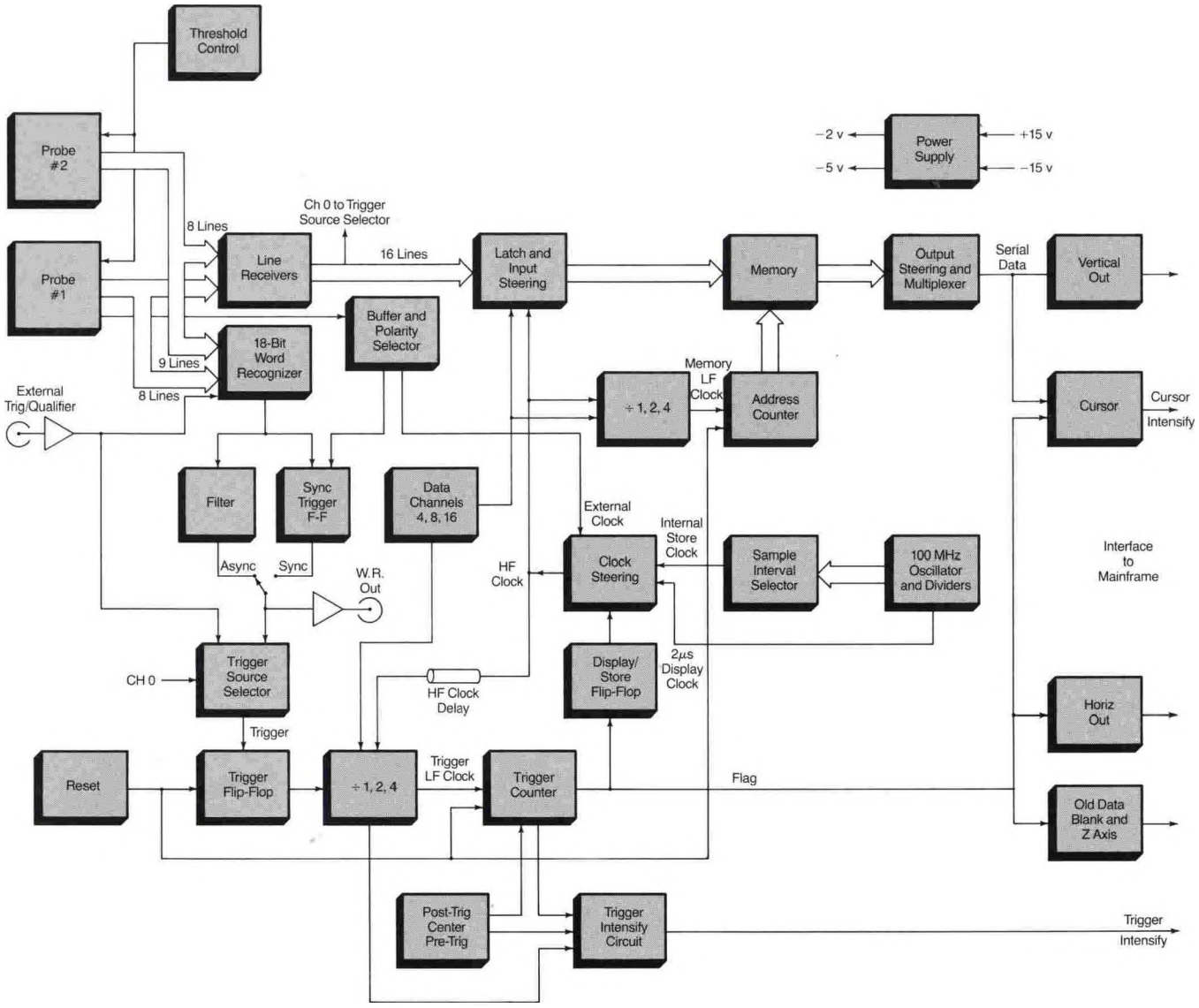
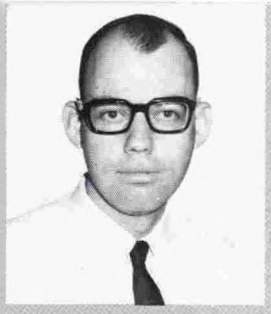


Fig. 4. Simplified block diagram of the 7D01.

acquisition and minimum loading afforded by active probes makes the 7D01 ideal for working with higher speed logic families.

Acknowledgments

Murlan Kaufman as Project Manager provided overall direction for the 7D01. Project Leader was Keith Taylor, with Morris Green and Jeff Bradford doing electrical design, and Ed Wolf mechanical design. Dick Anderson, Group Technician, provided valuable assistance, as did Beverley Kateley and Dona Fricker on prototype assembly and circuit board details. Roy Kaufman, Evaluation Engineer, and Dave McCullough, Marketing Program Supervisor, also made valuable contributions. Our thanks to Wendell Damm for his work on the active probe, and to the many others who contributed to the completion of the project.



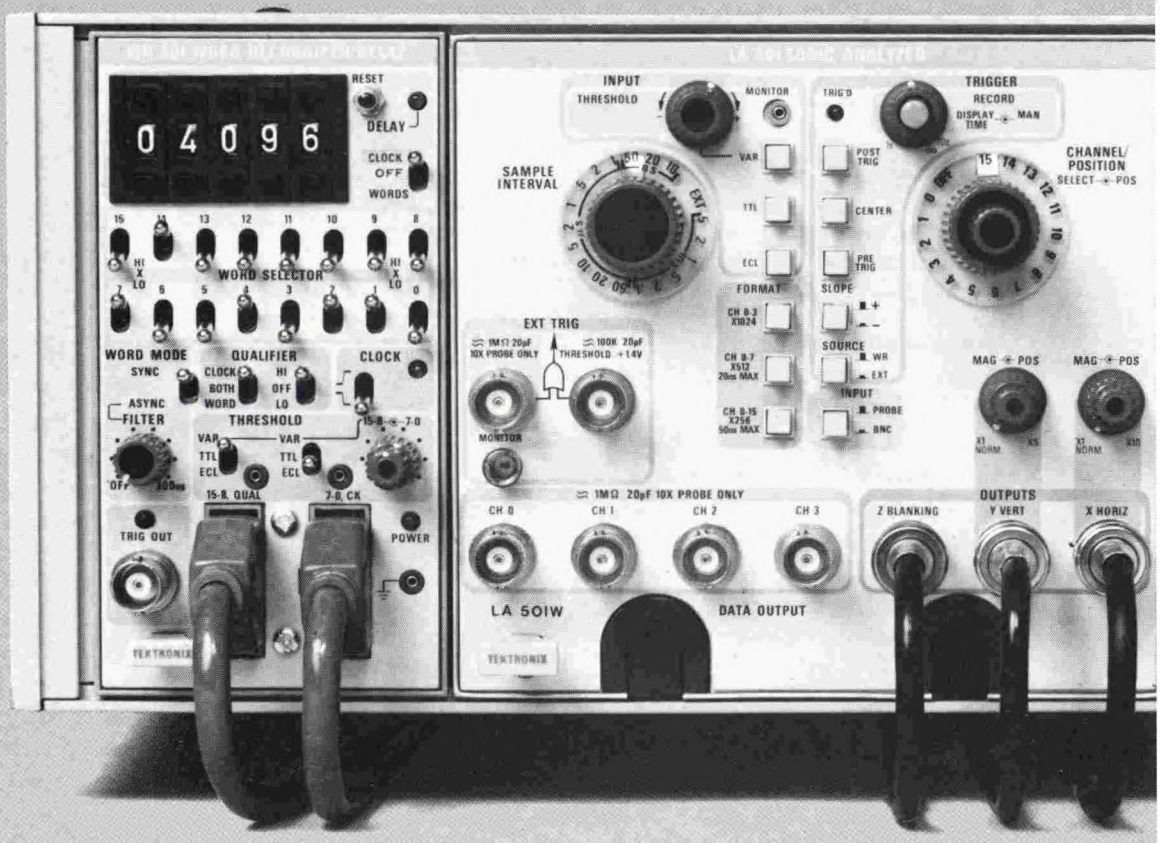
Pete Janowitz

A plug-in word recognizer with digital delay

For sports fans, instant replay quickly became one of the most appreciated improvements in televised sports programming. Engineers have long had the ability to view critical "happenings" in their electronic circuitry, with the aid of oscilloscopes.

Now, with the introduction of logic analyzers, an engineer has not only acquired instant-replay capabilities, he can instantly replay and view sixteen channels simultaneously. It's a companion tool, the word recognizer, that enables him to recapture the action at any point he chooses.

Sometimes the word recognizer is an integral part of the logic analyzer. In other instances, it's a separate entity – like the new TEKTRONIX WR 501 Word Recognizer. Designed primarily to work with the LA 501 Logic Analyzer, it occupies a single plug-in compartment in a TM 500 mainframe. When ordered with the LA 501, the package is called the LA 501W and includes all of the interfacing hardware needed to couple the WR 501 and LA 501 mechanically and electrically.



The WR 501 can also function as a stand-alone word recognizer/digital delay unit for those needing to expand the triggering capabilities of their logic analyzer, oscilloscope or other equipment. For example, WR 501s can be cascaded to obtain greater word width, dual word recognition/delay, or delay "nesting" (delay within a delay).

Using the new P6451 high-impedance (1 MΩ, 5 pF) active probes, the WR 501 can acquire up to sixteen channels of data, plus an external clock and qualifier signal. Maximum flexibility is afforded by using two probes, each with nine inputs. Separate threshold controls for each probe facilitate working with systems using mixed logic families, with preset threshold voltages for TTL and ECL signals selectable by front-panel switches. Variable controls provide a choice of threshold voltage over a range of ± 10 volts.

The Qualifier input can be used to expand the word recognizer to 17 bits, gate the external clock, or do both. In the LA 501W, the external clock can be gated by the Qualifier input, allowing you to selectively clock data into the memory.

Synchronous or asynchronous operation

In some applications it is advantageous for word recognition to be synchronous with the system clock. For others, it is desirable to generate a trigger whenever the word pattern occurs. With the WR 501, the choice is yours at the flip of a switch.

In the synchronous mode, the external clock signal acquired by the probe clocks the Sync Flip-Flop to generate a word recognizer output in step with the system clock.

In the asynchronous mode, a word recognizer output is generated whenever the selected word pattern occurs. A selectable-pulse-width filter with a range of 5 to 300 ns is automatically activated, to reduce the possibility of false triggering due to glitches or data skew.

A built-in digital delay

Another useful feature incorporated in the WR 501 is digital delay. You have a choice of delaying by up to 99,999 clock pulses or words at clock rates up to 50 MHz. Delay by words generates a trigger at the *n*th occurrence of the word so we can see what happens at the end of a program loop, for example. The count is set by convenient push-button thumbwheel switches.

The delay count is started by an output from the word recognizer when word recognition occurs. For those applications where you want to use the delay without the recognizer, you can start the count by using a single bit from one of the data inputs. Just set the appropriate WORD SELECTOR switch. A front-panel push-button lets you reset the delay counter manually at any point in time. Reset is automatic when the selected delay is reached.

The trigger output pulse generated by word recognition, or word recognition plus selected delay, is brought out to a front-panel BNC connector, and also routed to the LA 501 via an internal multi-pin connector. The output pulse is TTL compatible, with duration a function of the operating mode and signal inputs.

Interfacing to the LA 501

Special provisions are made to interface the WR 501 and LA 501 without the need for external connections. The sixteen data inputs, external clock, and word recognizer output are coupled internally through a short cable assembly, to the 25-pin probe-input connector in the LA 501, in place of the P6450 passive probe. The sixteen data inputs to the WR 501 are always present at the interface connector, irrespective of front-panel control settings. This arrangement of the WR 501, interface, and LA 501 make up the LA 501W.

The threshold controls on the WR 501 now control the probe inputs, with the threshold control on the LA 501 affecting only the front-panel external trigger and the BNC probe inputs. Attenuator probes can still be used with the BNC inputs for channels 0 through 3 on the LA 501 by setting the INPUT to BNC. Data channels 4 through 15 will be supplied from the WR 501 inputs. This gives you three individual threshold controls and the ability to view inputs separated some distance. The attenuator probes can handle signals up to ± 500 volts to accommodate many real time situations.

If you have a need for 16-bit word recognition while viewing more than four other data channels, you can remove the interface cable and use the WR 501 as a stand-alone word recognizer. The optional P6450 passive probe can then be used with the LA 501 for data acquisition. The output signal from the WR 501 is coupled externally to the LA 501 external trigger input in this instance.

Technical details

The WR 501 performs two major functions — word recognition and digital delay. The simplified block diagrams in figures 1 and 2 will be useful in understanding how each function is performed, and how they relate.

The sixteen data channels acquired by the WR 501 probes pass through a differential FET pair, with one output going to the word recognizer, and the other output through delay lines to the interface connector. The delay lines provide zero hold time for the LA 501 data inputs.

The Qualifier can gate either the word recognizer or external clock, or both, or can be turned off when not needed. The delay line in the word recognizer signal path provides zero hold time for synchronous operation.

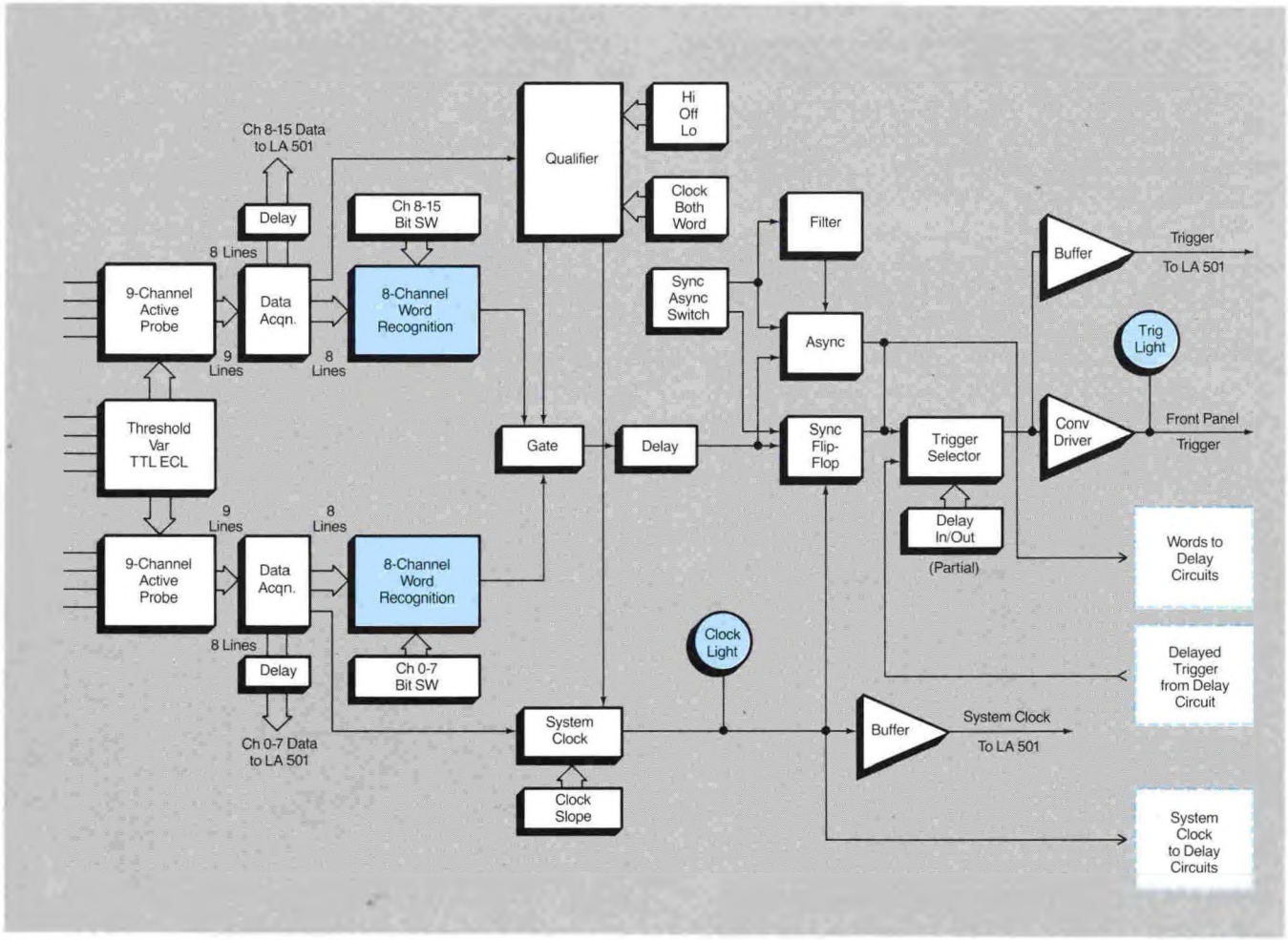


Fig. 1. Simplified block diagram of the word recognizer portion of the WR 501. Signals from the sixteen data input channels can be coupled directly to the LA 501W independent of word recognizer operation.

The 5 to 300 ns filter is activated whenever asynchronous triggering is selected, and can be set to assure valid word recognition.

Output trigger selection is controlled by the front-panel switch labelled CLOCK-OFF-WORDS, which corresponds to the Delay In/Out blocks in the diagrams. In the delay OFF position, the word recognizer output goes directly to the output buffer and output converter driver. The converter transforms the output signal from ECL to TTL level.

In the delay IN position, which corresponds to either delay by word or delay by clock, the delay circuitry is inserted in the trigger output path and no trigger output signal is generated until after the selected delay has been accomplished.

Moving along to the delay circuitry block diagram shown in figure 2, we see that the Delay By Selector routes either the system clock or the output from the word recognizer to the counter circuitry. The word recognizer output also goes to the start circuitry to initiate counting.

Five decade counters are used. The least-significant-bit (LSB) counter is ECL, with the remaining counters TTL. Counter operation is essentially straight-forward, using a 9's complement scheme. The Hold block is a latch that holds the 9999 Detector output level until the LSB counter reaches the nine count, while allowing the TTL counters to be reset.

When the selected count is reached, the Delay Output Flip-Flop is switched, generating a delayed trigger signal. The delayed trigger is routed to the Trigger Selector for availability as the output trigger signal.

Summary

The TM 500 Series family is designed to allow you to configure your measurement package to fit your measurement needs. The high-performance LA 501 has been meeting many of your logic analyzer needs. Now, the WR 501 with its high-impedance probes, 17-bit word recognition, and digital delay expands your logic analysis capabilities to include even the more sophisticated measurements. And you are not limited to the en-

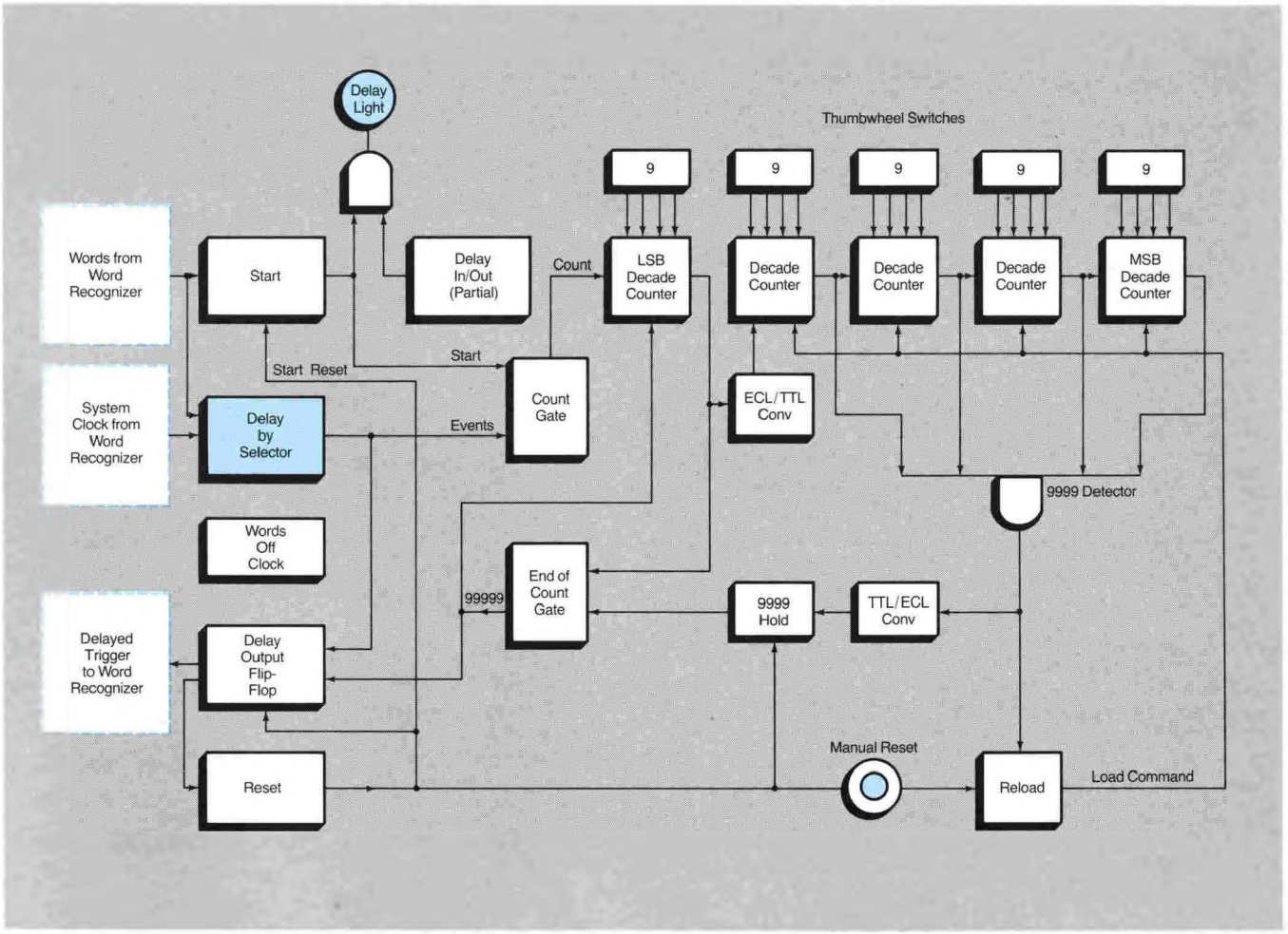


Fig. 2. Simplified block diagram of the digital delay portion of the WR 501. Delay is enabled by the word recognizer output. Manual reset provides for resetting the counter whenever the full count has not been reached.

gineering and production environment. The LA 501W, WR 501, and the SC 502 packed into a TM 515 mainframe give you a complete logic analysis system in a suitcase. They will help you solve those tough logic problems, wherever you encounter them.

Acknowledgments

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