FAST, REAL-TIME, DFT INSTRUMENT BASED ON VMEbus

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ABSTRACT

An emerging class of VMEbus-based test and measurement instruments is benchmarked by a recently introduced digital spectrum analyzer. The instrument performs real-time spectrum analysis in the dc-to-10 MHz range at 5,000 spectrums per second. Its architecture is based on the VMEbus[1], and is partly adapted for high-speed pipeline processing. The keyboard and color graphic displays suit basic spectrum analysis, as well as advanced analysis of amplitude vs. both frequency and time. The instrument provides a DSP programming environment when an RS232 terminal is attached. With addition of an RF spectrum analyzer, down converter and software, real time analysis is extended to 21 GHz and beyond. Post-processable spectral output suits the instrument for use in a larger signal analysis or test system. This digital spectrum analyzer, which has 17 boards on the bus, is representative of an emerging class of filled-enclosure instruments.

INTRODUCTION

VMEbus and VXIbus are architectures for down sizing test instrumentation. The idea is that functional modules or instruments-on-a-board can be grouped compactly in a single enclosure, and can communicate at high speed. However, these architectures also allow an up sizing of the power of single instruments by virtue of the same compactness and speed. Such instruments can have performance capability and user interfaces that are unprecedented.

Some functional modules and their interconnections are tailored to the special requirements of the instrument and its application. The rest are designed in accordance with the standard to gain its advantages. Peripherals and power supplies are added, and the enclosure adapted to meet instrument standards.

The 3052 Digital Spectrum Analyzer is a representative filled-enclosure instrument. It is a DFT filter bank analyzer that generates up to 5,000 spectrums per second, covering frequency spans to 10 MHz with 800 frequency points. It has applications in RF communications, signal analysis, radar signal processing and telephony.

INSTRUMENT CONCEPT

The 3052 is an outgrowth of research done by Tektronix Laboratories, and development by the DSP Unit of the Systems Group. New algorithms based on the DFT showed promise for a digital spectrum analyzer of unprecedented speed, frequency resolution, dynamic range and amplitude accuracy, and were studied. The performances of the more promising of these algorithms were simulated on a large computer. One was found that met the performance requirements, and yet required a practical, though challenging number of computations. The computations are implemented in a DSP architecture that makes efficient use of multipliers and adders, some custom designed DSP chips, and high-density boards. Speed is accomplished through parallel, synchronous, pipeline processing at a 25.6 MHz rate.

The result is that the 3052 performs at the rate of 3 G operations per second to output 5,000 spectrums per second (one every 200 μs). These spectrums cover frequency spans as wide as 10 MHz, with each one consisting of 800 complex frequency sample points. The output is suitable for post processing.

The VMEbus was selected as the basis for board development, because it could be adapted to support pipeline processing at the required speed, and to have sufficient board real estate to support the required number of DSP components in a volume that makes sense for a test and measurement instrument. The fact that VMEbus is standard has the great advantage that enclosures and memory, display processing, and remote control boards are available from various manufacturers. They improve their products from year to year, and VME-based instrument performance can be upgraded as new boards become available. Some manufacturers design to specification; and this was done particularly for the enclosure used for the Instrument Unit[2].

That the 3052 is virtually a filled VME enclosure came as the result of a simple design choice; however, it has proven to be key, and the 3052 now can serve as a benchmark for what can be accomplished in a test and measurement instrument based on the VMEbus.

ARCHITECTURE

The three main parts of the 3052 Digital Spectrum Analyzer are the instrument unit, keyboard and color display monitor (see Figure 1). The central part is the Instrument Unit, and it is a VMEbus enclosure. The enclosure is extended to accommodate modules that condition and digitize analog signals, and to accommodate disk drives and a power supply, as well as the main DSP modules. The bus is partly adapted for high speed, multi-board pipeline processing. The remainder is standard VMEbus (see Figure 2).

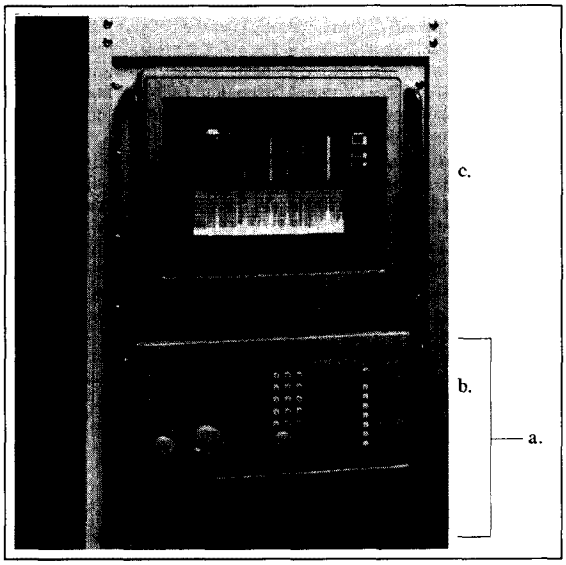

Figure 1. 3052 Digital Spectrum Analyzer: a. Instrument Unit, b. Keyboard, and c. Monitor.

[1]IEEE P1014/D1.2, IEC 821 BUS
[2]Manufactured by Electronic Solutions

CH2568-4/89/0000-0049 $1.00@ 1989 IEEE

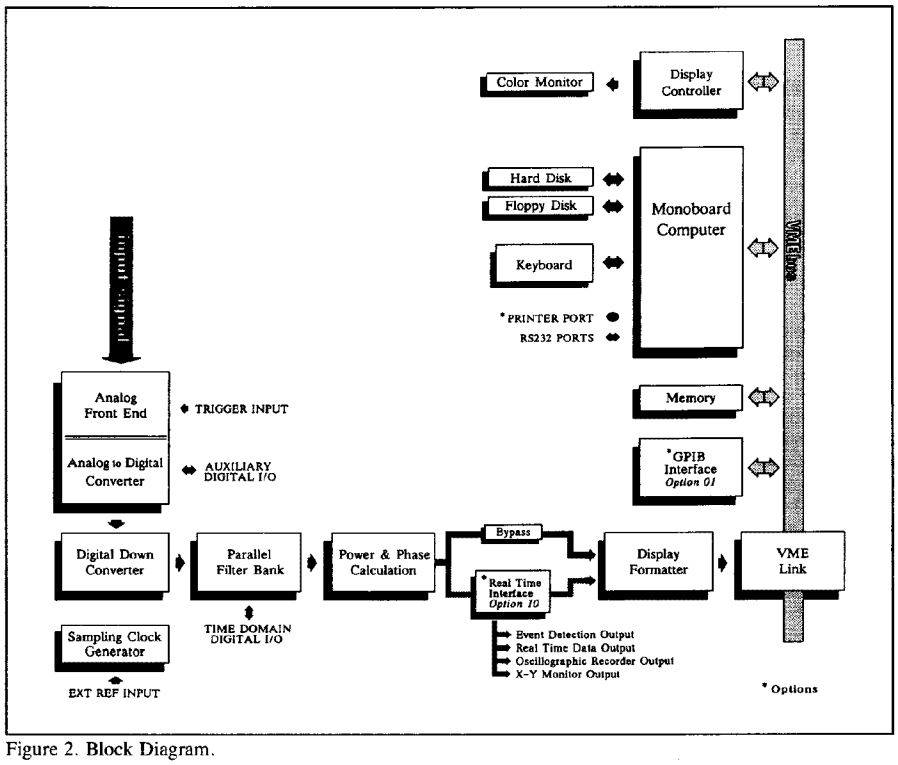

Figure 2. Block Diagram.

The adapted part of the bus is for pipeline processing. It accepts input signal from the Analog-to-Digital Converter and pipelines it synchronously through a series of DSP boards. In this pipe, time-domain data transformed to the frequency domain in a continuous stream: continuous in the sense that data rates are maintained above the Nyquist values in relation to the channel bandwidths in each part of the pipe. The VME Link board is at the end of the pipe. As its name implies, it links the pipeline to the standard VMEbus. Spectral data output from this link is loaded into an SRAM board where it is held for display processing, or for transfer to more permanent storage.

The bus has backplane connectors P1 and P2. Slots 1 through 6 are standard VME. P1 and P2b connections are standard throughout. P2a and P2c connections in Slots 20 through 7 are made to pipeline data from one board to the next (the pipeline proceeds in the direction of descending slot numbers). In each slot, the P2c row accepts input from the preceding board, and the P2a row sends output to the next board. Figure 3 illustrates how this scheme typically is carried through a DSP board.

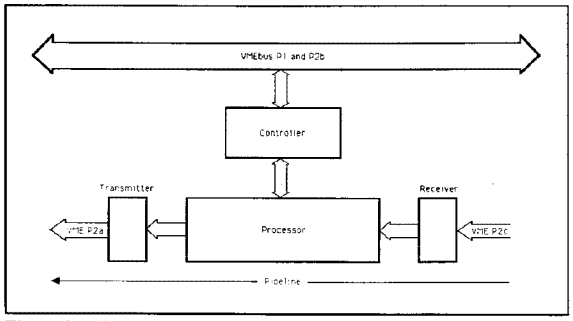

Figure 3. DSP board connection to VMEbus, showing pipeline.

The slots are connectors in the bus enclosure as diagrammed in Figure 4.

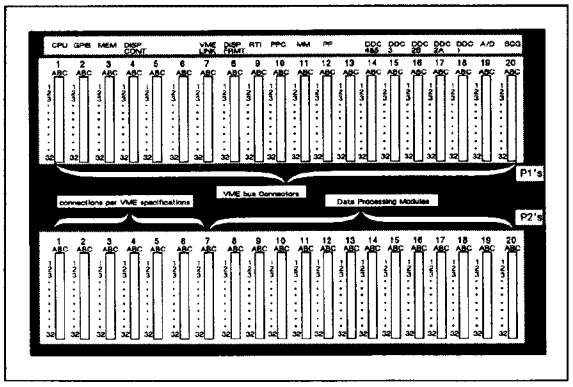

Figure 4. Backplane Slots (Viewed from rear of Instrument Unit)

Complex data words are carried through the pipeline in real and imaginary word pairs, each with 16-bit precision. By time multiplexing the real and imaginary data at every stage, the pipeline is made to process both components independently: real on, say, even clock cycles; and imaginary, on odd cycles.

Most of the modules shown in the block diagram, Figure 2, are VME boards, and therefore are represented in Figure 4. Table 1. relates the information in these two figures.

Table 1: 3052 Digital Spectrum Analyzer Modules and Backplane Slots.

Block Diagram (Figure 2)	Backplane Slots (Figure 4)	
	Slot Number	Slot Designation
Analog Front End	None	None
Analog to Digital Converter	19	A/D
Digital Down Converter	18, 17, 16, 15, 14	DDC 1, 2A, 2B, 3, 4&5
Parallel Filter Bank	12, 11	PF, MM
Power & Phase Calculation	10	PPC
*Real Time Interface/Bypass	9	RTI
Display Formatter	8	DISP FRMT
VME Link	7	VME LINK
Memory	3	MEM
*GPIB Interface	2	GPIB
Monoboard Microcomputer	1	CPU
Hard Disk	None	None
Floppy Disk	None	None
Keyboard	None	None
Display Controller	4	DISP CONT
Color Display Monitor	None	None
Sampling Clock Generator	20	SCG
(Not shown)	5, 6, 13	(Empty Slots)

*Optional boards

The Sampling Clock Generator module, which is phase locked to an oven controlled crystal oscillator, provides a 25.6 MHz clock that is carried through the pipe. However, in a scheme to reduce the effects of skew between clock and data, the clock is sent upstream through the pipe. First, it is sent on a parallel bus line directly to the end of the pipe, to the VME Link board. There it is buffered and injected into the pipe to travel back through all of the DSP boards. It is buffered after every point where it is used.

The Analog to Digital Converter samples the input signal at this same clock rate of 25.6 MHz, and digitizes it with 10-bit precision.

The pipeline DSP boards can be seen when the back panel of the Instrument Unit is removed, as is shown in Figure 5. It can be seen also that connections are made at the front edges of some of these boards in addition to those on the back plane. For this reason, the boards were not given metal front panels; and instead, there is a single panel that covers all of the DSP boards. The panel seen on the left-hand side of the unit contains I/O connectors from modules in the standard slots, 1 through 5.

The DSP boards are double height and double length (320 mm), as is seen in Figure 6. (The boards in the standard slots, 1 through 5 and single length [160 mm].) In the absence of a front panel on the DSP boards, ejectors were designed that are attached directly to the board.

The components on the board are a mixture of conventional dual in-line packages and surface mounted technology (SMT). SMT is used to get the high-density placement needed to achieve instrument performance, and to maintain functional modularity; that term meaning, major functions are confined to single DSP boards or groups of adjacent boards. In addition, some low-profile SMT components are mounted on the back sides of boards. The thermal design consequences of component numbers and placement density are discussed below.

There are variations, but typically the DSP boards have 8 layers: six signal layers, 1 ground layer and a 5V layer.

A set of five boards provides for selection of frequency span and center frequency tuning. The tuning range is over the entire dc-to-10 MHz frequency range of the instrument. This set of boards is the Digital Down Converter (DDC). It is a five-stage down converter, as is shown in Figure 7. Each stage is used or bypassed to provide 13 span selections from 1 kHz to 10 MHz in a 1, 2, 5, 10 sequence. Each stage has a digital local oscillator, quadrature mixer and low pass FIR filter. These filters provide antialiasing. The time-domain data output from the DDC is resampled at a rate that is appropriate to the frequency span selected.

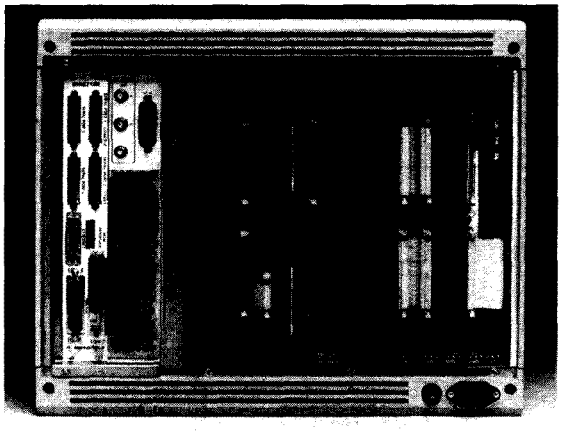

Figure 5. Pipelined DSP boards (Seen from Rear of Instrument Unit with Panel Removed).

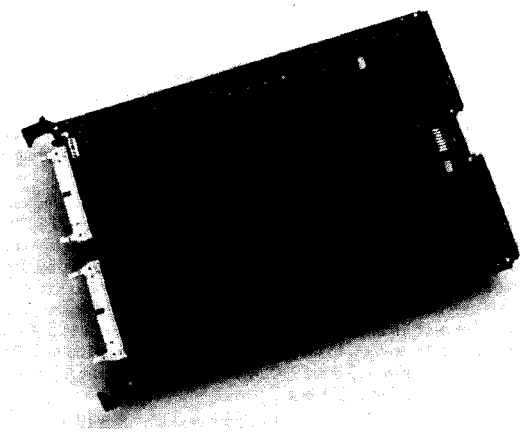

Figure 6. DSP Board (DDC 2A).

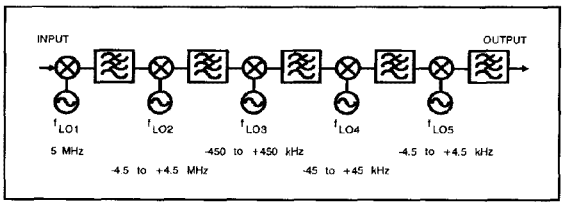

Figure 7. The Digital Down Converter stages used for span and center frequency selection.

The output of the DDC is applied to a two board set called the Parallel Filter Bank. It does the conversion from time to frequency domain, and does it at rates to 5,000 spectrums per second: a near hundred-fold speed up over conventional FFT analyzers. The first board of this set is the Periodic Filter, PF. This FIR filter provides the final filtering of time-domain data to set the frequency resolution, flatness, dynamic range and antialiasing of the frequency converted signal. The integrity of the spectral data is largely determined at this stage.

The second of the two boards in the Parallel Filter Bank is the Matrix Multiplier, MM. It replicates the Periodic Filter at 1024 different frequencies across the span. The replication is done with such speed in relation to the data rate that effectively a bank of 1024 parallel filters is created by the two boards operating together. Figure 8 illustrates what is meant by a parallel bank of filters. (The output of the central 800 of these filters is displayed across any span. The 112 outer filters on each side are unused; because the outermost frequencies coming through the DDC are rolled off and aliased.)

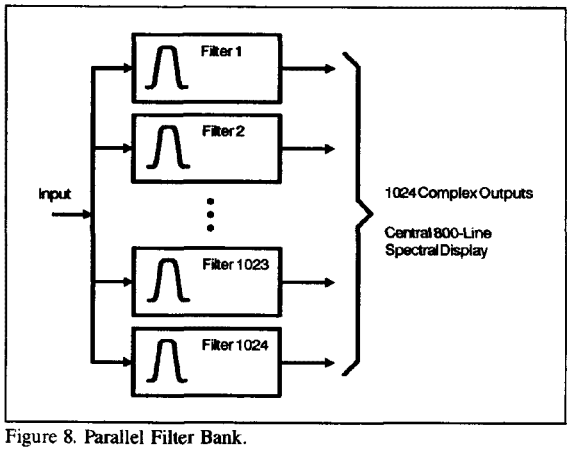

Figure 8. Parallel Filter Bank.

The coefficients of the Periodic Filter are soft; that is, they are values held in data registers on the PF board. A standard set of coefficients is down loaded from a disk file during instrument power up.

When loaded with this set of coefficients, the PF has an impulse response that is 6K time points in length (the maximum length for the PF). This standard filter, i.e., the PF loaded with the standard set of coefficients, has a flat passband (within 0.05 dB), which permits the accurate measurement of absolute power at each frequency. Furthermore, it has low spectral leakage (80 dB at an offset of two frequency points); and good antialiasing performance (80 dB at data rates that meet or exceed the Nyquist criterion, as they do for span settings of 2 MHz and below). The filter has an ultimate rejection (80 dB) that enables the instrument to operate with high dynamic range.

Since the coefficients of the Periodic Filter are soft, other filter shapes, stored on the disk, can be down loaded. For example, a 1K filter with a rectangular impulse response works better for short transient signals. The rectangular and a number of other 1K filter shapes are available on the disk. In fact, when the PF has a simple impulse response 1K long, the filter bank operates as a conventional FFT. The rectangular impulse response is equivalent to a rectangular window in FFT parlance. Hamming, Blackman and other conventional FFT windows are also stored on disk.

The output of the Parallel Filter Bank is 16-bit, real and imaginary (r, i) data pairs. Power, dB and linear (watts), voltage magnitude and phase are determined from these (r, i) pairs by calculation and look up from ROM tables. These operations are done on the Power & Phase Calculation board. After going through a bypass jumper, that is put in Slot 9 in the absence of the optional Real Time Interface (discussed below), the data is applied to the Display Formatter board.

This formatter board performs time-domain signal processing on sequential spectral data. The output data from each frequency point is a time-domain sequence. The board can calculate block averages, or sift out peak values or max/min values. The number of spectral frames over which these results are obtained may be set by the user to yield particular results; or by the monoboard microcomputer which will seek a system value that allows the greatest amount of data to be displayed on the monitor. A default mode of this board simply passes the last of the number of spectrums, and discards the others.

Testability is built into the pipeline by additional paths for data to enter and exit each module. A digital pattern generator, that is on the Sampling Clock Generator module, can put test patterns onto the parallel part of the bus or into the pipeline. These patterns can be routed through one or a series of DSP boards to test module interfaces and processors. The responses to these patterns are read and checked by the microcomputer for correctness and error reporting. The basic arrangement for individual boards is outlined in Figure 9.

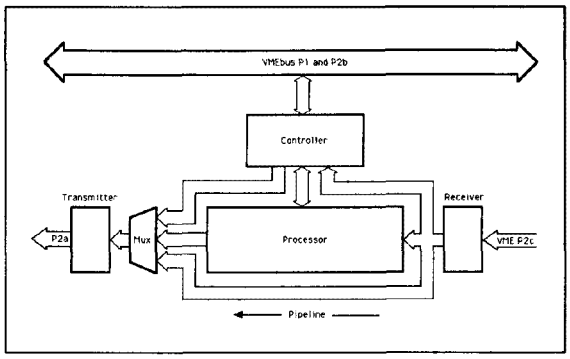

Figure 9. Board Testability Paths.

To check module interfaces, data is routed from the parallel bus, past the processor, to the module's pipeline transmitter; and from there to the receiver in the succeeding module, past its processor and back to the bus. Test data coming into a pipeline receiver, in addition to being routed directly to the bus, can be routed past the processor to the next module; or it can be passed through the module's processor. The pattern generator along with the large number of possible paths involving the pipeline and bus opens the way to extensive testing of connections, modules and combinations of them.

As mentioned above, the VME Link board outputs the pipeline processed data from the adapted VMEbus to the standard VMEbus. This output is stored in a 1 MByte SRAM in a format that is suitable for display processing by the monoboard microcomputer.

The monoboard computer is the 68030 microprocessor-based Motorola MVME147. Reading data from the SRAM, processing it for display and sending it to the Display Controller is essentially a full-time task for this computer. System housekeeping has higher priority, but takes little time. The disks are controlled through SCSI ports of the microcomputer. The RS232 and printer ports are also features of the computer.

The operator keyboard of the instrument is connected to the computer through a modified RS232 port. The Color Display monitor is connected to the Display Controller by three coaxial cables: RGB. The BNC connectors for these cables are visible in Figure 5.

Just behind the front panel of the Instrument Unit are the Analog Front End module, the disk drives and the power supply. The disk drives are accessible from the front panel (see Figure 1). A door in the bottom panel of the unit can be dropped down to gain access to the calibration adjustments and cables in the space between the VME backplane and these modules.

Thermally, the inside of the Instrument Unit is composed of two isolated compartments. One compartment contains the bus and its modules, and the other contains the power supply and peripherals. Air is drawn in low through the front, rear and sides of the unit and exhausted by five fans in the top panel. The intakes and fans are positioned for air flow diagonally from the bottom, fronts of the board to the top, backs. There is a 10°C rise in temperature of air passing through the unit. The five fans, running at a lower than rated voltage, have an acoustic noise level suitable for bench top as well as rackmount use of the instrument.

MANUAL OPERATION

The 3052 is easy to operate for anyone who has worked with a spectrum analyzer. After power-on, the instrument displays amplitude versus frequency from dc to 10 MHz. There is a span decrement key, center frequency tuning knob, and a reference level knob. With these controls, one can do a great deal of spectrum analysis.

The keyboard is designed to accommodate knob operation, keypad entry of settings, and menu call-ups (see Figure 10). There are keys to call up first level menus, and all menus are presented on an LCD display. The position of the current menu in the hierarchy is listed at the top of the LCD to prevent one from getting lost. When a menu calls for a numerical entry, it can be made by use of a third knob adjacent to the LCD, or by a numeric keypad. The keyboard can be unfastened from the Instrument Unit to be held or used in a more convenient position.

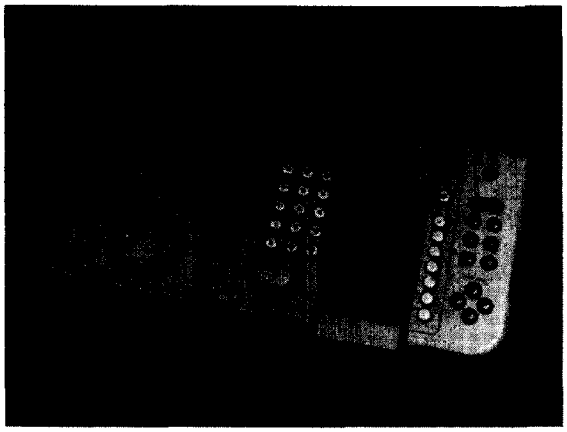

Figure 10. Keyboard.

Single- and split-screen color displays are scaled in amplitude, phase, frequency and time. They include amplitude vs. frequency, spectrogram and waterfall displays. There is also a phase vs. frequency display. The color spectrogram display shows amplitude vs. both frequency and time. This display is particularly useful with time-varying spectrums, as with modulated carriers, for example. The horizontal axis is scaled in frequency, the vertical in time, and amplitude is color coded. Figure 11 shows a split-screen display of an oscillator with a triangular sweep.

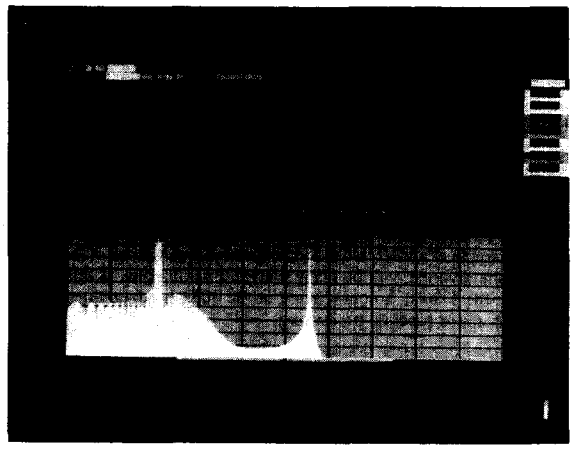

Figure 11. Split-Screen display with Spectrogram on top, and Amplitude vs. Frequency plot on bottom. Markers on peaks.

A display mode called Block Mode shows a block of 500 contiguous spectrums. Normally spectrums are not displayed sequentially, because the Instrument Unit generates them too fast for all to be displayed. In the Block Mode, a block of sequential spectrums is collected in the SRAM, and then displayed. During the display processing, of course, the SRAM is unavailable to collect further spectrums, and those spectrums are not displayed. This mode of display adds an important alternative to those provided by the Display Formatter board, which has no ability to collect spectrums.

Marker capability is now common in modern spectrum analyzers to assist the operator in reading out values, and to locate peaks and tune to them. On the 3052, the marker function keys are located on the right-hand side of the keyboard, and the markers are visible on the display. An added capability in this instrument is the readout of time by use of markers in a spectrogram. The marker readouts for this mode of operation are amplitude, frequency, and time; and their deltas.

As operators gain experience, they may notice that a certain sequence of key strokes is needed repeatedly. Thereafter the operation can be simplified by collecting the sequence in a keyboard macro. The operator simply calls up the Macro Program Menu prior to entering the sequence, and turns on Macro Learn. Then he enters the key strokes, as he normally does, turns off Macro Learn, and binds the macro to one key. Thereafter, the macro is executed by simply keying in Execute-Key, where Key is the key that was bound to the macro.

Color screen copy is executed from the keyboard by pressing the Screen Copy, when the optional 4693RGB Color Printer is attached to the 3052. This attachment is made by teeing into the RGB cables that connect the Display Controller to the Color Display Monitor.

DSP PROGRAMMING

Stored on the disk is Motorola System V/68™[3], which contains a version of UNIT™[4] suited to the VMEbus. Included are software tools for writing, compiling and storing C-language instrument control programs and signal processing programs. To access these facilities, the user connects a terminal to an RS232 port and logs into the operating system.

A C-library provides an interface to the instrument's master control program. Once the program has opened the instrument by execution of the ic_open( ) function, the extensive set of signal processing and control commands is available to the program. These commands are IEEE 488.2 compatible. The combination of software and hardware provides a DSP programming environment.

Control programs can be executed from the instrument keyboard, or from the terminal. Signal analysis programs can be executed on spectral data that has been saved on disk, or on data from the pipeline. Pipeline data can be streamed to analysis programs one spectrum at a time at rates up to 2 ms per spectral frame. The throughput of these programs, of course, depends upon their run time, and they run by far the fastest when the program puts the instrument in the sleep mode to free the monoboard microcomputer from display processing.

RF SYSTEM

Addition of a 2756P Spectrum Analyzer, RF160 Down Converter, a GPIB interface board, and driver software expands the 3052 into an RF system (see Figure 12). This system performs real-time spectral analysis in a 2 MHz span centered anywhere in the range 100 Hz to 21 GHz (or to 325 GHz when waveguide mixers are used).

The system software enables the 3052 to control the 2756P (or any other Tektronix 490 Series or 2750 Series Spectrum Analyzer) by GPIB (IEEE 488). The 2756P functions as a tunable RF receiver, and the RF160 brings its 110 MHz IF output down to 7.5 MHz for real-time analysis on the 3052. The operator controls the system from the 3052 keyboard while viewing correctly scaled displays on the Color Display Monitor.

[3] System V68 is a trademark of Motorola.
[4] UNIX is a trademark of AT&T.

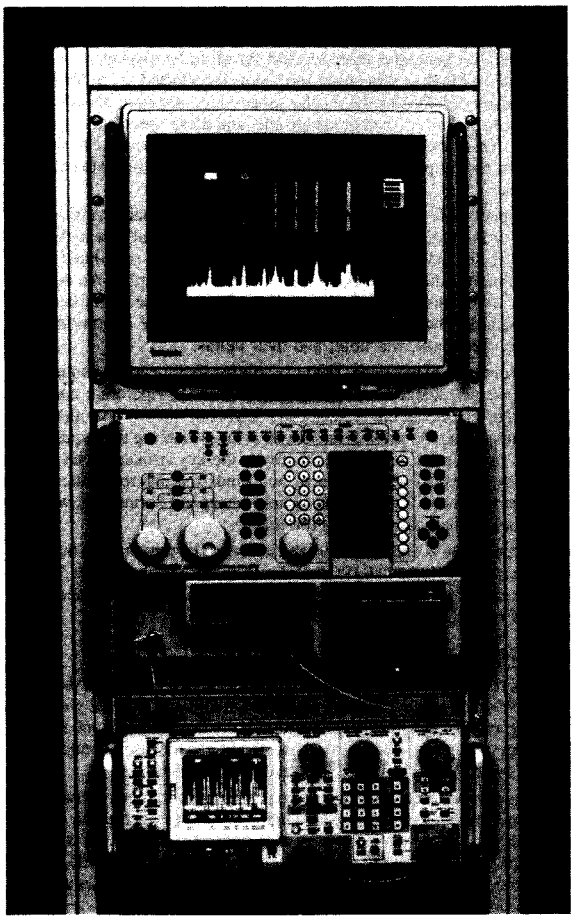

Figure 12. RF System: 3052 Digital Spectrum Analyzer, 2756P Spectrum Analyzer, RF160 Down Converter.

SYSTEM COMPONENT

The 3052 can also serve as a component in a larger signal processing or automated test system. For instance, it may be used as a DFT engine in a larger signal analysis system. The optional Real Time Interface (see Figure 2) provides spectral data output at full rates (up to 5,000 spectral frame per second). The complex data are output from two connectors operating in parallel; one carrying real data, and the other, imaginary. Magnitude and phase are also available by keyboard selection. This output is suitable for further real-time processing equipment capable of demodulation, signal correlation, or other analysis functions.

The 3052 has other data ports. Already digitized data may be input at the Auxiliary Digital I/O port, immediately following the analog to digital converter. Down converted and band limited time domain data can be output from the Digital Down Converter at the Time Domain Digital I/O port. This data might be digitally demodulated. In-phase and quadrature time-domain data also can be input at this port directly to the Parallel Filter Bank for immediate spectral conversion. Figure 13 shows the rear of the Instrument Unit complete with panel, and so highlights the ports.

The 3052 can be GPIB remote controlled for use in ATE. It accepts an extensive set of IEEE 488.2-compatible device dependent messages. Spectrums, blocks of spectrums, instrument settings, macros, and control programs can be down loaded from the GPIB controller at the beginning of a test, and then be called into use as needed by the test program. Alternatively, these items can be stored permanently on disk in the 3052 to reduce bus transfers during testing to simple commands and returns of finished measurement results. GPIB transfer rates of 300 kBytes/s are possible with the 3052.

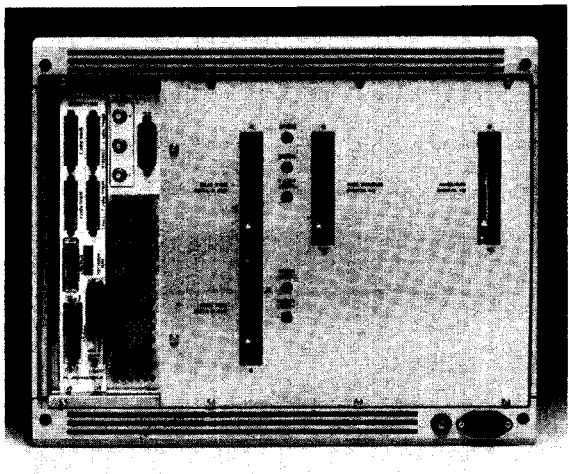

Figure 13. Rear Panel Ports.

Also useful in systems applications are the time-domain trigger and spectral event detection capabilities. Control of the acquisition of signals is available through an oscilloscope-like trigger capability. Spectral event detection capability is available on the Real Time Interface board. It tests every frequency in every spectral frame against an upper and lower limit spectrum. Each time a signal goes outside either of these limits, it is detected as a spectral event, and a spectral-event trigger is generated. This spectral event trigger may be used internally to, say, start execution of a key-stroke macro or stored program, or it may be used externally by the system.

CONCLUSION

The 3052 Digital Spectrum Analyzer is an example of a test and measurement instrument that is based on the VMEbus, and is essentially a filled-enclosure instrument. Though designed primarily to be a stand-alone instrument, it easily expands to system applications. As a real-time spectrum analysis instrument, its performance, capability and human interface represent a quantum advance. The advance is due in large part to the facility, modularity, compactness, and adaptability that the bus provides, and to the industry support that it has. The 3052 is perhaps not the only example of a VMEbus-based instrument, but it is one of the first, and undoubtedly there will be many powerful instruments of this class to come in the 1990's. A contribution of the 3052 is adaptation of the bus to high-speed pipeline processing.