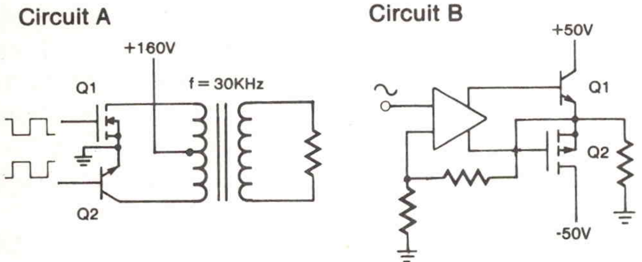
component news

February 4, 1981 COMPANY CONFIDENTIAL Issue 286

Power FET characteristics

The evolution of power MOSFETs has settled to the point where their general characteristics are now evident. Evaluation and characterization has revealed unexpected behavior in their temperature coefficients that will require compensation in most linear applications. Super linearity was predicted but was not found, while other traditional FET characteristics were verified. Distortion comparisons made with equivalently rated bipolar transistors found the bipolar superior in some respects.

Circuit A Circuit B



Which type transistor is best for each circuit, Q1 or Q2? The following article will help answer this question.

Introduction

The past year has seen the introduction of a variety of new power FETs, with the most important developments being high power switching types and N- and P-channel complements. Very soon it will be possible to choose a FET for almost any circuit that traditionally used bipolar transistors, and for other applications where no bipolar solution is possible. Then, a component will be selected not on the basis of availability but on other factors such as performance and cost effectiveness.

As far as prices are concerned, most FET manufacturers admit that exact price parity with bipolars will probably never be reached. However, they agree that the premium paid for FETs should be less that 15% in large quantities. Even then, other factors such as simpler drive requirements can make them the best and most cost-effective choice. Already the price of some parts has fallen to only slightly more than an equivalent (voltage and current rated) bipolar.

With the choice becoming one of performance alone, a detailed comparison of FETs and bipolars is in order. The power FET certainly does have many advantages over bipolars, but we now know that some of the early claims (I've made them myself) have been overly ambitious.

The four advantages of FETs that were originally thought to be inherent in them are:

1. Negative temperature coefficient of drain current (making thermal runaway impossible),

2. No secondary breakdown — power limited only (which is also related to their negative TC),

3. No storage time (due to majority carrier operation), and

4. High input impedance.

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Also in this issue

To these four also were added later claims of high voltage simultaneous with high f_T and high linearity (in some cases thought to be nearly perfect).

Each of these six characteristics will be discussed and comparisons made to bipolars to allow circuit designers to select the best part for a particular application.

Temperature coefficient

The assumption that all FETs have a negative TC of drain current stems from the days when most FETs in use were small signal JFETs. These parts did indeed have a negative TC over *most* of their drain current range. But, at low drain currents the TC was positive, passing through zero TC at some current then becoming negative from there on.

In small signal JFETs the zero TC crossover current was so low that most were never biased there because the g_m was also very small at that point. So, in the majority of applications a significant negative TC was always observed. With small MOSFETs the situation was the same.

Making a FET larger also raises its zero TC current proportionally, because it's like adding FETs in parallel. Thus, a power FET in general would have a more noticeable range of drain current where TC is positive.

A MOSFET's TC is the combined effect of the TC of the threshold voltage and channel resistance. In modern power FETs, the channel resistance is made very small for a given device size by reducing the channel length (which, incidentally, also increases the g_m and frequency response). But, another unexpected and somewhat undesireable result is that the channel resistance contribution to the overall TC is also reduced, which shifts the whole TC characteristic in the positive direction. In most power FETs the TC is positive to about 25% of the drain current rating where it passes through zero and goes negative.

Consequently, a 10A FET will have a positive TC up to 2.5A. If it's operated in a linear amplifier circuit with a smaller quiescent bias — say 200 mA — the bias will have to be temperature stabilized to keep the operating point constant (see Table 1).

Intersil	IVN5201	2.5
Supertex	VN1206	4.2
Supertex	VN0304 (400V)	2.5
Siliconix	VN84G	3.8
Siliconix	VN4002 (400V)	3.6
IR	IRF150	>16
IR	IRF350 (400V)	>16
Motorola	PF848 (400V)	4.2
Hitachi	2SK134	0.12

Table 1 — Zero TC drain current (A)

Learning that a FET needs thermal compensation would seem to make it no better than a bipolar in this regard. In fact, in one way it's worse: the bipolar V_{be} temperature coefficent is the convenient 2mV/°C, the same as for a diode which is the component frequently used for temperature compensation. The FET, on the other hand, has a TC that depends largely on how it's made and also varies with drain current.

Fortunately, the FET's positive TC is weaker (because of lower g_m) than a comparable bipolar and is self-stopping at some drain current. Nevertheless, it's not likely that many linear circuits will tolerate the TC without compensation. All power FET specs have, or soon will have, TC graphs from which compensation schemes can be designed (see Figure 1).

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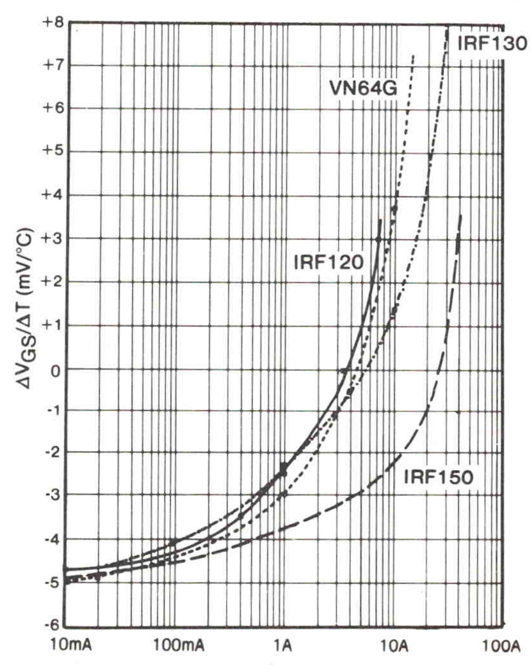

Figure 1

All of this is true for the "pentode" region of the operation only. When operated as a fully-on switch, the on-resistance will still have the expected positive TC (see Figure 2). This feature makes it possible to parallel devices without ballasting them and limits current at high temperatures.

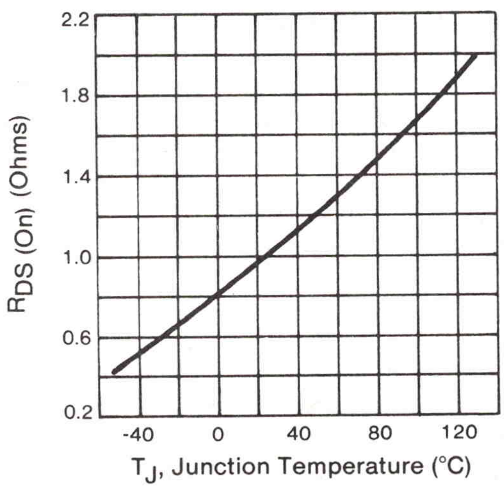

Figure 2

Secondary breakdown

The significance of secondary breakdown in a bipolar transistor is that a part's power rating diminishes badly with increasing collector voltage. This derating begins in some parts at only 10% of their rated voltage (see Figure 3). FETs, on the other hand, are power limited only out to

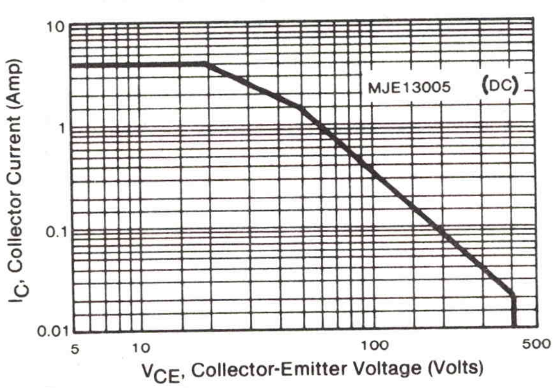

Figure 3A — This figure shows a typical bipolar transistor Safe Operating Area (SOA) graph. To be noted is the break in the 45° diagonal line at 60 volts. From that point on the angle is steeper — the significance of which is often not appreciated.

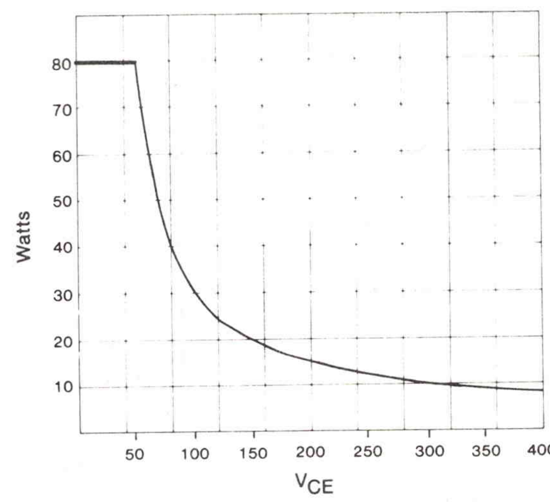

Figure 3B — This is Figure 3A replotted to reveal the rather gross amount of power rating lost at high collector voltages.

their maximum rated drain voltage and most can dissipate tremendous power levels for short periods of time (see Figure 4).

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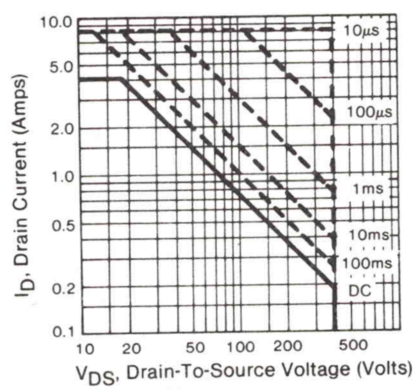

Figure 4A

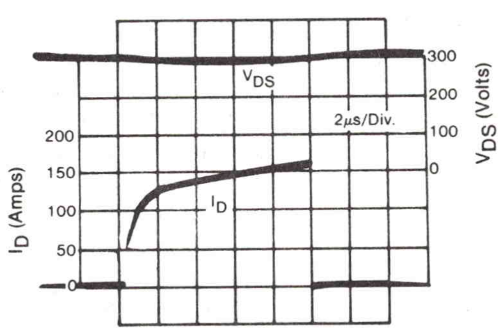

Figure 4B

Figure 4A and 4B — The Safe Operating Area graph for a power FET shows it is power limited only (no break in the 45° line). But, even more impressive is the fact that they can deliver tremendous power surges that totally eclipse any bipolar. Notice that the FET in Figure 4B (IRF350 HEXFET) is sustaining 45,000 watts of power!

If, however, the voltage is increased to the breakdown point, both FETs and bipolars can be quite fragile. Sometimes the drain or collector voltage will latch back to a lower value, passing through a negative resistance region. The collapsing impedance usually allows the power supply to dump into the part, causing permanent damage or destruction.

This phenomenon has mistakenly been called secondary breakdown by some, insinuating that FETs have it too. Two things can be said about this. First, that all power FETs can in fact deliver full power out to, but not including, their breakdown voltage. Operating any device beyond its rating is sort of illegal anyway. Second, power FET designers have found a way to completely eliminate the latch-back problem from parts in a way that is impossible with bipolars. Now, most power FETs can dissipate their whole power rating *in breakdown* and survive.

Storage time

Any P-N junction that is forward biased has a stored charge of minority carriers. In normal operation, a FET has no forward biased junctions, whereas a bipolar must forward bias the base-emitter junction to operate, and the collector-base junction gets forward biased when it's in saturation. Thus, by the nature of their operation, FETs have no storage time but bipolars do.

There is an operating condition in MOSFETs that creates an effect that resembles stored charge although it really isn't. Because the gate is insulated from the channel, it is possible and often desireable to apply a gate voltage much larger than the amount required to drive a part to its low on-resistance state. This is to ensure deep saturation of any part placed in the circuit. Keep in mind, though, that any gate voltage above the minimum required amount is just extra charge stored on the gate capacitance that must be removed before the FET will begin to turn off. However, even when present this effect is smaller than the real stored charge of a bipolar.

Input impedance

The high input impedance of the MOSFET is useful or even essential to some designs. But in fast switching power circuits the considerable gate capacitance must be driven from a low impedance source similar to that required for a bipolar, although the resulting switching speed of the FET is much faster. And, in the case of square waves, current only flows during transitions; no sustaining power is consumed by the gate.

Voltage-speed product

One area where FETs really shine is where high speed and high voltage are required simultaneously. Bipolar transistors are limited by the fact that a thick base region is required for high breakdown voltage, but a thick base also means long carrier transient time thus low f_T. In FETs there is a correlation with channel length, but the fundamental difference between a base and a channel is that of minority vs, majority carrier operation. Minority conduction through the base is by diffusion, a relatively slow process where channel minority carriers are aided by an accelerating electric field which greatly reduces their transient time.

For an example of this difference we can compare a 700V (BV_{CEO}) bipolar transistor (BU 207) to a 1,000V power FET (BUZ 54). The bipolar's f_T is 4MHz where the FET's equivalent f_T ($g_m/2\pi C_{in}$) is **928MHz.** Because of parasitic resistances the FET's high frequency performance won't go nearly that high, but it will still be far, far greater than any bipolar could ever hope for.

At the high frequency end of things we have FETs with f_T's of 1.5GHz with breakdowns of 160V, which is at least twice the breakdown of the best bipolar. The ultimate limitation in speed-voltage product for FETs is unknown, but the numbers given above are probably going to be hard to improve upon.

Linearity

The study of power FET linearity has produced some unexpected and somewhat disappointing results.

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Theoretically, the FET seemed always to enjoy a linearity advantage over the bipolar, which is evident from examining their transfer functions, where:

$$I_C = I_S \, e^{\left(\frac{q}{kT} V_{BE}\right)} \quad \text{for the bipolar, and}$$

$$I_D = \tfrac{1}{2}\mu C_{OX} \, W/L \, (V_G - V_{TH})^2 \quad \text{for the MOSFET}$$

The FET's "square law" characteristic indicates that only second harmonic distortion will be produced by it, while the bipolar's exponential function can be expected to produce all orders of harmonics.

Also, in FETs with short channels, carrier velocity saturation produces a saturating transconductance at high drain currents, resulting in a very straight gate voltage to drain current transfer function (see Figure 5). Such a FET should produce only second harmonics at low drain currents, and even these would diminish to practically zero when the device was biased into velocity saturation.

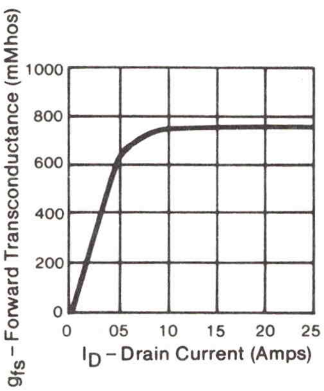

Figure 5A

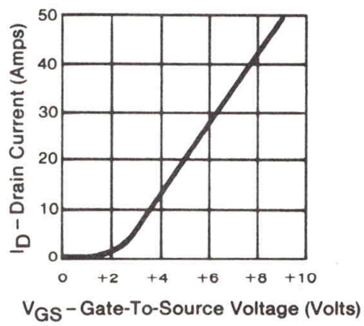

Figure 5B

Figure 5A and 5B — Here we have the effects of velocity saturation of the carrier in a short channel FET. From the looks of the graphs, the distortion produced by such a part should be near zero, but it's not, as can be seen by data following later.

The tests conducted to verify FET linearity showed the linearity of comparable FETs and bipolars to be not much different from one another in kind or quantity. The FET distortion did not disappear as theory predicted at any current, and traces of third harmonics were evident under most conditions. Far from being inherently inferior, the bipolars often gave better results (see Figures 6-9).

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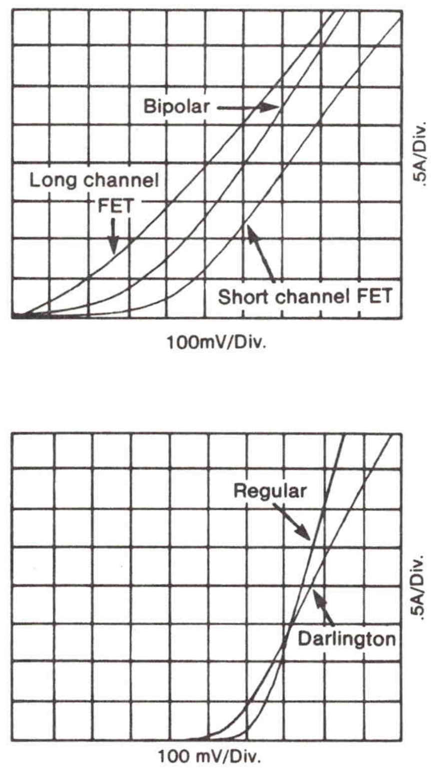

Figure 6 — Bipolar transistor linearity isn't bad. The top illustration compares the transconductance of a long channel FET, a short channel FET and a bipolar. The relative straightness of the lines is not much different and, as seen in Figure 7, produces about the same distortion.

The lower graph compares a Darlington to a regular part. The difference in angle shows the Darlington to have lower transconductance (gm) due to its two base-emitter junctions in series. A compounded curvature was expected for the same reason, but the transfer function is nearly ruler straight. (For this comparison the gate/base drives and horizontal position were adjusted to align the displays.)

The devices: **Bipolar — Motorola MJ15003**
Long channel FET — Hitachi 2SK134
Short channel FET — Supertex VN1206

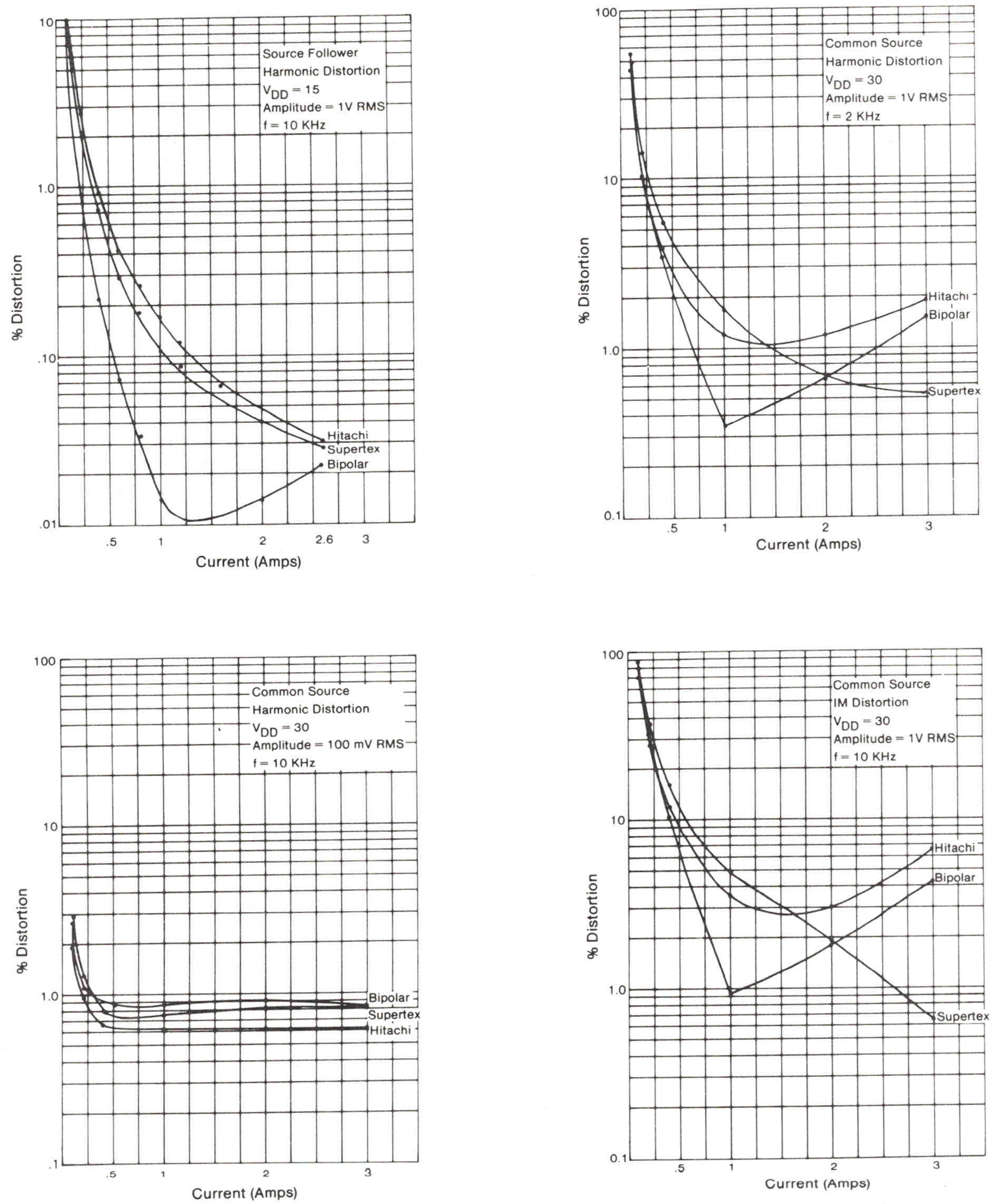

Figure 7 — Distortion measurements for FETs and bipolars. Source and load impedance was 600 and 8 ohms, respectively. The amplitude referenced is the RMS voltage across the 8 ohm load. The dip in bipolar distortion is curious and will be commented on later. (Devices are the same as in Figure 6.)

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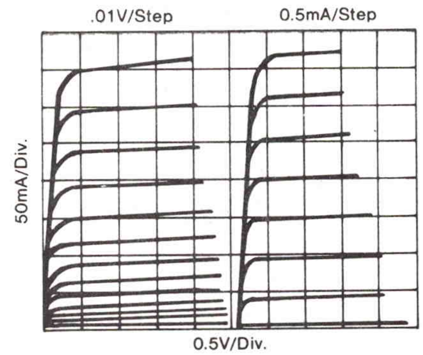


Figure 8A

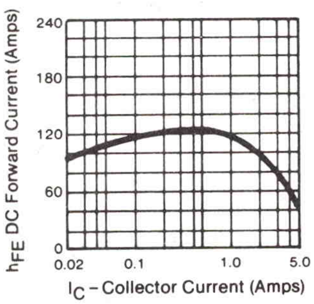


Figure 8B

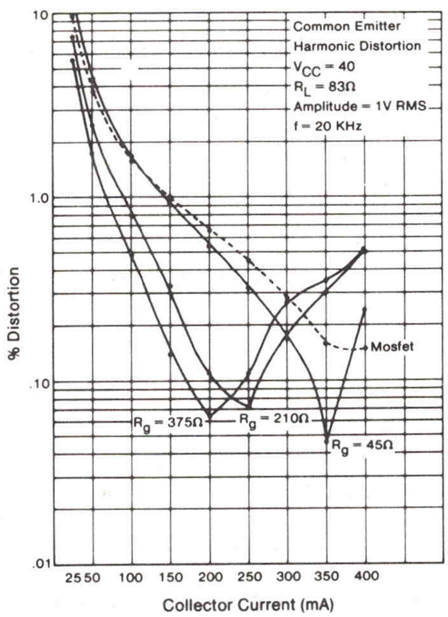


Figure 8C

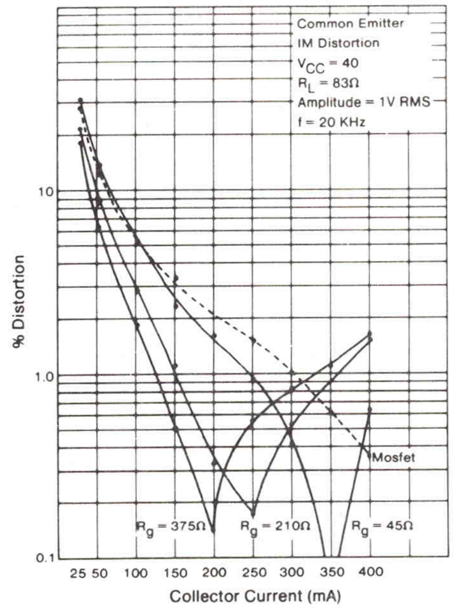


Figure 8D

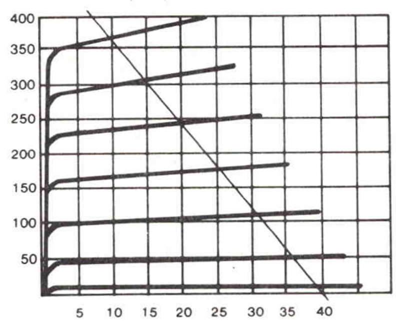


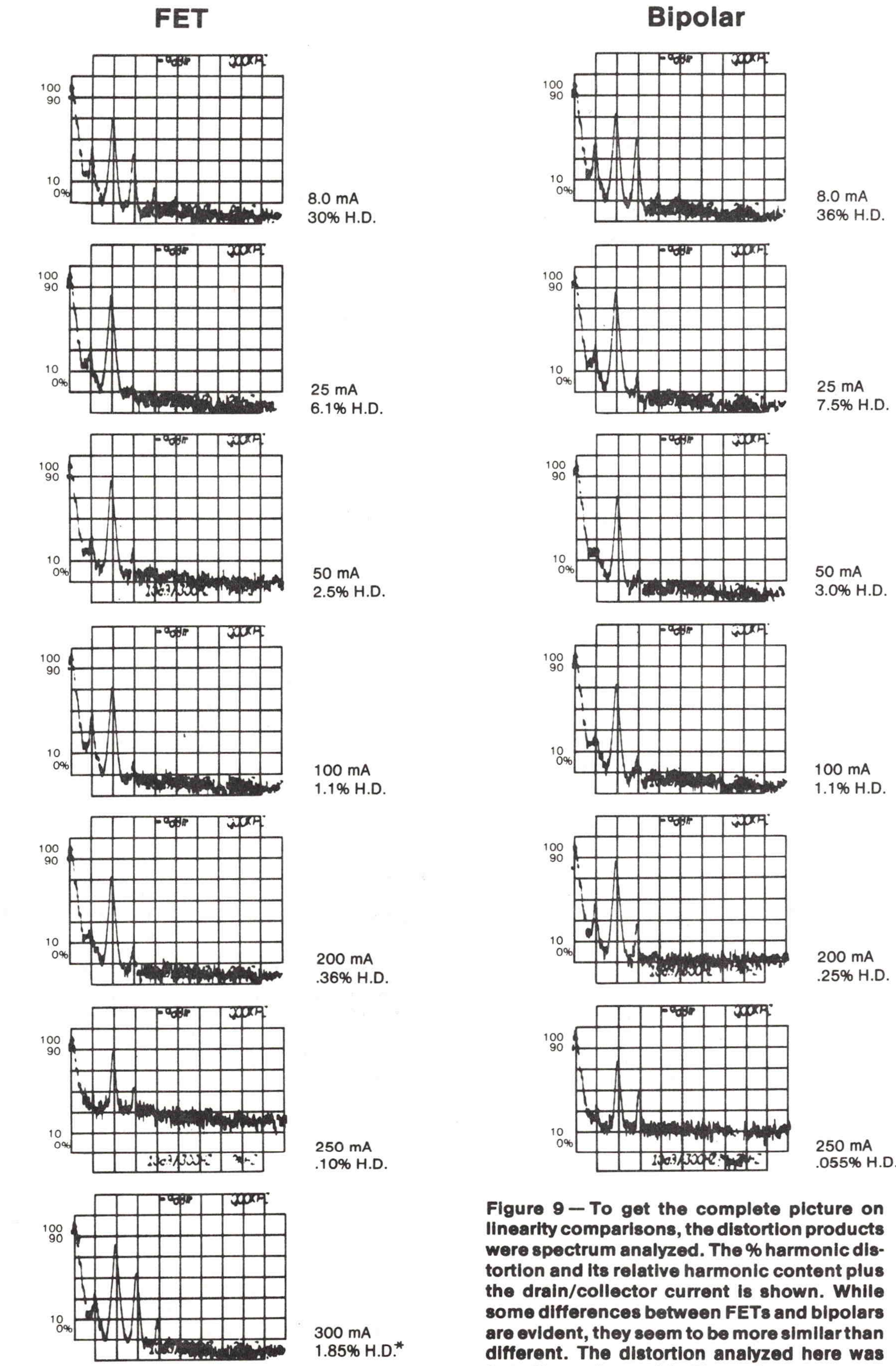
Figure 8E

Figure 8 — A possible explanation for the dip in the distortion of every bipolar transistor measured is that a bipolar produces two different characteristics when its driven from a voltage source and a current source.

When voltage driven, the family of curves expands with increasing collector current in more or less agreement with the formula given in the text. When current driven the situation is reversed – Beta (current gain) falls off a higher current (B). When driven from a source resistance in between, as is usually the case, the two conditions will tend to cancel one another, producing a zone of high linearity.

Changing the source impedance should have an effect on the location of the null – and indeed it seems to do just that (Figure 8C and 8D).

Figure 8E shows the load line, indicating that the sharp increase after the dip is not due to clipping. The devices tested were: Bipolar – 2N4895 (Fairchild), MOSFET — VN01 (Supertex). Note that the characteristic contour for bipolars is the same in spite of the parts being considerably different. The MJ13003 in Figures 6 and 7 is an epibase power part (20A, TO-3), while the 2N4895 is a small signal, double-diffused part (1A, TO-5).



*Clipping began at 300mA, so the bipolar measurement was not repeated.

Figure 9 — To get the complete picture on linearity comparisons, the distortion products were spectrum analyzed. The % harmonic distortion and its relative harmonic content plus the drain/collector current is shown. While some differences between FETs and bipolars are evident, they seem to be more similar than different. The distortion analyzed here was from the parts used in Figure 8.

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Conclusions

The clear advantages of the power FET over a bipolar can be summarized as:

1. No second breakdown, with high energy absorption capability in breakdown,
2. No storage time,
3. High speed with high voltage capability, and
4. High input impedance at DC.

Areas where the choice is not so distinct are:

1. Thermal stability of quiescent current. Here, unlike a bipolar, a FET will reach a stable current eventually but, depending on the application the stable current may be harmfully high. At lower and more common quiescent currents compensation must be used; and
2. Low distortion circuits. Overall amplifier distortion figures may be better with FETs, but it will be due to other condiderations, not linearity.

If you have any further questions, please contact me at 78-557, ext. DR-2539.

Jerry Willard
Analog Component Engineering

Ribbon cable stranding change

Stranding on Tek's 22 AWG ribbon cable will change from 19 strands of 34 AWG wire to 7 strands of 30 AWG wire. This change is due to continuing availability problems with 19/34 strand wire — our suppliers have difficulty meeting shipping dates and this often leaves us in a shortage situation.

Testing has shown that the 7-strand cable works well in production and provides greater flex strength than the 19-strand cable. Our tests compared the flex life of both cables, and the 7-strand material withstood an average 31% more flex cycles before failure. Test results are summarized below.

7-strand sample	Flex cycles to failure
1	420
2	260
3	250
4	370
5	260
6	425

19-strand sample	Flex cycles to failure
1	195
2	260
3	244
4	150
5	280
6	230

	7-strand	19-strand
Minimum flex cycles to failure	250	150
Average flex cycle to failure	331	227

By changing to the 7-strand cable Tek will realize a cost savings, lead time will be cut in half and we will no longer be faced with shortages.

If you have any questions about this change, please contact me at 78-552, ext. DR-2309.

Elizabeth Doolittle
Optoelectronic and Passive CE

International power options clarified

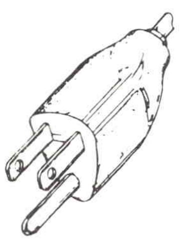
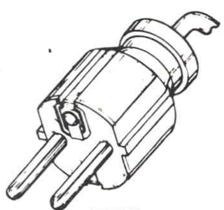
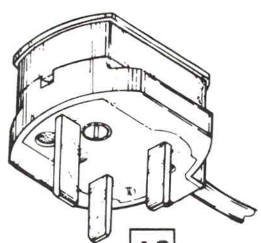
There have been several questions raised concerning the use of the international power cord options (see **Component News 269,** page 7). Due to different interpretations of the intent of the program, various methods of implementation have been used. The result has been confusion, both within the business units and by international support groups.

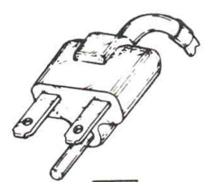
A common misconception has been that the power cord option is used **only** to obtain the appropriate power cord and plug configuration. If used that way, another option is then required to set the appropriate line voltage, frequency, etc. That results in a more complex ordering and processing structure.

It is intended that options A1 through A4 be used consistently throughout the company to provide instruments which are fully operable without ordering an additional (inconsistent) option. This will avoid confusion in the international marketplace and provide for accurate and efficient order processing.

Descriptions of the power cord options are shown below. Questions concerning these options should be directed to the appropriate individual:

Product Safety	Wally House (ext. 7374)
Order Processing	Yves Tournefier (ext. 5735)
New Product Introduction	Gary Hamrick (ext. 7965)



	50Hz operation	50Hz operation	50Hz operation	60Hz operation
Power Cord Option Number →	A1	A2	A3	A4
North American 120V/15A	**Universal Euro 220V/16A**	**UK 240V/13A**	**Australian 240V/10A**	**North American 240V/15A**
161-0017-00 →	161-0017-13	161-0017-14	161-0017-15	161-0017-16
161-0033-03	161-0033-27	161-0033-28	161-0033-29	161-0033-30
161-0033-04	161-0033-31	161-0033-32	161-0033-33	161-0033-34
161-0033-07	161-0033-35	161-0033-36	161-0033-37	161-0033-38
161-0033-09	161-0033-39	161-0033-40	161-0033-41	161-0033-42
161-0049-00	161-0049-06	161-0049-07	161-0049-08	161-0049-09
161-0066-00	161-0066-09	161-0066-10	161-0066-11	161-0066-12
161-0107-00	161-0107-03	161-0107-04	161-0107-05	161-0107-06

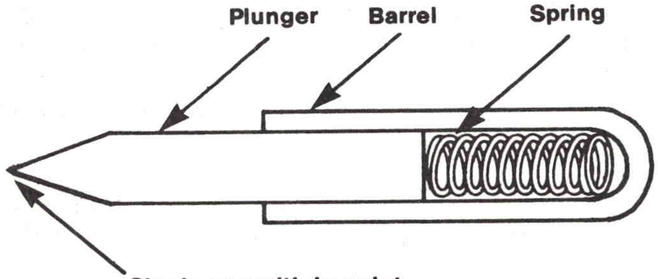
ATE probe pin evaluation completed

Unstable measurements on in-circuit components was recently traced to probe pins in some of our automated test equipment (ATE). Fluctuations of from 100mΩ to over 1Ω prompted an evaluation of probe pins from four vendors.

Why evaluate probe pins?

When Tektronix began operating in-circuit testers, it was soon noticed that measurements were unstable. In testing the same circuit boards for repeatability, consistent results could not be obtained. Today, the problem is more serious because probe pins must accommodate generation of currents and voltages in microamps and microvolts, plus allow for in-circuit testing of critical components.

Our analysis of probe pins began by generating programs that allowed testing and characterization of the pins within the fixtures themselves. We were able to characterize the pins from a few hundred milliohms to greater than one ohm. The average cost of the probe pins was about 80¢ in quantities of 10,000. However, the actual cost in lost production time, lost engineering time, lost machine time and excessive maintenance time placed the cost of replacing probe pins at around $10 or more per pin.



Typical spring probe contact

Before testing could begin we had to define what reasonable performance levels would be acceptable for probe pins used in production in-circuit testing. A reliable pin was defined as one capable of maintaining total resistances from point-of-contact to contact-of-wire wrap of 50 to 150mΩ maximum resistance (preferably a constant resistance), and capable of lasting approximately 10,000 mechanical cycles.

Contact degradation is the cause

Probe pin resistances were found to fluctuate from between 100 milliohms to over one ohm, when only the probe pins were measured. To find the cause of this problem, the Tek electron microscope facilities evaluated the probe pins for the following:

1. Contamination of the contact point
2. Wear of the contact point
3. Contamination of plunger to barrel
4. Wear of plunger to barrel
5. Contamination within barrel
6. Wear and spring pressure
7. Metals used in probe pins

This initial evaluation pointed to several problem areas. General immediate deterioration of the probe-to-circuit board contact (due to the loss of rhodium) and nickel-oxide and iron-oxide contamination was discovered. Also, a long term deterioration of overall critical measurement capabilities was caused by the continuous flaking of rhodium and oxidation of base metals. We concluded that these problems make the probe pins unacceptable for critical measurement systems.

Vendors notified

Our four vendors were notified of the test results, and work began to redesign the probe pins. We visited the vendors and offered suggestions concerning the type of metals, designs and QC changes that would hopefully resolve the problems. Within two months we began receiving sample probe pins. Production test sites were chosen in addition to the environmental lab testing. These new probe pins were then tested under the constraints placed on measurement capabilities — 50 to 150mΩ of resistance within minimum 10,000 mechanical cycles before failure.

The Tek Environmental Lab was used to generate life cycles on vendor probe pins and the electron microscope was used to evaluate the pins after testing for wear, contamination, etc. A life cycle fixture was selected that rotated the probe pins and provided side loading. The pin circuits were powered with a voltage of 200mV. This simulated general production in-circuit testing configurations. Periodically, the overall resistance of the probe pins was recorded.

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Test results

The four probe pin vendors are: Everett Charles, Pylon, Fairchild, and Ostby and Barton. At this time, Everett Charles has not submitted pins that are acceptable to production ATE needs. Following is a summary of the results from the remaining three vendors.

Two of the Pylon probe pins (P4703 and P4680B) were the best evaluated. These provided side loading via the design, and no erroneous measurements have been seen using these pins. However, the waffle head design tends to become more easily contaminated, so if the boards are dirty there is more chance of contamination.

The Fairchild crown head probe pin is the most versatile probe pin we tested because it can be used as a waffle, pointed and occasionally as a pyramid probe pin. For most applications this would be the best choice. However, the size of the probe pin head is larger than most, and it can cause contact to runs or pads that are close to the desired contact or node point location.

Another very minor problem with this pin is that it doesn't force a side loading contact. Its manufacture assumes that there will always be side loading present on the circuit board connection. Sometimes this side loading condition doesn't occur and the measurement becomes erroneous. After this probe pin was evaluated, Fairchild reported that they had redesigned a smaller crown headed probe pin which should correct the contact problem; no redesign is planned to accommodate side loading, though.

The Ostby and Barton probe pins were the poorest tested. General deterioration due to loss of plating materials was the biggest cause.

The results of these tests would indicate that the better performers in terms of overall low contact resistance through a large number of cycles have gold plated plungers and points. On the other hand, rhodium (although a hard, wear resistant material) appears to be ill-suited plating for the plunger and point. There is evidence that it flakes off, leaving the base material more prone to corrosion.

For more information

If you have any questions about this evaluation, or to receive a copy of the complete test results, please contact me or Bob Beville on ext. DR-2789. For information about the Environmental Lab test results, contact Tom Basta on ext. 7887.

Larry Cox
SID ATE Test Engineering

PIC switching components not recommended

Unitrode Corporation has a family of power transistor hybrids known as PIC (power integrated circuits). These components generally consist of one or two transistors, a diode and sometimes resistors. Packaging is done in non-standard, multi-leaded, exclusive to Unitrode variations of TO-3 and TO-66 metal can cases.

This family of devices is *not recommended* for several reasons. One crucial reason — no true alternate source exists. Even though Silicon General is supposed to be an alternate source, SG is a small bipolar integrated circuit company, *not* a power device manufacturer. In fact, SG has admitted that they buy these items from Unitrode. Another aspect of this problem is that the functions and packaging of PICs are so unique that no other industry standard device will function in its place.

If Unitrode was a more reliable source of supply, these objections could possibly be discounted. Unfortunately, this is not the case, and invites the risk of continuing problems with line shutdowns.

If you have any questions about these parts, please contact **Jim Williamson (78-557), ext. DR-2552.**

TECHNICAL STANDARDS

The function of Technical Standards is to identify, describe, and document standard processes, procedures, and practices within the Tektronix complex, and to ensure these standards are consistent with established national and international standards. Technical Standards also provides a central repository for standards and specifications required at Tektronix.

New documents (copies may be ordered through Technical Standards)

MIL-S-9395/27E	AMENDMENT 1 **Switches,** Pressure, Gauge (Type II), 3 Amperes
MIL-C-83503	AMENDMENT 2 **Connectors,** Electrical, Flat Cable, Nonenvironmental, General Specification
MIL-R-83725B	**Relays,** Vacuum, General Specification
MIL-C-81659/54A–Cancelled	**Connectors,** Electrical, Rectangular, Plug, Environment Resistant, Crimp Contacts, Triple Insert, Type II, Class 2
NBS-TN-910-1	Self-Study Manual on Optical Radiation Measurements. Part I — Concepts
NBS-TN-910-3	Self-Study Manual on Optical Radiation Measurements. Part I — Concepts, Chapter 6
MIL-0-83804A	Superseding MIL-0-83804. **Oscilloscope** (AN/USM-426(V)), 250 Megahertz (MHz), General Purpose
MIL-C-28804A	AMENDMENT 1 **Connectors,** Electrical, Rectangular, High Density, Polarized Center Jackscrew, General Specification for
ANSI	**Metric Fastener** Standards Log
DOD 4120.3-M	Defense Standardization and Specification Program Policies, Procedures and Instructions
MIL-M-63038B	Manuals, Technical: Organizational or Aviation Intermediate, and General Support Maintenance
MIL-F-60890	**Fuse,** Mechanical Time, M591, Assembly
MIL-E-51390A	Electronic Module Assembly
MIL-E-45962	Electronic Components Assembly (11691622)
MIL-A-55443B	**Analyzer, Spectrum** AN/UPM-110, Packaging of
MIL-M-85401	Manuals, Technical, Conventional To Microfilm Compatible, Conversion of
MIL-S-87966	**Safety Equipment,** Fall Arresting
MIL-S-40034B	**Screens,** Halftone Contact for Photolithography
MIL-P-46179	Plastic Molding and Extrusion Material, Polyamide-Imide
MIL-E-87145	General Design Specification Environmental Control, Airborne
IEEE Publications Bulletin	This Bulletin is the official announcement vehicle for IEEE publications, information and educational services. Its purpose is to list all conference records, standards, special issues of Transactions and Journals, and other nonperiodic publications that may be purchased from the IEEE Service Center.

100K ECL specs changed

Fairchild Semiconductor has recently informed us that all AC specifications for 100K ECL parts packaged in cerdips will be subject to a 200pS delay increase beyond current data book figures. This change arises from the fact that the corner-to-corner delay time for the 400 mil, 24-pin DIP is approximately 400pS longer than the same measured delay through a flatpack.

Fairchild intends to incorporate this change in their next ECL data book. In the interim, the maximum propagation delay times for 100K devices in cerdips can be calculated by adding 400pS to the published flatpack delays.

If you have any other questions, please contact **Ken Smith, ext. DR-2573.**

Applying digital delay lines

In recent months there has been an increase in interest and usage of digital delay lines. We have part numbered several lines with delays from a few nanoseconds to 200 nanoseconds.

Following are some application notes from Pulse Engineering, Inc. to aid engineers in applying this component.

Time synchronization

Information in a pulse train is stored two ways. One is the time between pulses; the other is the length of the pulses, more commonly known as the pulse width (see Figure 1). The primary application of delay lines is that of delaying one pulse train with respect to another to synchronize them in some manner.

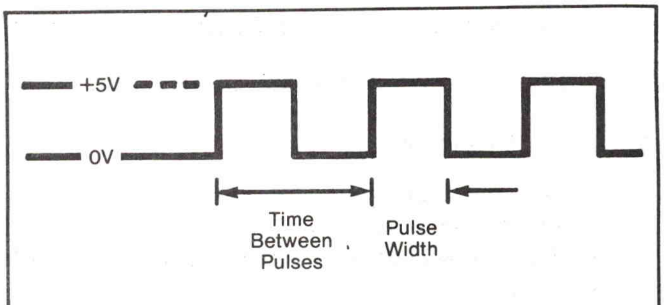

Figure 1

An example of time synchronization is shown in Figure 2. Here, pulse train 1 enters logic circuit 1 and is processed. The duration of the processing is 100nS. Pulse train 2 enters logic circuit 2 and is processed in 20nS. However, it is required that both pulse trains enter logic circuit 3 at the same time. What to do? Add an 80nS delay to pulse train 2.

This is the most common use of delay lines in a digital circuit.

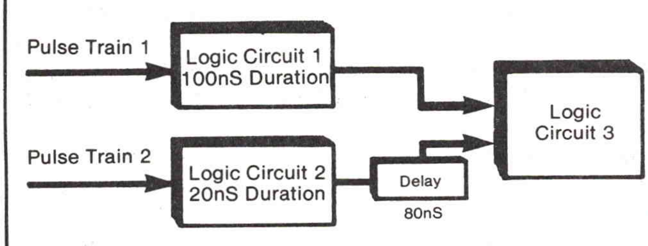

Figure 2

Pulse reshaping

In this application information is coming from a disc read head and the pulses are not very shapely. What is required is that the pulses be 150nS in width and occur as they are stored on the disc. The most economical way to do this is with a one-shot. However, due to the rapid speed (down to 300nS between pulses) one-shots are too unstable because of jitter at high duty cycle rates (see Figure 3).

Asynchronous clock generator

By combining inverters and AND gates, you can modify clock pulses to occur at different times and different pulse widths to perform many

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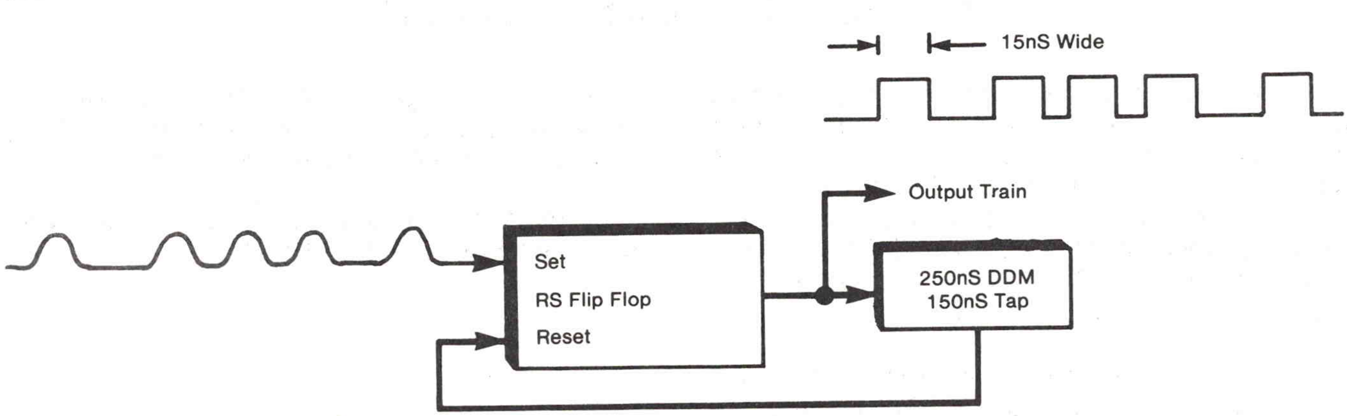

Figure 3

applications. One good example is in PMOS circuits. Here, three clock pulses are required (see Figure 4).

Why delay lines aren't typically used

A delay line is an analog device. All of its parameters, except delay and rise time, may be foreign terms to logic designers. For that matter, delay and rise time are somewhat ambiguous terms. Here are some terms to avoid using when discussing specification of delay modules:

1. Impedance
2. Distortion — pre-shoot, overshoot, ripple, input distortion, output
3. Reflections
4. Attenuation
5. Crosstalk
6. Low pass filter
7. Transmission line
8. Delay-to-rise time ratio
9. Sections

Logic designers deal in functions, drive capabilities, propagation delay, noise immunity, toggle rates, etc. But what do they need to know about digital delay modules (DDMs)?

1. The minimum pulse width they can put in and still get a pulse out. How much and in what direction the pulse width will change.
2. The maximum pulse repetition rate the DDM will handle and why. Namely, the delay will change slightly at first, then, as the PRR is increased, the delay variation will increase. This typically starts at four times the total delay, and increases as the period time decreases.

Another reason delay lines aren't often used involves the fact that their drivers, buffers and terminating resistors often use up a lot of precious board space. Also, delay lines require a circuit to drive a pulse down the line of sufficient voltage to not only trigger all the loads, but to have a good noise immunity margin. The higher the delay line's impedance, the easier it is to drive, because less current is required to drop more voltage through the terminating resistor (see Figure 5, next page). But, the higher the impedance the less likely you can load the line without causing reflections.

Finally, to get an output from the delay line, you must hang a gate or inverter on one or more of the taps. Each gate or inverter (of the high speed family) has an impedance of 2.8KΩ - 2 loads = 1.6K, 4 = 800Ω. And it doesn't take many to really honk up the delay line.

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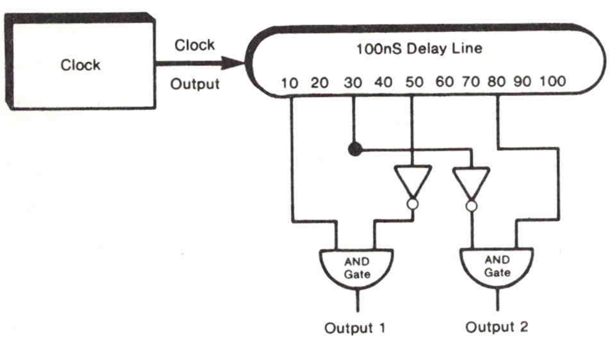

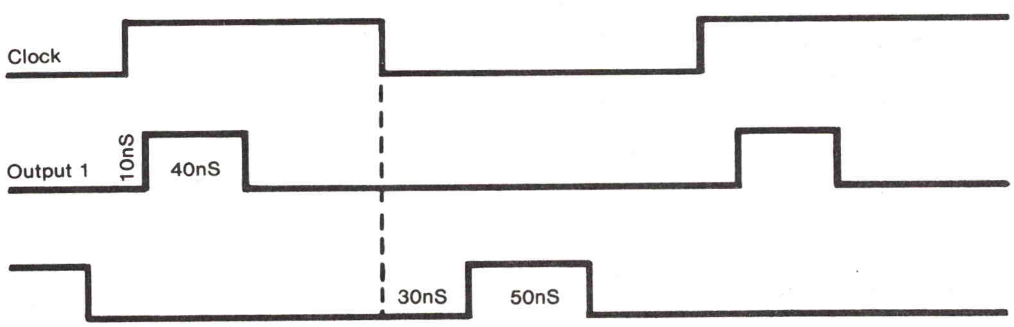

Figure 4

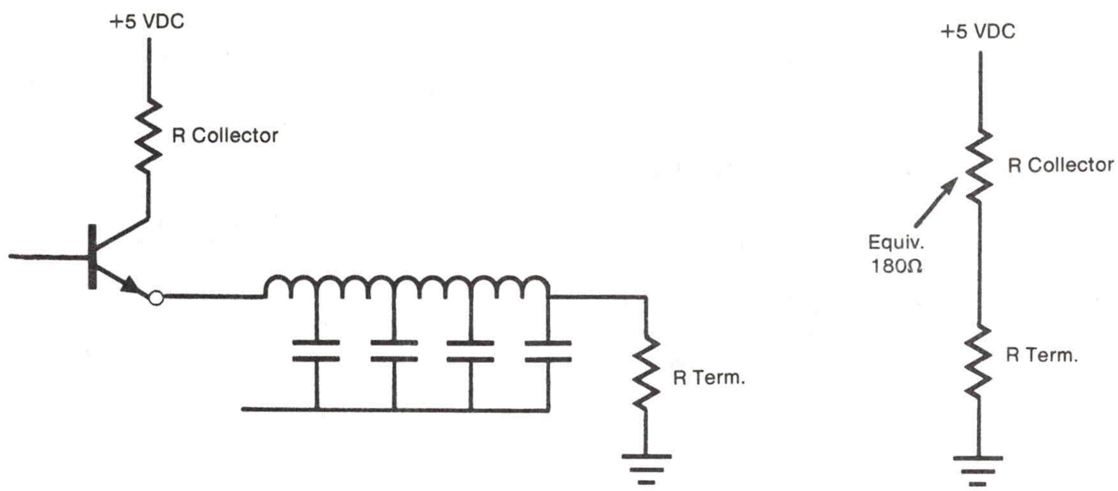

Figure 5

So, as a good rule of thumb, the lower the Z_O of the delay line, the more loads you can put on it. This is just the opposite criteria as that of driving the delay line.

Typically, delay lines of 100 ohms are used, and a discrete driver has to be used to pack enough poop in the line to drive the loads. But, the DDM is a horse of a different color.

Alternate digital delay techniques

Hooking gates in series is by far the simplest, cheapest and most straightforward way to get delay in digital circuits. The only hang-up is accuracy. Gate propagation delays are typically 6nS ± 2nS — a tolerance of 30%. Many applications are not all that critical, so this is what's used.

Family swapping is not too widely used, but is just as functional as hooking gates in series. The same accuracy is to be expected (±30%).

When accuracy is required, many people use one-shots. By adjusting the input capacitor and resistor, precision trimming can be accomplished. One-shots, however, are infamous for their jitter at high duty cycle, which is where the computer field is headed.

This is what leads us into the evaluation of DDMs.

DDM's advantages over the alternatives

To start with, DDMs have a ±5% delay tolerance, and this factor is most appealing. Second, it reproduces what you put into it. This puts DDMs head and shoulders above one-shots, not to mention the higher duty cycle handling capabilities. Further, a DDM has five incremental delay taps and is directly compatible to TTL circuitry. These features make the device unique in the digital market.

How the DDM works

The delay line is a 200 ohm device, not arbitrarily chosen either. 200 ohms is high enough to drive with a high speed hex inverter, and low enough to put five loads on without completely destroying the pulse. There are reflections in the device, but the noise immunity of approximately 0.5V is sufficient to keep them out of the buffers. The delay line is so severely loaded that the design of the line is altered to compensate it. This is why the customer cannot just do the same thing himself, not to mention the fact that the DDM is all in one package.

DDM design criteria

Minimum pulse width — This parameter is directly related to the rise time of the delay line used in the module. When the rise time is equal to the pulse width, this is as low as you can go (see Figure 6, next page).

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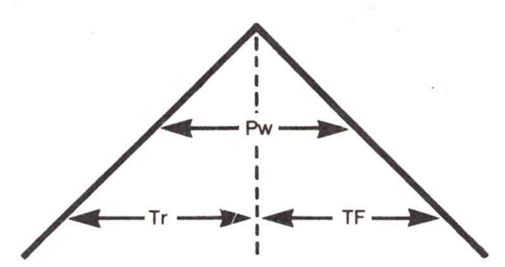

Figure 6

Maximum pulse repetition rate — This is a little harder to define. It is related to the rise time and distortion on the base line. This parameter is improved by increasing the number of sections of the delay line (see Figure 7). The faster the Tr, the less the delay varies due to distortion. Obviously, the less distortion the better.

Recently, engineers have required that the delay be specified from trailing edge to trailing edge, as well as leading edge to leading edge of the pulse. This places additional constraints on pulse width and repetition rate.

For more information

If you have any questions about delay lines or DDMs, please contact me at 78-552, ext. DR-2479.

Byron Witt
Electromechanical Comp. Eng.

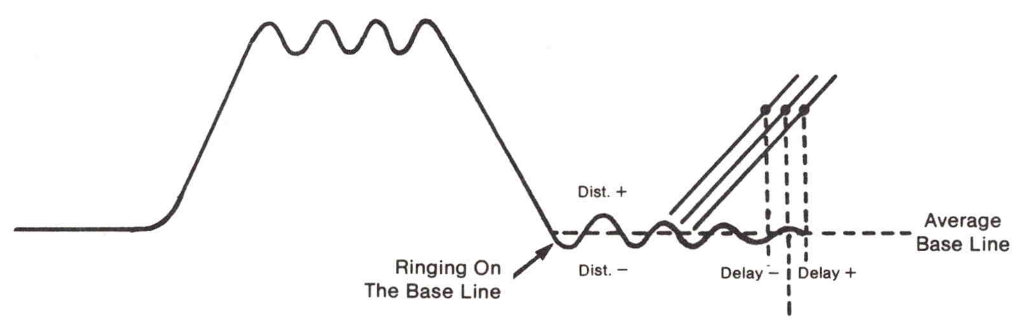

Figure 7

ComponentNewsNewComponents

Vendor	Number	Description	When Available	Tek P/N	Engineer to contact, ext.
		memory and I/O devices			
Electronic Arrays	EA8332A-DC	Masked ROM, 32K, 450nS T_{ACC}, Ceramic	—	062-5549-00	J. McKay, DR-2557
Electronic Arrays	EA8332A-PC	Masked ROM, 32K, 450nS, T_{ACC}, Plastic	—	062-5549-01	J. McKay, DR-2557
		optoelectronic and passive devices			
Bourns	84A1A-B24-J13	Precision Pot, 10 turn WW, 5KΩ±5%; 1W@70°C; ±0.25% independent linearity; B⅜×⅜, S¼×¾FMS, SD slot, w/locating lug, 9 o'clock; lug terminals; ⅝ sq×¾ long	—	311-2158-00	Gene Single, DR-2544
Mallory	TCX	Capacitor, aluminum electrolytic 9000µF, 25V axial lead, 6.6 ARMS ripple current	now	290-0953-00	Don Anderson, DR-2545
Sprague	32D	Capacitor, aluminum electrolytic computer grade, 4300µF, 35V	—	290-0954-00	Don Anderson, DR-2545
TRW	TRW-35	Capacitor, metallized polypropylene, 2.6µF±10%, 200V, 0.8"×1.6", 2.5 ARMS ripple current	now	285-1226-00	Don Anderson, DR-2545

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