Component News AND TECHNOLOGY

Tektronix

Component Information for Tektronix

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Contents

Overview Of PLD/FPGA Programmable Switch Technology

By Norman Adre

The key characteristic of PLDs/FPGAs is the programmable switch which interconnects various logic blocks, routing resources, and I/Os. Currently, there are five types of programmable switch technologies used: fuse-based, pass transistors, multiplexers, floating gate transistors, and antifuse. The properties of these programming technologies such as size, on-resistance, and capacitance, will dictate many of the tradeoffs in an FPGA architecture. Below is an overview of the various programming technologies used.

Fuse-Base

Early PLDs used electrically blown fuses made of various types of materials such as polysilicon, platinum silicide, tungsten-titanium, and nickel-chromium. These early PLDs targeted the simple PLD (SPLD) market because the technology was difficult to manufacture and to program with sufficient reliability for higher density devices. The most common difficulty found was that an inadequately blown fuse can grow back (reconnect) over time. Today, fuse-based SPLDs are in decline. Floating gate transistors are a more reliable and cost effective programmable switch technology for SPLDs. No new programmable logic products are being developed using fuse-based programmable switch technology.

Floating Gate Transistor

The floating gate transistor is the dominant programmable switch technology in SPLDs and complex PLDs (CPLDs). A floating gate transistor is switched on and off by injecting or removing electrons from the floating gate. There are three types of floating gate technologies being used today: EPROM, EEPROM and FLASH. All three can be programmed electrically. The EEPROM and FLASH transistor can be erased electrically, but the EPROM transistor requires ultraviolet light to be erased. Erasable EPROM-based SPLDs/CPLDs are in a windowed ceramic package to allow for erasing. Since the windowed ceramic package is very expensive, one-time programmable (OTP) EPROM PLDs in inexpensive plastic packages are commonly used for production.

Of the three floating gate transistor technologies, EEPROM is the leading programmable switch technology being used in SPLDs/

CPLDs. EPROM technology is declining, and FLASH technology is still in the introduction phase. Only Cypress and Altera (from the acquisition of Intel's PLD line) have FLASH technology in their SPLDs/CPLDs. However, Cypress has indicated they are switching future PLD technology to EEPROM. Xilinx has plans to use FLASH technology in their future CPLDs.

SRAM Technology — Pass Transistors and Multiplexers

The programmable switch technology used in SRAM based PLDs/FPGAs are either pass transistors or multiplexers. In a pass transistor, the SRAM cell determines the closing and opening of the pass transistor. Currently, Xilinx's XC2000, XC3000, XC4000 and XC5200 families; Altera's FLEX 8K and 10K; and AT&T's ORCA series of FPGAs all use pass transistors as a programmable switch.

In a multiplexer, the SRAM cells, which are tied to the select lines, determine which of the mux inputs are to be connected to the output. FPGAs using a mux as a programmable switch typically have fine-grained architectures — i.e. small logic blocks. In addition, they offer faster reconfiguration times, and support complete and partial reconfiguration. Atmel's AT6000 series of FPGAs uses a multiplexer as a programmable switch, and it seems from preliminary information that Xilinx's XC6000 family utilizes a mux.

Since SRAM cells are volatile, SRAM based FPGAs must be loaded and configured at the time the chip is powered up. The configuration data is typically stored in an external non-volatile memory — usually a PROM (often serial PROMs), EPROM, EEPROM or even a magnetic disk. Various FPGA vendors offer various configuration modes — see their data books for more information.

SRAM based FPGAs will continue to be the dominant programming switch technology in FPGAs, and, in some cases, will be the driving technology in sub-micron processes. The major advantage of using SRAM based FPGA is its reprogrammability which provides for rapid prototyping of designs. Also, reconfigurable hardware applications are becoming more and more popular with SRAM based FPGAs. Another advantage of using SRAM based FPGA is that it uses standard CMOS processes unlike other programming switch technologies which require additional masked steps.

Antifuse Technology

An antifuse is defined as an electrically programmable two terminal device which takes up a small area and exhibits low parasitic resistance and capacitance. When a high voltage is applied across its terminals the antifuse will "blow" and create a permanent low resistance link. Antifuses are built using either an oxygen-nitrogen-oxygen (ONO) dielectric between N+ diffusion and poly-silicon; or an amorphous silicon between metal layers or between polysilicon and the first layer of metal.

The advantage of using an antifuse is the small area it takes up. Antifuse FPGAs typically have fine-grained logic blocks which require a considerable amount of routing resources to be used efficiently. Hence, most fine-grained FPGAs have an abundance of antifuses. Often antifuse FPGA vendors tout the routability of their FPGAs compared to pass transistor type FPGAs. The antifuse FPGA does lose some chip area because it needs on-chip high voltage programming

circuits. These circuits reside on the chip's edges and do not restrict the interconnect density achievable on the rest of the chip. As processes scale to smaller feature sizes and allow for higher gate capacities, the relative area occupied by the high voltage circuits decreases. Another advantage antifuse has over pass transistor type FPGAs is its low "on" resistance and parasitic capacitance, which reduce RC delays. In addition, antifuses are normally off devices; only those antifuses that are needed are programmed (in a typical application about 2% of the antifuses are programmed).

Currently, there are three suppliers of antifuse FPGAs: Actel, QuickLogic (with Cypress as foundry and second source), and Xilinx. Actel's first generation antifuse technology, called PLICE (programmable low impedance circuit element), utilizes ONO dielectric between N+ diffusion and poly-silicon. Applying a sufficient voltage across the dielectric will cause it to break down, and create a low resistance (typ. 500Ω) connection. However, the PLICE technology adds three mask steps to a conventional double layer metal (DLM) CMOS process.

Although the amorphous silicon antifuse has been around for a long time, it has not been considered in the past as an FPGA programmable switch due to some difficulties with the technology. First, applying a reverse current across a programmed antifuse can return the amorphous silicon back to its nonconductive state. Second, an unprogrammed antifuse can pass a small but significant current — i.e. leakage current, and hence, will increase the power consumption of a part. Also, an amorphous silicon antifuse cannot have active transistors beneath them, and therefore, are only used in channeled architectures (unless triple layer metal is used).

However, several companies have overcome these difficulties. QuickLogic was the first FPGA company to use an antifuse consisting of an amorphous silicon sandwiched between metal layers. Their antifuse, called ViaLink, is no bigger than a standard metal interconnect, and can be packed very densely. Once programmed, the ViaLink connects the metal layers. The connection provides less than 50Ω resistance, and very low capacitance. This approach provides the least amount of loading compared to other programmable switch technologies. Also, Xilinx recently entered the antifuse FPGA arena with their XC8100 family. Xilinx's antifuse, called MicroVia, will consist of an amorphous silicon sandwiched between metal layers.

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From The Editor

By Peggy Butler

Welcome to Component News!

It is with much excitement that I begin working with *Component News & Technology*. For the last 11 years, I have been an engineering documentation writer for Component & Supplier Information group. I want to thank Dave Bartles for all of his help with the July issue. He has made the transition a pleasure.

In 1989, the Component Engineering group revived the *CN&T Newsletter* after being out of publication for ten years. I have watched it develop into a top publication. Beginning with this issue, all employees of Tektronix will be able to access *CN&T Interactive* through the World Wide Web. The URL is:

`http://www.cse.tek.com/CSI/NEWS/cn.html`

Component News & Technology is published six times a year by the CSI group. You are invited to submit your articles about commodity and component technologies and issues. If you feel you have information that could be helpful, please write about it. This publication is available for you to communicate design problems/solutions, new product information, and application notes. Through Reader Service Information, you may suggests topics of future articles, request copies of past articles, offer comments or suggestions, or be added to the mailing list. Please take advantage of these services.

The editor and the Component & Supplier Information group have tried to assure accuracy in the published material. We are not responsible for any errors or consequences of any errors in this publication. If you do find an error or an omission, please contact the editor.

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It's A Whole New Northcon

By Cliff Webb, Northcon Director

Northcon returns to Portland over the dates of October 10 -12, 1995. It is the Northwest's largest electronics event for design, test, manufacturing engineers and purchasing professionals. Northcon/95 will feature over 300 exhibits and live product demonstrations from suppliers of components, test and measurement equipment, production supplies and equipment, contract manufacturers, EDA tools and engineering software.

New in '95

IEEE proudly announces the first IEEE Technical Applications Conference to debut at Northcon/95. Topics covered include:

- A survey of test methods for embedded systems
- Design manufacturing engineering
- Surface mount manufacturing — issues and trends

- The future of the PC (views from Intel)
- Windows '95 preview
- Neural network application studies
- Data acquisition & optical sensors

Exhibits, Demonstrations, Workshops, Talks

- Special exhibit featuring hands-on demonstrations of the latest in PictureTel Video Conferencing
- Live Internet exhibit presented by Oneworld Internetworking and ACER America
- Special Windows '95 sessions and hands-on demonstrations
- A special purchasing workshop will discuss:
  - Getting started in true supplier partnerships
  - JIT: how to get started
  - Procurement cards: successes and failures
  - Cases of strategic supplier alliances to leverage continuous improvement
  - Supplier development and improvement
- Special Keynote Breakfast: *The Internet Challenge: Today's Evolution — Tomorrow's Revolution*

And There's More

Remember, Northcon is in Portland only once every two years. Mark Your Calendar Now!

Northcon '95

Oregon Convention Center

Exhibit Hours
Tuesday, October 10, *11 am – 8 pm (late night exhibit hours)
Wednesday, October 11, 9 am – 5 pm
Thursday, October 12, 9 am – 4 pm

Conference Hours
Tuesday, October 10, *9 am – 5:30 pm
Wednesday, October 11, 9 am – 5 pm
Thursday, October 12, 9 am – 5 pm

*Keynote Breakfast begins at 8:30 am

For complimentary registration and complete information on Northcon/95:

CALL:
Northcon Business Office
(800) 877–2668 ext.218

FAX:
(310) 641–5117
Include your name, title, complete mailing address, phone, fax, email address.

EMAIL:
northcon@ieee.org
Include your name, company, title, complete mailing address, phone, fax, email address.

ELECTRONICALLY:
`http://www.northcon.org/`

There will be some Northcon literature and complimentary previews available at Tektronix, in the CSI databook library located in the northwest corner of building 47, level 1.

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RF Preferred Supplier List

By Martin Baggs

I have been working with the RF Design Engineering and Component Engineering groups over the last few months on a project to compile a list of preferred RF suppliers. Ideally, this list will provide clear direction toward suppliers to consider first when we need to obtain new RF components.

Currently, most of the engineers in the two groups have given input to a proposed "straw man" version of the list. I will collate this input and organize a meeting to review the updated list. At this meeting, we will identify any final changes and then approve publication of this finalized supplier list. I expect this process to be completed by the end of October.

The final supplier list will be broken out by component category type, e.g. RF relays, RF transistors, RF filters, RF mixers, RFICs, etc. For each category we will identify the top two suppliers. It will thus prove beneficial to Tektronix engineering groups, and should focus our design activities with fewer suppliers. In addition, we are looking for additional components to add to the Preferred Parts List which are recognized as good candidates for reuse in future designs.

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Last Time Buys On The Web

By Merle Vanderzanden

For a list of all Last Time Buy part numbers, refer to a new web page from CSI (Component Supplier Information.) It is located at:

`http://www.cse.tek.com/CSI/NEWS/last_buy.html`

This list will have the Tek part number, supplier information, last buy and last ship dates, as well as the component engineer. It will show the parts that have a last time buy date still open. This list will be updated weekly if needed. It is available for local viewing (within Tektronix) only.

Check it out! If you have questions or suggestions for improvement, let me know.

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BBO Design Guidelines

By Ron Boyce

It is the policy of the Tektronix Board Build Operation (BBO) to provide products and services that consistently meet or exceed the total expectations of our customers.

— BBO Quality Policy

Our Quality Policy is a commitment that BBO takes very seriously. As a result, we look very carefully at the information our customers expect us to deliver. A key expectation is the delivery of information to guide the design effort toward a product that can be assembled in an efficient, cost effective, and high quality process. For example, defining the acceptable component spacing allows BBO to assemble the product with accurate, efficient, and low cost automated placement. BBO publishes a Design Guidelines document to deliver this information to the customer.

In order to maintain the Design Guidelines and provide our customers with the very best information, BBO is assembling an update to the document. The revised Design Guidelines will have a new name, *The BBO Design for Manufacturability Handbook*, or simply *BBO DFM*. Our approach to this revision is to give priority to an update of the most critical sections, surface mount technology, and depaneling. Areas with major revisions will be spacing requirements and depaneling techniques. These sections will be published in an update issued in the September-October time frame.

Information from all areas of BBO process engineering will be collected and assembled to create a document that meets the designers needs. I will be the person facilitating the collation of this information and act as a representative to our customers, the design community. I will also ensure the BBO DFM continues to stay up-to-date by initiating BBO updates and responding to requests from the design community.

The document will be in a revised format, as suggested by review and comments from representative members of the design community. The new organization provides the user with a logical, easy to use assembly of the design information. Our intention is to furnish designers with a good, user friendly tool to use in their daily activities.

Chapter one familiarizes the user with BBO, then describes the New Product Introduction (NPI) process, and defines the criteria for electronic data exchange. Chapter two discusses the board assembly architectures available and a selection process that will guide the designer to the best panel layout and technology level to achieve the product objectives. The depaneling section will also be clarified at this point. This is an area that is often neglected as a process step, but is highly critical to the production and delivery of a high quality, mechanically good product. Chapter three, the surface mount update, will address the critical technologies used in high performance electronic products.

In this issue of *Component News & Technology*, Ron Stanley outlines the depaneling philosophy that will set the direction for the BBO DFM. Please read his article and direct comments to me.

This direction for the update will address the most critical design issue first. Subsequent updates, planned during the next six to eight months, will complete the update of all portions of the BBO DFM. When this is

complete, all sections will be current. A continuous process of review and revision will follow to maintain this tool in an up-to-date condition.

The BBO DFM will be available on WorldView as well as hard copy. This will facilitate the process of providing up-to-date information to the designers.

The BBO DFM is viewed as a living document that we will constantly be updating and reviewing as needed. We invite our customers to initiate review and revision of areas they feel need attention. A key element in achieving our Quality Policy objective is to provide our customers with design information that will result in an easily manufactured, cost effective and high quality product.

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CADIS 3.0 Changes

By Wilton Hart

We are about to release an updated version of CADIS, our parametric search tool. Many of you have been using the tool for about nine months now. (If you need help getting access to CADIS please call Diane Argyle at 627–2533).

The new version of the program will be called CADIS 3.0. This is the first major revision to the program and it contains a number of Tek requested changes.

Here is a list of the changes and a description of each one. Some of the changes affect only the database editing screens, but they are listed here for completeness.

Starting Class

The current software requires you to pick the attributes that you want to display every time the program is started. The new version uses a default of all the root attributes. This should make the error notice "Display order must be set to use this command" a thing of the past.

Part Compare

A new header line contains "File Actions Options." Part Compare is found under Actions.

To compare parts, you must choose two parts in the display screen. Click on the line number at the left for the first part and then push shift and click on the second part. Pull down "Actions" and choose "Part Compare." The display will show the attributes of the parts side by side. If you then choose compare, the attributes which are the same will appear in green and the ones that are different will appear in red.

The "Close" button that was at the bottom of the screen is now under the "File" pull down.

Find Class

Find Class allows you to go directly to a class when you do not

know where it is located. This is very useful when trying to find where something is listed in the database.

This little-known feature first appeared in the last interim release. Use the "Find" pull down at the top of the screen. A stick up box lets you type in a class name. If you are not sure of the class name, choose a word and put * on each side. This will match any class name of the word you type. If the first occurrence was not the one you wanted, use Find Next to look at the next occurrence.

Concurrency

Today, we have two versions of the CADIS database running. CADIS does not allow concurrent edit and retrieve on the same database. With the new version, you can lock a portion of the tree while editing it. If someone tries to retrieve in that part of the tree, they will receive a message that it is locked and they will have to come back later.

Set Starting Class

The new version of CADIS will allow you to pick a class to open during startup. This is handy because if you only use digital logic you can set your startup there and not have to click through the upper classes each time you open the database. Starting Class is found under the "Options" pull down at the top of the screen. It chooses the current class as the startup class for next start.

Attribute Display

A new function under the "Options" pull down allows you to choose or hide root attributes. This is used if there are some attributes which you do not want to see. You can hide one or all of the root attributes so that the space can be used for parameter display.

Solaris Support

Version 3.0 supports Solaris clients. This means that groups who have updated their Unix operating systems to Solaris will be able to use CADIS. In the past this has not been the case.

Other Changes

CADIS, CEDB and the Parts Data Warehouse are now linked. Parametric data can now be found in the Oracle database (PDW) as well as CADIS.

A cleanup effort is under way in CADIS to make it more user friendly. We are rearranging some of the tree structure and eliminating duplicate parametric fields. If you have additional recommendations please contact Curt Bernal 627–6103, Gary Johnson 627–1985, or Wilton Hart 627–3035.

Future

We are working on linking the New Part Request system with CADIS so when someone does a search and does not find a part, they can automatically launch a request for a new part. This feature is planned for release in Q2.

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Convergence Technologies

By Martin Baggs

The world of telecommunications is rapidly changing. The digital revolution is here — or almost! Video-on-demand, video-to-the-desktop, personal communication services (PCS), multimedia, and the Internet have appeared on the scene and will change the way we work and play. To make an impact in this evolving arena, Tektronix must understand these technologies and their interaction.

Recently a "Convergence Seminar" was held within MBD sponsored by Brian Boso, VP of Technology. It was a broad overview for a diverse audience (including engineers, buyers, managers, etc.). Formally titled *Understanding Emerging Technologies in 1995*, Robert Calkins of Telecommunications Research Associates presented this three-day seminar. He discussed the convergence of the computing, video and telecommunications technologies. The topics addressed included:

- Advanced intelligent networks and signalling systems
- Personal communications service
- Video and multimedia, cable TV, wireless cable and competitive access
- Sonet/SDH (Synchronous Digital Hierarchy)
- Internet and TCP/IP
- Frame relay
- Asynchronous Transfer Mode (ATM)
- Switched Multimegabit Data Services (SMDS)
- Fiber Distributed Data Interface (FDDI)
- Wireless data
- Metropolitan-Area, Native mode LAN interconnect services

A valuable resource given to each attendee was a course notebook. This includes copies of all the slides that Bob Calkins used, and serves as a useful reference tool. Especially beneficial in this regard is its 130 page glossary of terms and acronyms. (To see just how valuable, take the following test and try defining these acronyms: 1) ADM; 2)CDMA; 3)FITL; 4)MPEG; 5) STS; 6) TCP/IP. The answers are given on page 12.)

To further our understanding of convergence technologies, a number of approaches are being taken in MBD. Arif Kareem will publish a bi-monthly newsletter, entitled appropriately, *Convergence Newsletter*. The goal of this newsletter is to inform MBD employees about the industry, customers, and competitors. Brian Boso is organizing an ongoing series of seminars at a more technical level. And, at the senior management level, Dan Terpack hosts a quarterly review of convergence technology for his staff.

For more information, or to see a copy of *Understanding Emerging Technologies in 1995*, contact me directly.

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Board Build Operation's Preferred Depaneling Method: NC Router

By Ron Stanley

BBO's method for board depaneling is the numerically controlled router. The router provides a rapid, reliable method of removing images from the panel. We recommend board scoring only on panels which can significantly benefit from high board utilization (typically panels with more than 30 images). Board scoring is considered on panels of 12 images or less only when at least one more image can be added because of the better board utilization.

Why not use board scoring on everything?

Board scoring has some unique advantages. A scored board can have a higher panel utilization due to the elimination of the 0.125″ routing paths between images. The elimination of the routing paths can also prevent flooding of boards which go through the wave solder process. Scoring allows images to be separated from the panel without the use of tools, by any operator, anywhere in the board build process. Unfortunately this is also its biggest disadvantage.

Scored boards are not as strong as conventional route-tab boards. Depending on board weight, web thickness, and scoring pattern the boards may break prematurely. In order to obtain a panel that is durable enough to survive the multiple processes and handling steps required, the score pattern must be changed or the web thickness increased.

If the web thickness is increased, the difficulty of depaneling is increased, requiring more force on the panel to bend and break the web. This bending stress is transferred to the parts as the board is flexed. The increased web thickness is particularly difficult to handle with very small images because of the reduced leverage.

Modifying the score pattern of the panel so that the score lines do not extend out to the edge is another way to decrease the likelihood of premature depaneling (for details see page 7 — *BBO Guidelines*.) Changing this feature eliminates the greatest benefit of board scoring — the ability to depanel without tools. When the score lines do not extend to the edge of the panel, the first step of depaneling is to use a shear to cut across two edges of the panel. Then, the operator can finish depaneling the board by breaking the scored area.

While there are several advantages to board scoring, it has proven reliable in only a limited number of cases. Until we experience better yields with board scoring, the NC Router will continue to be our preference.

NC Router vs. Board Scoring

The NC Router has several advantages over board scoring. With conventional tabs which are routed there is almost no possibility of premature depaneling. Router depaneled boards are not subjected to bending stresses during depaneling. Routed boards do not require our operators to apply force to the panels for depaneling (no risk of repetitive motion injuries.)

Disadvantages to the router are a limited capacity, slightly slower process, and dedicated resources for programming and maintenance.

What research are we doing to make scoring more feasible?

Board scoring is definitely a process that BBO wants to support in the future. To accomplish this we are working on several things:

- The investigation of a board scoring cutter to assist in the separation of very small scored boards.
- Continued work with Merix to help them control web thickness.
- More research on what web thickness is appropriate for different weights and thickness of boards.

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Answers to the Acronym Test (Page 10) — Convergence Technologies

1) ADM — Add/Drop Multiplexer
2) CDMA — Code Division Multiple Access
3) FITL — Fiber In The Loop
4) MPEG — Moving Picture Experts Group
5) STS — Synchronous Transport Signal
6) TCP/IP — Transmission Control Protocol/Internet Protocol

(Full definitions of these acronyms are given in the course book glossary.)

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Moving On-line

By Dave Bartles

As mentioned in the last issue of *Component News*, CSI has been working to make many of our current information resources and tools available through the World Wide Web. We are pleased to announce that the September issue of *Component News* will be available both in hardcopy and on the World Wide Web through the CSI web pages. The CSI web pages are accessible to all employees of Tektronix. You may view the CSI web pages by pointing your WWW (World Wide Web) browser to:

`http://www.cse.tek.com/CSI/index.html`

We are putting our services online in an effort to bring you the information you need to make informed and timely decisions about components for your designs. This new method of distributing commodity and component information provides a common cross-platform interface that will allow you to eventually launch databases and access tools that now require multiple passwords and interfaces.

The Framework

These pages are and will be under perpetual change and revision. We are starting with a basic structure which is composed of the following sections with an indicator of the current status of the section: "active" means the section has content now, "stub" means no content at this time.

- *NEWS* (active)
  (includes *Component News*, Last Time Buy Notices, and Component Alerts). This issue of CN is on the web now.
- *How To . . .* (active)
  (includes information on how to use, find or receive various CSI tools)
- *Preferred Part List* (stub)
  (will include the current version of the corporate Preferred Part List)
- *Databases and Tools* (stub)
  (will include eight tools and databases CSI currently supports)
- *Material Acquisition Plans* (active)
  (includes 4 of the 13 Corporate Material Acquisition Plans)
- *Corporate Mod Numbers* (stub)
  (will include information on how to pick up, search and update a Corporate Mod Number)
- *Staffing and Contacts* (active)
  (roster of CSI personnel — function and contact information)

A Dynamic Tool

We are working to fill in the other sections and we will announce new additions and changes to the pages as needed. As we continue to build these web pages, we will be looking to you for feedback on whether or not you find the information useful. This information, just like the information in *Component News,* is considered **Company Confidential.**

The Transition From Hardcopy

Although we consider use of web pages to be a major breakthrough in the information technology business here at Tek, we are still using hardcopy tools in the midst of this transition — this issue of *Component News* for example. In addition, if you need hardcopy of the web pages you find, you can print the page you are viewing directly from the WWW browser in a menu command. Because there are a number of different WWW browsers available and the print selections vary, please consult your system administrator if you are unfamiliar with this function.

For comments or more information, please contact:

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Component Engineering Commodity Support List

By Julie Vincent

The liaison support activities for the Component Engineers have been adjusted to better match the current organizational structure of the IBDs and their project plans for FY96. We are continuing our assignment of at least two Component Engineers to cover each IBD to better meet our customers requirements and provide faster response. Each of the Component Engineers are prepared to coordinate the appropriate resources to answer your questions.

Examples of the specific type of activities for Component Engineers:

IBD Liaison Activities

- Participation with Engineering Project Teams
- Take part in early Design Reviews

- ❖ Assist with Bill of Material Reviews to resolve issues with high risk parts
- ❖ Part and vendor reduction projects
- ❖ Design consulting

Commodity Coverage Activities

- ❖ Generation and maintenance of Preferred Part List
- ❖ Coordination of component strategies
- ❖ Review of new technologies
- ❖ Coordination of part evaluations
- ❖ Assistance with part selection
- ❖ Provide computer tools for easy access to part data

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VND				
VND — Oregon	Abe Ghahyasi	627-2567	abeg@mdhost.cse.tek.com	Memory/Hybrids
	Norm Adre	627-2524	normana@mdhost.cse.tek.com	Logic/Digital
	John Young	627-2165	johny@mdhost.cse.tek.com	Interconnects
Lightworks	TBD			
VND — GVG	Gary Johnson	627-1985	garyjo@mdhost.cse.tek.com	ASICs, Flat Panel Displays, Crystals
	John Young	627-2165	johny@mdhost.cse.tek.com	Interconnects

TBD = Level of support to be determined

For questions, comments or more information, please contact:

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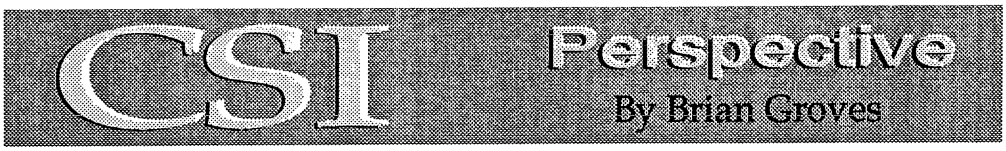

CSI Perspective – Combining Forces With Supply Base Management

Effective August 1, Component and Supplier Information has been merged with the Supply Base Management group. This is very exciting news with regard to our strategic focus on Preferred Parts and Suppliers. For two years, both groups have been working on two parts of the same equation. The SBM group has been focused on Preferred Supplier programs and initiatives. CSI has focused on Preferred Part usage, as well as tools for part information. By combining the two groups, we will capitalize on the combined energies and talents of both groups. Both groups now fall under the heading of Corporate Materials and report to Bob Drennan. My role shifts to one of transitioning the CSI organization and the major programs over to Bob. I have been part of this organization for almost five years now, and I am looking forward to a new position within VND. I feel very good about the results that we all have accomplished over the last five years.

Tek now has a world class Preferred Part program, with a variety of tools and processes in place to access and maintain the part information. The design engineering community has really adopted the Preferred Part model, with monthly BOM (Bill of Material) averages running at over 65% preferred. Over the next year, you can expect to see an increased focus on improving access to part information. We still have work to do with regard to fine tuning some of our tools, especially around performance. You can also expect to see an increased focus in placing more control around Preferred Part selection and maintenance within the divisions. Now that Tek is positioned for growth, it is important for CSI to assist the division with less emphasis on part reduction and process control and more directly on improving time to market for new products.

I would like to thank all of you who have helped make the last five years not only enjoyable, but very successful. I will remain active in the background for the next year, and would be glad to answer any questions. Thanks for listening!

For questions, comments or more information, please contact:

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Preferred Suppliers And Preferred Supplier Candidates

By Peggy Lewis

This is the most current list of Preferred Suppliers and Preferred Supplier Candidates from Supply Base Management. Shown in the list along with the supplier name is a code indicating the current status of the supplier and the Supply Base Manager's name for each commodity.

Legend:

SBM Supply Base Manager
C Candidate
P Preferred

Plastics:

SBM Harry Anderton
C Kaso Plastics Inc.
C Polycast Inc.
C Triquest Precision Plastic
C Vision

Sheet Metal:

SBM Harry Anderton
P Accra-Fab
P Delta Eng & Mfg
P Neilson Mfg
P Triax Metal Products
C Serra
C Gerome Mfg Inc.

Machined Parts:

SBM Harry Anderton
P EMI Precision, Inc.
C Beaverton Parts, Inc.
C Lite Specialty Mfg
C Davis Tool Inc.

Screw Machine Parts:

SBM Harry Anderton
C Revtek, Inc.
C Universal Precision, Inc.
C Enoch

Die Cast Parts:

SBM Harry Anderton
C TVT Die Casting
C SKS Die Casting

Fourslide Parts:

SBM Harry Anderton
P Northwest Fourslide

Rotary Controls:

SBM Harry Anderton
C Bourns

Power Conversion Products:

SBM John Shoberg
C Ault
C Coilcraft/Deyoung
C Computer Products
C Delta
C Zman
C Zytec
C Power One

Elastomeric Keypads:

SBM Harry Anderton
P CRT

Packaging:

SBM Harry Anderton
C Packaging Resources

Printed Materials:

SBM Bill Florine
C Xerox

Optical Components:

SBM Larry Hiatt

Optical Connectors:

SBM Larry Hiatt
C Rifocs

Optical Component Packaging:

SBM Larry Hiatt
C Photonic Packaging Co.

Discrete Lasers:

SBM Larry Hiatt
C NEC
C OKI

Discrete Detectors:

SBM Larry Hiatt
C NEC
C Photonic Packaging

Optical Modules: (Transmitters & Receivers)

SBM Larry Hiatt
C AT&T
C OKI

WDMs/Couplers:

SBM Larry Hiatt

C AOFR (ADC)
C Gould

Optical Fiber:

SBM Larry Hiatt

C Corning

Memory Components:

SBM Peggy Lewis

DRAMs/VRAMS:

SBM Peggy Lewis

P Toshiba
C NEC
C Samsung
C T.I. (VRAMs only)

EPROMs/FLASH:

SBM Peggy Lewis

C AMD
C Cypress (PROMs only)
C Intel
C Xicor (EEPROM only)

SRAMs:

SBM Peggy Lewis

P Dallas Semi (BB SRAMs)
P Toshiba
C Cypress
C NEC
C Samsung
C T.I. (FIFOs only)

MROMs:

SBM Peggy Lewis

C Samsung
C Toshiba

ASICs:

SBM Paul ten Zeldam

C Maxim
C National
C NEC
C US2

Peripheral Products:

SBM John Shoberg

C Seagate
C NMB (Keyboards)

Connectors:

SBM Bill Florine

(Complete connectors table on next page)

Connector Supplier Matrix

	Board to Board									Sockets							I/O				Power				
	Headers	Receptacles	<0.050	Backplane	Edgecard	Stacking	Elastomer	Screw Machine Typ	Hi Rel Contact	Screw Machine	Stamped	ZIF	SIMM	PCMCIA	Lamp Sockets	CRT Sockets	Trapazoidal	Circular	Jacks & Plugs	Audio, Circular	IEC Conn Modls	Terminal Blocks	.156 Center Conn.	Other Rectnglr Disc	Circular
3M Company	1	1		L		X					L	X	L				L						X		
A/D Electronics																			2	X					2
AMP	2	2	2	1	1	1	1	1	1	1	1	1	1	1			1	1					2	1	
Berg Electronics	3	3		2	X						L		L	X										L	
ETI							2																		
Feller-Neumeyer																					2				
Fox Conn	X															2	X								
JST (Japan Solderless)	X		3	L												3	2								
McKenzie Tech	L							2		2	L														
Molex Products	X		1	L	L						X		1	L			L	X					1	2	
Mueller																			1						
Neutrik																		X	X	1					
Phoenix Co.																						1			
Samtec	3				L	L	3	3		X	L														
Schurter																					1				
Singatron																		X	1	X					1
SMK																1									
Triquest																1									
Viking Electronics	L		L	2							L						X								
Virginia Panel			3																						

Legend: 1, 2, or 3 = Preferred Supplier Candidates and their relative ranking for potential new business.
X = Fully capable in this technology L = Limited capability in this technology

For questions, comments or more information, please contact:

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