M 82

PRODUCT PROPOSAL

(INTEGRATED CIRCUIT)

A SINGLE-CHIP MICROPOWER DVM WITH COMPUTING CAPABILITIES

Summary

This note outlines the design for an integrated analog-to-digital convertor (DVM) of wide applicability, primarily for use in conjunction with the 7000-series readout. Because of its small size (60 X 90 mils die in a 20-pin plastic package), low power drain (less than 240 mw from the standard plug-in supplies) and anticipated low cost, it should find use in situations where a DVM (or other special-purpose A-D convertor) would normally be out of the question.

The system features: one, two, three or four decimal digits; automatic polarity; automatic overrange; differential inputs for both signal and reference voltage inputs; electronic control of scaling factor (proportional and inverse); internal reference voltage availability. Easily added are: leading-zero suppression; last-digit round-off; 4-digit overflow indication; automatic ranging.

Barrie Gilbert

March 24, 1970

INTRODUCTION

There are a growing number of applications for an inexpensive analog-to-digital convertor of modest accuracy able to interface directly with a 7000-series mainframe or other display devices.

Included are:

1. Spectrum-analyzer applications (center-frequency readout, scan-width, attenuation, etc)
2. Distance-in-dieletric readout (TDR's, e.g. 7S12)
3. Voltage or current offset (7A11, 7A12, 7A13, 7A14, 7A22, etc.)
4. Delay-time readout (7B51, 7B52, 7B71, etc.)
5. Temperature readout (Miniscope)
6. Power-supply readout (I.C. tester, ITS plug-ins)

This list will grow rapidly once a sufficiently cheap convertor becomes available.

In addition to applications involving measurement of an unknown quantity against a known reference, there are applications for a ratiometer (quotient computation), or product meter -- for example, in the measurement of power. These, and other functions, can be performed by the circuit described.

GENERAL SYSTEM

The proposed 60 X 90 mil chip will actually consist of two sub-systems: one, the M59 (four-decade counter with buffer-storage) already designed and well-developed. This consumes 60 X 60 mils. The second sub-system, the primary subject of this note, uses the remaining 30 X 60 mils and contains what is essentially a voltage-to-count convertor. The two secions can be processed independently, to advantage, since the M59 has several other

uses and the convertor is designed to also be compatible with T^2L logic should it be desirable to use this.

The two sub-systems are interconnected by second-level metal, to avoid the need to produce a single large-area metallization pattern and to achieve the necessary crossovers. (Fig. 1) Approximately 150 circuits fit on a standard wafer. Anticipated yield is 20-30%.

It should be noted that the relatively few pin connections required are largely a consequence of using time-multiplexed analog data-coding. However, this data can be readily decoded by an M19 (analog-to-decimal decoder) which can drive thermionic display tubes, such as the "Digivac" tubes; appropriate time-sharing of the anodes is easily provided. Alternatively, by omitting the buried layer under the output transistors on the M19, this circuit could drive Nixie-tubes directly.

Other uses of this system, particularly in the two-chip form (which provides slightly better versatility in two 16-pin packages) will occur to the reader, for example, as a precision 4-digit comparator or hybrid analog/digital signal-processor. The four parallel analog outputs, available in the two-chip form, can directly drive moving-coil meters; thus, a further possibility is a portable 4-digit DVM operating on a power drain of 5 V at about 25 mA and 30 V at about 3.4 mA.

ADVANTAGES OF LOW-POWER OPERATION

Considerable effort is being spent to reduce the current requirements to an absolute minimum, limited by the present technology. The reasons, apart from the obvious desirability of reduced power expenditure, are:

1. Small temperature rise and trans-chip thermal gradients improve voltage offsets and drift performance.

2. Minimum-geometry devices can be used, so reducing chip area.
3. Metallization for the +15 V and -15 V supplies (used in the analog-to-digital convertor section to maintain a large common-mode range) is eliminated, since the small currents used can be supplied via the isolation diffusion (-15 V) and a buried-layer power-buss (+15 V). This permits further area-reduction.
4. The entire input convertor can be operated from a floating power supply of 30 V, to permit a true differential input mode with, say, ±500 V CMR.

OPERATION OF THE CONVERTOR

Of the multitude of methods available for analog-to-digital conversion, the antiquated "ramp" method was chosen, but some modernization has been applied. An historical objection to this method is that it requires careful control of the clock-frequency and the ramp rate. Consequently is it not uncommon to find crystal oscillators used. However, the method proposed here requires only that two capacitors and two currents track over the temperature range. Further, the dependence on these components can be put to good use, since it permits the readout to be scaled either by switching capacitors or changing currents.

Another objection to the "ramp" method is that it is sensitive to short spikes and disturbances on the signal. Whilst true, this objection is less serious in those cases where the signal is from a well-controlled, internal source, as will generally be the case in the major applications.

An advantage of the method is its superb simplicity: a ramp runs down from about +14 V, intersecting the two signal levels as it goes, and gating a count burst between these levels. At -14 V the ramp triggers a

circuit to return it to the upper level, and simultaneously causes a "TRANSFER" pulse to be generated, which puts the accumulated count into the buffer store. On the way back up, further counts are accumulated, but these are of no consequence because the arrival of the ramp back at +14 V causes a "RESET" pulse to be delivered to the counter*. (Fig. 2) Polarity indication is simply a matter of detecting which intersection occurs first.

A further advantage of the method is that when the counter overflows, the remainder is still valid (until analog overload occurs).

DETAILS OF THE OPERATION

The basic ramp and oscillator method is subject to errors, many of which are avoided by the modifications now described. The signal comparators (which detect the intersection of the ramp and the signal level) are quite accurate, offsets of 1 mV being anticipated over a common-mode range of 25 V. Thus, the reference voltage is also applied (differentially if desired) to an identical pair of comparators, which control the voltage amplitude of a ramp in the clock generator. Now, the total clock interval is determined by the time taken for this ramp to run between the reference levels (a precise interval) plus the time taken to return to the starting level (not precise), and if a precise signal ramp-rate were used, the count would be subject to errors. However, this is avoided by gating the current which generates the signal ramp so that it is on only when the clock ramp is running at the precise rate between reference levels. This is clarified

---

*In order to avoid improper operation of the overflow indicator described later, the count is actually inhibited during the return of the signal ramp, so the counter contents never exceed the numerical equivalent of the input.

by Fig. 3. Each time the clock ramp runs between V_3 and V_4 at a rate I_2/C_2, the signal ramp increments down a small step, the size of which is $I_1\tau/C_1$, where $\tau = (V_3-V_4)\ C_2/I_2$. To run between the signal levels V_1 and V_2, the clock ramp must run down $(V_1-V_2)\ C_1I_2/(V_3-V_4)\ I_1C_2$ times, and this is the number generated by the clock gate. (Details of the circuitry are available on request.) Notice that I_1 and I_2 can be generated by a pair of precision resistors connected to a common voltage source (which voltage need not be precise), or they may be signal inputs. Notice also that automatic polarity indication applies only to the V_1-V_2 input.

ACCURACY AND STABILITY

The accuracy can only be estimated at the present time, and not all of the error-sources can be anticipated. The most serious are:

1. Offset voltages in the comparators (signal and reference) -- approximately ±1 mV in each of the four.
2. Error currents in the timing-capacitors due to base currents in the comparators (approximately -0.5 μA ±0.2 μA, almost insensitive to temperature).
3. Error in the timing-capacitor currents from other sources (e.g. resistor errors) -- approximately ±0.2%.
4. Errors in the timing-capacitor absolute values -- about ±1%.
5. Tracking errors in the capacitors -- about ±0.2% over 20°range.
6. Count-gating errors. (±1 count)

(An apparently missing error-term -- that due to non-linearities in the ramp generators -- is not likely to be significant due to the very high effective resistance of the current generators.)

The combined effect of these errors is to modify the expression for the count to:

$$N = \frac{(V_1-V_2 \pm 2mV \pm 5\mu V/^\circ C)}{(V_3-V_4 \pm 2mV \pm 5\mu V/^\circ C)} \cdot \frac{(C_1 \pm 1\% \pm 0.01\%/^\circ C)}{(C_2 \pm 1\% \pm 0.01\%/^\circ C)} \cdot \frac{I_2 \pm 0.2\% \pm 0.2\mu A}{I_1 \pm 0.2\% \pm 0.2\mu A} \pm 1$$

Eliminating the absolute errors, by adjusting the reference voltage (or V_3-V_4 channel gain) and introducing a zero-offset, we can estimate stability:

$$N = \frac{(V_1-V_2 \pm 5\mu V/^\circ C)}{(V_3-V_4 \pm 5\mu V/^\circ C)} \cdot \frac{C_1 \pm 0.01\%/^\circ C}{C_2 \pm 0.01\%/^\circ C} \cdot \frac{I_2}{I_1} \pm 1.$$

For example, with a reference V_3-V_4 of 5V, a full-scale reading of 10 V, and a temperature range of $\pm 10^\circ C$, the ratio $C_1I_2/C_2I_1 = 5000$ (DVM reads (1)0,000 F.S.), the worst case error in N is about ±0.4% at full scale, entirely due to the capacitor tracing errors.

The figures chosen for capacitor tracking errors were actually pessimistic. By making the capacitors as a monolithic pair, tracking characteristics considerable better than ±0.2% should be attainable.

Linearity errors, after zero-suppression, are estimated as being less than ±0.1% over a 25 V common-mode range.

CONVERSION TIME

The time to make a complete conversion depends on several factors, including the number of displayed digits, capacitor values, timing currents and reset currents. Typically, the clock rate will be in the range 10 kHz to 1 MHz, and the full-scale count will be between 1,000 and 10,000. Thus, conversion times will be between 1 ms and 1S,

typically 100 ms. Some loss of accuracy will be incurred at clock rates above 100 kHz, but rates up to 2.5 MHz will be possible, permitting 1000-level conversions in 400 μs.

INTERNAL REFERENCE SOURCE

An internal temperature-compensated reference diode is included, having these characteristics:

Nominal voltage = 7.5V ±2% at 100 μA

Temperature coefficient = Better than ±0.0025% per degree C

Slope resistance = ≤200Ω at 100 μA

The positive terminal of this device is tied permanently to the V_3 input; the negative terminal is taken to a separate bonding pad, but in the single-chip version this terminal is tied back to the V_4 input. Thus, in most applications, it is only necessary to connect a -100 μA current source to the V_4 input and ground the V_3 input to set up the internal reference. Alternatively, if an external V_3-V_4 input is preferred, it can be used. In the single-chip version this input is limited to somewhat less than 7.5 V; in the two-chip version, it may be up to 25 V.

PIN-BY-PIN DESCRIPTION OF CONNECTIONS

1: Single-chip realization (20-pins)

Pin #	Function
1	Reference oscillator capacitor, C_2 (to ground)
2	Reference oscillator current, I_2 (into -14 V)
3	Signal oscillator current, I_1 (into -14 V)
4	Signal oscillator capacitor, C_1 (to ground)
5	+15 V @ ≤3 mA
6	V_1 (+ve sense signal input, I_{IN} = -0.5μA ±0.2μA)
7	V_2 (-ve sense signal input, I_{IN} = -0.5μA ±0.2μA)
8*	Timeslot pulse #2, via 100 K ±10%
9	Multiplexed output data (0 to - 1 mA into ≥ +5V)
10	Overflow output (one clock-width pulse, >500μA into +4 V to -30 V)
11	Readout control (special use)
12*	Timeslot pulse #4, via 13.3 K ±1% (MSD)
13*	Timeslot pulse #5, via 13.3 K ±1%
14*	Timeslot pulse #6, via 13.3 K ±1%
15*	Timeslot pulse #7, via 13.3 K ±1% (LSD)
16	Ground (I_{OUT} = + ≤25 mA)
17	+5 V @ ≤25 mA
18**	V_3 (+ sense reference input, I_{IN} = -0.5μA ±0.2μA)
19**	V_4 (- sense reference input, I_{IN} = -0.5μA ±0.2μA)
20	-15 V @ ≤3 mA

Notes: *) Timeslots used in "standard" readout format; may be any suitable currents.

**) Reference voltage is supplied from external source if less than 7.5 V. The internal reference diode of 7.5 V is activated by passing a current of 100 μA from pin 18 to pin 19.

2. Two-chip realization. (Only the A-D convertor pins are listed here. The M59 is described elsewhere)

Pin #	Function
1	V_3
2	V_4
3	C_2
4	I_2
5	I_1
6	C_1
7	V_1
8	V_2
9	V_{REF} (-7.5 V to pin 1)
10	COUNT OUT
11	+15 V
12	RESET OUT
13	TRANSFER OUT
14	POLARITY OUT
15	TS2 (OR POLARITY CURRENT)
16	-15 V

PACKAGE CONFIGURATION

The present 20-pin Tektronix package is not suitable for general use, due mainly to mechanical problems. Under a separate proposal entitled "I. C. packaging" some suggestions are made for an improved packaging scheme.

TYPICAL APPLICATIONS

1. Simple DVM in a plug-in using single-chip version.

This is shown in Fig. 4. The internal reference diode is used, the current for which is supplied by R1. Calibration is by adjustment of R2, leaving the "I2" input available for use as a scaling-factor input (shown here connected to a fixed current provided by R3). The components on the right-hand side of this figure are used to shift the data back to the ground-level of the column data line (not necessary if the DVM is used in the main-frame, where the data can be summed at a positive level). Resistors have also been shown whose function is simply to add the letter "V" after the digits, and position a decimal point after the second digit.

With the component values shown, the DVM reads ±10.00 V for a ±10 V input, and can overrange with no extra components to ±25 V differentially (input floating) or ±12.5 V (one input grounded). No zero-adjustment is needed on this scale, since the last digit represents 10 mV, well below the anticipated zero-error of the convertor.

The indicated polarity can be inverted (without reversing the signal connections) by adding an additional -100 μA to the column data during TS2, should this be necessary.

Conversion time is approximately 75 ms; this is composed of 2,800 increments of 25 μs, plus 5 ms reset time for the signal ramp.

2. More precise version, with 1 mV/digit resolution.

To change the scale to read 1 mV per digit, it is necessary to increase the ratio C_1/C_2 by a factor of ten, add a zero adjustment, change the decimal point location, and possibly add a 4th-digit overflow indicator,

since digital full-scale (9.999 V) is now less than the full-scale analog capability. These changes are shown in Fig. 5.

The overflow indicator works this way: If a count in excess of 9999 occurs, an overflow pulse is generated by the I.C. This charges C_3 and causes a 1 mA timeslot pulse to be gated into the column data line during TS3. This introduces the ">" symbol between the polarity symbol and the digits. If desired, the symbol could be a "1", but the resulting five-digit display is misleading in its precision. For an input of -12.345 V the display will read either ->2.345 V or -12.345 V. Notice that in the first case the ">" symbol is on its proper location: the form >-2.345 V is ambiguous.

3. Addition of an input buffer and amplifier.

The above configurations present only a modest load to the source: the typical input current for an input of 10 V is 0.3 μA. For those applications where reduced signal loading is desirable, an input buffer may be used. If a high-quality operational amplifier is used, it can be put to good use in also providing gain and input protection. Fig. 6 shows a scheme offering full-scale readings of ±1000 V, ±100.0 V, ±10.00 V, ±1.000 V and ±100.0 mV (100μV resolution). Input impedance is 10 MΩ on the first two ranges, but goes up to beyond 1 GΩ on the last three. The Intech A-100 costs about $15. A zero-adjust is needed for the most sensitive range, but no additional adjustments are required. Full readout coding to produce the above format is included in this drawing. No overflow indication is needed, since the analog system overloads before the digital system.

4. An example of a computing application.

To illustrate the use of the auxiliary signal inputs, Fig. 7 shows a scheme to display the quantity XY/PQ. The clock timing capacitor, C_2, must be trimmed to an exact value, if all inputs are to be used. The accuracy of this scheme is limited largely by the simple circuits used to convert the Y and Q input voltages to currents.

5. Two-package version as complete DVM.

To illustrate the possibilities for making an entirely self-contained DVM, the circuit shown in Fig. 8 is given. This uses the two-chip realization to allow access to the data outputs in parallel form. These outputs drive 100 μA moving-coil meters, of the vertical, side-by-side type. A polarity light indicates a negative input.

6. Two-package version with floating inputs.

To achieve a truly differential-input capability, the input convertor must be operated from a floating supply of 30 V, and A.C. coupling of the COUNT, TRANSFER, RESET and POLARITY signals must be used. This coupling could be simply by means of capacitors. However, there are advantages in transformer coupling. First, there is less capacitive loading of the floating "low" input. Second, the signal input can have large common-mode a.c. components superimposed on it without disturbing the operation of the system.

A suitable arrangement is shown in Fig. 9. Only the components relevant to interfacing are discussed. T1 transmits the COUNT pulses; C3 forms a return path for this signal, and serves another purpose, discussed later. T2 transmits the RESET pulse; Q1, R1 and C4 are required because of the limited current available from the RESET output on the

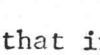
convertor. T3 transmits the TRANSFER pulse; C5 is required to maintain correct bias conditions in the M59.

Since the polarity is stored in the convertor in static form, it is necessary to chop this signal. This is the purpose of C3 and D1. Instead of the usual -100 μA timeslot current to pin 10 of the convertor, a pulsed current at the clock rate is applied. The resulting output from T3 is a pulse burst (equal in length to the count burst) when the input polarity is negative. D2 and C6 store this burst, which may be only a single pulse, for a conversion cycle. Q2 generates a -100 μA output during TS2 if its base is at ≥200 mV, thus modifying the polarity symbol from "+" to "-".

7. A continuous-hold analog memory.

Another application of this I.C. is as an analog memory with infinite hold time. This may be useful in sampling applications, in drift-correction applications (can sample zero-level at intervals of perhaps a minute) and in ITS and APD applications. The relatively long conversion time of the DVM could be reduced, in one step and with good accuracy, to 100 ns, and maybe as short as 10 ns, by means of a gated, fed-back memory, such as was developed for the 7524.

The precision of the re-constituted signal in the open-loop mode is limited by the accuracy of the D-A convertors within the M59, to about ±1%. However, by closing a loop around the system, a storage precision approaching that of the digital scale (one part in 10,000) could be achieved. (Fig. 10). The fact that the 10,000-level staircase generated by the M59 is not monotonic, due to the inexactness of each decades' contribution, means that there may be several levels at which balance

can occur, and that the digital contents of the buffer store are not correct, neither of which are important in this application. Precise operation is ensured by generating a "lightning-bolt" waveform () so that increasing jumps () are absent, and every value is generated.

Notice that the ramp timing capacitor is now absent, and the digitally generated ramp connected back to this point. The clock runs continuously, and an output is taken to the M59 from the lower end of the capacitor C_2. Also, the "COUNT" output of the convertor is now used as a "TRANSFER" pulse; the TRANSFER & RESET outputs of the convertor are not connected.

Operation is simple. A "START" pulse resets the counter and transfers the 0000 state into the buffer store. This causes the output of the op-amp to drop to about -12 V, which in turn allows "COUNT" pulses to appear at pin 15 of the convertor. Since the counter receives a continuous clock input, these pulses transfer the increasing count to the D-A convertor, and the digital ramp rises. When it is equal to the input, the transfer pulses end, and the analog output remains at the input level until the next start pulse.

If there is sufficient interest in this application, a second-layer metal having interconnections for this configuration could be made, and the whole put in a 20-pin package.

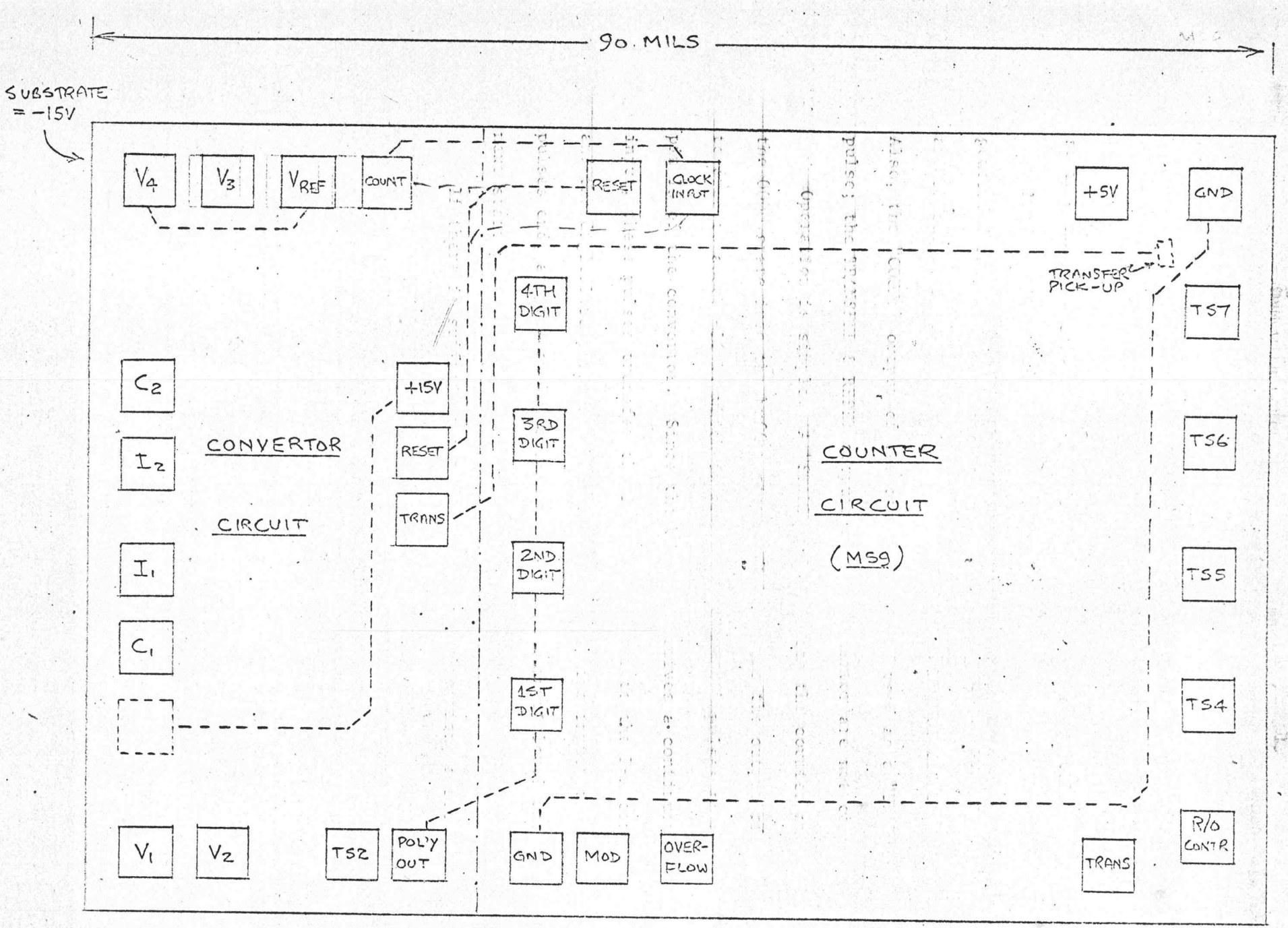


FIG 1 : CHIP ORGANIZATION

Barrie 28 MAR 70

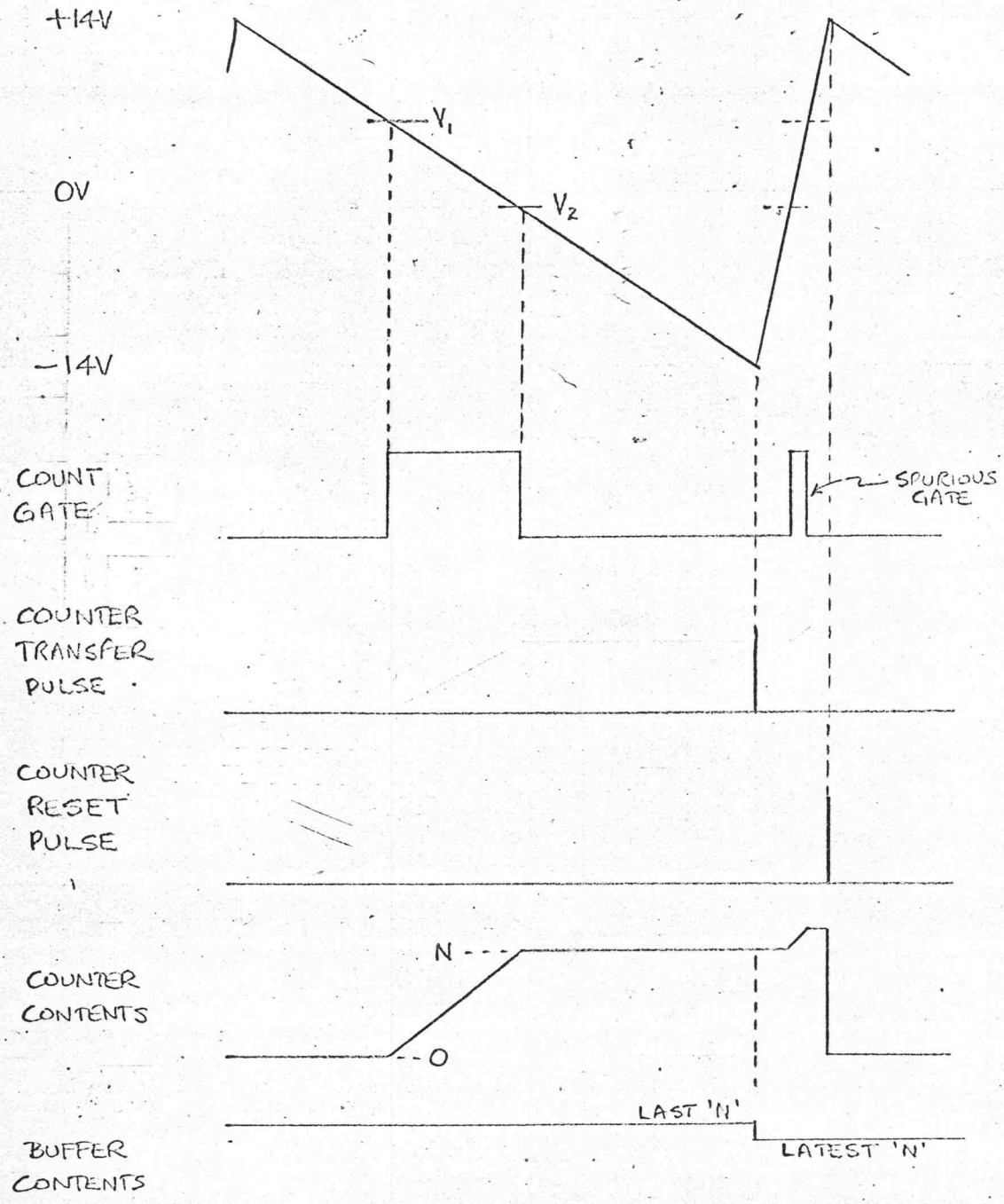


FIG 2 : RAMP-CONVERSION

Banie 28 MAR 70

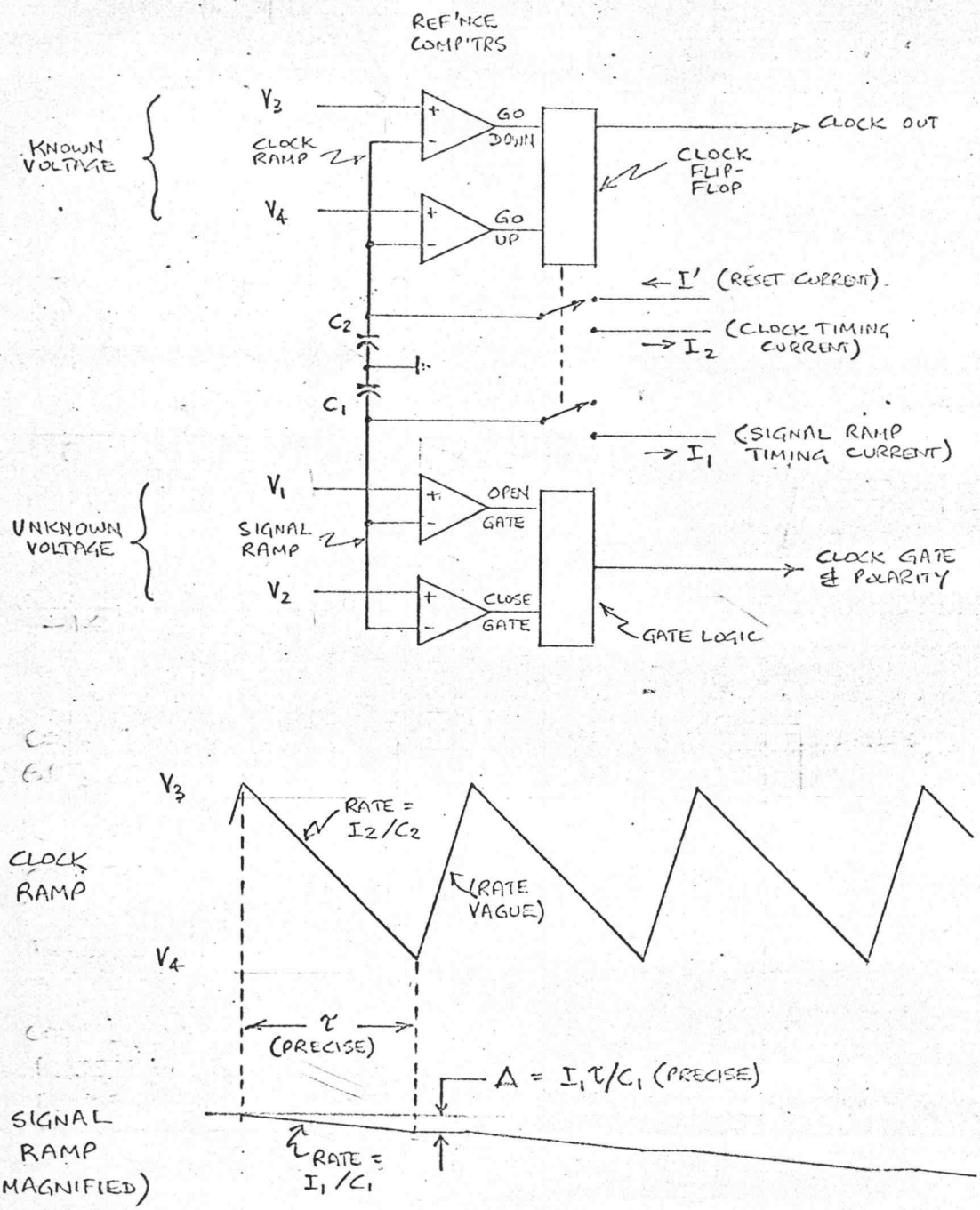


FIG 3: IMPROVED RAMP-CONVERSION

Banie 28 MAR 70

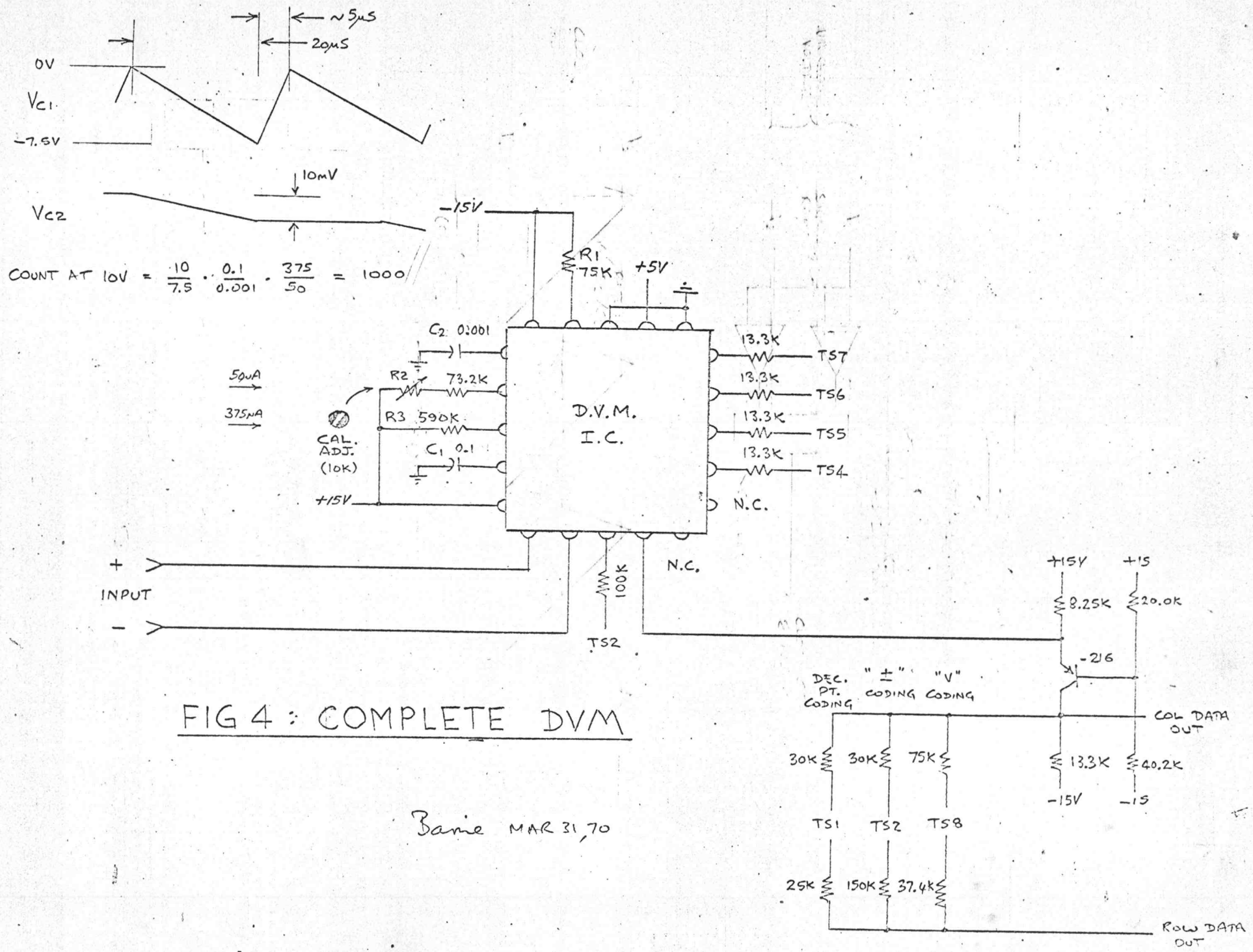


FIG 4 : COMPLETE DVM

Barrie MAR 31, 70

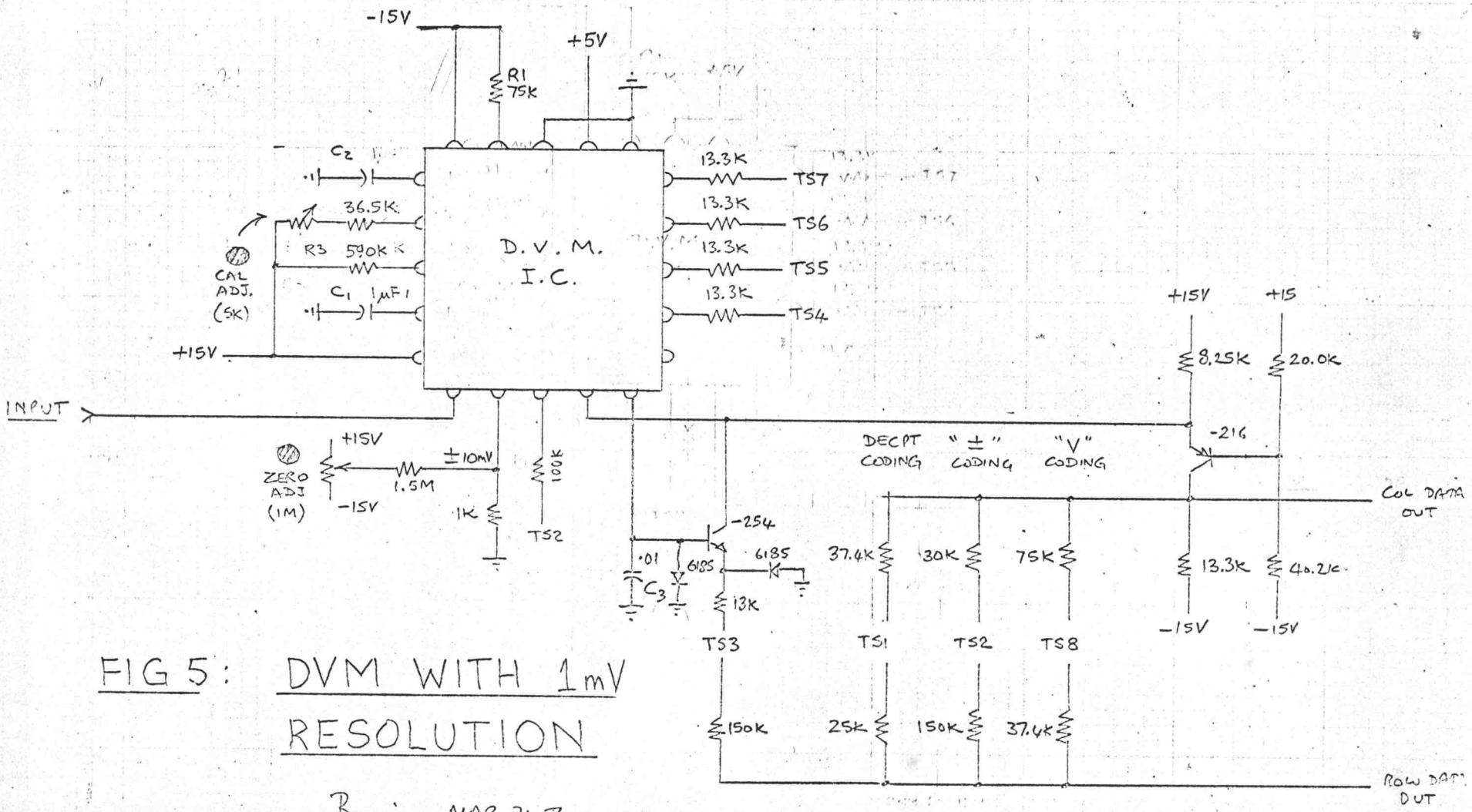


FIG 5: DVM WITH 1mV RESOLUTION

Barnie MAR 31, 70

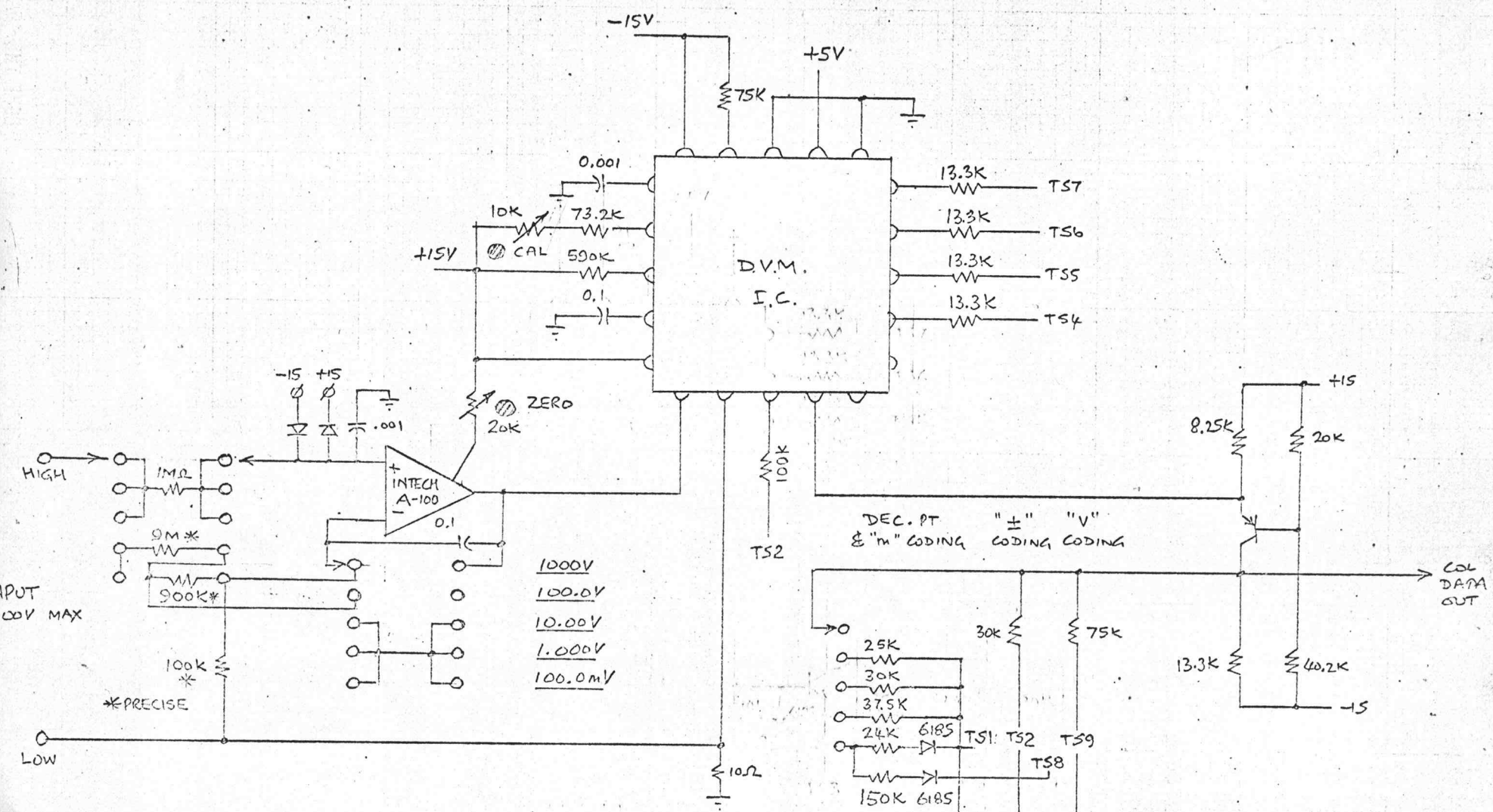


FIG 6: MULTIRANGE DVM

Bamie MAR 31,70

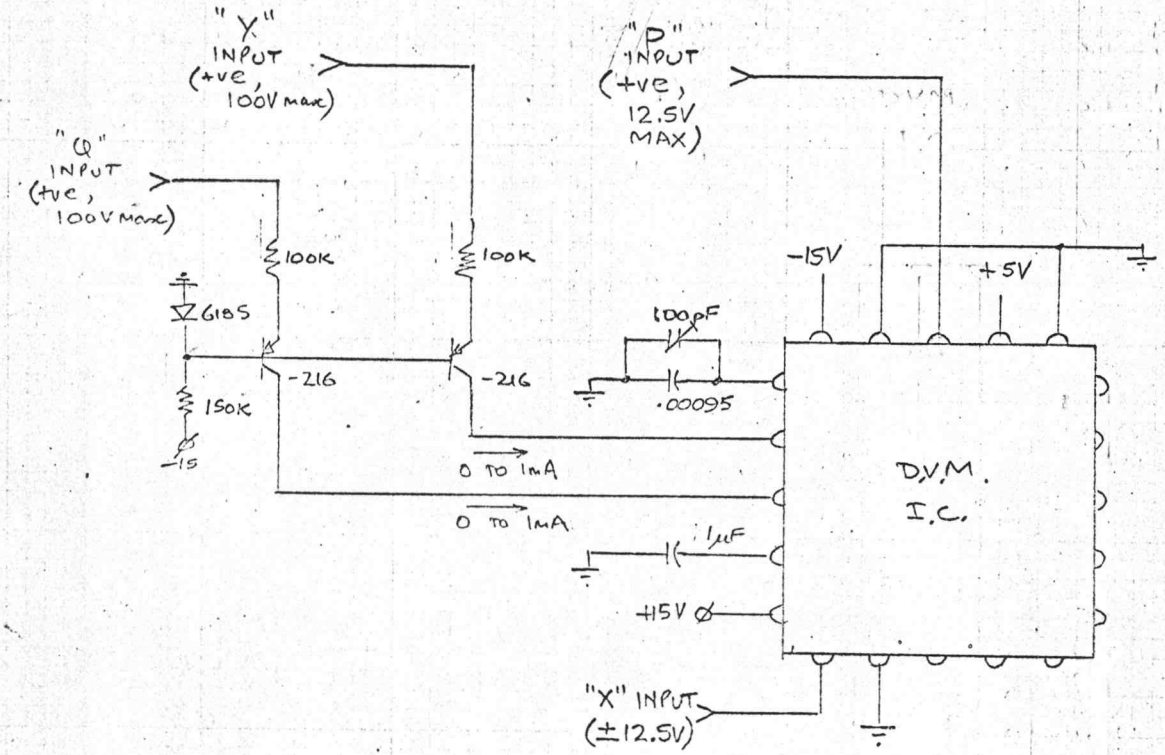


FIG 7 : ANALOG/DIGITAL ARITHMETIC

Barnó 1 APR 70

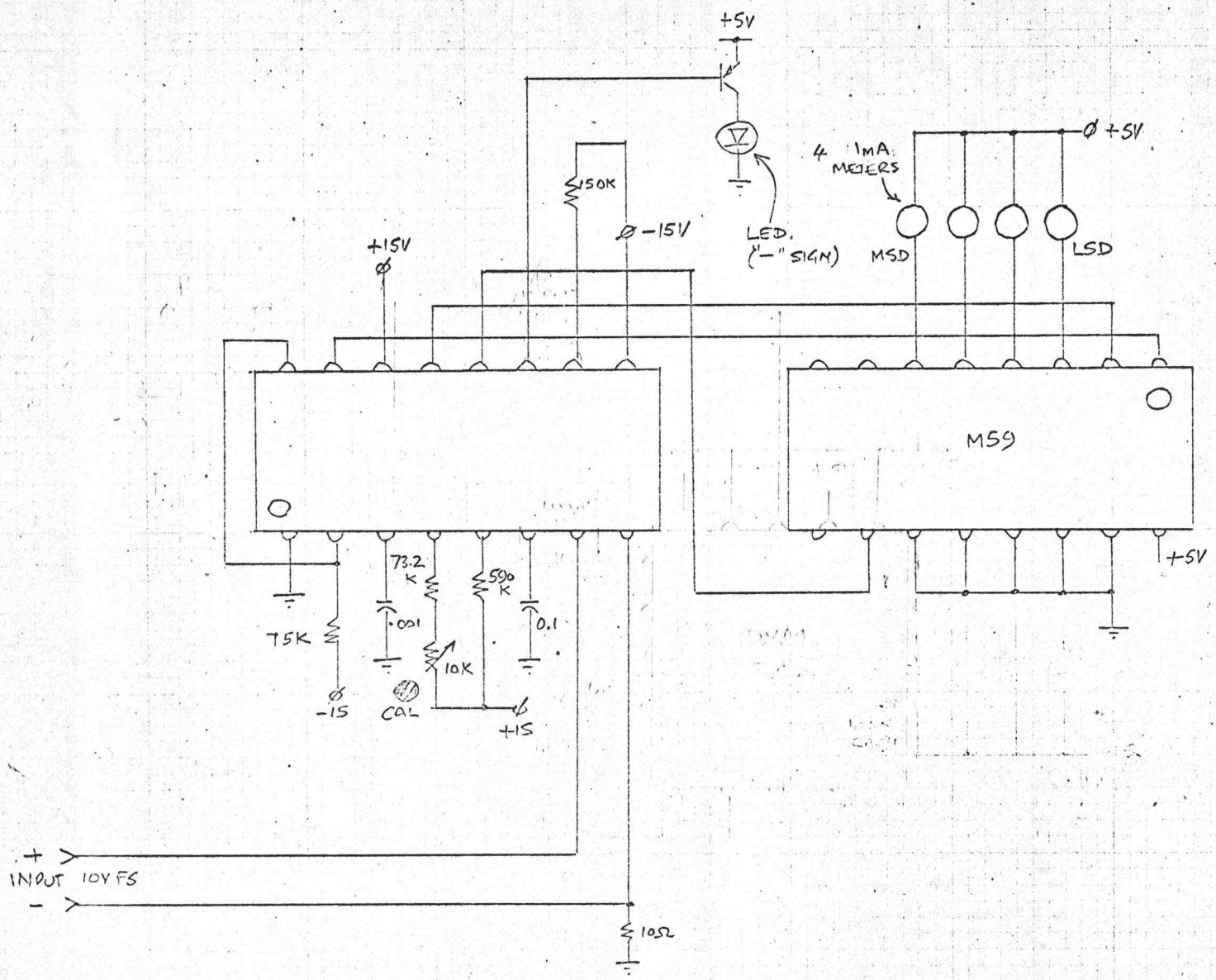


FIG 8 : SELF-CONTAINED DVM Barié 1 APR 70.

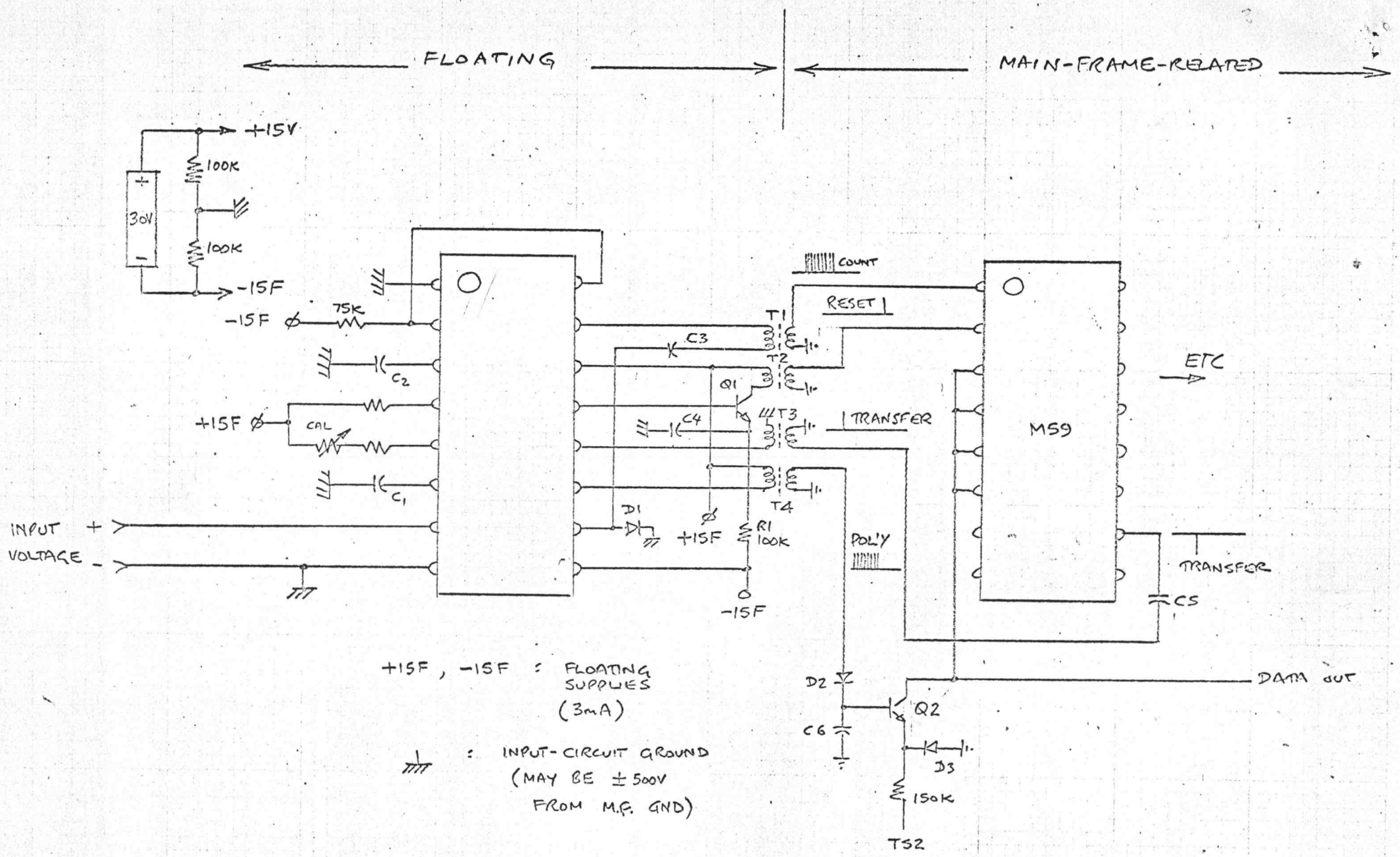


FIG 9 : FULLY-FLOATING INPUT CONVERTOR

(Requires 30V 3mA supply).

Barrie MAR 31, 70

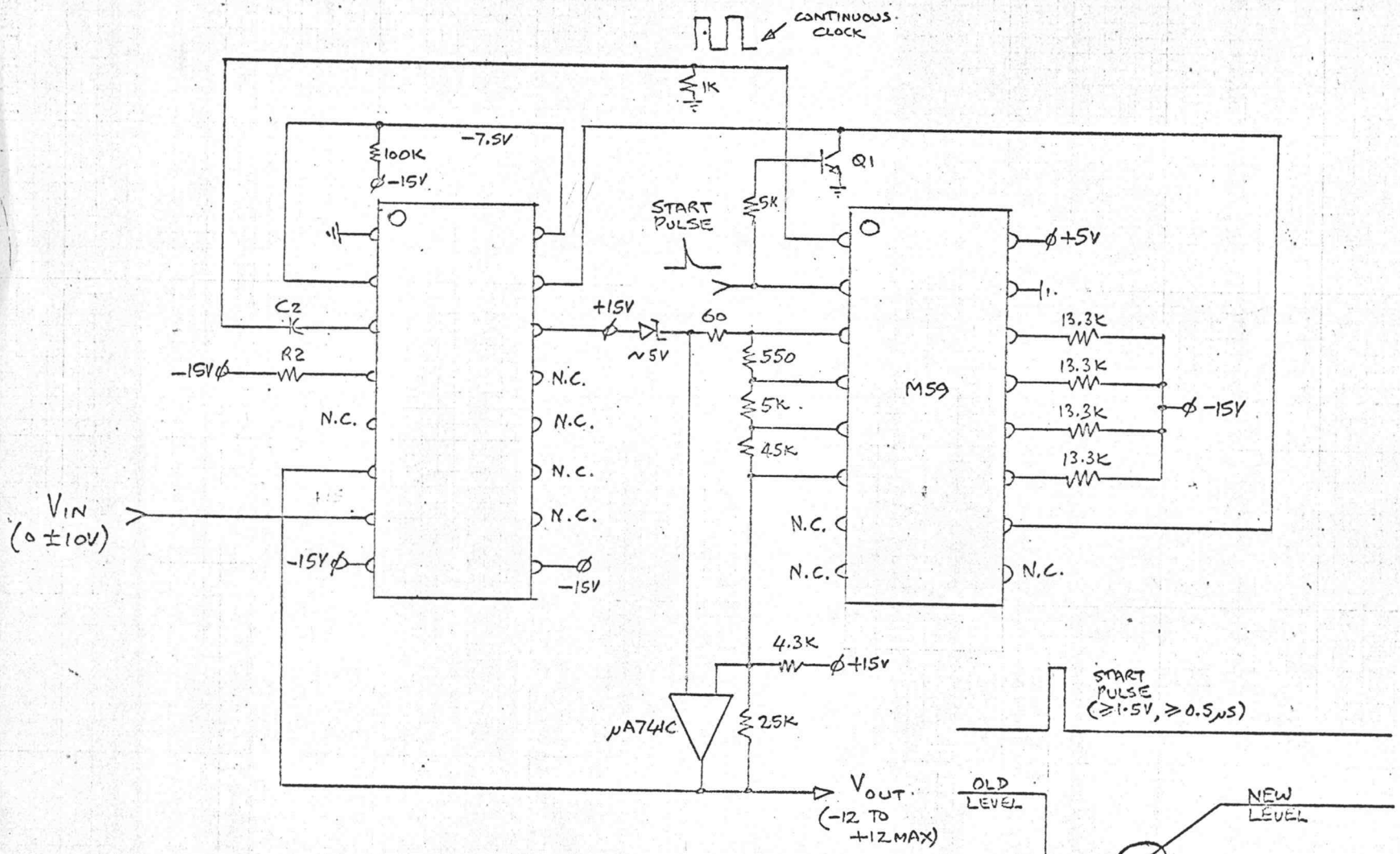


FIG 10 : ANALOG MEMORY

Barrie MAR 31 70