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SEPTEMBER 1983

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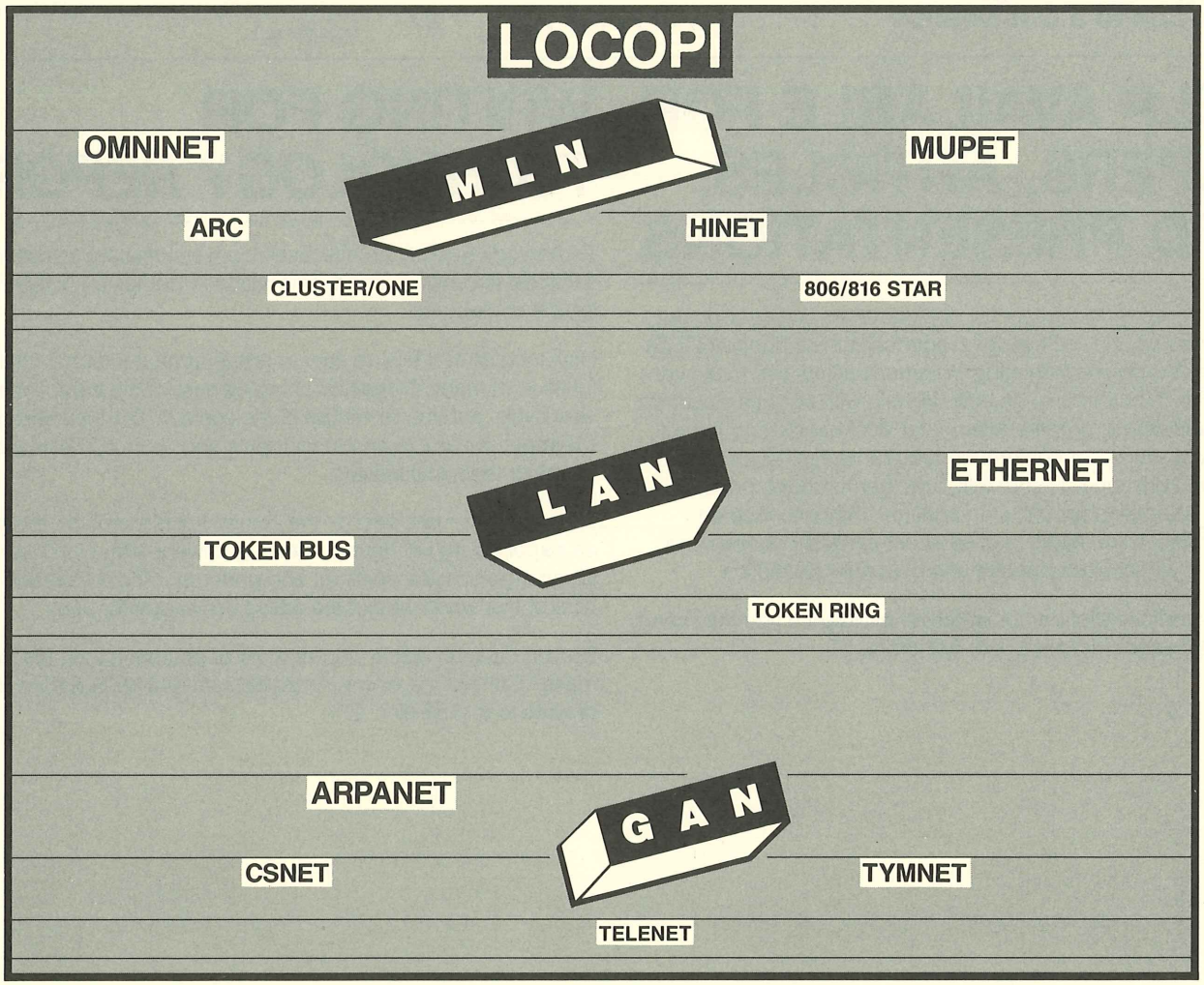

LOCOPI–MICROCOMPUTER LOCAL NETWORK

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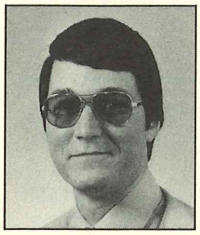
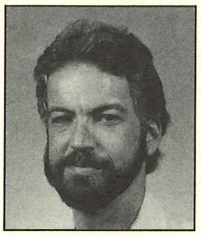
LOCOPI – THE ARCHITECTURE OF A MICROCOMPUTER LOCAL NETWORK

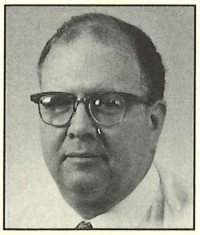
David Jiang is a project leader in the Data Communications and Networking group, part of IDD. David joined Tek in 1982 after receiving his PhD EE from the University of Kansas. He also has an MSEE from the University of Kansas.



Dan Sheley is a project manager in the Data Communications and Networking group, part of IDD. Dan joined Tek in 1974 after receiving his BSEE from Ohio State University.



Keith Parker is an electronic engineer in the Data Communications and Networking group, part of IDD. Keith joined Tek in 1973 after serving in the U.S. Army Security Agency.



Donlan Jones is the engineering manager of the Data Communications and Networking group, part of IDD. Donlan joined Tek in 1969. In addition to his BEE from the University of Santa Clara, Donlan holds an MS in engineering from the University of California, Los Angeles and the Degree of Electrical Engineering from Stanford.

IDD needs a low-cost standard network for its products. This article describes LOCOPI, a Tektronix-developed candidate for such a standard.

A recent survey by Strategic, Inc. indicates that high-performance, high-speed local area networks such as Xerox's Ethernet – although they receive much publicity – are less numerous than lower performance networks. Over 12,000 low-performance networks are in use; in contrast, there are just 800 high-performance networks. This 15 to 1 ratio is due to performance needs, costs, protocols, and to political considerations.

Computer networks are generally divided into three levels based on areas covered: Global Area Network (GAN), Local Area Network (LAN), and Microcomputer Local Network (MLN) (see figure 1). Ethernet is a LAN. LOCOPI is an MLN.

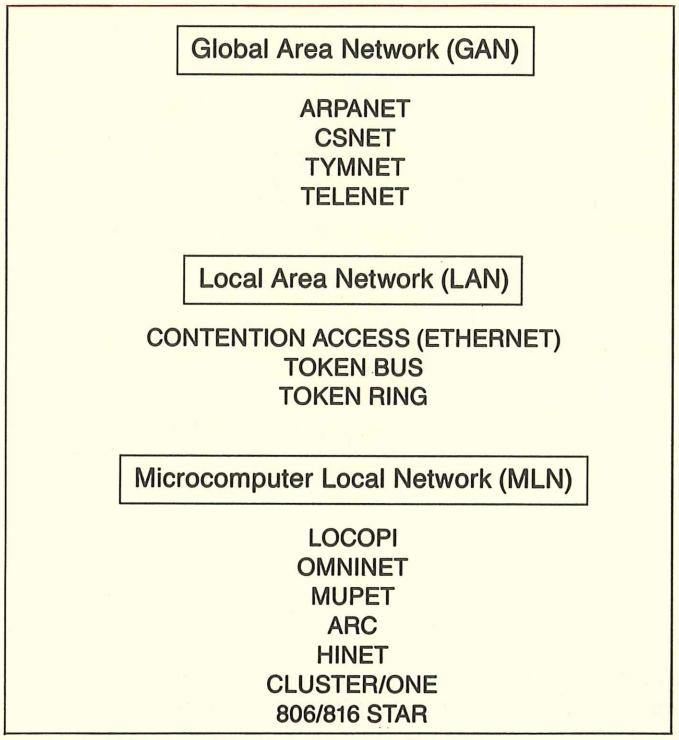


Figure 1. The three levels of computer networks and examples of networks and network types.

The Tektronix Information Display Division requires both high-end and low-end communications capabilities (figure 2). On the high end, Ethernet-like systems are available to interface IDD products to most major hosts. But IDD also needs a better communication link for low-end terminals and peripherals. Ideally, this link should be inexpensive but still fast enough to handle the higher data rates of future products.

Today, several million computers are configured in small work groups of 4 to 8 personal computers. In these small networks (MLNs), PCs share printers, hard disks, and other expensive peripherals; or they share a desk-top workstation interface to printers, copiers, and plotters. By comparison, only a few thousand companies have the 1000 plus employees that make them candidates for expensive, high-performance networks such as Ethernet.

Today, the cost of a connection into a high-performance network, such as Ethernet, averages more than $2000. In contrast, connections into small networks cost less than $500 each. Because personal computers average about $2000 – one reason for their popularity – it is seldom economical to link PCs with a LAN.

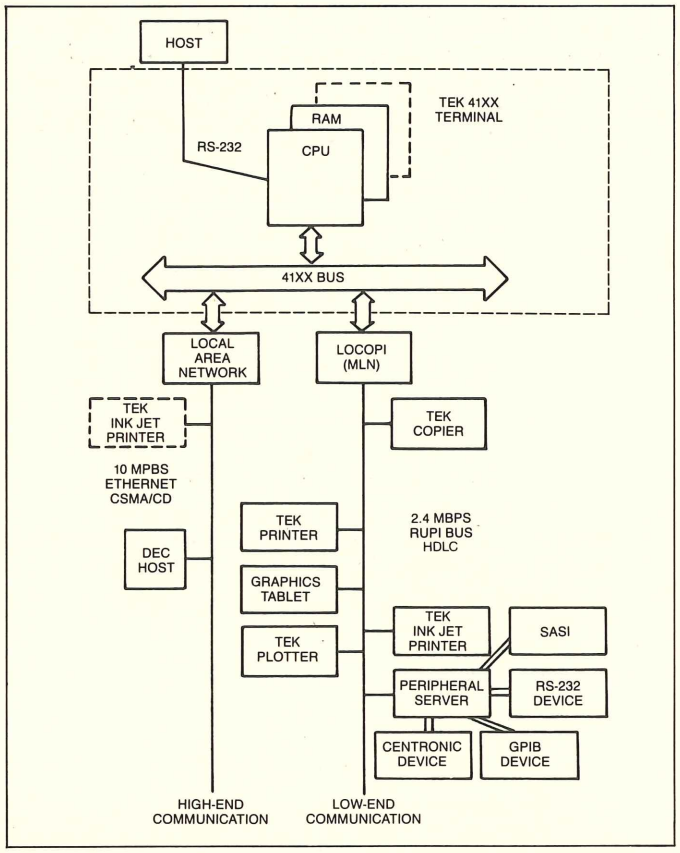


Figure 2. High-end applications of IDD products are served well by high-end communication networks such as Ethernet. At the low-end, however, a system such as LOCOPI is needed to efficiently tie small groups of products and peripherals together. LOCOPI would greatly reduce network engineering expense by providing a standard low cost peripheral interface based on the INTEL 8044 Remote Universal Peripheral Interface (RUPI).

Network Standards Slow In Coming

Network standards are desirable, but such standards are not yet complete. They are slow in coming.

The IEEE-802 LAN standard covers only layers 1 and 2 of the ISO-OSI 7-layer Protocol. The proposed IEEE standard for higher layer protocols (layers 3 to 7) is still several years away. The need for a practical peripheral interface/MLN is immediate.

The two giants, IBM and AT&T, haven't committed to the IEEE-802 standard. Bell Labs, on the other hand, is developing its own local area network called the Bell Local Network (BLN), which is scheduled for announcement this year. IBM most likely will not support IEEE-802.3 CSMA/CD Ethernet-like LANs, which were invented by its competitor Xerox. IBM has recently announced its own token ring local area network.

IDD, too, needs a low-cost locally distributed computer network for its products.

LOCOPI Design

In many applications for IDD products, several terminals share an expensive peripheral. But with no standard interconnection scheme, not one but several interface schemes are used, including RS-232-C, GPIB, Centronics, and SCSI (figure 3). This variety imposes a heavy hardware and software burden on all peripheral and terminal interfaces.

A standard, modular, intelligent, high-speed serial interface would reduce both the hardware and software burden. Such a standard interface would also enable us to reduce power supply, slot space, cable, connector, and ECB requirements.

We think the Low Cost Peripheral Interface (LOCOPI) concept can solve the problem. LOCOPI is a standard low-end communication link. As such, it would replace the various interface schemes now used for IDD products.

The Data Communications and Networking group is developing LOCOPI in three phases. The first phase emphasized interfacing a single computer to several peripherals. This phase is complete.

Phase two will focus on multiple computers sharing multiple peripherals. It will also include a peripheral server to allow existing products (without LOCOPI) to function in the network.

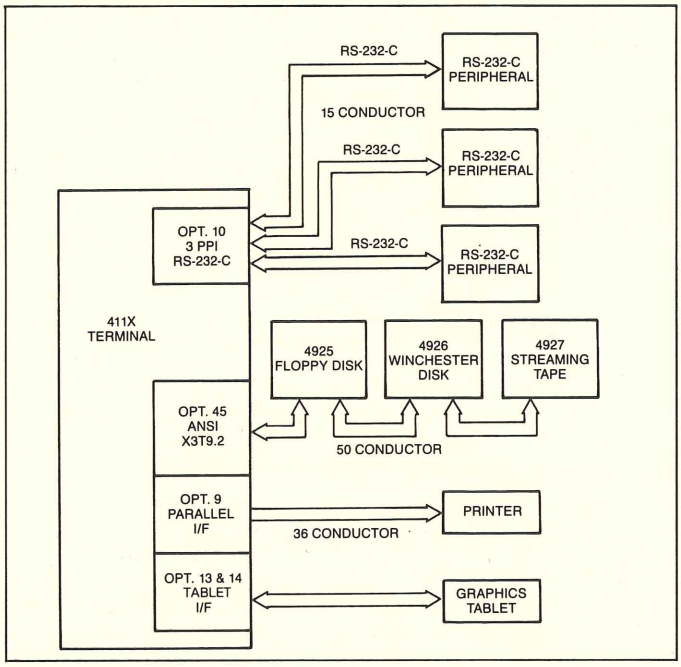


Figure 3. Today, IDD low-end networks include a variety of networking schemes. This requires extra design, documentation, and after-sales support.

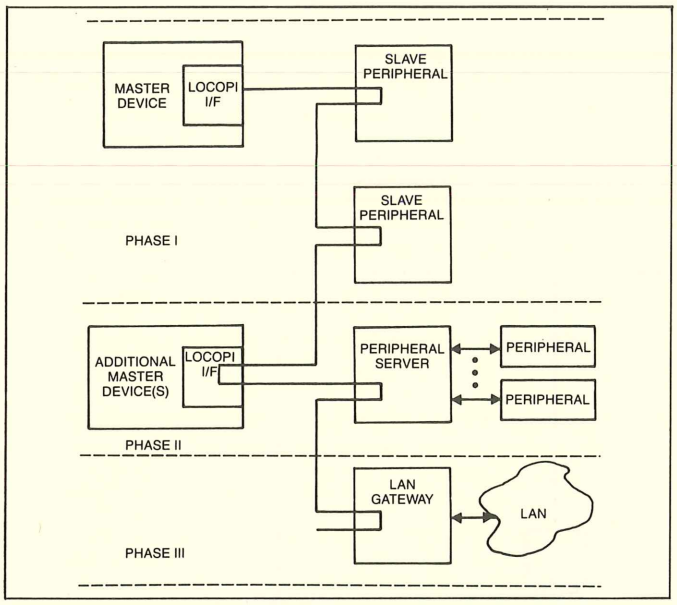


Figure 4. A LOCOPI configuration such as this will enable both existing and developing IDD products to communicate in MLNs and LANs.

Phase three will develop gateway bridges between LANs and LOCOPI. Figure 4 shows how it will enable both existing and developing IDD products to communicate in MLNs and LANs.

The remainder of this article discusses the design of phase one and some experimental results.

LOCOPI Architecture

Most MLN node architectures (figure 5) consist of an 8-bit CPU, a protocol controller, a DMA controller, EPROM, buffer RAM, and an RS-422 line driver/receiver. Nodes communicate with each other using one or two twisted-pairs of wire, (using either separate clock and data lines or a Manchester Encoder/Decoder (MED)). Nodes communicate at 1–3 MBPS and are separated by less than 2000 feet.

Recent VLSI technology has simplified MLN design. The Intel 8044 RUPI (remote universal peripheral interface) supports data rates up to 2.4 MBPS. The 8044 RUPI is an Intel 8051 single-chip microcomputer with an independent HDLC/SDLC protocol controller (also known as a serial interface unit – SIU). The RUPI also contains a local bus with 192-bytes RAM, 4-Kbytes ROM, two 16-bit timer/counters, a Boolean processor, and 32 I/O lines – all of this in a single 40-pin package. The LOCOPI was designed to fully use the power of the 8044 RUPI with few external components.

A nodal network requires that the individual nodes be designed to have good modularity. Then, connecting them to networks becomes easier. The first phase of LOCOPI is implemented with one master 8044 RUPI and up to 255 slaves. A low cost twisted-pair of wires links the master and slaves. The network runs at 2.4 MBPS with standard HDLC protocol.

Each LOCOPI interface can be partitioned into 3 sections:

(1) IMP – Interface Message Processor

(2) HIL – Host Interface Logic

(3) MED – Manchester Encoder and Decoder

The twisted pairs between LOCOPIs carry the Manchester encoded data. Each interface has two loop-through connectors. The basic LOCOPI configuration is shown in figure 6.

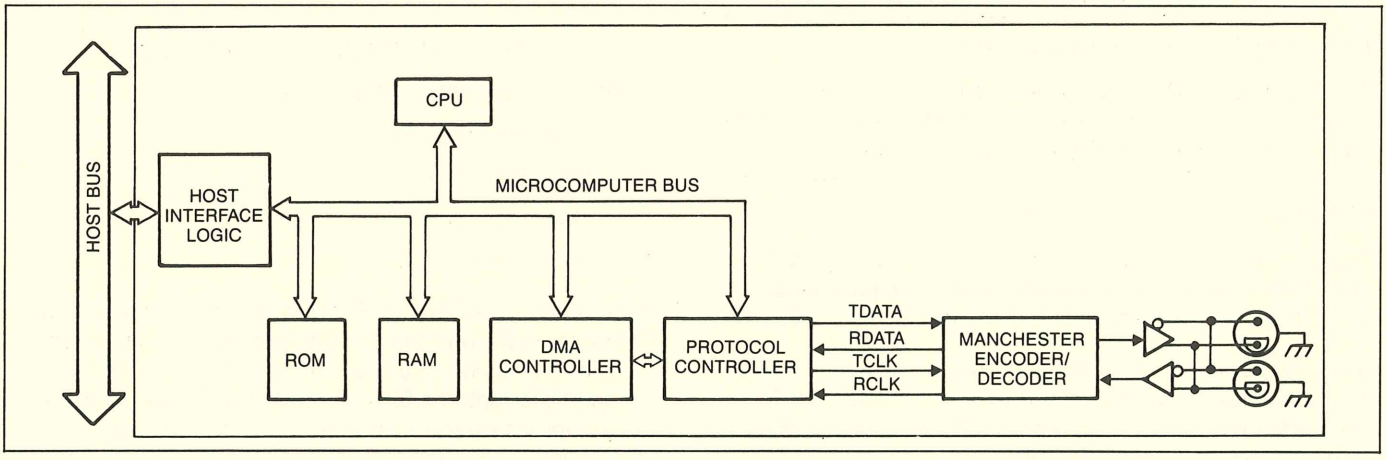


Figure 5. Typical architecture of a MLN node. Nodes communicate at 1 to 3 MBPs over twisted pairs. Nodes are separated by no more than 2000 feet. (See figure 7 for LOCOPI nodal architecture.)

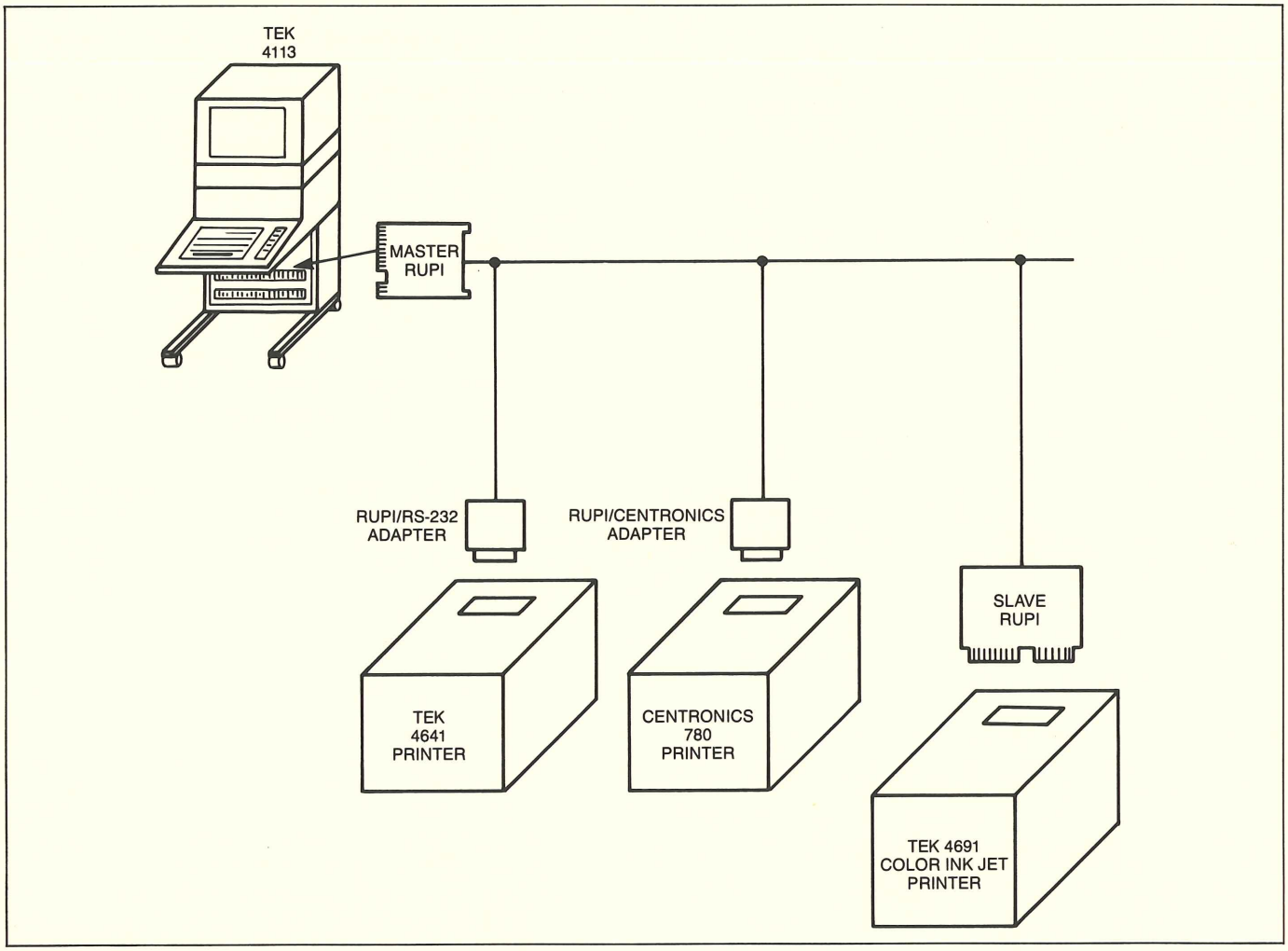


Figure 6. The configuration used to evaluate LOCOPI.

IMP – Interface Message Processor

The master LOCOPI, based on the Intel 8044 RUPI, controls handshaking with the host and also controls the SIU; therefore the master SIU is initialized with the CPU. It is the RUPI's task to encode and decode control fields, manage acknowledgements, and adhere to the HDLC protocols.

The slave LOCOPI is also based on the Intel 8044 RUPI. The RUPI transfers commands and data to and from peripherals with the SIU. The SIU of the slave LOCOPI is initialized to AUTO mode.

In the AUTO mode, the SIU implements in hardware a subset of the SDLC/HDLC protocol such that the SIU independently responds to most HDLC frames without CPU intervention. All AUTO mode responses to the master station conform to the HDLC standard. The AUTO mode requires little software to implement a secondary station, and the hardware response to polls is much faster than a software generated response.

HIL (PIL) – The Host (Peripheral) Interface Logic

The Host Interface Logic (HIL) includes:

8DR – 8044 Data Register

8SR – 8044 Status Register

HCR – Host Command Register

HDR – Host Data Register

After power-on, the 8044 RUPI sets a "ready" status bit in the HCR to inform the host that the HIL is ready to accept a command. When the host issues a command, via the HCR, the command interrupts the 8044. The 8044 RUPI then jumps to the interrupt service routine and reads the command and clears the interrupt. Data is transferred in a similar way via the HDR.

In the case of the Tek 4691 Color Ink-jet Plotter, the host writes nine bytes of copy preamble. The RUPI SIU transmits this preamble and then waits for the "ready" acknowledgement from the peripheral. When data transfers begin, the host transfers 128 bytes at a time. A 4691 B-size (11 x 14″) image requires 640 lines of 480 bytes (307,200 bytes of data).

The PIL structure is quite different from the HIL. The 8044 RUPI writes data to the copier using a data string mode. The peripheral does not acknowledge except for preamble, end-of-line, and end-of-transmission.

MED – Manchester Encoder/Decoder

The 2.4 MBPS Manchester encoder/decoder (MED) emulator has been designed and tested (figure 7). It consists of a 74S86, a 74S08, two 74SL4s, and a 300-ns delay line. This MED emulator can be easily implemented as a hybrid IC. The hybrid emulator would probably include self-test logic and a line transceiver. Recently, AMD announced a 1–3 MBPS Manchester transceiver (AM7960). Harris Semiconductor has also announced a 1 MBPS MED (HD-6409).

Migration

A low cost peripheral server can interface products that use standard interfaces such as RS-232-C, Centronics, GPIB, and SCSI.

ACRONYMS AS ADJECTIVES

In this article LOCOPI has two meanings. The simplest is as a short noun substituting for the noun phrase *low cost peripheral interface.* The second usage is as an adjective or noun relating to the network whose character is pretty much determined by the characteristics of the LOCOPI interface. If you've ever been stopped by the redundancy in such usages as ECL logic and GPIB bus, you may be bothered by "LOCOPI interface," but some redundancy is better than chancing misunderstanding.

The LOCOPI/RS-232-C interface (figure 8) consists of an 8044 RUPI, a National 8250B asynchronous communication element (ACE), RS-232-C level converters (1488 & 1489), and a 74LS373 octal latch.

The LOCOPI/Centronics interface design (figure 9) consists of an 8044 RUPI, a 74LS138 octal decoder, a 74LS374 octal latch, a 74LS373 octal latch, and a 74LS244 octal buffer.

The LOCOPI/GPIB and LOCOPI/SCSI interfaces are being developed.

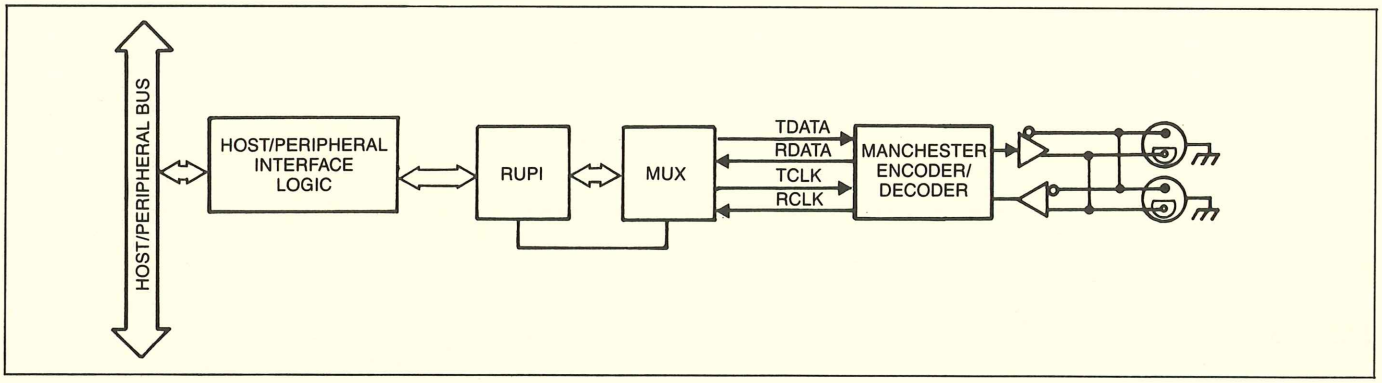


Figure 7. LOCOPI nodal architecture.

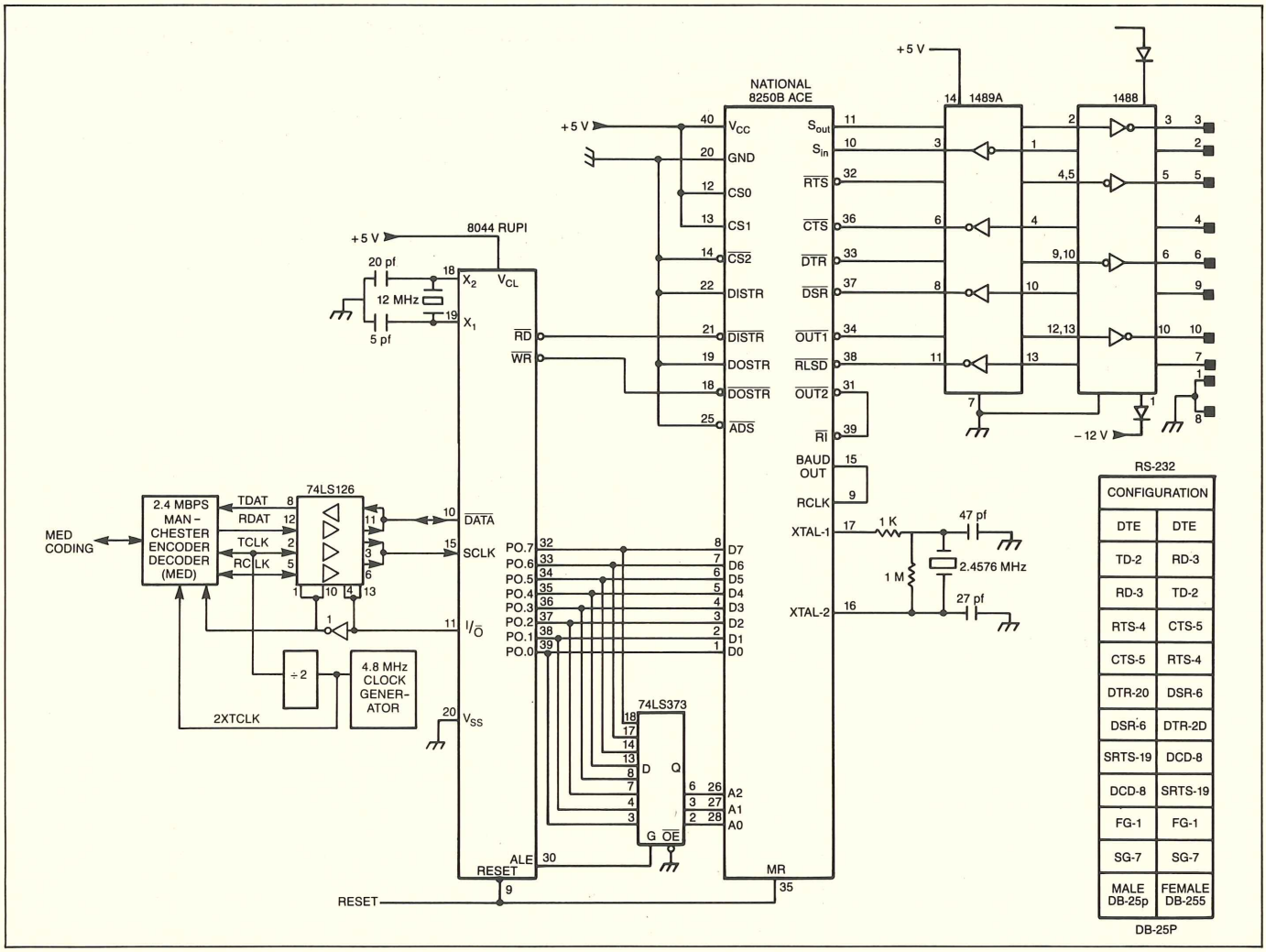


Figure 8. LOCOPI/RS-232 interface adapter.

Summary

The RUPI one-chip solution demonstrated that:

(1) A low cost, intelligent standard interface is practical.

(2) The 8044 RUPI can control high performance peripherals, such as the Tek 4691 Color Ink-Jet Plotter.

(3) A low-cost peripheral server can interface existing products that use RS-232-C, Centronics, GPIB, and SCSI.

A factory-mask RUPI that provides standard high level protocol as well as common code for various peripherals such as printers, copiers, etc. is being developed. This peripheral interface will cost less than $200 and will provide 2.4 MBPS performance. The $200 will cover electronics, board space, connectors, internal cables, labor, and built-in memory for optional firmware. In contrast, an Ethernet interface costs about $2000 and most MLNs are $500.

This high-speed, serial bus structured interface, employing a simple protocol and a completely distributed-control intelligent peripheral interface is practical.

For More Information

For more information, call Dan Sheley, 685-3696 (d.s. 63-489). □

Acknowledgements

The authors would like to thank everyone involved for their support and help: Phil Meany, Larry Mukai, Ray Goolsbey, Jocelyn Yu, Kelly Sims, Pete Radochonski, Art Yerkes, and Gloria Kelly.

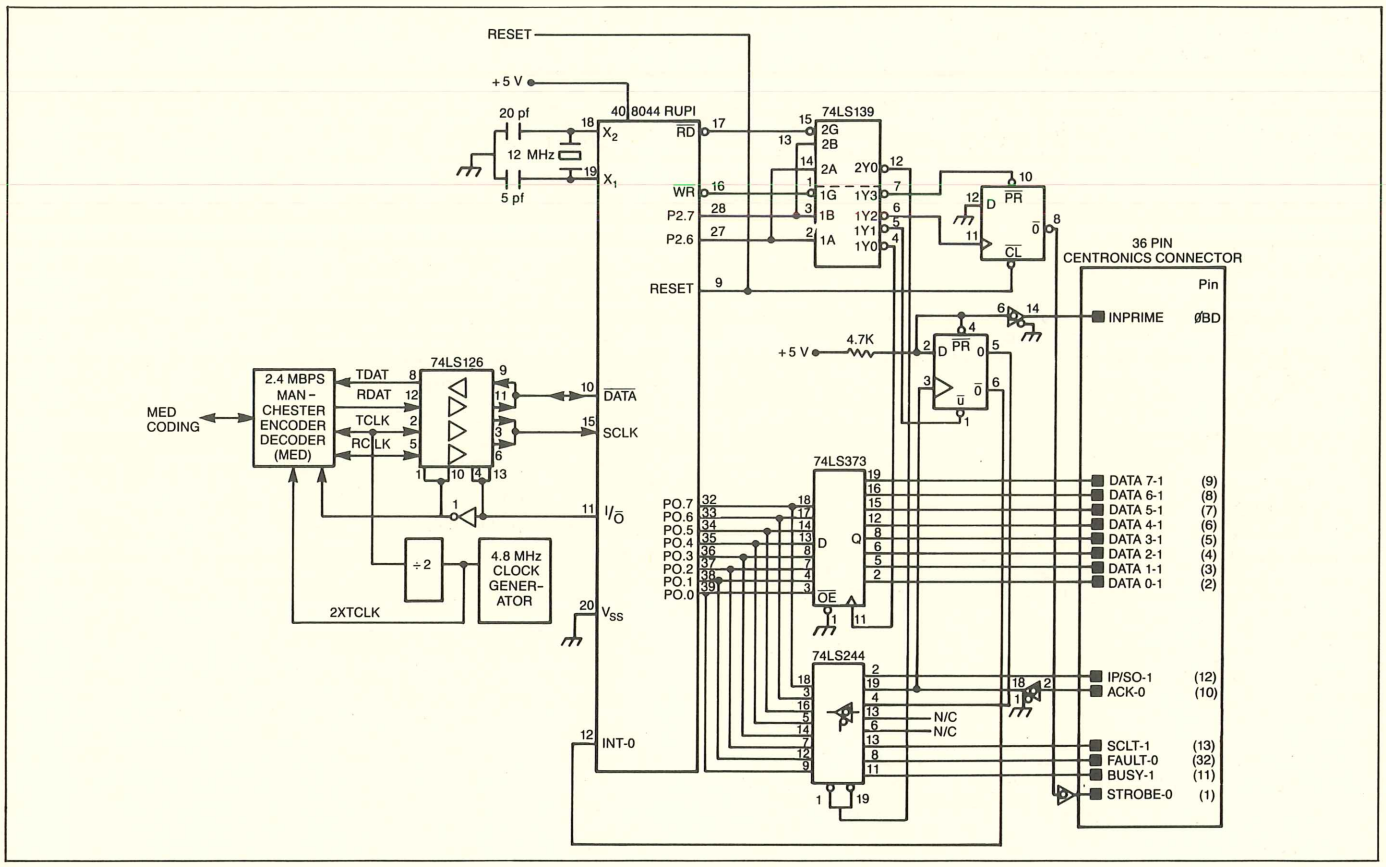


Figure 9. RUPI Centronics Interface.

Glossary

8DR – 8044 data register

8SR – 8044 status register

Centronics Interface – Parallel printer interface developed by Centronics Corp.

CSMA/CD – Carrier Sense Multiple Access/Collision Detect (An access priority concept)

GPIB – General Purpose Interface Bus (IEEE-488 Standard)

I/F – Interface

Ethernet – A coax-based, contention-access network developed by Xerox

GAN – Global Area Network

HCR – Host Command Register – LOCOPI acronym

HDLC – High-level Data Link Controller

HDR – Host Data Register

HIL – Host Interface Logic (sometimes called PIL)

IEEE-802 – IEEE local area network standard

LAN – Local Area Network

LOCOPI – LOw COst Peripheral Interface

Migration – Moving from present products to next generation products

MBPS – Megabits Per Second

MED – Manchester Encoder/Decoder

MLN – Microcomputer Local Network

PIL – Peripheral Interface Logic (see HIL)

RS-232-C – ANSI standard interface for serial data communication

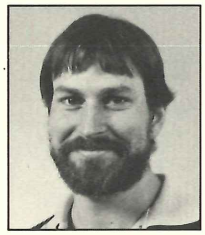
RUPI – Remote Universal Peripheral Interface (Intel 8044) Intel 8051 except that the SIU handles SDLC/HDLC

SCSI – Small Computer System Interface (ANSI X3T9.2 standard)

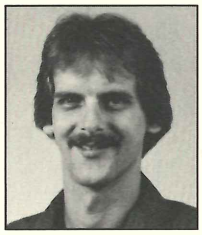
Peripheral Server – A device that manages access to multiple peripherals by one or more processors

SIU – Serial Interface Unit – 8044 RUPI acronym

COMPOSITE PRODUCES HIGH QUALITY CHASSIS



Ken Dobyns is an electromechanical design engineer in Storage Scopes, part of Portable Oscilloscopes. Ken joined Tek in 1980. He received his BSME from Oregon State University.



Jim Tsadilas is an electromechanical design engineer in Storage Scopes, part of Portable Oscilloscopes. Jim joined Tek in 1980. He received his BSME from Montana State University.

A composite of aluminum and spotmolded plastic produces a less expensive chassis of high quality. Portables Engineering has developed such a chassis to be incorporated into future products.

The basic concept for a better chassis design came out of an objective look at old and new manufacturing technologies. We assumed that since we were making widespread use of concepts which have been in use for many years, we could make significant gains with the newer technologies. The technology that seemed most promising was spotmolded plastic.

By using plastic in a composite with aluminum, we expected to build a product of as high a quality as the traditional all-aluminum chassis but with lower manufacturing costs. These were our goals:

1. Substantially lower manufacturing costs while keeping the best attributes of the conventional chassis.
2. Reduce instrument assembly time. To do this we had to reduce the part and hardware count. ("Hardware" here means screws, nuts, etc.)
3. Reduce or eliminate the manufacturing difficulties in the present technology, particularly the tolerance problems inherent in punching, bending, and then welding sheet metal. Typically, tolerances tighter than ±.015 inch are difficult to achieve.
4. Reduce the problems inherent in installing captive hardware, that is, the wrong or missing part in a given location or the correct part installed on the wrong side of the sheet. Both these errors are serious as they are often not discovered until the later stages of final assembly; rework, at this point, can involve disassembly of the instrument.

The Ideal Chassis

Before radically changing the construction of a chassis, we needed to think about what a chassis does electrically, and mechanically. Mechanically, the chassis ties the instrument components together. Circuit boards and electrical components are mounted on it. By its rigidity, the chassis protects these components from shock and vibration.

To the electrical engineer, the chassis is a convenient source of ground potential for circuit boards and electrical components. The chassis also provides shielding between circuit boards or circuit elements.

By considering the mechanical functions along with modern manufacturing methods we can characterize some potential ways to make an inexpensive chassis.

Molded plastic is easy to manufacture

Strictly from a manufacturing standpoint, a chassis of injection-molded plastic is attractive, and the cost of molded plastic parts is low. Many parts, such as brackets, holders, and spacers, that are added by hand during final assembly, can be molded-in as part of the chassis. Molding-in eliminates many separate parts and greatly reduces final assembly time. With this parts reduction comes a corresponding reduction of hardware.

With molded plastic, you can hold much tighter tolerances over large areas than with sheetmetal. Typically, tolerances of ±.005 inch or better are easily achieved in plastic. In contrast, ±.015 inch is difficult in aluminum.

However, an injection-molded scheme has several drawbacks:

(1) Captive hardware is almost as troublesome with a plastic chassis as it is in sheetmetal. If conventional inserts are used, human errors, such as leaving parts out of the mold and improper sonic insertion, are frequent.

(2) Most plastics, as insulators, do not make good circuit grounds. Most plastics cannot be used for electrical shielding for the same reason.

Reducing hardware

From an assembly standpoint, a chassis incorporating some type of plastic rivet, push fastener, or snap fastener for mounting circuit boards and other components is desirable. Because such fasteners generally mate with a simple round hole, there is no need to bother with any type of captive hardware. And too, final assembly is usually simplified since these plastic fasteners are installed without tools.

But plastic fasteners have several drawbacks: Connections are less mechanically secure than with screw-type fasteners. These fasteners can't ground circuit boards since they are made from plastic.

But, sheetmetal is dependable . . .

After considering these pros and cons, it was tempting to stick with conventional methods.

A chassis made from .050 inch sheetmetal is attractive for several reasons: The technology is known. Hardware is readily available and easy to install. Sheetmetal makes an excellent ground for circuit boards. Sheetmetal also makes an effective shield.

It should be noted, however, that the initial reason for this project was to address the drawbacks of a conventional chassis. Our objectives were to use best attributes of both plastic and sheet metal.

The Composite Chassis

This brings us to spotmolding on aluminum and the events that made it possible. Our basic idea was to continue using sheetmetal as the basis for the chassis. The metallic part (substrate) should, however, be very simple, nothing more than a flat sheet of .025 inch stock with punched holes (see figure 1). We decided that .025 inch sheet would be strong enough as it would be reinforced by plastic. We also concluded much of the structure in a chassis could be eliminated by using the circuit boards and cabinet for support. This substrate is then loaded, as an insert, into an injection molding machine that adds needed details, forming a composite chassis.

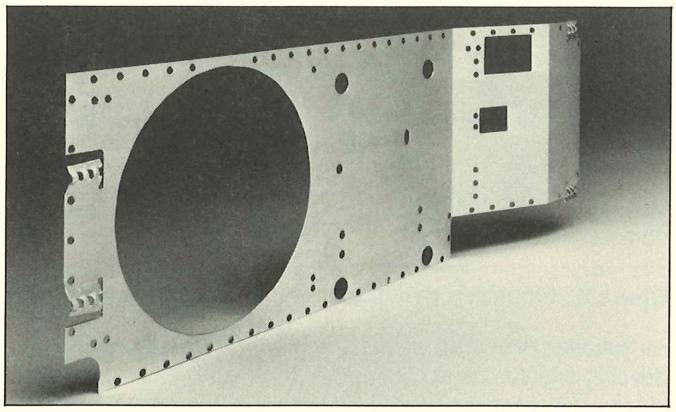


Figure 1. The aluminum substrate before spotmolding.

The benefits of this system are: (1) The simple sheet metal part can be made in one or two stamping operations, reducing costs of manufacturing considerably. (2) Since a thin guage of metal is used, the material cost is also reduced. (3) The metalworking is reduced, since there is little or no bending or welding. By using the molding machine to make all details – flanges, brackets, holders, and so forth – we get all of the benefits of an injection molded chassis.

COST COMPARISONS

	Spotmolded		Conventional	
	Tooling	Part	Tooling	Part
Chassis	75K	7.00	75K	14.40
Grommets	0	0	14K	.39
Anode Lead Clip	0	0	0	.15
Fanshroud	0	0	9K	.59
Powerswitch Holder	0	0	10K	.30
Flange Blocks	0	0	10K	1.22
Hardware	0	1.70	0	.25
Assembly of Hardware	0	1.23	0	1.89
Total Costs ($)	75K	9.93	117K	19.19
Savings ($)	42K	9.26	–	–
Savings (%)	36%	48%	–	–

Table 1. Although tooling for spotmolding costs more than tooling for conventional (all aluminum) construction, part and assembly costs are less in a spotmolded design.

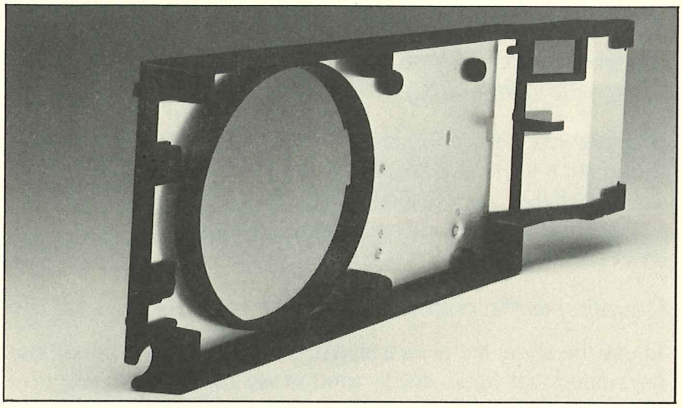


Figure 2. The spotmolded chassis showing the aluminum substrate with molded in details such as grommets, anode-lead clip, circuit board mounting details, fan shroud, casting-ground details, and structural flanges.

Composite chassis advantages

(1) Boards are shielded with the sheet metal substrate.

(2) The substrate is a source of ground potential for the circuit boards.

(3) Weight is reduced about 30% over a conventional chassis.

(4) Assembled chassis costs are reduced by up to 50% or more over the conventional chassis; tooling costs are reduced about 35%.

(5) Part count is reduced by 20% or more over the conventional chassis.

(6) With part count reduction, there is a corresponding reduction in assembly time for the chassis.

The electrical team buys in

To use this new technology, the electrical design team would have to handle grounds differently. The electrical design team agreed to not use the chassis as a ground except where absolutely needed. Instead, most grounds would be in the signal-interconnect system. Although this scheme should enhance instrument performance, it will add cost to the instrument because interconnect cables will be wider.

Chassis Development

Choosing a plastic

Choosing materials for this application required much thought. We chose 15% teflon, 20% glass-filled polycarbonate for several reasons:

Warpage – Assuming an operating die temperature around 160°F, and knowing thermal expansion of aluminum is .000013 inch per inch per degree F, we know the substrate will expand by about .0013 inches per inch when placed in the die (assuming 60°F ambient). This approximates the shrinkage of our polycarbonate, about .0015 inches per inch per degree. This similarity of shrinkage will prevent the finished parts from warping after they are removed from the die.

Storage temperatures – The coefficient of thermal expansion of the plastic is .000018 inches per inch°F. This is close enough to that of the aluminum; the finished parts should not build up appreciable internal stresses over the range of storage temperatures (–62°C to +85°C).

Structural properties – The plastic is very rigid (800 ksi modulus), strong (14.5 ksi tensile and 21 ksi flexural strength), and fairly ductile (9 ft-lb/in unnotched impact). As such, the material is suitable for this structural application. In addition, it has a UL 94-VO flame rating.

Mounting to the chassis

To use the sheet metal as a shield, a mounting detail had to be developed that would solidly ground the front casting, rear chassis to the main chassis. To do this, we slit and shaped (deformed) the edge of the sheet to form a round hole. This mounting detail is then reinforced with plastic (figure 3.). When a self-tapping screw is inserted into the detail, the metal provides electrical continuity while the plastic provides structural strength. The technique proved to be strong.

Tensile tests were performed on a sample of this detail that had a .124 inch finished hole. With a .500 inch engagement of a #6 taptite screw, the detail proved stronger than the screw during a pull-out test. Humidity or temperature did not degrade this strength.

However, although the screw can be unscrewed and reinserted at least 15 times without destroying the electrical or structural integrity of the detail, we can't recommend the detail in locations requiring more than a one-time assembly.

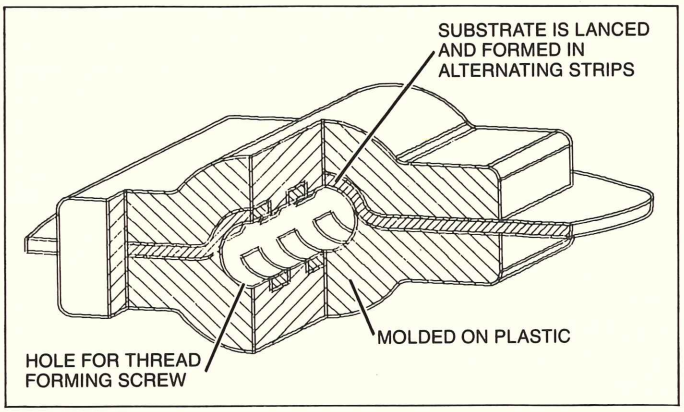


Figure 3. Detail used for grounding chassis to casting and rear plate.

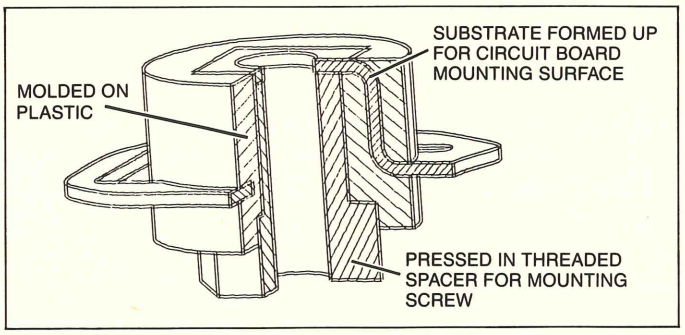


Figure 4. Detail used for mounting circuit boards where a chassis ground is necessary.

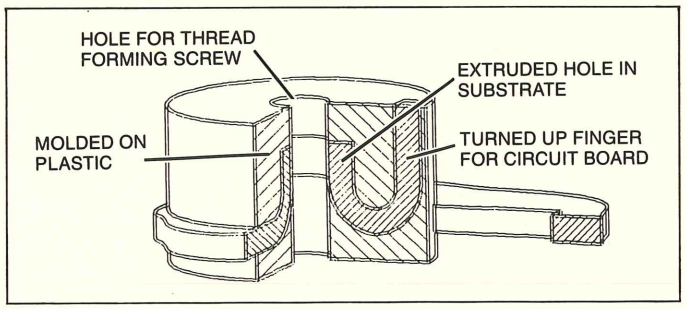


Figure 5. Mounting detail used where creep is a problem.

As the need eventually arose for a chassis ground, we had to develop a feature to accommodate this (figure 4) .In final assembly, an insert is installed in this detail.

Where plastic is stressed, creep is a potential problem. The chassis mounting points are most succeptable. Creep can be a serious problem where a ground is necessary, since gas-tight seals require constant tensile loading. Donn Alexander (627-2975) solved this problem with a detail for circuit board mounting. The detail uses a finger turned out of a .050 inch sheet as a solid surface against which to clamp the circuit board (figure 5).

We choose a fastener

The original choice for a circuit board fastener was the Ny-Latch captive fastener. However, there were problems with this system: (1) Because the fasteners were captive, circuit board installation was blind and difficult. This difficulty made it easy to catch a leg of the Ny-Latch upon insertion, which usually destroyed the fastener. (2) Since the Ny-Latch holds by friction and not by locking to the sheet, early shake and shock results were discouraging.

These shortcomings prompted development of a custom quarter-turn fastener that was estimated to cost $.05, versus $.12 for the Ny-Latch. This fastener solved all but one problem associated with the Ny-Latch – the new fastener was equally awkward to install. We chose not to use it because of this. Still, it should be appropriate for some low cost applications.

The part we are now using is a quarter-turn fastener supplied by the company that supplies the Ny-Latch. It affixes to the chassis, like the Ny-Latch; after the circuit board is placed over the fastener, a quarter turn locks it in place. This fastener costs $.10, close to the $.12 cost of the Ny-Latch, but installs easily and works well.

Cautions

Even though the shrink of the plastic differs only slightly from aluminum, the plastic will not stick to the aluminum substrate. Therefore, through-holes in the substrate must be used to fix the molded details. The details must be "backed up" to create a reinforcing pad of plastic on the opposite side of the sheet. This system allows the details to be "sewn" to the substrate.

Although the plastic and aluminum have been matched quite closely, we have experienced slight problems with oil-canning. Oil canning occured where long slots were near long runs of plastic. We eliminated the problem by moving the slots at least .050 inches away from the plastic.

Plastic reinforcements around the exposed edges of the sheet-metal are needed since the thin (0.025 inch) substrate can be damaged when dropped.

Snap-type details should be designed with great care since the plastic chosen is relatively brittle.

The thin substrate does not allow heat-sinking components to the chassis. In the absence of heat sinking, airflow and component placement must be carefully analyzed to reduce thermal problems.

Prototype Tooling Expensive

Although a composite chassis is relatively simple to prototype, substantial time is invested in preparing to make these parts. To reduce preparation, we kept the molding die simple by using few side pulls and many pass cores. Even so, our die required around 315 hours of model shop time. One factor that makes this cost tolerable is that revisions are simple to add to the die since you mold only in spots and plastic surface finish (appearance) is not critical.

The lead time for prototyping is a serious problem and can extend the schedule. The designer needs to give this detailed attention. Prototype time can be reduced with a "cut and glue" technique. This is a quick and inexpensive way to get something to look at. However, this does not give a representative sample for testing.

Other Applications for Spotmolding

During this project several potential applications of the spotmolding concept surfaced:

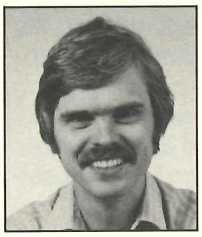
Rather than making separate parts, such as covers or plugs, which are usually installed during final assembly, mold these parts into the plastic – without any attachment to the aluminum substrate. The user (customer) could remove such parts when necessary for servicing.

It is simple to mold on "extra" parts such as special tools for service, parts used in the assembly (such as the plastic board fasteners), labels, and so forth. Such "built-in" parts provide manufacturing efficiencies and after-sales convenience.

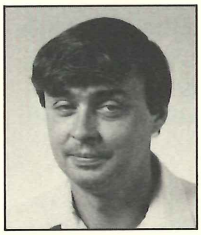
For More Information

For more information call Ken Dobyns or Jim Tsadilas, 627-2978. □

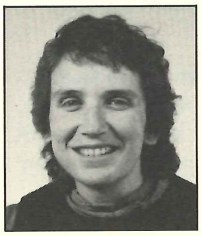
PRODUCING COLORS FROM A "MONOCHROME" DISPLAY



Philip J. Bos is the project leader for the liquid crystal color switch project. He joined Tek in 1979. He was an associate member in the Liquid Crystal Institute at Kent State University. He has a BA from Hope College and a MA and a PhD from Kent State University, Ohio.



Philip A. Johnson is a senior engineer in Color Shutter Device Engineering, part of the Display Device group. Phil joined Tek in 1964. He has a BA in physics and math from Albion College.



Rickey Koehler-Beran is an electron device process engineer in Imaging Research, part of the Applied Research Labs. She joined Tektronix in 1969. Rickey has a BS in home economics and English from the University of California, Northridge.

Rolf Vatne is a physicist manager in the Display Devices group. Rolf joined Tek in 1979 from Boeing. He has a BS in physics from the University of Puget Sound and PhD in physics from Washington State University.

Tektronix has recently developed a new display system that merges CRT and liquid crystal (LC) technology to produce color images from a "monochrome" display.

This system (shown in figure 1) generates color images by alternately displaying two different colored fields and letting the observer's eye integrate both to produce a range of colors.

How color is produced can be seen by referring to the example in the figure. In this case, the "monochrome" CRT uses a phosphor which emits both red and green light when excited by the electron beam. The resulting yellow light is passed into a pair of color polarizers. The polarizers are arranged to transmit only red polarized light along one axis and only green along the other, orthogonally oriented axis. By polarization, the initially unpolarized light is now "tagged" with color identifiers.

When viewed with a normal linear polarizer, tagged light will appear green for one polarizer orientation, red for another, orthogonal orientation. The light can range between these two colors for arbitrary polarizer orientations. (To the eye unaided by the linear polarizer, the tagged light will still appear yellow.)

Naturally, physically rotating the linear polarizer is not the preferred technique for rapidly producing color fields. It is better to rotate the polarization states of the tagged light such that either green or red polarized light is passed to the transmission axis of the final linear polarizer. This function is provided by the LC cell referred to as a λ/2 LC retarder" in the figure. The cell will either pass the light with polarization directions unaltered or rotate the polarization directions by 90° depending upon which of two states the LC retarder cell has been switched to by an applied AC voltage.

Colored images are generated by first switching the cell so that only one color, for instance green, can be transmitted by the cell/polarizer package. All the information that is to be pure green or contains green is then written on the CRT screen. Next, the cell is switched to transmit only red and all the information containing red is written.

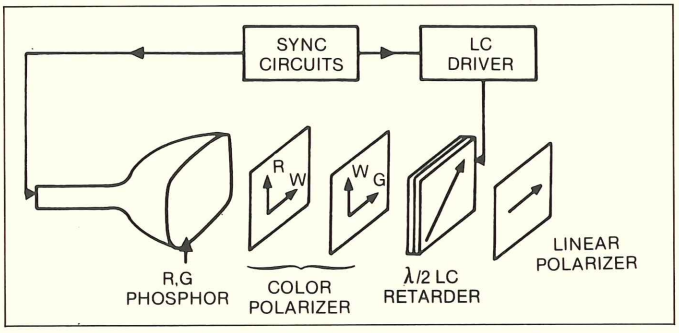


Figure 1. The liquid-crystal CRT color system. Red and green information is written on a phosphor that produces both red and green light. Color polarizers polarize each color so that they are orthogonal. The retarder rotates the polarity of the light passing through it in sequence with the color field being written. If the field-sequencing is rapid enough, the observer's eye integrates the red and green light and sees the combination. This system eliminates the inherent mechanical limitations of physically rotating the linear polarizer.

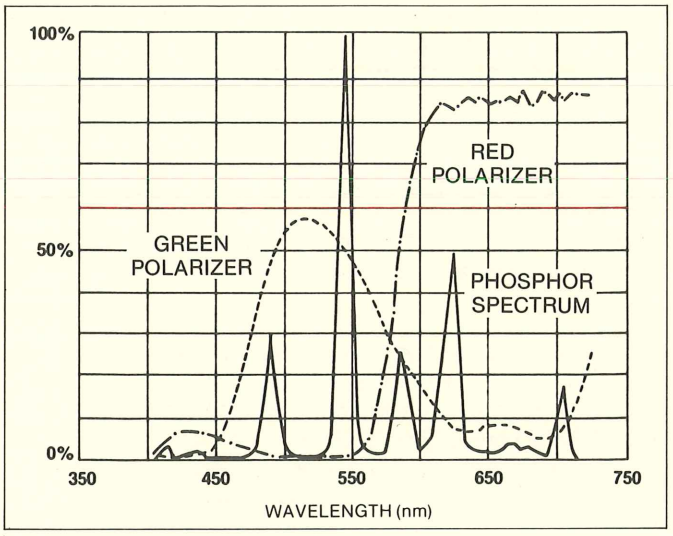


Figure 2. The polarizer transmission and phosphor emission spectra for a typical system.

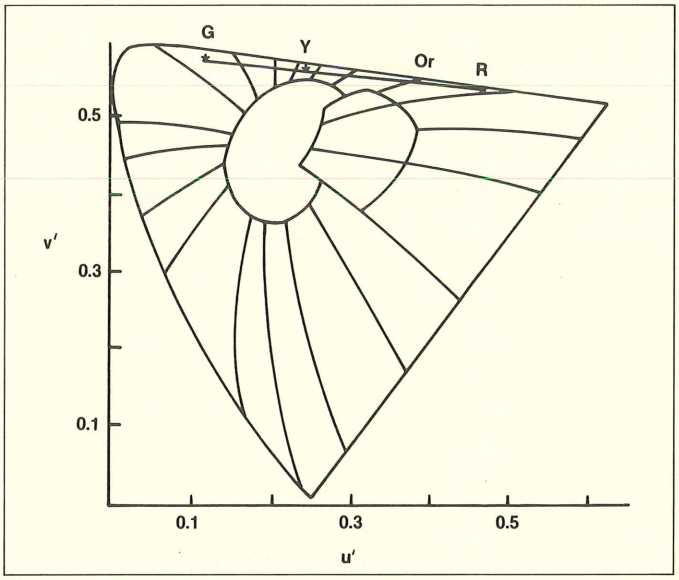


Figure 3. The color gamut achievable in a liquid crystal CRT display using the polarizers and phosphors as shown in figure 2. Field-sequential beam current modulation can create any colors on the line ranging from red to green.

If the switching is rapid and repetitive, the eye integrates the color images. Any information written in only one field will appear green and that written in the other field will appear red. Information written in both fields will appear yellow or an intermediate color depending on the relative intensities of the red and green light contained. Displays that operate in this manner and depend upon the color integrating ability of the eye are called *field-sequential color displays.*

The example described would use a matched color polarizer/phosphor combination as shown in figure 2. The color gamut of this system would extend over the range shown in figure 3. Naturally, using a different color polarizer set and phosphor mix could produce different colors.

Systems Implications for Field-Sequential Displays

A field-sequential system, such as the one described, has significant advantages relative to some color displays. Some advantages derive from the fact that a single gun addresses an unpatterned phosphor. This gun has a fixed electron-beam energy. Using only one beam and no shadow mask means that many of the difficulties associated with conventional color displays, such as misconvergence and color purity problems, are either eliminated or more easily corrected.

There are no constraints imposed by effects such as moire patterns, which are created by the electron-beam raster beating with the mask aperture pattern. The resolution and sharpness of the image equals that of a high quality monochrome display.

The liquid crystal CRT system can be applied widely. It works well for either raster or calligraphic displays, with either magnetic or electrostatic deflection systems. The ability to generate color in electrostatic systems is particularly significant. There have been few practical ways to do this until now.

The combination of linear and color polarizers not only selects colors, it improves display contrast, particularly in high ambient light. First, the narrow spectral ranges transmitted by the filter package differentiates the displayed data from the wider-spectrum ambient light. Second, ambient light reflected off the face plate is attenuated twice – once before it reflects off the CRT phosphor surface, then again on the way out. By having to pass through the package twice, CRT reflections are much reduced.

A design drawback of field-sequential operation is the need to double the scanning and Z-axis drive frequencies. However, Tek has the advanced skills needed to build appropriate circuits. Such Z-axis circuits are now used in the 4115 and other high-resolution systems. When these Z-axis circuits have been coupled with the horizontal circuits designed by Gordon Meigs, 900 by 1200 pixel displays have been shown to be practical. Vertical circuits present no significant problems.

Although the image quality is not degraded by the color switch, brightness is reduced since color is displayed with a 50 percent duty cycle; there is light lost in polarizing too. System light is about 12 percent of the monochrome CRT alone. Offsetting this, the high contrast of the colored light to the competing ambient light makes traces standout. With this contrast and better light-transmitting face plates, the system appears to "yield" about one third of the monochrome tube's light potential.

In the Tek system, brightness can be increased by increasing the accelerating potential, the beam current, or both. Increasing the accelerating potential shrinks the beam spot, producing very crisp and legible images.

In perspective, the shadow mask blocks much of the beam power in a shadow mask tube; and the tube does not have the inherently high contrast of the liquid crystal CRT.

In summary, the excellent resolution, purity, convergence, and contrast of the LC/CRT display more than compensate for the extra design effort needed.

The Color Switch

The color switch consists of colored polarizers and a liquid crystal device that can rotate the polarization of incident light. Tektronix has improved these components to provide the best system available.

A polarizer is made by aligning dye molecules that absorb light along only one axis. Together with a major supplier of polarizers, we have developed new dyes and alignment means that enable us to produce high quality polarizers of almost any color. Colorimetry measurement and analysis equipment have been developed to enable us to match the polarizers with Tek developed phosphors. This allows the system designer to select from a wide range of colors those best for the application.

Although the liquid crystal device that rotates the polarization is very simple, it represents some "firsts." The device uses the remarkable properties of a liquid crystaline material to switch between a state of half-wave optical retardation to a state of no retardation.

In the cell's half-wave retardation state, incident light is resolved into two components; each travels through the device at different velocities. The velocity difference and the device thickness are chosen so as to phase shift the two components by one-half wave.

If linearly polarized light is incident on the cell (as shown in figure 1) the interference of the phase-shifted components leaving the cell linearly polarize the light perpendicular the incident direction.

The conventional construction of a liquid crystal device that does this is shown in figure 4. The device consists of nothing more than two pieces of ITO-coated glass that have been also coated with polyimide as the liquid crystal alignment layer. (ITO is a transparent conductor.) The pieces of glass are spaced about five microns apart and a liquid crystal material placed between them.

Figure 5 shows an end-on view of the molecular configuration in the cell in its on, relaxing, and off states. In the off state, the molecules are roughly parallel to the surface and if the cell thickness is chosen properly the device is a half-wave optical retarder. In the on state, about 20 volts is applied to the transparent ITO conductors to produce an electric field within the cell that aligns the liquid crystal molecules as shown.

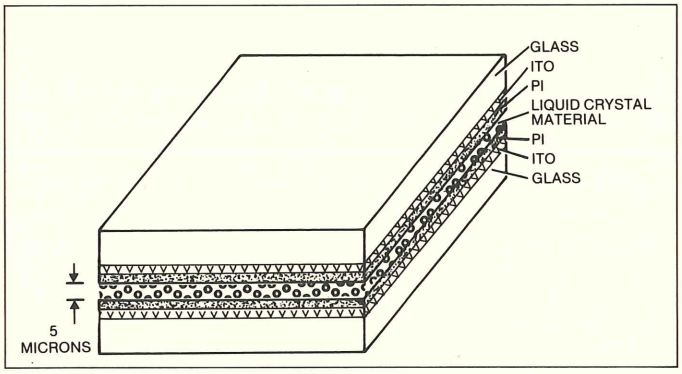


Figure 4. Liquid crystal cell construction.

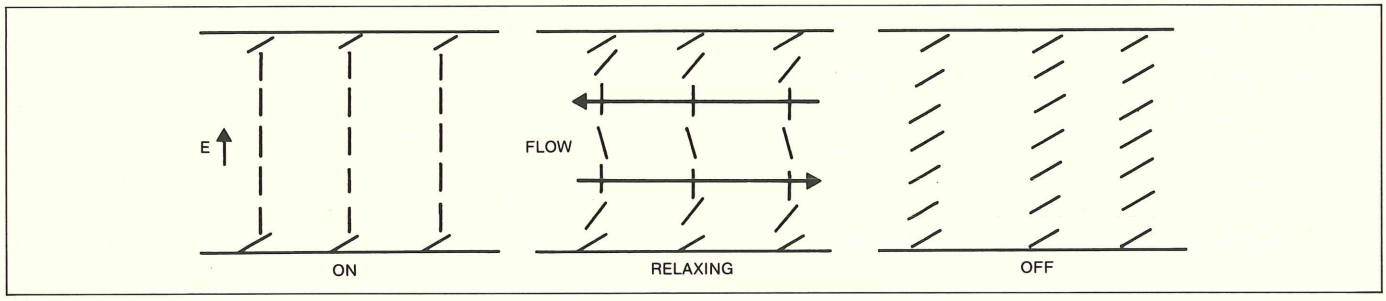


Figure 5. The back-flow effect in a parallel-aligned LC cell. When the electron field is removed, the flow of the relaxing molecules creates a viscous torque that prevents fast relaxation to an off state.

In the aligned state, the cell does not optically retard and does not rotate light polarization. However when the applied voltage is removed, the molecules tend to relax back to the off state, but unfortunately in doing so fluid flow patterns within the cell (shown by arrows) slow the relaxation. This slow relaxatior. delays the switch to the off state, causing an undesirable effect called optical bounce.

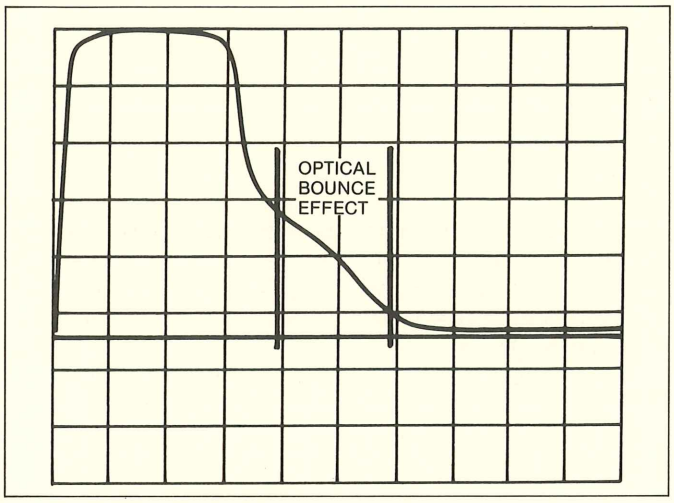


Figure 6. The optical bounce effect in a parallel-aligned LC cell. Note the initial fast decay – a desirable characteristic – slows in optical bounce region.

This problem has been solved with the π-cell. In this device, the alignment of the device is modified as shown in figure 7 so that the flow in the relaxing cell is not a problem. The result is a device that can switch between optical states in one to two milliseconds, and fulfills the requirements of the polarization rotator in the color switch.

Future Work

The π-cell can be used in systems which are capable of generating both limited and full-color displays. While present efforts are aimed primarily at producing cost-effective high-resolution limited-gamut color displays, full-color systems have been and will continue to be investigated. These systems can produce very high performance and may eventually prove to be very formidable competitors in applications which are currently dominated by rastered shadow-mask displays.

Tektronix has had a dominant position in the graphics market achieved with novel technologies such as the DVST, color write through systems, and others. The liquid-crystal CRT system may well prove to be equally important.

For More Information

For more information, contact Rolf Vatne, 627-6702. □

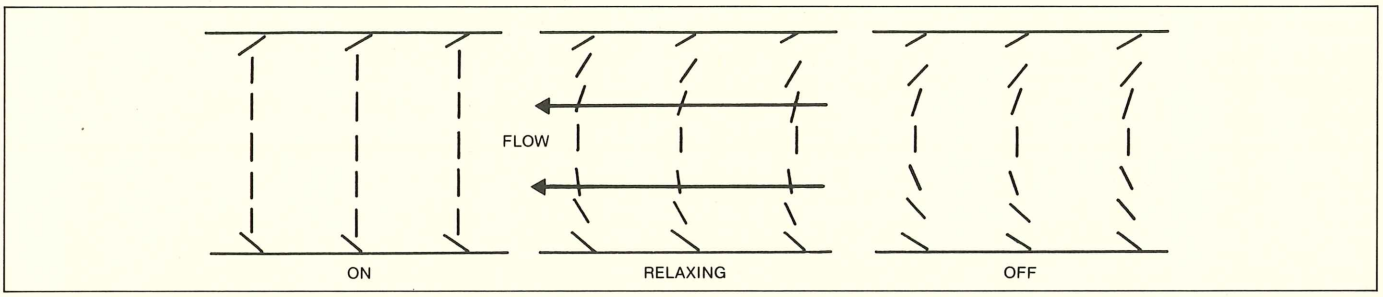


Figure 7. Optical bounce is "cured" by using a π-cell. In a π-cell, torque on the central molecules due to flow is zero. The result is fast relaxation and, therefore, no optical bounce.

THE QUADRUPOLE LENS JOINS LONG LINE OF CRT IMPROVEMENTS

Norm Franzen is an electron device designer in Display Device Engineering. Norm joined Tek in 1973. He had earlier taught math at Oregon State University. He has a BS in math from OSU and a PhD in math from the University of Colorado.

Bo Janko is a manager in the Applied Research Labs. He joined Tek in 1968 as a physicist and has helped develop storage and conventional CRTs and other electron devices. He has written several computer programs that are the basis for CRT CAD at Tek.

CRTs In Oscilloscopes

Although relatively ancient in concept, the modern CRT is the primary signal-detection and output port for the modern oscilloscope. Flat panels, electroluminescence, and LEDs have challenged but are unable to replace the CRT. The CRT, itself, is a remarkable device. As circuit technology has advanced, the CRT has not stood still.

Inexpensive logic has allowed us to incorporate in portables features that were previously practical only in the more expensive lab scopes. Three of these features are alphanumeric readout, display cursors, and autofocus. In addition, circuit designers have been able to reduce costs by driving the CRT directly from integrated circuits. System designers have been able to reduce size and weight without compromising the display size or heat-dissipation.

Let's consider for a moment what these achievements mean for the CRT designer.

Roughly speaking, the instrument's bandwidth dictates how fast the fastest sweep rate must be. Sweep rate, in turn, determines the trace-brightness or writing-speed requirement. Secondly, alphanumeric CRT readout requires fine spot size and no visible jitter. The compactness of the instrument package is limited directly by the CRT length, as well as indirectly by the power needed to drive the deflection system. More power requires larger transformers, less dense circuitry, and more volume to dissipate heat.

Consequently, for a given bandwidth and a specified display size CRT designers focus on four parameters:

1. Trace brightness or writing speed
2. Trace quality (spot size)
3. Tube length
4. Power consumption

These four parameters interrelate complexly. Trace quality is influenced by such CRT factors as lens aberrations, space-charge repulsion within the beam, deflection defocusing, and the magnifications of the optical system. These CRT factors, in turn, interact with brightness, tube length, and power – parameters 1, 2, and 3. Therefore, the CRT designer always finds optimization difficult. These problems have driven the CRT to take another step upward. This step is the new quadrupole scan expansion CRT[1].

The Evolution of the CRT

Figure 1 shows a CRT as the output port of a system, interfacing to X and Y deflection amplifiers and to a Z-axis beam-intensity modulating circuit. The focus system and low- and high-voltage power supplies are not shown. This simple *monoaccelerator* CRT closely resembles the earliest oscilloscope CRTs, which used only a beam source that also accelerated the beam toward the phosphor target, an axi-symmetric (round) focus lens, and two sets of simple deflection plates.

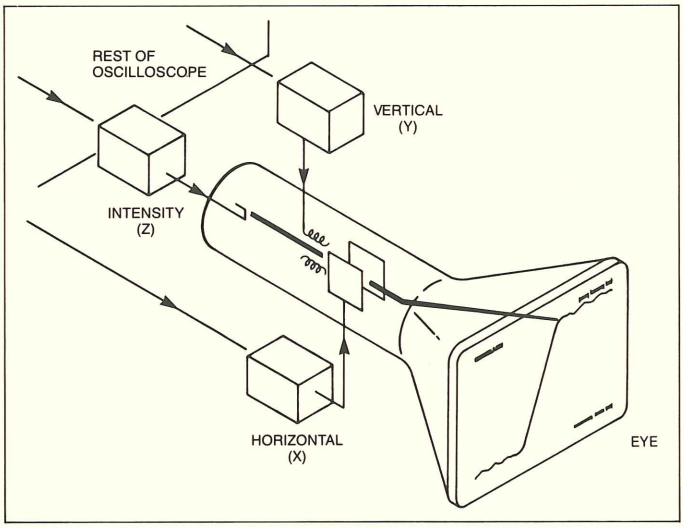


Figure 1. The CRT as part of a system.

Although monoaccelerators can produce excellent traces, writing rate can be a problem. To display fast signals, the beam energy must be increased to the point where the deflection sensitivity becomes very poor. Consequently, deflection requires too much power. These problems led to the introduction of the post-deflection acceleration (PDA) designs. In these designs, the beam is accelerated only modestly before deflection. This low-energy beam is again accelerated following deflection. In this way, higher writing speed is attained.

One post-deflection scheme, the helix PDA, was used by Tek in the late 50s and 60s. Helix PDA use was common when Tek started using it in oscilloscopes.

In this type of PDA CRT, a resistive helix distributes the accelerating voltage so that while the writing speed is substantially increased, the deflection sensitivity is more or less preserved; in some cases, it drops, but not severely.

In the 60s, deflection sensitivity in the helix scheme was improved by shaping the accelerating field with an electron-transparent electrode. This electrode was often a grid of fine metal wire, hence the name "framegrid PDA" was applied to these improved tubes. In 1965, Chris Curtin developed the first truly high performance CRT for a Tektronix portable, the 453.

In the late 60s, CRTs using a fine metal mesh as a lens to shape the accelerating field were introduced; these came to be known industrywide as "mesh scan expansion CRTs."

Scan expansion designs use a post-deflection lens to magnify in both axes as much as three times. Because deflection system power is proportional to the square of the electron energy in the deflection region and inversely proportional to the square of the scan magnification, designs using both scan expansion and post-deflection acceleration enjoy both improved deflection sensitivity and higher writing speed.

The Mesh Scan Expansion CRT

The mesh PDA CRT (figure 2(A)) has a final divergent lens formed of a very fine wire electroformed mesh. The beam passes through this mesh. After passage, the beam is deflected away from the long axis by fields formed between the mesh and the high-voltage conductor on the wall of the CRT. These fields magnify the scan up to three times. This form of scan expansion has enjoyed great success over the past decade, and has become almost universal in high-performance scopes.

In spite of this success, CRTs employing mesh technology have serious drawbacks:

1. The mesh intercepts and scatters the beam.
2. The mesh emits secondary electrons and produces the phenomenon of mesh halo around the spot. (Unless it is coated with MgO, which partially relieves the problem.)
3. The mesh is easily contaminated by small particles during manufacturing, causing defects visible in the display.
4. Horizontal sensitivity is difficult to increase.

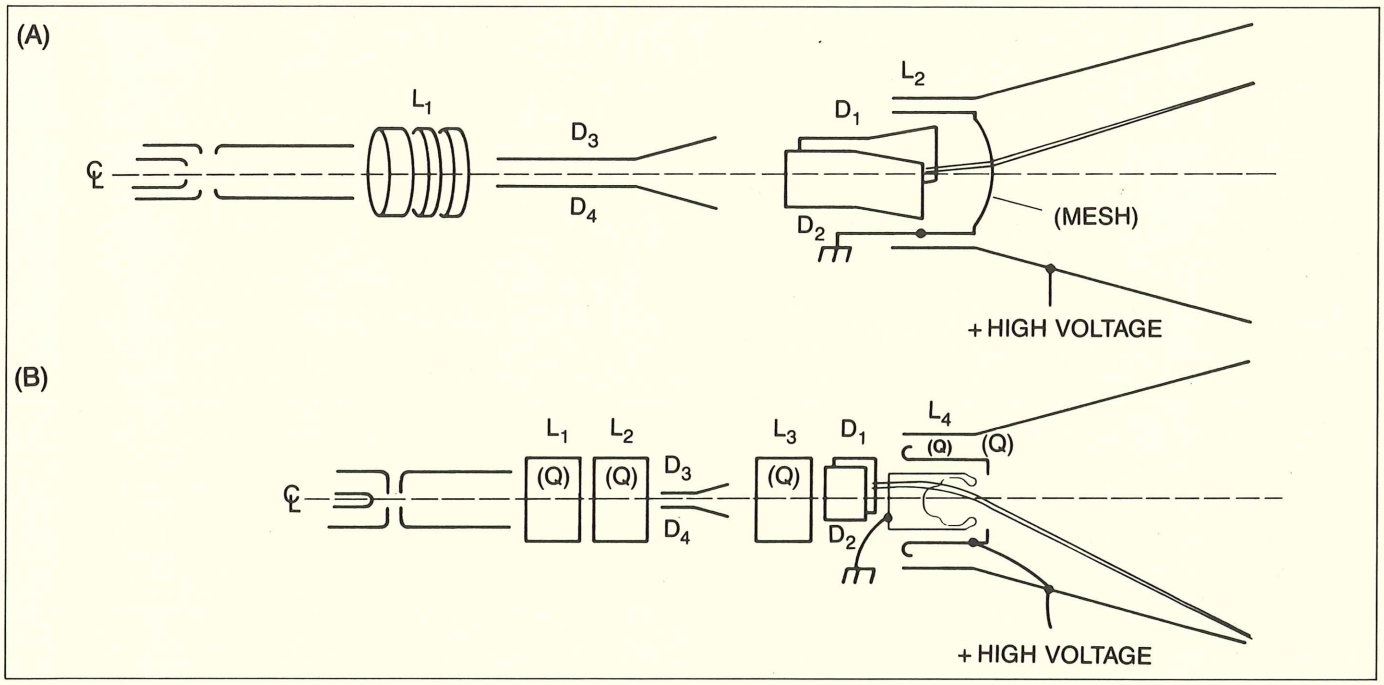


Figure 2. Schematic diagrams of (top) the conventional mesh CRT, and (bottom) the new quadrupole meshless scan expansion (MSE) CRT.

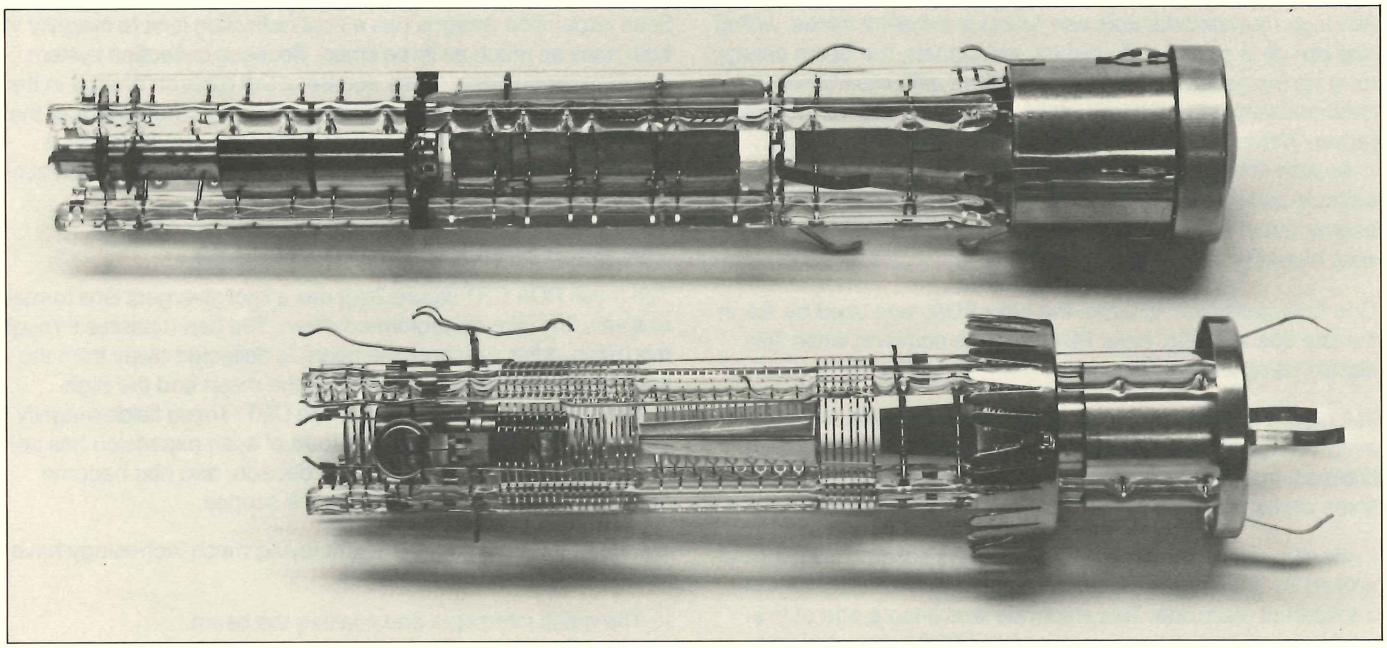


Figure 3. The MSE system (bottom) offers more scan expansion than a conventional mesh system, allowing shorter deflection plates and a shorter overall gun for the same performance level.

5. The horizontal deflectors have fairly high capacitance.
6. Most important, the deflection system is not sensitive enough to be compatible with high-speed IC drivers.
7. Finally, due to space-charge repulsion in the beam, at high Z-axis drive the spot area increases more rapidly than the beam current (the writing speed falls).

All these problems are very difficult; in fact, very little further progress is possible.

In the early 70s, while the mesh was still novel, the manufacturing problems associated with mesh burrs and the mesh halo were already strong motives to search for a better scan-expansion technology. Recently, the driving forces of costs and IC compatibility, and those mentioned earlier, have added impetus.

The Search for a New Approach to Scan Expansion

Keeping high-performance portable CRTs in mind, let's look at the two alternatives to the dome PDA mesh.

All axially symmetric lenses not employing a mesh must cross the scan in both axes. This not only makes attaining good sensitivity in both axes impossible without using extremely high scan magnification, it also leads to other problems. Thus, these lenses need not be considered further.

The only other alternative is a quadrupole system. In a quadrupole (figure 4) the scan is converged towards the axis in one plane (A) and diverged away from the axis in the other (B). The crossection normal to the center axis of the lens (C) shows the classic hyperbolic-shaped equipotential lines.

In 1971, Martin and Deschamps[3], at Thomson-CSF, introduced a short 11.5-inch scan-expansion CRT. This CRT employed two quadrupoles. One quadrupole was placed between the two sets of deflectors, and the second was located just ahead of an accelerating slot-aperture lens. The aperture lens exits into high-voltage post-acceleration space.

The two quadrupoles together develop scan expansion in both axes, and this scan expansion is further enhanced by the unique design of the accelerating slot-lens. This design approach, however, is difficult to model as the field of the accelerating slot lens is difficult to compute.

In 1978, Odenthal and Hall, at Tektronix, introduced the box lens[4]. This quadruple scan-expansion lens was used in a mono-accelerator CRT. Although the box-lens can be made to operate in a PDA mode, the system is too large and complex for portable oscilloscope applications.

The Klemperer Lenses

In 1970s, the meshless scan expansion (MSE) concept that appeared promising was described in the textbook of 0. Klemperer[5] published in the 30s. The lenses in figure 5A and B closely resemble the two proposed by Klemperer. The one in 5A is called the in-line lens, and the bottom one the low-voltage profile lens, or LVMSE for short. Both lenses are bipotential accelerating quadrupole lenses that act on the scan in a way very similar to the action shown in Figure 4.

The configuration of the in-line lens corresponds to a classic electrostatic field problem. In this case, the field can be obtained by solving LaPlace's equation in cylindrical coordinates by the separation of variables method. This solution leads to a sum of terms of the form $I_m(kr)\cos(m\theta)\cos(kz)$, where $I_m(x)$ is the modified Bessel function. Because these lenses have two planes of symmetry, only terms in even values of m appear. The resulting series is the well known Fourier-Bessel expansion[6].

From these earlier works, we developed an extensive software package to model Klemperer lenses of both types. Because Fourier methods alone will not solve the second class of Klemperer lenses, relaxation methods in cylindrical coordinates were used to calculate the field. The Fourier-Bessel expansion was then used to analyze the field near the center axis of the lens. Something in excess of 20,000 lines of FORTRAN code were written to investigate these interesting structures. This effort lead to the new quadrupole MSE CRT design[7,8], which is discussed next.

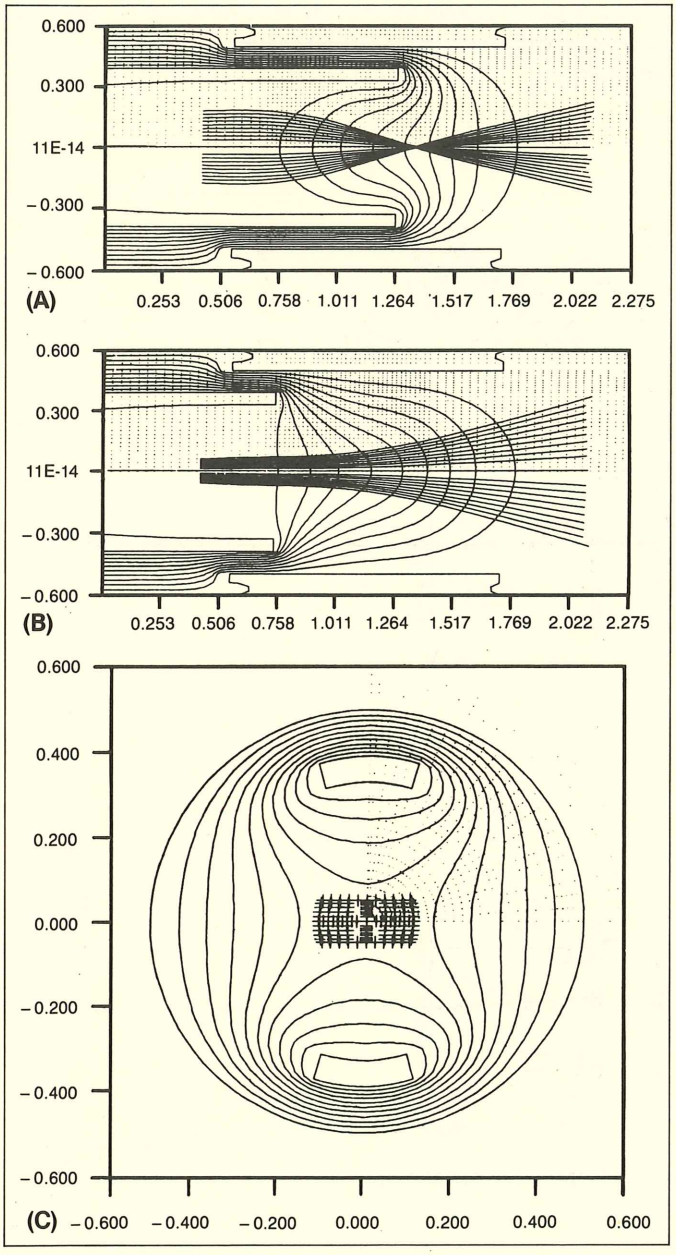


Figure 4. These computer-plotted diagrams show the action of quadrupole lenses in (A) vertical plane, (B) horizontal plane, and (C) cross-section of lens. In a quadrupole, the scan is converged towards the axis in one plane (A) and diverged away from the axis in the other (B). The cross-section normal to the center axis of the lens (C) shows the classic hyperbolic shaped equipotential lines.

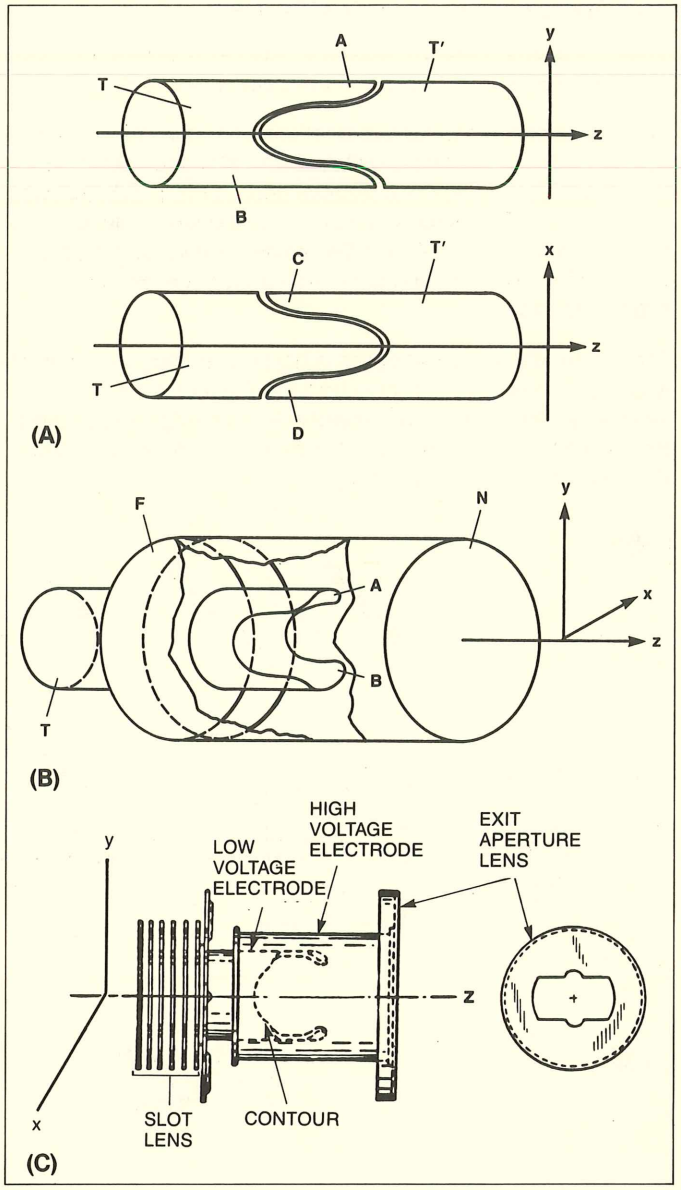


Figure 5. (A) The in-line Klemperer lens and (B) the type II Klemperer (low-voltage profile) lens. Klemperer described these lenses more than 40 years ago.[5] (C) The new low-voltage MSE configuration.

The Tektronix Quadrupole MSE CRT

The new Tektronix Quadrupole MSE CRT architecture is shown in figures 2(B) and 3(B) and in more detail in figure 6.

Figure 2(B) shows the relative positions of the two focus quadrupoles (Q1, Q2), the vertical deflector (D3, D4), the interdeflector quadrupole (Q3), and the horizontal deflector (D1, D2), followed by the new MSE lens (Q4), which is itself a quadrupole. Q1 and Q2 are paired, as are Q3 and Q4. While Q1 and Q2 are used primarily for focus, Q3 and Q4 together produce the desired scan expansion.

The action of quadrupole optics is best understood by separately studying how they effect the beam in the X and Y planes of symmetry. This action is displayed in figures 6(A) and (B), the Y-axis being the vertical plane of symmetry and the X-axis being the horizontal plane of symmetry.

Beginning with Q1, the behavior alternates between convergence and divergence in each plane of symmetry. In normal operation, the voltages of Q3 and Q4 are static, while those of Q1 and Q2 may be varied to maintain focus as the beam intensity changes. The field of the Q4 lens is roughly twice as strong in the horizontal plane as it is in the vertical. To gain sufficient vertical scan expansion, the Q3 lens is oriented to assist the vertical deflector and Q4 in crossing the scan through the axis at a sufficient angle.

A second important feature of this quadrupole configuration is that the beam is not compactly focused until it reaches the high-voltage space. Wide beams are less affected by space-charge repulsion.

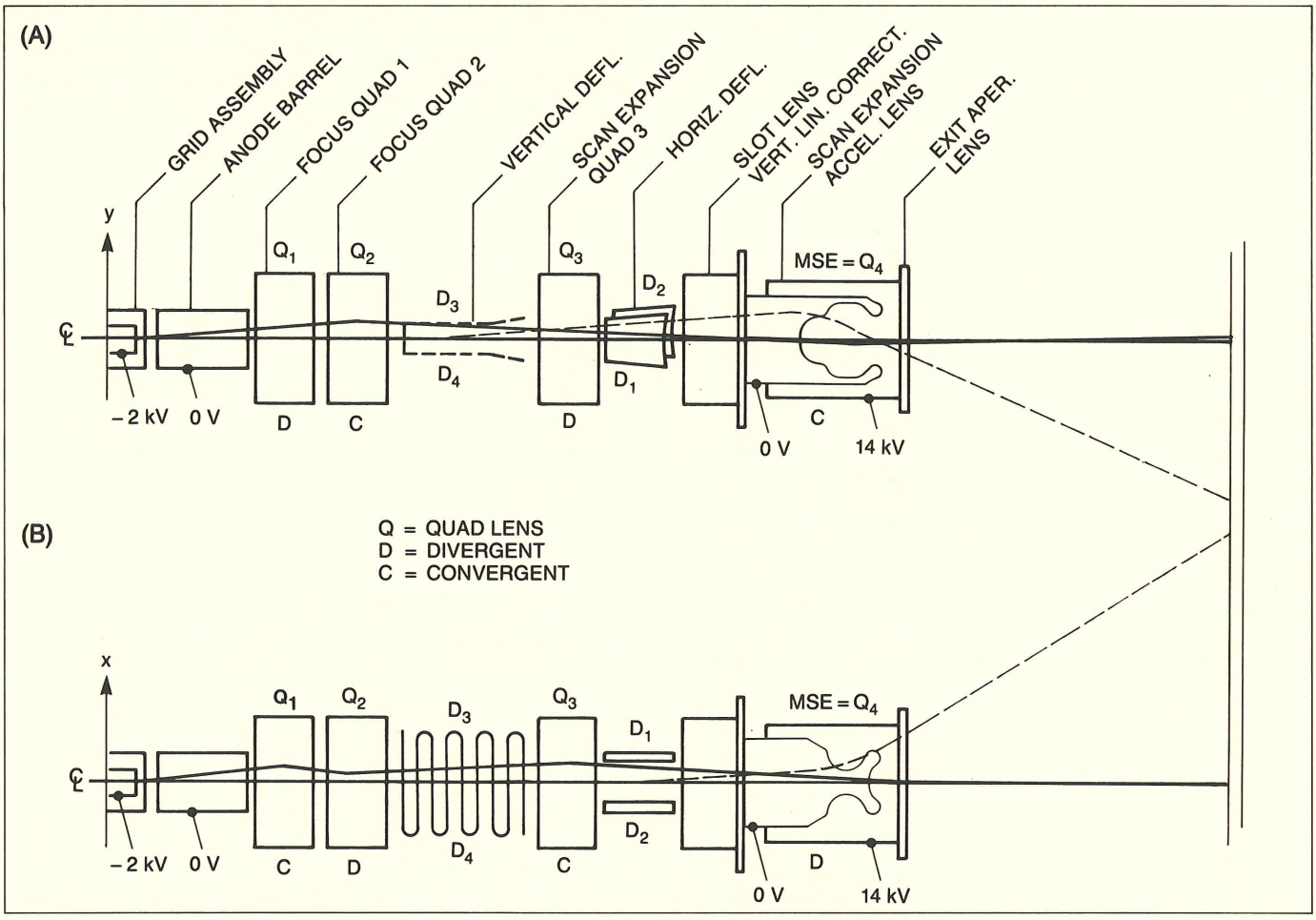


Figure 6. Schematic diagrams of MSE CRT: (top) vertical axis; (bottom) horizontal axis.

Technological Features of the Tektronix Quadruple Lens CRT

LVMSE lens

The contoured inner electrode shown in figure 5(C) is shaped to tailor the geometry and linearity of the display. Although this lens is predominantly a quadrupole, it also contains higher-order multipole elements, such as octopole (m = 4) and dodecapole (m = 6). Without these corrective elements, the display would be badly pincushioned. The Fourier-Bessel expansion, therefore, must include terms in cos(mθ) for m = 0,2,4,6.

Figure 4 shows the distribution of equipotentials and the action on the scan in each axis. The lens has a horizontal focal length of about 0.4 inch and a vertical focal length of about 0.8 inch. The scan is expanded in quadrupole fashion, magnified 3.5X vertically and horizontally. At the same time, the electron beam is accelerated from 2000 volts to 16,000 volts.

Other important features of the MSE lens are that it is lightweight, very rugged, and simple to manufacture from a piece of stainless-steel tubing. After forming, the part is conditioned to withstand high-gradient fields. The result is an inexpensive high-quality lens that can survive high mechanical shock. Because the lens is small (approximately 2 inches in length and 1.5 inches in diameter) and is a simple bipotential system, it is excellent for portable applications.

Meanderline deflector

Figure 7(A) shows the unique Tektronix patented meandering-line deflector[9]. This deflector has a bandpass adequate for at least a 400-MHz applications. It also possesses the unusually high impedance (for a meanderline) of 335 ohms (side-to-side). It is etched in the flat from a single piece of stainless steel (figure 7(B)), formed at rodding, and held firmly in the glass rods to provide a lightweight, very rigid, and shock-resistant deflector. Compared to the helical deflector subassembly shown in figure 7(C), it is very inexpensive.

Snubber system

Another unusual feature of this CRT is the unique front snubber system that cradles the gun within the glass funnel. This snubber permits very little gun motion; shocks in excess of 150 g will not fracture the rods, funnel, or feedthroughs.

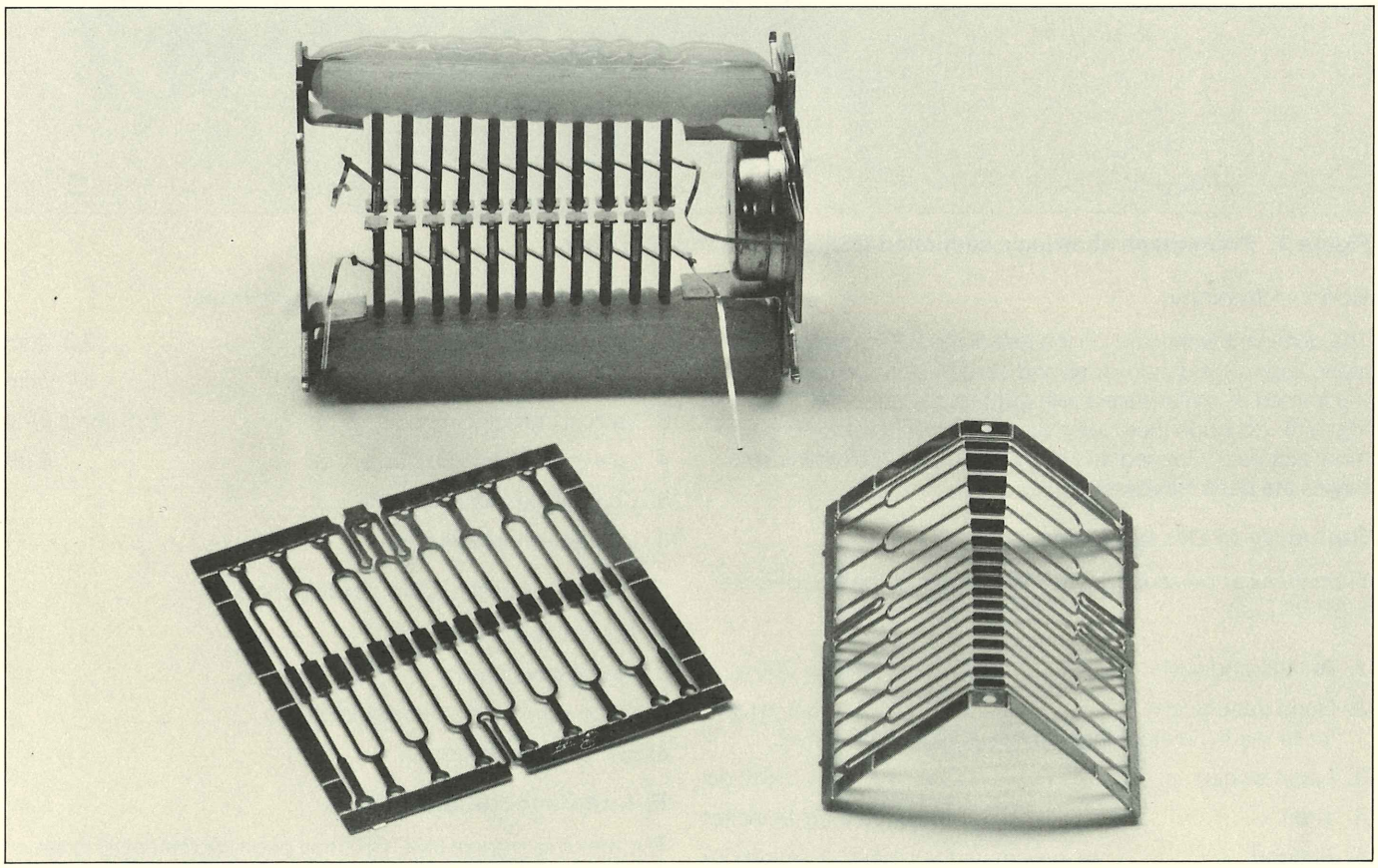


Figure 7. A meanderline in the flat (bottom left), the formed meanderline (bottom right), and a helical deflector (top).

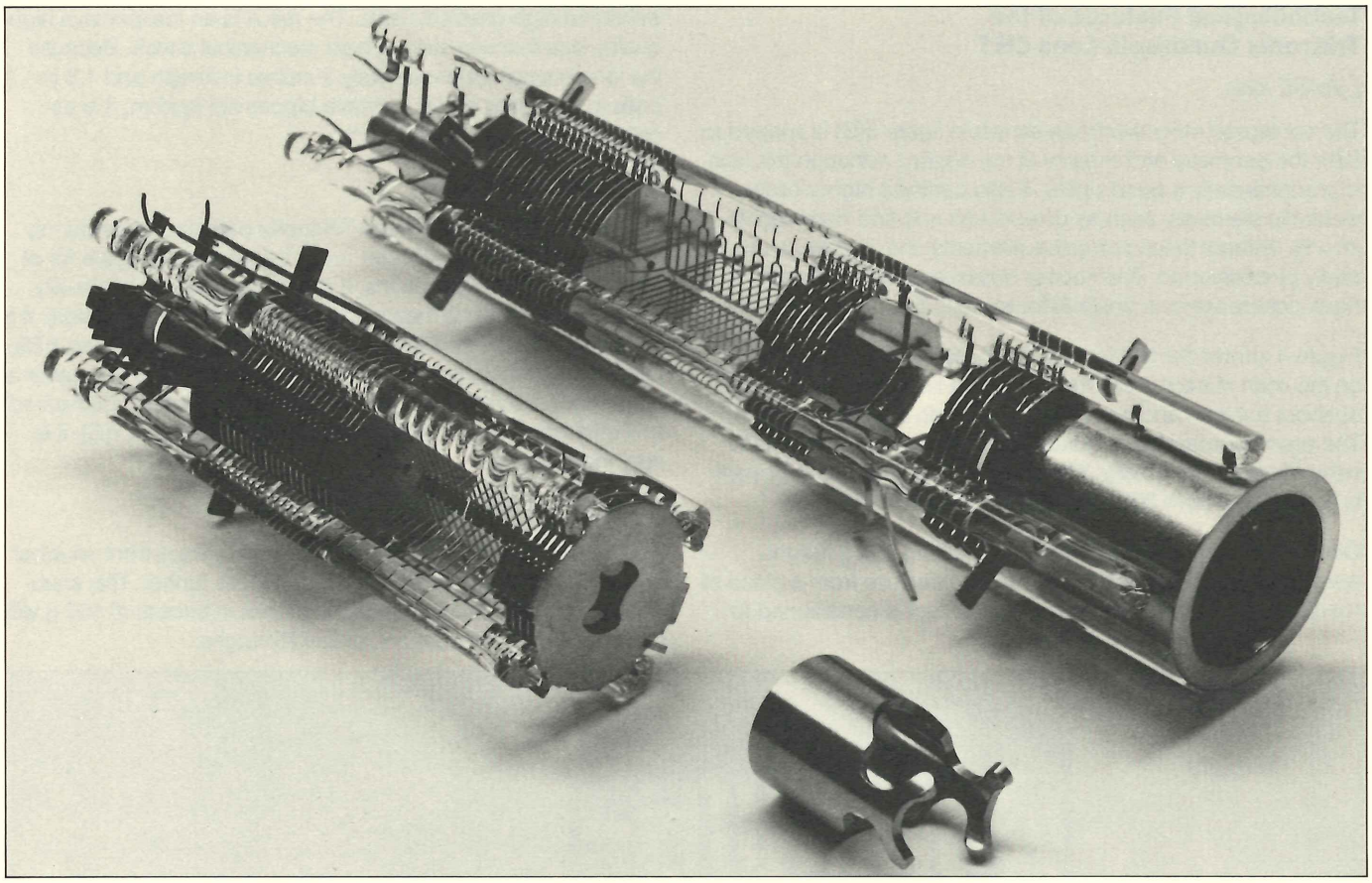


Figure 8. Photograph showing a sectioned MSE gun and the MSE lens.

Wafer technology

The dominant technology in the rest of the CRT is wafer-lens technology. The quadrupoles and several other components are formed as metal wafers with appropriate apertures (see figure 8). Although there are many wafer parts, wafers can be more accurately formed and aligned. Automated forming also makes the parts inexpensive.

Summary of Design Goals

From the user perspective, the key features of the Quadrupole MSE CRT are:

1. Broad bandwidth . . . . . at least 300 MHz
2. Good trace quality . . . . . 8-9 mil spot (crisp trace, no more than 30 mils at high Z-axis drive)
3. Large screen . . . . . 8 × 10 cm
4. Short . . . . . no more than 14 inches
5. Rugged . . . . . survives more than 150 g, 11-ms shock
6. High writing speed . . . . . WSI at least 3.0
7. CRT readout capability
8. Autofocus w/intensity

Features of interest to the circuit designers are:

1. Vertical deflection sensitivity . . . . . 2.3 V/cm
2. Horizontal deflection sensitivity . . . . . 3.7 V/cm
3. Vertical deflector impedance . . . . . 335 ohms (S-S)
4. Low capacitance D1D2 . . . . . 5 pF
5. Compatible with IC drivers
6. Low power consumption

Features of interest to CRT manufacturers:

1. Amenable to automation
2. Inexpensive parts
3. Good scheme for part alignment
4. No complex processes.

Future Expectations

The new quadrupole MSE CRT has been implemented in the 2400 family of oscilloscopes. (See "High-Speed Monolithic Horizontal Amplifier . . .," *Technology Report,* June 1983). Most of the design goals have been met in this application. It is expected that even better results will be achieved with this new technology. The quadrupole lens should replace mesh scan expansion in most real-time waveform CRTs. □

Elementary Design Rules

B = power density in beam (writing speed or trace brightness)
= energy/unit area/unit time
$\sim$ (beam current) $\times$ (accelerating voltage)/(trace width)
$= I_b \times V_p / T_w$

V_d = deflection voltage required
$\sim$ (gun voltage)/(scan magnification)
$= V_g / M$

P = power required by the deflector
= (deflection voltage)^2/(impedance)
$= V_d^2 / Z$
$\sim (V_g/M)^2$

Fourier-Bessel Expansion

$$V(r,\theta,z) = \sum_{k=0}^{\infty} \sum_{m=0}^{\infty} Cmk\, I_{2m}(\hat{k}r) \cos(2m\theta) \cos(\hat{k}z)$$

where:

R = radius at which boundary values $V(\theta,z)$ hold
L = length of field region where symmetry conditions $V(\theta,L-z) = V(\theta,z) = V(\pi-\theta,z)$ are assumed
$I_m(r)$ = modified Bessel function of order m
$\hat{k}$ = $(2\pi/L)k$
$C_{mk} = (1/N_{mk}) \int\int V(\theta,z) \cos(2m\theta) \cos(\hat{k}z)\, d\theta\, dz$
$N_{mk} = 4\pi^2 I_{2m}(\hat{k}R)$

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1. B. Janko, U.S. Patent No. 4,134, 479.
2. J. Hawes and G. Nelson, "Mesh PDA Lenses in Cathode-Ray Tubes," *Proc. SID,* Vol. 19, No. 1, 1978.
3. A. Martin and J. Deschamps, "A Short-Length Rectangular Oscilloscope Tube with High Deflection Sensitivity by an Original Technique," *Proc. SID,* Vol. 12/1, 1971.
4. C. Odenthal, "A Box-Shaped Scan-Expansion Lens for an Oscilloscope CRT," *SID Digest,* 1977.
5. O. Klemperer, *Electron Optics,* Cambridge Univ. Press, 2nd ed., 1953.
6. J.D. Jackson, *Classical Electrodynamics,* John Wiley and Sons, 2nd ed., 1975.
7. Janko, Franzen, Sonneborn, "New CRT Architecture with Meshless Scan Expansion," *SID Digest,* 1983.
8. N. Franzen, "A Quadrupole Scan-Expansion Accelerating Lens System for High-Performance Oscilloscopes," *SID Digest,* 1983.
9. Tomison, Janko, Bostwick, Silzars, U.S. Patent No. 4,207,492.

PAPERS AND PRESENTATIONS

The table below is a list of papers published and presentations given during recent months.

While providing recognition for Tektronix engineers and scientists, the presentation of papers and articles contributes to Tektronix' technological leadership image.

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JUNE

TITLE	AUTHOR	PUBLISHED	PRESENTED
Wire-OR Logic on Transmission Lines	John Theus	**IEEE Micro**	
Analytical Model and Characterization of Small-Geometry Devices	Tad Yamaguchi Seiichi Morimoto	**IEEE Transactions on Electron Devices**	
Developing Reconfigurable IEEE-488-Based Test Systems	Nicholaas Gerbracht		ASQC Meeting, San Francisco, CA
Developing Reconfigurable IEEE-488-Based Test Systems	Nicholaas Gerbracht		Technology Transfer Society Meeting, Los Angeles, CA
Solid Modeling in the Design Process	Larry Eisenbach		SDRC Users Meeting, Chicago, IL
A Turnkey Alternative	Jay Clark		National Computer Graphics Association (NCGA) Conference, Chicago, IL
Testing Fiber-Optic Links	Richard Osborn		Expocon '83, Boston, MA

JULY

TITLE	AUTHOR	PUBLISHED	PRESENTED
Ergonomics of Instrument Design: Effective Use of Color	Gerry Murch	**Electronics Test**	
Small Logic Analyzers from Sony/Tek Pack High Performance	Russ Anderson	**Electronic Design**	
Thin-Film Analytical Methods	Gary McGuire		UCLA Short Course
ECB vs. Ceramic Hybrid in SMT	Tom Kahrmann		Surface Mount Technology Fair, Wilsonville, OR
Product Cleanliness: Contamination Control	Nancy Townes		Institute of Environmental Sciences Northwest Chapter Seminar, Seattle, WA

AUGUST

TITLE	AUTHOR	PUBLISHED	PRESENTED
An Industry/University Exchange Program	Barry Ratihn Ruth Tallman		University of Portland CAD/CAM Exchange
LWT Resistor Design and Circuit Considerations for Precision Components	Wes Mickanin Clayton Mohr		Midwest Symposium on Circuits and Systems, Pueblo, Mexico
A Dynamically Precise, 50-MHz, 12-Bit DAC Using Laser Wafer Trimming	Stewart Taylor Pat Hanlon		Midwest Symposium on Circuits and Systems, Pueblo, Mexico

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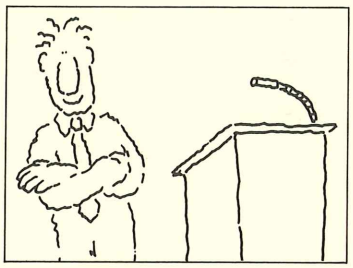

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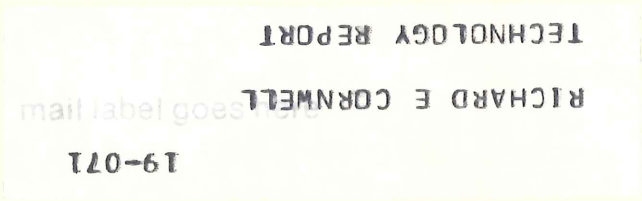

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