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S-3270
Automated Test System

S-3270 DEVICE TESTING FUNDAMENTALS

INSTRUCTION MANUAL

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SECTION I

HARDWARE OPERATING DESCRIPTION

What Is The S-3270?

The S-3270 is an automated testing system especially designed to test fast digital devices. It is used to perform functional and parametric tests on devices such as circuit cards, hybrid modules, shift registers, LSI memories, etc. In general, the devices are digital; however, some linear devices requiring digital control can also be tested. It is an automated system because all tests are performed under program control. The TEKTEST III software package provides this control.

The following section is a discussion of the S-3270 hardware to help programmers better understand the description of the test commands.

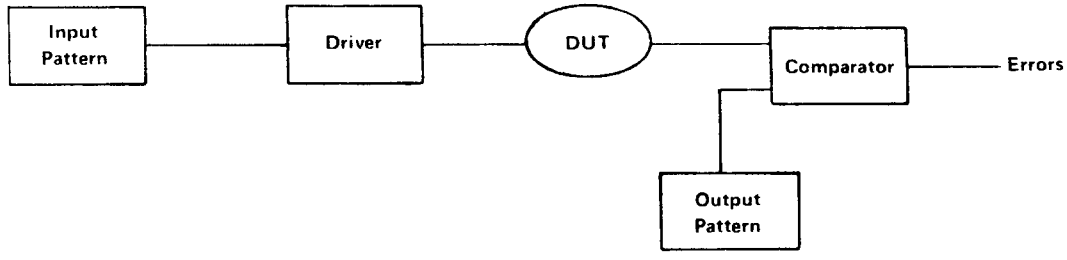
Functional Testing vs. Parametric Testing

Functional testing generally means simulating actual operating conditions on a device or circuit, and checking that the device is operating correctly. These tests usually involve checking the response of the device to a pattern of logic levels on a pass/fail basis. Parametric testing is measuring specific DC and time-interval parameters of the device.

The S-3270 is both a functional test instrument and a parametric test instrument. It performs functional tests at rates of up to 20 MHz, and parametric tests at rates of up to 250 Hz.

Functional Testing

Functional testing consists of forcing the inputs of the device under test (DUT) with an input pattern, then comparing the outputs of the DUT against an expected output pattern.



Patterns

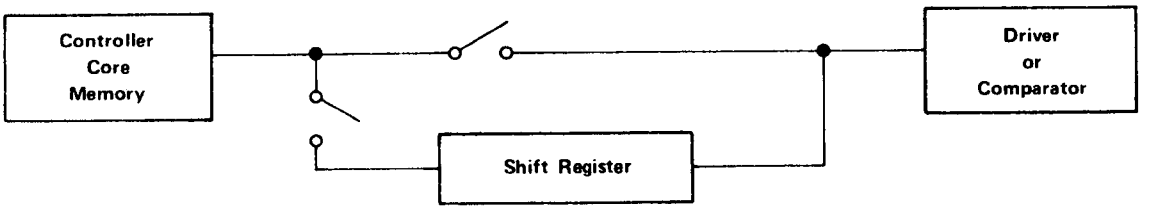
Patterns are sequences of binary data (1's and 0's) that are applied to or checked for on each pin of the DUT in the course of a test. For display purposes, pattern data is arranged in tabular form. Each column of a pattern table defines the binary data to be input to or output from one pin of the DUT. Each row (word) gives the input and output data to define one state or operating condition of the device. A functional test thus involves applying a pattern to the DUT pins, one row at a time, and checking that the output of the DUT responds as expected.

A pattern may be a truth table of the device or, in the case of a memory module test, a special-purpose data sequence such as a checkerboard, walking one, etc.

Patterns are usually generated prior to test time and stored on the system's disk. They are moved to core or to the shift registers at the pin electronics under the control of the test program. Either the pattern editor or the algorithmic pattern generator can be used for this purpose (see the TEKTEST III Programmer's Instructions manual). Patterns can also be generated at test time using the real-time pattern generator.

Memory Buffers

The patterns can be applied directly from core memory in the system controller to the drivers and comparators or through shift register memory buffers. If a pattern is applied directly, the controller data transfer rate limits the test rate. To increase the test rate, a pattern is first read into the memory buffers. Then at test time, the pattern is moved into the drivers and comparators at rates up to 20 MHz.



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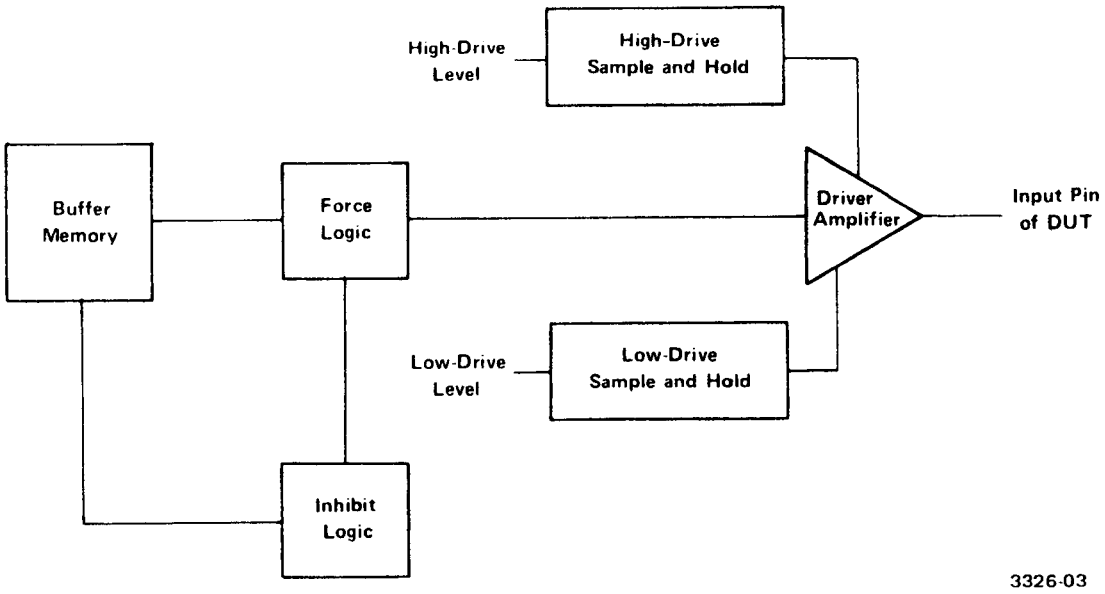
Sector Cards

The drivers, comparators, and shift register memory buffers are located on the sector cards. There can be up to 64 sector cards in the S-3270. The sector cards are located in the 1804 carrousel. Each standard sector card has a driver circuit, a comparator circuit, one memory buffer, and switching to connect the driver and comparator to as many as two pins of the DUT (one input pin and one output pin). The D70 sector card driver has a ±30 V range, and the comparator has a ±30 V range.

Driver Circuit

The driver circuit forces a logic level on an input of the DUT. This level may be either high or low (1 or 0) or inhibited. The voltage level for the D70 sector cards can be selected within a range of ±30 V with a maximum difference between the high and low level of 30 V.

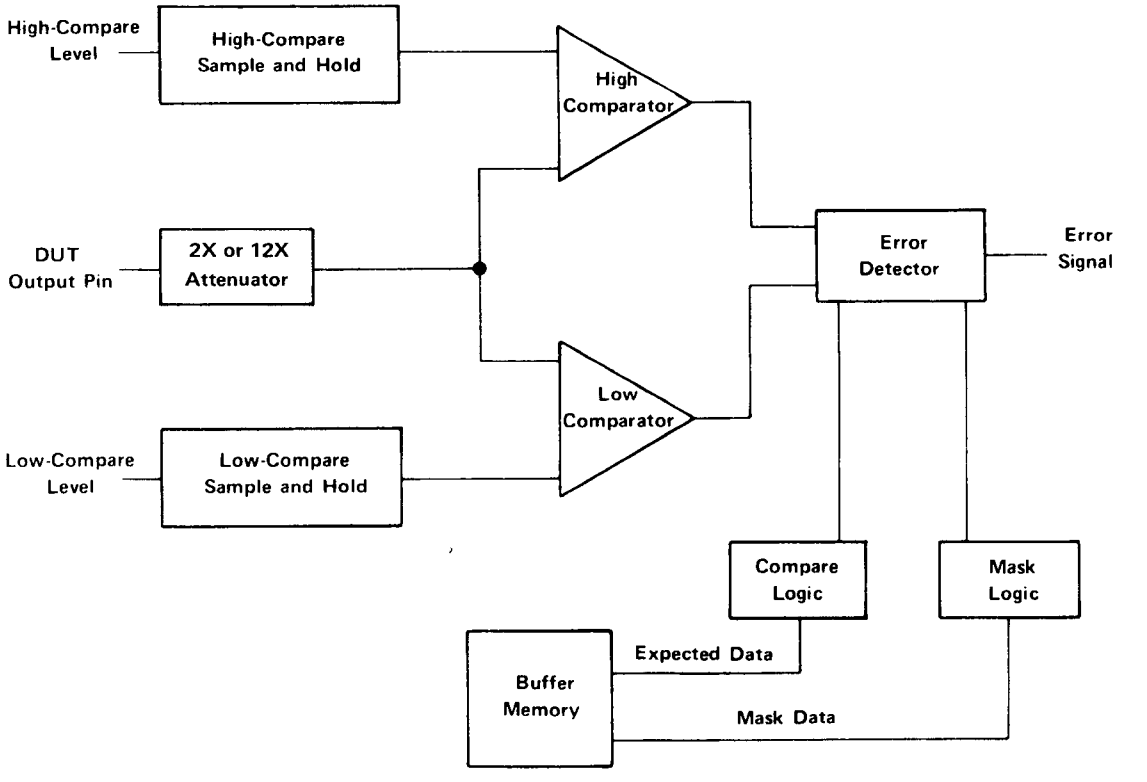


Prior to test time, the high and low levels are stored in high-drive and low-drive sample and hold circuits, respectively. When the test is run, each input pattern bit from the buffer memory tells the driver amplifier to force the DUT pin high or low. The driver amplifier then looks at the appropriate sample and hold circuit and produces the corresponding voltage level.

The D70 driver can be switched to a high-impedance state. This function, called INHIBIT, is used when testing devices with I/O pins. The driver must assert a high impedance to allow the DUT output to drive the signal line. A driver may be inhibited any time during a cycle.

Comparator Circuit

The comparator circuit compares the logic level on a DUT output pin with an expected logic level. It then outputs an error signal if the output is not as expected. The comparison level may be either a high or a low (1 or 0). The voltage of the comparison levels can be selected within a range of ±30 V for D70 sector cards.



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As with the driver circuit, the high and low comparison levels are stored in the high-compare and low-compare sample and hold circuits, respectively, prior to test time. At test time, each comparator compares the level from the DUT output pin with the level stored in its respective sample and hold circuit. At the same time, an output pattern bit from the buffer memory tells the error detector if the output level should be high or low. If the expected level is not detected, an error pulse is generated.

The output of the error detector can also be masked, i.e., the error detector ignores the level of the DUT output pin. The mask function has two uses. Like the inhibit function, the mask function is used when the DUT pin being tested is an input/output pin. When this pin is used as an input, the comparator output may be masked. Masking is also used when you don't care about the output at a particular pin or when the output is indeterminant.

Clock Generator

The Programmable Multiphase Clock Generator controls the timing of the entire system. It performs three functions:

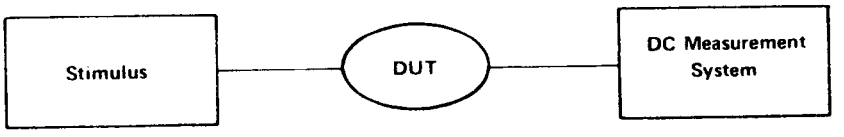
1. Clocks data through the memory buffers.
2. Clocks force data, and
3. Clocks compare data.

The Clock Generator supplies a 14-phase clock (fourteen individual pulses time referenced to a single system clock pulse) that has a repetition rate of up to 20 MHz. The position and width of each phase pulse can be independently programmed. On a 14-phase system, the phases may be distributed by several different methods.

All clock phases are referenced to the T-zero (TØ) signal that occurs at the beginning of each clock cycle.

Parametric Testing

Parametric testing consists of stimulating the DUT and measuring its response. There are two kinds of parametric tests: DC and time-interval. Both kinds may be preceded by a functional test sequence to initialize the DUT to a particular state.



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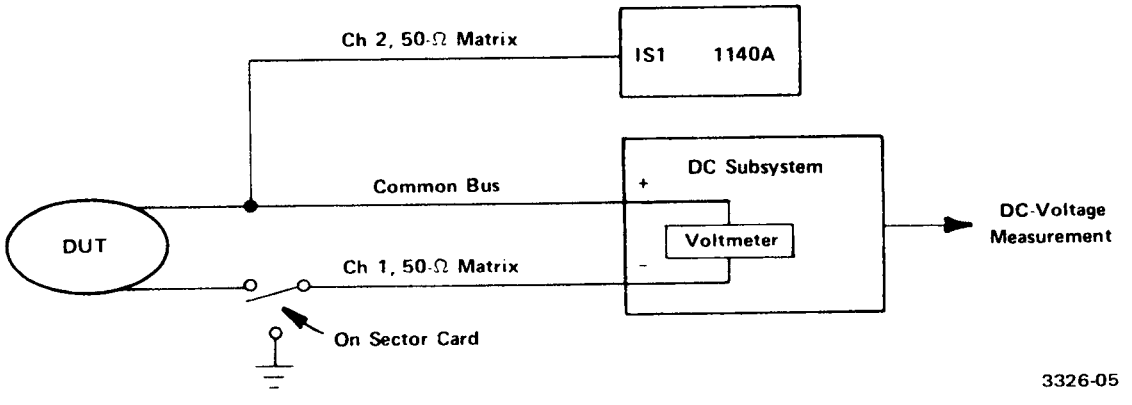
DC Measurements (DC Subsystem)

DC measurements are made with the DC subsystem. There are two basic kinds of DC measurements: measure voltage and measure current while forcing a voltage. (The DC subsystem also provides the added capability of forcing a DC voltage or a current without measuring.) The DC subsystem can measure voltages from 0 to ±100 V in four ranges. It can measure currents from 0 to ±500 mA in seven ranges.

For a DC-voltage measurement, the DC subsystem is connected to the DUT through the sector cards, the common bus, and channel 1 of the 50-Ω switching matrix. To force a DC current while measuring a DC voltage, the current is forced through channel 2 of the 50-Ω switching matrix.



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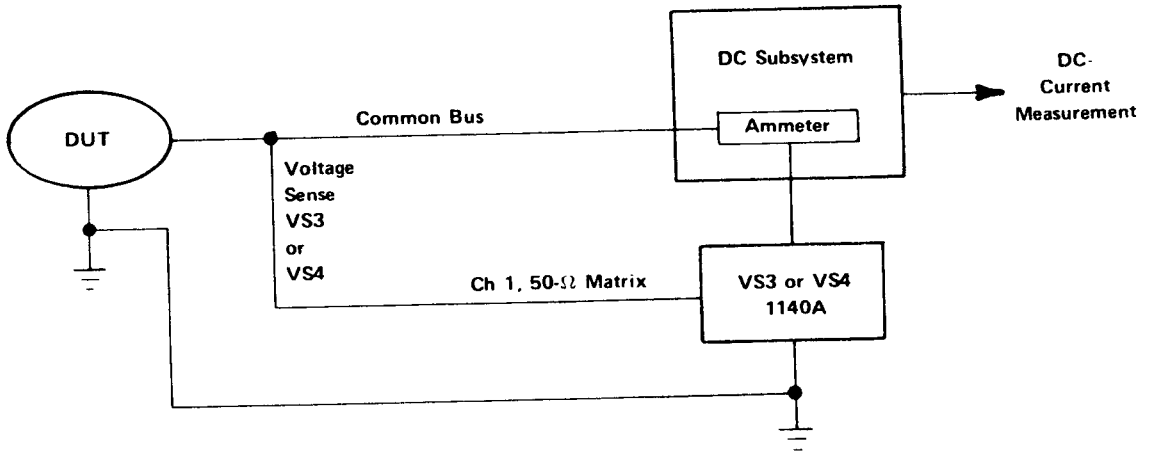
For a DC-current measurement, the DC subsystem is connected to the DUT through the common bus only. To make a current measurement, the DC subsystem forces a voltage on the pin of the DUT, then measures the resulting current. The force voltage must thus be specified. The current through the common bus is in some cases large enough to cause a drop in forcing voltage between the DC subsystem and the DUT pin. On some ranges, therefore, the voltage sense line of the forcing supply is connected to the DUT pin through channel 1 of the 50-Ω switching matrix. This Kelvin connection assures that the correct, programmed voltage is applied to the DUT.

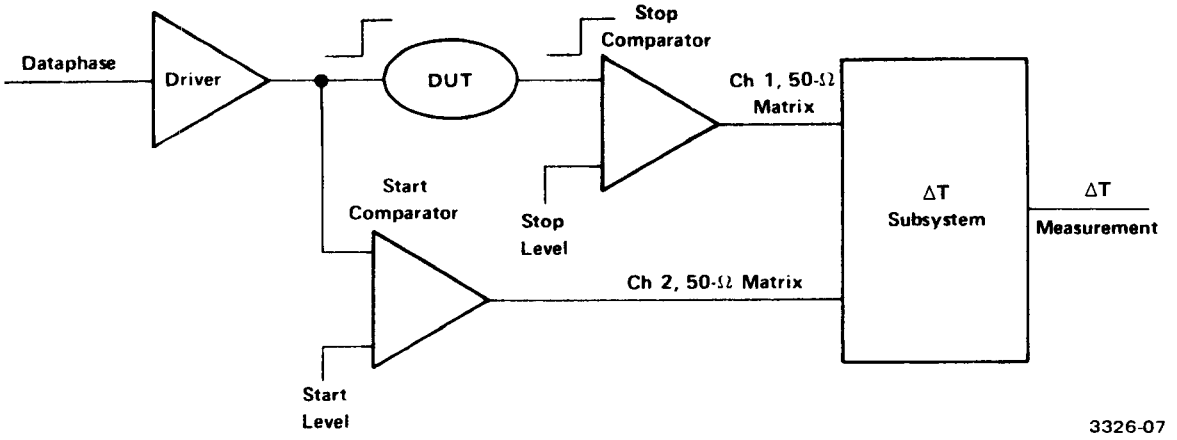


3326-06

Time-Interval Measurements (ΔT Subsystem)

Time-interval measurements are made with the ΔT subsystem. Propagation delay-time, risetime, period, and width measurements can all be made with the ΔT subsystem. The ΔT subsystem has five ranges, 100 ns through 1 ms, full-scale.

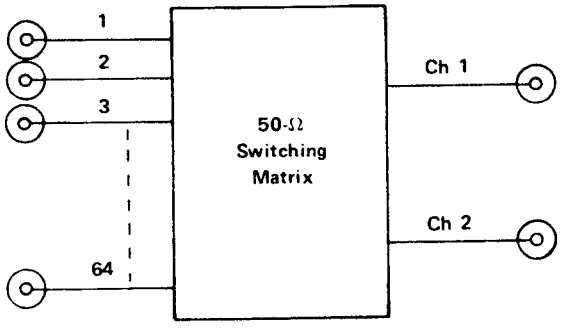
A ΔT measurement consists of stimulating the DUT with a pulse or step (generally one of the clock generator phases), then measuring a time-related response of the DUT to that signal with the ΔT subsystem. The ΔT subsystem can be thought of as a very accurate "stop watch." The comparator circuits on the sector cards turn it on and off.



For example, to make a propagation delay measurement, one comparator circuit (called the start comparator) is connected to a DUT input pin and another comparator (the stop comparator) is connected to an output pin. A start level is then set in the start-comparator sample and hold circuit and a stop level in the stop-comparator sample and hold circuit. The DUT input pin is then stimulated with a step signal (the Dataphase might be used in this case). When the DUT input pin goes above the start level, the start comparator turns on the ΔT subsystem. When the DUT output pin goes above the stop level, the stop comparator turns off the ΔT subsystem. The propagation delay time is thus the time interval the ΔT subsystem measures. The start and stop signals are transmitted to the ΔT subsystem through the two channels of the 50-Ω switching matrix.

50-Ω Switching Matrix

The 50-Ω switching matrix consists of two 1-to-64 switchers. It is used to transmit signals, voltages, and currents between the sector cards and the DC and ΔT subsystems, or external devices such as an oscilloscope, pulse generator, etc.



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Digitizer

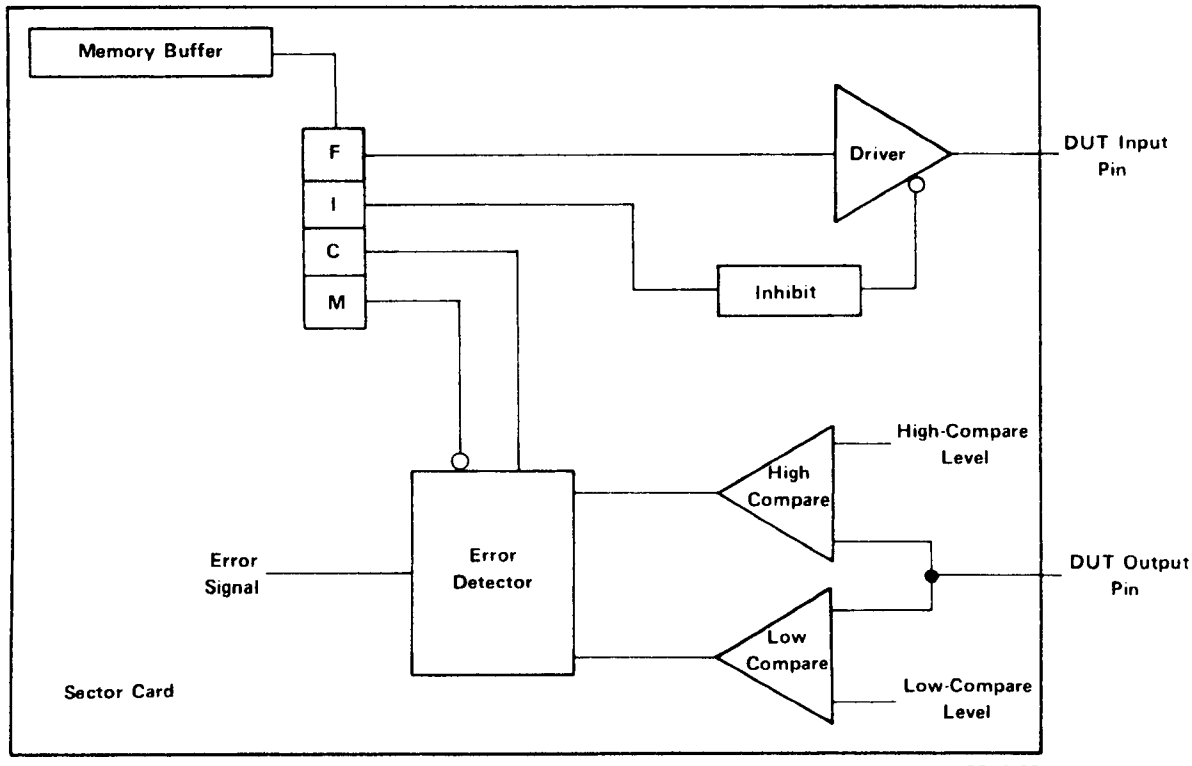
A waveform digitizer package is available with the S-3270. The digitizer package consists of a two-channel programmable sampling oscilloscope, a waveform digitizer, and the waveform analysis (WAFORM Subprograms) software package. To use the digitizer package, signals are transmitted from any two pins of the DUT, through the D70 card's EXT.OUT connection to the sampling heads. The oscilloscope and the digitizer then convert the signals from analog to digital form and store them in the computer memory. The stored waveforms can then be analyzed using the WAFORM subprograms. Measurements such as peak amplitude, RMS level, average level, risetime, falltime, width, delay, and period can all be made on or between two stored waveforms. Other waveform measurements may be defined by the user.

Summary of Sector Card Functions

As was shown earlier, each sector card can perform four clock-rate data functions:

1. Force – Drive a DUT input pin between specific logic levels.
2. Inhibit – Sets the driver in a high-impedance state to allow the DUT to set its own voltage level.
3. Compare – Check the level of a DUT output pin against expected levels.
4. Mask – Prevent comparator output from generating errors.

These functions are abbreviated F, I, C, and M and are all used to perform functional tests.



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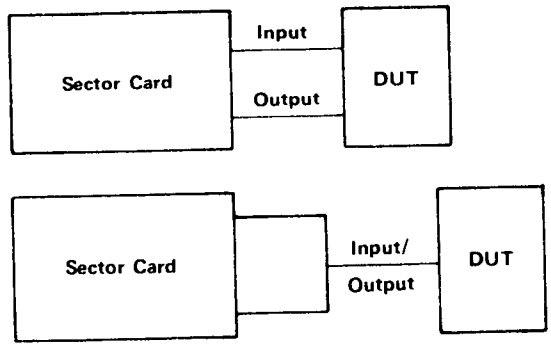
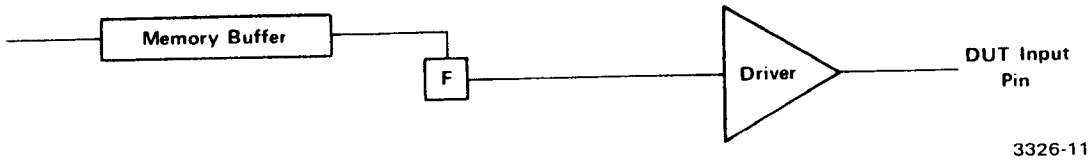
Each sector card can also be connected to two DUT pins at a time, one input pin and one output pin. Or, it can be connected to one pin that is used both as an input and an output.



3326-10

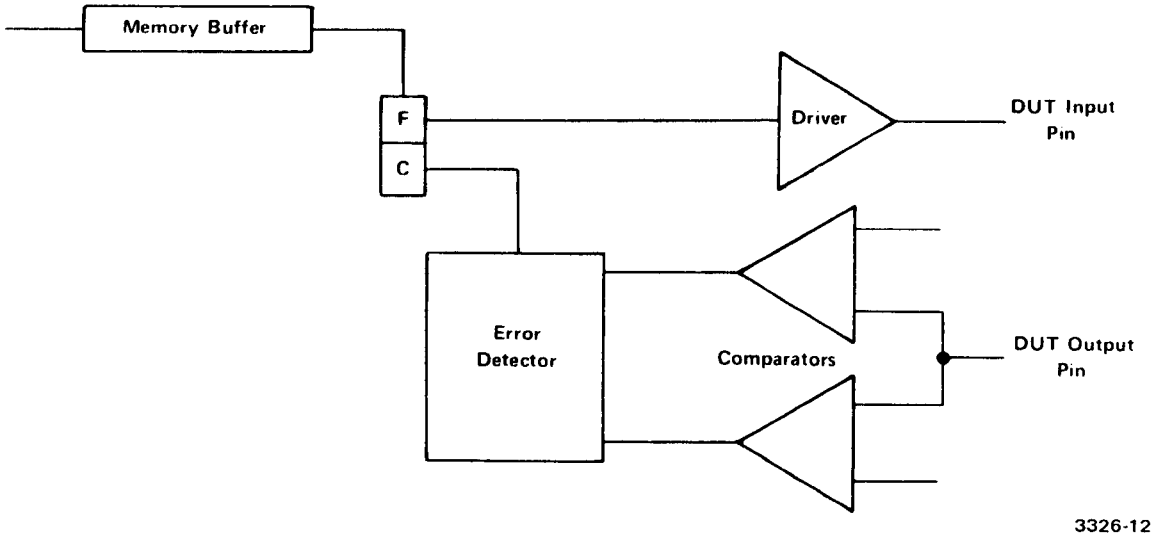
As was also previously mentioned, each sector card has a shift register memory buffer. Each of these memory buffers can store 4104 bits.

One bit from the memory buffer is required to define the state of each sector-card function used. Thus, if one function per sector card is used to perform a test on a device, one bit per memory buffer is required for each clock cycle of the test.



3326-11

If two functions are used per sector card, then two bits per memory buffer are required for each clock cycle.



The maximum rate of data transfer through the memory buffers is 20 MHz (20×10^6 bits/second). If only one function is used per sector card, tests can be run at this 20-MHz rate. If two functions are used, however, the test rate is reduced to 10 MHz, because it now takes two bits from each memory buffer to define the state of the two functions on each sector card. If all four sector-card functions are used, the test rate is further reduced to 5 MHz.

One technique is available that allows the use of multiple sector-card functions while still operating at the faster test rate: parallel chaining. This is described in the following discussion.

As has been shown above, the sector cards can be used in a variety of ways depending on:

1. What kind of tests are to be performed,
2. How many pins on the DUT are to be tested, and
3. The desired test rate.

The diagrams on the following pages use these abbreviations:

SR – designates a shift register

SR N – designates that sector card shift register that is connected to the DUT pin (sector N)

SR N-1 – designates the shift register next to sector N

In the following examples, shift registers look like a box divided into compartments, with each compartment containing one bit. For simplicity, these illustrations show only a few of the 4104 bits.

The Four Test Modes

The sector cards have four operating modes:

Mode 1: F,I,C,M

Mode 2: FC

Mode 3: FI,CM

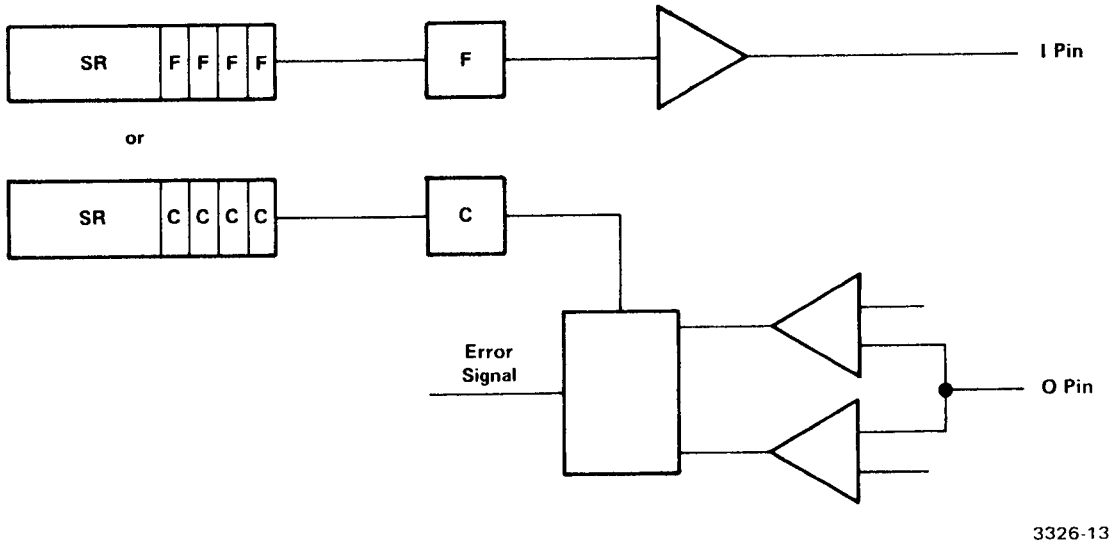
Mode 4: FICM

Each mode is selected station-wide. All sector cards must operate in the same mode simultaneously.

Mode 1

In mode 1, the sector card is connected to only one DUT pin and only one sector card function is used – either force or compare. In mode 1, the system can operate at its full 20 MHz test rate and test up to 64 DUT pins at a time.

Mode 1 F,I,C,M



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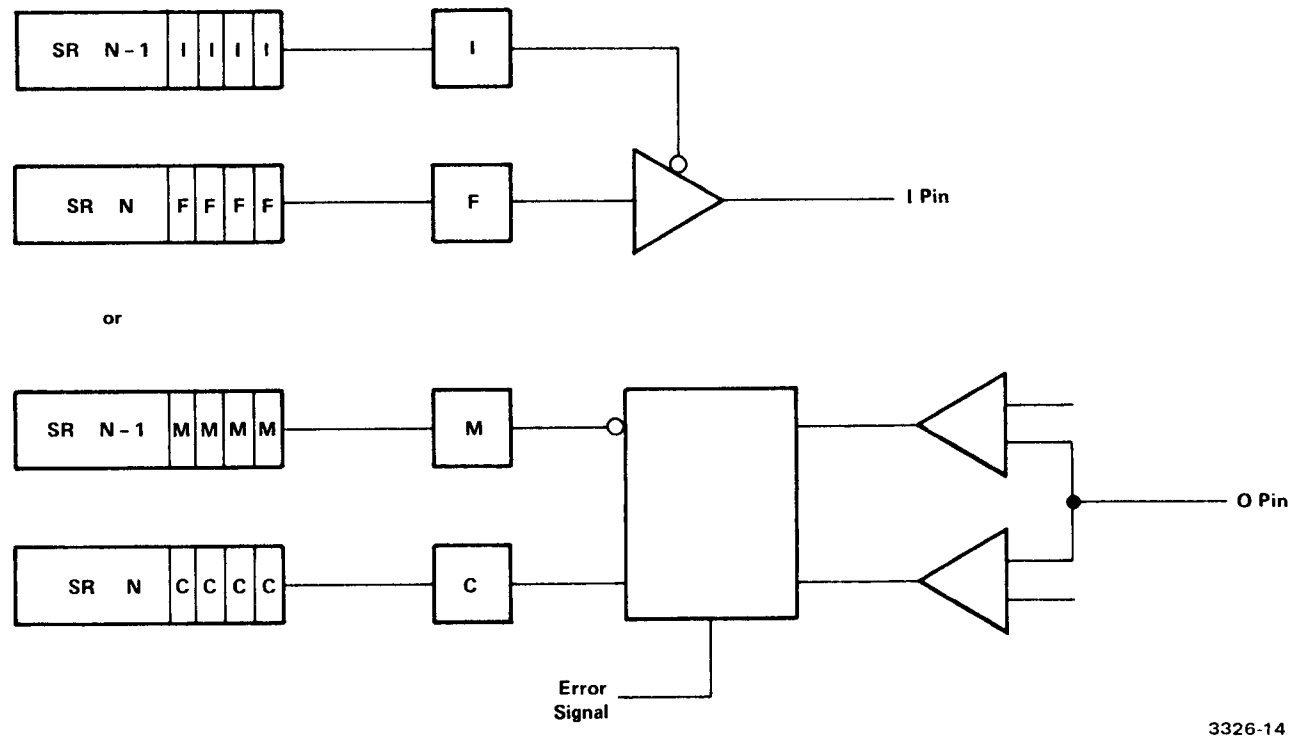
Mode 1 with Parallel Chaining

In this mode, the sector card is connected to one DUT pin. The card uses its own memory buffer to supply force or compare data and the buffer of an adjacent sector to supply inhibit or mask data. This way, the S-3270 operates at a 20 MHz test rate and can test up to 32 DUT pins in any mixture of I and O.

Mode 1 with Parallel Chaining



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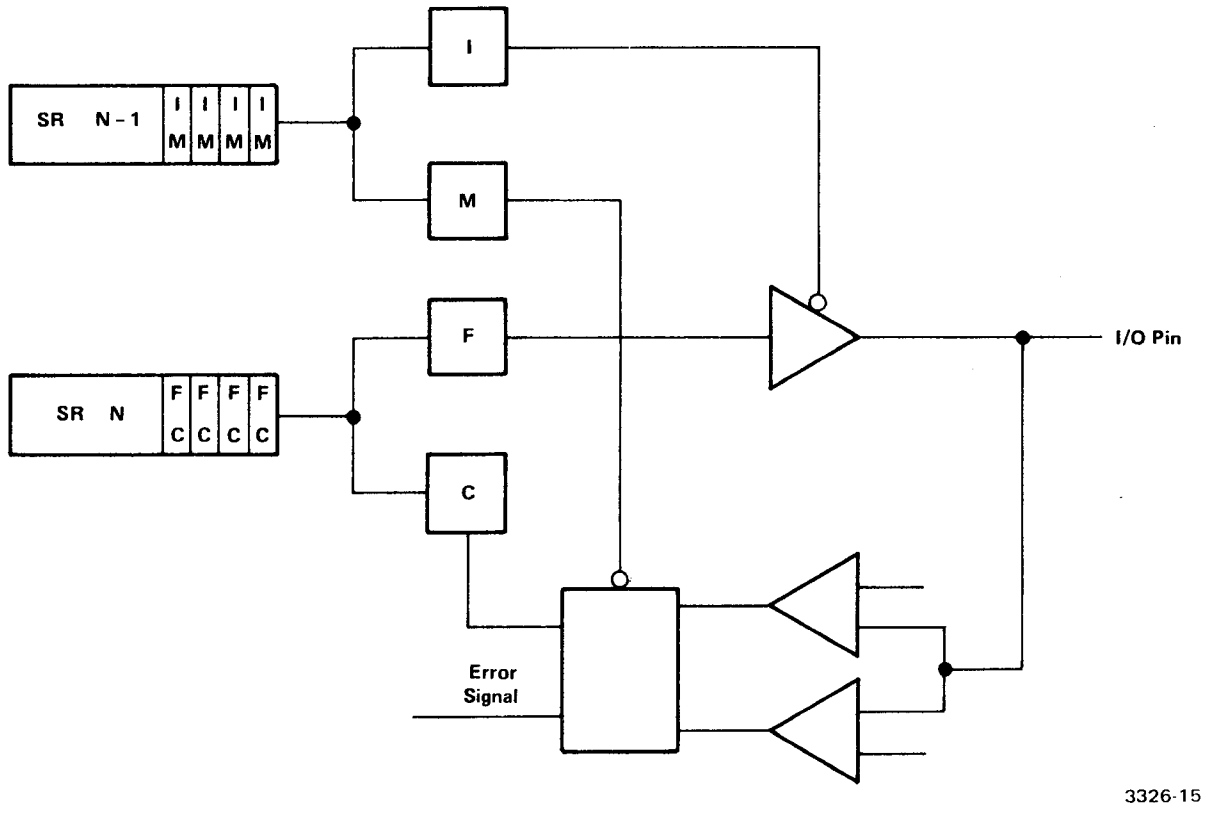
Mode 1 with Parallel Chaining for I/O Pins

In this mode, the sector card is connected to a DUT I/O pin. The sector card uses its own memory buffer to supply force and compare data and the buffer of the adjacent sector to supply inhibit and mask data. With the driver inhibited, the comparator is not masked and vice versa. The system operates at the 20 MHz test rate and can test up to 32 DUT pins in any mixture of I/O and O.

Mode 1 with Parallel Chaining for I/O Pins

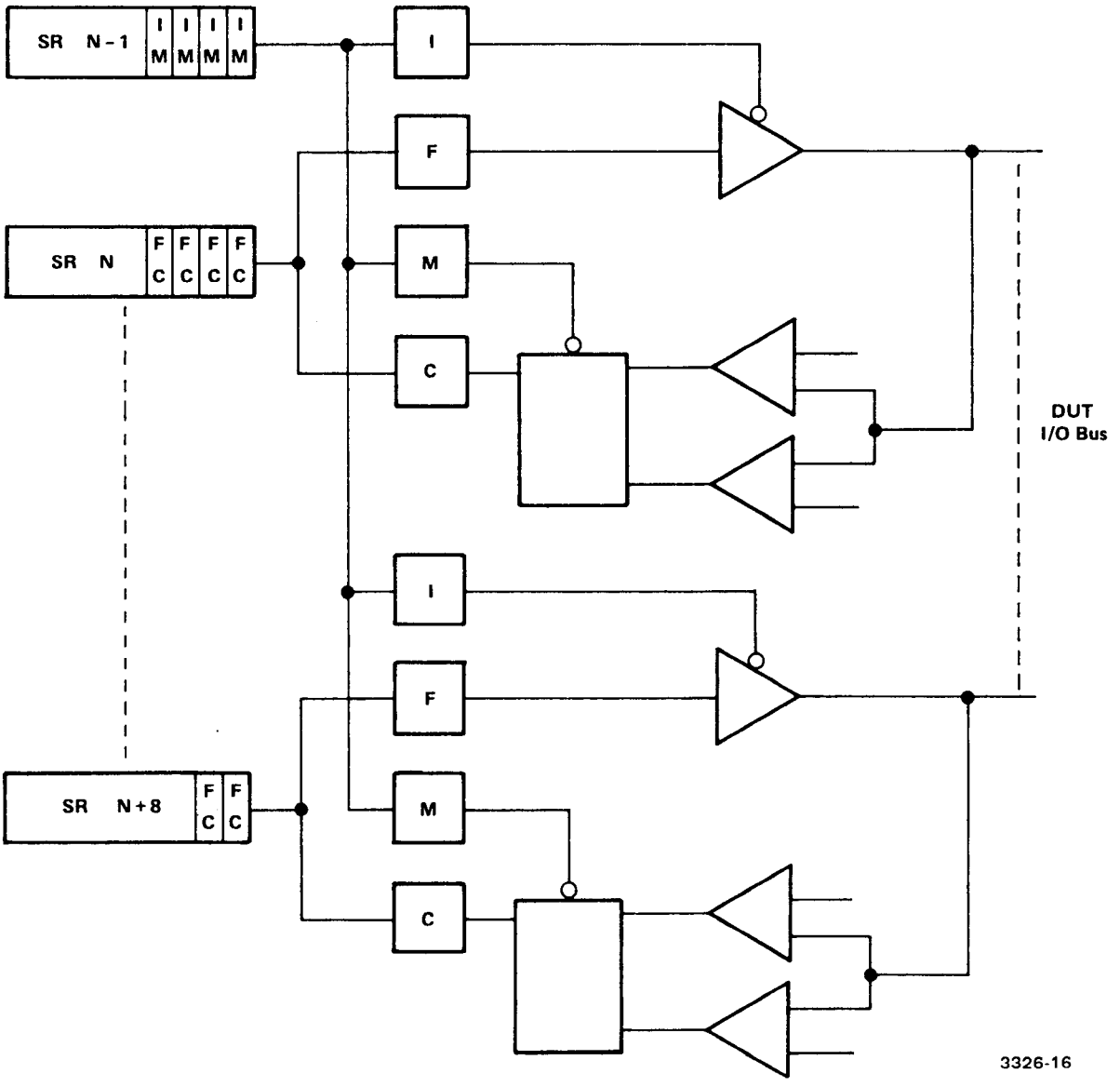


3326-15

Mode 1 with Parallel Chaining for I/O Buses

In this mode, one memory buffer provides inhibit mask data for several sectors connected to I/O pins of an I/O DUT bus. Each sector provides the force and compare data from its own memory buffer. The system operates a test rate of less than 20 MHz. The test rate depends on the number of sectors that use the inhibit mask data from one memory buffer. The number of DUT pins that can be tested also depends on the number of sectors that use inhibit mask data from one memory buffer.

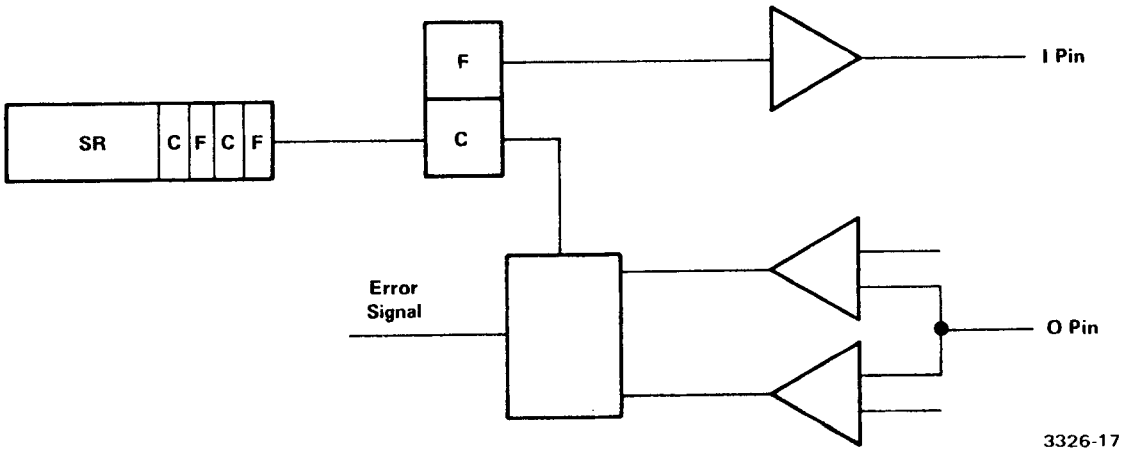
Mode 1 with Parallel Chaining for I/O Buses



Mode 2

Mode 2 allows an input and an output to be forced and compared, respectively, with one sector card. This mode increases the number of testable DUT pins to 128, but the test rate is reduced to 10 MHz.

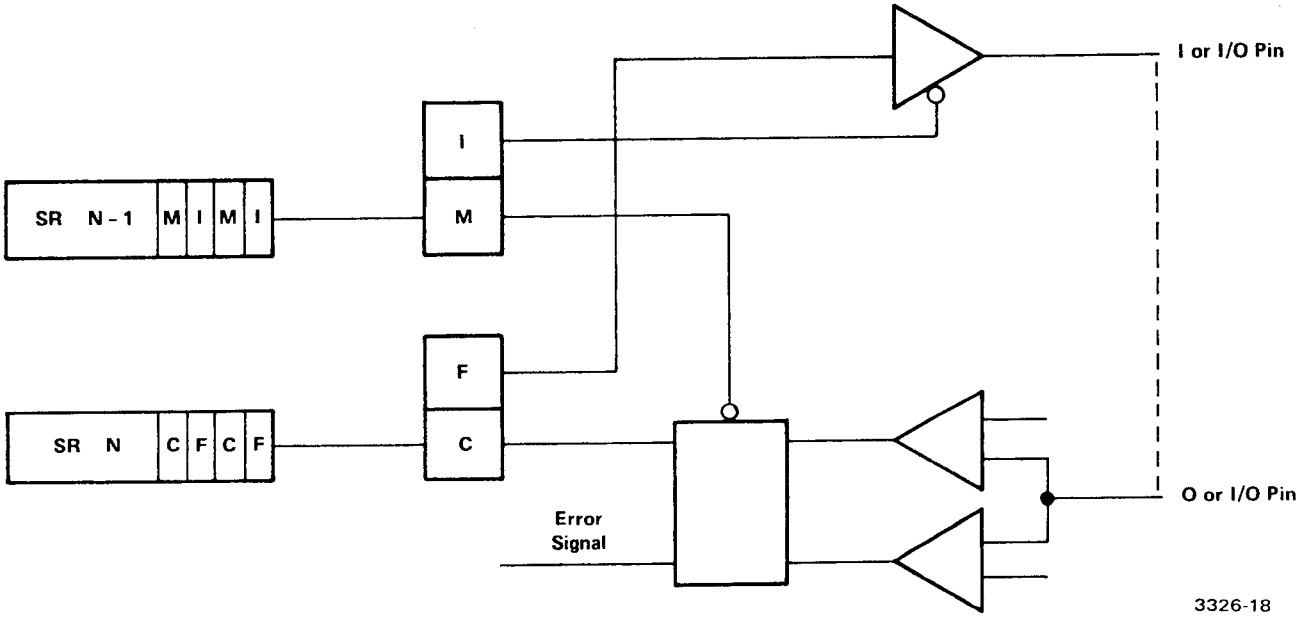
Mode 2



Mode 2 with Parallel Chaining

In this mode, a sector uses data from an adjacent sector card as inhibit and mask information and data from its own buffer memory as force and compare information. The sector can test one O pin and one I pin or one I/O pin. This mode tests up to 64 pins (32 I and 32 O) at a maximum test rate of 10 MHz.

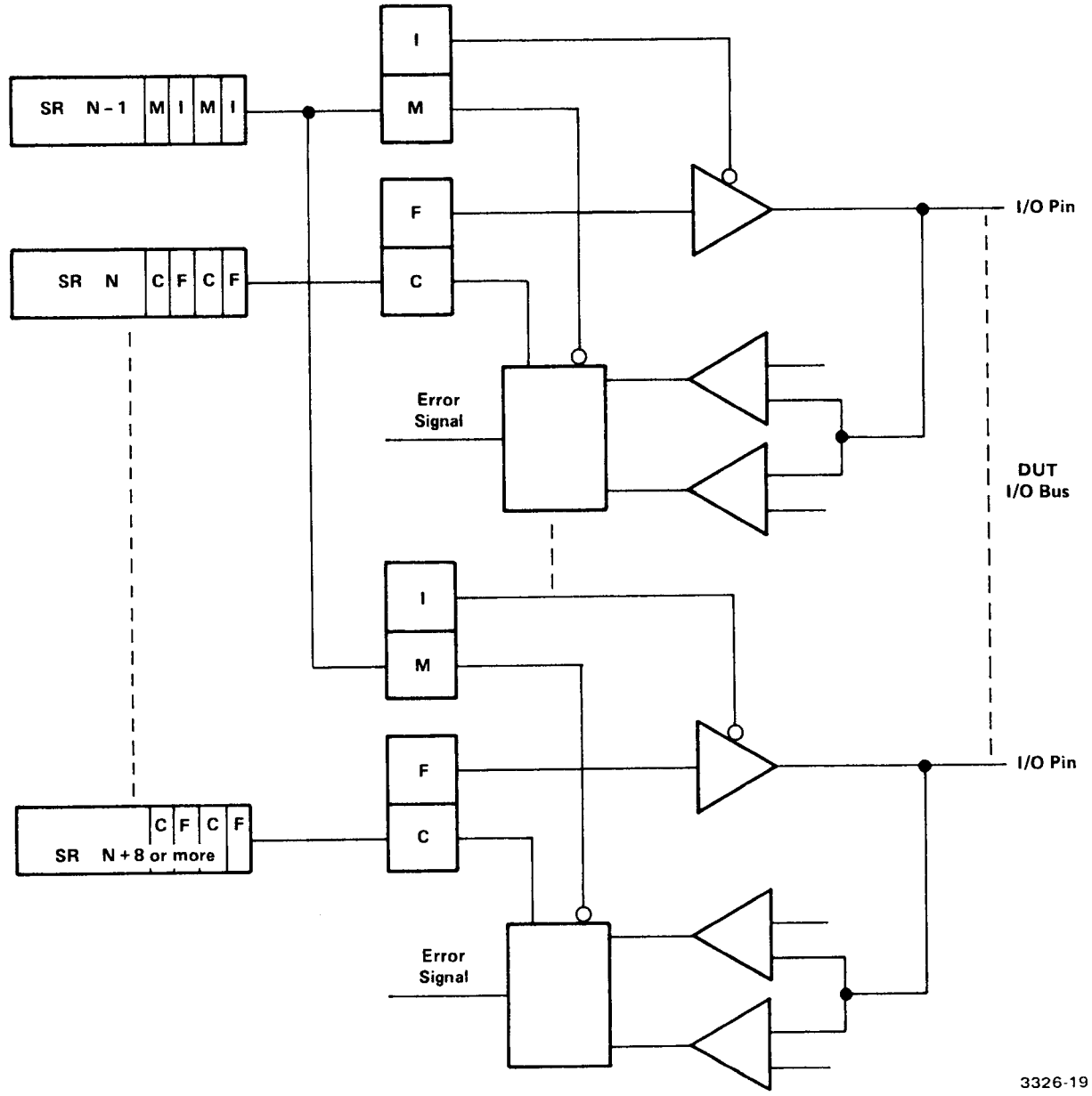
Mode 2 with Parallel Chaining



Mode 2 with Parallel Chaining through Multiple Sectors

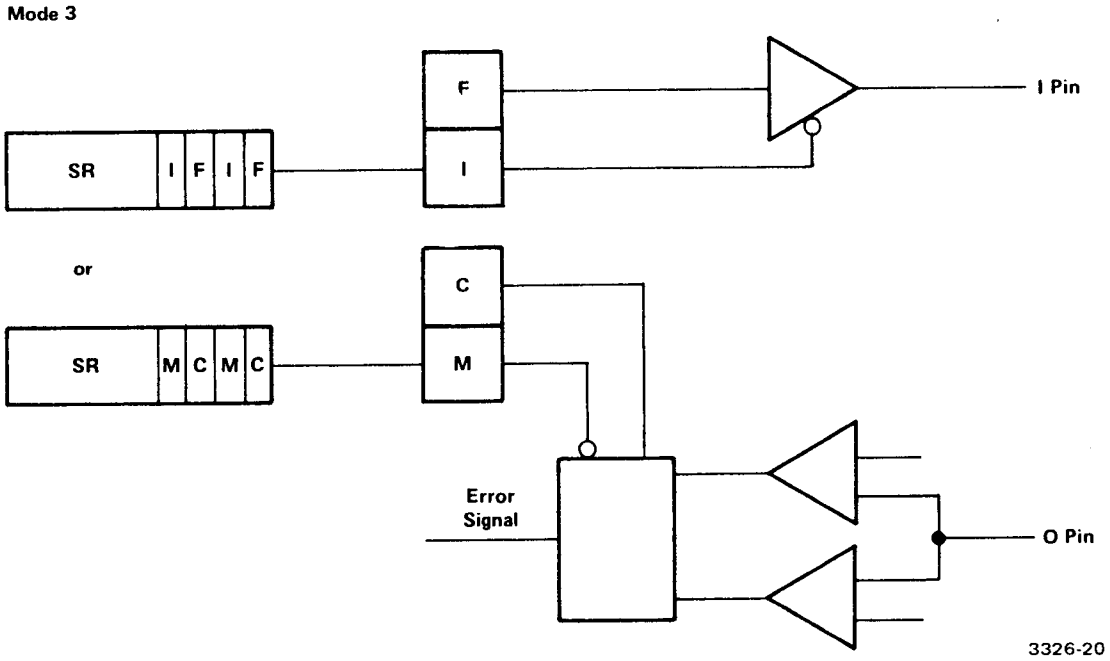
In this mode, several sectors use data from one sector as inhibit and mask information. Each sector uses its own memory buffer to provide force and compare data. The total number of testable DUT pins and its subsequent test rate depends on the number of sectors that use data from a single sector to inhibit and mask. The maximum test rate is less than 20 MHz.

Mode 2 with Parallel Chaining through Multiple sectors



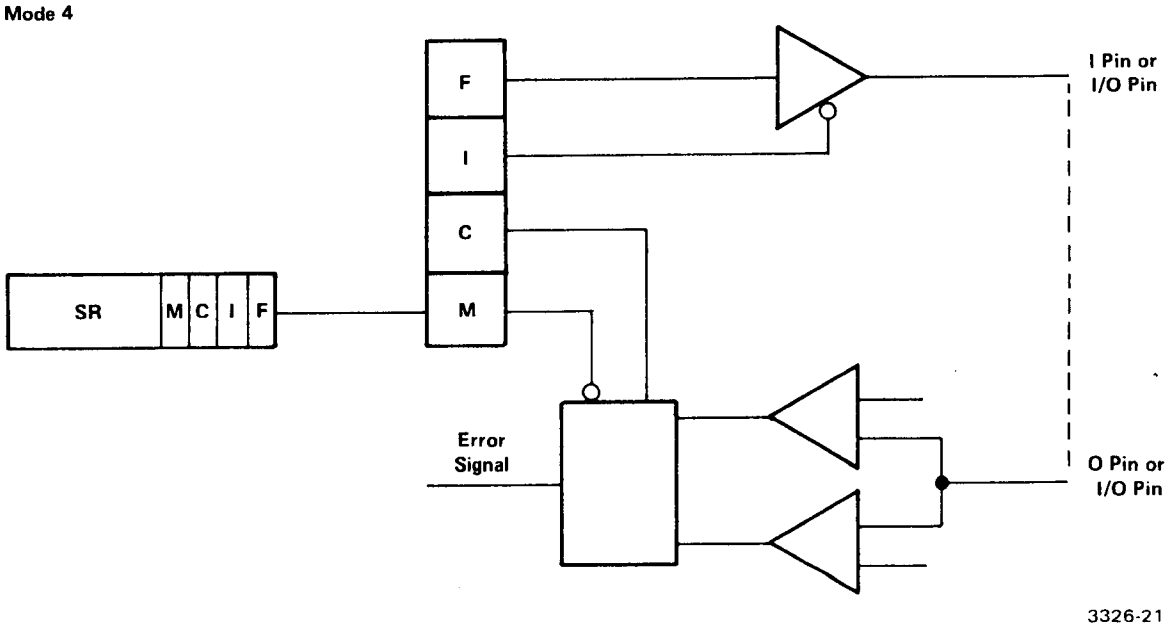
Mode 3

Mode 3 provides the force and inhibit data, or the compare and mask data from the sector card buffer memory. Mode 3 tests 64 pins maximum at a test rate of up to 10 MHz.



Mode 4

In mode 4, the force, inhibit, compare, and mask data comes from the sector card memory buffer. Up to 128 pins or 64 I/O pins can be tested at a maximum test rate of 5 MHz.



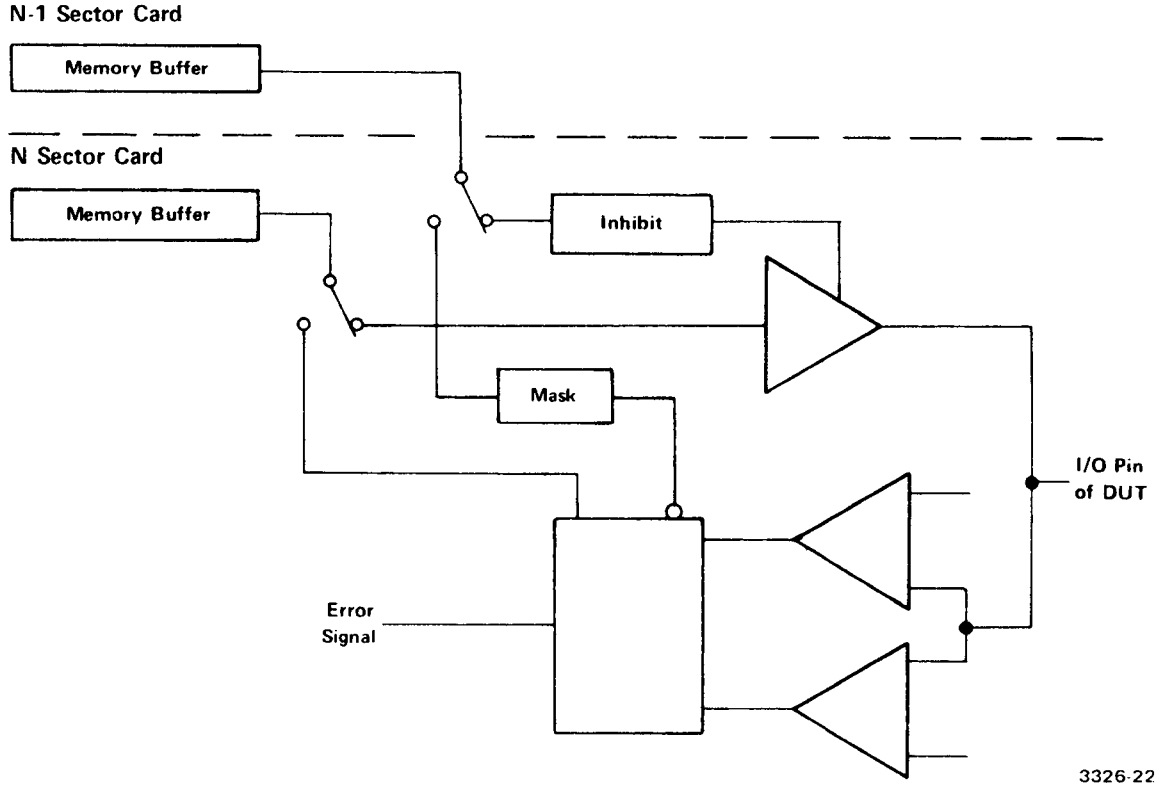
Chaining

The term chaining refers to connecting a buffer memory from one sector card to another sector card. There are two kinds of chaining: parallel chaining and serial chaining.

Parallel Chaining

When using parallel chaining, the memory buffer from the N-1 sector card controls one of the functions of the N sector card. Thus two functions of the N sector card such as F and I or C and M can be used simultaneously but at the 20 MHz mode 1 test rate rather than the 10 MHz mode 2 test rate. The trade off is that none of the clock-rate data functions of the N-1 sector card can be connected to the DUT. However, fixed or toggling data may be forced or compared at the N-1 sector card.

Parallel chaining is available only when operating in mode 1 or mode 2.



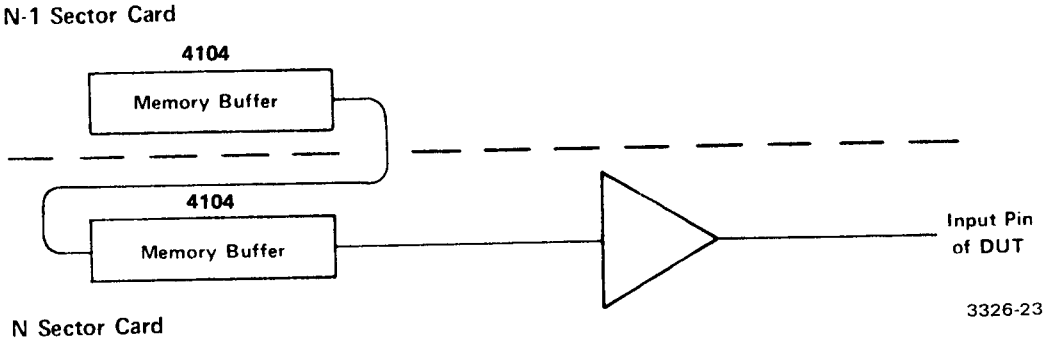
Serial Chaining

When using serial chaining, the memory buffer from the N-1 sector card is connected in series with the memory buffer of the N sector card. The number of bits that can be moved into a pin of the DUT from the N sector card is thus doubled from 4104 to 8208. As with parallel chaining, none of the clock-rate data functions of the N-1 sector card can be connected to the DUT. Fixed or toggling data can be connected, however.

Serial chaining is useful when patterns with more than 4104 rows are to be run continuously at 20 MHz. Without serial chaining, the test must be halted after each 4104 rows (words) of the pattern are applied to the DUT, to allow reloading the memory buffers. The actual test rate may still be 20 MHz, but the total time it takes to test the DUT is determined by the length of the pattern and the cycle time, plus the time it takes to reload buffers.

Chaining can be different at each pin. That is, two registers can be chained to handle one pin while, say, six registers are chained to handle another pin. If the application requires, as many as 32 sector cards can be serial chained to allow patterns with up to 131,328 bits to be run.

Recirculation is not compatible with serial chaining. Also, serial chaining cannot be carried through parallel-chained sector pairs.

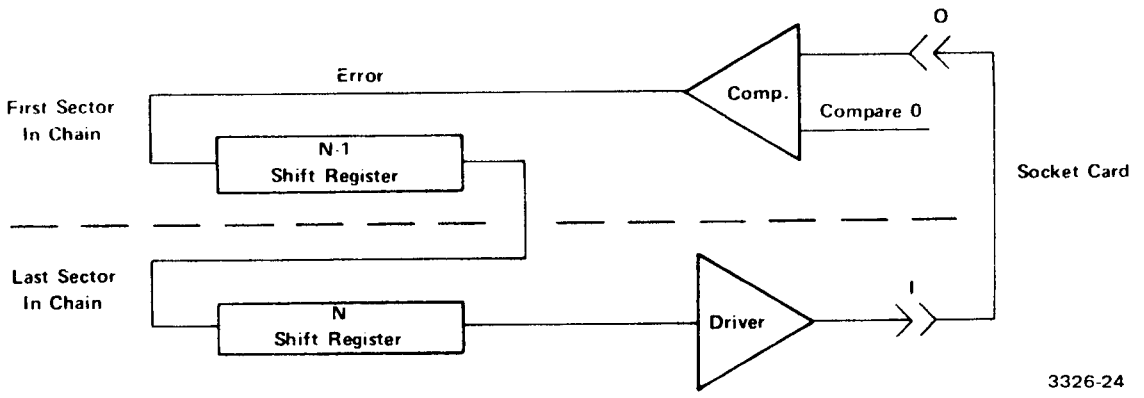


Recirculation

Data in any individual or group of memory buffers may be recirculated for repeated use without reloading from core or disk. Address sequences for RAM's or ROM's may thus be stored once and used repeatedly throughout a test.

Recirculation is compatible with modes 1, 2, 3, and 4 and with parallel chaining. Address sequences longer than 4104 bits per pin must be partitioned into 4104 (or less)-bit groups. Each group is used repeatedly by recirculation followed by reloading of the memory buffer, repeated use of the next group, and so on.

Serial chains may only be recirculated by connecting, at the socket card, the driver at one end of the chain to the comparator at the other end of the chain.



Summary of Modes and Parallel Chaining

The following table summarizes the information discussed in this section on the sector-card functions. All possible uses except those involving serial chaining are shown.

MODE	MAXIMUM TEST RATE	MAXIMUM NUMBER OF PINS*	MAXIMUM PATTERN DEPTH	FUNCTIONS CONTROLLED AT SECTOR N		PIN USE AT SECTOR N	PARALLEL CHAINING
				FROM MEMORY BUFFER AT SECTOR N	FROM MEMORY BUFFER AT SECTOR N-1		
F,I,C,M (Mode 1)	20 MHz	64 I or 64 O (any mixture)	4104	F	None	I	No
				C		O	
	20 MHz Less if chained more than one sector	32 I or 32 O (any mixture) More if chained more than one sector		F and	I	I	Yes
				C and	M	O	
				F and C	I and M	I/O	
FC (Mode 2)	10 MHz	64 I and 64 O	2052	FC	None	I and O	No
FI,CM (Mode 3)		64 I or 64 O (any mixture)		FI		I	
				CM		O	
FICM (Mode 4)	5 MHz	64 I and 64 O	1026	FICM		I and O	
FC (Mode 2)	10 MHz Less if chained more than one sector	32 I or 32 O (any mixture) More if chained more than one sector	2052	FC	IM	I and O and I/O	Yes

*For the clock-rate data functions indicated. All four (F,I,C, and M) functions at all 64 sector cards may always be controlled by fixed or toggling data.

Some Examples of Serial Chaining

The following table gives several examples of serial chaining as discussed in this section. Many more could have been formulated.

MODE	MAXIMUM TEST RATE	MAXIMUM NUMBER OF PINS	MAXIMUM PATTERN DEPTH	FUNCTIONS CONTROLLED AT SECTOR CARD N		PIN USE AT SECTOR N	PARALLEL CHAINING
				FROM BUFFER MEMORY AT SECTOR N	FROM BUFFER MEMORY AT SECTOR:		
F,I,C,M (Mode 1)	20 MHz	32 I or 32 O (any mixture)	*2064	F	N-1	I	No
				I		O	
				C			
				M			
		16 I or 16 O (any mixture)	*4128	F	N-1 through N-3	I	
				I		O	
				C			
				M			
FC (Mode 2)	10 MHz	16 I and 16 O	*2064	FC	N-1 through N-3	I and O	
FI,CM (Mode 3)		32 I or 32 O (any mixture)	*1032	FI	N-1	I	
				CM		O	
FICM (Mode 4)	5 MHz	32 I and 32 O	*1032	FICM	N-1	I and O	
		16 I and 16 O	*516		N-1 through N-3		

*Limited by the Sequence Counter of the 2941 Multiphase Clock Generator to 4095, $\frac{4095}{2}$, and $\frac{4095}{4}$.

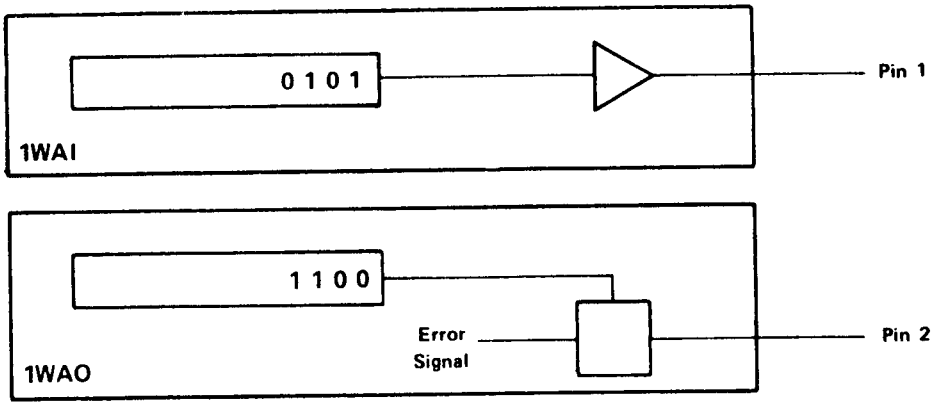
Section 3 of the TEKTEST III Programmer's Manual contains a description of the various means of generating patterns. Patterns are generated on a pin-by-pin basis using one of the TEKTEST III pattern generation methods (PEDIT, APG).

If only one function per sector card is used to exercise one pin of the DUT, the pattern data will consist of columns of force data and columns of compare data. In this case, one column of the pattern is loaded into each buffer memory and read into the driver or comparator circuits one bit at a time.

When more than one sector-card function is used to exercise a DUT pin (e.g., FI or CM), or when two DUT pins are exercised by one sector card (e.g., F and C), more than one column of data needs to be loaded into a buffer memory (or buffer memories if chaining is used).

	Pin 1	Pin 2
0001:	1	0
0002:	0	0
0003:	1	1
0004:	0	1

Pin 1 is connected to Sector Card 1WAI and Pin 2 is connected to Sector Card 1WAO Mode 2 (FC) has been selected.



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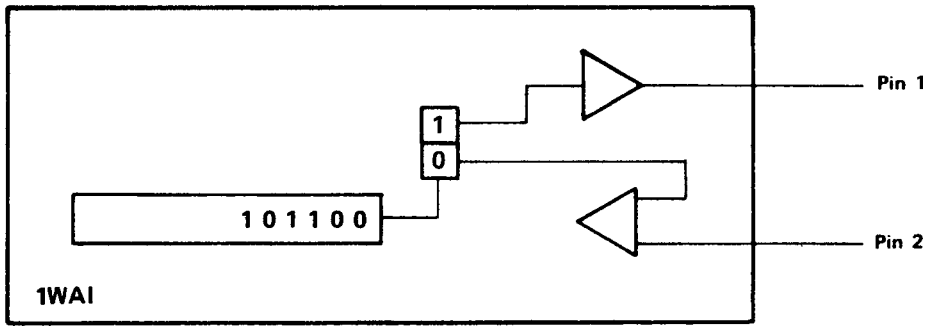

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The reformatting of patterns so they can be loaded in proper order in the buffer memories is called swizzling. Swizzling is performed by the TEKTEST III translator and is done automatically.

Clock Generator

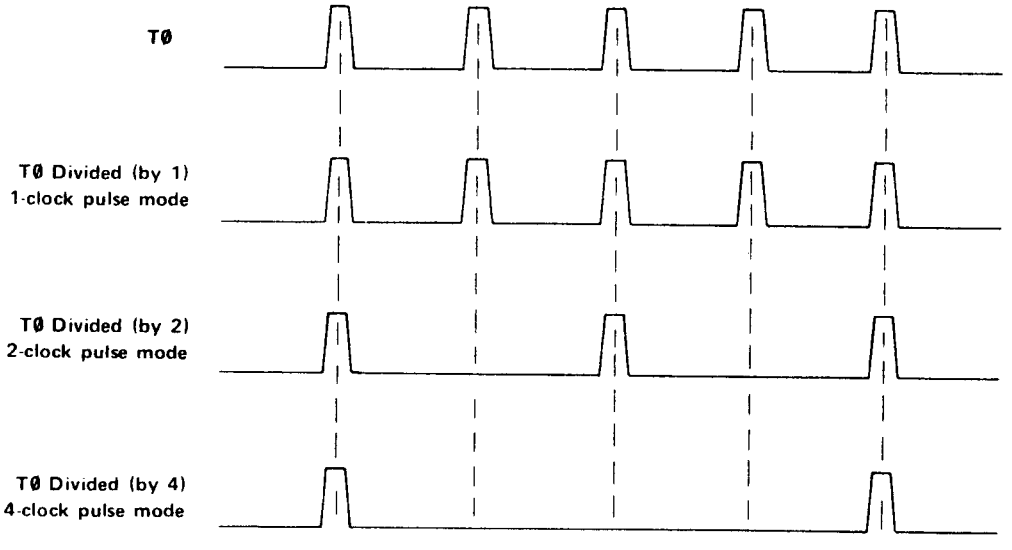
As mentioned previously, the Clock Generator outputs 14 clock phases. Each phase is delivered from the Clock Generator to a separate connector. The 14 phases are called phase 1 through phase 14 and are referenced to the TØ signal that marks the beginning of each clock cycle. Phases on 14-phase systems may be distributed in several ways. The distribution schemes run from a combination that uses 8 force phase and 6 compare phases through others that use 12 force phases and 2 compare phases.

The TØ Signal

The TØ signal determines the DUT test rate. During each TØ cycle, one test pattern row is applied to the DUT. This period can be programmed from 48 ns to 4.192 ms in two ranges (4.192 ms is achieved only in mode 4; see the description of modes).

As has been discussed, the sector cards have four modes of operation. Mode 1 requires one bit from each memory buffer for each clock cycle of the DUT, modes 2 and 3 each require two bits, and mode 4 requires four bits. Thus each memory buffer must be clocked 1, 2, and 4 times, respectively, for each clock cycle. The signal controlling the clocking of the memory buffers is therefore divided by 1, 2, or 4 to control the DUT cycle time. TØ (Divided) can thus be generated in one of three possible modes, called the 1-clock pulse, 2-clock pulse, or 4-clock pulse mode.

The cycle time programmed by the test writer is the TØD period.



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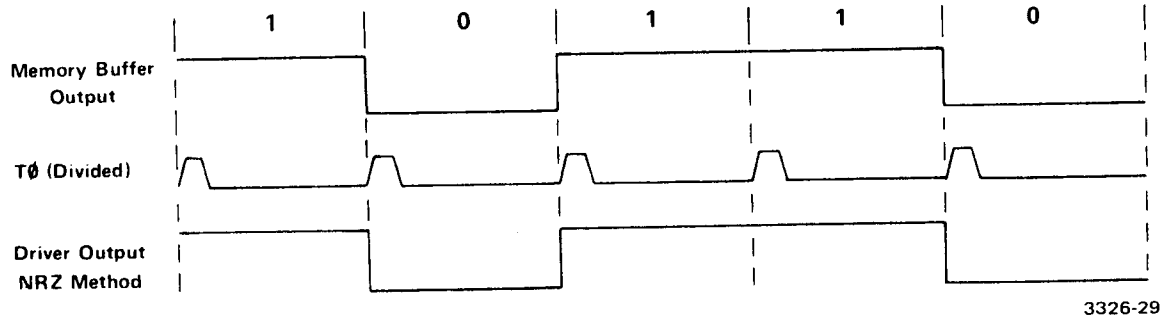
CLOCK PULSE MODE	SECTOR CARD MODE
1	1 (F,I,C,M)
2	2 and 3 (FC and FI,CM)
4	4 (FICM)

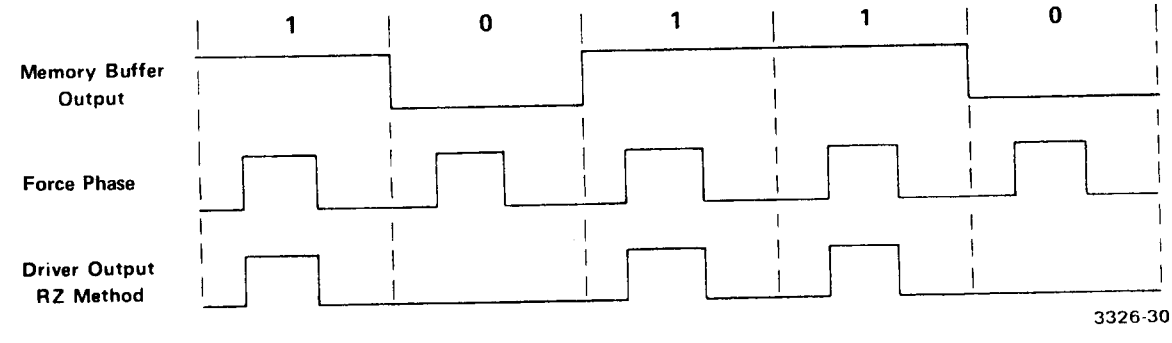
Force Data

Force data is sent to the DUT by one of four methods: non-return-to-zero (NRZ), return-to-zero (RZ), return-to-complement (RC), and return-to-inhibit (RI). In the NRZ method, the TØ (Divided) signal clocks a force bit into the driver at the beginning of each DUT cycle. In the RZ method, one of the Phase pulses gates the force bit into the driver.

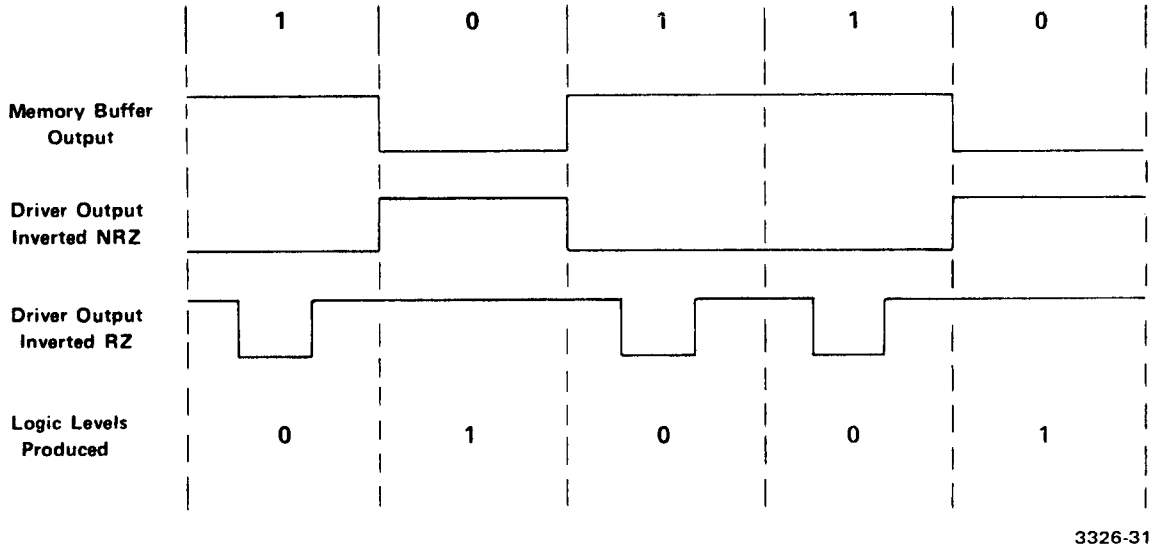
When using the NRZ method, the driver essentially follows the output of the memory buffer. At the beginning of each DUT cycle, the driver forces the DUT pin to the level that the force bit specifies. The pin is held at this level until the end of the cycle.



When using the RZ method, the driver output is held at the zero level until the force bit from the memory buffer is gated to the driver input. If the force bit is a one, the driver will go high for the duration of the gating pulse, then return to the zero level for the remainder of the cycle. If the force bit is a zero, the driver output will remain at zero for the whole cycle.

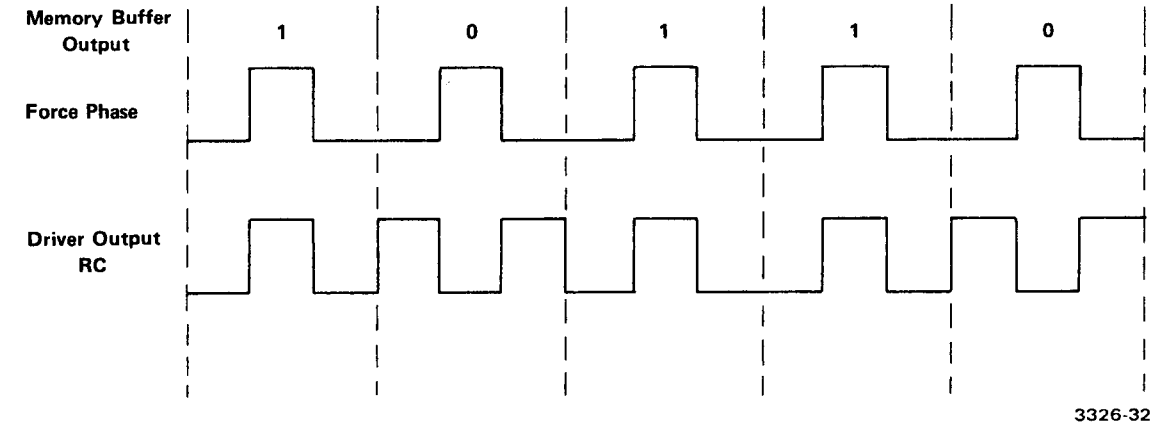


The output of the data stream can be inverted. Thus with the Inverted-NRZ method, the state of the force bit at the memory buffer is simply inverted at the driver output. The Inverted-RZ method, in this case, gives the complement of RZ, i.e., Return-to-One data.

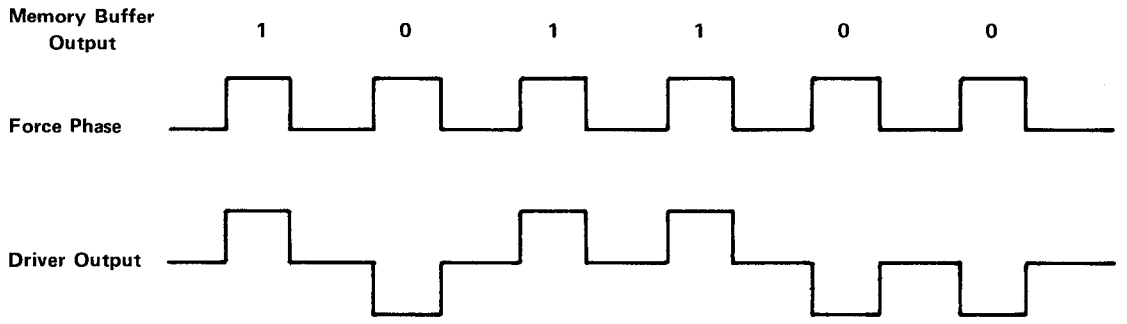


Note that to get Return-to-One data from the driver, you must call for Inverted-RZ data and complement the pattern column.

When using the RC method, the data is exclusive ORed with the clock phase.



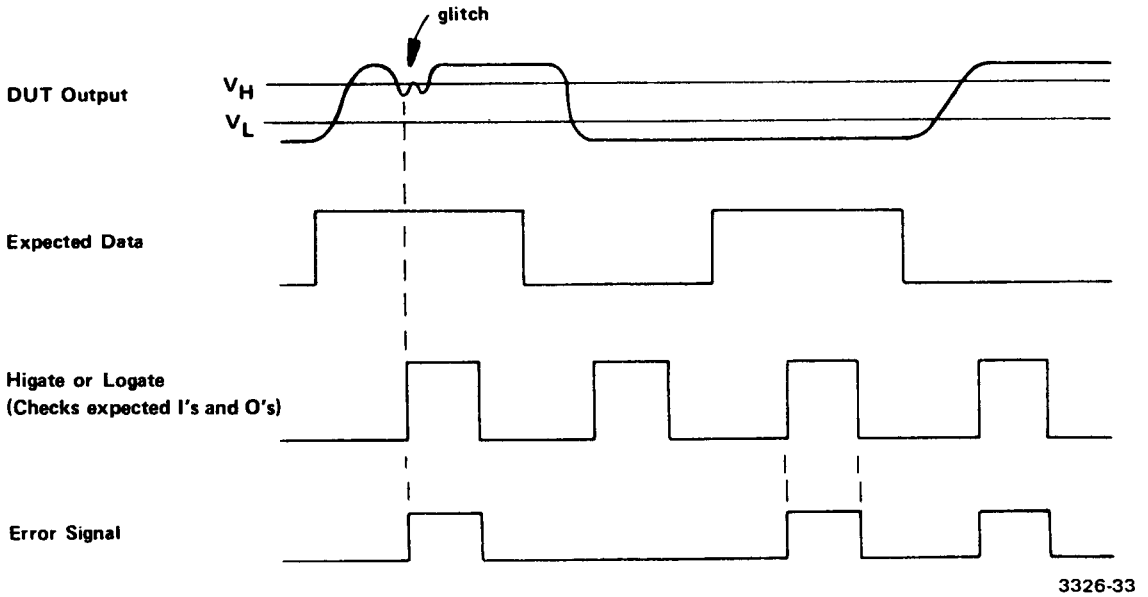
When using the RI method, the driver is inhibited when the phase is low. The driver forces the DUT only when the phase is high. The following diagram shows the driver inhibited by a midlevel voltage. This voltage, however, could be at any level between the high and low limits after the driver is inhibited.



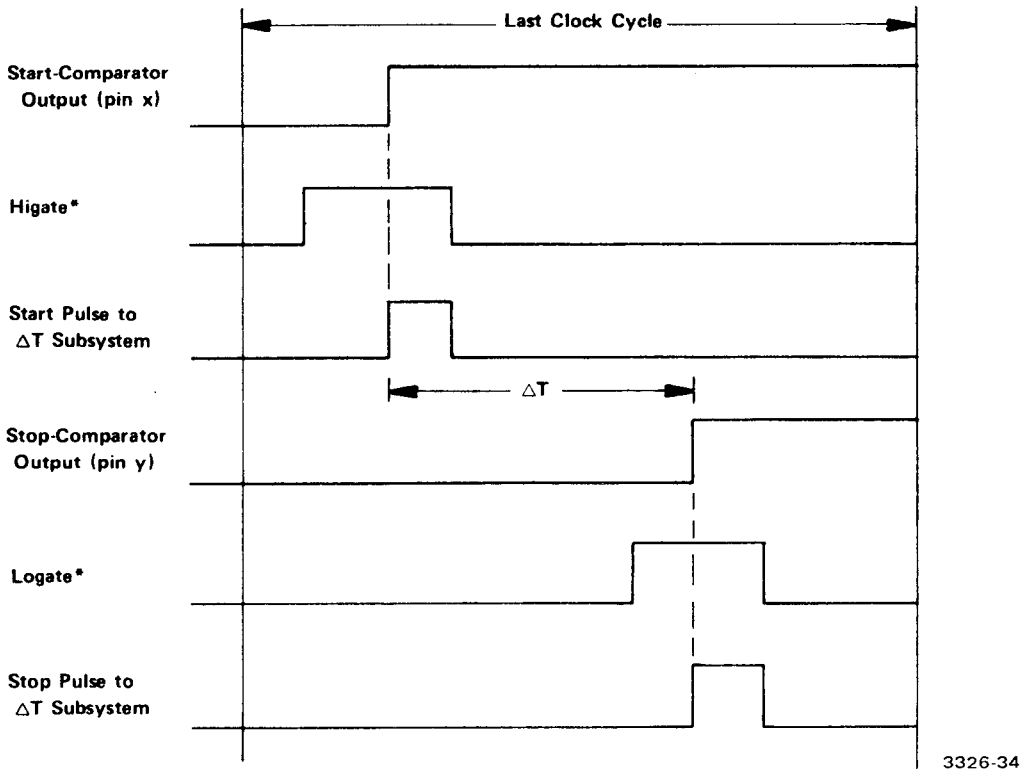
Compare Data

The Higate or Logate pulses gate the hicompare and locompare circuitry. When a comparator is gated, its output is transmitted to the error circuitry for the duration of the gate.

When using the comparators for functional testing, the gating pulses are set to start after the DUT output has gone to its expected level. The gating signal must end before the DUT output again changes state. Any transition of the DUT output through the comparison level during the gating signal causes an error to be recorded.



The comparators are also used in conjunction with the ΔT subsystem. The comparators in this case turn the ΔT subsystem on and off. One comparator (either hicompare or locompare), defined as the start comparator, turns the ΔT subsystem on when the output of the DUT pin crosses the specified level. Another comparator, the stop comparator, turns the ΔT subsystem off when the output of another DUT pin crosses a specified level. For time-difference measurements, the comparator transition must occur during the gating time. The resulting error has no meaning and should be masked by the test writer.



*Higate and Logate are normally set rather wide unless it is desired to blank out portions of the clock cycle to eliminate unwanted glitches, for example.