Tektronix®
COMMITTED TO EXCELLENCE

PM102/PM103
PERSONALITY MODULE FOR 6800/6802 MICROPROCESSORS

INSTRUCTION MANUAL

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PERSONALITY MODULE FOR 6800/6802 MICROPROCESSORS

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Tektronix, Inc.
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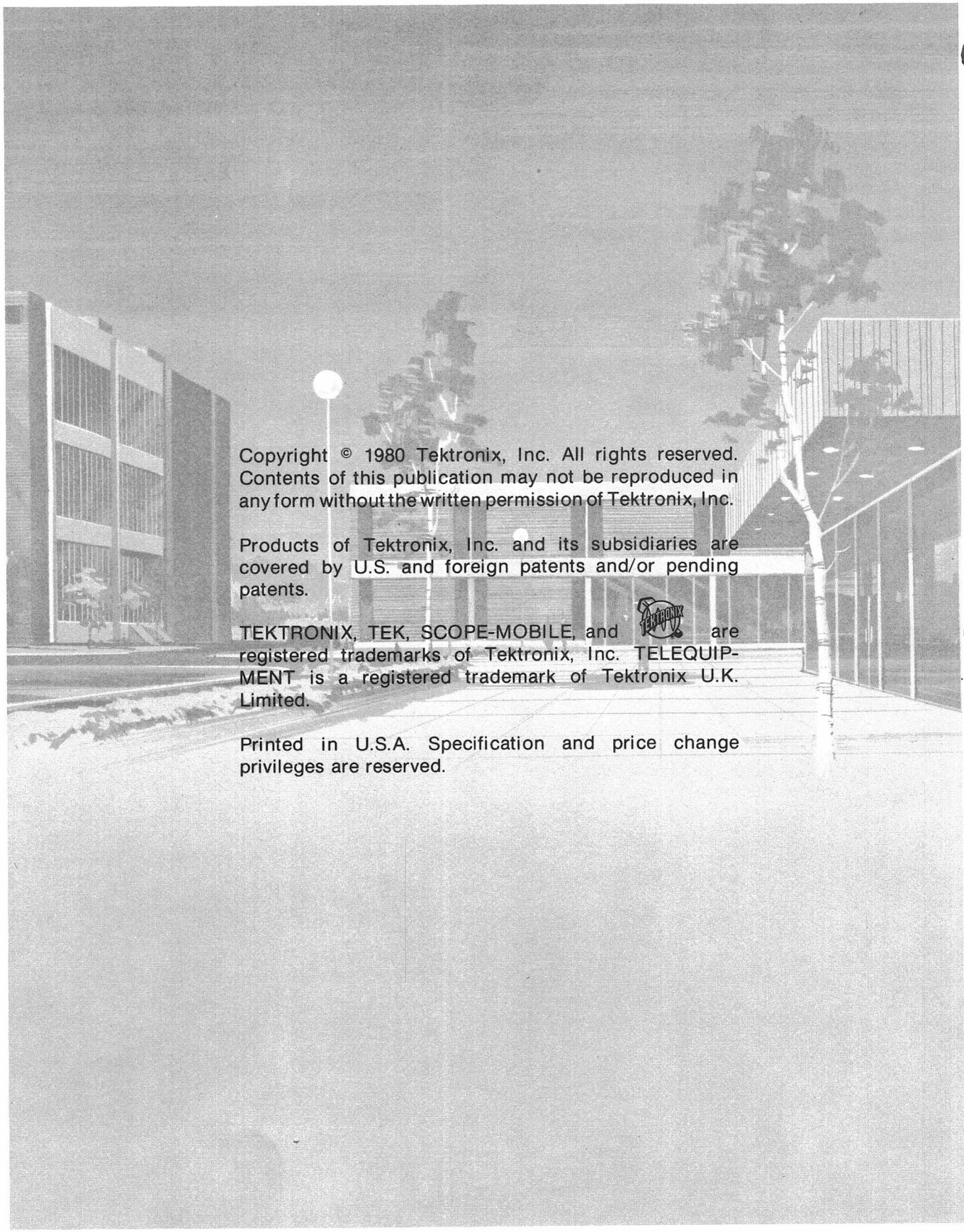

About This Manual

This manual describes operation and service of the PM102 and PM103 Personality Modules. The first part of the manual, the operator's part, describes connection of the personality modules to the logic analyzer, connection of the personality modules to the system under test (S.U.T.) and other information necessary for operation. The second part, the service part, is found after the colored divider page. That information is intended for use by qualified personnel in servicing the personality modules. It contains circuit descriptions, diagnostic technniques, schematic diagrams, and parts lists. Refer to the Table of Contents for the specific location of information.

Since the PM102 and PM103 are tools to aid design of 6800- and 6802-based products, Tektronix assumes that the reader has access to a Motorola M6800 Microcomputer System Design Data manual, or other manual relating to this microprocessor.

This manual often refers to a "logic analyzer." This means the 7D02 Logic Analyzer. It is assumed that the reader has access to a Tektronix 7D02 Operator's Manual and 7D02 Service Manual.

The PM102 supports the 6800, 68A00, and 68B00 microprocessors. The PM103 supports the 6802, 6808, and 68A02 microprocessors. Whenever a reference is made to the PM102/PM103, it means that whatever is being said applies to either personality module.

Throughout this manual, references are made to signals. The following conventions should be kept in mind:

1. The slash (/) preceding a signal name indicates the signal is active or asserted in the low state.
2. The components are numbered with assembly number, then component number. For example, A1U3040 is a component on assembly A1, the top board in the personality module pod. A2 is the bottom board. In Section 8, on the schematic for Board 1, component A1U3040 is shown without the assembly number, e.g. U3040.
3. For more information about signal lines, consult the Signal Glossary in Section 10.

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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

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List of Illustrations

OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

In This Manual

This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment

DANGER — High voltage.

Protective ground (earth) terminal.

ATTENTION — refer to manual.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts can render an electric shock.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Operate Without Covers

To avoid personal injury, do not operate this product without covers or panels installed.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

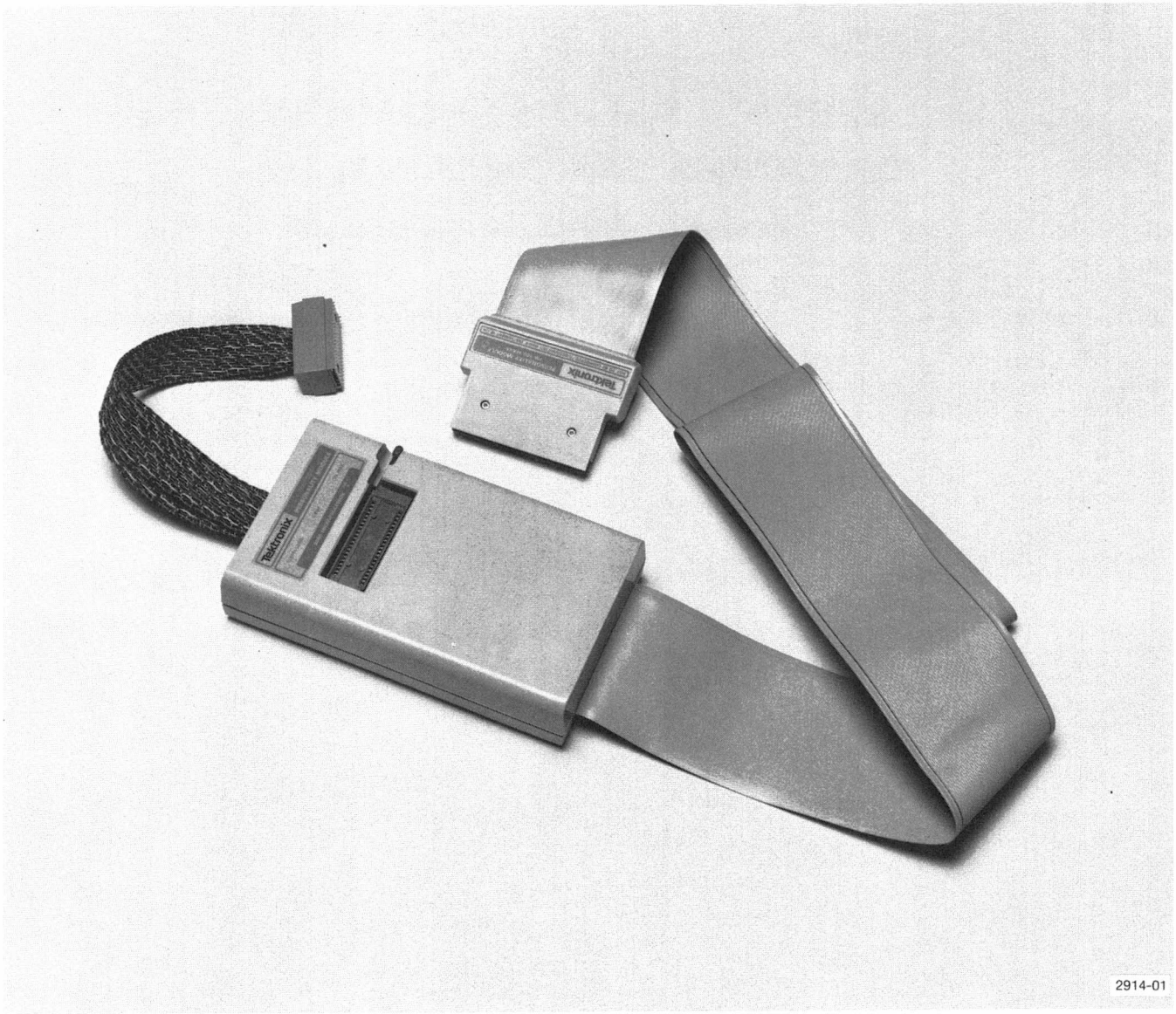
Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

To avoid personal injury, do not operate this product without covers or panels installed.

Disconnect power before removing protective panels, soldering, or replacing components.



The PM103 Personality Module.

INTRODUCTION TO THE PM102/PM103

The PM102/PM103 Personality Module collects data from a 6800/6802-based system-under-test (S.U.T.) and transfers it to a Tektronix logic analyzer in a format that the logic analyzer can interpret.

The microprocessor in the S.U.T. is removed and plugged into the personality module. The microprocessor plug on the personality module is then inserted into the S.U.T., replacing the microprocessor. The microprocessor then drives the S.U.T. as before, through the personality module. This allows the logic analyzer to acquire data by monitoring the address, control, data, and clock lines. The personality module also generates additional information needed by the logic analyzer.

Physically, the PM102/PM103 personality module consists of a circuitry pod with a ribbon cable and logic analyzer plug on one end, and a twisted-pair woven cable and microprocessor plug on the other end.

The personality module pod contains:

a. An interface assembly that "personalizes" the logic analyzer to work with the 6800/6802 microprocessor.

b. A zero-insertion-force (ZIF) socket on the pod for the 6800 or 6802 microprocessor from the system under test.

c. Firmware that allows the logic analyzer to disassemble the information it receives into the mnemonics of the 6800/6802, and set up displays.

d. Circuitry to generate the state clock, and other inputs to the logic analyzer.

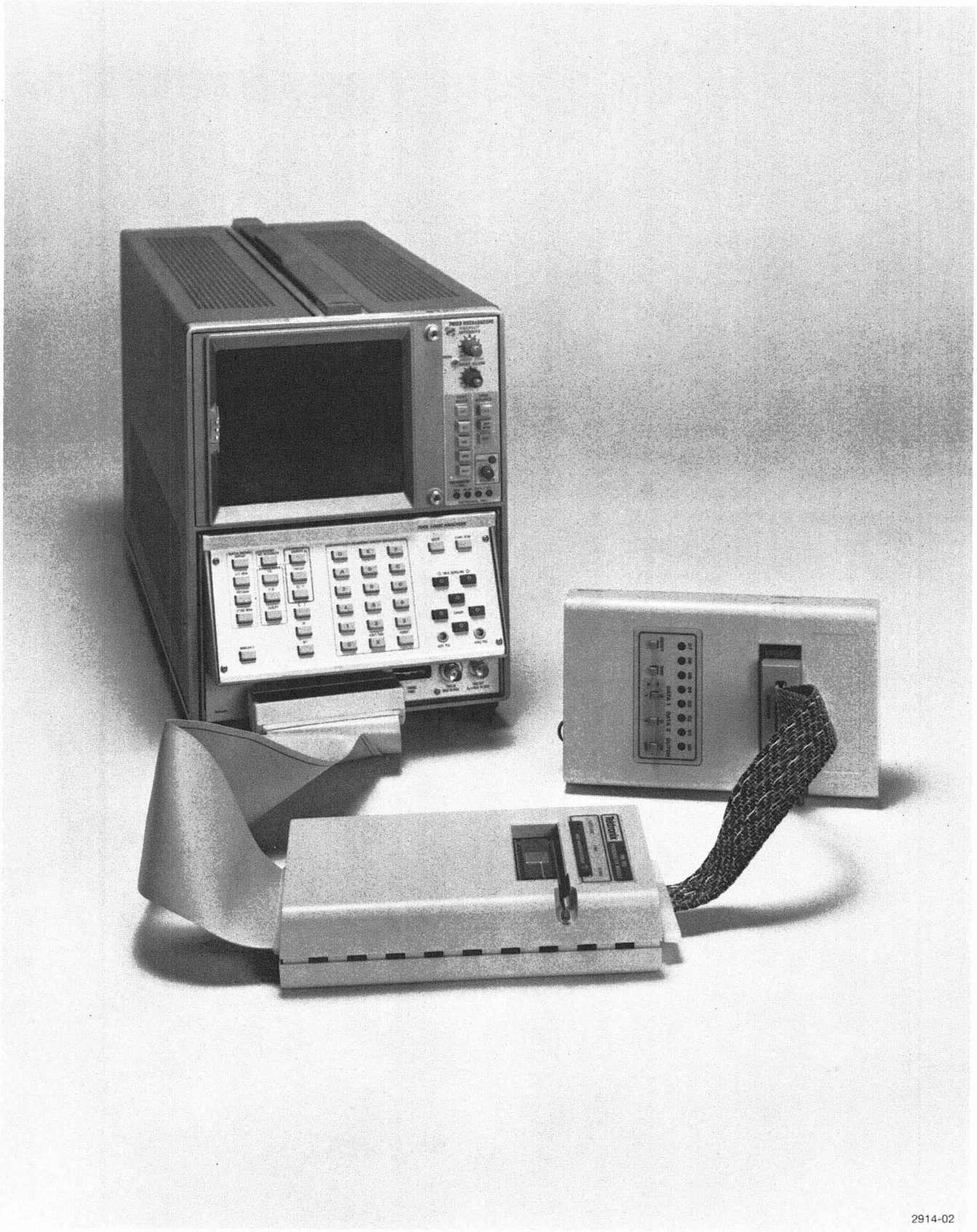


Fig. 1-1. The PM103 Personality Module.

Personality module is connected to 7D02 logic analyzer and system-under-test. Notice the microprocessor in the zero-insertion-force (ZIF) socket of the PM103.

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OPERATING INSTRUCTIONS FOR THE PM102/PM103 PERSONALITY MODULE

Storage and Installation of Personality Module

Storing the Personality Module

When storing the Personality Module, protect the P.M. microprocessor plug with the plastic protector, part number 200-2445-00. This prevents damage to the pins during storage and protects the Personality Module from static electricity.

Connecting Personality Module to Logic Analyzer

CAUTION

Always turn the mainframe power switch OFF before connecting the Personality Module to the logic analyzer mainframe. Before removing the microprocessor from your system under test and installing the microprocessor plug, turn off your system power switch. Failure to take this precaution may cause permanent damage to the logic analyzer, the personality module, and the system under test.

1. Turn mainframe power switch to the OFF position.
2. Insert the PM102/PM103 logic analyzer plug, label side up, into the socket on the front of the Logic Analyzer.

Connecting Personality Module to the system under test (S.U.T.).

1. Turn OFF the power to your S.U.T. and the logic analyzer.
2. Ground yourself to drain static electricity.
3. Remove the microprocessor from your S.U.T. and insert it into the ZIF socket in the Personality Module Pod. Be sure to insert it correctly, with pin 1 of your microprocessor next to the lever on the ZIF socket.
4. Plug the PM microprocessor plug into the empty microprocessor socket on your S.U.T. Again, make sure to insert the plug correctly. Pin 1 of the microprocessor plug is marked with a notch and an arrow.
5. Turn on the logic analyzer mainframe power switch and power up your S.U.T.

NOTE

To save wear to the microprocessor socket on your S.U.T., you may insert another socket into your S.U.T. socket.

A socket appropriate for this purpose is available through your Tektronix Field Office, part number 136-0623-00.

Using personality module

The 7D02 Operator's Manual provides general operating information for use with all personality modules. The 7D02 will operate slightly differently when used with each different personality module.

This sub-section is devoted to operating the 7D02 with a PM102/PM103 Personality Module.

7D02 Displays

The following 7D02 screen displays contain PM102/103-specific elements. For more information about signal lines, consult Section 4, Theory of Operation, and Section 10, Signal Glossary.

- WD RECOGNIZER event format

When the PM102/PM103 is attached to the 7D02, the 7D02 WD RECOGNIZER key will produce the following test display. The radices of the data bus and address bus may be changed with the 7D02 FORMAT key.

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX
1 ADDRESS=XXXX
1 /NMI=X /IRQ=X FETCH=X R/W=X
1 BA=X INVAL OP=X EXT TRIG IN=X
1 TIMING WR=X
1THEN DO
1
```

DATA—The 8-bit data bus, normally in hexadecimal, unless changed with the FORMAT key. The logic analyzer stores information from the data bus when a program is run.

ADDRESS—The 16-bit address bus, normally in hexadecimal, unless changed with the FORMAT key. The 7D02 stores information from the address bus when a program is run.

/NMI—This is a latched non-maskable interrupt line, not to be confused with the /NMI pin on the processor-under-test. The /NMI is generated by the personality module when the /NMI pin on the microprocessor is low. The /NMI is held low until the next valid memory address is asserted. The 7D02 will recognize an /NMI if a 0 is entered for this element. The radix for this element is always binary. The logic analyzer stores information on this line when the program is run.

/IRQ—The /IRQ pin on the microprocessor. The 7D02 will recognize an /IRQ interrupt request if a 0 is inserted for this element. The radix for this element is always binary. The logic analyzer stores information on this line as a program is run.

FETCH—The instruction fetch line to the logic analyzer. This line is generated by the personality module. See Section 4 for a detailed description of this line. When the FETCH line is high, the first byte of a 6800/6802 instruction is on the data bus. For the 7D02 to recognize an instruction fetch, the FETCH element requires a 1. The radix for this element is always binary. The logic analyzer stores information from this line as the program is run.

R/W—The read/write line tells the user that the microprocessor is in a Read (1) or Write (0) state. The logic analyzer stores information from the R/W line as the program is run.

BA—The bus available signal from the microprocessor to the S.U.T. BA is normally in a 0 state. When it goes to 1, it indicates that the microprocessor has stopped and the address bus, data bus, and R/W line are in tri-state and available. This will occur if the microprocessor has halted, or after a WAI instruction. Information from the BA line is not stored by the logic analyzer.

INVAL OP—The invalid op code signal to the logic analyzer. This signal is generated by the personality module. It indicates that the op code on the bus at the last instruction fetch cycle was illegal. See Section 4 for a detailed description of this line. The 7D02 will recognize an invalid op code if a 1 is inserted for this element. The logic analyzer does not store information from this line.

- TRIGGER command format

```
1 TRIGGER 0-MAIN
1           0-MAIN
1           1-TIMING
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    0-STANDARD CLOCK QUAL.
```

The only field of specific interest to the PM102/PM103 user is the

```
0-STANDARD CLOCK QUAL.
```

When the cursor is placed on this element, this display appears:

```
0-STANDARD CLOCK QUAL.
 0 STANDARD CLOCK QUAL.
 1 USER CLOCK QUAL.
```

If "1 USER CLOCK QUAL." is selected, the following display appears:

```
 1-FALLING EDGE OF CLOCK
  0 RISING EDGE OF CLOCK
  1 FALLING EDGE OF CLOCK
C9-C4 (ANDED CLOCKS)=XXX1XX
```

C9-C4, shown in the above example, are PM102/PM103 control lines that may be used to re-define the state clock. The selected state is ANDED with the selected state of the pin 37 clock. If both states are true, a clock is generated.

NOTE

Redefining the state clock is not a normally recommended procedure, and may produce unpredictable results.

If the TRIGGER-MAIN command is deleted from the program, the values last entered in the USER CLOCK QUAL. will be retained. STANDARD CLOCK QUAL. is restored after logic analyzer power-up.

Notice the default value of 1 given to C6. This is the VMA (Valid Memory Address) line, explained below.

If none of the control lines are set to be ANDED with the clock, the 7D02 will use all pin 37 clock cycles.

For example, if the display is

```
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXX1XX
```

then the 7D02 clocks when

1. pin 37 is on the falling edge, AND
2. VMA is in its high state.

See Fig. 2-1.

C9 /RESET. The reset pin on the microprocessor. The /RESET is an input line to the microprocessor that resets and starts the microprocesor from a power-down condition. When this line first goes high after a power down or system reset, the microprocessor begins the software restart sequence. If the /RESET element is 1, the 7D02 clock qualifies on the software restart sequence of the S.U.T. C8=This line is connected to ground. It will always be in the "0" state.

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C7=/HALT is line from the PM102/PM103 to the logic analyzer. This line tells the logic analyzer that the microprocessor of the system under test is in a halt state at the command of either the logic analyzer or the system. 7D02 clock qualifies on a halt state if a 0 is entered for this element.

C6=VMA The valid memory address pin on the processor that, when high, tells the S.U.T. that a valid memory address is on the address bus. Note the default value of 1, or "clock qualify on VMA line positive".

C5=IOC The illegal op code line to the logic analyzer from the personality module. Because it goes to its active state one cycle after an illegal op code, its use as a clock qualifier is not recommended.

C4=BA The bus available line from the microprocessor to the S.U.T. It goes high when the microprocessor enters a halt state or when the S.U.T. executes a WAI instruction.

- FORMAT mode display

When the PM102/PM103 is installed in a 7D02 logic analyzer with a timing option, the 7D02 FORMAT key produces the following default display.

```
TIMING OPTION WORD RECOGNIZER
   0-BINARY
WORD RECOGNIZER ADDRESS FIELD
   2-HEX
WORD RECOGNIZER DATA FIELD
   2-HEX
TIMING OPTION DATA DISPLAY
   0-BINARY
ADDRESS FIELD DISPLAY
   2-HEX
DATA FIELD DISPLAY
   2-HEX
HIGHLIGHT MEMORY DIFFERENCES?
   1-NO
DISPLAY GLITCHES?
   0-YES
TIMING OPTION DATA INVERSION
   DATA=00000000
```

The WORD RECOGNIZER ADDRESS FIELD menu sets the radix for the ADDRESS field in the WD RECOGNIZER display. Its default state is hexadecimal. It does not affect the acquired display.

The WORD RECOGNIZER DATA FIELD menu sets the radix for the DATA field in the WD RECOGNIZER display. Its default state is hexadecimal. It does not affect the acquired data display.

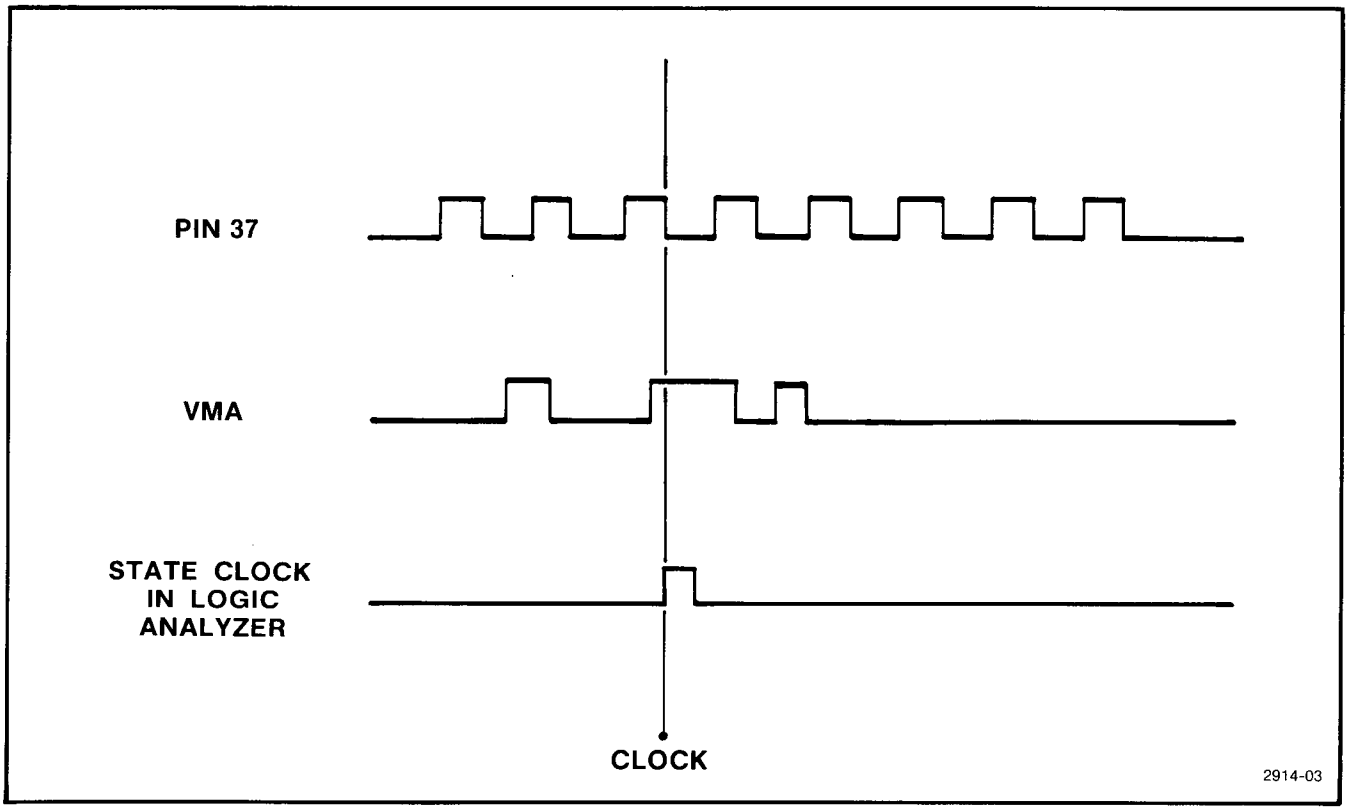

Fig. 2-1. State Clock Generation.

The ADDRESS FIELD DISPLAY sets the radix for the acquired address data when displayed in Absolute display mode. Its default radix is hexadecimal.

The DATA FIELD DISPLAY sets the radix for the acquired data when displayed in Absolute display mode. Its default radix is hexadecimal.

- Absolute Display of Acquired Data

The 7D02 with the PM102/PM103 will produce an Absolute display format like the one in Fig. 2-2, unless the 7D02 FORMAT key has been used to change the radices:

```
LOC      ADDRESS     DATA   CNTL
000       494B        6B     R10
001       494C        8C     W10
002       494D        AD     F10
```

Fig. 2-2. Absolute Display.

where:

LOC is a decimal number, 0-255, indicating the location in 7D02 acquisition memory. In order of acquisition, 000 is the oldest acquired data, and 255 is the newest.

ADDRESS is a value in the 6800/6802 address bus. Its default radix is hexadecimal unless changed with 7D02 FORMAT key.

DATA is value on the 6800/6802 data bus. Its default radix is hexadecimal unless changed with 7D02 FORMAT key.

CNTL is made up of three characters:

1. An F, R, or W
   a. F stands for Fetch, indicating the acquired data was a 6800/6802 instruction. Compare location 002 in Fig. 2-2 and Fig. 2-3.
   b. R stands for Read, indicating the acquired data is a read cycle. Compare location 000 in Fig. 2-2 and Fig. 2-3.
   c. W stands for write, indicating the acquired data is a write cycle. Compare location 001 in Fig. 2-2 and Fig. 2-3.
2. The state of the /IRQ line. If a 0 is present, it indicates an interrupt is being requested.
3. The state of /NMI. If a 0 is present, it indicates an interrupt is being requested.

- Mnemonic Disassembly Display of Acquired Data

The 7D02 when used with the PM102/PM103 produces a mnemonic disassembly display like the one in Fig. 2-3.

The Mnemonic Disassembly Display cannot be changed with the 7D02 FORMAT key.

```
LOC   ADDRESS OPERATION /IRQ/NMI
000    494B     6B READ     10
001    494C     8C WRITE    10
002    494D    JSR    $0E,X 10
```

Fig. 2-3. Mnemonic Disassembly Display.

LOC is a decimal number, 0-255, indicating the location in 7D02 acquisition memory. In order of acquisition, 000 is the oldest acquired data, and 255 is the newest.

ADDRESS is a value in the 6800/6802 address bus. Its radix is hexadecimal.

OPERATION is the disassembled data on the 6800/6802 data bus, including data and a READ or WRITE statement, or 6800/6802 instruction mnemonics and operands. Compare Fig. 2-2 and Fig. 2-3. You will find the same information, per memory location, in both Absolute and Mnemonic Disassembly displays.

/IRQ/NMI indicates the states of the /IRQ and /NMI control lines, respectively. In both cases, if a 0 is present, it indicates an interrupt request.

The mnemonic disassembly display cannot be changed with the 7D02 FORMAT command.

An illegal op code in the data bus may cause an incorrect disassembly. A series of asterisks (***) in the OPERATION field indicates the microprocessor attempted to execute an illegal opcode.

If a series of question marks (???) appears the instruction fetch predictor circuitry incorrectly predicted a FETCH cycle. This may be due to the microprocessor attempting to execute an illegal opcode. The best way to resume operation is to reset the system under test.

@

NOTE

Correct mnemonic disassembly of acquired data is guaranteed only if 1) data qualification is not used at all (so that all cycles are stored) or 2) if data qualification is used, all Fetch Cycles are stored also.

This may be accomplished by using the QUALIFY block. Store only on Word Recognizer N, where the Word Recognizer is set to all "Don't Care", except FETCH = 1. This guarantees that all instruction fetches will be stored.

6800/6802 Instruction Set

The table below provides a detailed description of the information present on the Address Bus, Data Bus, Valid Memory Address line (VMA), and the Read/Write line (R/W) during each cycle for each instruction.

This information is useful in comparing actual with expected results during debug of both software and hardware. The information is categorized in groups according to addressing mode and number of cycles per instruction.

Fig. 2-4. 6800/6802 Instruction Set.

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
IMMEDIATE						
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	2	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Operand Data
CPX LDS LDX	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Operand Data (High Order Byte)
		3	1	Op Code Address + 2	1	Operand Data (Low Order Byte)
DIRECT						
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	1	Address of Operand	1	Operand Data
CPX LDS LDX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	1	Address of Operand	1	Operand Data (High Order Byte)
		4	1	Operand Address + 1	1	Operand Data (Low Order Byte)
STA	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Destination Address
		3	0	Destination Address	1	Irrelevant Data (Note 1)
		4	1	Destination Address	0	Data from Accumulator
STS STX	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	0	Address of Operand	1	Irrelevant Data (Note 1)
		4	1	Address of Operand	0	Register Data (High Order Byte)
		5	1	Address of Operand + 1	0	Register Data (Low Order Byte)
INDEXED						
JMP	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Operand Data
CPX LDS LDX	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Operand Data (High Order Byte)
		6	1	Index Register Plus Offset + 1	1	Operand Data (Low Order Byte)

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Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
INDEXED (Continued)						
STA	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		6	1	Index Register Plus Offset	0	Operand Data
ASL LSR ASR NEG CLR ROL COM ROR DEC TST INC	7	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Current Operand Data
		6	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		7	1/0 (Note 3)	Index Register Plus Offset	0	New Operand Data (Note 3)
STS STX	7	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		6	1	Index Register Plus Offset	0	Operand Data (High Order Byte)
		7	1	Index Register Plus Offset + 1	0	Operand Data (Low Order Byte)
JSR	8	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer	0	Return Address (Low Order Byte)
		5	1	Stack Pointer − 1	0	Return Address (High Order Byte)
		6	0	Stack Pointer − 2	1	Irrelevant Data (Note 1)
		7	0	Index Register	1	Irrelevant Data (Note 1)
		8	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
EXTENDED						
JMP	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Jump Address (High Order Byte)
		3	1	Op Code Address + 2	1	Jump Address (Low Order Byte)
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Operand Data
CPX LDS LDX	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Operand Data (High Order Byte)
		5	1	Address of Operand + 1	1	Operand Data (Low Order Byte)
STA A STA B	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Destination Address (High Order Byte)
		3	1	Op Code Address + 2	1	Destination Address (Low Order Byte)
		4	0	Operand Destination Address	1	Irrelevant Data (Note 1)
		5	1	Operand Destination Address	0	Data from Accumulator
ASL LSR ASR NEG CLR ROL COM ROR DEC TST INC	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Current Operand Data
		5	0	Address of Operand	1	Irrelevant Data (Note 1)
		6	1/0 (Note 3)	Address of Operand	0	New Operand Data (Note 3)

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Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
EXTENDED (Continued)						
STS STX	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	0	Address of Operand	1	Irrelevant Data (Note 1)
		5	1	Address of Operand	0	Operand Data (High Order Byte)
		6	1	Address of Operand + 1	0	Operand Data (Low Order Byte)
JSR	9	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Subroutine (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Subroutine (Low Order Byte)
		4	1	Subroutine Starting Address	1	Op Code of Next Instruction
		5	1	Stack Pointer	0	Return Address (Low Order Byte)
		6	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		7	0	Stack Pointer – 2	1	Irrelevant Data (Note 1)
		8	0	Op Code Address + 2	1	Irrelevant Data (Note 1)
		9	1	Op Code Address + 2	1	Address of Subroutine (Low Order Byte)
INHERENT						
ABA DAA SEC ASL DEC SEI ASR INC SEV CBA LSR TAB CLC NEG TAP CLI NOP TBA CLR ROL TPA CLV ROR TST COM SBA	2	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
DES DEX INS INX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Previous Register Contents	1	Irrelevant Data (Note 1)
		4	0	New Register Contents	1	Irrelevant Data (Note 1)
PSH	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	1	Stack Pointer	0	Accumulator Data
		4	0	Stack Pointer – 1	1	Accumulator Data
PUL	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Operand Data from Stack
TSX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	0	New Index Register	1	Irrelevant Data (Note 1)
TXS	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Index Register	1	Irrelevant Data
		4	0	New Stack Pointer	1	Irrelevant Data
RTS	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 2)
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Address of Next Instruction (High Order Byte)
		5	1	Stack Pointer + 2	1	Address of Next Instruction (Low Order Byte)

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Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
INHERENT (Continued)						
WAI	9	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	1	Stack Pointer	0	Return Address (Low Order Byte)
		4	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		5	1	Stack Pointer – 2	0	Index Register (Low Order Byte)
		6	1	Stack Pointer – 3	0	Index Register (High Order Byte)
		7	1	Stack Pointer – 4	0	Contents of Accumulator A
		8	1	Stack Pointer – 5	0	Contents of Accumulator B
		9	1	Stack Pointer – 6 (Note 4)	1	Contents of Cond. Code Register
RTI	10	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 2)
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Contents of Cond. Code Register from Stack
		5	1	Stack Pointer + 2	1	Contents of Accumulator B from Stack
		6	1	Stack Pointer + 3	1	Contents of Accumulator A from Stack
		7	1	Stack Pointer + 4	1	Index Register from Stack (High Order Byte)
		8	1	Stack Pointer + 5	1	Index Register from Stack (Low Order Byte)
		9	1	Stack Pointer + 6	1	Next Instruction Address from Stack (High Order Byte)
		10	1	Stack Pointer + 7	1	Next Instruction Address from Stack (Low Order Byte)
SWI	12	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 1)
		3	1	Stack Pointer	0	Return Address (Low Order Byte)
		4	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		5	1	Stack Pointer – 2	0	Index Register (Low Order Byte)
		6	1	Stack Pointer – 3	0	Index Register (High Order Byte)
		7	1	Stack Pointer – 4	0	Contents of Accumulator A
		8	1	Stack Pointer – 5	0	Contents of Accumulator B
		9	1	Stack Pointer – 6	0	Contents of Cond. Code Register
		10	0	Stack Pointer – 7	1	Irrelevant Data (Note 1)
		11	1	Vector Address FFFA (Hex)	1	Address of Subroutine (High Order Byte)
		12	1	Vector Address FFFB (Hex)	1	Address of Subroutine (Low Order Byte)
RELATIVE						
BCC BHI BNE BCS BLE BPL BEQ BLS BRA BGE BLT BVC BGT BMI BVS	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Branch Offset
		3	0	Op Code Address + 2	1	Irrelevant Data (Note 1)
		4	0	Branch Address	1	Irrelevant Data (Note 1)
BSR	8	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Branch Offset
		3	0	Return Address of Main Program	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer	0	Return Address (Low Order Byte)
		5	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		6	0	Stack Pointer – 2	1	Irrelevant Data (Note 1)
		7	0	Return Address of Main Program	1	Irrelevant Data (Note 1)
		8	0	Subroutine Address	1	Irrelevant Data (Note 1)

Note 1. If device which is addressed during this cycle uses VMA, then the Data Bus will go to the high impedance three-state condition. Depending on bus capacitance, data from the previous cycle may be retained on the Data Bus.
Note 2. Data is ignored by the MPU.
Note 3. For TST, VMA = 0 and Operand data does not change.
Note 4. While the MPU is waiting for the interrupt, Bus Available will go high indicating the following states of the control lines: VMA is low; Address Bus, R/W, and Data Bus are all in the high impedance state.

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SPECIFICATIONS

INTERFACE TO LOGIC ANALYZER (64 PINS)

PIN	SIGNAL	DESCRIPTION
1	AI1	STTL OUTPUT BACK TERMINATED TO 68 OHMS
2	CLK	DIFFERENTIAL ECL LEVEL, HI -0.8V. LO -1.7V. DIFFERENTIALLY TERMINATED INTO 124 OHMS.
3	/CLK	ECL LEVEL; HI -0.8V. LO -1.7V. DIFFERENTIALLY TERMINATED INTO 124 OHMS
4	AI3	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
5	AI0	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
6	AI5	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
7	AI2	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
8	AI6	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
9	AI4	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
10	GND	GROUND
11	AI7	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
12	AI8	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
13	AI9	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
14	AI11	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
15	AI10	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
16	AI13	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
17	AI12	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
18	AI15	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
19	AI14	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
20	GND	GROUND
21	N/C	
22	N/C	
23	N/C	
24	N/C	
25	N/C	
26	N/C	
27	N/C	
28	N/C	
29	DI1	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
30	GND	GROUND
31	DI3	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
32	DI0	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
33	DI4	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
34	DI2	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
35	DI6	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
36	DI5	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
37	N/C	
38	DI7	STTL OUTPUT BACK TERMINATED INTO 68 OHMS
39	N/C	
40	GND	GROUND
41	N/C	
42	N/C	

43	N/C	
44	N/C	
45	+5V	TTL SUPPLY
46	N/C	
47	C0	READ/WRITE STTL OUTPUT BACK TERMINATED INTO 68 OHMS
48	N/C	
49	C2	/IRQ STTL OUTPUT BACK TERMINATED INTO 68 OHMS
50	GND	GROUND
51	C5	IOC STTL OUTPUT BACK TERMINATED INTO 68 OHMS
52	C1	/NMI STTL OUTPUT BACK TERMINATED INTO 68 OHMS
53	10C7	/HALT STTL OUTPUT BACK TERMINATED INTO 68 OHMS
54	C3	IFC (FETCH) STTL OUTPUT BACK TERMINATED INTO 68 OHMS
55	C9	/RESET STTL OUTPUT BACK TERMINATED INTO 68 OHMS
56	C4	BA STTL OUTPUT BACK TERMINATED INTO 68 OHMS
57	+5V	TTL SUPPLY
58	+15V	SUPPLY
59	-15V	SUPPLY
60	C6	VMA STTL OUTPUT BACK TERMINATED INTO 68 OHMS
61	/HALT PUT	1 LSTTL INPUT LOAD
62	C8	GROUNDED
63	/SEL P	4 LSTTL INPUT LOADS
64	LOOK	4 LSTTL INPUT LOADS

SYSTEM DESCRIPTION

Control Lines

/HALT PUT is an output from the logic analyzer. The 6800/6802 generates /STOP PUT from the /HALT PUT signal.

LOOK is a control line generated by the 7D02 that disables the A10-A15 and D10-D17 buffers in the Personality Module.

/SEL P is a control line generated by the 7D02 that is used to read the PROM in the personality module.

Electrical Specifications

Items listed in the Supplemental Information column are either explanatory notes or performance characteristics for which no limits are specified. They may not be verified.

Microprocessor Compatability

PM102	6800 68A00 68B00
PM103	6802 68A02 6808

Signal Inputs

Maximum number of channels	33	
	Data	8
	Address	16
	Control	9

Clock

Maximum Frequency	
PM102	2 MHz (6800)
PM103	6 MHz (6802)

Display

Maximum Number of Channels Displayed	28	
	Data 8	
	Address 16	
	Control 4	
	Read/Write	C0
	/NMI	C1
	/IRQ	C2
	FETCH	C3
Qualifiers Not Displayed	BA	C4
	IOC	C5
	VMA	C6
	/HALT	C7
	/RESET	C9

Processor Halt

Schottky TTL level that is approximately 90 ns after the 7D02 stops acquisition. In zero delay mode, this is 2 qualified state clocks after the trigger event is clocked into the 7D02.

Data Input Channels

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
TTL Input Levels		0V-7V Signal Swings 1/2 LSTTL Load
Input Capacitance		40 pf nominal
Voltage in low limits (operating)	Min. 0.0V, max. 0.6V	
Voltage in high limits (operating)	Min. 2.0V, max. 7.0V	
Hysteresis		0.2V min.
Current in low limits (V. in low=0.4V)		-0.2 mA max.
Current in high limits (V in =7.0V)		0.1 mA max.
Current in high limits (V in high =+2.7V)		+0.02 mA max.
Maximum voltage in, non-operating, non-destructive		-15V to +15V continuous on any two inputs simultaneously
Threshold Voltage		Fixed +1.4V nominal Nominal hysteresis 0.4V TTL compatible
HALT output drive		
VOH VOL		2.4V, IO=1mA 5V, IO=-1mA

Clock Input Pin 37

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Input Resistance		50K ohms nominal
Input Capacitance		35 pF nominal
Clock Period	500 ns min.	
Clock Pulse Width (min.)	180 ns high, 180 ns low	
Voltage in low limits (operating)	Min. 0.0V, Max. 0.6V	
Voltage in high limits (operating)	Min. 2.0V, Max. 7.0V	
Hysteresis		.4 V. nominal
Threshold Voltage		Fixed 1.4V nominal
Maximum voltage in non-operating non-destructive		-15V to +15V

Propagation Delays Through Personality Module

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Delay through ECL clock		10.5 to 14.5 ns
Delay added to /PHALT line (from replacement plug to micro-processor	55 ns max.	
Channel delay		
IOC (clocked)		60 ns min., 150 ns max.
/NMI		35 ns min., 75 ns max.
INST FETCH (clocked)		40 ns min., 95 ns max.
Delay, data channel DIO-7		25 ns min., 45 ns max.

Propagation Delays Through Personality Module (contd.)

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Delay, all other channels		20 ns min., 50 ns max.

Test Clock

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Clock Period		400 ns min., 500 ns max.
Clock Pulse Width (high or low)		135 ns min.

System Specifications with Logic Analyzer

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Setup time		
C0, C2, C4, C6, C9		40 ns approx.
C7		100 ns approx.
Hold Time		0 ns max.
Data DI0-7		
Set-up Time	40 ns	
Hold Time	0.0 ns	
Data Acquisition Period	500 ns. min.	

Mechanical Specifications

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Size		4.7" x 8" x 1.7" (12 x 20.3 x 4.3 cm.)
Weight		Approx. 2 lbs. with cables (approx. 1 Kg. with cables)
Cable length (Logic Analyzer to pod)		4 ft. plus/minus 1.0 in. (122 cm. plus/minus 2.5 cm)
Cable Length Replacement plug to personality module conductor in module pod		13 inches plus/minus 1/2 inch (33 cm. plus/minus 1.3 cm)

Environmental Specifications

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Temperature		
Operating		-15 degrees C to +55 degrees C
Non-operating		-62 degrees C to +85 degrees C
Relative Humidity		95-97% non-condensing
Altitude		
Operating		4.5 Km (15,000 feet)
Non-operating		15 Km (50,000 feet)

PM102/PM103 Microprocessor Plug

TO POD CONNECTOR	ZIF	PROTECTION PM103	PROTECTION PM102	SIGNAL NAME PM103	SIGNAL NAME PM102
7020-1	Z1	NO	NO	GND	GND
-3	N/C	YES	YES	/HALT	/HALT
-5	Z3	NO	NO	MR (N/U)	Q1 (N/U)
-7	Z4	YES	YES	/IRQ	/IRQ
-9	Z5	YES	YES	VMA	VMA
-11	Z6	YES	YES	/NMI	/NMI
-13	Z7	YES	YES	BA	BA
-15	Z8	NO	NO	VCC (N/U)	VCC (N/U)
-17	Z9	YES	YES	A0	A0
-19	Z10	YES	YES	A1	A1
-21	Z11	YES	YES	A2	A2
-23	Z12	YES	YES	A3	A3
-25	Z13	YES	YES	A4	A4
-27	Z14	YES	YES	A5	A5
-29	Z15	YES	YES	A6	A6
-31	Z16	YES	YES	A7	A7
-33	Z17	YES	YES	A8	A8
-35	Z18	YES	YES	A9	A9
-37	Z19	YES	YES	A10	A10
-39	Z20	YES	YES	A11	A11
6020-39	Z21	NO	NO	GND	GND
-37	Z22	YES	YES	A12	A12
-35	Z23	YES	YES	A13	A13
-33	Z24	YES	YES	A14	A14
-31	Z25	YES	YES	A15	A15
-29	Z26	YES	YES	D7	D7
-27	Z27	YES	YES	D6	D6
-25	Z28	YES	YES	D5	D5
-23	Z29	YES	YES	D4	D4
-21	Z30	YES	YES	D3	D3
-19	Z31	YES	YES	D2	D2
-17	Z32	YES	YES	D1	D1
-15	Z33	YES	YES	D0	D0
-13	Z34	YES	YES	R/W	R/W
-11	Z35	NO	NO	VCC STANDBY N/U	N/C N/U
-9	Z36	YES	YES	RE (N/U)	DBE (N/U)
-7	Z37	YES	YES	E	Q2
-5	Z38	YES	NO	BIAS TO CRYSTAL OSCILLATOR	N/C N/U
-3	Z39	NO	NO	EXTAL (N/U)	TSC (N/U)
-1	Z40	YES	YES	/RESET	/RESET

Note: All lines from the replacement plug connect to the microprocessor in the ZIF socket. All even numbered lines are ground.

N/U = Not used

N/C = Not connected

MC6802 Timing Specifications

		Min.	Max.	
Frequency of Operation (Input Clock/4)	f	0.1	1.0	MHz
	f(Xtal)	1.0	4.0	MHz
Clock Timing Specifications:				
Cycle time	t(cyc)	1.0	10	microsec
Clock pulse width (measured at 2.4V)		450	4500	nsec
Fall time (measured between +0.4V and +2.4V)			25	nsec

[end]
[Strip number 23]

MC68A02 Timing Specifications

		Min.	Max.	
Frequency of Operation (Input Clock/4)	f	0.1	1.5	MHz
	f(Xtal)	1.0	6.0	MHz
Clock Timing Specifications:				
Cycle time	t(cyc)	1.0	6.6	microsec
Clock pulse width (measured at 2.4V)		300	3000	nsec
Fall time (measured between VSS +0.4V and VSS +2.4V)			25	nsec

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

THEORY OF OPERATION

Overview

The primary function of a Personality Module is to collect data from a system under test (S.U.T.) and transfer it to the logic analyzer in a format that the logic analyzer can interpret.

The PM102/PM103 Personality Module achieves this result by performing the following separate functions:

1. The PM102/103 allows the logic analyzer to monitor almost all communication between the processor-under-test in the ZIF socket (P.U.T.) and the system under test (S.U.T.) as the system operates.
2. The personality module generates additional control signals needed by the logic analyzer, that are not provided by the processor under test. See the Illegal Op Code Detector, the Instruction Fetch Decoder, and the NMI Detector.
3. The personality module buffers the pin 37 clock from the P.U.T. into a differential ECL clock signal to run the logic analyzer master clock system.
4. Before data acquisition the personality module PROM
   - sets up the acquisition hardware
   - personalizes the logic analyzer program display into a format for 6800/6802-based systems.

After data acquisition the PROM allows the logic analyzer to

- display the acquired data in a usable format
- disassemble the acquired data into 6800/6802 mnemonics, if desired.

5. The personality module lets the user halt his S.U.T. after the logic analyzer acquires the requested data.
6. In self test mode, the personality module outputs a predictable set of test signals, designed to simulate a subset of 6800/6802 instructions and special modes. The signals may be used to test the personality module and the logic analyzer.

Refer to Fig. 4-1, the Detailed System Block Diagram.

Circuit Description

Refer to Fig. 4-2, the PM102/PM103 Detailed Block Diagram, and the schematics, Section 8.

Block Description

Components on the schematic are grouped into functional blocks. The blocks are outlined on the schematic in grey. Fig. 4-2, the System Block Diagram, is a graphic functional representation of the blocks.

Input Buffers

Address and data input is double-buffered by two sets of octal buffer-drivers with 3-state outputs. The first set, A1U6040, A1U2040, and A1U3040, are protected against static discharge that could damage the personality module.

The second set of buffers are A1U6050, A1U2050, and A1U5040.

The first buffer set acquires address and data information and sends it to the Instruction Fetch Decoder and to the second set of buffers.

The second buffer set sends data to the logic analyzer, unless the logic analyzer is reading the PROM. See the PROM block description.

Clock Comparator

The ECL Comparator is a hysteresis-controlled high speed comparator with a 50K ohm, 4 x attenuator input. The S.U.T. signal to the ECL Comparator is the TTL level clock from pin 37 of the microprocessor in the ZIF socket. The ECL Comparator (A1U1040) output is differential ECL at standard levels, which is used in the logic analyzer to generate a master state clock.

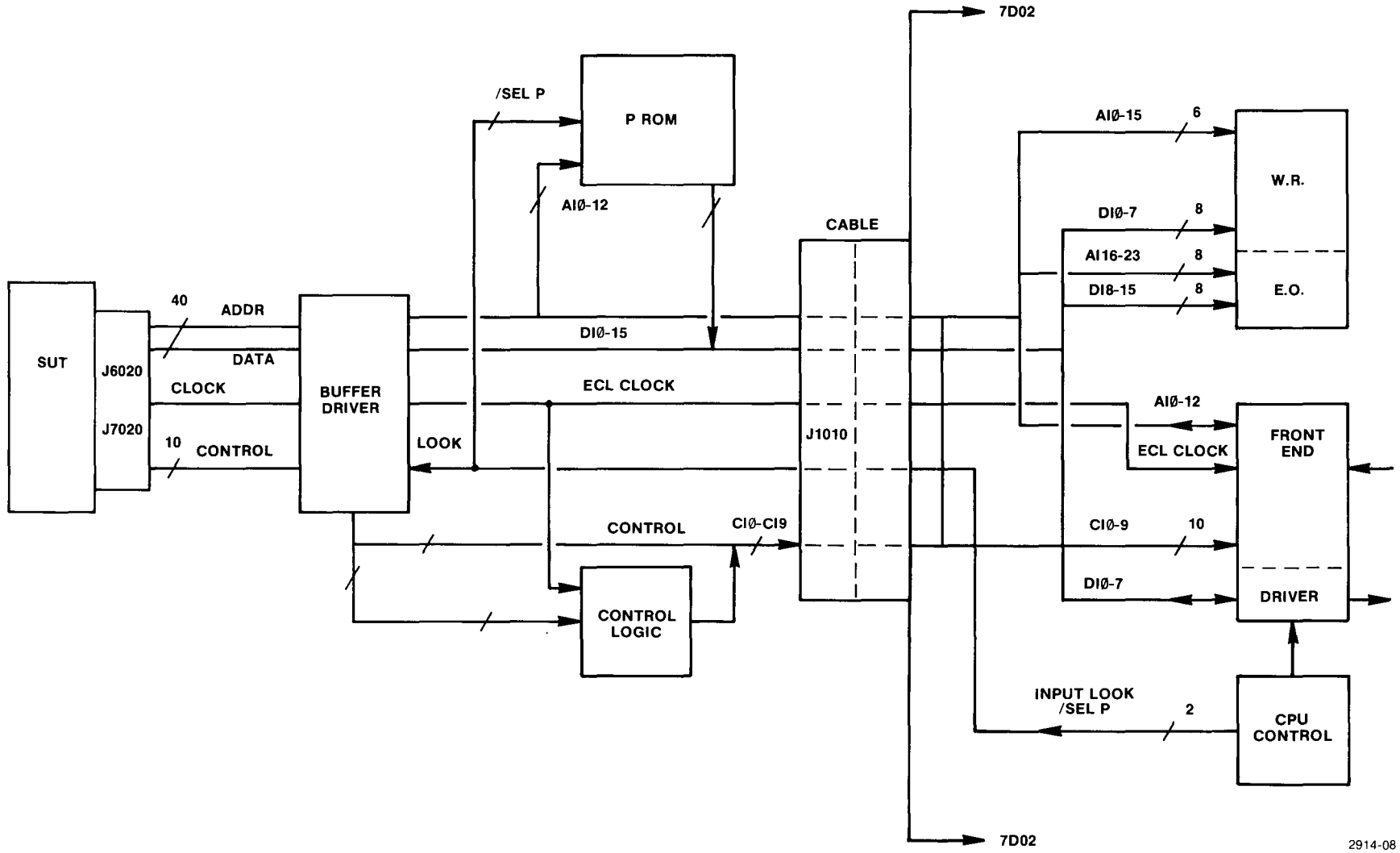

Fig. 4-1. Detailed System Block Diagram.

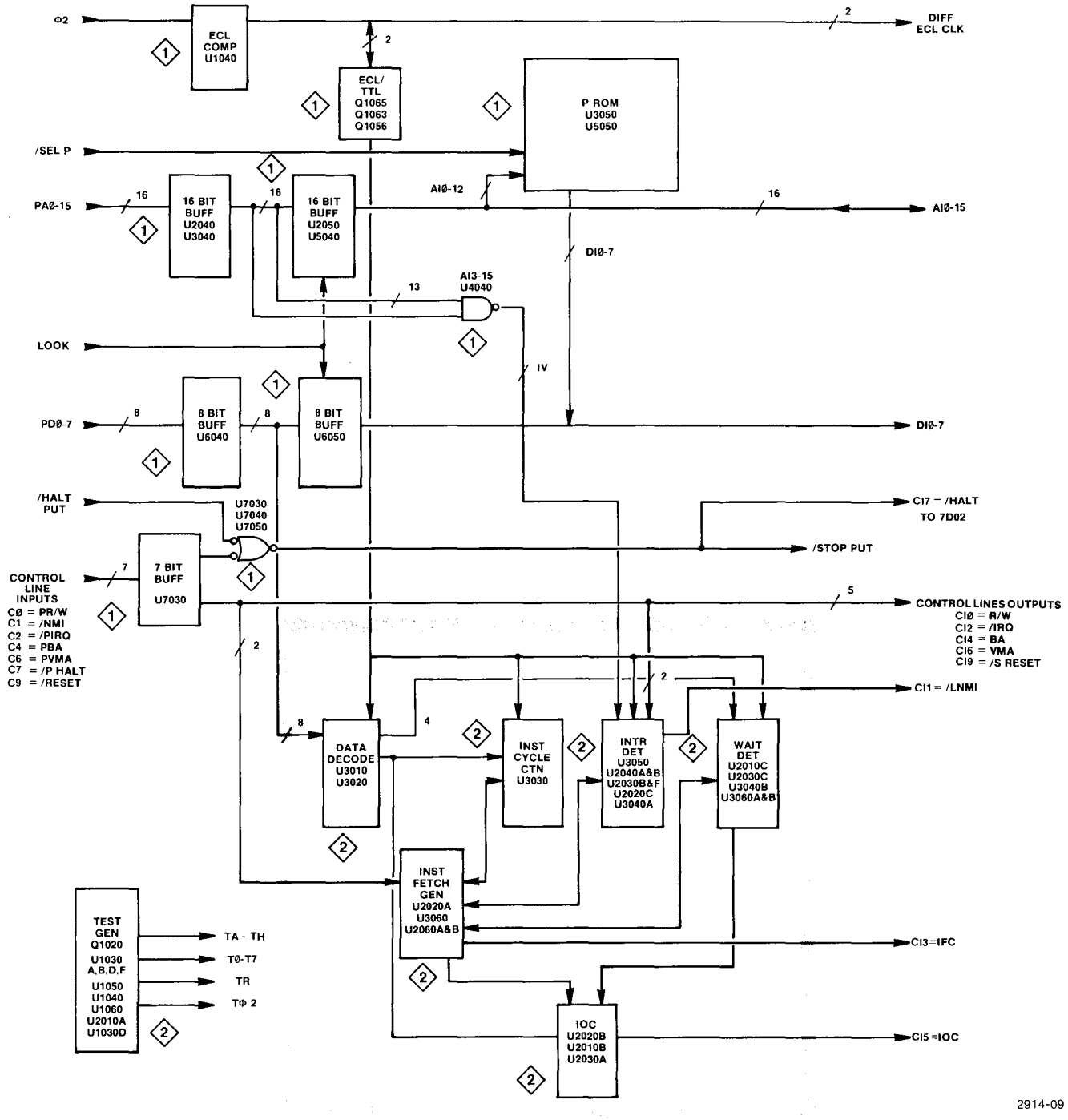

Fig. 4-2. PM102/PM103 Detailed Block Diagram.

ECL/TTL Converter

The ECL/TTL converter takes the differential ECL signal and converts it to an inverted TTL signal, Φ2TTL. Φ2TTL has a fast rising edge for the necessary timing and clocking characteristics of the Instruction Fetch Decoder.

Interrupt Vector Detector

The Interrupt Vector Detector, A1U4040, is a 13-input positive NAND gate that outputs a low on the /IV line to the Interrupt Generator whenever a vector FFF8, -9, -A, -C, -D, -E, or -F appears on the address bus.

Instruction Fetch Decoder

The Instruction Fetch Decoder includes the following blocks: Data Decoder, the Instruction Cycle Counter, the Instruction Fetch Generator, Illegal Op Code Detector, Wait Detector, and Interrupt Detector.

The IFC, or instruction fetch signal, is one of the control lines generated by the PM102/PM103. It tells the logic analyzer when it is reading a 6800/6802 instruction opcode on the data bus. Otherwise, the opcodes are indistinguishable in the continuous data flow. The following block descriptions illustrate how the Instruction Fetch signal is generated.

- Data Decoder

The Data Decoder latches data off the data bus from the Input Buffers, decodes it, and sends the code to the Instruction Cycle Counter in the first clock cycle. (See Fig. 4-3.)

A2U3010, a positive-edge-triggered D-type flip-flop, latches inverted data from the data bus buffer. The data addresses A2U3020, which sends output to the Instruction Cycle Counter when A2U3010 receives a Φ2TTL clock signal.

The 6800/6802 instruction set is unique in that the number of machine cycles needed to execute each instruction never changes. Once the number of cycles in the first instruction is known, the next instruction can be predicted. For example, if a six-cycle instruction is executing, another instruction can be expected at the end of six cycles.

A2U3020, the Instruction Fetch Predictor PROM, is encoded with the number of cycles for each 6800/6802 opcode. The input to the PROM is the complement of the opcode. The output of the PROM is the complement of the number of machine cycles plus 2. This output goes to the Instruction Cycle Counter.

For example, if the instruction input is STORE ACCUMULATOR (INDEX) the data bus contains an 'A7H'. (See the 6800/6802 Instruction Set, Section 2. You will find that STORE ACCUMULATOR (INDEX) is a 6-cycle instruction) The complement of A7H is 58H. Address 58H of A2U3020 contains a 'B' B equals the complement of 6, plus 2. The B goes to the Instruction Cycle Counter.

Exceptions to the A2U3020 encoding rules are the illegal opcodes, which cause A2U3020 to output 0000; and the WAIT FOR INTERRUPT instruction, which causes A2U3020 to output a 0001.

- Instruction Cycle Counter The Instruction Cycle Counter, A2U3030, is a synchronous 4-bit counter that loads a number from the Data Decoder, counts once for each clock cycle from the loaded number to F, (see Fig. 4-3) and outputs a signal on its ripple-carry-out line to the Instruction Fetch Generator and Interrupt Detector.

A2U2030D inverts the clock cycle to the Counter, so the counter loads and counts at the falling edge of the clock cycle.

To illustrate, take the previous example of the Data Decoder block. For a 6-cycle instruction, the Data Decoder loads a B into the Instruction Cycle Counter. (B = the complement of 6, plus 2.) To count from B to F requires 4 counts, or the number of machine cycles, minus 2. To understand the reason for only four counts, see Fig. 4-3.

The ripple-carry-out signal from the Instruction Cycle Counter is a prerequisite for all normal instruction fetches. (See Normal Instruction Fetch Generation.)

- Instruction Fetch Generator

For a normal instruction fetch (IFC) generation, the Instruction Fetch Generator waits for a signal from the Instruction Cycle Counter. When it receives the signal, it waits for the next clock, and outputs an instruction fetch signal to the logic analyzer if the bus is available and if it is a valid memory cycle. Notice that by waiting for the next clock, the Instruction Fetch Generator adds one more count to the output of the Instruction Cycle Counter (see Fig. 4-3).

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Instruction Cycle Counter Loads	Instruction Cycle Counter Counts to F	Instruction Fetch Generator Outputs Instruction Fetch Signal
1 cycle	X cycles	1 cycle

X = Number of machine cycles minus 2.

Fig. 4-3.
Relating machine cycle count to Instruction Fetch signal generation

After an interrupt, the Instruction Fetch Generator generates an Instruction Fetch Signal when the last interrupt vector is asserted from the Interrupt Vector Detector, through the Interrupt Detector.

For Instruction Fetch signal generation after hardware halts, WAI instructions, illegal op codes, and resets, see the Circuit Description sub-section.

- Interrupt Detector

The Interrupt Detector detects an interrupt when any of the following occurs:

1. The AD0 line from the address bus is the same for two cycles in a row, and the second cycle was after a fetch (indicating an /NMI, /IRQ, or software interrupt).
2. The /RESET line from the P.U.T. goes low.

When the Interrupt Detector senses an interrupt occurring, it enables the instruction fetch generator.

When the interrupt is about to be serviced, the interrupt detector signals the Instruction Fetch Generator to output an instruction fetch on the next clock cycle.

One of the Interrupt Detector components is a dual J-/K positive-edge- triggered flip-flop that latches the /NMI interrupt from the P.U.T. on its negative edge and holds it until the next valid memory address.

Any /NMI interrupt request, even a glitch, from the system under test sets the flip-flop, causing it to output a /LNMI signal to the logic analyzer until the next valid memory address.

This means the logic analyzer sees any /NMI interrupt request from the S.U.T., even if it is only a glitch.

- Wait Detector

When a "Wait For Interrupt" (WAI) instruction is executed, the Data Decoder outputs a 1 to the Wait Detector. The Wait Detector enables the Instruction Fetch Generator, allowing it to wait for interrupt.

- Illegal Op Code Detector

The illegal op code (/IOC) signal is generated by the PM102/PM103 for the logic analyzer.

When A2U3020 outputs a 0 one clock past the previous instruction fetch, that instruction fetch was for an illegal op code.

- PROM

The PROM circuitry consists of a 2K x 8 PROM (A1U3050) and an 8-bit tri-state buffer driver (A1U5050).

The logic analyzer LOOK signal turns off the second set of Input Buffers. This gives the logic analyzer access to AI0-12 and DI0-7 on the bus. The logic analyzer /SEL P then enables A1U3050 and turns on A1U5050, allowing the logic analyzer to read information from the PROM. See Data Acquisition.

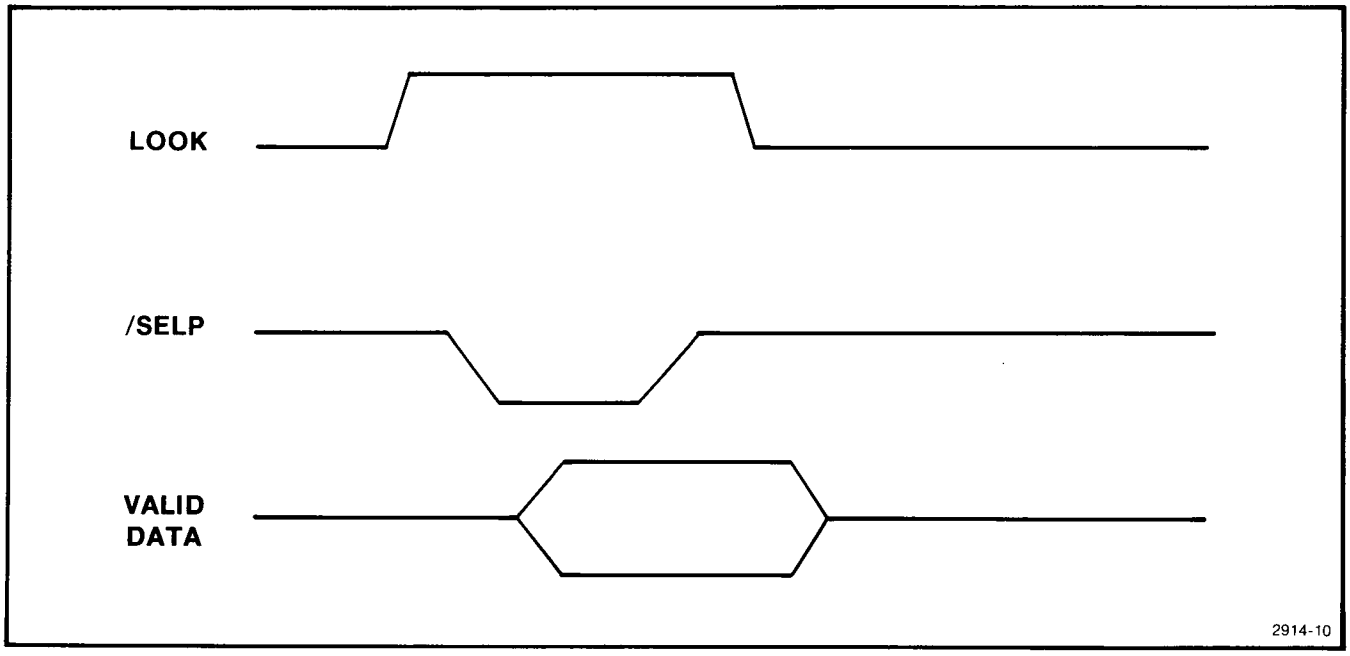

Fig. 4-4. Relating data bus to LOOK and /SEL P.

- Self Test Block

The Self Test block consists of a 2.5 MHz clock, two 4-bit binary counters (A2U1050 and A2U1040) and a 256 x 8 PROM (A2U1060). The PROM and counters exercise the hardware in the PM102/PM103 Personality Module by generating test signals. The PROM is also addressed by the counters. See 4-5 for the test-signal/microprocessor plug relationship.

PM102/PM103 Microprocessor Plug pin	A2U2070 Pin	Test Circuit Output Pin
D0	33	TA
D1	32	TB
D2	31	TC
D3	30	TD
D4	29	TE
D5	28	T5 (PROM A2U1060)
D6	27	T6 (PROM A2U1060)
D7	26	T7 (PROM A2U1060)
R/W	34	T1 (PROM A2U1060)
BA	7	T2 (PROM A2U1060)
/IRQ	4	T4 (PROM A2U1060)
/NMI	6	TH
VMA	5	TR
/RESET	40	T3 (A2U1060)
/HALT	2	T0 (A2U1060)
A0	9	TA
A1	10	TB
A2	11	TC
A3	12	TD
A4	13	TE
A5	14	TF
A6	15	TG
A7	16	TH
A8	17	TD
A9	18	TF
A10	19	TF
A11	20	TD
A12	22	TE
A13	23	TF
A14	24	TG
A15	25	TH

Fig. 4-5. Self-Test Circuit Relationship to PM102/PM103 Microprocessor Plug Pins.

For the absolute and mnemonic 7D02 displays generated by the Self Test circuit, see Section 5, the Performance Check.

Detailed Circuit Description

Refer to the schematics in Section 8.

Data Acquisition

Refer to the timing diagram, Figure 4-6.

When the logic analyzer is acquiring data and address information from the S.U.T., data enters Board I (A1) at A1P6020 and is acquired by the input buffer A1U6040. A1U6040 sends the data to buffer A1U6050. From there, it goes through DI0-7 to the logic analyzer by way of A1P1010, pins 29-36.

Address information enters the personality module on A1P7020 and A1P6020. It is acquired first by buffers A1U2040 and A1U3040, and then buffers A1U2050 and A1U5040. It goes to the logic analyzer through AI0-15 to pins 5-20 of A1P1010.

When the logic analyzer is acquiring data from the PROM, it first sends a high signal out on the LOOK line, which forces buffers A1U6050, A1U2050, and A1U5040 into their high impedance state.

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The logic analyzer next sends out a low on /SEL P, and applies the address of the information that it wants to AI0-10 on P1010. AI0-10 goes to A1U3050. A1U5050 drives DI0-7 as soon as /SEL P goes low. The logic analyzer reads the data on DI0-7, and simultaneously returns /SEL P to its high state. Last, LOOK goes back to a low state, and the address and data buffers A1U6050, A1U2050, and A1U5040 are no longer inhibited. The information going to the logic analyzer on DI0-7 and AI0-15 is again from the system under test.

Notice that the LOOK signal has no effect on the data and address information going to the instruction fetch decoder on board II (A2). It still receives data on DA0-7, and address information on /IV and AD0.

Instruction Fetch Signal Generation

The IFC, or instruction fetch signal tells the logic analyzer when it is reading a 6800/6802 instruction opcode on the data bus. The personality module generates the Instruction Fetch signal several different ways.

- Normal Instruction Fetch Generation

Refer to the timing diagram in Fig. 4-6.

At the rising edge of the Φ2TTL clock, the last RIFC (Read Instruction Fetch Cycle) is latched into the logic analyzer. A2U3010 latches in DA0-DA7, which contains the opcode. A2U3020 decodes the data into number of machine cycles of this instruction, complemented plus 2. A2U2060B, a dual D-type positive-edge-triggered flip-flop, outputs a low that enables LD on the Instruction Cycle Counter.

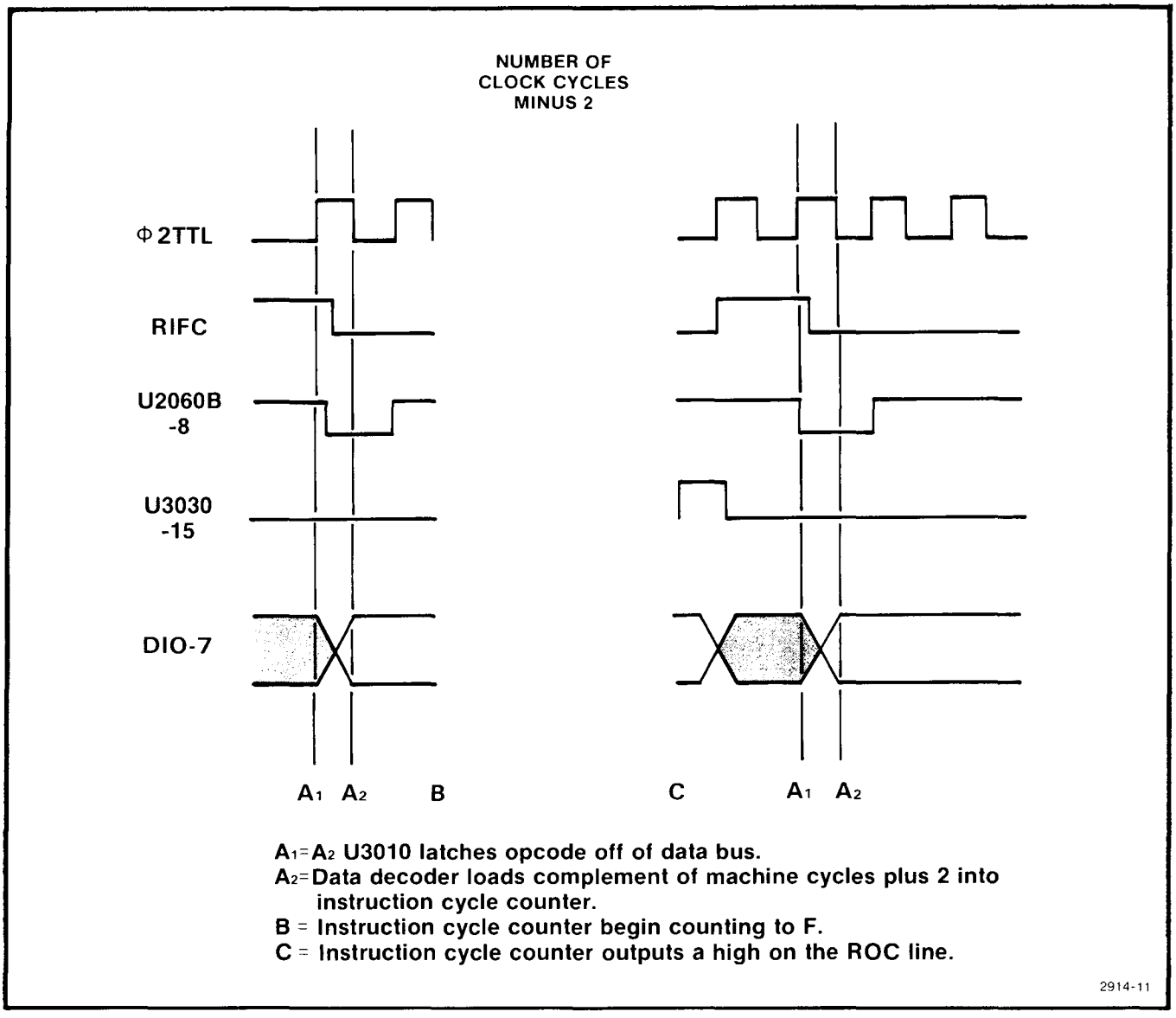

Fig. 4-6. Normal Instruction Fetch Signal Generation.

On the falling edge of Φ2TTL, A2U3030 loads the number of machine cycles in this instruction complemented plus 2.

On the next rising edge of Φ2TTL, A2U2060B pin 8 outputs a high, disabling the load line of A2U3030.

On the next falling edge of Φ2TTL, A2U3030 starts counting, from the complement of the number of machine cycles of this instruction plus two, to F. The number of clock cycles required to reach F equals the number of machine cycles minus 2. As A2U3030 reaches F, it outputs a high on the RCO (ripple-carry-out, A2U3030 pin 15), which goes to A2U3040 pin 2 to disable any illegal interrupts, and pulls A2U3060 pin 5 high. A2U3060 is a 4-wide and/or invert gate. If there is no interrupt, A2U3060 pin 3 is already in a high state following the last instruction fetch, and A2U3060 pin 4 is high because the WAIT detector did not detect a WAI instruction. All inputs to A2U3060-D are, therefore, high. When A2U3060-D goes high, A2U3060 pin 6 outputs a low to A2U2060A, pin 2.

At the rising edge of the next clock cycle, A2U2060A latches the low out on pin 5.

The low:

1. stops the Instruction Cycle Counter.
2. is applied to A2U2020A, a triple 3-input positive-NOR gate.
3. sets A2U3040A if there were any interrupts.

If the bus available (BAB) is low and if it is a valid memory cycle (/VMAB is low), A2U2020A outputs the instruction fetch signal.

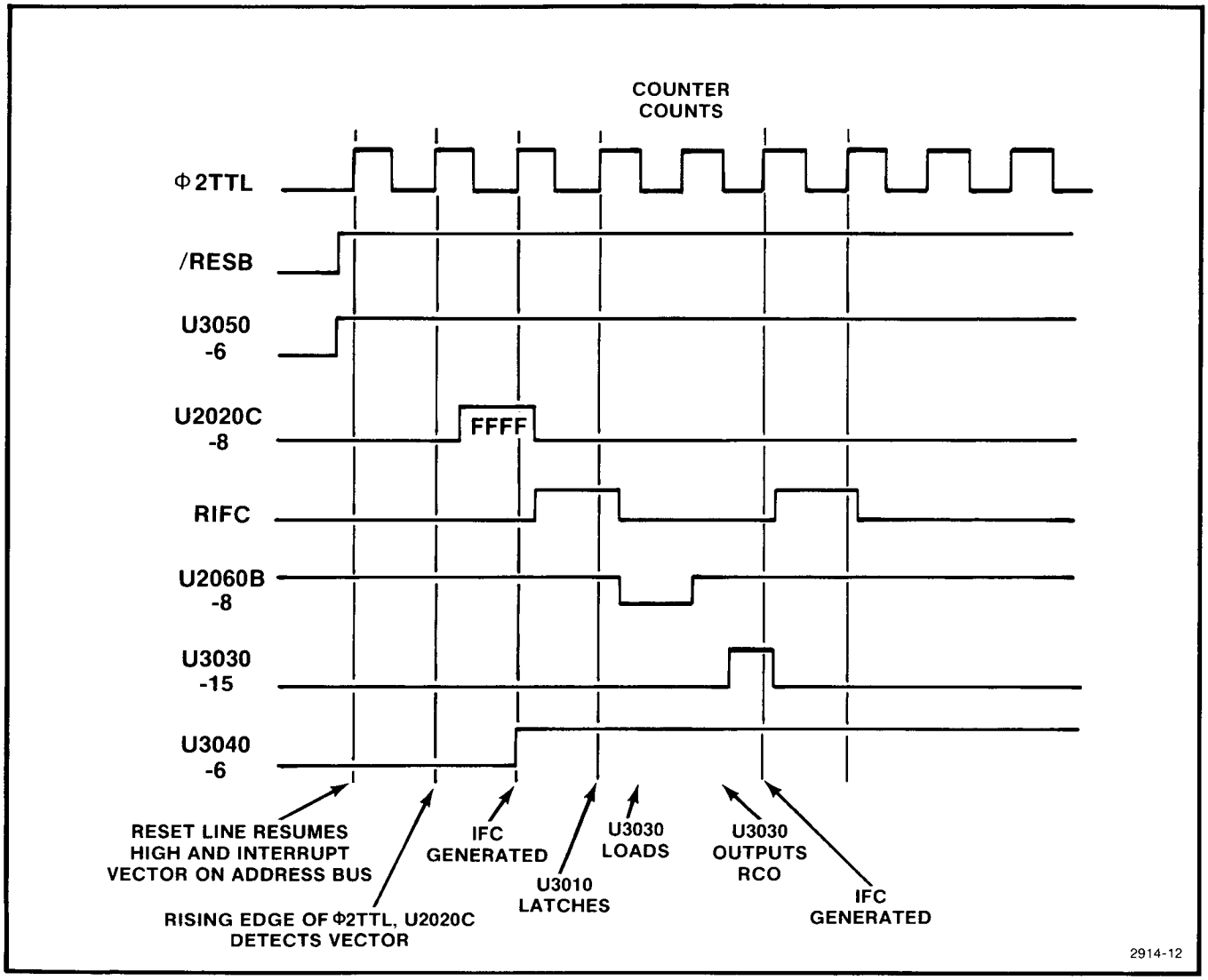

Fig. 4-7. Instruction Fetch After Reset.

- Instruction Fetch After RESET

Refer to the timing diagram in Figure 4-7.

When RESET is asserted on the S.U.T., the /RESET line on the processor goes down for at least eight clock cycles. After it goes high again, the microprocessor loads the contents of vectors FFFE and FFFF into the program counter. This is the address of the restart routine. Valid memory address (PVMA) goes high on the next pin 37 clock.

On the personality module, A1J6020 pin 1 goes low. The low goes into buffer A1U7030 on pin 2 and out pin 18. The low signal is sent to the logic analyzer on pin 55 of A1P1010 (/SRESET). The low is also applied to the Instruction Fetch Decoder on pin 3 of A1P1015 (/RES B).

A2U2030B inverts the low to a high and sends it to A2U3050-C. A2U3050 pin 6 outputs a low. The low goes to pin 1 of A2U3030, the Instruction Cycle Counter, clearing it to prevent false instruction fetch signals. The low is also applied to A2U3040A, which outputs high on pin 7 on the next clock. A high on pin 7 enables A2U3060-C. A2U3060-D is disabled by a low from A2U3040A pin 6.

When the address bus stabilizes A1U4040 detects FFFE and FFFF on the address bus, it sends a low on the /IV line to A2U2020C. If it is a valid memory cycle (/VMAB is low), and if the inverted least significant address bit (AD0) is 1 (indicating an FFF9, FFFB, FFFD, or FFFF) Pin 8 of A2U2020C sends a high signal to pin 2 of A2U3060-C, causing A2U3060 pin 6 to go low, starting the next instruction fetch.

- Instruction Fetch After Hardware Halt

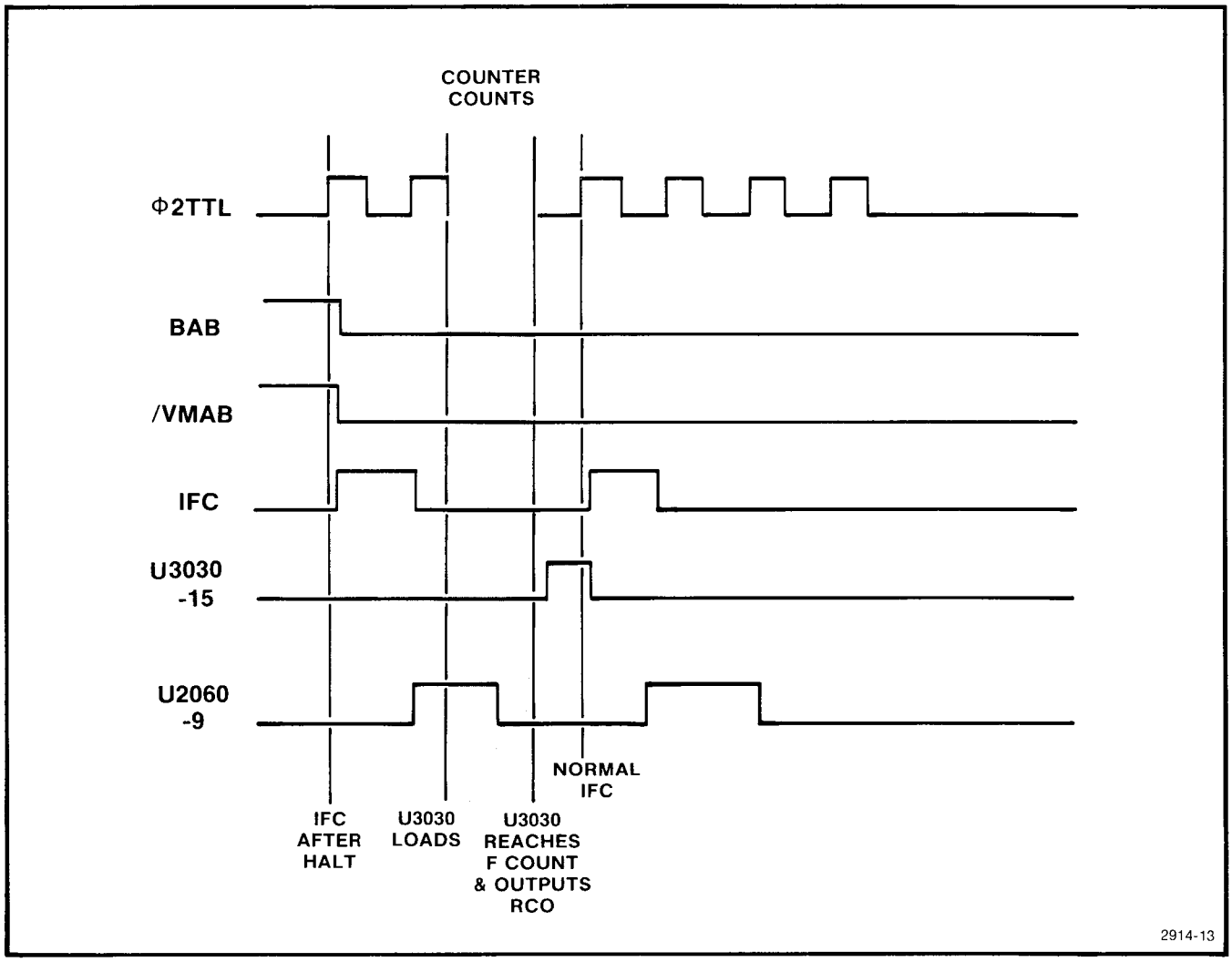

Fig. 4-8. Instruction Fetch After Halt.

Refer to the timing diagram in Figure 4-8.

Either the logic analyzer or the system under test can halt the processor under test. The logic analyzer sends a low on pin 61 of A1P1010 (/HALT P.U.T.). The low is applied to A1U7040, a quadruple 2-input positive-nand Schmitt trigger. A1U7040 outputs a high to inverter A1U7050. A1U7050 sends the low to A1U4020 pin 2. The processor, receiving a low on A1U4020 pin 2, the /STOP P.U.T. line, halts on the next instruction.

Or, pin 3 of A1P7020 (/P HALT) from the S.U.T. goes low, with the same result. Notice the octal buffer, A1U7030, on the /P HALT line.

When the 6800/6802 receives a low signal on its /HALT pin (shown on the schematic as /STOP P.U.T.) it acknowledges with a high on the BA line, a low on VMA, and puts its address bus, data bus, and R/W line into high impedance state.

The high on the BA line causes pin 13 of A1J7020 PBA to go high. The signal splits into BA and BAB. The BA goes to the logic analyzer via A1P1010 pin 30, and BAB goes to the instruction fetch decoder on board II (A2) via A1P1015 pin 2. The high state of BAB is applied to pin 2 of A2U2020A in the Instruction Fetch Generator, disabling it, and pins 9 and 10 of A2U3060. (Notice that the high on the /VMAB line is also being applied to pin 13 of A2U2020A.)

A2U3060-B is enabled by pin 11 going high after the last instruction fetch. (A2U3060-A is enabled for the WAI instruction) A2U3060 pin 6 outputs a continuous low. However, no instruction fetch is generated since A2U2020A is disabled. This is a hardware halt.

The next instruction fetch is generated by the BA line on the processor returning to its normal low state and VMA returning to normal high. BAB and /VMAB go low. Pins 2 and 13 of A2U2020A go low, and because A2U2060 holds the low output of A2U3060 for one cycle, A2U020A receives three low inputs and outputs the instruction fetch signal onto pin 1 of A2J1015.

- Instruction Fetch After WAI Instruction

When a WAI instruction is executed by the processor under test, the BA line goes high, VMA goes low, and address bus, R/W and data bus are all in high impedance state (same conditions as a hardware halt).

In the personality module, BAB goes high, as does A2U2020A pin 2, which disables the instruction fetch generator.

When an opcode "WAIT FOR INTERRUPT" enters A2U3020, it outputs a 0001. The 000 is applied to input pins 3, 4, and 5 of A2U2020B, a triple 3-input NOR gate, which outputs a high signal. The high is applied to A2U2010C, a triple 3-input NAND gate. The 1 from Q1 of A2U3020 is applied to A2U2010C pin 9. Pin 10 of A2U2010C is high from the latched instruction fetch, so A2U2010C outputs a low on pin 8.

A2U2030C inverts the low to a high, and applies it to the J input of of A2U3040B, a dual J-/K positive-edge triggered flip flop.

On the falling edge of the Φ2TTL clock, A2U3040B pin 9 goes low and pin 10 goes high. enabling A2U3060-A and disabling A2U3060-B and -D. A2U3060-A now waits for the interrupt.

Refer to Figure 4-9.

When the interrupt vector on the address bus causes A1U4040 to output a low on the /IV line, and the least significant bit of the address bus is 1 (AD0 high inverted to low) and it is a valid memory address (/VMAB is low), A2U2020C sends a high to A2U3060 pin 13. A2U3060 then outputs a low on pin 6, which starts the next instruction fetch.

- Instruction Fetch After Interrupts

See Figure 4-10.

An NMI, IRQ, or software interrupt causes the same address to appear twice on the address bus. If AD0, the low order bit on the address bus, is the same for an instruction fetch cycle and for the following cycle, interrupt detector triggers. A2U2030F, A2U2040A and A2U3050-A and -B detect the same instruction fetched twice from the same address.

When AD0 is the same for two cycles in a row, and the second cycle is after an instruction fetch, either A2U3050 9, 10, and 11; or A2U3050 3, 4, and 5 are in a high state. When this occurs, A2U3050 pin 6 outputs a low, which is applied to A2U3040A pin 3. A2U3040A pin 7 goes high on the next clock edge, enabling A2U3060-C. Now all that is needed to start the next instruction fetch is for the interrupt vector to appear on the address bus.

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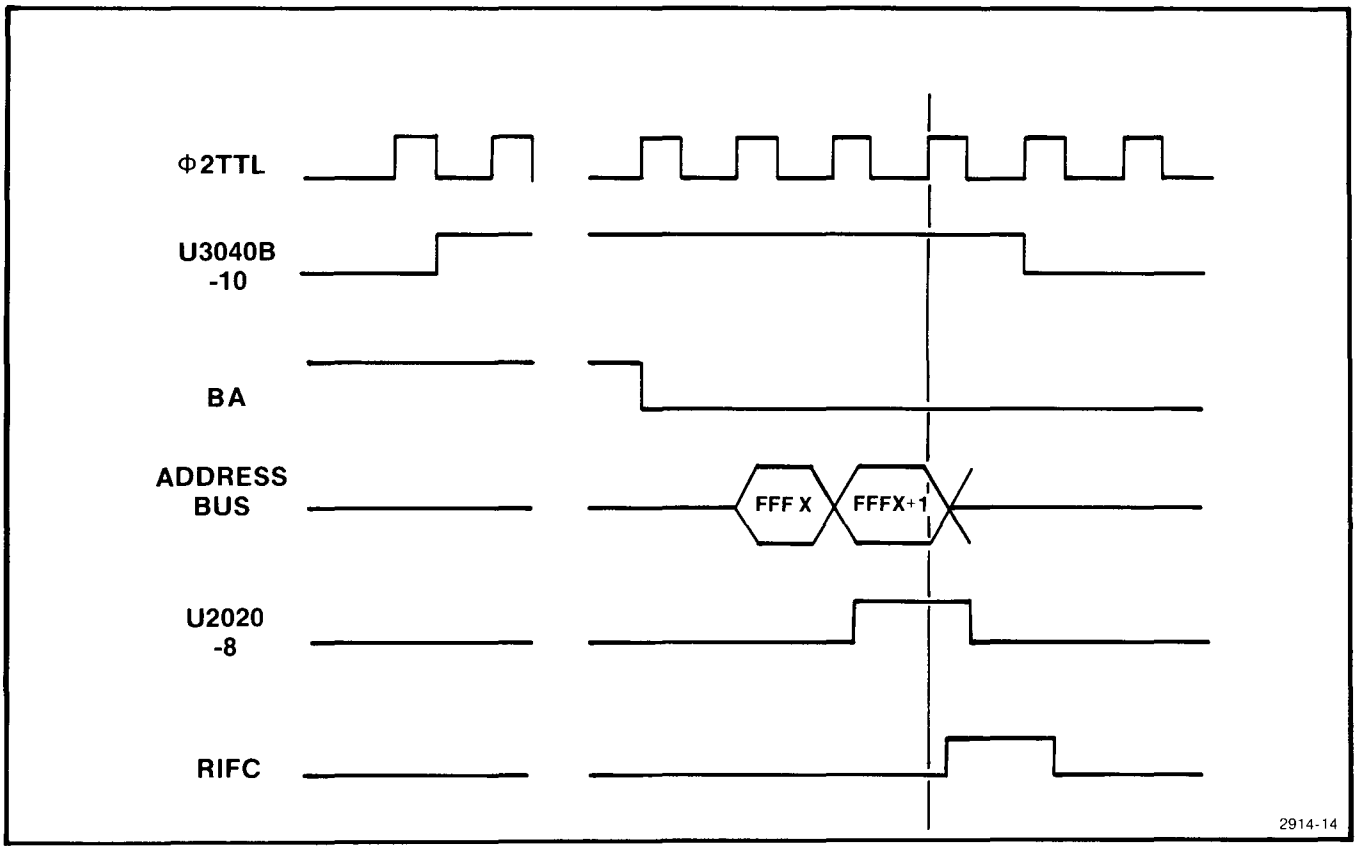

Fig. 4-9. Instruction Fetch After WAI Instruction.

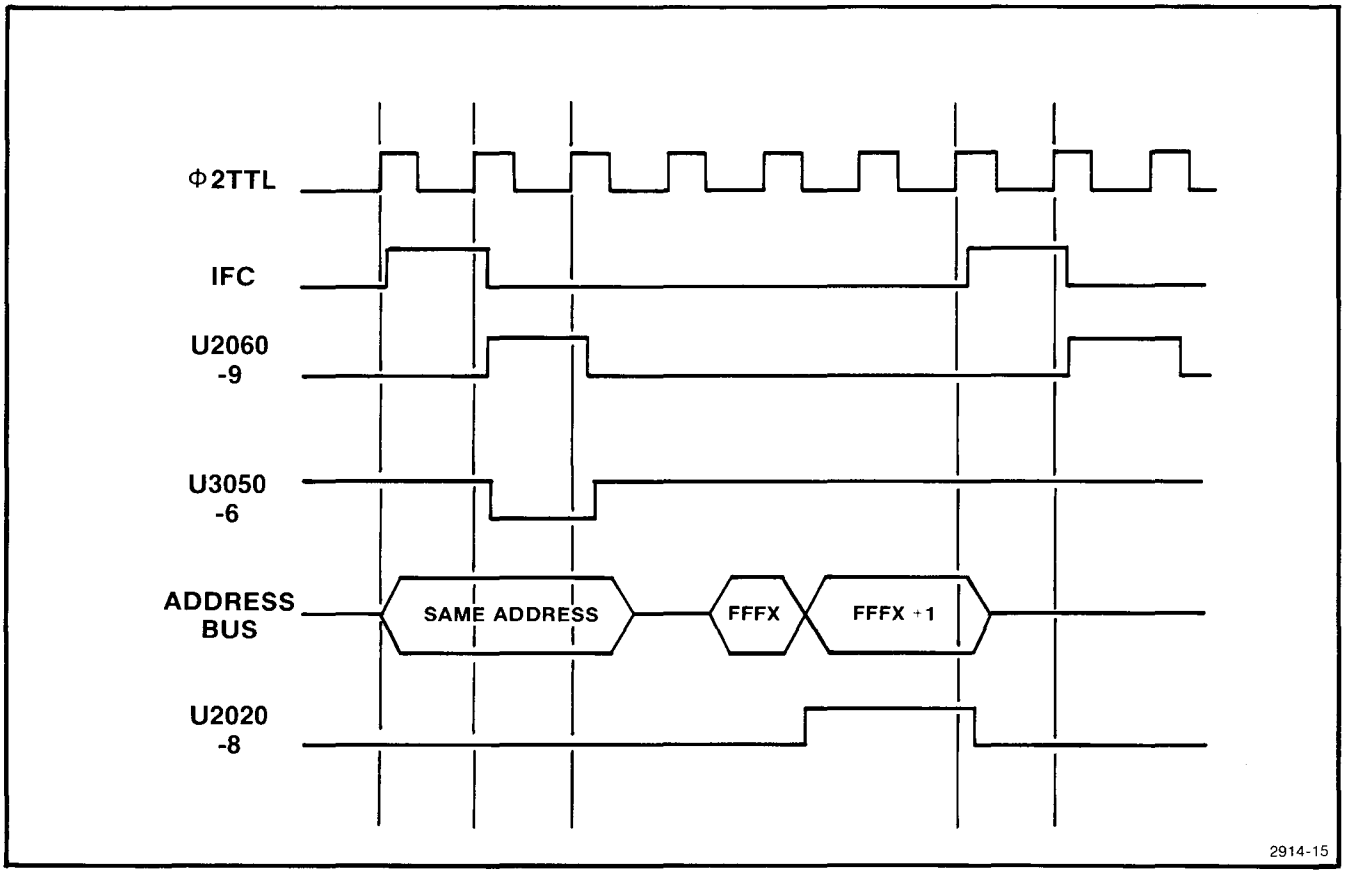

Fig. 4-10. Instruction Fetch After Interrupts.

The interrupt vector for an IRQ, NMI, or software interrupt is applied to A1U4040, and AD0. A1U4040 outputs the low /IV signal to A2U2020C pin 9. The high on AD0 is inverted by A2U2030F and applied to pin 11 of A2U2020C. Pin 10 of A2U2020C is low for any valid memory address. With all three inputs low, A2U2020C outputs a high on pin 8.

The high signal is applied to A2U3060 pin 2. A2U3060 outputs a low, which starts the next instruction fetch.

Illegal Op Code Detection

Any opcode being executed by the processor under test is also being read on the data bus by A2U3020. If the opcode is illegal, A2U3020 outputs a zero on output pins 9, 10, 11, and 12. The zeroes on 9, 10, and 11 cause A2U2020B pin 6 to go high. The zero on 12 is inverted to a high by A2U2030A. A2U2010B receives the high inputs on pins 3 and 5. The next rising edge of Φ2TTL after an instruction fetch will cause the Q output of A2U2060B to output a high. The high goes to pin 4 of A2U2010B. When all three inputs of A2U2010B are high, pin 6 outputs a low onto the /IOC line, which goes to Board I (A1), is inverted to IOC, and goes to the logic analyzer.

Notice that this signal is generated one Φ2TTL cycle after the instruction goes to the data bus. Therefore, it is one cycle late. The illegal opcode is detected when it is executed, rather than predicted before execution

NMI Interrupt Detection

When the S.U.T. requests an /NMI interrupt, the /NMI line to the processor goes to low state. A1U7030 buffers the low onto line /NMIB. /NMIB goes to the NMI Interrupt Detector on board II (A2) through A1P1015, pin 13.

On Board II (A2), the low is applied to the Set input of A2U2040B. If the low lasts 25 ns, the edge-sensitive Set input latches the low into A2U2040B, a dual J-/K positive-edge triggered flip-flop. When A2U2040B is set, the Q output, pin 10, outputs a positive signal, LNMI.

A low-going pulse on the /VMAB line, applied to the A2U2040B /K input, stops the LNMI output.

LNMI goes to A2J1015 pin 8. A1U7050 inverts the positive signal LNMI to /LNMI. /LNMI goes to the logic analyzer on A1P1010, pin 47.

Oscillator Bias for the PM103 Microprocessor Plug

A1P6020 pin 5 provides an oscillator bias for the PM103 microprocessor plug. It does not affect the PM102 microprocessor plug.

Self Test Circuit

The clock circuit consists of a discrete LC oscillator that provides a somewhat symmetrical 2-2.5 MHz output. This is pulse-shaped by Schmidt gates A2U1030A and B into a digital clock.

The resulting clock is applied to A2U2070 pin 37 as the master clock. When the personality module is in self test mode, the master clock negative edge defines the synchronous transfer of data to the logic analyzer.

The clock signal is also inverted by A2U1030F and applied to an 8-bit binary counter consisting of A2U1050, and A2U1040. The binary outputs of A2U1050 and A2U1040 are applied to the address and data lines of A2U2070 (See Fig. 4-4.) to produce part of the self test output indicated in Fig. 5-2.

The Ripple Carry Out outputs of each of the 4-bit counters are anded together by A2U2010A to produce a non-valid memory address signal every 16 clocks, except on the 256th clock (See Fig. 5-2.). The binary outputs of the counters are applied as addresses to A2U1060, a 256 x 8 bipolar PROM. This causes A2U1060 to output 8 bits of information as indicated in Fig. 4-4. The outputs of A2U11060 primarily determine the instructions that appear in Fig. 5-2 and the special mode signals like halt and interrupt.

NOTE

When in the "on" position, A2P1070 powers A2U1050, A2U1040 and A2U1060.

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PERFORMANCE CHECK

The following procedure is designed to confirm that a PM102/PM103 is operating within specified levels of performance.

Equipment

1. 7D02 Logic Analyzer mounted in 7000-Series Mainframe
2. PM102 or PM103
3. Tektronix PG502 Pulse Generator
4. Tektronix PG508 50 MHz Pulse Generator
5. Tektronix DM501A or DM502 Digital Multimeter
6. 40 pin wire-wrap DIP socket, Tek part no. 136-0622-00
7. 1 pair test leads for Digital Multimeter, Tek part no. 003-0120-00
8. Oscilloscope with 200 MHz bandwidth
9. 2 matched (delay must be equal, plus or minus 0.5 ns) 10X oscilloscope probes, 200 MHz bandwidth.
10. 2 BNC-male-to-BNC-male adapters, Tek part no. 103-0029-00
11. 50-ohm 10" coax cable, Tek no. 012-0208-00
12. 2 BNC female to EZ-ball adapters, Tek part no. 013-0076-01

Test Procedures

NOTE

To ensure correct test results, apply power to 7D02 and test equipment for a minimum of 20 minutes before proceeding with tests.

- Using Self Test Circuitry to Check Personality Module

1. Read and follow How To Use Self Test in Section 6.
2. Turn on 7D02 mainframe power switch, while holding down any 7D02 key to force 7D02 into diagnostic mode.
3. Press X to obtain DIAGNOSTIC MONITOR.
4. Press 0 to obtain TEST ALL diagnostic test.
5. Press START key to run diagnostic test.
6. Check 7D02 screen display for the PER. MOD. SYSTEM PASS message.
7. Enter the program in Fig. 5-1 on the 7D02.

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA = XX
1 ADDRESS=0000
1 /NMI=X /IRQ=X FETCH=X R/W=X
1 BA=X INVAL OP=X EXT TRIG IN=X
1 TIMING WR=X
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXXX
 END TEST 1
```

Fig. 5-1. Test Program.

8. Press 7D02 START/STOP key to run program.
9. The 7D02 should trigger on address 0000.
10. Compare the contents of 0-255 in the 7D02 acquisition memory with Fig. 5-2.

NOTE

The "Special" column in the table below is not shown. It is to show special modes generated by the test circuit.

```
LOC   ADDRESS OPERATION /IRQ/NMI          Special
000     F6F1     F1 READ      01          BA
001     F6F2     F2 READ      01          BA
002     F6F3     F3 READ      01          BA
003     F6F4     F4 READ      01          BA
004     F6F5     F5 READ      01          BA
005     F6F6     F6 READ      01          BA
006     F6F7     B7 READ      01
007     FFF8     B8 READ      01
008     FFF9     B9 READ      01          IRQ VECTOR
009     FFFA    ORA A  $1B    01
010     FFFB     1B READ      11
011     FFFC     3C READ      11
012     FFFD    *** (1D)      11          Illegal op code
013     FFFE     7E READ      11          /RESET
014     FFFF     9F READ      11          RESET VECTOR
015T---0000---NEG A---------10
016     0001     01 READ      10
017     0002    SBC A #$03    10
018     0003     03 READ      10
019     0004    LSR    $05,X  10
020     0005     05 READ      10
021     0006     26 READ      10
022     0007     47 READ      10
023     0908     68 READ      10
024     0909     89 READ      10
025     090A     AA WRITE     10
026     090B    SEV           10
027     090C     0C READ      10
028     090D    BLT    $091D  10
029     090E     0E READ      10
030     090F     2F READ      10          not VMA
031     1010     50 READ      10
032     1011    CBA           10
033     1012     12 READ      10
034     1013    PUL B         10
035     1014     14 READ      10
036     1015     35 READ      10
037     1016     56 READ      10
038     1017    TBA           10
039     1918     18 READ      10
040     1919    ADC A  $1A    10
041     191A     1A READ      10
042     191B     3B READ      10
043     191C    INC    $1D3E  10
044     191D     1D READ      10
045     191E     3E READ      10
046     191F     5F READ      10
047     2620     60 READ      10
048     2621     81 WRITE     10
049     2622    BHI    $2627  10
050     2623     03 READ      10
051     2624     24 READ      10
052     2625     45 READ      10
053     2626    ROR    $07,X  10
054     2627     07 READ      10
055     2F28     28 READ      10
```

```
056   2F29   49 READ      10
057   2F2A   6A READ      10
058   2F2B   8B READ      10
059   2F2C   AC WRITE     10
060   2F2D  BSR    $2F3D  10
061   2F2E   0E READ      10
062   2F2F   2F READ      10    not VMA
063   3630   50 WRITE     10
064   3631   71 WRITE     10
065   3632   92 READ      10
066   3633   B3 READ      10
067   3634   D4 READ      10
068   3635  BIT A  $16     10
069   3636   16 READ      10
070   3637   37 READ      10
071   3F38  EOR A  $19     10
072   3F39   19 READ      10
073   3F3A   3A READ      10
074   3F3B  RTI            10
075   3F3C   1C READ      10
076   3F3D   3D READ      10
077   3F3E   5E READ      10
078   3F3F   7F READ      10    not VMA
079   4040   80 READ      10
080   4041   A1 READ      10
081   4042   C2 READ      10
082   4043   E3 READ      10
083   4044   04 READ      10
084   4045  BIT B #$06     10
085   4046   06 READ      10
086   4047  STA A  $08,X   10
087   4948   08 READ      10
088   4949   29 READ      10
089   494A   4A READ      10
090   494B   6B READ      10
091   494C   8C WRITE     10
092   494D  JSR    $0E,X  10
093   494E   0E READ      10
094   494F   2F READ      10    not VMA
095   5050   50 READ      10
096   5051   71 WRITE     10
097   5052   92 WRITE     10
098   5053   B3 READ      10
099   5054   D4 READ      10
100   5055  TXS           10
101   5056   16 READ      10
102   5057   37 READ      10
103   5958   58 READ      10
104   5959  ADC A  $1A3B   10
105   595A   1A READ      10
106   595B   3B READ      10
107   595C   5C READ      10
108   595D  TST    $1E3F   10
109   595E   1E READ      10
110   595F   3F READ      10    not VMA
111   6660   40 READ      10
112   6661   61 READ      10
113   6662   82 WRITE     10
114   6663  COM    $04,X  10
115   6664   04 READ      10
116   6665   25 READ      10
117   6666   46 READ      10
118   6667   67 READ      10
119   6F68   88 READ      10
120   6F69   A9 WRITE     10
121   6F6A  ORA B #$0B     10
122   6F6B   0B READ      10
123   6F6C  BGE    $6F7B   10
124   6F6D   0D READ      10
125   6F6E   2E READ      10
126   6F6F   4F READ      10    not VMA
127   7670  SBA           10
128   7671   11 READ      10
129   7672  SBC A  $1334   10
130   7673   13 READ      10
131   7674   34 READ      10
132   7675   55 READ      10
133   7676  PSH A         10
134   7677   17 READ      10
135   7F78   38 WRITE     10
136   7F79   59 READ      10
137   7F7A  DEC B          10
138   7F7B   1B READ      10    /HALT
139   7F7C   3C READ      10    BA /HALT
140   7F7D   5D READ      10    BA /HALT
141   7F7E   7E READ      10    BA /HALT
142   7F7F   9F READ      10    BA /HALT /VMA
143   8080   A0 READ      10    BA /HALT
144   8081   C1 READ      11    BA
145   8082  SBC A  $03,X   11
146   8083   03 READ      11
147   8084   24 READ      11
148   8085   45 READ      11
149   8086   66 READ      11
150   8087  ASR    $08,X   11
151   8988   08 READ      11
152   8989   29 READ      11
153   898A   4A READ      11
154   898B   6B READ      11
155   898C   8C READ      11
156   898D   0D WRITE     11
157   898E  LDS    $0F,X   11
158   898F   0F READ      11    not VMA
159   9090   30 READ      11
160   9091   51 READ      11
161   9092   72 READ      11
162   9093   93 READ      11
163   9094  DES           11
164   9095   15 READ      11
165   9096   36 READ      11
166   9097   57 READ      11
167   9998  EOR B  $193A   11
168   9999   19 READ      11
169   999A   3A READ      11
170   999B   5B READ      11
171   999C  INC    $1D3E   11
172   999D   1D READ      11
173   999E   3E READ      11
174   999F   5F READ      11    not VMA
175   A6A0   60 READ      11
176   A6A1   81 READ      11
177   A6A2  SBC B #$03     11
178   A6A3   03 READ      11
179   A6A4  LSR A          11
180   A6A5   05 READ      11
181   A6A6  LDA A  $07,X   11
182   A6A7   07 READ      11
183   AFA8   28 READ      11
184   AFA9   49 READ      11
185   AFAA   6A READ      11
186   AFAB  ADD A #$0C     11
187   AFAC   0C READ      11
188   AFAD  TST    $0E,X   11
189   AFAE   0E READ      11
190   AFAF   2F READ      11    not VMA
191   B6B0   50 READ      11
192   B6B1   71 READ      11
193   B6B2   92 READ      11
194   B6B3   B3 WRITE     11
195   B6B4  AND A  $15     11
196   B6B5   15 READ      11
197   B6B6   36 READ      11
198   B6B7  STA B  $1839   11
199   BFB8   18 READ      11
200   BFB9   39 READ      11
201   BFBA   5A READ      11
202   BFBB   7B WRITE     11
203   BFBC  INC    $1D3E   11
204   BFBD   1D READ      11
205   BFBE   3E READ      11
206   BFBF   5F READ      11    not VMA
207   C0C0   60 READ      11
208   C0C1   81 WRITE     11
209   C0C2  SBC B  $03,X   11
210   C0C3   03 READ      11
211   C0C4   24 READ      11
212   C0C5   45 READ      11
213   C0C6   66 READ      11
214   C0C7  BEQ    $C9D1   11
215   C9C8   08 READ      11
216   C9C9   29 READ      11
217   C9CA   4A READ      11
218   C9CB  ADD A  $0C,X   11
219   C9CC   0C READ      11
220   C9CD   2D READ      11
221   C9CE   4E READ      11
222   C9CF   6F READ      11    not VMA
223   D0D0  NEG B          11
224   D0D1   11 READ      11
225   D0D2  SBC B  $1334   11
226   D0D3   13 READ      11
227   D0D4   34 READ      11
228   D0D5   55 READ      11
229   D0D6  ROR    $1738   11
230   D0D7   17 READ      11
231   D9D8   38 READ      11
232   D9D9   59 READ      11
233   D9DA   7A READ      11
234   D9DB   9B WRITE     11
235   D9DC  INC B          11
236   D9DD   1D READ      11    WAI
237   D9DE  WAI            11    not VMA
238   D9DF   1F READ      11
239   E6E0   20 WRITE     11
240   E6E1   41 WRITE     11
241   E6E2   62 WRITE     11
242   E6E3   83 WRITE     11
243   E6E4   A4 WRITE     11
244   E6E5   C5 WRITE     11
245   E6E6   E6 READ      11    BA
246   E6E7   E7 READ      11    BA
247   EFE8   E8 READ      11    BA
248   EFE9   E9 READ      11    BA
249   EFEA   EA READ      11    BA
250   EFEB   EB READ      11    BA
251   EFEC   EC READ      11    BA
252   EFED   ED READ      11    BA
253   EFEE   EE READ      11    BA
254   EFEF   EF READ      11    BA not VMA
255   F6F0   F0 READ      01    BA
```

Fig. 5-2. 7D02 Acquisition Memory Contents.

Enter the basic test program in Figure 5-3.

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX
1 ADDRESS=XXXX
1 /NMI=X /IRQ=X FETCH=X R/W=X
1 BA=X INVAL OP=X  EXT TRIG IN=X
1 TIMING WR=X
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    0-STANDARD CLOCK QUAL.
 END TEST 1
```

Fig. 5-3. Test Program.

```
Leaving everything else in its "X"
"X" (Don't Care) state, make these
changes (one at a time) to the
program in Fig. 5-3 and press
the 7D02 START/STOP key.            Trigger Should Occur On

/IRQ=0                              /IRQ=0
/IRQ=1                              /IRQ=1
/NMI=1                              /NMI=1
/NMI=0                              /NMI=0
ADDRESS=E6E7, BA=1                  Address E6E7
ADDRESS=E6E7, BA=0                  No Trigger
INVAL OP=1                          Cycle After ***
```

11. Enter the basic test program in Fig. 5-4.

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX
1 ADDRESS=FFFE
1 /NMI=X /IRQ=X FETCH=X R/W=X
1 BA=X INVAL OP=X  EXT TRIG IN=X
1 TIMING WR=X
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=1XX1XX
 END TEST 1
```

Fig. 5-4. Test Program.

Press the 7D02 START/STOP key. Trigger should NOT occur, and program should continue to run.

Stop the program by pressing the 7D02 STOP key and change the basic program to

```
ADDRESS=7F7B

C9-C4 (ANDED CLOCKS)=XX0XXX
```

The trigger should occur on

```
7F7B
7F7C
7F7D
7F7E
7F7F
8080
```

- Clock Input Resistance

1. Insert PM102/PM103 logic analyzer plug into 7D02.
2. Place 40-pin wire-wrap DIP socket on microprocessor plug to protect pins.
3. Turn on mainframe power switch.
4. Place one DM501A or DM502 test lead on ground (pin 1 of 40-pin wire-wrap DIP socket). Place one DM501A or DM502 test lead on pin 37.
5. Measure resistance. Resistance should be within 5% of 50K ohms.

- Set-up and hold time.

1. Insert PM102/PM103 logic analyzer plug into 7D02.
2. Protect PM102/PM103 microprocessor plug with 40-pin wire-wrap socket.
3. Turn on mainframe power switch.
4. Set PG502 period adjustment to 1 microsecond. Turn variable period knob to the X 1 position.
5. The PG502 will trigger the PG508. Connect the coaxial cable from the "+ Trigger Out" of the PG502 to "Trigger/Gate In" of the PG508.
6. Set the PG508 period knob to external trigger. Adjust the trigger/gate level knob until the green triggered/gated indicator is blinking, indicating the PG508 recognizes trigger/gate impulse and is triggering on it.
7. Set the PG502 to reverse termination by pulling out the BACK TERMINATION knob.
8. Set the oscilloscope to channel 1. Connect the channel 1 scope probe to the PG502 output. Switch the input coupling switch to ground. Position the trace 1.4V below the center graticule line. Switch the input coupling switch to DC. Adjust the PG502 output pulse for a low level of +.6 and high level of +2.0V.
9. Set the PG502 Normal/Complement button to the normal (out) position.
10. Disconnect the scope probe from the PG502 output, and connect the PG502 output across ground (pin 1) and A0 (pin 9) on the PM102/PM103 microprocessor plug.
11. Connect the channel 1 oscilloscope probe to the same pins as the PG502, ground to pin 1 and the probe to pin 9.
12. Switch the PG502 pulse duration knob to 5 ns. Adjust the PG502 variable pulse duration knob so that a 40 ns pulse appears on the oscilloscope screen. Check that the voltage levels of the pulse are +0.6 to +2.0 V.
13. Switch the oscilloscope to channel 2. Using the channel 2 output, test the PG508 output pulse voltage levels for +.6 to +2.0V. After adjusting the PG508 for the desired output, connect the PG508 outputs across ground (pin 1) and pin 37 on the PM102/PM103 microprocessor plug.
14. Connect the channel 2 scope probe to ground (pin 1) and pin 37 on the PM102/PM103 microprocessor plug.
15. Adjust the oscilloscope time base to 20 ns/div. Switch the PG508 pulse duration knob to 0.1 microsecond. Adjust the variable duration for a 180 ns pulse.
16. Obtain both displays, channels 1 and 2 on the oscilloscope.
17. Adjust the PG508 delay adjustment to 0.1 microsecond. Adjust the variable position knob until the trailing edge of the clock pulse (the PG508 output) and the trailing edge of the data pulse (PG502) coincide at the center horizontal graticule line of the oscilloscope screen. See Fig. 5-5 for an example of this.

18. The data pulse should be 40 ns wide. The clock pulse should be 180 ns wide.
19. Enter the following program on the 7D02:

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX
1 ADDRESS=XXXX
1 /NMI=X /IRQ=X FETCH=X R/W=X
1 BA=X INVAL OP=X EXT TRIG IN=X
1 TIMING WR=X
1THEN DO
1 TRIGGER 0-MAIN
1     0-BEFORE DATA
1     0-SYSTEM UNDER TEST CONT.
1     1-USER CLOCK QUAL.
1     1-FALLING EDGE OF CLOCK
1     C9-C4 (ANDED CLOCKS)=XXXXXX
1OR IF
1
```

20. Enter format mode with the FORMAT key, and change the Word Recognizer Address and Data fields to binary radix. Exit the format mode by pressing the FORMAT key. The program will now look like this:

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XXXXXXXX
1 ADDRESS=XXXXXXXXXXXXXXXX
1 /NMI=X /IRQ=X FETCH=X R/W=X
1 BA=X INVAL OP=X  EXT TRIG IN=X
1 TIMING WR=X
1THEN DO
1 TRIGGER 0-MAIN
1     0-BEFORE DATA
1     0-SYSTEM UNDER TEST CONT.
1     1-USER CLOCK QUAL.
1     1-FALLING EDGE OF CLOCK
1     C9-C4 (ANDED CLOCKS)=XXXXXX
1OR IF
1
```

21. Change A0, the far right address bit in the 7D02 program, to 0. All other elements should be in the X ("don't care") state.
22. Run the program by pressing the 7D02 START/STOP key.
23. The program should run without triggering or indicating a slow clock. This indicates the 7D02 is seeing the minimum clock pulse width, and making 40 ns setup, and 0 ns hold.
24. Stop the program by pressing the 7D02 STOP key.
25. Place the PG502 Complement button in the "complement" position. Adjust the scope so the pulses are on the screen, Verify the pulse out of the PG502 is 40 ns delayed and that the 2 trailing edges of the pulses cross at the threshold.
26. Change A0, the far right address bit in the 7D02 program to 1. Press the 7D02 START/STOP key.
27. Again, you should see no slow clock indication, and no trigger.
28. Stop the 7D02 program.
29. Complement the PG508, adjust the scope display so the trailing pulse edges cross at the threshold. Verify the pulse out of the PG508 is 180 ns wide.
30. Change the 7D02 program. Leave a 1 in A0, but change to rising edge of clock. Press the 7D02 START/STOP button.
31. Check for no slow clock and no trigger.
32. Complement the PG502 and change Address bit 0 back to 0. Press the START/STOP key.
33. Check for no slow clock and no trigger.
34. Repeat the test for pin A1 on the microprocessor plug. Move the PG502 and scope probes from A0 (pin 9) to A1 (pin 10).
35. Change the 7D02 program. The rightmost address bit, A0, should be returned to X, and next address bit, A1, should be changed to 0.
36. Repeat the above procedure for A1 and all address and data lines, and remember:

Address or Data bit	PG502 Complement Button
0	Normal
1	Complemented

Clock Edge	PG508 Complement Button
Falling	Normal
Rising	Complemented

See Fig. 5-5

- Halt delay from the microprocessor plug to the ZIF socket.

1. Insert the PM102/PM103 personality module into the 7D02.
2. Protect the Personality Module microprocessor plug with 40-pin wire wrap socket.
3. Turn on mainframe power switch.
4. Set the PG502 output pulse voltage levels to +.4V low and +2.4V high.
5. Connect the PG502 output across ground (pin 1) and /HALT (pin 2) on the personality module microprocessor plug.
6. Connect the channel 1 oscilloscope probe across the same two pins.
7. Insert square pins in the personality module ZIF socket, pins 1 and 2.
8. Connect the channel 2 oscilloscope probe across pins 1 and 2 in the ZIF socket. Pin 1 is ground.
9. Set the scope time base to 10 ns/div. Position the trace 1.4 divisions below the center graticule line. Switch the vertical input attenuator to 1V/div. The rising edge of the PG502 output pulse should be positioned on the left graticule line at the point where the leading pulse edge passes through the center horizontal graticule.
10. Obtain both displays on the oscilloscope.
11. Set the PG502 variable pulse duration at 50 ns. Turn the variable position knob to X1.
12. Measure the time delay of the rising edge of the pulse going into the plug to the rising edge of the pulse coming out of the ZIF socket. Rising edge to rising edge should be less than or equal to 55 ns.
13. Repeat the test with the falling edges.
14. Falling edge to falling edge should be less than or equal to 55 ns.
15. Complement the PG502, and repeat the measurements for the two sets of edges.

See Fig. 5-6.

@

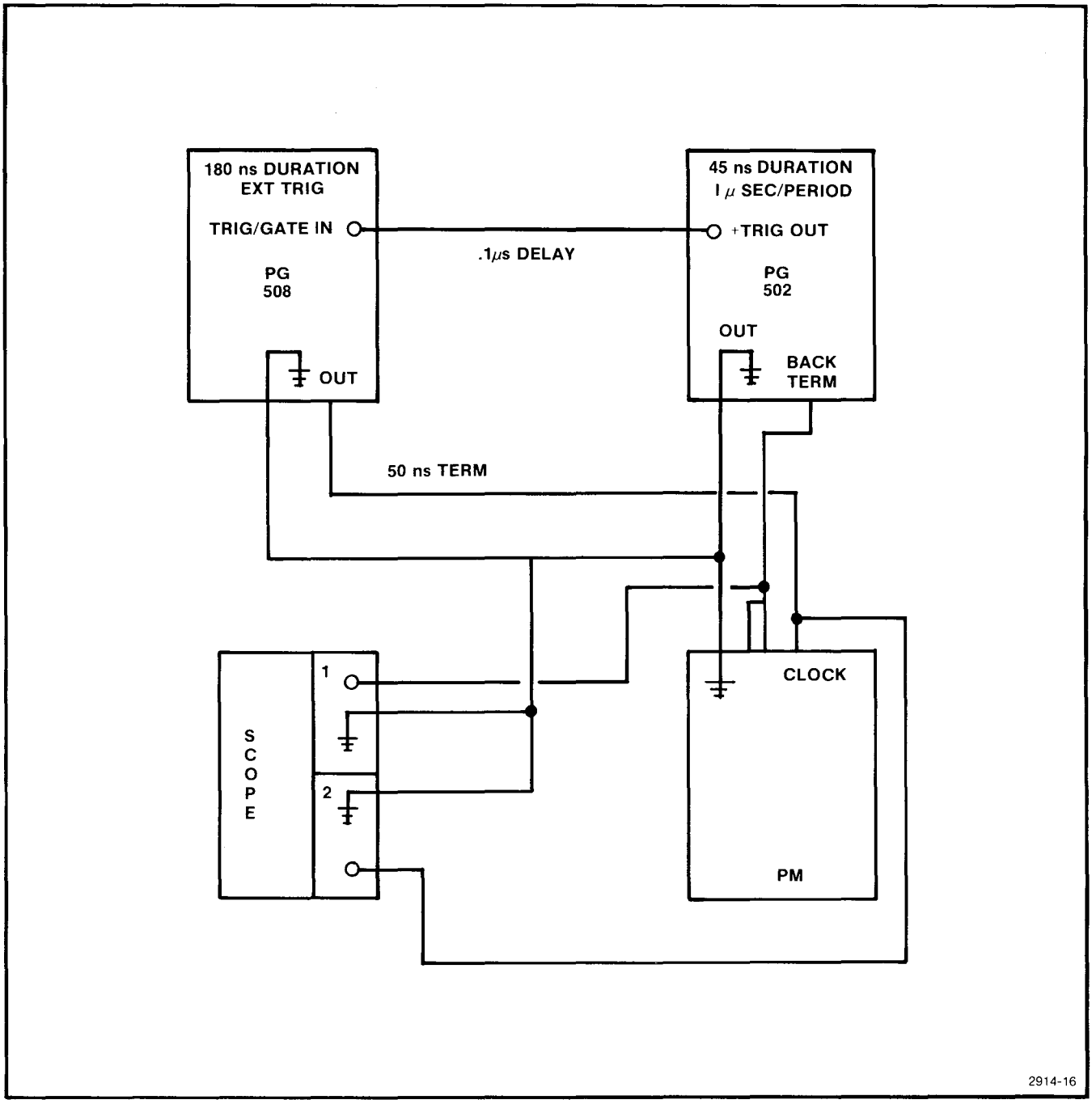


Fig. 5-5A. Setup and hold time test.

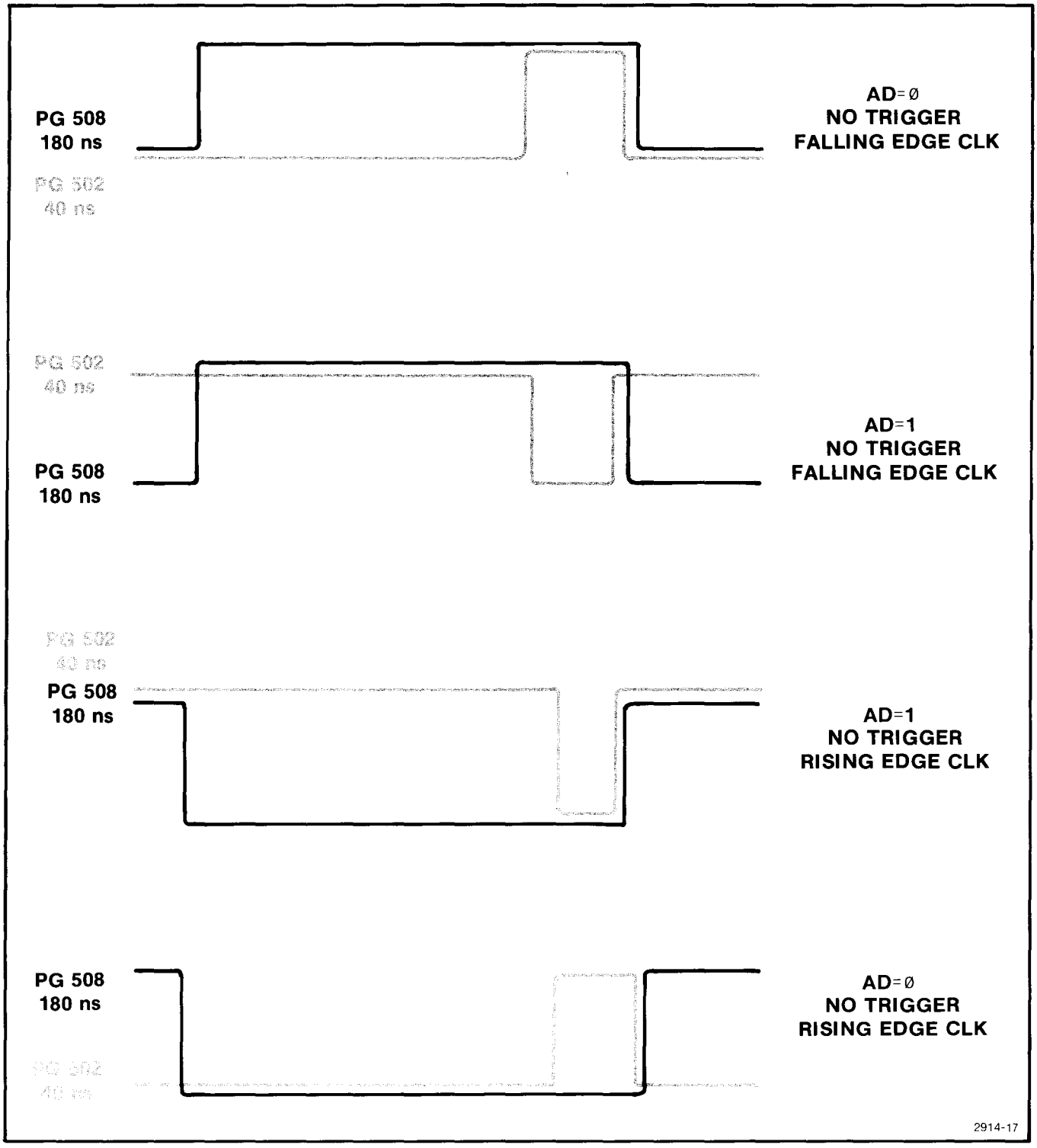


Fig. 5-5B. Setup and hold time test.

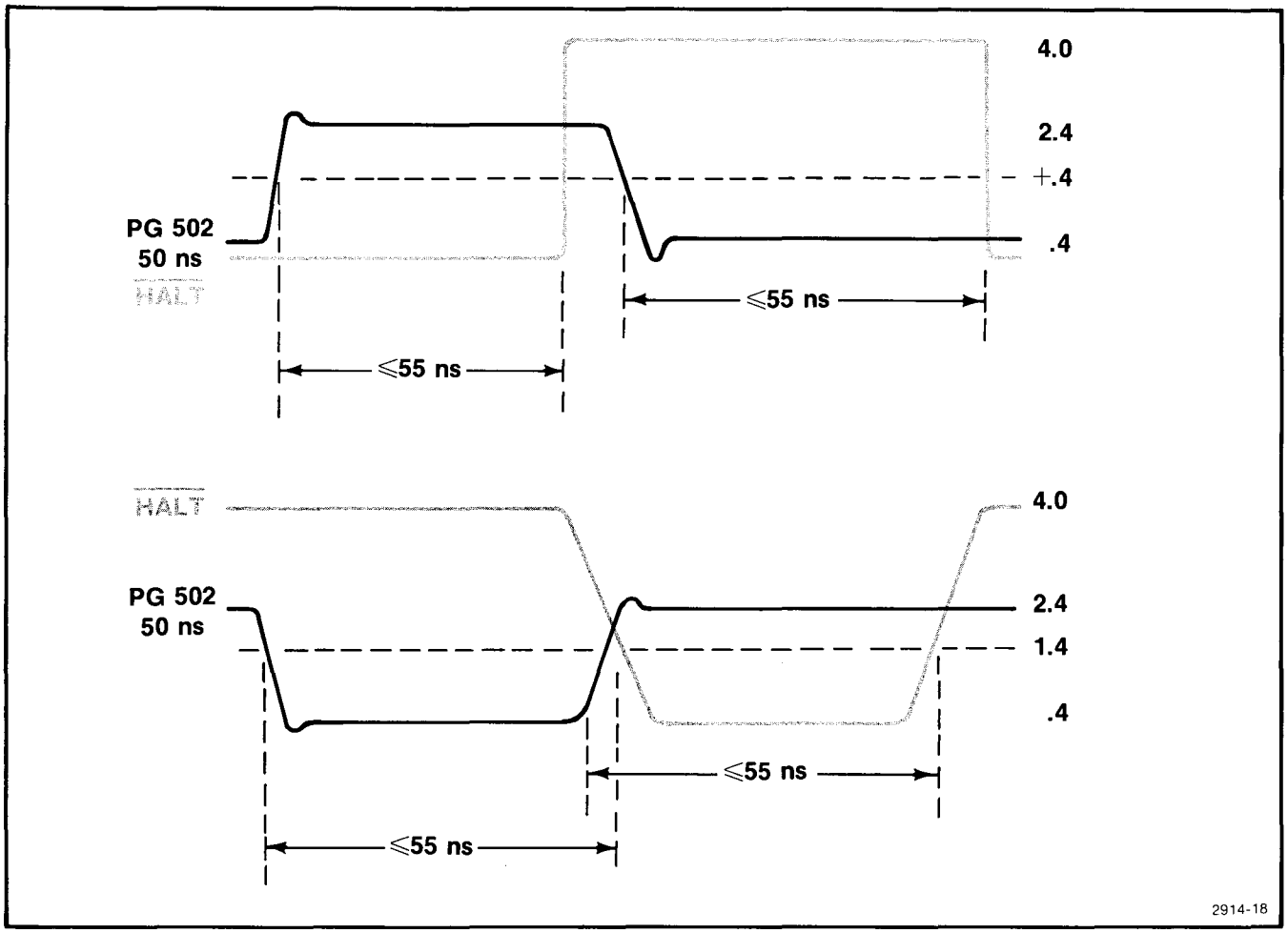


Fig. 5-6. Halt Delay Test.

MAINTENANCE AND TROUBLESHOOTING

Maintenance and Cleaning

Repair

Tektronix, Inc., provides complete instrument service at local Field Service Centers and at the Factory Service Center. Contact your local Tektronix Field office or representative for further information.

Obtaining Replacement Parts

Most electrical and mechanical parts can be ordered through your local Tektronix Field Office or representative. However, you should be able to obtain many of the standard electronic components from a local commercial source in your area. Before you purchase or order a part from a source other than Tektronix, Inc., please check the Replaceable Electrical Parts List, Section 7, and the Replaceable Mechanical Parts List, Section 9, for the proper value, rating, tolerance, and description.

Ordering Parts

When ordering replacement parts from Tektronix, Inc., it is important that all of the following information be included to ensure receiving the proper parts.

1. Instrument type (include modification or option numbers).
2. Instrument serial number.
3. A description of the part (if electrical, include component and number from the Electrical Parts List.)
4. The Tektronix part number.

Cleaning Instructions

This instrument should be cleaned as often as operating conditions require. Accumulation of dirt on components acts as an insulating blanket and prevents efficient heat dissipation, which can cause overheating and component breakdown.

Exterior

Loose dust on the personality module pod can be brushed off. Dirt that remains can be removed with a soft cloth dampened with a mild detergent and water solution. Abrasive cleaners should not be used.

CAUTION

Use only enough water to dampen the cloth or swab. Prevent water from getting inside the pod. Don't get the microprocessor plug or logic analyzer plug wet. DO NOT use chemical cleaning agents. They may damage the plastics used in the instrument. In particular, avoid chemicals that contain benzene, toluene, xylene, acetone or similar solvents.

Interior

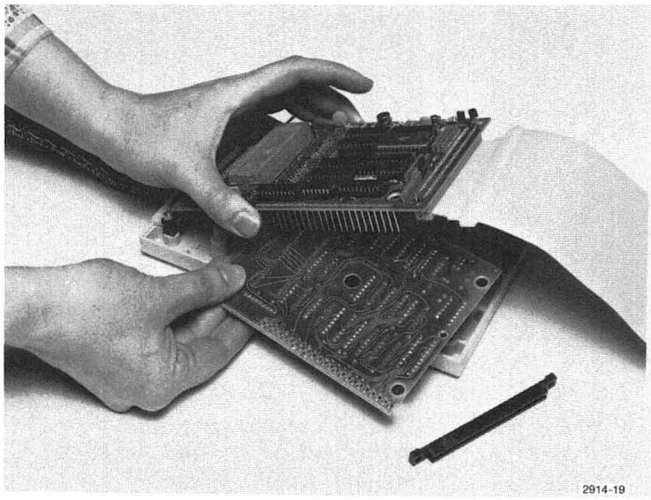
Dust in the interior should be removed with a jet of dry, low pressure air and a soft brush.

After major repairs flush the board well with clean isopropyl alcohol. Make certain soldering resin and dirt are removed from the board.

How to Disassemble Personality Module Pod

1. To remove the top cover, unscrew the four middle screws on the bottom of the Personality Module.
2. Lift the top cover off. The top board, A1, is now accessible.
3. To access the bottom board, A2, loosen the two end screws on the twisted pair woven cable end so that the cable can move inside the strain relief.
4. Remove the two end screws on the other end of the pod.
5. Lift up gently on the top board. It will remain attached on the twisted pair woven cable end.
6. Lift the bottom board out and turn it face down.
7. Plug A2J1015 into A1P1015.
8. The pod may now be operated, with both boards accessible for signature analysis.

To reassemble the instrument, reverse the above procedure.



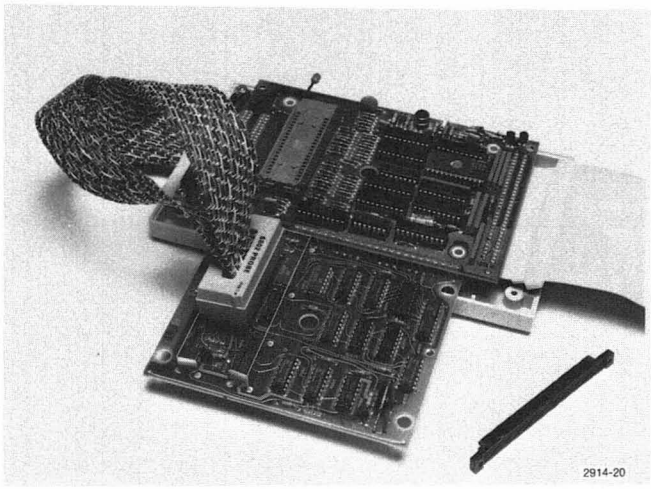


Fig. 6-1.
How to Disassemble Personality Module Pod

How to Disassemble Microprocessor Plug

If the pins on the microprocessor plug bend or break, the pin assembly is replaceable. Simply remove the two screws on the front of the plug and lift off the front. Replace the pin assembly (Tektronix part number 352-0536-00). Replace the plug front and the two screws.

Troubleshooting -- where to find:

- Performance Check—Section 5
- Troubleshooting Procedure—Section 6
- Circuit Descriptions—Section 4
- Schematics—Section 8
- Signature Analysis Tables—Section 6
- Signal Glossary—Section 10

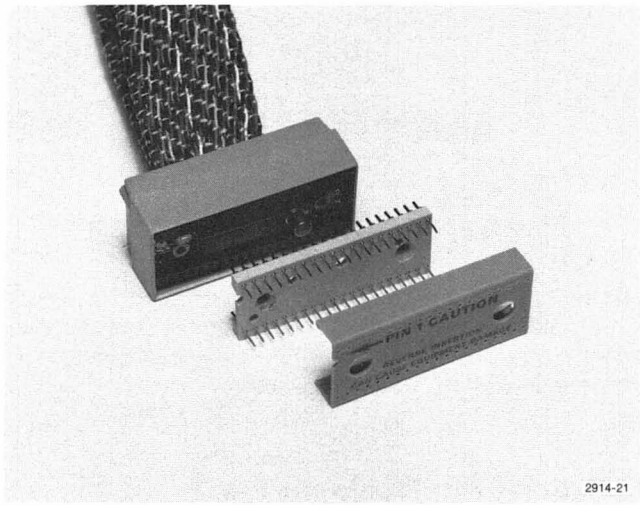


Fig. 6-2.
How to Disassemble Personality Module Microprocessor Plug

Several methods of verifying performance are available to the service technician for localizing and identifying problems in the PM102/PM103. The Performance Check in Section 5 tests many of the functions of the Personality Module. The 7D02 Diagnostics also test the Personality Module. The Troubleshooting Procedure in this section is designed 1) to verify that the fault lies with the personality module, and not the logic analyzer; and 2) to aid the user in isolating the problem in the personality module. The procedure makes use of the personality module self-test circuitry, 7D02 Diagnostics, and signature analysis.

How to Use the Self Test Circuitry

On the bottom side of the PM102/PM103 Personality Module is a plastic door covering the self-test stimulus generator outputs. Some 7D02 diagnostic tests will run only if the self-test plug is inserted into the test socket. The 7D02 indicates when this is necessary with the message "PLEASE CONNECT SELF TEST STIMULUS."

The self test should only be used in a service situation. For a better understanding of self test circuitry, see Section 4, Theory of Operation.

Before starting the Self Test procedure, the mainframe power switch is turned off, the 7D02 is installed in the mainframe, PM102/103 is installed in the 7D02.

1. If a microprocessor is in the personality module ZIF socket, remove it. Never operate the self test with the microprocessor in the ZIF socket.
2. Open the plastic cover on the bottom of the pod by inserting a small screw driver into the latch slot and gently prying up the cover.
3. Switch jumper P1070 to pins 2 and 3, the power-on position for self-test. (Pin 1 is marked with an arrow.)

4. Insert the P. M. microprocessor plug into the test socket. Make sure the microprocessor plug is inserted correctly, with pin 1 in the proper position. The cable should not be twisted. (See Fig. 6-3.)

5. Connect the 7D02 timing option plug to TP10-17, located next to the test socket.

Personality Module Test Point	Timing Option
TP 9	White
TP 10	Black
TP 11	Brown
TP 12	Red
TP 13	Orange
TP 14	Yellow
TP 15	Green
TP 16	Blue
TP 17	Violet

6. While holding down any 7D02 key to force the 7D02 into diagnostic mode, turn the mainframe power switch on.

7. Select and execute the desired 7D02 diagnostic tests. The only 7D02 diagnostic tests that require the microprocessor plug in the self test socket are 0 - TEST ALL, 9 - PER. MOD. - SYSTEM, and B -TIMING OPTION.

8. For more information about the diagnostic tests for the PM102/PM103, see Troubleshooting Procedure, below.

9. When testing is completed, turn off the mainframe power switch.

10. Remove the microprocessor plug from the self test socket. Remove the 7D02 timing option plug from TP9-17.

11. Return P1070 to pins 1 and 2.

12. Replace the plastic cover.

CAUTION

Always protect the self test socket by replacing the plastic cover when through testing.

How to Use the 7D02 Diagnostic Module 9 — PER. MOD. — SYSTEM

This module consists of eight subtests. The PM102/PM103 supports only subtests 1, 2, 3, 4, and 7. Subtests 3, 4, and 7 require that the microprocessor plug be connected to the self-test circuitry. Read the subsection "How To Use the Self-Test Circuitry."

1. Subtest 1 reads a byte at address 3:E010 in the Personality Module PROM to determine the PROM length. This tells the location of the PROM trailer, YY. The value at YYFC is compared with the value in the next byte, YYFD, which should be its complement. If the two bytes are not complementary, an error message is printed as follows:

```
1    FAIL    3E7FD-X
1    FAIL    3YYFD-X   ; INCORRECT VALUE @ 3:E010
```

Where: YY is the value read from E010.
X is the first non-complementary bit after the two bytes are compared on a bit-by-bit basis.

If the part number is correct, the following message is printed:

```
1 PASS 0854-00
```

2. Subtest 2 calculates a 16-bit checksum on the PROM. If the checksum does not match the expected value of 1E57, the calculated value is reported as an error, as follows:

```
2 FAIL XXXX
```

where XXXX = the calculated value.

3. Subtest 3. The personality module microprocessor plug must be connected to the self-test circuitry for this and the following subtests. Read "How To Use the Self-Test Circuitry." Prior to running this test, the four 7D02 Word Recognizers are programmed as follows:

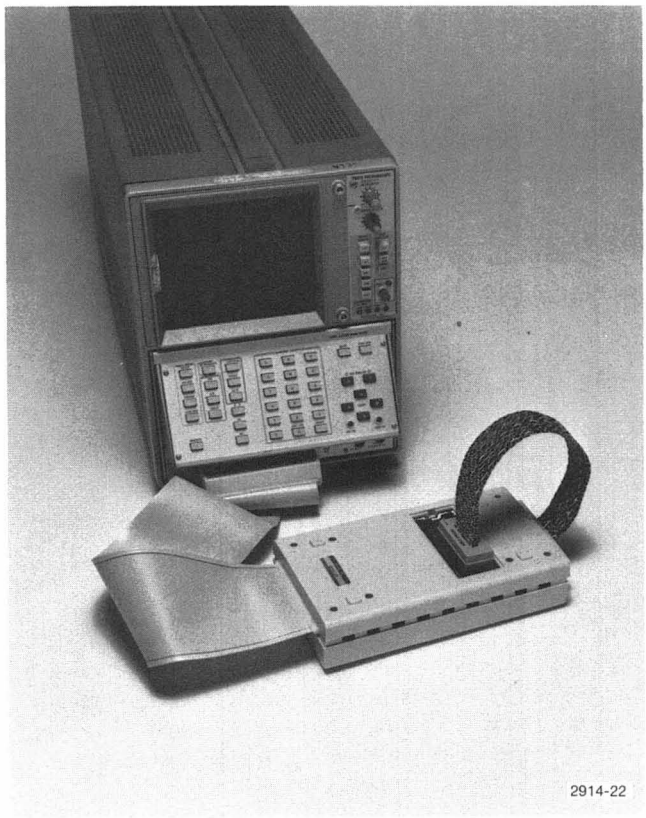


Fig. 6-3.
PM102 with microprocessor plug inserted into Self-Test socket.

	D7-D0	A15-A0	IOC	BA	FETCH	/IRQ	/NMI	R/W
WR1	40	0000	0	0	1	1	0	1
WR2	35	5055	0	0	1	1	0	1
WR3	A0	8080	0	1	0	1	0	1
WR4	7E	FFFE	1	0	0	1	1	1

Since the PM102/PM103 does not support the expansion option, A16-A23 and D8-D15 are set to X (don't care). The External Trigger and ASYNC Trigger are set to X (don't care). The Word Recognizers remain programmed to these values throughout the remaining Personality Module subtests.

The 7D02 State Machine is programmed to execute the following test sequence:

```
1   IF WR1 THEN TRIGGER MAIN AND TIMING
1   IF WR2 OR WR3 OR WR4, THEN DON'T TRIGGER
1   GOTO 1
```

The 7D02 Acquisition Memory board is set for zero delay. The 7D02 front end qualifiers and the clock shifter/Divider are programmed to default values (falling clock edge, C9-C4=XXX1XX) according to data stored in the personality module ROM. After all setups are complete, a DISPLAY command is sent and the 7D02 slow clock detector is checked. A slow clock indication will result in the following error:

```
3       FAIL   0FF60-1  ;  SLOW, OR NO CLOCK
```

This can be caused by an erratic or missing clock from the personality module. Anything that generates or transfers the test clock to the 7D02 should be checked.

If the clock appears to be running, the Personality Module ROM is read to determine how long to wait for a trigger to occur. Then, a STORE command is sent. After waiting the specified length of time, the activity monitor on the acquisition memory board is examined to see if the Main Section has triggered and returned to DISPLAY mode. If the main section is still in STORE mode, the following error is generated.

```
3       FAIL   2E803-7  ;  MAIN SECTION FAILED TO TRIGGER
```

Failure to trigger can be caused by failure of the personality module to generate the WR1 value.

4. Subtest 4. This test involves all four 7D02 Word Recognizers, the two 7D02 Counters, the 7D02 State Machine and the 7D02 Acquisition Memory.

The 7D02 word recognizers are programmed the same as for subtest 3. The 7D02 state machine is also programmed with the following program:

```
IF WR1 THEN GO TO 2, AND RESET CTR 1 AND 2
IF WR2 THEN GO TO 3
   ELSE INC. CTR 1
IF WR3 THEN GO TO 4
   ELSE INC. CTR 2
IF WR4 THEN TRIGGER MAIN
```

The 7D02 front end qualifiers are programmed to default values. After all steps are complete, a DISPLAY command is sent and the slow clock detector is checked. A slow clock indication results in the following error:

```
4       FAIL   0FF60-1  ;  SLOW, OR NO CLOCK
```

This can be caused by an erratic or missing clock from the personality module. Anything in the personality module that generates or transfers the test clock should be checked.

If the clock appears to be running, the personality module ROM is read to determine how long to wait for a trigger. Then, a STORE command is sent. After waiting 2 Msec., the activity monitor on the 7D02 acquisition memory board is examined to see if the main section has triggered and returned to DISPLAY mode. If still in the STORE mode, the following error is generated:

```
4       FAIL   2E803-7    ;  MAIN SECTION FAILED TO TRIGGER
```

Failure to trigger can be caused by failure of the personality module to generate any one of the four 7D02 word recognizer values.

Next, all bytes in the 7D02 acquisition memory between 2:E000 and 2:E3FF are summed and the result of the checksum is compared with the expected data stored in the personality module ROM.

Failure of the comparison results in the following error message:

```
4          FAIL          3E035-X  ;  MAIN ACQ. MEM. FAILS CHECKSUM
```

Failure of the checksum to match is either an intermittent channel, or the FETCH predictor circuitry operating erratically.

5. Subtest 7. This test checks the clock qualifier lines C9-C4 on the 7D02 Front End Board.

The 7D02 state machine is programmed with the following test sequence:

```
1      IF WR1      THEN TRIGGER MAIN
1                  ELSE GO TO 1
```

C9-C4 are given the following values, respectively: 101100.

@

Word recognizer 1 was programmed in an earlier subtest to a value specified by the personality module ROM. This test uses each of the control lines in turn to qualify out the value to which Word Recognizer 1 has been programmed.

If the control line works correctly, the state clock that occurs with Word Recognizer 1 will be inhibited and the state machine will not see the Word Recognizer output. A PASS condition, then, is indicated by the failure of the Main Section to trigger. The processor waits 2 Ms. to trigger.

Six bytes in the personality module ROM specify the value to sent to the 7D02 front end to inhibit State Clocks when word recognizer 1 occurs for each of the six control lines. The following sequence is repeated six times, once for each control line or until a failure occurs:

- Read value from personality module ROM
- Write value to Front End Latch
- Send STORE command
- Wait specified length of time
- Check Activity Monitor on Acquisition Memory board
- If in DISPLAY mode, print FAIL and STOP

If subtest 3 and 4 pass, it is safe to assume that this test is operating correctly.

The test results are interpreted as follows:

```
7       FAIL   3E039       ; C4 DIDN'T INHIBIT TRIGGER
7       FAIL   3E03A       ; C5 DIDN'T INHIBIT TRIGGER
7       FAIL   3E03B       ; C6 DIDN'T INHIBIT TRIGGER
7       FAIL   3E03C       ; C7 DIDN'T INHIBIT TRIGGER
7       FAIL   3E03D       ; C8 DIDN'T INHIBIT TRIGGER
7       FAIL   3E03E       ; C9 DIDN'T INHIBIT TRIGGER
```

How to Use 7D02 Diagnostic Module B - TIMING OPTION

This module consists of 3 subtests. The only subtest supported by the PM102/PM103 is subtest 3.

This test requires stimulus from the Personality Module and is not run during the Power-up Verification. See "How To Connect the Self-Test Circuitry" for directions on plugging in the P6451 probe to the correct pins in the self-test socket.

The personality module provides the stimulus via the P6451.

The Timing Option Word Recognizer is set to trigger on the occurrence of 55H.

The 7D02 state machine is programmed with the following test program:

```
1 IF TIMING OPTION WR = 55H WR1 = TIMING WR
1 AND WR2, 3, 4, = DON'T CARE
1 THEN
1 GO TO 4

4 IF TIMING OPT WR = 55H WR1 = TIMING WR
4 WR 2, 3, 4, = DON'T CARE
4 THEN TRIGGER
4 TIMING
4 AND
4 MAIN
```

The timing option memory address counter is set to 0. All word recognizers except the timing option are set to x (don't care).

The slow clock indicator is checked for the presence of a clock. If non is detected, the following error is printed:

```
3   FAIL  0FF60-1   ; SLOW OR NO CLOCK DETECTED
```

If the clock appears to be running, a byte is read from the personality module ROM that specifies how long to wait for a trigger. Then a STORE command is sent. After waiting the specified time (2 msec.) the 7D02 acquisition memory activity monitor is examined to see if the main section has triggered. If it hasn't, the following error is reported:

```
3       FAIL   2E803-7   ;  MAIN SECTION FAILED TO TRIGGER
```

This can be caused by the self test circuitry not generating the 55H value or the P6451 not transferring data properly.

If the trigger occurred, the timing option memory address counter is examined to determine the last data location and the trigger location is calculated. The value saved in the trigger location is then compared with the value in the personality module ROM that was used to program the timing option word recognizer. If the two are not complementary (data are inverted), the following error is reported:

```
3   FAIL   3E03F-X    ;   TRIGGER VALUE INCORRECT
```

This can be caused by a bad timing relationship between the clock and data.

If the trigger test passes, the timing option acquisition memory at address 2:F000-2:F0FF is checksummed (with the exception of one data byte which is X's) and the result compoared with the expected value stored in the personality module ROM. If the values are not the same, the following error is reported:

```
3 FAIL  3E040-X    ; CHECKSUM ERROR 2:F000-2:F0FF
```

Where: X indicates the bit that didn't match.

This can be caused by the self test circuitry not generating the correct pattern all the time or an intermittent failure in the P6451.

Signature Analysis

Introduction A "signature" is a four-digit hexadecimal number representing time-dependent logic activity during a specified measurement interval for a given circuit node. Any change in the behavior of this node (even a transition that occurs one clock cycle late) will produce a different signature, indicating a probable malfunction in the circuit.

The signal that causes the node to produce a signature is the "stimulus". In signature analysis, the stimulus is supplied by the personality module itself. This way, a controlled environment is created wherein selected portions of the circuit are tested independently, while maintaining full dynamic operation. The personality module supplies this predictable stimulus when the microprocessor plug is inserted into the self test socket.

1. Use a Sony/Tektronix Type 308 with P6451 probe.
2. Insert the Personality Module logic analyzer plug into a logic analyzer. Leave the mainframe power switch OFF.
3. Lay out the Personality Module boards as described in "How to Disassemble Personality Module Pod."
4. Connect the microprocessor plug to the self-test socket on the bottom board, A2. Be careful to insert pin 1 in the proper position.
5. Move jumper P1070 to pins 2 and 3 to enable the self-test circuit.
6. Connect the Signature Analyzer probe clock lead to Test Point 7.
7. Connect the Signature Analyzer start/stop leads to Test Point 17.
8. Set start and stop triggering to rising edge.
9. Set clock to rising edge.
10. Turn on the logic analyzer power switch and hold down any key on the keyboard to force the logic analyzer into diagnostic mode.
11. Press the X key on the logic analyzer to obtain a display of the diagnostic menu on the screen.
12. Press the F key to select SIGNATURE EXERCISER MENU.
13. Press the 7 key to select PER. MOD. - SYSTEM
14. The signature for the +5 is CC34.
15. The signature for GND is 0000.

Signature Tables

		S/W	SIG
Clock	TP7	^	N/A
Start	TP17	^	H58A
Stop	TP17	^	H58A

Test Point	Signature
0	3362
1	F05C
2	F5AH
3	60PF
4	HUHU
5	722C
6	08U6
7	0000
10	96PF
11	725C
12	P5PH
13	5CP0
14	7P25
15	85PA
16	77F7
17	H58A

U1030	Signature
1	0000
2	0000
3	CC34
4	0000
5	CC34
6	0000
8	086U
9	C3F2
10	0000
11	CC34
12	CC34
13	0000

U1040	Signature
1	CC34
2	CC34
7	CC34
9	CC34
10	826P
11	H58A
12	77F7
13	85PA
14	7P25
15	C3F2
16	CC34

U1050	Signature
1	CC34
2	CC34
7	CC34
9	CC34
10	CC34
11	5CP0
12	P5PH
13	725C
14	96PF
15	826P
16	CC34

U1060	Signature
1	96PF
2	725C
3	P5PH
4	5CP0
5	7P25
6	HH85
7	85FA
8	PC6A
9	HFC1
10	0000
11	35F5
12	0A78
13	88AA
14	4UPF
17	85PA
18	77F7
19	H58A

U2010	Signature
1	08U6
2	08U6
3	1U86
4	188P
5	8856
6	HFC1
8	HHU3
9	3362
10	188P
11	1U86
12	8A98
13	826P

U2020	Signature
1	HUHU
2	PC6A
3	F05C
4	F5AH
5	60PF
6	1U86
8	C05H
9	6CH3
10	31AF
11	2HH8
12	311H
13	31AF

U2030	Signature
1	3362
2	8856
3	HFC1
4	6785
5	HHU3
6	66F7
8	0000
9	CC34
12	2HH8
13	96PF

U2040	Signature
2	96PF
3	96PF
4	CC34
6	2HH8
7	96PF
10	0810
11	H58A
12	CC34
13	31HF
14	0810

U2060	Signature
2	65PA
3	CC34
5	HUHU
8	A3CA
9	188P
11	CC34
12	311H

U3010	Signature
2	96PF
3	2HH8
4	F96U
5	P4C7
6	2U6F
7	5PH9
8	P0H4
9	U06A
11	CC34
12	P288
13	F511
14	C14F
15	3P08
16	7U61
17	339P
18	U4H8
19	7A6F

U3020	Signature
1	7U61
2	3P08
3	P288
4	U06A
5	96PF
6	P4C7
7	2U6F
9	60PF
10	F5AH
11	F05C
12	3362
15	7A6F

U3030	Signature
1	HFC1
2	0000
3	3362
4	F05C
5	F5AH
6	60PF
9	H3CH
10	HUHU
15	1PFP

U3040	Signature
2	1PFP
3	HFC1
4	0000
5	HUHU
6	08U6
7	C3F2
9	F91U
10	722C
12	0000
14	66F7
15	HUHU

U3050	Signature
1	0000
2	0000
3	96PF
4	2HH8
5	188P
6	HFC1
8	0000
9	2HH8
10	96PF
11	188P
12	6785
13	6785

U3060	Signature
1	C3F2
2	C05H
3	08U6
4	F91U
5	1PFP
6	65PA
8	0000
9	PC6A
10	PC6A
11	F91U
12	722C
13	C05H

U7030	Signature
2	HFC1
3	HH85
4	H58A
5	35F5
6	8A98
7	PC6A
8	311H
9	85FA
11	85FA
12	311H
13	PC6A
14	8A98
15	35F5
16	H58A
18	HFC1

U7040	Signature
1	CC34
2	HH85
3	66C1

U2040	Signature
2	H58A
3	96PF
4	85PA
5	P5PH
6	5CP0
7	7P25
8	725C
9	77F7
11	77F7
12	725C
13	7P25
14	5CP0
15	P5PH
16	85PH
17	96PF
18	H58A

U3040	Signature
2	5CP0
3	H58A
4	85PA
5	77F7
6	85PA
7	85PA
8	5CP0
9	7P25
11	7P25
12	5CP0
13	85PA
14	85PA
15	77F7
16	85PA
17	H58A
18	5CP0

U4040	Signature
1	7P25
2	H58A
3	H58A
4	77F7
5	85PA
6	5CP0
7	85PA
9	6CH3
10	7P25
11	5CP0
12	85PA
13	85PA
14	5CP0
15	77F7

U5040	Signature
2	77F7
3	85PA
4	7P25
5	5CP0
6	85PA
7	85PA
8	5PC0
9	H58A
11	H58A
12	5CP0
13	85PA
14	85PA
15	5CP0
16	7P25
17	85PA
18	77F7

U6040	Signature
2	88AA
3	F96U
4	7P25
5	P0H4
6	P5PH
7	C14F
8	96PF
9	U4H8
11	4UPF
12	2HH8
13	0A78
14	5PH9
15	5CP0
16	F511
17	725C
18	339P

U2050	Signature
2	77F7
3	725C
4	7P25
5	5CP0
6	P5PH
7	85PA
8	96PF
9	H58A
11	H58A
12	96PF
13	85PA
14	P5PH
15	5CP0
16	7P25
17	725C
18	77F7

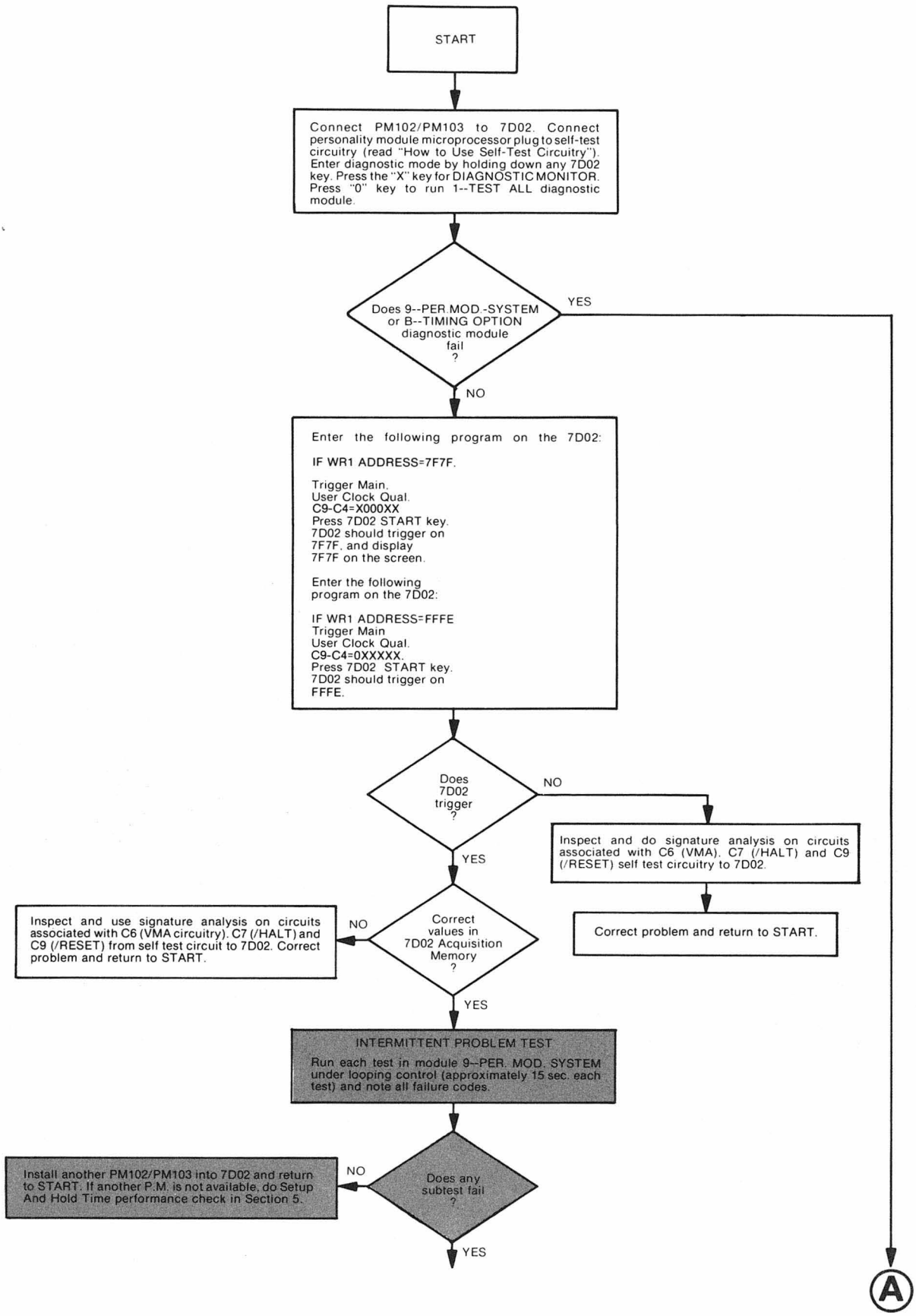
U3050	Signature
1	H58A
2	77F7
3	85PA
4	7P25
5	5CP0
6	P5PH
7	725C
8	96PF
18	CC34
19	85PH
21	CC34
22	85PA
23	5CP0

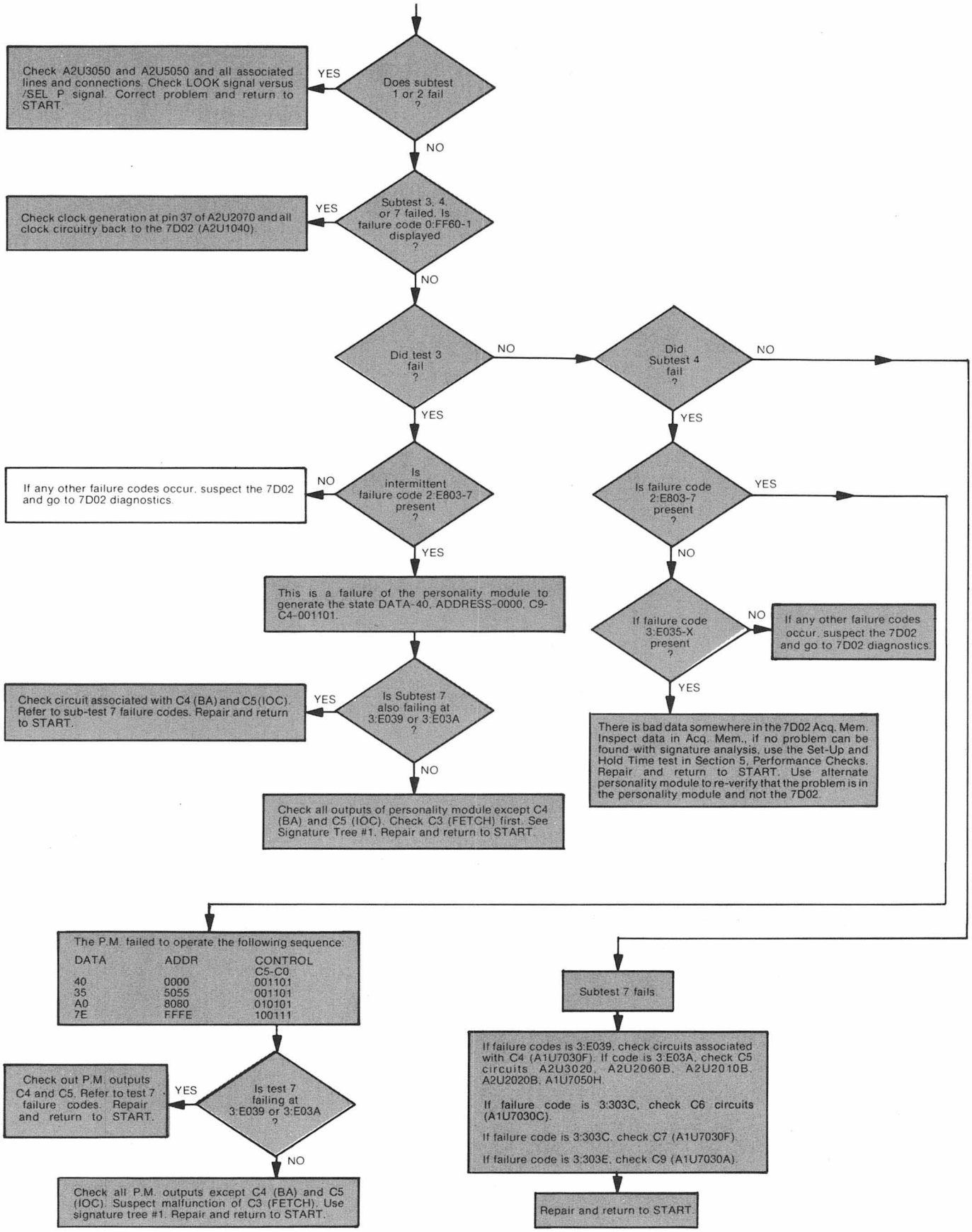
U5050	Signature
3	96PF
5	P5PH
7	7P25
9	88AA
12	725C
14	5CP0
16	0A78
18	4UPF

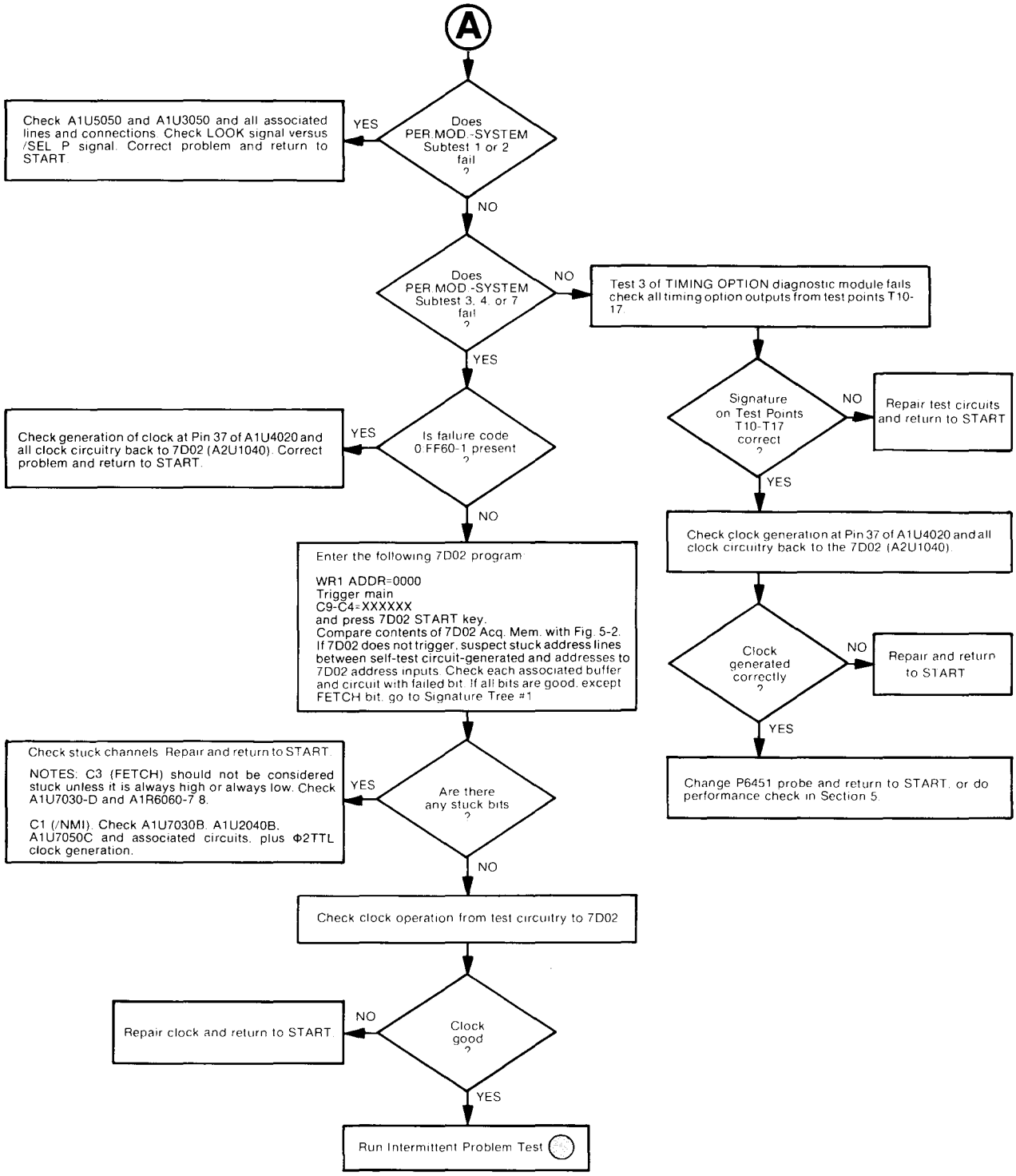
U6050	Signature
1	0000
2	U4H8
3	96PF
4	C14F
5	P5PH
6	P0H4
7	7P25
8	F96U
9	88AA
11	339P
12	725C
13	F511
14	5CP0
15	5PH9
16	0A78
17	2HH8
18	4UPF

U7050	Signature
1	0000
2	66C1
3	6785
4	8A98
6	0810
9	HH85
11	66C1
14	C324
16	31HF
17	HFC1

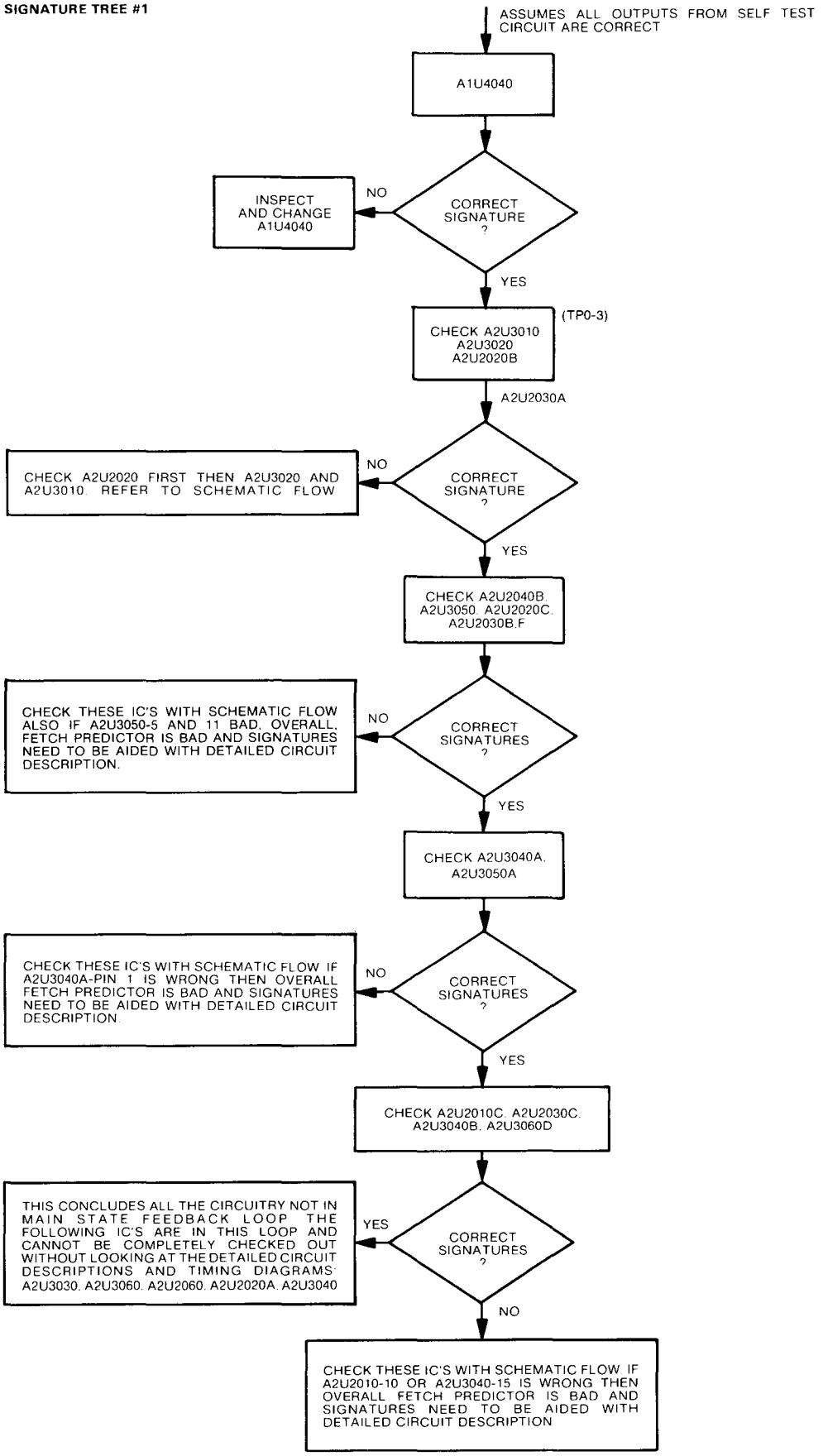
Troubleshooting Procedures







SIGNATURE TREE #1



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REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

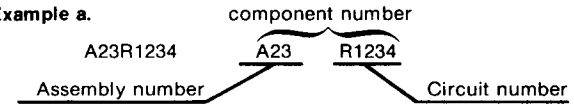
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

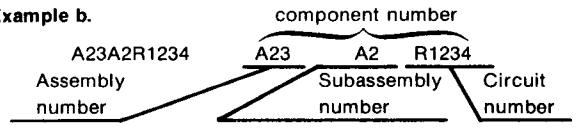
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
14433	ITT SEMICONDUCTORS	3301 ELECTRONICS WAY P O BOX 3049	WEST PALM BEACH, FL 33402
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
52648	PLESSEY SEMICONDUCTORS	1641 KAISER	IRVINE, CA 92714
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-6117-00			CKT BOARD ASSY:6800 PROBE #1	80009	670-6117-00
A2	670-6118-00			CKT BOARD ASSY:6800 PROBE #2	80009	670-6118-00
A3	670-6149-00			CKT BOARD ASSY:PROBE CONNECTOR	80009	670-6149-00
	----- -----			(NO ELECTRICAL PARTS)		
A4	----- -----			CKT BOARD ASSY:6800 PROBE(PM102)		
	----- -----			(NOT REPL ORDER 175-2678-00. NO ELEC PARTS)		
A5	----- -----			CKT BOARD ASSY:6802 EMULATOR PROBE(PM103)		
	----- -----			(NOT REPLACEABLE ORDER 175-2679-00)		
A1	----- -----			CKT BOARD ASSY:6800 PROBE #1		
A1C1020	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A1C1039	283-0342-00			CAP.,FXD,CER DI:6.PF,0.5%,2000V	72982	808-536A659D
A1C1041	283-0168-00			CAP.,FXD,CER DI:12PF,5%,100V	72982	8101B121C0G0120J
A1C1046	283-0330-00			CAP.,FXD,CER DI:100PF,5%,50V	72982	8111N068C0G0101J
A1C1049	283-0157-00			CAP.,FXD,CER DI:7PF,5%,500V	72982	8111B064C0H0709J
A1C1051	281-0700-00			CAP.,FXD,CER DI:3.3PF,10%,200V	72982	374005S3B0339K
A1C1056	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C1060	283-0346-00			CAP.,FXD,CER DI:0.47UF,+80-20%,100V	72982	8131-M100F474Z
A1C2060	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A1C3064	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C3066	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C6044	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C6049	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C6054	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A1C7029	283-0346-00			CAP.,FXD,CER DI:0.47UF,+80-20%,100V	72982	8131-M100F474Z
A1C7030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1CR1033	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR1034	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR1035	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR1036	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR1037	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR1038	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR1039	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR1043	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR1044	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR1055	152-0071-00			SEMICOND DEVICE:GERMANIUM,15V,40MA	14433	G865
A1CR1056	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A1CR1059	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A1CR2035	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR2036	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR2037	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR3035	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR3036	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR3037	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR3038	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR3039	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR4035	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR4036	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR4037	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR5037	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR5038	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR5039	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR6033	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR6034	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR6035	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR6036	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1CR6038	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR6039	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A1CR7012	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR7025	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR7026	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR7027	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR7028	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR7051	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A1Q1056	151-0282-00			TRANSISTOR:SILICON,NPN	80009	151-0282-00
A1Q1063	151-0427-00			TRANSISTOR:SILICON,NPN	80009	151-0427-00
A1Q1065	151-0427-00			TRANSISTOR:SILICON,NPN	80009	151-0427-00
A1R1023	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R1024	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R1025	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R1026	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R1027	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R1028	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R1029	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R1032	321-0344-00			RES.,FXD,FILM:37.4K OHM,1%,0.125W	91637	MFF1816G37401F
A1R1042	321-0631-00			RES.,FXD,FILM:12.5K OHM,1%,0.125W	91637	MFF1816G12501F
A1R1045	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A1R1051	321-0274-00			RES.,FXD,FILM:6.98K OHM,1%,0.125W	91637	MFF1816G69800F
A1R1052	321-0286-00			RES.,FXD,FILM:9.31K OHM,1%,0.125W	91637	MFF1816G93100F
A1R1053	321-0208-00			RES.,FXD,FILM:1.43K OHM,1%,0.125W	91637	MFF1816G14300F
A1R1057	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R1058	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A1R1062	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	01121	CB1625
A1R2010	315-0182-00 ----- -----	B010100	B010160X	RES.,FXD,CMPSN:1.8K OHM,5%,0.25W (PM102 ONLY)	01121	CB1825
A1R2010	315-0182-00 ----- -----	B010100	B010220X	RES.,FXD,CMPSN:1.8K OHM,5%,0.25W (PM103 ONLY)	01121	CB1825
A1R2031	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R2032	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R2033	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R2060	307-0721-00			RES.,NTWK,FXD,FI:5.68 OHM,2%,1.5W	01121	210A680
A1R2070	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.W	01121	210A680
A1R2080	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210A680
A1R3031	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R3032	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R3033	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R3034	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R3035	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R4031	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R4033	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R4034	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R4050	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210A680
A1R5031	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R5032	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R5033	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R5034	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R5060	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210A680
A1R6031	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R6032	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R6033	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R6035	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R6036	315-0331-03			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A1R6060	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210A680

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1R7011	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R7015	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R7016	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R7021	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R7022	315-0821-03			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R7060	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	01121	210A680
A1U1040	156-1344-00			MICROCIRCUIT,LI:COMPARATOR	52648	SP9685CM
A1U2040	156-0956-04			MICROCIRCUIT,DI:OCTAL,BFR W/3 STATE OUT	80009	156-0956-04
A1U3040	156-0956-04			MICROCIRCUIT,DI:OCTAL,BFR W/3 STATE OUT	80009	156-0956-04
A1U3050	160-0854-00			MICROCIRCUIT,DI:2048 X 8 EPROM	80009	160-0854-00
A1U4040	156-0866-02			MICROCIRCUIT,DI:13 INP NAND GATES	80009	156-0866-02
A1U5040	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	80009	156-0956-04
A1U5050	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A1U6040	156-0914-03			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	80009	156-0914-03
A1U6050	156-0914-03			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	80009	156-0914-03
A1U7030	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	80009	156-0956-04
A1U7040	156-0721-02			MICROCIRCUIT,DI:QUAD 2-IN NAND,SCHMITT TRIG	80009	156-0721-02
A1U7050	156-0914-03			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	80009	156-0914-03
A1VR1061	152-0611-00			SEMICOND DEVICE:ZENER,0.4W,9V,2%	80009	152-0611-00
A1VR2010	152-0195-00	XB010161		SEMICOND DEVICE:ZENER,0.4W,5.1V,5% (PM102 ONLY)	04713	SZ11755
A1VR2010	152-0195-00	XB010221		SEMICOND DEVICE:ZENER,0.4W,5.1V,5% (PM103 ONLY)	04713	SZ11755

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2	----- -----			CKT BOARD ASSY:6800 PROBE #2		
A2C1010	283-0114-00			CAP.,FXD,CER DI:0.0015UF,5%,200V	72982	805-509B152J
A2C1011	283-0114-00			CAP.,FXD,CER DI:0.0015UF,5%,200V	72982	805-509B152J
A2C1034	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C1044	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C1049	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C1070	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2015	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2029	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2059	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2076	283-0260-00 ----- -----	XB010200		CAP.,FXD,CER DI:5.6PF,5%,200V (PM102 ONLY)	72982	8111B200C0G569C
A2C2076	283-0260-00 ----- -----	XB010380		CAP.,FXD,CER DI:5.6PF,5%,200V (PM103 ONLY)	72982	8111B200C0G569C
A2C3039	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C3069	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2L1018	108-0766-00			COIL,RF:FIXED,7.07UH	80009	108-0766-00
A2Q1020	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A2R1021	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A2R1023	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	01121	CB1335
A2R2075	315-0682-00 ----- -----	XB010200		RES.,FXD,CMPSN:6.8K OHM,5%,0.25W (PM102 ONLY)	01121	CB6825
A2R2075	315-0682-00 ----- -----	XB010380		RES.,FXD,CMPSN:6.8K OHM,5%,0.25W (PM103 ONLY)	01121	CB6825
A2U1030	156-0645-02			MICROCIRCUIT,DI:SCHMITT-TRIG POS-NAND	01295	SN74LS14
A2U1040	156-0784-02			MICROCIRCUIT,DI:SYNC 4 BIT BINARY COUNTER	27014	DM74LS163ANA+
A2U1050	156-0784-02			MICROCIRCUIT,DI:SYNC 4 BIT BINARY COUNTER	27014	DM74LS163ANA+
A2U1060	160-0855-00			MICROCIRCUIT,DI:256 X 8 PROM,PROGRAMMED	80009	160-0855-00
A2U2010	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74LS10NP3
A2U2020	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	80009	156-0718-03
A2U2030	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A2U2040	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGETRIGGERED	01295	SN74S374JP3
A2U2060	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A2U3010	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A2U3020	160-0856-00			MICROCIRCUIT,DI:256 X 4 PORM,PROGRAMMED	80009	160-0856-00
A2U3030	156-0784-02			MICROCIRCUIT,DI:SYNC 4 BIT BINARY COUNTER	27014	DM74LS163ANA+
A2U3040	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGETRIGGERED	01295	SN74S374JP3
A2U3050	156-0452-02			MICROCIRCUIT,DI:4-WIDE,2-INP AOI,SCREENED	07263	74LS54
A2U3060	156-0452-02			MICROCIRCUIT,DI:4-WIDE,2-INP AOI,SCREENED	07263	74LS54
A5	----- -----			CKT BOARD ASSY:6802 EMULATOR PROBE		
A5C1009	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A5CR1014	152-0322-00	XB010221		SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A5CR1020	152-0008-00			SEMICOND DEVICE:GERMANIUM,75V,60MA	14433	G1409
A5Q1020	151-1049-00	B010100	B010220	TRANSISTOR:SILICON,JFE,N-CHANNEL,DUAL	80009	151-1049-00
A5Q1020	151-1031-00	B010221	B010379	TRANSISTOR:SILICON,FE,N-CHANNEL,DUAL	80009	151-1031-00
A5Q1020	151-1027-00	B010380		TRANSISTOR:SILICON,JFE,N-CHAN	80009	151-1027-00
A5R1010	317-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.125W	01121	BB1055
A5R1014	317-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.125W	01121	BB1055
A5R1020	317-0131-00	B010100	B010379	RES.,FXD,CMPSN:130 OHM,5%,0.125W	01121	BB1315
A5R1020	317-0270-00	B010380		RES.,FXD,CMPSN:27 OHM,5%,0.125W	01121	BB2705
A5R1024	317-0101-00	B010100	B010379	RES.,FXD,CMPSN:100 OHM,5%,0.125W	01121	BB1015
A5R1024	317-0200-00	B010380		RES.,FXD,CMPSN:20 OHM,5%,0.125W	01121	BB2005
A5U1010	156-0645-00			MICROCIRCUIT,DI:HEX SCHMITT-TRIG INVERTER	80009	156-0645-00

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

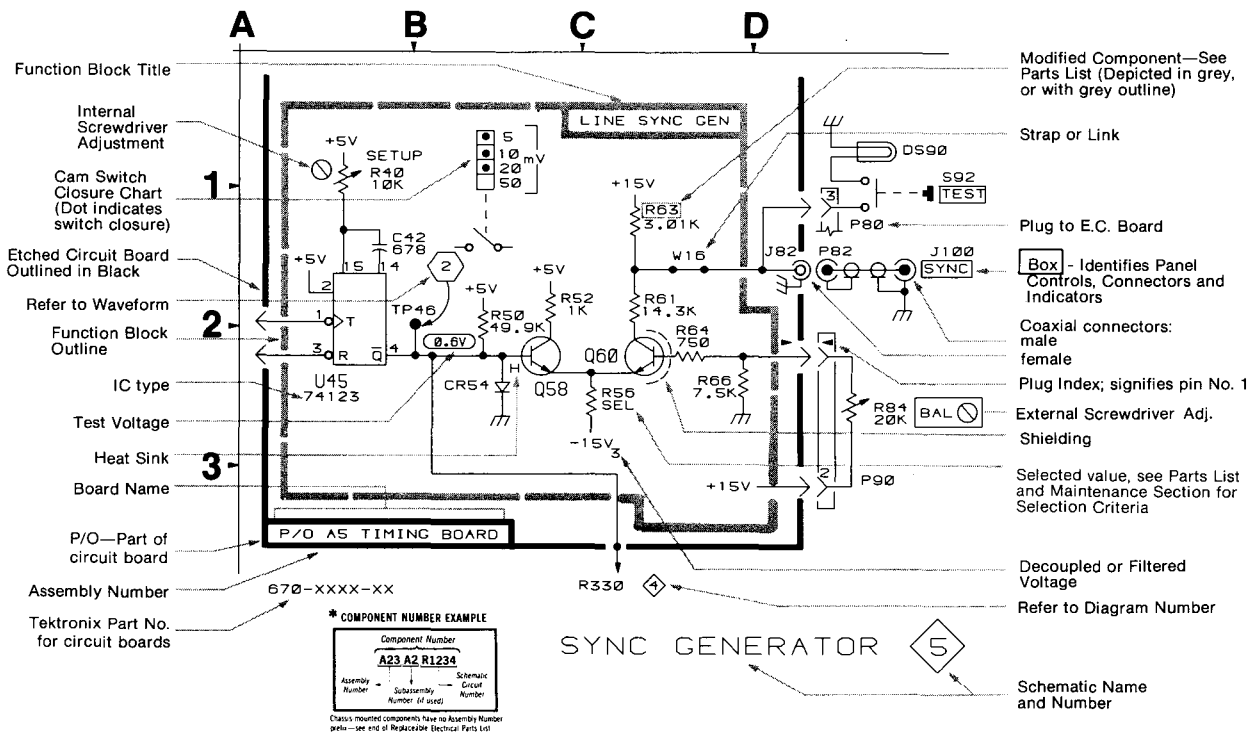
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



@

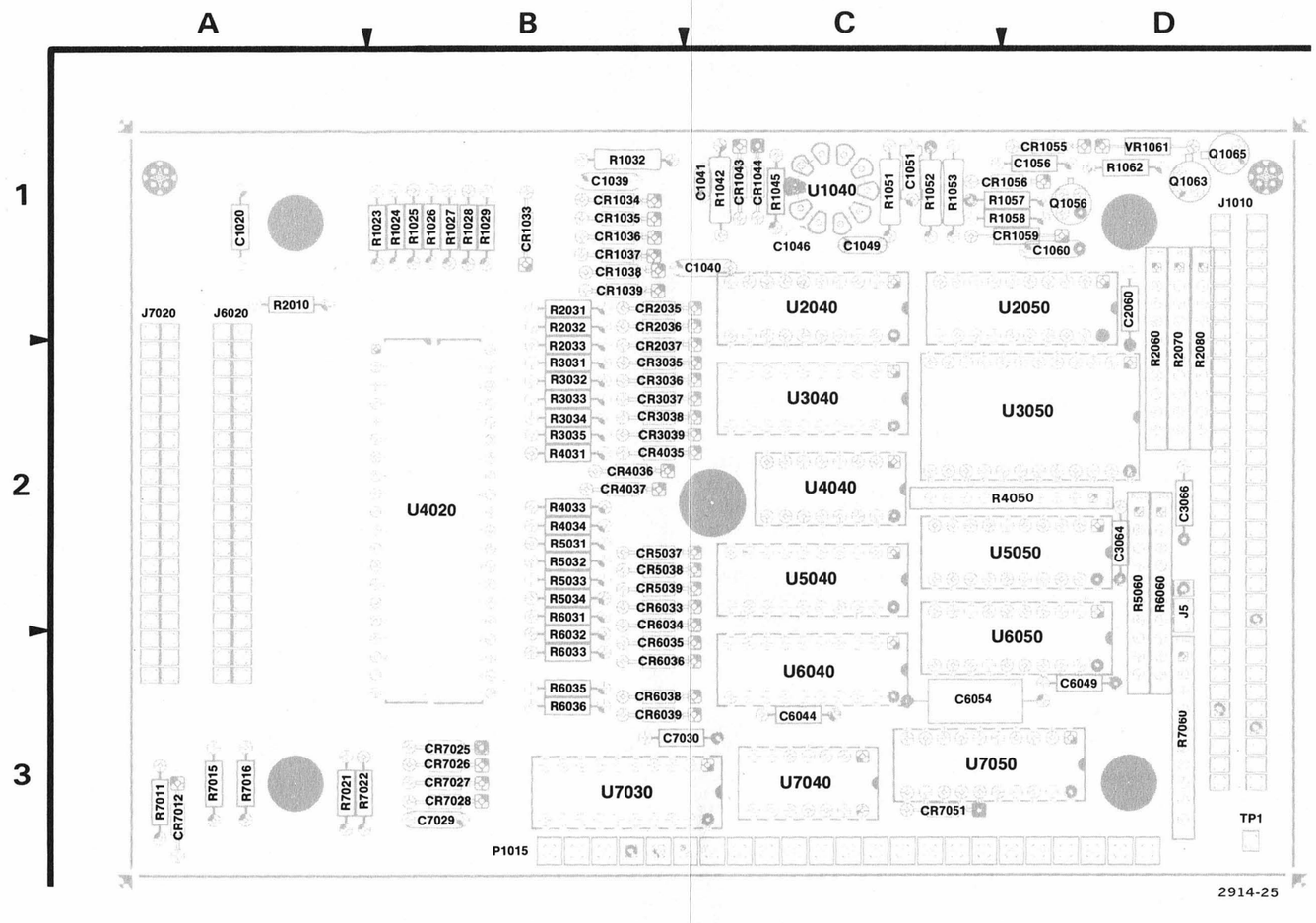


Figure 8-1. A1 Upper Board Component Locations.

Table 8-1

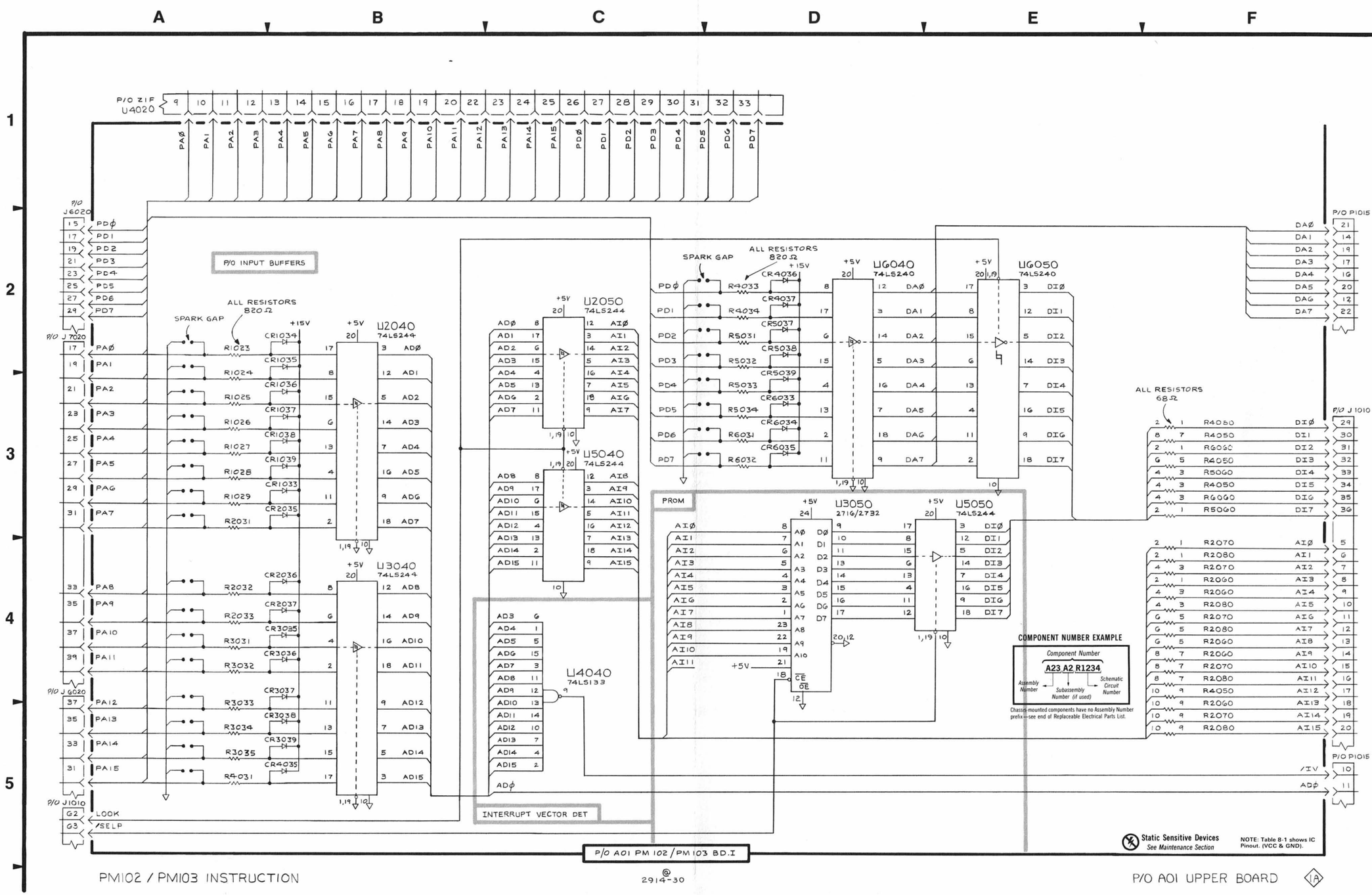
IC Pin Information

Device Type	VCC	GND
2716	24	12
74LS04	14	7
74LS10	14	7
74LS14	14	7
74LS27	14	7
74LS54	14	7
74LS74	14	7
74LS109	16	8
74LS132	14	7
74LS133	16	8
74LS163	16	8
74LS240	20	10
74LS244	20	10
74LS273	20	10
74S472	20	10
93427	16	8

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
CR01033	B3	B1	R1027	A3	B1
CR1034	B2	B1	R1028	A3	B1
CR1035	B3	B1	R1029	A3	B1
CR1036	B3	B1	R2031	A3	B1
CR1037	B3	B1	R2032	A4	B1
CR1038	B3	B1	R2033	A4	B2
CR1039	B3	B1	R2060	F4	D1
CR2035	B3	B1	R2070	F4	D1
CR2036	B4	B1	R2080	F4	D1
CR2037	B4	B2	R3031	A4	B2
CR3035	B4	B2	R3032	A4	B2
CR3036	B4	B2	R3033	A5	B2
CR3037	B4	B2	R3034	A5	B2
CR3038	B5	B2	R3035	A5	B2
CR3039	B5	B2	R4031	A5	B2
CR4035	B5	B2	R4033	D2	B2
CR4036	D2	B2	R4034	D2	B2
CR4037	D2	B2	R4050	F3	C2
CR5037	D2	B2	R4050	F4	C2
CR5038	D2	B2	R5031	D2	B2
CR5039	D3	B2	R5032	D2	B2
CR6033	D3	B2	R5033	D3	B2
CR6034	D3	B2	R5034	D3	B2
CR6035	D3	B3	R5060	F3	D2
			R6031	D3	B2
J1010	F3	D1	R6032	D3	B3
J1010	D2	D1	R6060	F3	D2
J6020	A5	A2			
J6020	A2	A2	U2040	B3	C1
J7020	A2	A2	U2050	C2	D1
			U3040	B4	C2
P1015	A1	B3	U3040	B4	C2
P1015	F5	B3	U3050	D4	D2
P1015	D2	B3	U4020	A1	B2
			U4040	C4	C2
R1023	A2	B1	U5040	C3	C2
R1024	A3	B1	U5050	E4	D2
R1025	A3	B1	U6040	D2	C3
R1026	A3	B1	U6050	E2	C3

Partial A1 also shown on diagram 1B.



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P/O A01 UPPER BOARD 1A

A1 UPPER BOARD 1A

A1 UPPER BOARD

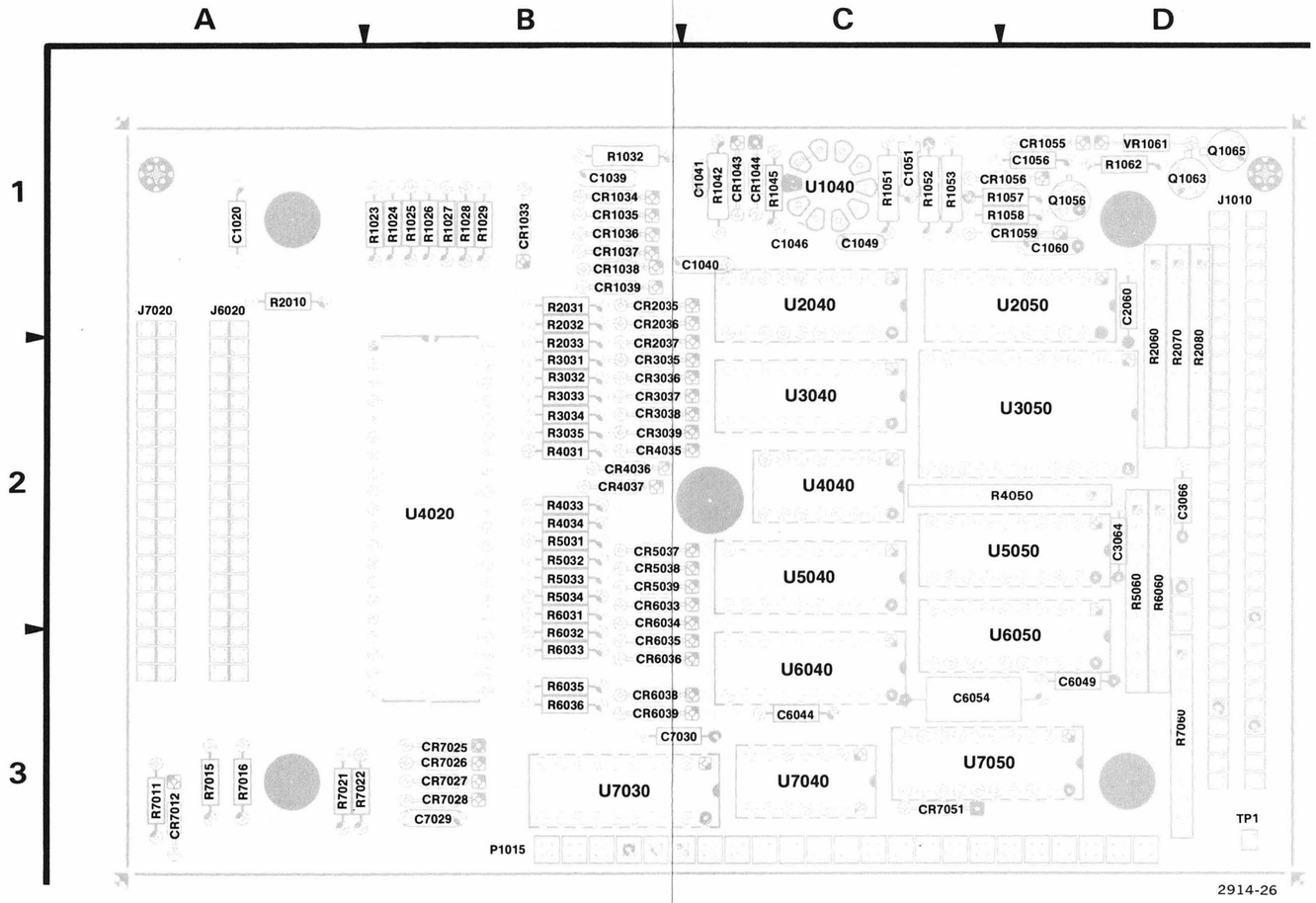
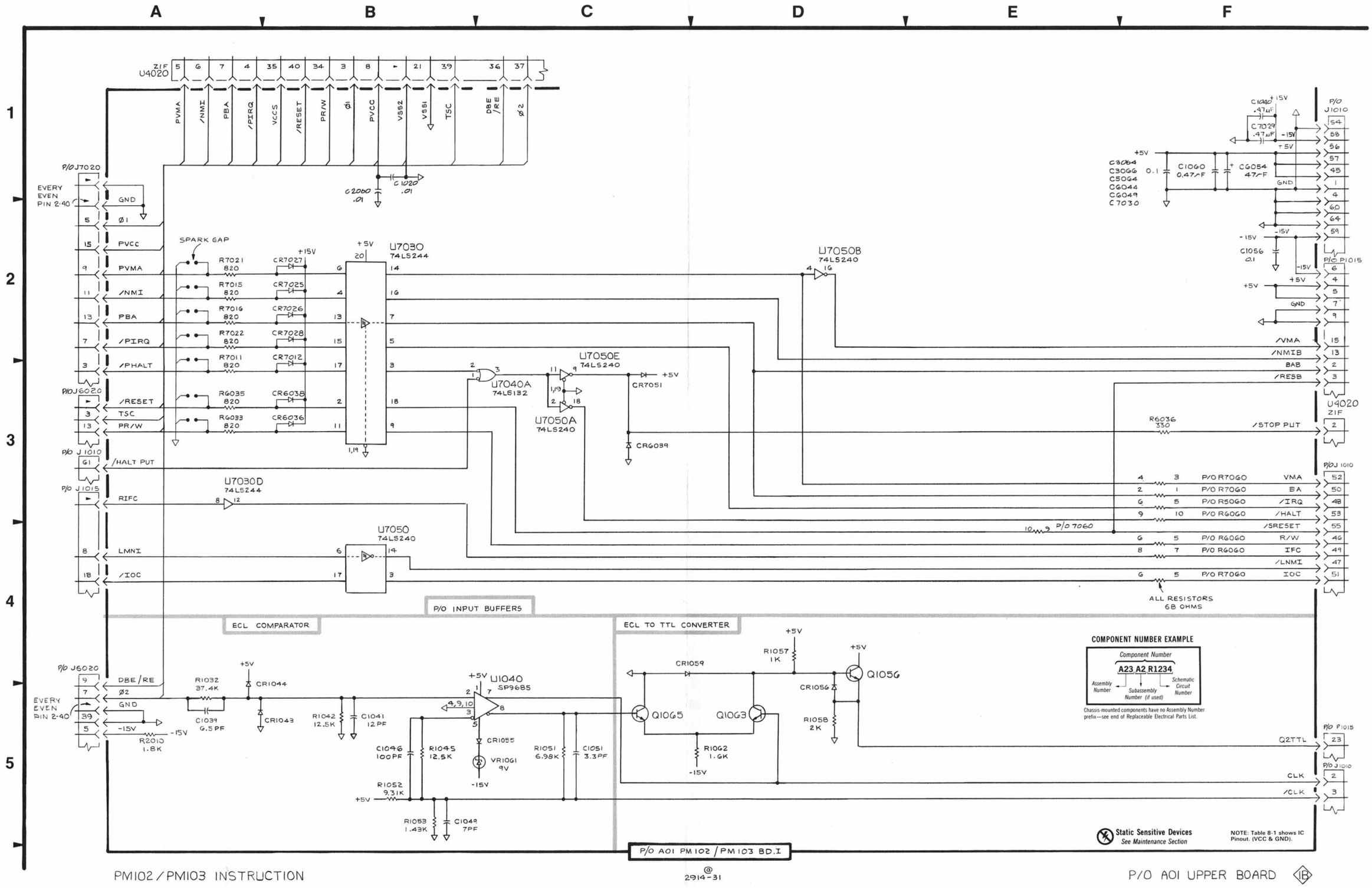


Figure 8-1. A1 Upper Board Component Locations.

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1020	B2	A1	P1015	A3	B3
C1039	A5	B1	P1015	F5	B3
C1041	B4	C1			
C1046	B4	C1	Q1056	D5	D1
C1049	B4	C1	Q1063	D5	D1
C1051	C5	C1	Q1065	C5	D1
C1056	F2	D1			
C1060	F1	D1	R1032	A5	B1
C2060	B1	D1	R1042	B4	C1
C3064	F1	D2	R1045	B4	C1
C3066	F1	D2	R1051	C5	C1
C6044	F1	C3	R1052	B4	C1
C6049	F1	D3	R1053	B4	C1
C6054	F1	C3	R1057	D5	D1
C7029	F1	B3	R1058	D5	D1
C7030	F1	B3	R1062	D5	D1
			R2010	A5	A1
CR1043	B5	C1	R5060	F3	D2
CR1044	B5	C1	R6033	A3	B3
CR1055	C5	D1	R6035	A3	B3
CR1056	D5	D1	R6036	F3	B3
CR1059	D5	D1	R6060	F3	D2
CR6036	B3	B3	R7011	A2	A3
CR6038	B3	B3	R7015	A2	A3
CR6039	C3	B3	R7016	A2	A3
CR7012	B2	A3	R7021	A2	A3
CR7025	B2	B3	R7022	A2	A3
CR7026	B2	B3	R7060	F3	D3
CR7027	B2	B3			
CR7028	B2	B3	U1040	C5	C1
CR7051	C3	C3	U7030D	A3	B3
			U7030	B2	B3
J1010	F1	D1	U7040A	C3	C3
J1010	A3	D1	U7050A	C3	C3
J1010	F5	D1	U7050B	D2	C3
J6020	A3	A2	U7050E	C3	C3
J6020	A4	A2	U7050	B4	C3
J7020	F4	A2			
			VR1061	C5	D1
P1015	F2	B3			

Partial A1 also shown on diagram 1A.



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P/O A01 UPPER BOARD

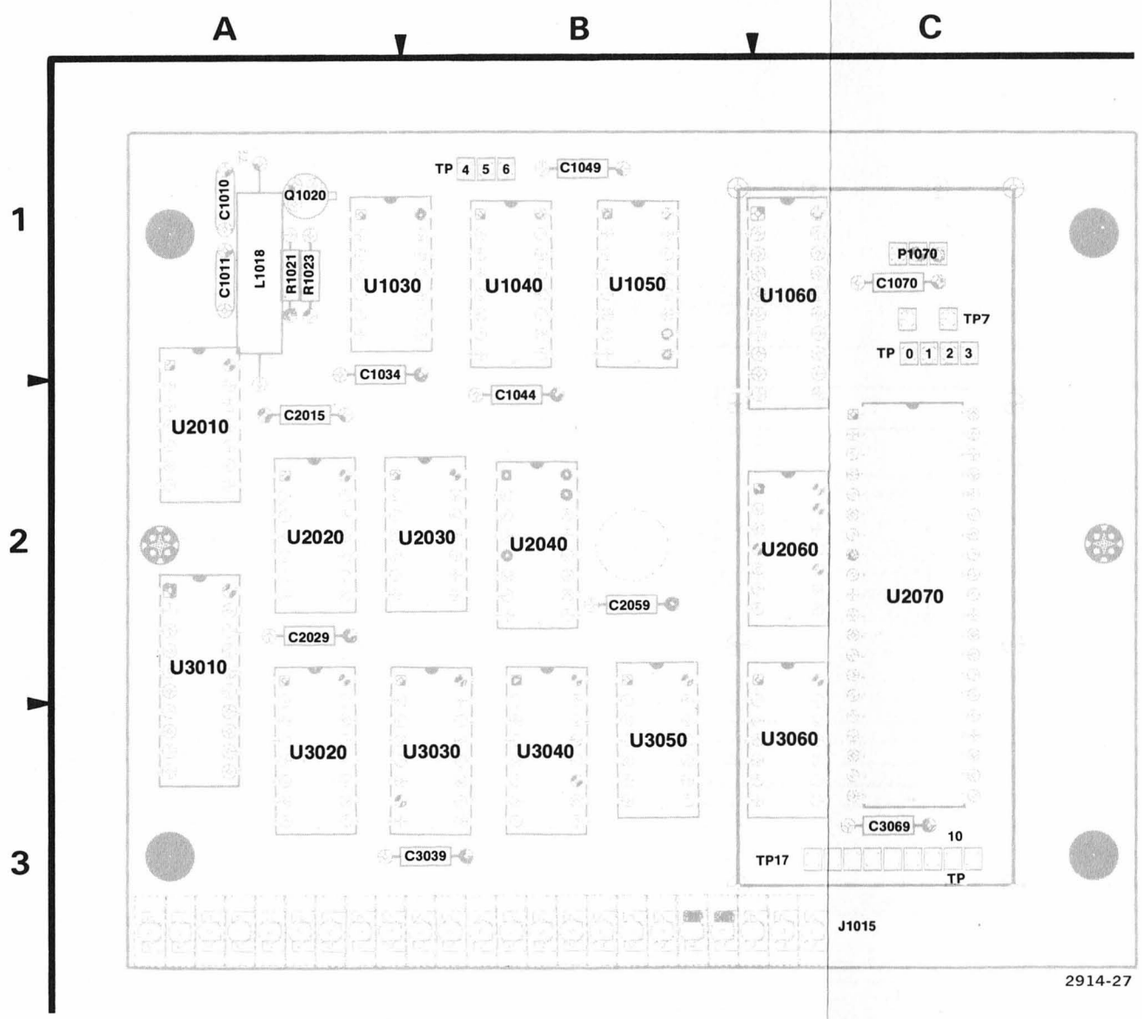
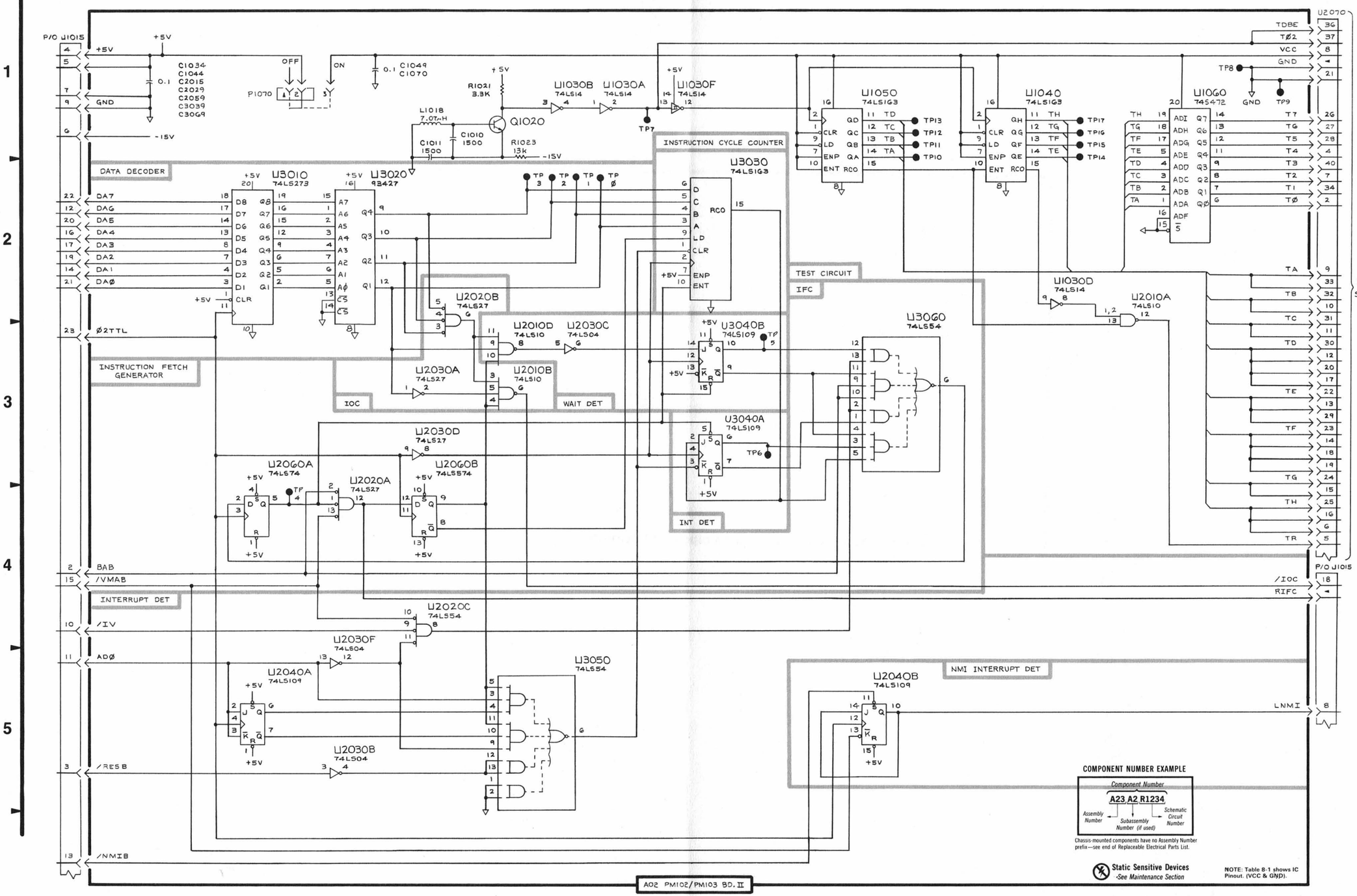


Figure 8-2. A2 Lower Board Component Locations.

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1010	B1	A1	TP11	E1	C3
C1010	B1	A1	TP12	E1	C3
C1011	B1	A1	TP13	E1	C3
C1011	B1	A1	TP14	E1	C3
C1034	A1	A1	TP15	E1	C3
C1044	A1	B2	TP16	E1	C3
C1049	B1	B1	TP17	E1	C3
C1049	B1	B1			
C1070	B1	C1	U1030A	C1	A1
C1070	B1	C1	U1030B	C1	A1
C2015	A1	A2	U1030D	E2	A1
C2029	A1	A2	U1030F	C1	A1
C2059	A1	B2	U1040	E1	B1
C3039	A1	B3	U1050	D1	B1
C3069	A1	C3	U1060	F1	C1
			U2010A	F2	A2
L1018	B1	A1	U2010B	C3	A2
L1018	B1	A1	U2010D	C3	A2
			U2020A	B4	A2
P1015	F4	A3	U2020B	B2	A2
P1015	A1	A3	U2020C	B4	A2
P1070	B1	C1	U2030A	B3	B2
P1070	B1	C1	U2030B	B5	B2
			U2030C	C3	B2
Q1020	C1	A1	U2030D	B3	B2
			U2030F	B5	B2
R1021	C1	A1	U2040A	A5	B2
R1023	C2	A1	U2040B	D5	B2
			U2060A	A4	C2
TP	C2	C1	U2060A	B4	C2
TP1	C2	C1	U2060B	B4	C2
TP2	C2	C1	U2070	F1	C2
TP3	C2	C1	U3010	A2	A2
TP4	B4	B1	U3020	B2	A3
TP5	D3	B1	U3030	D2	B3
TP6	D3	B1	U3040A	D3	B3
TP7	C1	C1	U3040B	D3	B3
TP8	F1	C1	U3050	C5	B3
TP9	F1	C3	U3060	D3	C3
TP10	E1	C3			



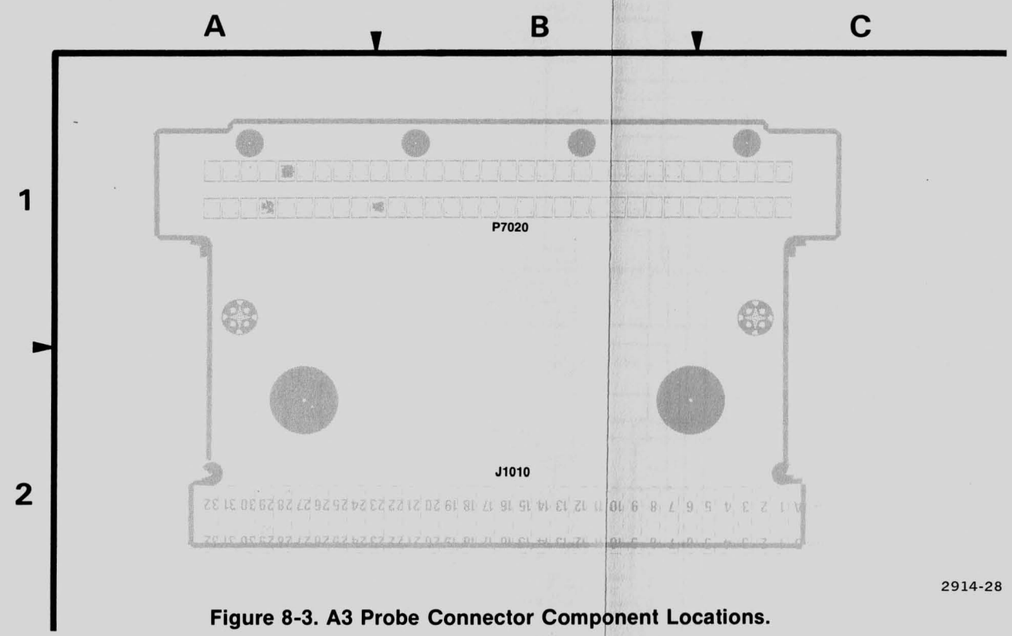


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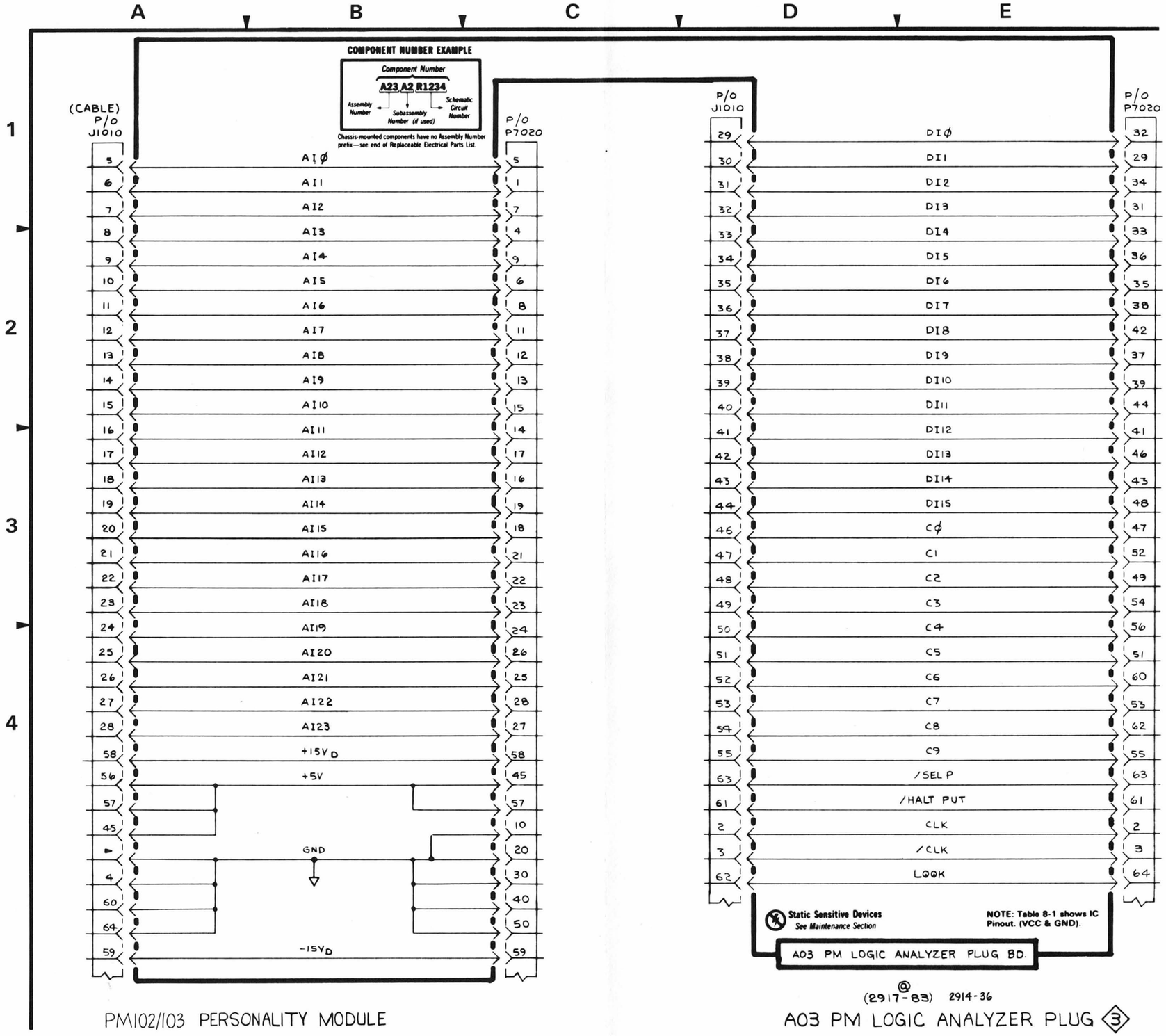
Figure 8-3. A3 Probe Connector Component Locations.

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1010	A1,C1	B2
J7020	B1,E1	B1



PM102/103 PERSONALITY MODULE

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A03 PM LOGIC ANALYZER PLUG ◇3◇

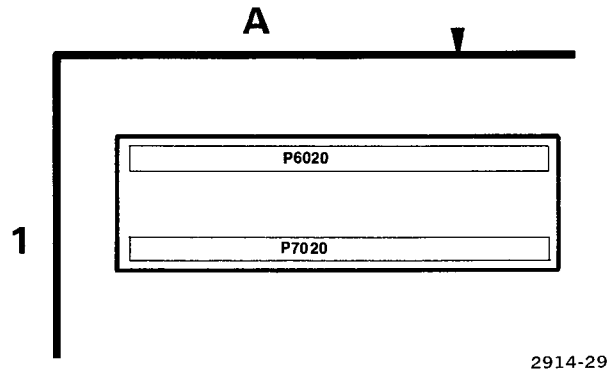
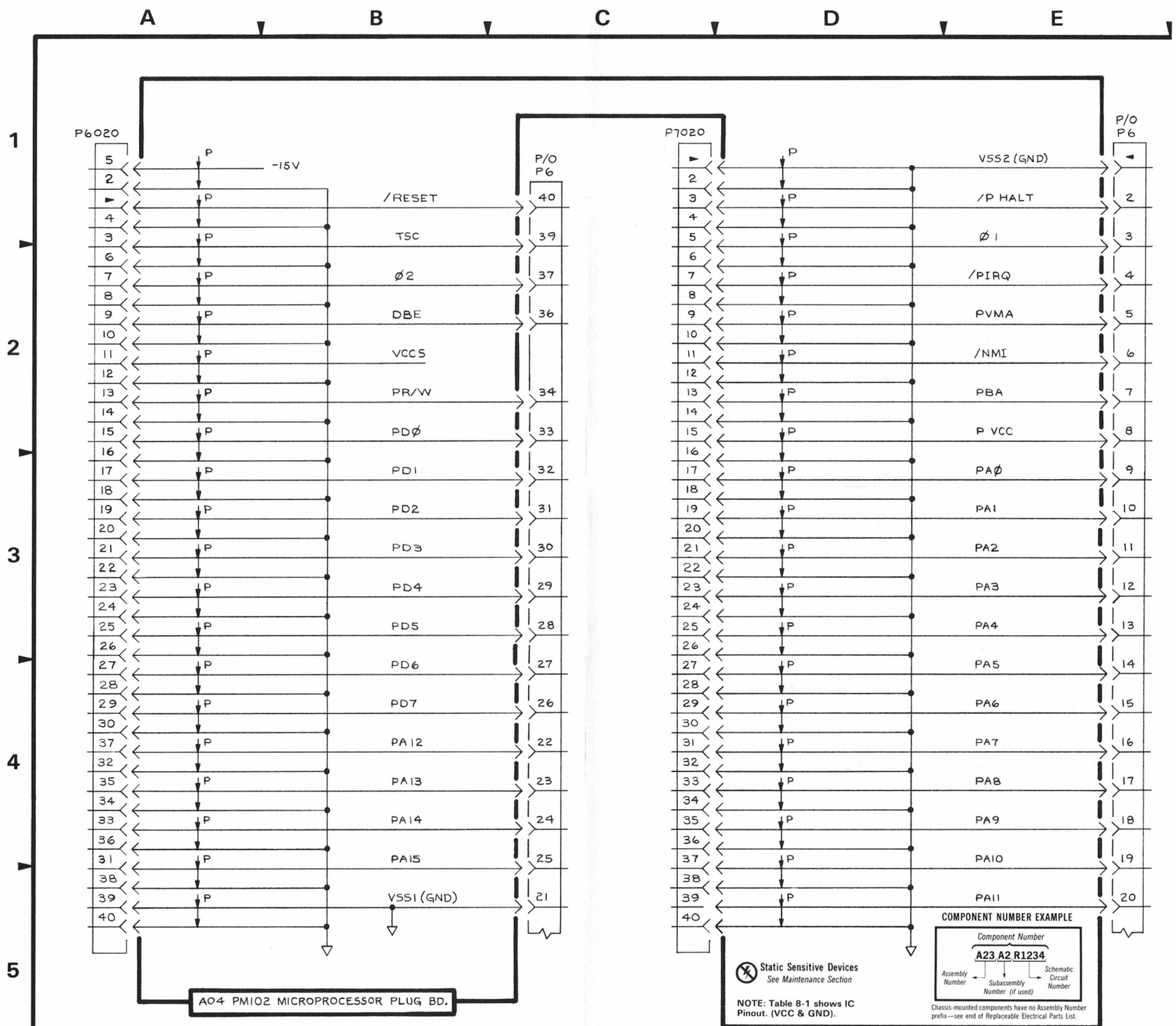


Figure 8-4. A4 PM102 Probe Board Component Locations.

ASSEMBLY A4

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P6020	A1	A1
P7020	C1	A1



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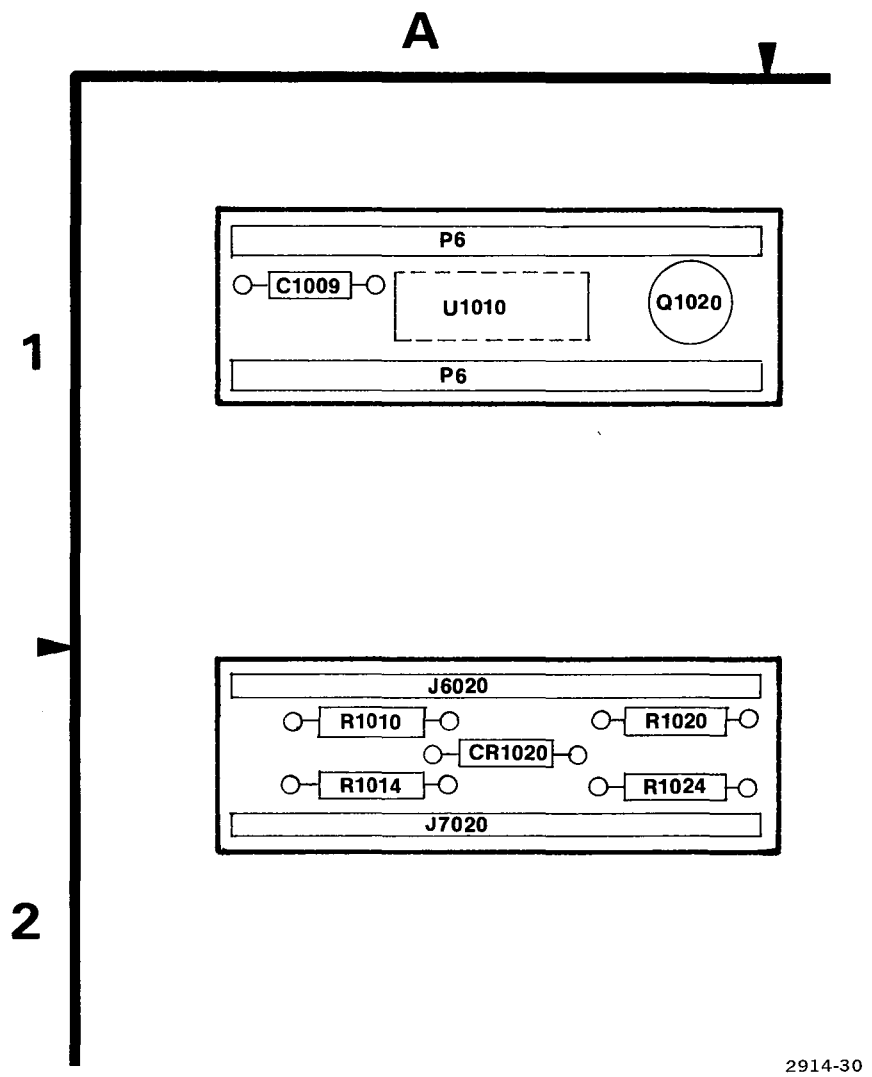
A04 PM102 MICROPROCESSOR PLUG 4

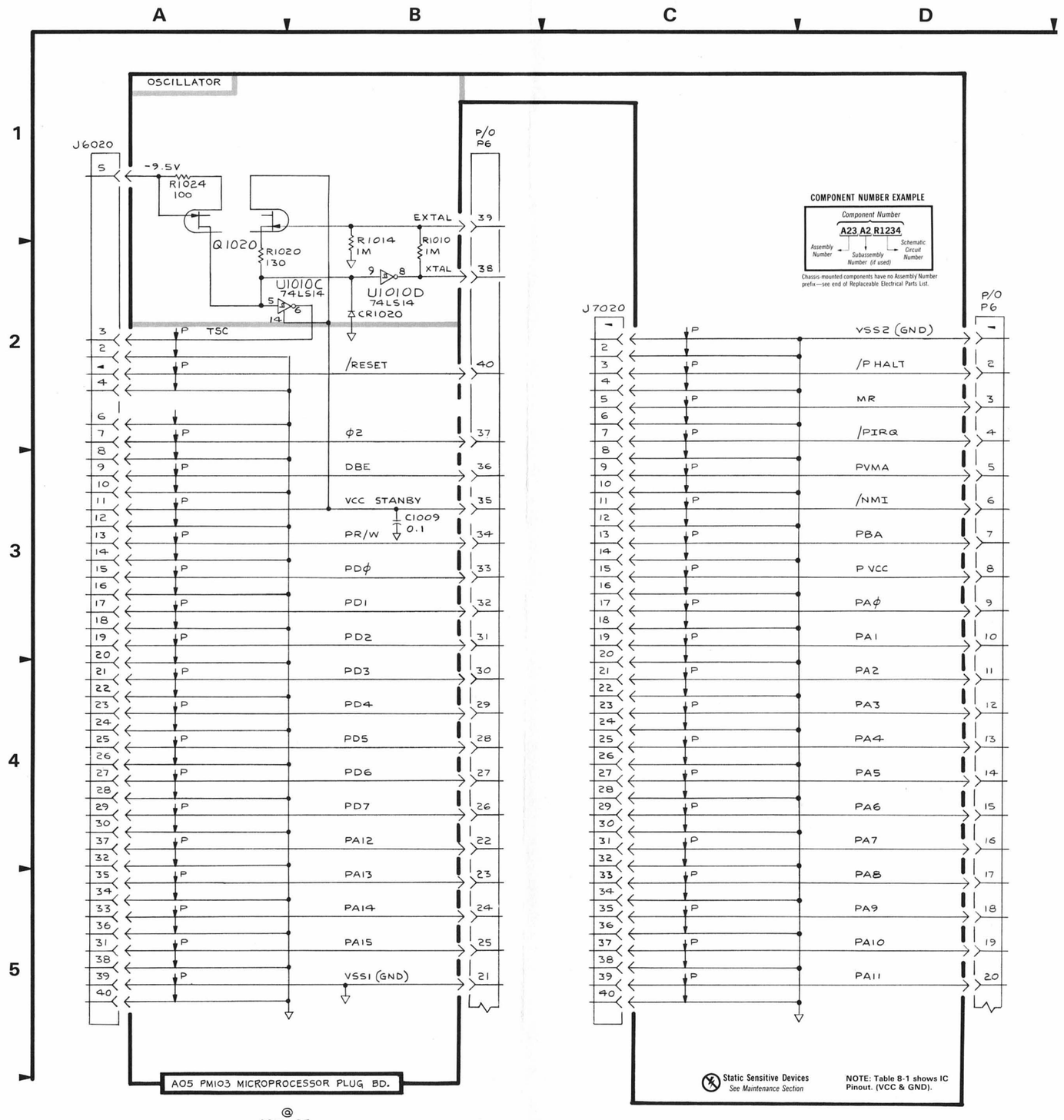


A5 PM103 PROBE BOARD

Figure 8-5. A5 PM103 Component Locations.

ASSEMBLY A5

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1009	B3	A1
CR1020	B2	A2
J6020	A1	A2
J7020	C1	A2
P6	B1,E1	A1
Q1020	A1	A1
R1010	B1	A2
R1014	A1	A2
R1020	A1	A2
R1024	A1	A2
U1010	A2	A1



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A05 PM103 MICROPROCESSOR PLUG 5

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

```
1 2 3 4 5                    Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
                - - - * - - -
   Detail Part of Assembly and/or Component
   Attaching parts for Detail Part
                - - - * - - -
      Parts of Detail Part
      Attaching parts for Parts of Detail Part
                - - - * - - -
```

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000AH	STANDARD PRESSED STEEL CO., UNBRAKO DIV.	8535 DICE ROAD	SANTA FE SPRINGS, CA 90670
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
19613	TEXTOOL PRODUCTS, INC.	1410 W PIONEER DRIVE	IRVING, TX 75061
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
23880	STANFORD APPLIED ENGINEERING, INC.	340 MARTIN AVE.	SANTA CLARA, CA 95050
71785	TRW, CINCH CONNECTORS	1501 MORSE AVENUE	ELK GROVE VILLAGE, IL 60007
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	334-3724-00			1		PLATE,IDENT:MKD 6800 MICROPROCESSOR	80009	334-3734-00
	----- -----			-		(PM102 ONLY)		
	334-3725-00			1		PLATE,IDENT:MKD 6802 MICROPROCESSOR	80009	334-3725-00
	----- -----			-		(PM103 ONLY)		
-2	380-0593-00			1		HSG HALF,CKT BD:TOP	80009	380-0593-00
						(ATTACHING PARTS)		
-3	211-0093-00			4		SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
						- - - * - - -		
-4	380-0594-00			1		HSG HALF,CKT BD:BOTTOM	80009	380-0594-00
						(ATTACHING PARTS)		
-5	211-0093-00			4		SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
-6	210-0586-00			4		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
-7	343-0836-00			4		CLAMP,CABLE:3,72 L,ALUMINUM	80009	343-0836-00
-8	200-2415-00			1		DOOR,ACCESS:PLASTIC	80009	200-2415-00
	175-2678-00			1		CA ASSY,SP,ELEC:40,28 AWG,15.0 L	80009	175-2678-00
	----- -----			-		(PM102 ONLY)		
	175-2679-00			1		CA ASSY,SP,ELEC:40,28 AWG,15.0 L	80009	175-2679-00
	----- -----			-		(PM103 ONLY)		
	200-2445-00			1		. COVER,PROBE:PIN PROTECTOR,PLASTIC	80009	200-2445-00
-9	386-3814-00			1		. PLATE,CONN BODY:	80009	386-3814-00
-10	352-0536-00			1		. HOLDER,CONTACT:40 PIN,NYLON	80009	352-0536-00
						(ATTACHING PARTS)		
-11	211-0102-00			2		. SCREW,MACHINE:4-40 X 0.500",FLH,STL	83385	OBD
						- - - * - - -		
-12	334-3754-00			1		. MARKER,IDENT:	80009	334-3754-00
-13	334-3753-00			1		. MARKER,IDENT:	80009	334-3753-00
-14	----- -----			1		. CKT BOARD ASSY:6800 PROBE(SEE A4,A5 REPL)		
-15	131-2093-00			2		. . SKT,PL-IN ELEK:MICROCKT,20 CONT,LOW PF	23880	CSA-3200-208
-16	136-0252-01			6		. . CONTACT,ELEC:0.178 INCH LONG	00779	1-332095-2
	----- -----			-		. . (PM103 ONLY)		
-17	136-0252-07			14		. . SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
	----- -----			-		. . (PM103 ONLY)		
-18	200-2429-00			1		. . CABLE NIP,ELEC:0.69 L X 3.6 W	80009	200-2429-00
	131-2443-00			1		CONN,RCPT,ELEC:CABLE,32/64 MALE	80009	131-2443-00
-19	334-3722-00			1		. PLATE,IDENT:MKD P6460 MICROPROCESSOR	80009	334-3722-00
-20	380-0591-00			1		. HSG HALF,CKT BD:TOP	80009	380-0591-00
						(ATTACHING PARTS)		
-21	211-0225-00			2		. SCR,CAP,SOC HD:4-40 X 0.312 INCH,STL	000AH	OBD
-22	211-0093-00			2		. SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
-23	210-0551-00			4		. NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	83385	OBD
						- - - * - - -		
-24	380-0590-00			1		. HSG HALF,CKT BD:BOTTOM	80009	380-0590-00
-25	343-0836-00			2		. CLAMP,CABLE:3.72 L,ALUMINUM	80009	343-0836-00
-26	200-2412-00			2		. CABLE NIP,ELEC:3.45 L X 0.05 ID	80009	200-2412-00
-27	175-2683-00			1		. CA ASSY,SP,ELEC:64,28 AWG,48.0 L	80009	175-2683-00
-28	----- -----			1		. CKT BOARD ASSY:PROBE CONNECTOR(SEE A3 REPL)		
-29	131-0608-00			64		. . TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-30	361-0998-00			4		SPACER,CKT BD:0.245 ID X 0.38 OD	80009	361-0998-00
-31	----- -----			1		CKT BOARD ASSY:6800 PROBE #1(SEE A1 REPL)		
-32	131-0590-00			23		. CONTACT,ELEC:0.71 INCH LONG	22526	47351
-33	136-0269-02			1		. SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP,LOW CLE	73803	CS9002-14
-34	136-0537-00			1		. SOCKET,PLUG-IN:40 PIN,W/LOCKING LEVER	19613	240-0333-00-0602
-35	131-0608-00			105		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-36	136-0252-07			10		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-37	131-0787-00			40		. CONTACT,ELEC:0.64 INCH LONG	22526	47359
-38	136-0634-00			9		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-39	136-0578-00			1		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-40	----- -----			1		CKT BOARD ASSY:6800 PROBE #2(SEE A2 REPL)		
-41	136-0263-04			23		. SOCKET,PIN TERM:FOR 0.025 INCH SQUARE PIN	22526	75377-001
-42	136-0634-00			1		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-43	136-0260-02			1		. SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CLE	71785	133-51-92-008
-44	131-0993-00	B010100	B010199	1		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
	----- -----			-		. (PM102 ONLY)		
	131-0993-00	B010200		2		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
	----- -----			-		. (PM102 ONLY)		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-	131-0993-00	B010100	B010379	21		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
	----- -----			-		. (PM103 ONLY)		
	131-0993-00	B010380		22		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
	----- -----			-		. (PM103 ONLY)		
-45	131-0608-00	B010100	B010199	21		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			-		. (PM102 ONLY)		
	131-0608-00	B010200		23		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			-		. (PM102 ONLY)		
	131-0608-00	B010100	B010379	1		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			-		. (PM103 ONLY)		
	131-0608-00	B010380		23		. TERMINAL.PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	----- -----			-		. (PM103 ONLY)		
-46	136-0623-00			1		. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
-47	337-2722-00			1		. SHIELD,ELEC:ACCESS DOOR,BRASS	80009	337-2722-00

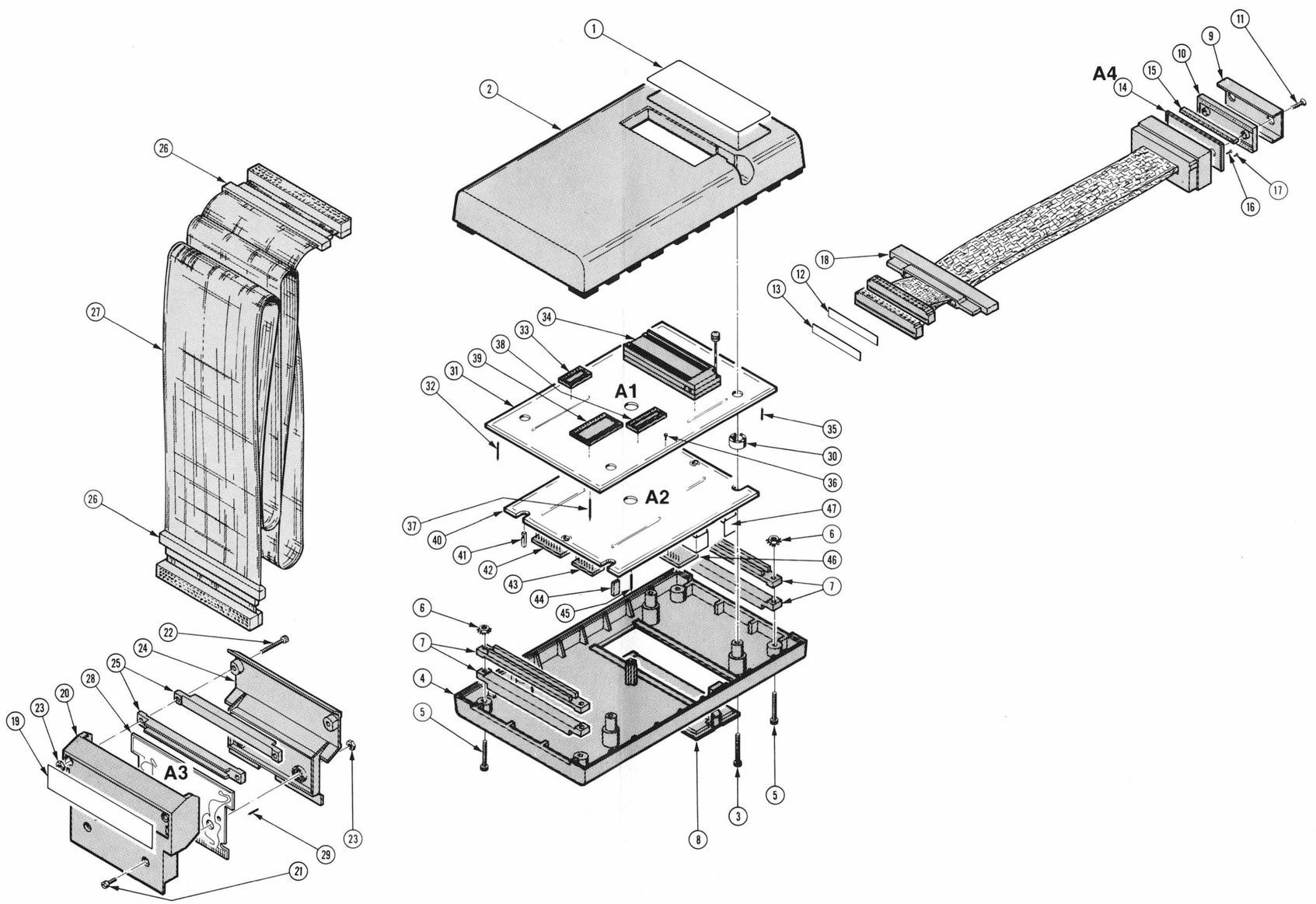

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
	070-2914-00			1		MANUAL,TECH:INSTR,010-6460-01 6800/6802	80009	070-2914-00

SIGNAL GLOSSARY

- AD0—The address line from bit A0 on the S.U.T. address bus to the personality module. The personality module inverts and ANDs this signal with the /IV line to detect interrupt vectors on the S.U.T. address bus. See the /IV line.
- AI0-15—The buffered address lines from the personality module to the logic analyzer.
- BAB—The BA line from the P.U.T., buffered and used by the personality module to detect HALT states and WAI instructions.
- C0—The R/W line from the P.U.T. to the personality module. See PR/W and CI0.
- C1—The /NMI line from the S.U.T. to the personality module. See CI1 and /NMI.
- C2—The /IRQ line from the S.U.T. to the personality module. See CI2 and /PIRQ.
- C4—The BA line from the S.U.T. to the personality module. See PVMA and CI6.
- C7—The /P HALT from the S.U.T. to the personality module. See CI7, /STOP P.U.T., /HALT P.U.T.
- C9—The /RESET line from the S.U.T. to the personality module. See CI9 and /RES B.
- CI0—The buffered R/W line from the personality module to the logic analyzer. See C0 and PR/W.
- CI1—The /LNMI line from the personality module to the logic analyzer. This line goes low whenever the /NMI line on the S.U.T. goes to a low state for 25 ns. It stays low until the first VMA cycle after /NMI goes high. See C1 and /NMI.
- CI2—The buffered /IRQ line from the personality module to the logic analyzer. See C2 and /PIRQ.
- CI3—The personality module-generated IFC (instruction fetch cycle) indicator to the logic analyzer.
- CI4—The buffered BA line from the personality module to the logic analyzer. See PBA and C4.
- CI5—The personality module-generated IOC (illegal op code) indicator to the logic analyzer.
- CI6—The buffered VMA line from the personality module to the logic analyzer. See C6 and PVMA.
- CI7—The /HALT line from the personality module to the logic analyzer. See /STOP P.U.T., /PHALT, and /HALT P.U.T.
- CI9—The buffered /S RESET line from the personality module to the logic analyzer. See C9 and /RES B.
- DI0-7—The buffered data lines from the personality module to the logic analyzer.
- /HALT P.U.T. —The /HALT line from the logic analyzer to the P.U.T. See /STOP P.U.T., C7 and CI7.
- /IOC—The inverted signal from the Illegal Op Code Detector. /IOC is inverted to C5.
- /IV—The /IV line is used to detect interrupt vectors on the S.U.T. address bus. Any signals on AD3-AD15 are NANDed together by A1U4040, producing the /IV signal. The /IV signal is NANDed with the inverted AD0 signal, detecting an FFF9, FFFB, FFFD, or FFFF on the S.U.T. address bus. See AD0.
- LNMI—The non-maskable interrupt signal from the NMI Interrupt Detector, which is inverted to C1.
- LOOK—The signal from the logic analyzer to the personality module that stops the personality module from sending address and data to the logic analyzer.
- /NMI—The non-maskable-interrupt line of the S.U.T.
- /NMIB—The buffered non-maskable-interrupt line that goes to the /NMI Interrupt Detector.
- PD0-7—The data lines from the S.U.T. data bus to the personality module.
- Pin 37—The clock signal from the S.U.T. to the personality module. For a 6800-based S.U.T., the signal name is Φ2.
- /PIRQ—The IRQ line from the S.U.T. to the personality module.
- PVMA—The VMA line from the S.U.T. to the personality module.
- Φ2TTL — The converted clock signal from the ECL to the TTL Converter.
- /RES B—The buffered /RESET line that goes to A2, is inverted, and is then applied to the Interrupt Detector.
- RIFC—The output of the Instruction Fetch Generator.
- /SEL P—The signal from the logic analyzer to the personality module, enabling the logic analyzer to read the contents of the personality module PROM.
- /STOP P.U.T.—The /HALT pin from the personality module to the P.U.T.

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

SERVICE NOTE

Because of the universal parts procurement problem, some electrical parts in your instrument may be different from those described in the Replaceable Electrical Parts List. The parts used will in no way alter or compromise the performance or reliability of this instrument. They are installed when necessary to ensure prompt delivery to the customer. Order replacement parts from the Replaceable Electrical Parts List.

CALIBRATION TEST EQUIPMENT REPLACEMENT

Calibration Test Equipment Chart

This chart compares TM 500 product performance to that of older Tektronix equipment. Only those characteristics where significant specification differences occur, are listed. In some cases the new instrument may not be a total functional replacement. Additional support instrumentation may be needed or a change in calibration procedure may be necessary.

Comparison of Main Characteristics

DM 501 replaces 7D13		
PG 501 replaces 107	PG 501 - Risetime less than 3.5 ns into 50 Ω.	107 - Risetime less than 3.0 ns into 50 Ω.
108	PG 501 - 5 V output pulse; 3.5 ns Risetime	108 - 10 V output pulse 1 ns Risetime
PG 502 replaces 107		
108	PG 502 - 5 V output	108 - 10 V output
111	PG 502 - Risetime less than 1 ns; 10 ns Pretrigger pulse delay	111 - Risetime 0.5 ns; 30 to 250 ns Pretrigger pulse delay
PG 508 replaces 114	Performance of replacement equipment is the same or better than equipment being replaced.	
115		
2101		
PG 506 replaces 106	PG 506 - Positive-going trigger output signal at least 1 V; High Amplitude output, 60 V.	106 - Positive and Negative-going trigger output signal, 50 ns and 1 V; High Amplitude output, 100 V.
067-0502-01	PG 506 - Does not have chopped feature.	0502-01 - Comparator output can be alternately chopped to a reference voltage.
SG 503 replaces 190, 190A, 190B	SG 503 - Amplitude range 5 mV to 5.5 V p-p.	190B - Amplitude range 40 mV to 10 V p-p.
191		
067-0532-01	SG 503 - Frequency range 250 kHz to 250 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
SG 504 replaces 067-0532-01	SG 504 - Frequency range 245 MHz to 1050 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
067-0650-00		
TG 501 replaces 180, 180A	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	180A - Trigger pulses 1, 10, 100 Hz; 1, 10, and 100 kHz. Multiple time-marks can be generated simultaneously.
181		181 - Multiple time-marks
184	TG 501 - Trigger output-slaved to market output from 5 sec through 100 ns. One time-mark can be generated at a time.	184 - Separate trigger pulses of 1 and 0.1 sec; 10, 1, and 0.1 ms; 10 and 1 μs.
2901	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	2901 - Separate trigger pulses, from 5 sec to 0.1 μs. Multiple time-marks can be generated simultaneously.

NOTE: All TM 500 generator outputs are short-proof. All TM 500 plug-in instruments require TM 500-Series Power Module.

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MANUAL CHANGE INFORMATION

Date: 3-11-81 Change Reference: C1/381

Product: PM102/PM103 PERSONALITY MODULE Manual Part No.: 070-2914-00

DESCRIPTION

TEXT ADDITION

Section 2 OPERATING INSTRUCTIONS

p.2-1 Connecting Personality Module to the system under test (S.U.T.)

ADD, following step 3:

NOTE

(6802 Users Only)

Due to future changes in chip specifications, when using an external TTL clock, pin 39 (EXTAL) must be driven by the clock signal and pin 38 (XTAL) left open. The recommended method is to use a 40-pin low-profile socket (P/N 136-0736-00) which has had the lead for pin 38 removed. The 6802 from the S.U.T. is inserted the Zero-Insertion Force socket of the PM103.Then the replacement socket is inserted into the 40-pin low-profile socket and the whole assembly is inserted in the S.U.T.

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MANUAL CHANGE INFORMATION

Date: 8-26-81 Change Reference: C2/881

Product: PM 102/PM 103 Personality Module Manual Part No.: 070-2914-00

DESCRIPTION

TEXT CHANGES

SECTION 5 PERFORMANCE CHECK

Page 5-3 Clock Input Resistance

DELETE:

All five steps