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P7001/IEEE 488 INTERFACE

021-0206-00

INSTRUCTION MANUAL

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INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

LIST OF ILLUSTRATIONS

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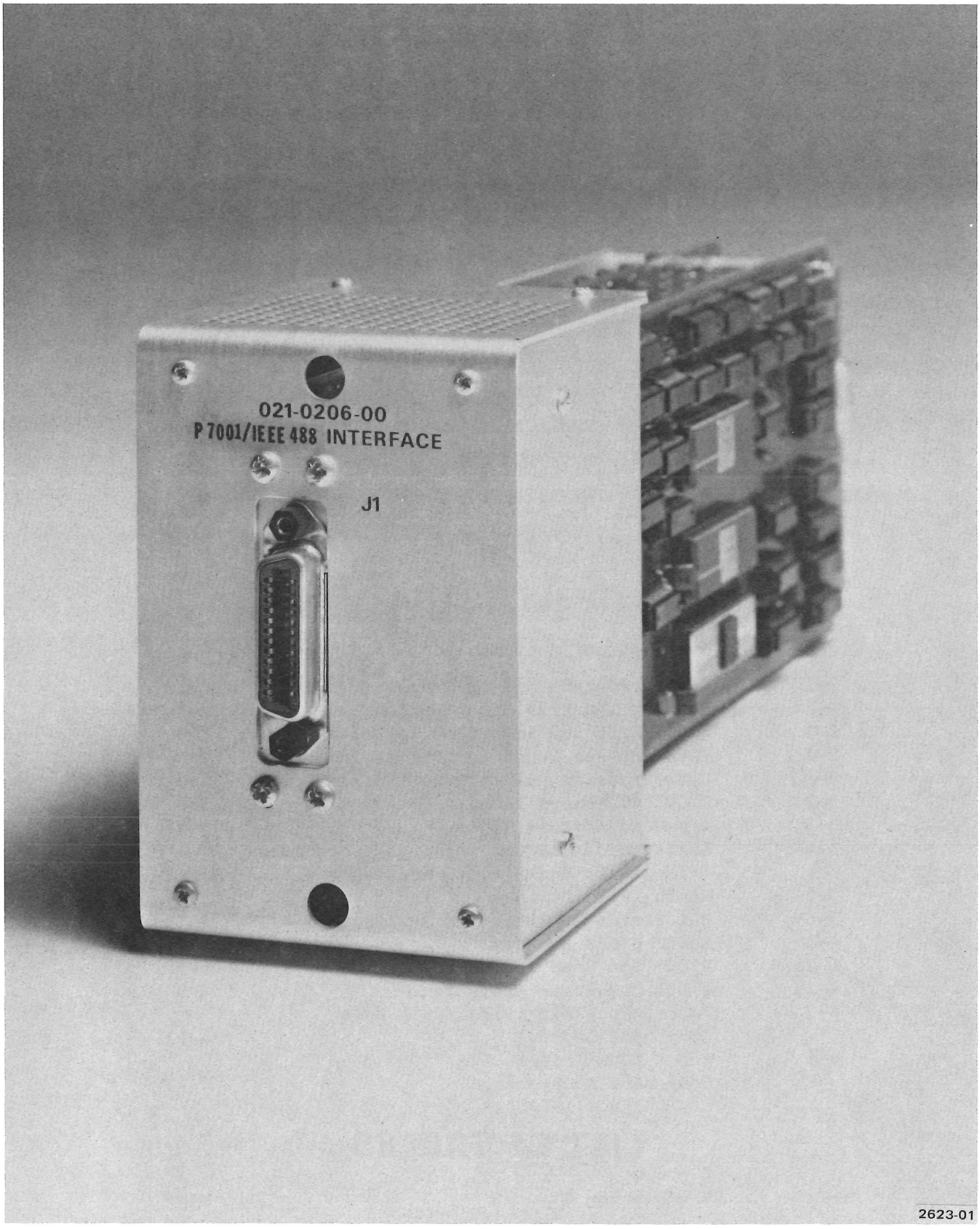


P7001/IEEE 488 INTERFACE @

Section 1
GENERAL INFORMATION

INTRODUCTION

This manual contains both operational and maintenance information for the Tektronix P7001/IEEE 488 Interface, Tektronix Part No. 021-0206-00. This interface is used to interconnect the P7001 Processor section of a Tektronix Digital Processing Oscilloscope (DPO) with any of several Tektronix manufactured devices designed to operate in accordance with IEEE Standard 488-1975, "IEEE Standard Digital Interface for Programmable Instrumentation". The IEEE 488 Bus is commonly known as the General Purpose Interface Bus (GPIB), and may be referred to by that name.

A system configured from IEEE 488 compatible devices is limited to a maximum of 15 devices, and includes a system controller, such as a Tektronix 4051 Graphic System, as well as "talkers" and "listeners". The DPO in such a system functions as both a talker and a listener. As a talker, the DPO sends current status messages, data captured by the Acquisition Unit, and readout information to the system controller or other system listeners. As a listener, it receives commands and data from the system controller or other system devices.

IEEE 488 INTERFACE CAPABILITY

The capabilities of the P7001/IEEE 488 Interface are defined in Table 1-1 by referencing the applicable sections of the IEEE Standard 488-1975 document.

PHYSICAL CHARACTERISTICS

The P7001/IEEE 488 Interface is a dual card assembly designed to be installed into the interface slot of the P7001 Processor section of a DPO. All necessary operating power (+5, -5, +15 and -12VDC) is taken from the P7001 Power Supply via the P7001 Main Interface Board.

Table 1-1 P7001/IEEE 488 Interface Capability

Interface Function	IEEE Std. 488 Section	Interface Capability
Source Handshake *(SH)*	2.3	Complete *(SH1)*
Acceptor Handshake *(AH)*	2.4	Complete *(AH1)*
Talker *(T)*	2.5	No "Talk Only" Mode *(T6)*
Listener *(L)*	2.6	No "Listen Only" Mode *(L4)*
Service Request *(SR)*	2.7	Complete *(SR1)*
Remote-Local *(RL)*	2.8	None *(RLØ)*
Parallel Poll *(PP)*	2.9	None *(PPØ)*
Device Clear *(DC)*	2.10	None *(DCØ)*
Device Trigger *(DT)*	2.11	None *(DTØ)*
Controller *(C)*	2.12	None *(CØ)*

@

Section 2
INSTALLATION

INTRODUCTION

This section of the manual contains operator/user information for the Tektronix P7001/IEEE 488 Interface, used to interconnect the P7001 Processor section of a Tektronix Digital Processing Oscilloscope (DPO) with any IEEE 488 compatible device. Included are instructions for selecting the Device Address and for setting a strap option that facilitates the use of different controllers.

INSTALLATION

The P7001/IEEE 488 Interface assembly may be installed in a P7001 Processor using the instructional steps listed on the Installation Diagram, Figure 2-3. Before the interface is installed, however, the IEEE 488 Bus Device Address and the P123 Strap Option should be set as explained in the following paragraphs.

SELECTING DEVICE ADDRESS

Selecting the Device Address is accomplished by setting the 5-bit DIP switch, SW412 on the MPU/GPIB board (shown in Figure 2-1), to a unique binary number. For devices with talk/listen capabilities, such as the DPO, this number must be between ØØØØØ and Ø111Ø (0 to 14 decimal), inclusive.

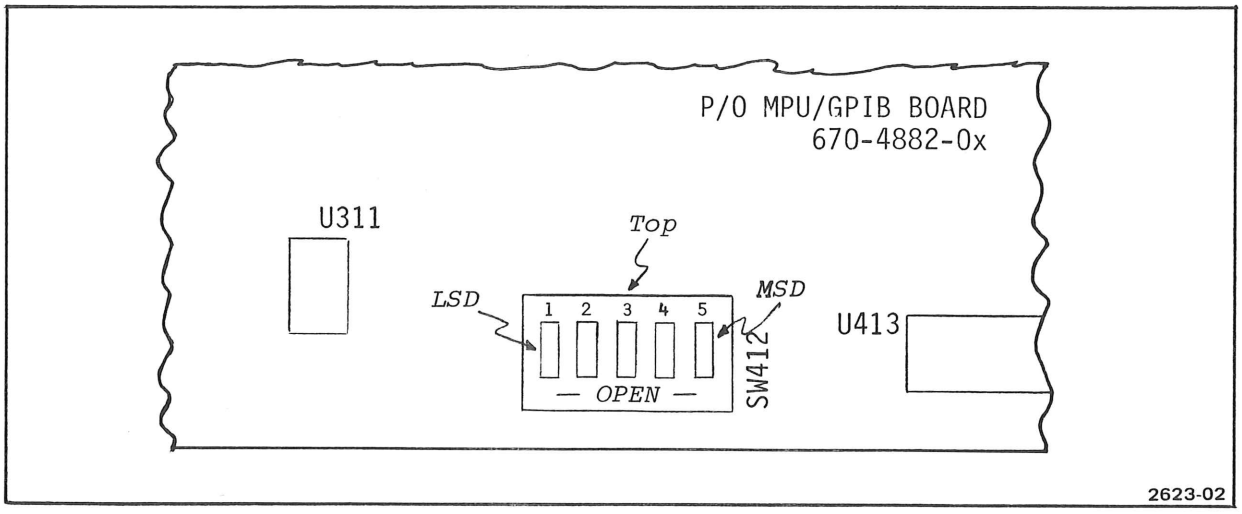


Figure 2-1 Device Address Switch SW412

SELECTING DEVICE ADDRESS (Continued)

Each of the five bits is set to 1 or Ø by five corresponding rocker switches, numbered 1 on the left (Least Significant Digit) to 5 on the right (Most Significant Digit). Note that this is reversed from the order in which the numbers are read. When a rocker switch is pushed in at the top, that bit has been set to a binary 1; e.g., if the first two switches on the left are pushed in at the top and the other three are in at the bottom, the Device Address is set to ØØØ11 (3 decimal).

When the DPO memory location button 'D' is pushed in, the Device Address that has been selected with SW412 will be displayed in the lower right-hand corner of the CRT. Note that when Device Address is elicited, any data previously stored at Channel 7 of memory 'D' (Field Ø) will be destroyed.

SETTING P123 STRAP OPTION

The P123 strap option allows the interface to operate more efficiently with different controllers. A more thorough explanation of use of the strap option may be found in Section 3 of this manual. Figure 2-2 shows connector P123 set for both "Standard" operation (jumper not installed) and "Optional" operation (pin 1 jumpered to adjacent pin - pin 1 is indicated with ►).

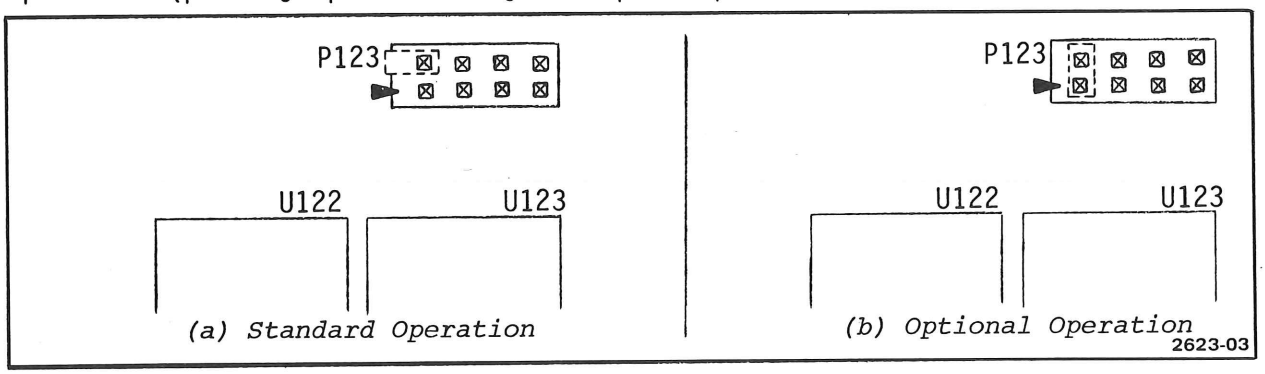
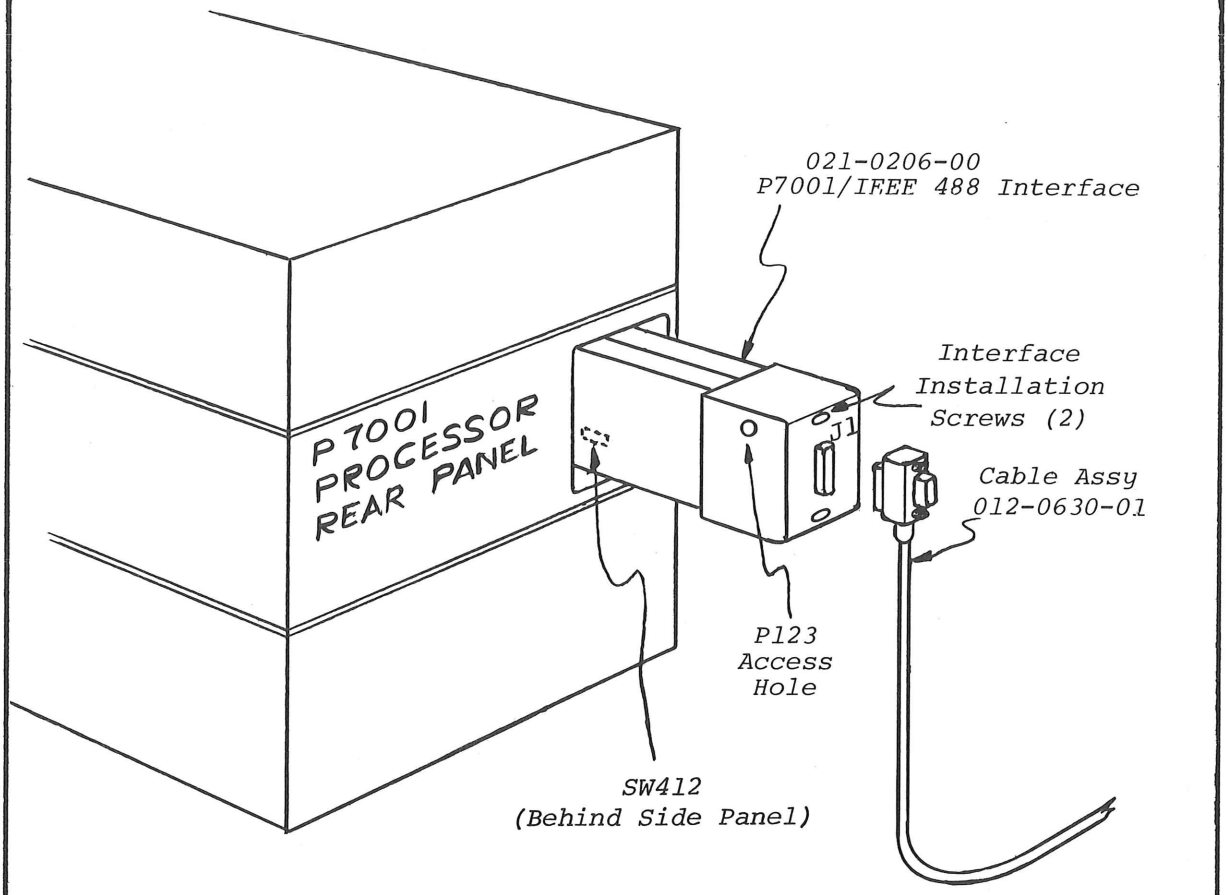


Figure 2-2 Setting the P123 Strap Option

Access to the jumper is gained through a hole in the left rear of the interface housing (see Figure 2-3). To change operating modes, remove the plug from the hole and reach in with longnose pliers to re-position the jumper. To avoid loss when operating in the "Standard" mode, the jumper may be placed on pin 1 or the adjacent pin (above pin 1) with the free end extending to the left. If the DPO was energized while the jumper was re-positioned, it must now be de-energized and a "power-up" sequence performed to activate the change.

@



INSTALLATION/REMOVAL

1. With AC power off, insert the interface into the rear of the P7001 Processor and press in slowly until the assembly is firmly seated.
2. Tighten both interface installation screws.
3. Connect either end of the IEEE 488 bus cable (Tektronix Part No. 012-0630-01) to the interface assembly at J1 and secure with thumbscrews.
4. Prior to removal, set the AC power to OFF and ensure that the interface installation screws and thumbscrews are fully disengaged.

2623-04

Figure 2-3 P7001/IEEE 488 Interface Installation

IEEE 488 BUS CONNECTOR

The IEEE 488 Bus Connector is located at the rear panel of the interface, as shown on Figure 2-3, and is physically attached to the MPU/GPIB Board. This 24-pin female ribbon connector has attached 16 active signal lines and 8 interlaced ground lines, and is used to interconnect the DPO with a system controller or other IEEE 488 compatible device. Figure 2-4 shows the connector pin arrangement and signal line nomenclature.

The interface also includes the mating connector and cable, Tektronix Part No. 012-0630-01 (standard 2 meter IEEE 488 cable). This connector is double-sided, with a male side to mate with the connector on the interface and a female side for connecting additional system components to the bus.

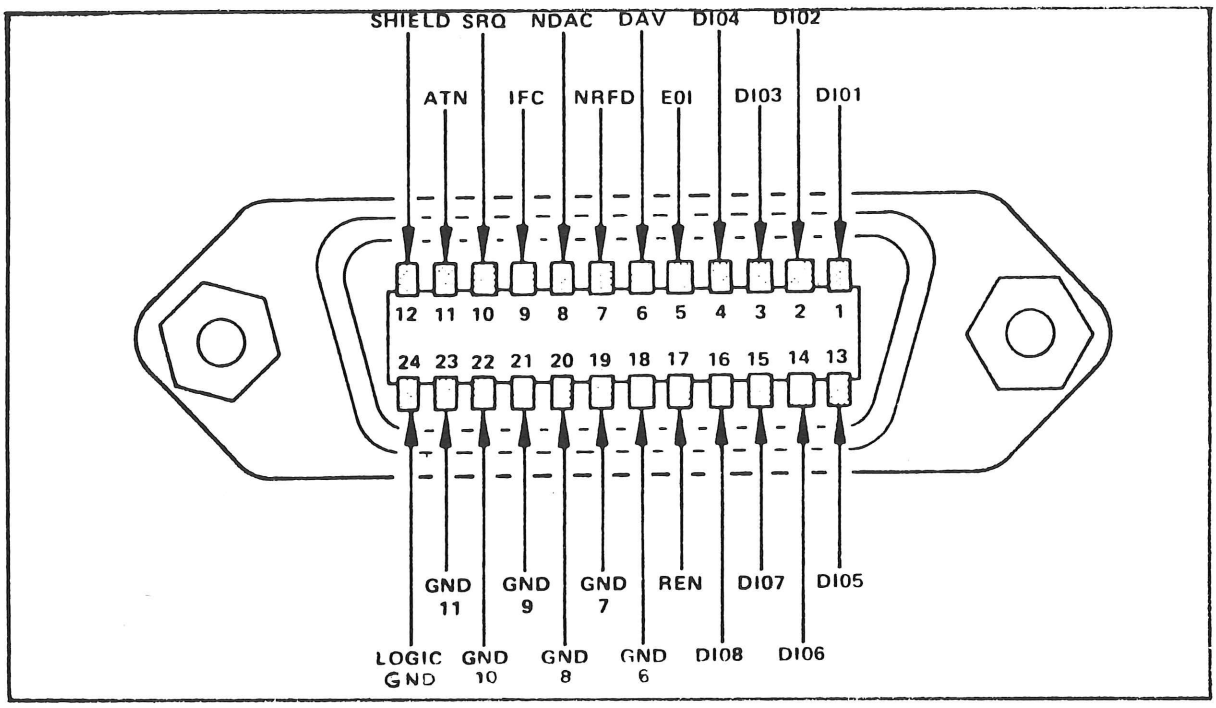


Figure 2-4 IEEE 488 Bus Connector Pin Assignments

Section 3

PROGRAMMING INFORMATION

INTRODUCTION

This section of the manual contains operator/user information both of a general nature and for a specific type of system utilizing the Tektronix 4051 Graphic System as system controller. Included are commands and command formats used to operate the DPO under program control from any IEEE 488 compatible controller. Examples given are in the TEK 4051 BASIC language.

For non-Tektronix controllers, such as the HP-9825 and HP-9830, familiarity with the programming language of the system controller is essential. Regardless of which controller is being utilized, familiarity with the operation of the DPO, or use of the DPO Operators Manual will be useful, as will an understanding of IEEE Standard 488-1975, "IEEE Standard Digital Interface for Programmable Instrumentation".

In addition, for non-Tektronix controllers, the paragraph entitled "Strap Option" in this section of the manual, and the corresponding instructions in Section 2 for setting the strap option, must be read and understood. Additional information on use with the HP-9825 is contained in Appendix II at the rear of this manual.

GENERAL INFORMATION

The P7001/IEEE 488 Interface can be used to interconnect any IEEE 488 compatible device with the P7001 bus of a Tektronix Digital Processing Oscilloscope (DPO). There are three different types of devices on the IEEE 488 bus; "controllers", "talkers", and "listeners". IEEE Standard 488-1975 allows specific listeners and talkers to be selected and de-selected independently. The responsibility of the controller is to designate which system connected instruments are to listen or to talk. The DPO in such a system functions as both a talker and a listener. As a talker, it sends data captured by the DPO (i.e., waveforms), current status messages, and graticule readout information to the bus. As a listener, the DPO receives data (waveforms), commands, and internal memory addresses from the bus.

OPERATING INSTRUCTIONS

Most of the operating instructions included here are specifically for use with a TEK 4051 Graphic System as system controller. Operating instructions for other IEEE 488 controllers may be inferred from a comparison of the instructions included here and those for the controller utilized. An appendix to this manual gives operating examples for the HP-9825 controller.

Power On/Initialization

When a DPO goes through the power-on transition, it automatically generates (through the interface) an interrupt request (SRQ) signal on the IEEE 488 bus. This condition may be cleared and the nature and source of the interrupt determined by programming the controller to take a serial status poll, as shown in a subsequent paragraph entitled "Servicing Interrupts with the TEK 4051".

Power On/Initialization (Continued)

If no interrupt handling instructions are included in the program, or for some other reason the controller does not service the interrupt, the interface must be cleared. This can be accomplished by using the "DCLØ" command explained later in this section.

Status Word

The DPO Status Word is used to indicate to the controller the reason for a DPO interrupt request (SRQ), or may be solicited with a POLL statement. When no SRQ has been generated, the interface will respond with one of the following decimal status words:

Status Word = Ø	Meaning:	Interface idle *(Both cases return decimal*
= 16	:	Interface busy *16 with HP controllers)*

When the DPO issues an interrupt, its interface asserts the SRQ signal line on the IEEE 488 bus. The system controller should be programmed to conduct a status poll in order to release the SRQ. The interface will respond with one of the following decimal status words (the DPO will issue an interrupt request for each of these conditions):

Status Word = 81	Meaning:	DPO powered up.
= 82	:	DPO was hung but has self-corrected.
= 83	:	DPO PROGRAM CALL button pushed.
= 84	:	DPO Single Sweep completed.
= 85	:	HSA aborted (if HSA is installed).
> 1ØØ	:	Error has occurred (see following paragraph entitled "Error Messages").

Error Messages

Four different error conditions may exist for the DPO; each will be indicated to the system controller by an SRQ. A status poll conducted after receipt of the SRQ will result in one of the following decimal status words:

Status Word = 113	Meaning:	Communication Error - the data input is meaningless or impossible to implement. If the data will affect the DPO operation, the error is not a communication error. Examples include parity errors, unintelligible commands, or syntax errors.
= 114	:	Programming Error - intelligible commands have been received which involve out of range parameters. The DPO attempts to carry out the assigned operation but finds it impossible to complete. Examples include overflowing DPO data size, and invalid addressing of the DPO internal memory.
= 115	:	Internal Error - an Interface or P7001 hardware error has occurred. This may mean a permanent hardware malfunction or a transient condition.
= 112	:	Other Error - the DPO has discovered an error which is none of the previously described cases.

Servicing Interrupts with the TEK 4051

When the DPO issues an interrupt service request (SRQ) through the interface, the 4051 is normally programmed to finish executing the current statement, then transfer to an interrupt handling routine, as shown in the following example:

```
1ØØ    ON SRQ THEN 5ØØ
---
---
5ØØ    POLL N,M;4;5;1
51Ø    PRINT N,M
52Ø    GOTO N OF 6ØØ,7ØØ,8ØØ
---
---
8ØØ    IF M=83 THEN 4ØØØ
81Ø    IF M=84 THEN 5ØØØ
82Ø    RETURN
---
---
4ØØØ   (service routine for DPO Front Panel PROGRAM CALL buttons)
----
429Ø   RETURN
5ØØØ   (service routine for DPO Single Sweep)
----
519Ø   RETURN
```

In the foregoing example, line 1ØØ enables the 4051 to respond to an SRQ condition; the program then executes in normal sequential order. When the DPO (or any other peripheral device) signals an SRQ, the 4051 finishes the present statement, then transfers to the POLL statement at line 5ØØ. The POLL statement contains the two numeric variables N and M as parameters followed by device addresses 4;5;1. As the 4051 executes the POLL statement, it first addresses device number 4 to see if it is requesting service. Assuming the DPO has been assigned device address 1, the 4051 will continue to poll devices in the order shown until it reaches device 1. When the 4051 finds that device 1 issued the SRQ, it assigns the number 3 to variable N in the POLL statement, because device 1 is the third device on the list.

The DPO returns a decimal status word (previously explained) which is assigned to the variable M. Line 51Ø causes N and M to be printed on the 4051 screen. Line 52Ø sends the program to N, or the third (8ØØ) line number in the list 6ØØ,7ØØ,8ØØ. In line 8ØØ, if the status word (M) is 83 the program moves to line 4ØØØ, which begins a service routine for the DPO PROGRAM CALL buttons. Line 81Ø performs the same function for status word 84.

If the 4051 does not have the DPO's device address in its program (listed in the POLL statement) when an SRQ is received, processing will halt and the 4051 will "hang" pending further instructions. At this point, the operator should find the line containing the POLL statement and re-enter the statement so that the list of devices to be polled includes the DPO. Subsequent status polls will then recognize the address.

NOTE

This condition will not occur when using the HP-9825 as system controller, because it will time out and resume processing if unable to identify a device.

Servicing Interrupts with the TEK 4051 (Continued)

If the TEK 4051 is being used as system controller but is idle, or does not have interrupt handling instructions in its program, the following error message will be printed on the screen when an SRQ is received:

NO SRQ ON UNIT - MESSAGE NUMBER 43

To clear this condition, the operator should enter the following statement in the immediate mode (no line number):

POLL N,M;(DPO Device Address)

Strap Option

The IEEE 488-1975 standard is a hardware standard. As such, its main purpose is to confirm the electrical characteristics of the interface bus and the handshake procedures, addressable messages, unaddressable messages, and universal messages. It does not specify the delimiters and terminators that pass through the bus together with the data and command information. A strap option is provided to allow the user to set the interface to send or accept different kinds of delimiters and terminators.

Implementation of the strap option is described and illustrated in Section 2 of this manual. The option provides two operating modes, "Standard" operation and "Optional" operation. Standard operation is defined as between the DPO and a Tektronix controller, such as the TEK 4051. Optional operation should be used with Hewlett-Packard controllers, such as the HP-9825, to speed up transfer time, use less core, and ease programming.

Delimiters and terminators used for Standard data transfers are as follows:

Accepts into DPO: delimiters "," or "Ø" or "CR" or "LF" or any combination.

: terminators - any character with EOI asserted.

Sends to controller: delimiter ","

: terminator - the sequence of "CR", then "LF" with EOI asserted.

Delimiters and terminators used for Optional data transfers are as follows:

Accepts into DPO: delimiters - same as for Standard operation.

: terminators - "LF" without EOI asserted, or any character with EOI asserted.

Sends to controller: delimiter and terminator - same as standard operation.

The characters used above and their ASCII decimal equivalents are as follows (the complete ASCII code chart is included as a supplement to this manual):

"," = comma (ASCII 44)
"CR" = CARRIAGE RETURN (ASCII 13)
"LF" = LINE FEED (ASCII 10)
"Ø" = space (ASCII 32)
EOI = End Or Identify (IEEE 488 bus management signal).

Strap Option (Continued)

Use of the delimiters and terminators is illustrated in Figure 3-1, which shows the last four elements of a data (waveform) transfer from the DPO to the controller. The strap option is set for "Standard".

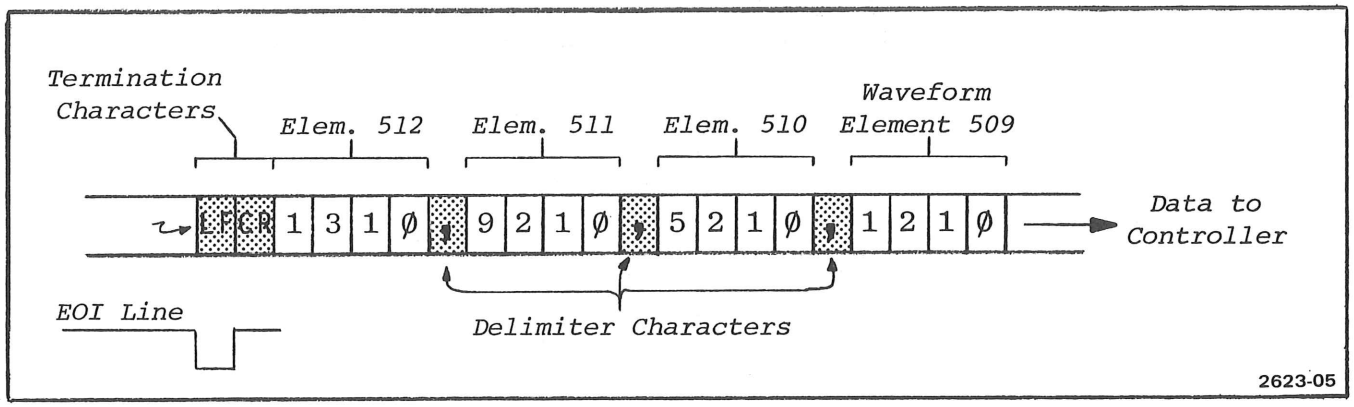


Figure 3-1 Data Transfer Delimiters and Terminators

COMMAND FORMAT

The general command format (the sequence in which commands occur) is as follows: (MTA or MLA)(DAB).

Where: MTA (My Talk Address) and MLA (My Listen Address) are the primary addresses used to command the DPO to transmit data (talk) or receive data (listen), respectively. MTA and MLA are identical to the I/O Address referred to in the TEK 4051 manual, and may collectively be referred to as Hardware Unit Number (HUN) or Device Address. Instructions for setting this address are in Section 2 of this manual.

DAB (Command Data Bytes) consist of three data bytes of ASCII characters followed by either a question mark or a blank space (both also ASCII).

NOTE

The Secondary Address (MSA) described in the IEEE 488-1975 standard is not applicable to this interface.

Depending on the intended operation, commands from the system controller may be received in one of three specific formats, as follows:

Write to DPO - This command format consists of the DPO's Device Address (MLA in this case), then a three character mnemonic from the Setting Commands of Table 3-1 followed by a space, then the data to be sent to the DPO [i.e., (MLA)(DABØ)data].

COMMAND FORMAT (Continued)

Set DPO to be read - This command format consists of the DPO Listen Address, then a three character mnemonic from the Query Commands of Table 3-2 followed by a question mark [i.e., (MLA)(DAB?)]. This command asks the DPO a question that it (the DPO) will not be able to answer until the "Read from DPO" operation is executed.

Read from DPO - This command format consists only of the assignment of the DPO as talker, after which the requested information is sent from the DPO. The terminating characters ("CR", then "LF" with EOI asserted) are generated automatically by the interface. Before a "Read from DPO" operation can be performed, the "Set DPO to be read" operation must be executed.

Table 3-1 Setting Commands

ADR	Address	*Page:* 3-9
CHL	Channel	3-11
CLI	Clear (Front Panel) Interrupt	3-19
DAT	Data	3-10
DCL	Device Clear	3-20
DPA	Waveform A of DPO Memory is selected	3-8
DPB	Waveform B of DPO Memory is selected	3-8
DPC	Waveform C of DPO Memory is selected	3-8
DPD	Waveform D of DPO Memory is selected	3-8
HAV	Hardware Average (if HSA is installed)	3-18
HIS	Histogram (if HSA is installed)	3-18
HOL	Hold	3-17
OCT	Octal	3-16
SCL	Scale Factor	3-13
SSR	Single Sweep Reset	3-17
STO	Store	3-17
TAB	Transfer Waveform A to Waveform B	3-20
TAC	Transfer Waveform A to Waveform C	3-20
TAD	Transfer Waveform A to Waveform D	3-20
TBA	Transfer Waveform B to Waveform A	3-20
TBC	Transfer Waveform B to Waveform C	3-20
TBD	Transfer Waveform B to Waveform D	3-20
TCA	Transfer Waveform C to Waveform A	3-20
TCB	Transfer Waveform C to Waveform B	3-20
TCD	Transfer Waveform C to Waveform D	3-20
TDA	Transfer Waveform D to Waveform A	3-20
TDB	Transfer Waveform D to Waveform B	3-20
TDC	Transfer Waveform D to Waveform C	3-20
WRD	Word	3-10
X-Y	Set DPO to X-Y Display Mode	3-18
Y-T	Set DPO to Y-T Display Mode	3-18

COMMAND DESCRIPTIONS

Commands from the IEEE 488 controller are structured in one of two ways. Setting Commands are used to transfer data to or set the status of the DPO, and are structured as a three-character mnemonic followed by a blank space, enclosed by quotation marks, such as "ADRØ" (the character Ø is used to designate a blank space). The Setting Commands are shown in Table 3-1.

The Query Commands, used to transfer data or status information from the DPO to the controller, consist of a three-character mnemonic followed by a question mark, enclosed by quotation marks. Using the Address command again as an example, this would look like "ADR?". The Query Commands are shown in Table 3-2.

Table 3-2 Query Commands

ADR?	Address	*Page:* 3-9
DAT?	Data	3-10
DPA?	Send Waveform A of DPO memory	3-9
DPB?	Send Waveform B of DPO memory	3-9
DPC?	Send Waveform C of DPO memory	3-9
DPD?	Send Waveform D of DPO memory	3-9
FPI?	Front Panel Interrupt	3-19
OCT?	Octal	3-16
SCL?	Scale Factor	3-11
WRD?	Word	3-11

DATA TRANSFER

The DPO memory contains four waveform locations, designated A, B, C and D, Each waveform is a 512-element array. The data for each element is an integer in the range Ø to 1Ø23 (decimal). Figure 3-2 shows a memory map for a P7001 4K memory. At the top are four blocks labeled A, B, C and D. These blocks represent the four waveform locations in memory as selected from the DPO front panel. Each waveform location has an address range of 512 (decimal). Waveform A, for example, is ØØØ to 511, Waveform B is 512 to 1Ø23, etc.

Data may be transferred to and from the DPO in three different ways, as follows:

1. Use of the DPA, DPB, DPC and DPD commands;
2. Use of the ADR and DAT commands;
3. Use of the ADR and WRD commands.

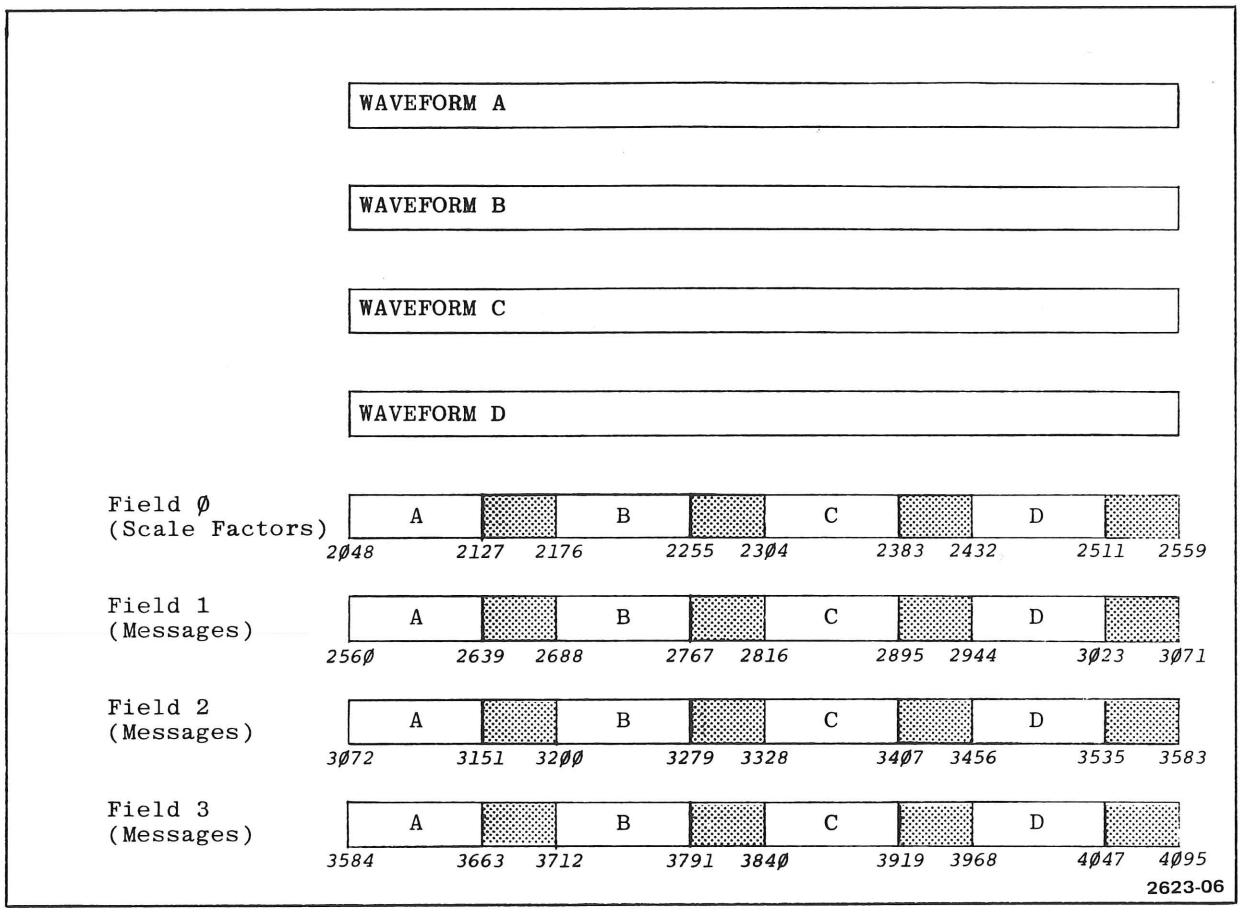


Figure 3-2 P7001 4K Memory Map

DPA, DPB, DPC and DPD Commands

The DPA, DPB, DPC and DPD commands are used to transfer 512 data words, or waveform elements, to or from DPO memory locations A, B, C and D, respectively. Data transfers from the DPO to the controller are normally performed after "Store" and "Hold" operations in the DPO. Store and Hold operations may be performed using the "STOØ" and "HOLØ" commands explained later, or may be executed manually from the DPO Front Panel (see DPO Operators Manual, Tektronix P/N 070-1599-00).

A single blank space after the command mnemonic, such as "DPAØ" or "DPCØ" indicates a data transfer from the TEK 4051 to the DPO. The command is delimited with a semicolon. The following TEK 4051 example shows how a 512-element array, Z, would be transferred from the controller to Waveform location A of a DPO with a Device Address of 1:

```
PRINT @1:"DPA ";Z;
```

Note the use of the delimiter (;) after the Z character. This speeds up data transfer time in the 4051. If it is not used, the 4051 will send up to six spaces between each data word, depending on the number of digits of the data.

DPA, DPB, DPC AND DPD Commands (Continued)

When the command mnemonics DPA, DPB, DPC and DPD are followed by a question mark, such as "DPA?" or "DPC?", the interface is set up to allow data to be transferred from the DPO to the controller or other IEEE 488 bus listener. In the following TEK 4051 example, line 9Ø dimensions B to a 512 element array, line 1ØØ outputs the ASCII characters "DPB?" to the bus and sets up the DPO to output the requested data, and line 11Ø inputs the 512 data words of the Device Address 1 (the DPO), Waveform B, into the 4051.

```
 9Ø    DIM B(512)
1ØØ    PRINT @1:"DPB?"
11Ø    INPUT @1:B
```

ADR Commands

The "ADRØ" (Address) command is used to set up the DPO Address Register residing in the interface. It allows the controller to select each memory cell independently. The addressable DPO memory is from decimal Ø to 8191. (See Figure 3-2, "P7001 4K Memory Map", and Figure 3-3, "DPO Card Address Map"). The following TEK 4051 example shows Device Address 1, the DPO, address 256Ø (the start of Field 1) being selected:

```
PRINT @1:"ADR ";256Ø
```

Note that the argument following the command mnemonic (256Ø in the above example) may also be a numeric variable that is defined elsewhere in the program.

The "ADR?" command is used to set the DPO ready to output the current status of its address register when assigned to talk. In the following TEK 4051 example, line 1ØØ readies the DPO to talk, and line 11Ø assigns the DPO to talk and the controller to listen.

```
1ØØ    PRINT @1:ADR?"
11Ø    INPUT @1:P
```

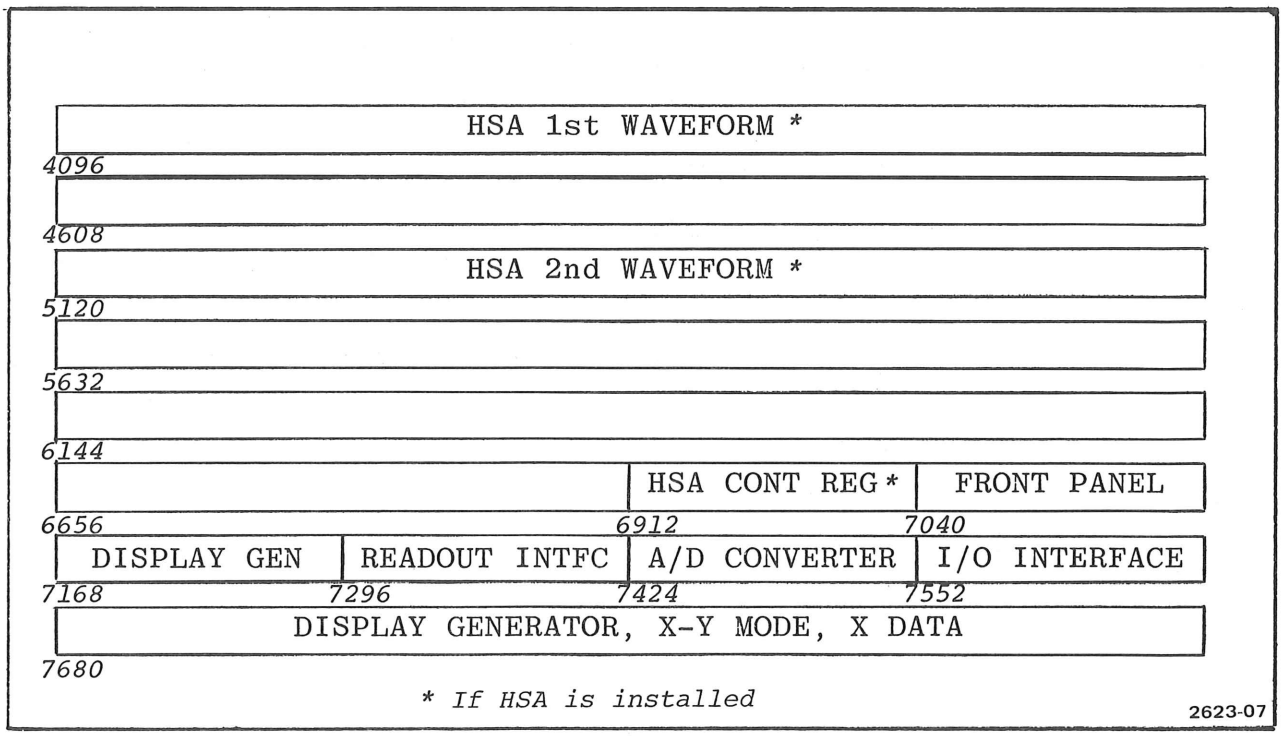


Figure 3-3 DPO Card Address Map

DAT Commands

The DAT (Data) commands allow 512 elements of data to be transferred to or from the DPO, with the beginning address pointed to by the DPO Address Register (set up with the "ADRØ" command). After execution of these commands, the DPO Address Register is advanced by decimal 512.

In the following TEK 4051 example, line 5ØØ dimensions the array Y to 512 elements, line 51Ø defines Y, line 6ØØ sets the Address Register of the DPO to 256, and line 61Ø actually transfers array Y from the 4051 to the DPO (into the second half of Waveform location A and the first half of Waveform location B). After line 61Ø, the DPO Address Register will be at 768.

```
5ØØ    DIM Y(512)
51Ø    LET Y=1ØØ
6ØØ    PRINT @1:"ADR ";256
61Ø    PRINT @1:"DAT ";Y;
```

Note the delimiter (;) after Y in line 61Ø. This is explained after the "DPAØ" command example in a previous paragraph.

In the following TEK 4051 example, line 1ØØ dimensions array X to 512 elements, line 11Ø sets the Address Register of the DPO to 256, or the address of the beginning of the second half of Waveform A (see Figure 3-2), line 12Ø readies the DPO to talk, and line 13Ø transfers the 512 data words from the DPO to the controller. After completion of this sequence, array X is holding the second half of Waveform A and the first half of Waveform B.

```
1ØØ    DIM X(512)
11Ø    PRINT @1:"ADR ";256
12Ø    PRINT @1:"DAT?"
13Ø    INPUT @1:X
```

WRD Commands

The WRD (word) commands allow the 10 bits of a DPO data word to be transferred to or from the DPO (in decimal form). The "ADRØ" command is used to set up the DPO Address Register. After execution of either of the WRD commands, the Address Register is automatically incremented by 1. These commands can be used to transfer an array of n elements to or from the DPO, where n is defined by the controller.

In the following TEK 4051 example, the array Y is first dimensioned to 1Ø24 elements in line 5ØØ, Y is defined in line 51Ø, then line 52Ø sets the Address Register of the DPO to 512, or the beginning of Waveform B. Lines 53Ø and 55Ø perform the FOR LOOP function of the 4051, and line 54Ø transfers the 1Ø24-element array, one word at a time, to DPO memory (Waveforms B and C).

```
5ØØ    DIM Y(1Ø24)
51Ø    LET Y=5ØØ
52Ø    PRINT @1:"ADR ";512
53Ø    FOR N=1 to 1Ø24
54Ø    PRINT @1:"WRD ";Y(N)
55Ø    NEXT N
```


@

WRD Commands (Continued)

In the following TEK 4051 example, an array (L) is dimensioned to 128 elements in line 1ØØ (note - a standard DPO waveform array is 512 elements, therefore this is only the first quarter of a whole waveform). In line 11Ø, the beginning of DPO Waveform B is selected as the starting address. Line 13Ø sets up the DPO to output the data, line 14Ø reads the first data word of Waveform B into the controller array L, and line 15Ø (together with line 12Ø) performs the FOR LOOP function.

```
1ØØ    DIM L(128)
11Ø    PRINT @1:"ADR ";512
12Ø    FOR I=1 to 128
13Ø    PRINT @1:"WRD?"
14Ø    INPUT @1:L(I)
15Ø    NEXT I
```

Scale Factor and Message Transfers

Below the waveform blocks in Figure 3-2 are four additional blocks designated Field Ø, Field 1, Field 2 and Field 3. These represent the four fields of data or messages that can be stored in DPO memory and displayed on the DPO's CRT or read into the controller. The default mode of display is Field Ø. Field Ø is the only field that can display scale factors for the plug-ins directly, and is the field in which the scale factor information is stored when a waveform is stored through the use of the Front Panel buttons. Fields 1, 2 and 3 are used mainly for displaying messages.

Each field has four designated areas for Waveforms A, B, C and D, as shown on Figure 3-2. Also shown are the addresses for each of the waveforms in the four fields (e.g., waveform C of field 2 uses addresses 3328-3407).

Each waveform in a Field has 80 displayable positions. These 80 positions are grouped in 8 channels, each with 10 displayable characters. This is illustrated in Figure 3-4, "Location of Readout Words & Characters (Timeslots) and Field Ø Addresses". Figure 3-4 shows the 8 channels (plug-in readout word positions) and corresponding addresses for Field Ø. The channels are shown as they appear on the CRT, numbered from left to right across the top (CH. Ø-3) then left to right across the bottom (CH. 4-7). Also shown are the ten characters (timeslots) for each channel.

Reading Scale Factors

Scale factors from Field Ø may be read into the controller using the "CHLØ" command, which selects the waveform and channel of a scale factor transfer, followed by the "SCL?" command. In the following TEK 4051 example, line 1ØØ selects Waveform B, Channel 3 of the DPO. Line 11Ø sets up the DPO to output the selected scale factors when assigned to talk, and line 12Ø assigns the DPO to be a talker, thus reading the selected scale factor information (Y$) into the controller.

```
1ØØ    PRINT @1:"CHL ";"B3"
11Ø    PRINT @1:"SCL?"
12Ø    INPUT @1:Y$
```

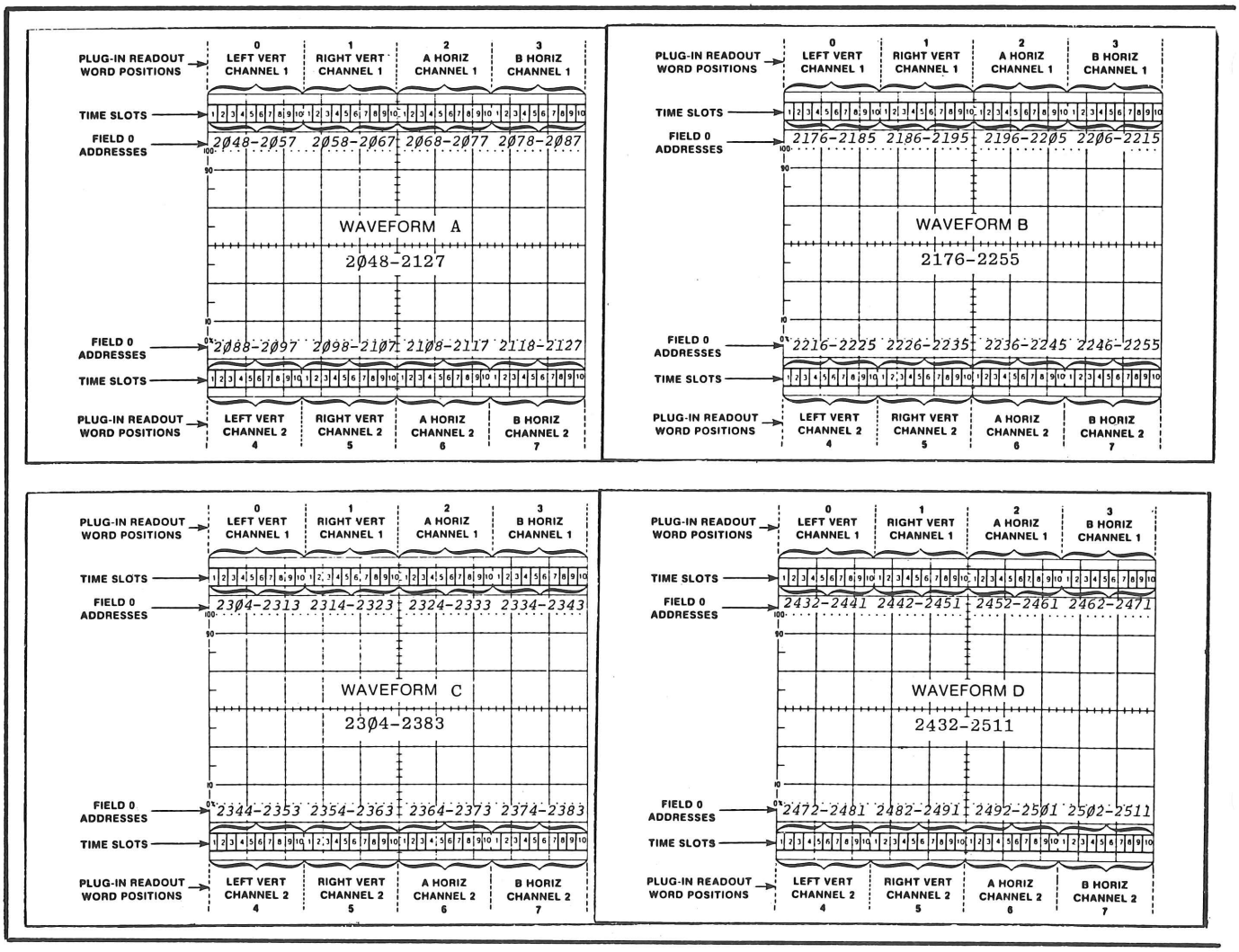


Figure 3-4 Location of Readout Words and Characters (Timeslots) and Field Ø Addresses

Reading Scale Factors (Continued)

Reading scale factors or messages that overlap channels requires a more complex program, such as the following TEK 4051 example:

```
10Ø    LET B$=""
11Ø    PRINT @1:"ADR ";2432
12Ø    FOR I=1 to 4Ø
13Ø    PRINT @1:"WRD?"
14Ø    INPUT @1:A
15Ø    LET A$=CHR(A)
16Ø    LET B$=B$ & A$
17Ø    NEXT I
18Ø    PRINT B$
```


@

Reading Scale Factors (Continued)

In the foregoing example, line 1ØØ initializes B$, line 11Ø selects Field Ø, Waveform D of the DPO, line 12Ø sets up the FOR LOOP function to read in 40 characters, lines 13Ø and 14Ø read in one data word, then the DPO is auto-incremented by 1. Line 15Ø stores the ASCII character having the decimal number A in string variable A$. Line 16Ø concatenates these characters in B$. Line 18Ø prints out the actual readout ASCII character string.

Displaying Messages

Messages can be displayed on the screen (CRT) of the DPO using the "SCLØ" command. The scale factors may be accidentally overwritten by not selecting a field of display (since Field Ø is the default condition). Messages may be written into Fields 1, 2 or 3 for display by using a special command, "OCTØ" (explained later), to set up the Readout Interface Register in the DPO. In the following TEK 4051 example, line 1ØØ selects Field 2, Waveform D of the DPO, line 11Ø writes the message to the designated area (up to 80 characters may be displayed at a time), and line 12Ø selects the Readout Interface Register in the DPO. Addressing the Readout Interface Register and other DPO Registers is explained in greater detail in subsequent paragraphs. Line 13Ø sets up the Readout Interface to display the message residing at Field 2, Waveform D.

```
1ØØ    PRINT @1:"ADR ";3456
11Ø    PRINT @1:"SCL ";"TEKTRONIX STILL MAKES THE BEST OSCILLOSCOPES"
12Ø    PRINT @1:"ADR ";7296
13Ø    PRINT @1:"OCT ";"Ø4Ø1ØØ"
```

NOTE

This command does not set other registers (A/D Converter, Display Generator, Front Panel) to display Waveform D. Only the CRT readout displays the Field 2, Waveform D information. Therefore, the data previously stored at Waveforms A, B, C and D is not affected.

DPO Readout Characters

The set of characters that may be displayed on the DPO CRT (scale factor readout and message information) includes a portion of the 96-character ASCII Code set (the complete ASCII Code set is included as an appendix to this manual) plus some characters unique to the DPO readout. The characters available for display are: digits 0 through 9; all 26 upper case letters (upper case letter O shares the same character with digit 0); lower case letters c, d, m, n and p; space; and characters <, >, ↓, Ω, μ, Δ, /, +, -, and . (decimal point). All of these except ↓, Ω, μ and Δ are standard ASCII characters.

The four unique readout characters (↓, Ω, Δ and μ) are transferred (in either direction) as the following ASCII character:

Readout Character	ASCII
↓	!
Ω	@
Δ	=
μ	u

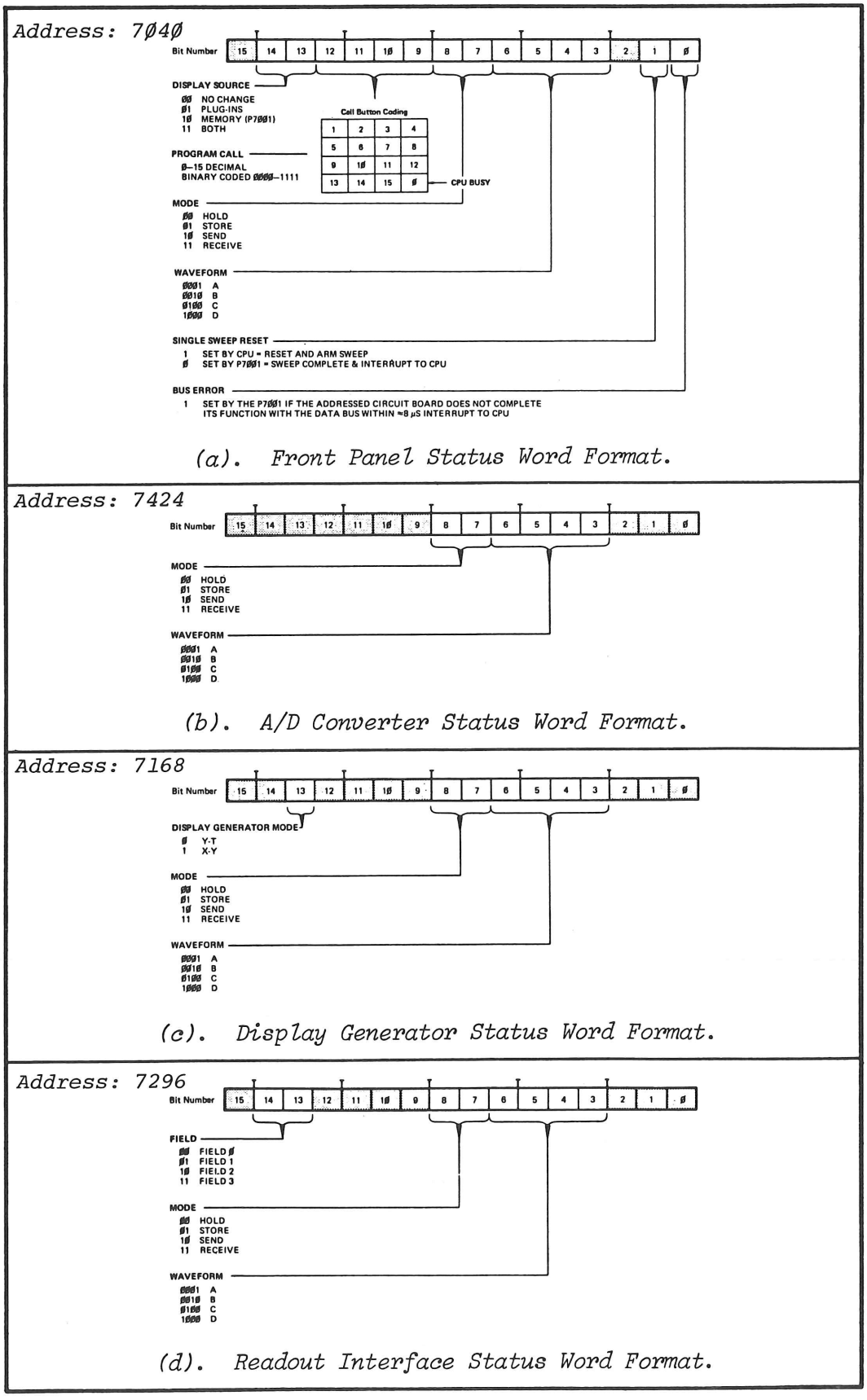


Figure 3-5 Status Word Formats

@

Controlling the DPO

There are four (five if the HSA is installed) registers which can be programmed to control the P7001 Processor of the DPO. These are: A/D Converter, residing at decimal address 7424; Readout Interface, 7296; Display Generator, 7168; Front Panel, 7Ø4Ø; and Hardware Signal Averager (if installed), 6912. Further information on the registers involved in controlling the DPO may be found in the P7001 Processor Manual (Tektronix Part No. 070-1882-00), the P7001 A/D Converter Manual (070-1809-00), the P7001 Sample & Hold Manual (070-1810-00), the P7001 Readout Interface Manual (070-1609-00), the P7001 Display Generator Manual (070-1608-00), the P7001 Front Panel/Z-Axis Manual (070-1610-00), and the Hardware Signal Averager Manual (061-1344-00).

Status word format for the A/D Converter, Readout Interface, Display Generator and Front Panel Registers is illustrated in Figure 3-5. Figure 3-6 shows the HSA status word.

In most cases, the user does not have to learn to operate and set up these registers because the microprocessor residing in the interface takes over most of the operating procedures. However, there are some operations where it is necessary or desirable to control these registers bit by bit. In those cases, the "ADRØ" command is used to select the appropriate register, then the "OCTØ" command, which is explained in a subsequent paragraph, is used to set up the contents of the selected register.

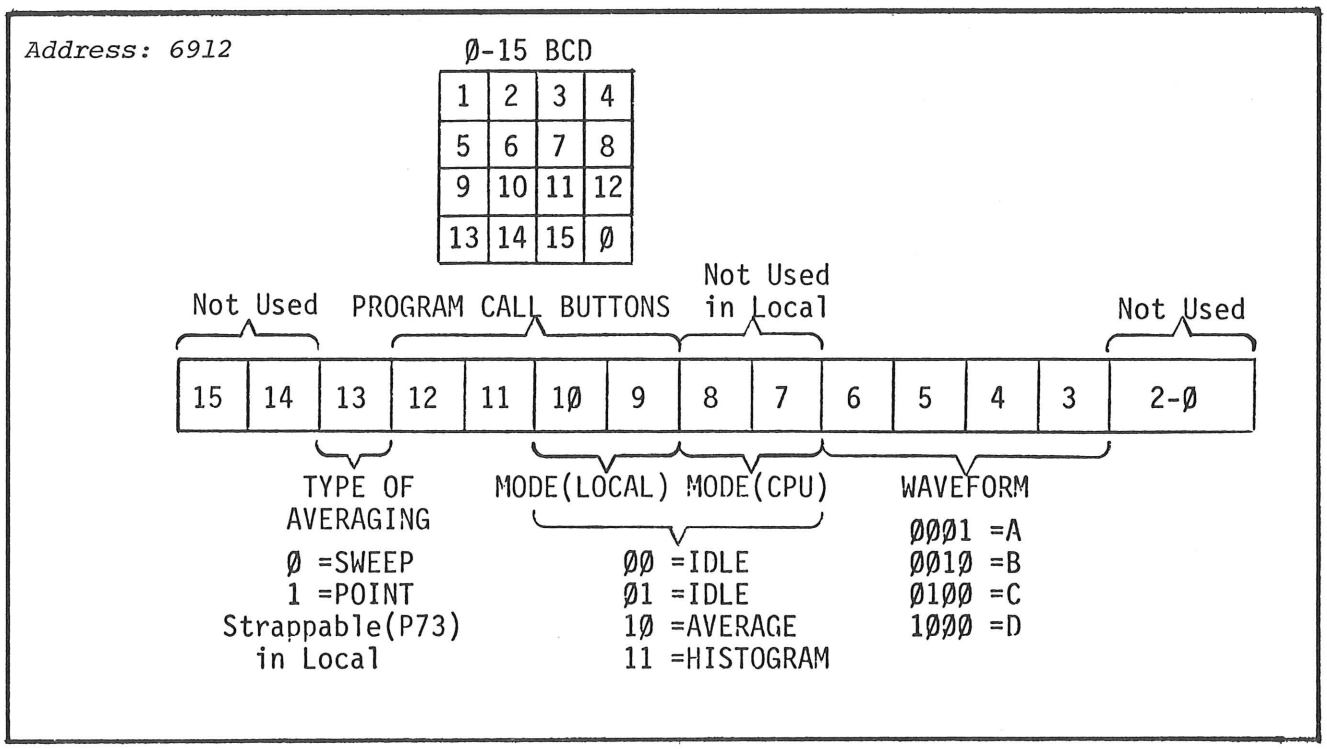


Figure 3-6 HSA Status Register Bit Assignments

OCT Commands

The OCT (Octal) commands are used to send or receive octal representations of the 16-bit Status Words in the DPO Status Register (see Figures 3-5 and 3-6). The octal form is used to ease programming. Note that the octal numbers must be enclosed in quotation marks and treated as characters (i.e., in the form of a string literal). If not enclosed in quotation marks, the TEK 4051 will suppress the leading zero(s), which will cause the DPO to assert SRQ to the controller with a Status Word 113, indicating illegal operation. The octal representation may also be in the form of a string variable that is defined elsewhere in the program.

The DPO Address Register in the interface will not be affected after execution of the "OCTØ" or "OCT?" commands. In most cases, OCT will be immediately preceded by an "ADRØ" command to set the P7001 address on which OCT is intended to operate.

In the following TEK 4051 example, line 1ØØ selects address 7Ø4Ø (Front Panel Status Register), and line 11Ø sets the Front Panel Display source to P7001 Memory, Waveform A.

```
1ØØ    PRINT @1:"ADR ";7Ø4Ø
11Ø    PRINT @1:"OCT ";"Ø4ØØ1Ø"
```

The following example may be used to transfer the contents of the Front Panel Status Register to the controller. Note that in line 22Ø, the string variable A$ is used rather that the numeric variable A. This is so the 4051 won't suppress the leading zero of the octal number.

```
2ØØ    PRINT @1:"ADR ";7Ø4Ø
21Ø    PRINT @1:"OCT?"
22Ø    INPUT @1:A$
```


@

STO and HOL Commands

The "STOØ" (Store) command is used to place the DPO in the Store mode, and consists of the command mnemonic followed by a one, two, three or four character string representing the DPO channels to be placed in the Store mode. The argument following the command mnemonic can be A, B, C or D or any combination in any order, as long as all adjacent characters are delimited with a comma (e.g., "A,C,D" or "D,C,A,B").

The "HOLØ" command puts the selected DPO channels in the Hold mode, and follows the same rules as the "STOØ" command for delimiters in the character string.

The "STOØ" and "HOLØ" commands are used together to program the DPO to capture 1 to 4 input signals through the Vertical Amplifier and Time Base plug-ins. In the following TEK 4051 example, line 1ØØ sets Channels A and B of the DPO to Store mode, lines 11Ø and 12Ø create a time delay to permit acquisition of a full waveform, and line 13Ø sets Channels A and B to the Hold mode.

```
1ØØ    PRINT @1:"STO ";"A,B"
11Ø    FOR I=1 to 20
12Ø    NEXT I
13Ø    PRINT @1:"HOL ";"A,B"
```

Note that the time delay required in lines 11Ø and 12Ø of the preceding example depends on the repetition rate of the input signal and the sweep speed at which the DPO is operating. A more detailed discussion of this, along with a graph showing digitizing time for various combinations of sweep speed and input signal repetition rates, may be found in the DPO Operators Manual (Tektronix Part No. 070-1599-00) starting on page 2-2 under the heading "SAMPLE & HOLD and A-D CONVERTER". Each 4051 FOR LOOP step uses approximately 4.5 milliseconds. Therefore, lines 11Ø and 12Ø in the above example insert approximately 90 milliseconds of delay into the program.

SSR Command

The "SSRØ" (Single-Sweep-Reset) command can reset and arm the DPO triggering functions so that from one to four waveforms of single-shot events can be captured if the Time Base plug-ins are set up correctly. The command mnemonic is followed by a a one, two, three or four character string enclosed in quotation marks, as in the "STOØ" and "HOLØ" commands. Once again, a comma must serve as delimiter between characters.

In the following TEK 4051 example, after the programmed number of single-event waveforms (four in this example) have been captured, the DPO asserts the SRQ line to tell the controller that it has something to report. The controller should then be programmed to conduct a poll to determine the origin and nature of the SRQ. The DPO will send a status word of 84 decimal to indicate the single-sweep operation is complete.

```
1ØØ    INIT
11Ø    ON SRQ THEN 2ØØ
12Ø    PRINT @1:"SSR ";"A,B,C,D"
13Ø    GOTO 13Ø
2ØØ    POLL N,M;1
21Ø    IF M=84 THEN 3ØØ
22Ø    RETURN
3ØØ    PRINT "SINGLE-SWEEP COMPLETED"
31Ø    RETURN
```

X-Y and Y-T Commands

The display mode of the DPO can be controlled either by addressing the Display Generator Status Register and using the "OCTØ" command to set bit 13 (as explained under OCT commands), or by using the "X-YØ" and "Y-TØ" commands. If no display mode is specified, the program will default to the Y-T mode.

In the following TEK 4051 example, the Display Generator of the DPO is set to the Y-T mode of display (vertical input vs time).

```
PRINT @1:"Y-T "
```

In the following example, the Display Generator is set to the X-Y mode of display (horizontal input vs vertical input).

```
PRINT @1:"X-Y "
```

Controlling the Hardware Signal Averager (HSA)

If a Hardware Signal Averager (Tektronix Part No. 644-0092-00) is installed in the DPO, it (the HSA) may be controlled with the "HAVØ" and "HISØ" commands. The "HAVØ" command places the HSA in the averaging mode, selects the source and destination of the waveform to be averaged, specifies the number of averages to be taken, and chooses between Point and Sweep averaging. The following example shows how the "HAVØ" command is used:

```
PRINT @N:"HAV ";"S/D ";M;" X"
```

Where: N is the Device Address of the DPO, and;

S is the source of the waveform to be averaged (DPO Waveform A, B, C or D), and;

D is the destination of the averaged waveform, A, B, C or D *(note that S/D must be followed by a space)*, and;

M is a positive decimal integer from 1 to 12 (for "Sweep" averaging) or from 1 to 7 (for "Point" averaging), with the number of averages equal to 2^M, and;

X represents the type of averaging, "ØP" for Point and "ØS" for Sweep *(note that P or S must be preceded by a space)*. If the type of averaging is not specified, the program will default to "Sweep".

Note that source and destination arrays may be the same if desired.

The "HISØ" command, shown below, may be used to place the HSA in the Histogram mode of operation.

```
PRINT @N:"HIS ";"S/D/H ";M;" X"
```

Where: N, S, D, M and X are as described for the "HAVØ" command, and;

H is the destination of the Histogram, DPO Waveform A, B, C or D *(note that H must be followed by a space)*.

Note

The HSA must be strapped for "CPU" operation when used with the TEK 4051. See HSA Manual (TEK P/N 061-1344-00) for details.

Front Panel Interrupts

When any one of the DPO front panel PROGRAM CALL buttons 1-15 is pushed, an SRQ is generated, then the controller should be programmed to conduct a poll. The response to the serial poll is decimal status word 83, indicating that one of the PROGRAM CALL buttons was pushed. In order to find out which button was pushed, the "FPI?" command is used, as in the following example:

```
100    PRINT @1:"FPI?"
110    INPUT @1:F
```

In the foregoing example, line 100 sets up the DPO to output the button information, and line 110 transfers the decimal number of the pushbutton (F) to the controller. If no front panel button was pushed, F in line 110 will be 0.

Since only one level of interrupt is allowed, all previous interrupts must be serviced and cleared before the PROGRAM CALL buttons become active again. It is also necessary to extinguish (clear) the CPU BUSY lamp (PROGRAM CALL button 0) if it is illuminated and it is desired to re-enable the PROGRAM CALL buttons. Previous interrupts and the CPU BUSY lamp may be cleared with the "CLI0" command. This command has no effect on any other DPO status or memory. An example of the "CLI0" command follows:

```
PRINT @1:"CLI "
```

The following sample routine shows a way to service the DPO PROGRAM CALL buttons. *(Note - this sample routine only services Front Panel interrupts. A sample routine for Single-sweep interrupts is given under the heading "SSR Command".)*

```
100    INIT
110    ON SRQ THEN 2000
---
---
----
----
2000   POLL N,M;1
2010   IF M=83 THEN 2100
2020   RETURN
2100   PRINT @1:"FPI?"
2110   INPUT @1:F
2120   IF F>9 THEN 2200
2130   GOSUB F OF 3100,3200,3300,3400,3500,3600,3700,3800,3900
2140   GOTO 2220
2200   F=F-9
2210   GOSUB F OF 4000,4100,4200,4300,4400,4500
2220   PRINT @1:"CLI "
2230   RETURN
```

In the foregoing example, lines 3100 through 4500 are service subroutines for PROGRAM CALL buttons 1 through 15, respectively. Lines 2220 and 2230 serve to clear the Front Panel PROGRAM CALL buttons for all of the service subroutines before returning to the main program flow.

DCL Command

The "DCLØ" command performs the function of the "CLIØ" command (i.e., clears front panel interrupts and re-enables the DPO PROGRAM CALL buttons). In addition, execution of a "DCLØ" commands the interface to go through a firmware initialization, initializes (sets to Ø) the DPO Address Register, and sets all DPO operations with a default mode to the default mode. This command can also be used to clear service requests (SRQ). Device Clear can be executed as follows:

```
PRINT @1:"DCL "
```

Transferring Waveform Arrays

Waveforms may be transferred from one DPO memory location (A, B, C or D) to another with the following command:

```
PRINT @1:"TAB "
```

Where: A is the waveform source (can be A, B, C or D), and;

B is the waveform destination (can also be A, B, C or D)..

Acquiring and Scaling Data

The following routine is an example of how to acquire data from the DPO, to subtract a zero reference, and to appropriately scale the data. In this example, it is assumed that the left vertical plug-in slot in the 7704A mainframe is being used.

```
1Ø      DIM W(512)
2Ø      PRINT @1:"STO ";"B"
3Ø      FOR I=1 to 3Ø
4Ø      NEXT I
5Ø      PRINT @1:"HOL ";"B"
6Ø      PRINT "GROUND PROBE, PRESS RETURN"
7Ø      INPUT A$
8Ø      PRINT @1:"STO ";"C"
9Ø      FOR I=1 to 3Ø
1ØØ     NEXT I
11Ø     PRINT @1:"HOL ";"B"
12Ø     PRINT @1:"DPC?"
13Ø     INPUT @1:W
14Ø     Z=Ø
15Ø     FOR I=1 to 5Ø
16Ø     Z=Z+W(I+2ØØ)
17Ø     NEXT I
18Ø     Z=Z/5Ø
19Ø     PRINT @1:"DPB?"
2ØØ     INPUT @1:W
21Ø     W=W-Z
22Ø     PRINT @1:"CHL ";"BØ"
23Ø     PRINT @1:"SCL?"
24Ø     INPUT @1:S$
25Ø     V=VAL(S$)
26Ø     M=POS(S$,"V",1)
27Ø     T$=SEG(S$,M-1,1)
28Ø     M=POS("munp",T$,1)
29Ø     V=V*1Ø↑(-3*M)
3ØØ     W=W*(V/1Ø2.3)
```

In the preceding example, lines 1Ø through 5Ø "STORE" and "HOLD" a waveform in DPO memory location B. Line 6Ø displays a message to prompt the user to set up a ground reference waveform. Line 7Ø is simply a method to stop the controller until the user makes the necessary changes to ground the probe (or plug-in), then he would type in a carriage return to make the program continue (A$ would not be used in subsequent computations). Lines 8Ø through 13Ø STORE, HOLD, and then transfer the ground reference waveform to the 4051. Lines 14Ø through 18Ø take an average of 50 elements from the middle of the ground reference waveform (to avoid end point inaccuracies) which becomes the zero reference value.

The raw data transfer of the original waveform occurs in lines 19Ø and 2ØØ, and the zero reference value is subtracted from the raw data in line 21Ø. Lines 22Ø through 24Ø acquire the knob readout of the vertical plug-in which is stored in S$. Lines 25Ø through 29Ø decode S$ and translate it to a numerical value. Line 3ØØ multiplies the data to the scale factor. The array W now contains the scaled data.

Selecting Display Source

The following routine changes the "DISPLAY SOURCE" selector buttons of the DPO:

```
1Ø    PRINT @1:"ADR ";7Ø4Ø
2Ø    PRINT @1:"OCT?"
3Ø    INPUT @1:S$
4Ø    S$=REP("x",2,1)
5Ø    PRINT @1:"OCT ";S$
```

Where: In line 4Ø, x=2 (plug-ins), or x=4 (memory), or x=6 (both).

In the foregoing example, lines 1Ø through 3Ø acquire the current settings of the Front Panel Status Word. Line 4Ø replaces the two binary bits that affect the display source setting, and line 5Ø outputs the new status word. It is necessary to read the status first so that the other front panel controls do not change when the new status word is sent.

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

Section 4
MAINTENANCE

INTRODUCTION

This section of the manual includes a Basic Block Diagram of the P7001/IEEE 488 Interface (Figure 4-1) and two Functional Block Diagrams (Figure 4-3, (MPU/GPIB Board) and (Figure 4-4, PIA/P7001 Board). The Basic Block Diagram provides a cursory examination of the interface's basic functions while a more detailed description is keyed to the Functional Block Diagrams. Each of the functional blocks within Figures 4-3 and 4-4 contains an alphanumeric designator enclosed in a diamond (e.g., <1A>, <2B>) that references a specific schematic diagram illustrating the circuitry involved. Where practical, IC numbers are included in the functional blocks to provide additional cross-referencing.

Familiarity with IEEE Standard 488-1975, "IEEE Standard Digital Interface for Programmable Instrumentation" is required for a comprehensive understanding of the IEEE 488 Bus functions and signals. For further information on P7001 data and control signals, see the P7001 Processor Service Manual (Tektronix Part No. 070-1882-00) and P7001 Main Interface Service Manual (Tektronix Part No. 070-1604-00). Signals associated with the MPU are explained in Motorola's M6800 Microprocessor Applications Manual and M6800 System Design Data Manual. Excerpts from the latter are included as an Appendix to this manual.

BASIC BLOCK DIAGRAM DESCRIPTION

Refer to Figure 4-1 for the following discussion. Data to be exchanged between the P7001 (Processor section of a Tektronix Digital Processing Oscilloscope) and an IEEE 488 Bus device are transferred from the bus of the "talker" through transceivers (buffers) to the PIA's (Peripheral Interface Adapters). The function of the PIA's is to adapt the data and control signals from the IEEE 488 Bus and P7001 Bus to the Microprocessor Bus.

The information from the PIA's is stored in RAM (Random Access Memory), where it is manipulated by the MPU (Microprocessor) in accordance with instructions stored in the PROM (Programmable Read-Only Memory). The informa-

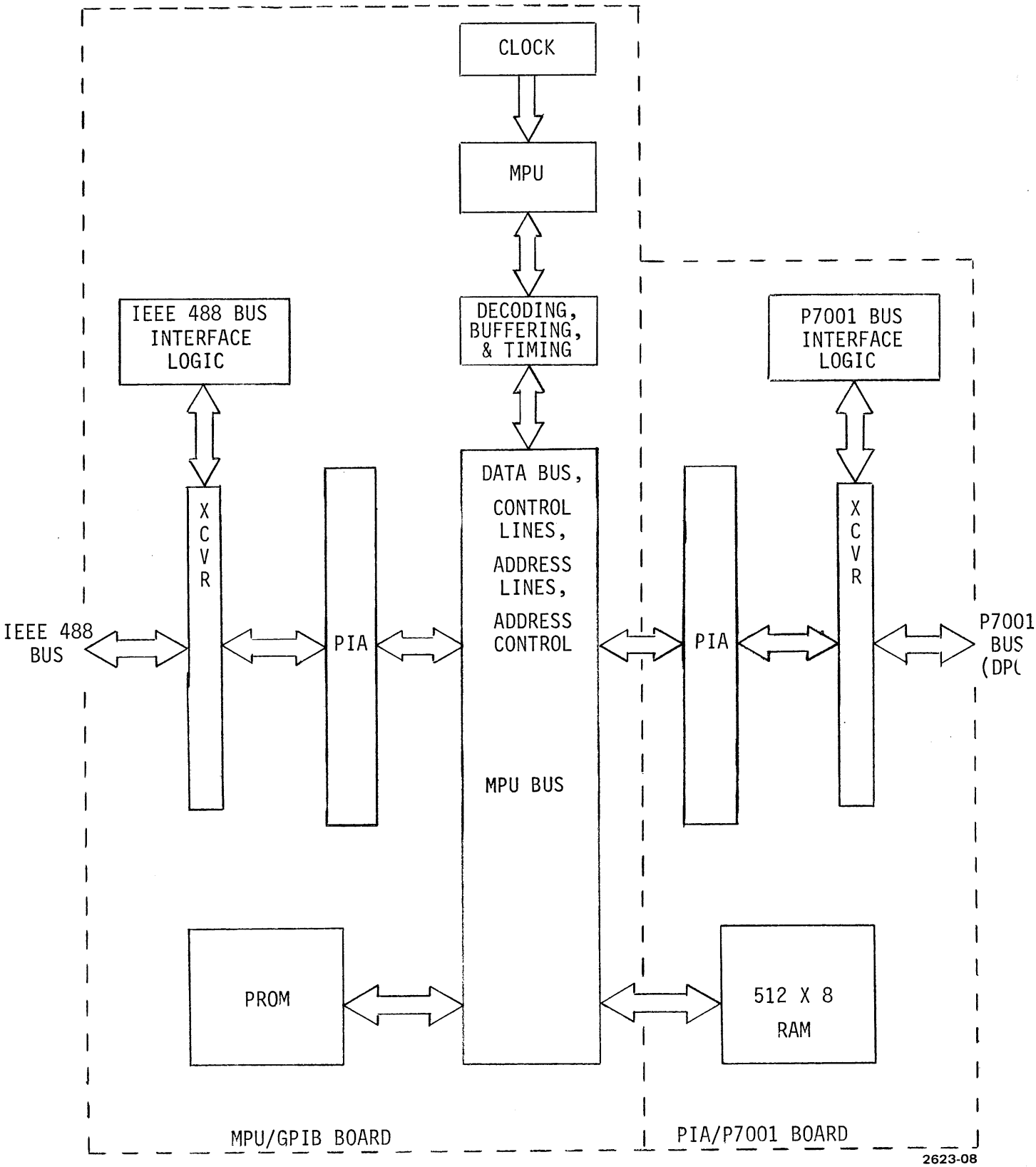


Figure 4-1. Basic Block Diagram

BASIC BLOCK DIAGRAM DESCRIPTION (Continued)

tion is then adapted to the "listener" bus by a second group of PIA's before being buffered out of the interface.

BLOCK DIAGRAM SIGNAL DEFINITIONS

The following signal definitions are provided as an introduction to the signal names used on the Functional Block Diagram (Figures 4-3 and 4-4) and to show their mnemonic derivations. More detailed signal descriptions may be obtained from the appropriate documents mentioned earlier in this section.

IEEE 488 Bus Signals (Refer to Figure 4-3)

$\overline{NRFD}$	-	Not Ready for Data	Data Transfer Control (Handshake) Lines
$\overline{NDAC}$	-	Not Data Accepted	
$\overline{DAV}$	-	Data Valid	
$\overline{ATN}$	-	Attention	Interface Management Lines
$\overline{IFC}$	-	Interface Clear	
$\overline{SRQ}$	-	Service Request	
$\overline{REN}$	-	Remote Enable	
$\overline{EOI}$	-	End or Identify	
$\overline{DIO1}$ through $\overline{DIO8}$			Data Input/Output Lines

MPU (Motorola M6800) Bus Signals (Refer to Figure 4-3)

VMA - Valid Memory Address; this MPU output indicates to the PIA's, RAM and PROM that there is a valid address on the address bus.

R/$\overline{W}$ - Read when high/Write when low; this MPU output signals to the PIA's and RAM whether the MPU is in the read or write state.

$\overline{RESET}$ - This input is used to reset and start the MPU from a power-down state.

ϕ_1, ϕ_2 - Phase 1 and Phase 2; two phases of a clock running at the V_{CC} level.

$\overline{NMI}$ - Mon-Maskable Interrupt; a low-going edge on this input requests that a non-mask interrupt sequence be generated within the MPU.

$\overline{IRQ}$ - Interrupt Request; a low level on this input requests that an interrupt sequence be generated in the MPU.

MPU (Motorola M6800) Bus Signals (Continued)

DBE - Data Bus Enable; this MPU input is tied to clock ϕ_2.

AØ through A15 - Three-state Address Bus outputs.

DØ through D7 - Bi-directional data bus.

$\overline{\text{HALT}}$, TSC, BA - The $\overline{\text{HALT}}$ and Three-State Control inputs, and the Bus Available output, are not used.

P7001 Bus Signals (Refer to Figure 4-4)

$\overline{\text{P-BIT Ø}}$ through $\overline{\text{P-BIT 15}}$ - P7001 Data Bits Ø (least significant) through 15.

$\overline{\text{PAØ}}$ through $\overline{\text{PA12}}$ - P7001 Card Address Bits Ø (LSD) through 12.

$\overline{\text{I/O STROBE}}$ - In/Out Interface Strobe from P7001 Front Panel Card Controller.

$\overline{\text{SYNC ACK}}$ - Sync Acknowledge to/from P7001 Common Bus.

$\overline{\text{DATA MODE Ø}}$ - Data Mode Ø to P7001 Common Bus; functions as Read/Write select in DPO.

$\overline{\text{DATA CH REQ}}$ - Data Channel Request to P7001 Front Panel Priority Logic.

$\overline{\text{SELECT ACK}}$ - Select Acknowledge to P7001 Front Panel Priority Logic.

$\overline{\text{CONT SYNC}}$ - Controller Sync to P7001 Common Bus.

$\overline{\text{BUS BUSY}}$ - Bus Busy to/from P7001 Common Bus.

DATA CH GRANT IN - Data Channel Grant Input from next lower-priority card on P7001 common bus.

DATA CH GRANT OUT - Data Channel Grant Output to P7001 common bus.

$\overline{\text{POWER FAIL}}$ - Signal from P7001 common bus, engendered by DPO turn-on.

Internal Signals, GPIB Interface (Refer to Figure 4-3)

talk - "talk" enable signal from PIA U121. Used by control logic circuitry to enable transceivers to send information.

listen - "listen" enable signal from PIA U121. Used by control logic circuitry to enable the interface to control the $\overline{\text{NDAC}}$ and $\overline{\text{NRFD}}$ lines when the DPO is listening.

rdy - "ready" signal from PIA U121. Used by control logic circuitry to control $\overline{\text{NRFD}}$ line. See "Acceptor Handshake State Diagram" on page 21 of IEEE Standard 488-1975.

rfd - "ready for data" signal from PIA U122. Used by control logic to control $\overline{\text{NRFD}}$ line. See "Source Handshake State Diagram" on page 19 of IEEE Standard 488-1975.

@

Internal Signals, GPIB Interface (Continued)

$\overline{\text{out-enable}}$ - enabling signal from control logic circuitry to transceivers.

BDØ through BD7 - Buffered Data Bits Ø through 7.

Rx, Tx, Clk X 8 - RS232C test signals, not part of Interface operation.

Internal Signals, MPU & Control (Refer to Figure 4-3)

EDØ through ED7 - Data Bits Ø through 7 from PROM to MPU.

ØXXX - 4-digit hexadecimal number decoded from MPU address bus; 'X' indicates "don't care" condition. This line, together with several additional lines from the MPU bus, is used to enable the PIA's and the RAM.

5XXX, 6XXX, 7XXX - Signal descriptions same as ØXXX; these lines are used with PE1 - PE4 to enable the PROM.

$\overline{\text{XØXX}}$ through $\overline{\text{X7XX}}$ - Signal descriptions same as ØXXX; $\overline{\text{XØXX}}$ and $\overline{\text{X1XX}}$ are used for RAM enable, along with ϕ_2, VMA and ØXXX. $\overline{\text{X2XX}}$ through $\overline{\text{X7XX}}$ are used for PIA enable, along with ϕ_2, VMA and ØXXX.

PE1 through PE4 - These are the inverted, OR'ed combination of decoded hexadecimal address lines $\overline{\text{XØXX}}$ through $\overline{\text{X3XX}}$, $\overline{\text{X4XX}}$ through $\overline{\text{X7XX}}$, $\overline{\text{X8XX}}$ through $\overline{\text{XBXX}}$ and $\overline{\text{XCXX}}$ through $\overline{\text{XFXX}}$, respectively. They are used, in conjunction with 5XXX, 6XXX and 7XXX as PROM enable lines.

Internal Signals, P7001 Bus Interface (Refer to Figure 4-4)

Done - Signal from control logic circuitry to PIA U29, indicates P7001 bus transfer is completed.

IRPT - Interrupt signal from control logic circuitry to PIA U29, indicates DPO interrupt.

Read Data - Signal from control logic enables data latch to read incoming data.

P7001 Data Strobe - Signal from control logic enables data transceivers.

Clear - Signal from PIA U27 clears the control logic flip-flops.

Read/$\overline{\text{Write}}$ - Signal from PIA U27 tells the control logic to read (high) or write (low) input from/to P7001 common bus.

P7001 Address Strobe - Signal from control logic enables address output buffers.

Enable - Signal from PIA U27, positive-going edge enables the control logic to read or write input from or to P7001 common bus.

Internal Signals, P7001 Common Bus (Continued)

D IN Ø through D IN 15 - Data in from P7001 common bus.
D OUT Ø through D OUT 15- Data out to P7001 common bus.
PDØ through PD15 - Latched data from P7001 common bus.

Internal Signals, RAM (Refer to Figure 4-4)

RAM enable - Signal from control logic enables RAM.

CLOCK

The clock circuitry consists of a crystal-controlled 4 MHz oscillator followed by a divide-by-four counter. Both output phases of the counter are used, providing the two clock phase signals, ϕ_1 and ϕ_2. ϕ_1 is used by the MPU to set up its own internal registers. ϕ_2 is used, along with the VMA signal, to provide timing for the PIA's, the RAM and the PROM.

RESET

When power in the DPO is first turned on, the $\overline{\text{POWER FAIL}}$ pulse is generated in the P7001 and applied from the P7001 bus to the RESET circuitry in the Interface. The RESET One-Shot, U310, delays the pulse approximately 200 milliseconds before it releases $\overline{\text{RESET}}$. The $\overline{\text{RESET}}$ pulse accomplishes the following:

1. Initializes the MPU and the PIA's.
2. Under firmware control (instructions stored in PROM), initializes the RAM and programs the PIA's to the required status.
3. Through the Address Decode and other logic circuitry, causes PIA U122 to assert $\overline{\text{SRQ}}$, the GPIB Service Request line. The MPU will remember why the $\overline{\text{SRQ}}$ was generated by storing a decimal status word (81 in the case of DPO power-up) in the SRQ table of the RAM.

PROM

The 1K X 8-bit UV-erasable static PROM (Programmable Read-Only Memory) contains the firmware necessary to operate the P7001/IEEE 488 Interface.

RAM

The 512 X 8-bit static RAM (Random Access Memory) contains all the read/write registers for the interface, including the DPO Address Register, DPO Data Register, DPO Status Register, and input and output buffers for the GPIB. Detailed information on these chips will be found in Motorola's MCM6810A Data Sheets, found in *Appendix A* in the rear of this manual, and the M6800 Microcomputer System Design Data Manual.

PIA

The PIA's provide a means of interfacing external devices to the MPU. Data sheets for the PIA's (Motorola MC6820) will also be found in *Appendix A* and Motorola's M6800 Microcomputer System Design Data Manual.

MPU & CONTROL

The MPU & Control section contains the decision-making circuitry for the interface. Operation of the MPU (Microprocessing Unit or Microprocessor) is quite complex and will not be analyzed to any great extent in this manual. Information regarding the MPU can be found in Motorola's M6800 Applications Manual, M6800 Microcomputer System Design Data Manual, or *Appendix A* of this manual.

The Address Decode Logic receives address lines A8 through A14 from the MPU, and when gated by the $\overline{\text{VMA}}$ line, provides hexadecimal outputs used to address/select the PIA's, RAM and PROM.

The Data Latch (U117) is used to latch the PROM Data (ED$\emptyset$ - ED7) in order to provide faster access to the PROM data and decrease the capacitive load on the Data Transceivers. This provides a more reliable data transfer from the PROM to the MPU and from the Data Transceivers to the PIA's and RAM.

GPIB INTERFACE

The GPIB Interface includes PIA's and associated circuitry required to

GPIB INTERFACE (Continued)

interface data and control signals between the MPU and IEEE 488 Bus. All control and interface management signals except $\overline{\text{NRFD}}$ are generated or accepted from the bus under firmware control.

$\overline{\text{NRFD}}$ is under hardware control because of the limited time in which it must respond to the system controller. When $\overline{\text{ATN}}$ is asserted by the controller, the Control Logic will cause $\overline{\text{NRFD}}$ to be asserted in less than 200 nanoseconds, much faster than the MPU could respond. When $\overline{\text{NRFD}}$ has been asserted, the Control Logic will respond to any interface message received or transmitted by controlling the rdy, rfd, talk or listen lines.

SW412 connected to PIA U121 is the 5-bit DIP switch used to select the Device Address of the DPO.

P7001 INTERFACE

The P7001 Interface circuitry includes PIA's and associated Data Latches, Transceivers and Buffers, and control logic needed to interface the DPO's P7001 Bus to the MPU. Bus timing diagrams are shown in Figures 4-2A and 4-2B.

When the MPU wants to read data from, or write data to the DPO, it first sets up the PIA's (U29 for READ, U27 and U28 for WRITE) by programming. After a 10 microsecond delay to ensure that all Address lines, Read/Write and other control lines are settled, the Enable line (from U27) is asserted, causing the Control Logic to send out $\overline{\text{DATA CH REQ}}$. The Front Panel Priority Logic in the P7001 replies with DATA CH GRANT IN, provided that another P7001 card (e.g., A/D Converter, Display Generator) is not in control of the bus.

As soon as DATA CH GRANT IN is received, the Control Logic will send out $\overline{\text{SELECT ACK}}$. This returns to the P7001 Front Panel Priority Logic and terminates DATA CH GRANT IN. The Control Logic then checks to make sure $\overline{\text{SYNC ACK}}$ and $\overline{\text{BUS BUSY}}$ are not present. If not, the Control Logic goes to the Master State and gates the Address lines with P7001 Address Strobe. If the operation is a "write", the Data lines are also gated via the P7001 Data Strobe.

@

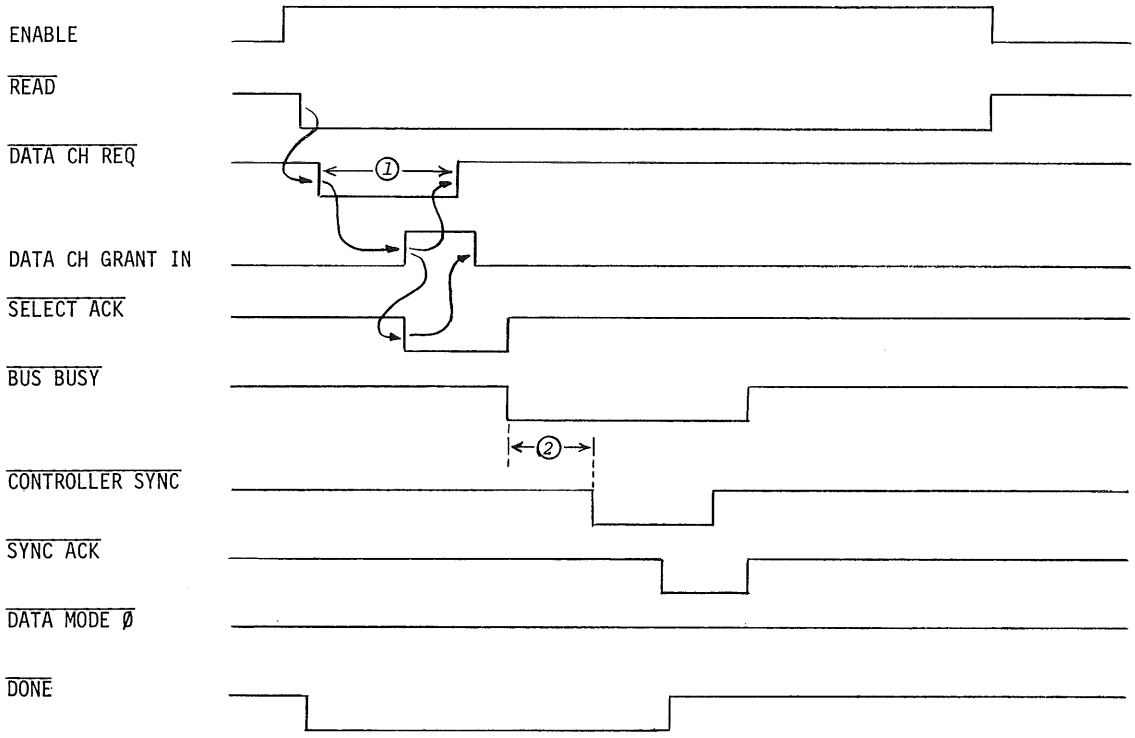
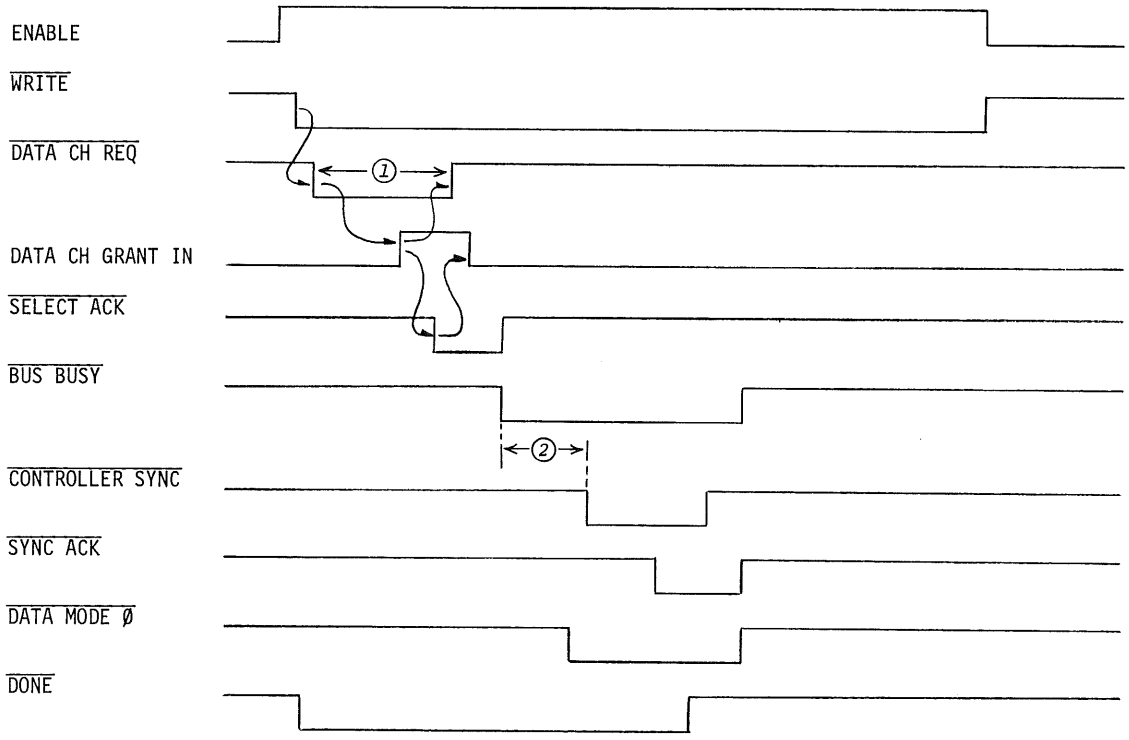


Figure 4-2A. P7001 Bus Read Operation



NOTES: (1) *3.5usec max; if greater than 3.5usec, P7001 Bus will time-out (hardware error).*

(2) *50nsec minimum.*

(3) *Drawing not to scale.*

Figure 4-2B. P7001 Bus Write Operation

P7001 INTERFACE (Continued)

If the P7001 Front Panel is being addressed, it will now disconnect the Interface Control Logic for 500 milliseconds so that it cannot be disturbed for that 500 milliseconds. If the operation is a "write", the P7001 Front Panel will latch the status word and perform the appropriate operation. The Front Panel then sends $\overline{\text{SYNC ACK}}$ back to the Control Logic. This sets the DPO to the idle state and terminates $\overline{\text{BUS BUSY}}$.

If one of the P7001 PROGRAM CALL buttons is pushed, an $\overline{\text{I/O STROBE}}$ is generated. The Control Logic receives the $\overline{\text{I/O STROBE}}$ and interrupts the MPU via PIA U29 and the IRPT signal. The MPU programs PIA U29 to ignore IRPT (to discourage continuous interrupt), and looks at the P7001 Front Panel status to determine why the $\overline{\text{I/O STROBE}}$ was issued. If it was for a valid reason (the MPU determines this under program control), the MPU will enable U29 to recognize IRPT again, and will assert $\overline{\text{SRQ}}$ on the IEEE 488 Bus.

@

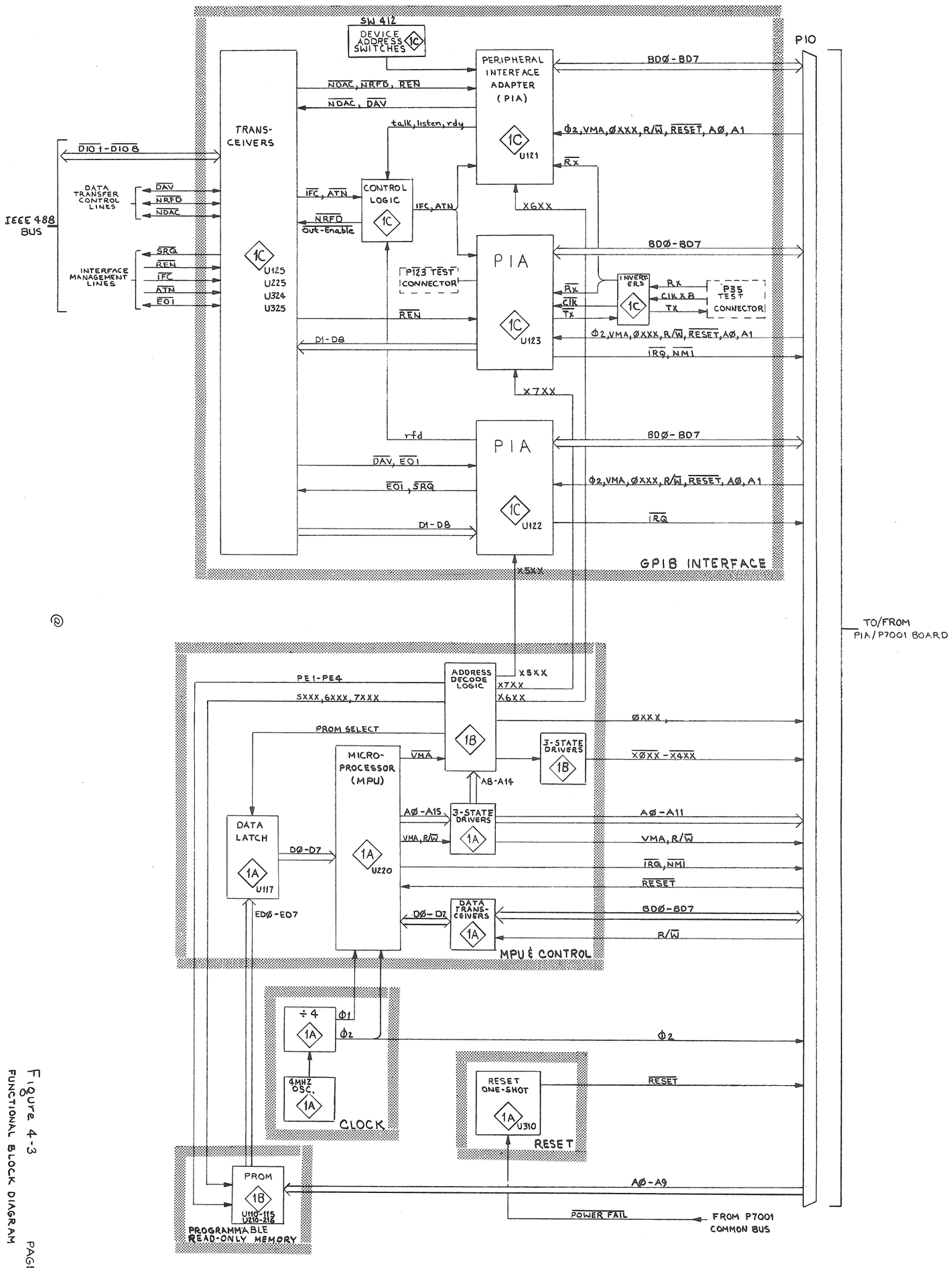
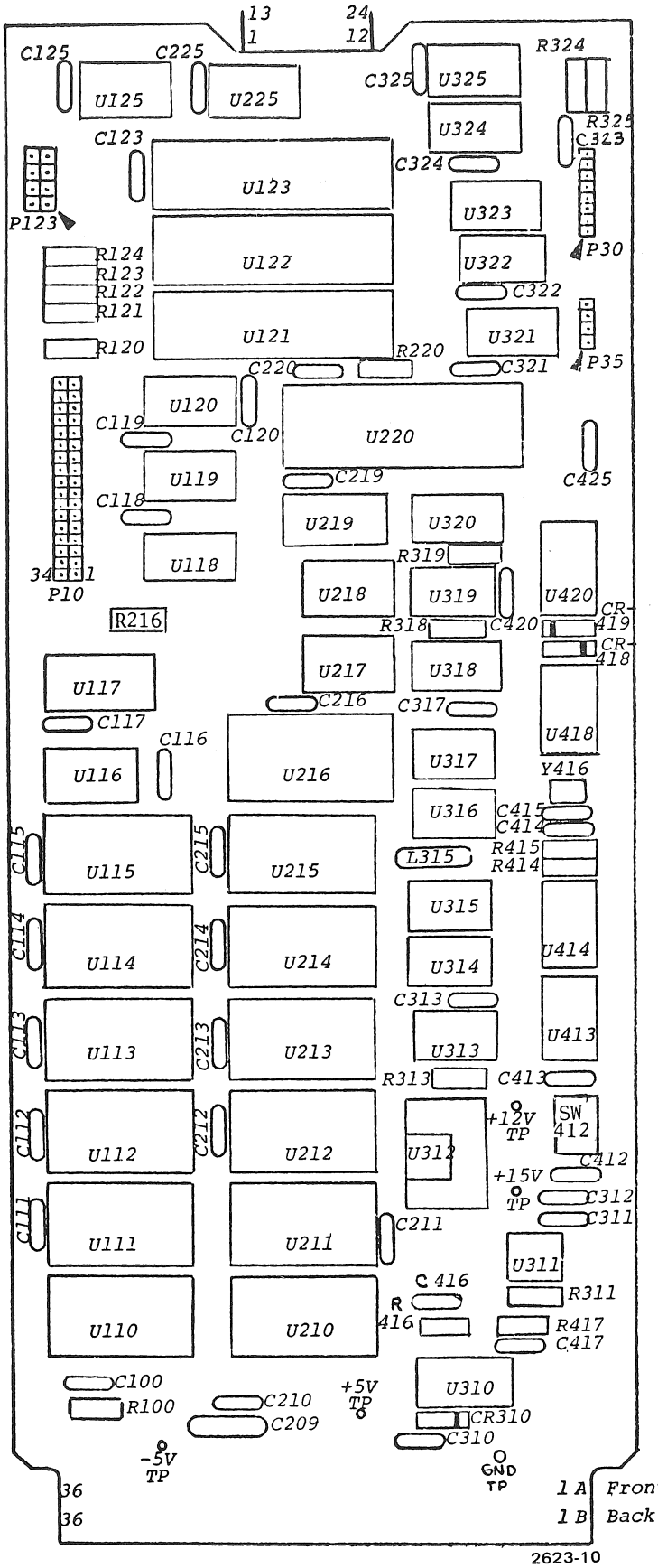


Figure 4-3
FUNCTIONAL BLOCK DIAGRAM
MPU/GPIB BOARD

MPU/GPIB BOARD
COMPONENT LOCATOR



2623-10

Component Location
MPU/GPIB Board

@

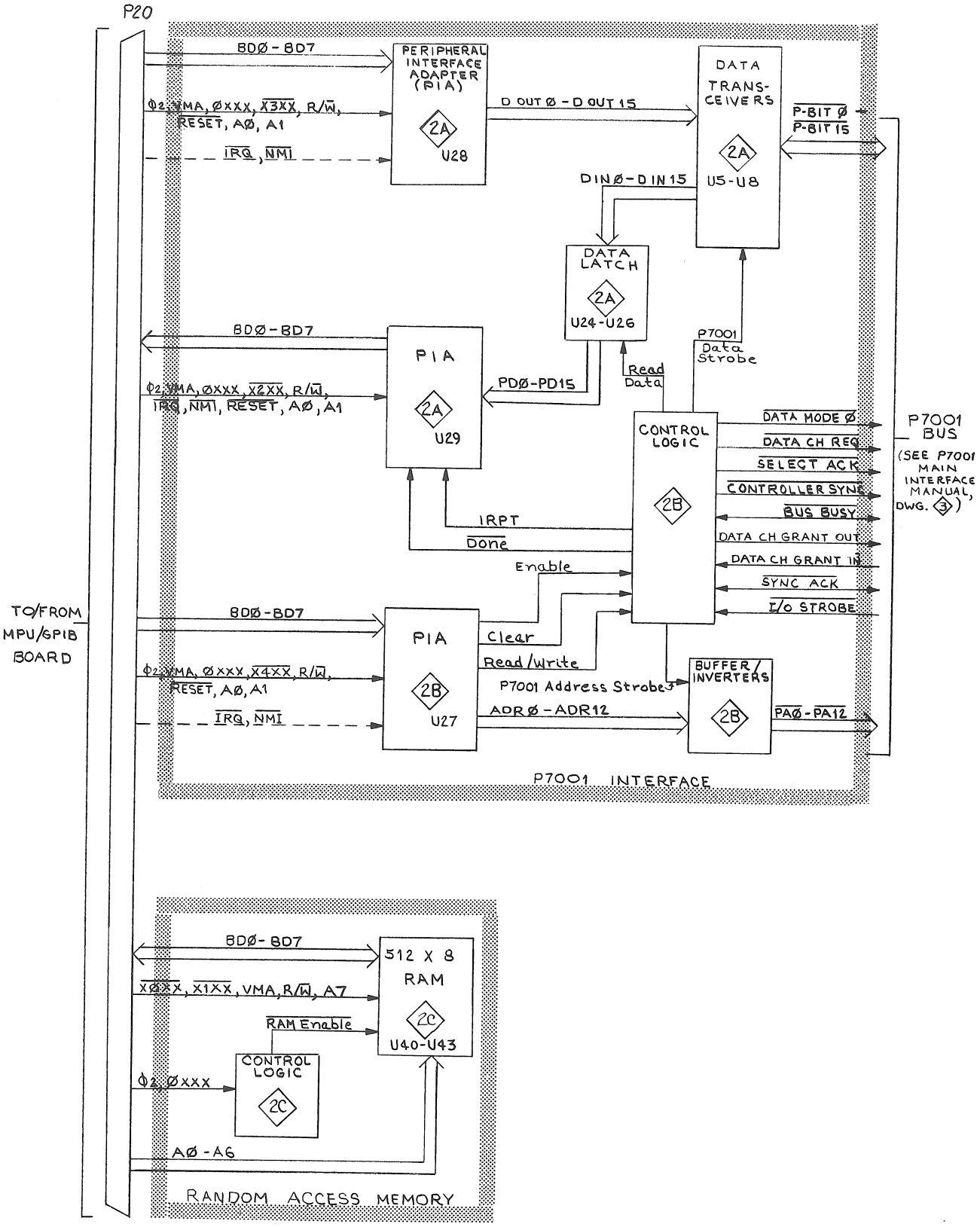


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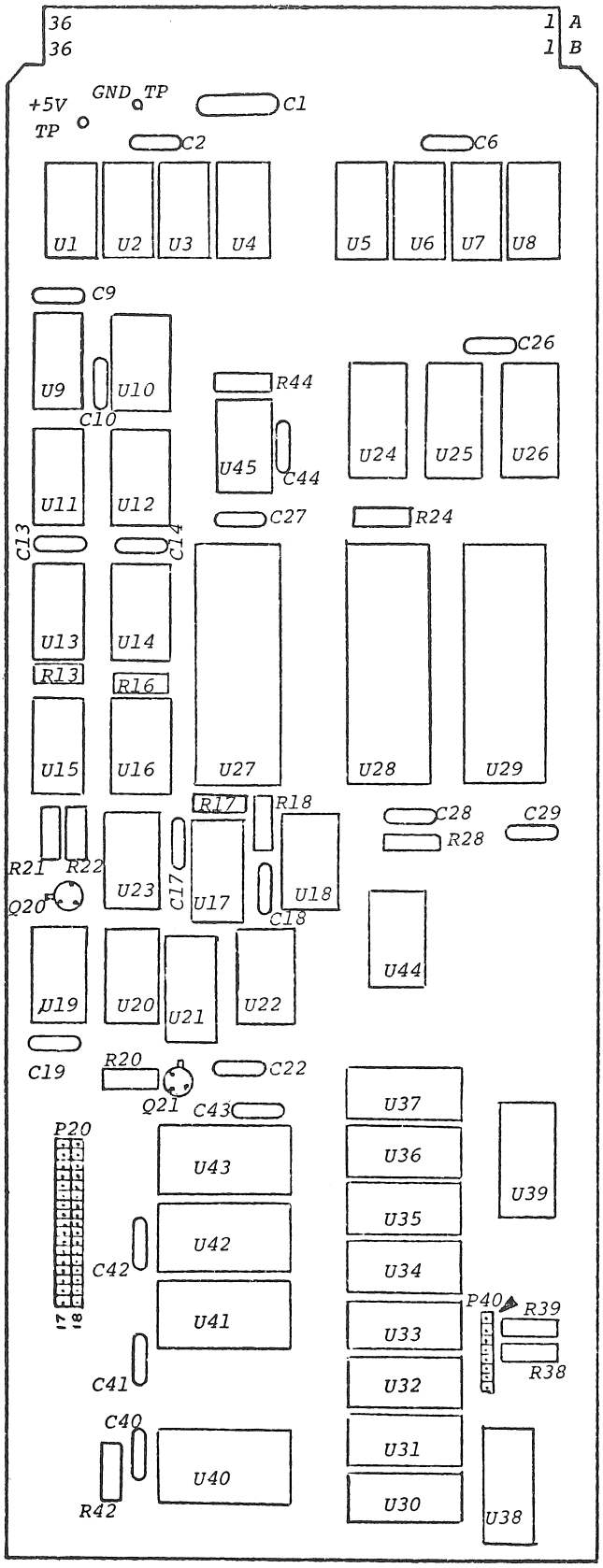
Figure 4-4 PAGE 4-12

FUNCTIONAL BLOCK DIAGRAM
PIA/P7001 BOARD 2/78

PIA/P7001 BOARD
COMPONENT LOCATOR



2623-09

Component Location

PIA/P7001 Board

@

DIAGRAMS

Symbols and Reference Designators

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF).
Values less than one are in microfarads (μF).

Resistors = Ohms (Ω).

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it goes to the low state.

Abbreviations are based on ANSI Y1.1-1972.

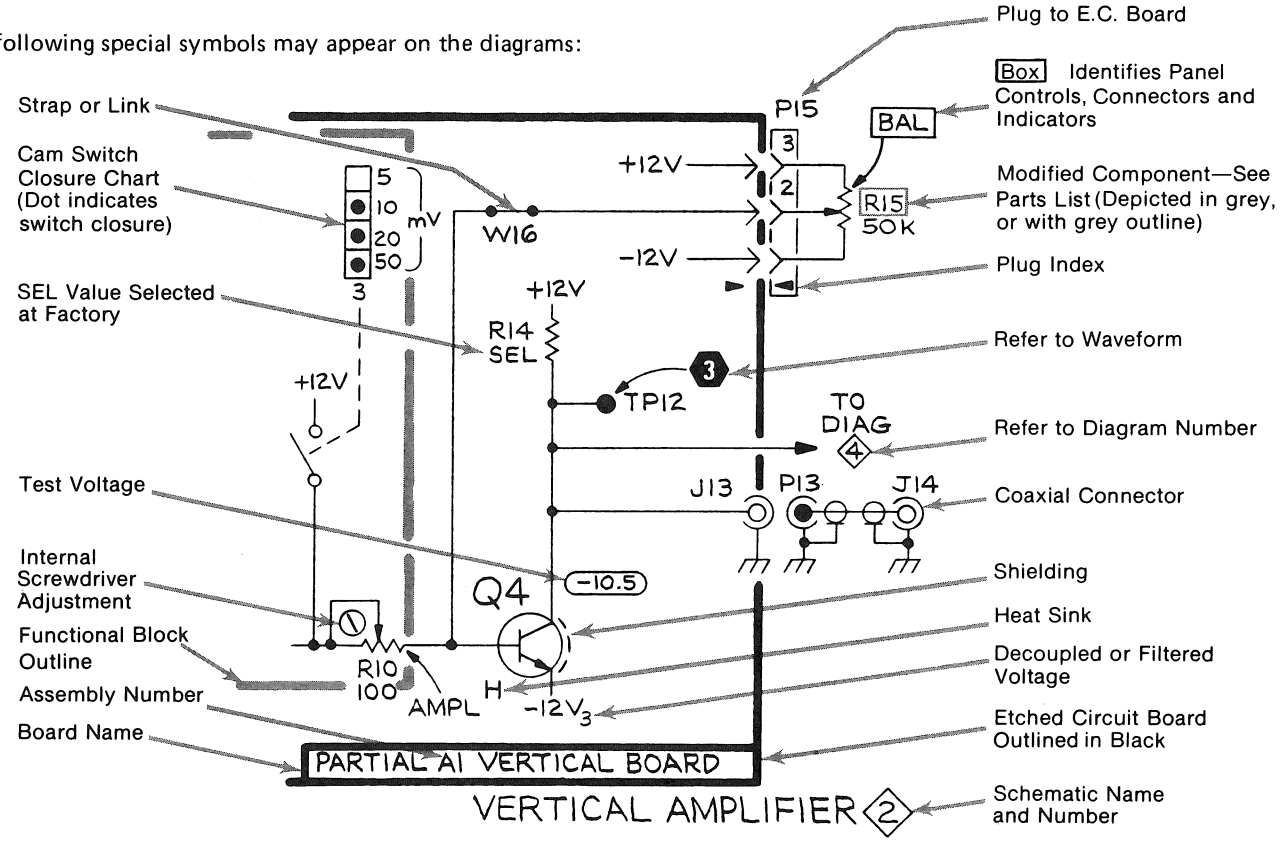
Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

The following prefix letters are used as reference designators to identify components or assemblies on the diagrams.

A	Assembly, separable or repairable (circuit board, etc)	H	Heat dissipating device (heat sink, heat radiator, etc)	S	Switch or contactor
AT	Attenuator, fixed or variable	HR	Heater	T	Transformer
B	Motor	HY	Hybrid circuit	TC	Thermocouple
BT	Battery	J	Connector, stationary portion	TP	Test point
C	Capacitor, fixed or variable	K	Relay	U	Assembly, inseparable or non-repairable (integrated circuit, etc.)
CB	Circuit breaker	L	Inductor, fixed or variable	V	Electron tube
CR	Diode, signal or rectifier	M	Meter	VR	Voltage regulator (zener diode, etc.)
DL	Delay line	P	Connector, movable portion	W	Wirestrap or cable
DS	Indicating device (lamp)	Q	Transistor or silicon-controlled rectifier	Y	Crystal
E	Spark Gap, Ferrite bead	R	Resistor, fixed or variable	Z	Phase shifter
F	Fuse	RT	Thermistor		
FL	Filter				

The following special symbols may appear on the diagrams:



R414 820
U418 74S04
C415 43PF
Y416 4.0MHz
R415 820
U418
L315 15μH
C414 105 PF
U418
+3V1 U413 7474
+3V1 U413
+3V1
+3V1
U414 74LS27
C412 0.47
+15V
U420 75325
+5V
CR419
R318 62
U418
74LS04 U418
U414
+5V
CR418
C425 0.47
R319 62
Φ2
Φ1
A0 → U110-U115, U210-U215-8 U121, U122-36 & U123-35
A1 → U110-U115, U210-U215-7 U121, U122-35 & U123-36
A2 → U110-U115, U210-U215-6
A3 → U110-U115, U210-U215-5
A4 → U110-U115, U210-U215-4
A5 → U110-U115, U210-U215-3
A6 → U110-U115, U210-U215-2
A7 → U110-U115, U210-U215-1
A8 → U110-U115, U210-U215-23 U216-23
A9 → U110-U115, U210-U215-22 U216-22
A10 → U216-21
A11 → U216-20
1B

DPO MAIN INTERFACE, J10 B16
POWER FAIL
U310 NE555
R416 10K
C416 10
C417 0.01
+5V
U217 7404
P/O P10
24
RESET
VMA
U217 7404
U121, U122, U123-22 → 1C
U216-18 → 1B
U116-12 → 1B

U220 6800
Vss RESET
HALT TSC
Φ1
IRQ Φ2
VMA DBE
NMI
BA
Vcc
Vss
DØ D1 D2 D3 D4 D5 D6 D7
NC
R122 1K
+5V
RESET → U121, U122, U123-34 1C
Φ2 → U121, U122, U123-25 1C
U318 8097
ALL 8097
U219
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 NC
U320
U118
U116-15 U116-14 U116-13 → 1B
R/W
R220 1K
+5V
U121, U122, U123-21 → 1C
R/W
P/O P10
28
34 33 32 31 30 29 1 2 3 4 5 6
2

1C U122-37,38 U123-37 → IRQ
+5V R124 3K
U219
11 IRQ
12 VMA
10 NMI
1C U123-38 U121-38 → NMI
+5V R123 3K
+5V C219 0.1

U120 N8833
U119 N8833
BUS
DISABLE
DRVR RCVR
20 BDØ
19 BD1
18 BD2
17 BD3
16 BD4
15 BD5
14 BD6
13 BD7
2

1C U121, U122, U123-33 → BDØ
U121, U122, U123-32 → BD1
U121, U122, U123-31 → BD2
U121, U122, U123-30 → BD3
U121, U122, U123-29 → BD4
U121, U122, U123-28 → BD5
U121, U122, U123-27 → BD6
U121, U122, U123-26 → BD7

1B U414-12 → PROM SELECT
READ
WRITE
R216, 1K +5V
U319 74S38

U110-U115, U210-U215 1B
EDØ EDI ED2 ED3 ED4 ED5 ED6 ED7
A Y
DØ D1 D2 D3 D4 D5 D6 D7
U117 81LS97
+5V C117 0.1

SHEET 1 OF 3; MPU/POWER FAIL/CLOCK CIRCUITRY
P/O 670-4882-00 MPU/GPIB BOARD

P7001/IEEE 488 INTERFACE 1A 6/78

MPU/GPIB BOARD 1A

DPO MAIN INTERFACE J10

+3V1 +3V2 R313 1K R324 1K TP +5V
A18 B18 A1 B27 C209 100 0.1 TP C420 0.47
C116, 118, 119, 120, 123, 216, 219, 310, 312, 313, 317, 322, 323, 413
TP -5V A29
TP +15V U312 LM340T TP +12V B31
R100 91 -12V A30
CR310 12.0V C310 0.1

U318 8097
X0XX X1XX X2XX X3XX X4XX
X5XX X6XX X7XX → U122-23 U121-23 U123-24 (1C)

P/O P10 7 8 27 26 25 (2)

U216 74154 +5V 24
U217-10 VMA 18
U320-11 A8 23 A
U320-9 A9 22 B
U320-7 A10 21 C
U320-5 A11 20 D
(1A)

U317 74LS20: X0XX X1XX X2XX X3XX → PE1
U316 74LS20: X4XX X5XX X6XX X7XX → PE2
U316: X8XX X9XX XAXX XBXX → PE3
U317: XCXX XDXX XEXX XFXX → PE4

U313 74LS00 C100 0.1 · U313 C111 0.1 · U313 C210 0.1 · U313 C211 0.1
U314 74LS00 C112 0.1 · U314 C113 0.1 · U314 C212 0.1 · U314 C213 0.1
U315 74LS00 C114 0.1 · U315 C115 0.1 · U315 C214 0.1 · U315 C215 0.1
U113* · U212* · U213* · U114* · U115* · U214* · U215*
+12V -5V +5V

U116 7442 +5V 16
U118-3 A12 15 · U118-9 A13 14 · U118-11 A14 13 · U217-10 BVMA 12
(1A)
U218 74LS04 · U319 7438 · R121 1K · R120 1K
U217 7404
XXXX → U121-24 U122-24 U123-24
5XXX 6XXX 7XXX

U414
PROM SELECT → U117-1 : 19 (1A)

P10 22 23 (2)
XXXX
0XXX

* TYPICAL IC
U113-U115
U212-U215

U219-13 U219-11 U219-9 U219-7 U320-3 U320-5 U320-7 U320-13 U320-11 U320-9 (1A)
A0 8 · A1 7 · A2 6 · A3 5 · A4 4 · A5 3 · A6 2 · A7 1 · A8 23 · A9 22
V_{DD} 19 · V_{BB} 21 · V_{CC} 24 · V_{SS} 12 · PROGRAM 18 · ROM · $\overline{CS}$/WE 20
ED0 9 · ED1 10 · ED2 11 · ED3 13 · ED4 14 · ED5 15 · ED6 16 · ED7 17
ED0 U117-18 · ED1 U117-16 · ED2 U117-14 · ED3 U117-12 · ED4 U117-8 · ED5 U117-6 · ED6 U117-4 · ED7 U117-2 (1A)

SHEET 2 OF 3; DECODER/PROM
P/O 670-4882-00, MPU/GPIB BOARD

P7001/IEEE 488 INTERFACE

U122 MC6820 — U121 MC6820 — U123 MC6820

* NOTE : W1 IS INSTALLED ONLY FOR "OPTIONAL" CONTROLLER OPERATION.

U125 MC3446 — U225 MC3446 — U325 MC3446 — U324 MC3446

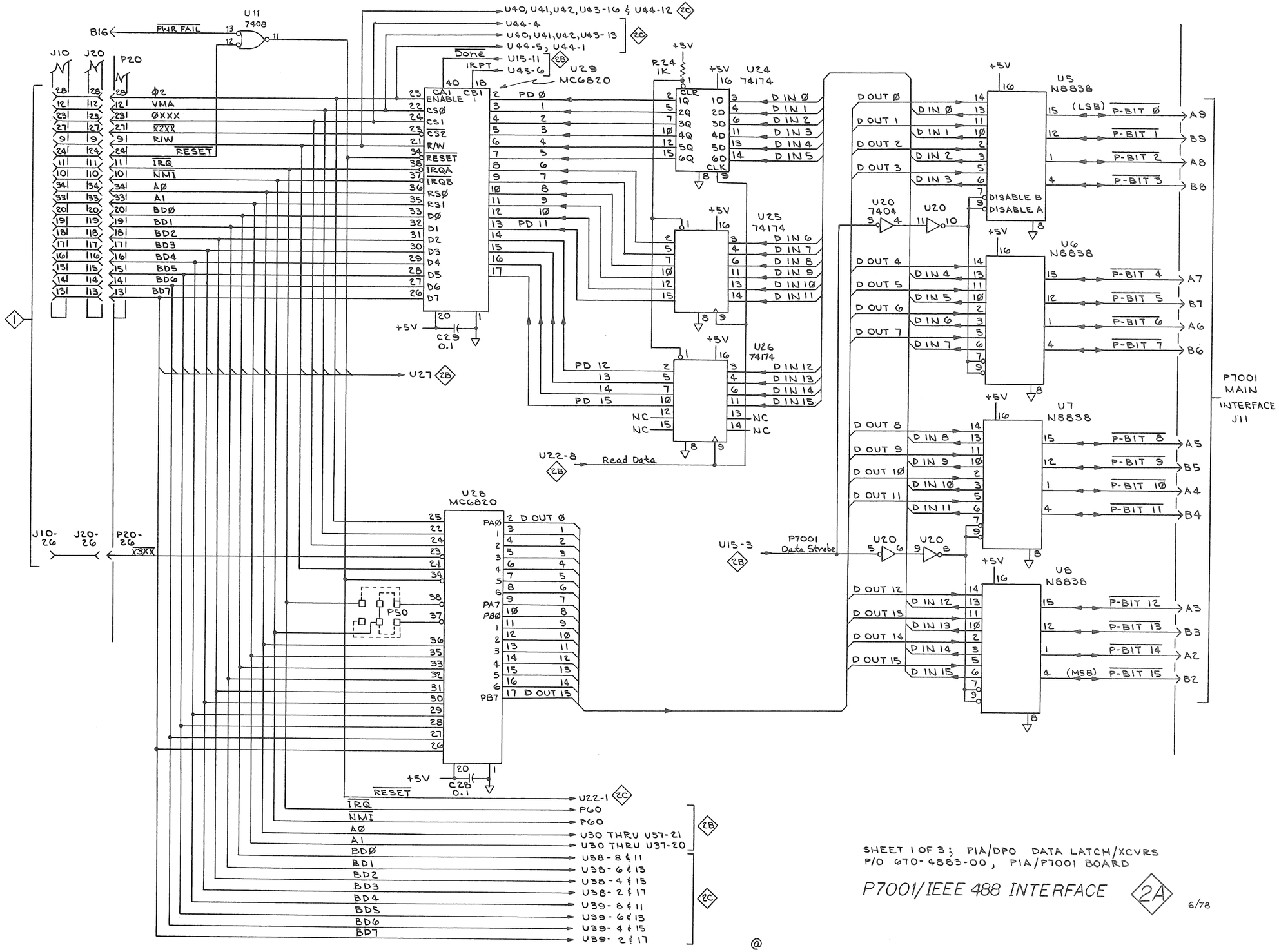
U323 74LS02 — U322 74LS02 — U322 74LS04 — U319 7438 — U218 74LS04 — U311 75150 — U321 75154

IEEE 488 BUS

USED FOR TEST PURPOSES ONLY

SHEET 3 OF 3 ; PIA'S/GPIB TRANCEIVERS
P/O 670-4882-00 MPU/GPIB BOARD

P7001/IEEE 488 INTERFACE 1C 6/78



SHEET 1 OF 3; PIA/DPO DATA LATCH/XCVRS
P/O 670-4883-00, PIA/P7001 BOARD

P7001/IEEE 488 INTERFACE 2A

6/78

P7001 MAIN INTERFACE J11

A18 — R16 1K — V_t

B18 — +5V

C1 100 (+) — C2,6,9,14,19,22,26 0.1

A1

B27

ADR0
ADR1
ADR2
ADR3
ADR4
ADR5
ADR6
ADR7
ADR8
ADR9
ADR10
ADR11
ADR12

U4 7438 — U3 7438 — U2 7438 — U1 7438

LSB

PA0 → A19
PA1 → B19
PA2 → A20
PA3 → B20
PA4 → A21
PA5 → B21
PA6 → A22
PA7 → B22
PA8 → A23
PA9 → B23
PA10 → A24
PA11 → B24
PA12 → A25

MSB

U10 7404

P7001 Address Strobe

P7001 Data Strobe → U20-3 & 5 (2A)

U15 7400 — U11 7408

J10 J20 P20

Φ2
VMA
ØXXX
XRXX
R/W
U11-11 (2A)
IRQ
NMI
AØ
A1
BDØ
1
2
3
4
5
6
BD 7

U28 & U29 (2A)

U27 MC6820

RESET — P60

U28 & U29 (2A) — +5V — C27 0.1

PSO & U29 (2A)

Read/Write

R17 180 — C17 220 — Q21 — +5V — R18 10K — C18 .001

R20 4.7K

U17 74121 (SEE DETAIL 'A')

WRITE — Read

U21 7442

U15 7400 — U16

U19 7410 — U11

U18 7402

Clear

U22 7404

U22 — Read Data → U24,U25,U26-9 (2A)

U16 7474

U15 — Done → U29-40 (2A)

U12

U14 7474 — U13

U20 7404 — U12 7400

U19 — U20 7404

U1 — DATA CH REQ → A14

U1 — SELECT ACK → B15

U11 — U12 — U10 — U9 CONTROLLER SYNC → A11

U1 BUS BUSY → A15

U10 — C10 .001

U13 — DATA CH GRANT OUT → A13

U23 74LS04 — +5V — R21 1K — 180 R22 — Q20 — R13 180 — C13 650PF

U23 — DATA CH GRANT IN → B13

SYNC ACK → B11

+5V — 10K R44 — C44 .001

U29-18 (2A) IRPT — U45 74121 (SEE DETAIL 'A')

U9 — U10 — I/O STROBE → B17

DETAIL 'A' FOR 74121

REXT/CEXT — CEXT RINT — Vcc 14 — B 5 — Q 6 — $\overline{Q}$ 1 — A_1 3 — A_2 4 — GND 7

P7001 MAIN INTERFACE J11

SHEET 2 OF 3; DPO CONTROL
P/O 670-4883-00, PIA/P7001 BOARD

P7001/IEEE 488 INTERFACE 2B

2/78

PIA/P7001 BOARD 2B

J10 J20 P20

Φ2
ØXXX
U27,U28,U29-25
U27,U28,U29-24
U27,U28,U29-22
U27,U28,U29-21
VMA
R/W

U44 7438 OC
+5V R42 1K
RAM Enable
VMA
R/W

A0-A6

U40 MC6810
U41 MC6810
U42 MC6810
U43 MC6810

BD0 BD1 BD2 BD3 BD4 BD5 BD6 BD7
+5V
C40 0.1
C41 0.1
C42 0.1
C43 0.1

U22 7404
U23 74LS04
A7

P10 J20 J10
X1XX
XØXX
BD0 BD1 BD2 BD3 BD4 BD5 BD6 BD7

J10 J20 P20
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11

U44 7438 OC
+5V R38 1K
R/W.12
READ

U44 7438 OC
+5V R39 1K
WRITE

U30-U39 RESERVED FOR FUTURE USE

U39 U38 U37 U36 U35 U34 U33 U32 U31 U30

U44 7438 OC
+5V R28 1K

IXXX
U22 7404
Φ2

SHEET 3 OF 3; 512 X 8 RAM
P/O 670-4883-00, PIA/P7001 BOARD

P7001/IEEE 488 INTERFACE

2/78

PIA/P7001 BOARD

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

ACTR	ACTUATOR	PLSTC	PLASTIC
ASSY	ASSEMBLY	QTZ	QUARTZ
CAP	CAPACITOR	RECP	RECEPTACLE
CER	CERAMIC	RES	RESISTOR
CKT	CIRCUIT	RF	RADIO FREQUENCY
COMP	COMPOSITION	SEL	SELECTED
CONN	CONNECTOR	SEMICOND	SEMICONDUCTOR
ELCTLT	ELECTROLYTIC	SENS	SENSITIVE
ELEC	ELECTRICAL	VAR	VARIABLE
INCAND	INCANDESCENT	WW	WIREWOUND
LED	LIGHT EMITTING DIODE	XFMR	TRANSFORMER
NONWIR	NON WIREWOUND	XTAL	CRYSTAL

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
32159	WEST-CAP ARIZONA	2201 E. ELVIRA ROAD	TUCSON, AZ 85706
34630	TYCO FILTERS DIV., INC.	3940 W. MONTECITO	PHOENIX, AZ 85019
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
59660	TUSONIX INC.	2155 N FORBES BLVD	TUCSON, AZ 85705
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
81073	GRAYHILL, INC.	561 HILLGROVE AVE., PO BOX 373	LA GRANGE, IL 60525
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY AND CO., INC.	3029 E. WASHINGTON STREET P. O. BOX 372	INDIANAPOLIS, IN 46206
91418	RADIO MATERIALS COMPANY, DIV. OF P.R. MALLORY AND COMPANY, INC.	4242 W BRYN MAWR	CHICAGO, IL 60646

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-4882-03			CKT BOARD ASSY:MPU/GPIB	80009	670-4882-03
A2	670-4883-03			CKT BOARD ASSY:PIA/P7001	80009	670-4883-03
C1	290-0296-00			CAP.,FXD,ELCTLT:100UF,20%,20V	56289	150D107X0020S2
C2	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C6	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C9	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C10	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	59660	831-519-Z5U-102P
C13	283-0150-00			CAP.,FXD,CER DI:650PF,5%,200V	59660	835-515B651J
C14	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C17	283-0108-00			CAP.,FXD,CER DI:220PF,10%,200V	56289	272C13
C18	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	59660	831-519-Z5U-102P
C19	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C22	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C26	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C27	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C28	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C29	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C40	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C41	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C42	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C43	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C44	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	59660	831-519-Z5U-102P
C100	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C111	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C112	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C113	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C114	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C115	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C116	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C117	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C118	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C119	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C120	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C123	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C125	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C209	290-0296-00			CAP.,FXD,ELCTLT:100UF,20%,20V	56289	150D107X0020S2
C210	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C211	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C212	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C213	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C214	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C215	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C216	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C219	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C220	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C225	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C310	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C311	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C312	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C313	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C317	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C321	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C322	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C323	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C324	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C325	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
C412	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
C413	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
C414	283-0052-00			CAP.,FXD,CER DI:105PF,1%,500V	72982	0841541C0G01050F
C415	283-0331-00			CAP.,FXD,CER DI:43PF,2%,100V	72982	805-505A430G
C416	290-0536-00			CAP.,FXD,ELCTLT:10UF,20%,25V	90201	TDC106M025FL
C417	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	91418	SP103Z151-4R9
C420	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
C425	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
CR310	152-0168-00			SEMICOND DEVICE:ZENER,0.4W,12V,5%	04713	SZG35009K4
CR418	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
CR419	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
L315	108-0317-00			COIL,RF:FIXED,15UH	32159	71501M
Q20	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
Q21	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
R13	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
R16	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R17	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
R18	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R20	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R21	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R22	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
R24	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R28	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R38	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R39	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R42	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R44	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R100	315-0910-00			RES.,FXD,CMPSN:91 OHM,5%,0.25W	01121	CB9105
R120	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R121	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R122	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R123	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
R124	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
R216	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R220	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R311	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R313	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R318	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
R319	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
R324	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R325	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R414	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
R415	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
R416	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
SW412	260-1827-00			SWITCH,ROCKER:5,SPST	81073	76SB05S
U1	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0145-00
U2	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0145-00
U3	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0145-00
U4	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0145-00
U5	156-0653-00			MICROCKT,INTFC:QUAD UNIFIED BUS XCVR	80009	156-0653-00
U6	156-0653-00			MICROCKT,INTFC:QUAD UNIFIED BUS XCVR	80009	156-0653-00
U7	156-0653-00			MICROCKT,INTFC:QUAD UNIFIED BUS XCVR	80009	156-0653-00
U8	156-0653-00			MICROCKT,INTFC:QUAD UNIFIED BUS XCVR	80009	156-0653-00
U9	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0145-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U10	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U11	156-0129-00			MICROCIRCUIT,DI:QUAD 2-INPUT GATE	80009	156-0129-00
U12	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN7400(N OR J)
U13	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U14	156-0041-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U15	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN7400(N OR J)
U16	156-0041-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U17	156-0072-00			MICROCIRCUIT,DI:MONOSTABLE MV,TTL,14 DIP	01295	SN74121(N OR J)
U18	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U19	156-0047-00			MICROCIRCUIT,DI:TPL 3-INPUT POS NAND GATE	80009	156-0047-00
U20	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U21	156-0061-00			MICROCIRCUIT,DI:SGL,BCD TO DEC DECODER	01295	SN7442(N OR J)
U22	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U23	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0385-00
U24	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	80009	156-0222-00
U25	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	80009	156-0222-00
U26	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	80009	156-0222-00
U27	156-0427-00			MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
U28	156-0427-00			MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
U29	156-0427-00			MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
U40	156-0716-00			MICROCIRCUIT,DI:RAM,128 X 8 STATIC	04713	MCM6810S
U41	156-0716-00			MICROCIRCUIT,DI:RAM,128 X 8 STATIC	04713	MCM6810S
U42	156-0716-00			MICROCIRCUIT,DI:RAM,128 X 8 STATIC	04713	MCM6810S
U43	156-0716-00			MICROCIRCUIT,DI:RAM,128 X 8 STATIC	04713	MCM6810S
U44	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0145-00
U45	156-0072-00			MICROCIRCUIT,DI:MONOSTABLE MV,TTL,14 DIP	01295	SN74121(N OR J)
U113	160-0180-00			MICROCIRCUIT,DI:1024 X 8 STATIC,PRGM	80009	160-0180-00
U114	160-0179-00			MICROCIRCUIT,DI:1024 X 8 STATIC,PRGM	80009	160-0179-00
U115	160-0178-00			MICROCIRCUIT,DI:1024 X 8 STATIC,PRGM	80009	160-0178-00
U116	156-0061-00			MICROCIRCUIT,DI:SGL,BCD TO DEC DECODER	01295	SN7442(N OR J)
U117	156-0916-00			MICROCIRCUIT,DI:EIGHT 2-INP 3-STATE BFR	80009	156-0916-00
U118	156-0535-00			MICROCIRCUIT,DI:TRI-STATE HEX BUFF	27014	DM8097M
U119	156-0531-00			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR	27014	DM8833N
U120	156-0531-00			MICROCIRCUIT,DI:QUAD UNIFIED BUS XCVR	27014	DM8833N
U121	156-0427-00			MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
U122	156-0427-00			MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
U123	156-0427-00			MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
U125	156-0849-00			MICROCIRCUIT,DI:QUAD INTERFACE BUS XSVR	80009	156-0849-00
U212	160-0177-00			MICROCIRCUIT,DI:1024 X 8 STATIC,PRGM	80009	160-0177-00
U213	160-0176-00			MICROCIRCUIT,DI:1024 X 8 STATIC,PRGM	80009	160-0176-00
U214	160-0175-00			MICROCIRCUIT,DI:1024 X 8 STATIC,PRGM	80009	160-0175-00
U215	160-0174-00			MICROCIRCUIT,DI:1024 X 8 STATIC,PRGM	80009	160-0174-00
U216	156-0078-00			MICROCIRCUIT,DI:1 OF 16 DECODER-DEMUX	80009	156-0078-00
U217	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U218	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0385-00
U219	156-0535-00			MICROCIRCUIT,DI:TRI-STATE HEX BUFF	27014	DM8097M
U220	156-0426-00			MICROCIRCUIT,DI:MICROPROCESSOR	04713	MC6800S
U225	156-0849-00			MICROCIRCUIT,DI:QUAD INTERFACE BUS XSVR	80009	156-0849-00
U310	156-0402-00			MICROCIRCUIT,LI:TIMER	27014	LM555CN
U311	156-0139-00			MICROCIRCUIT,LI:DUAL LINE DRIVER	01295	SN75150P
U312	156-0285-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	27014	LM340T-12
U313	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00(N OR J)
U314	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00(N OR J)
U315	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00(N OR J)
U316	156-0464-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	07263	74LS20PC OR DC
U317	156-0464-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	07263	74LS20PC OR DC
U318	156-0535-00			MICROCIRCUIT,DI:TRI-STATE HEX BUFF	27014	DM8097M

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U319	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0145-00
U320	156-0535-00			MICROCIRCUIT,DI:TRI-STATE HEX BUFF	27014	DM8097M
U321	156-0138-00			MICROCIRCUIT,LI:CORE LINE RECEIVER	01295	SN75154N
U322	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	80009	156-0383-00
U323	156-0480-00			MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	01295	SN74LS08(N OR J)
U324	156-0849-00			MICROCIRCUIT,DI:QUAD INTERFACE BUS XSVR	80009	156-0849-00
U325	156-0849-00			MICROCIRCUIT,DI:QUAD INTERFACE BUS XSVR	80009	156-0849-00
U413	156-0041-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U414	156-0718-00			MICROCIRCUIT,DI:TRIPLE 3-INP POS-NOR GATES	80009	156-0718-00
U418	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U420	156-0206-00			MICROCIRCUIT,DI:DUAL SCE/SINK MEM DRVR PR	01295	SN75325(N OR J)
Y416	158-0056-00			XTAL UNIT,QTZ:4MHZ,0.003%,SEERIES	34630	150-6070

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 *Name & Description*

Assembly and/or Component
Attaching parts for Assembly and/or Component
**** END ATTACHING PARTS ****
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
**** END ATTACHING PARTS ****
Parts of Detail Part
Attaching parts for Parts of Detail Part
**** END ATTACHING PARTS ****

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

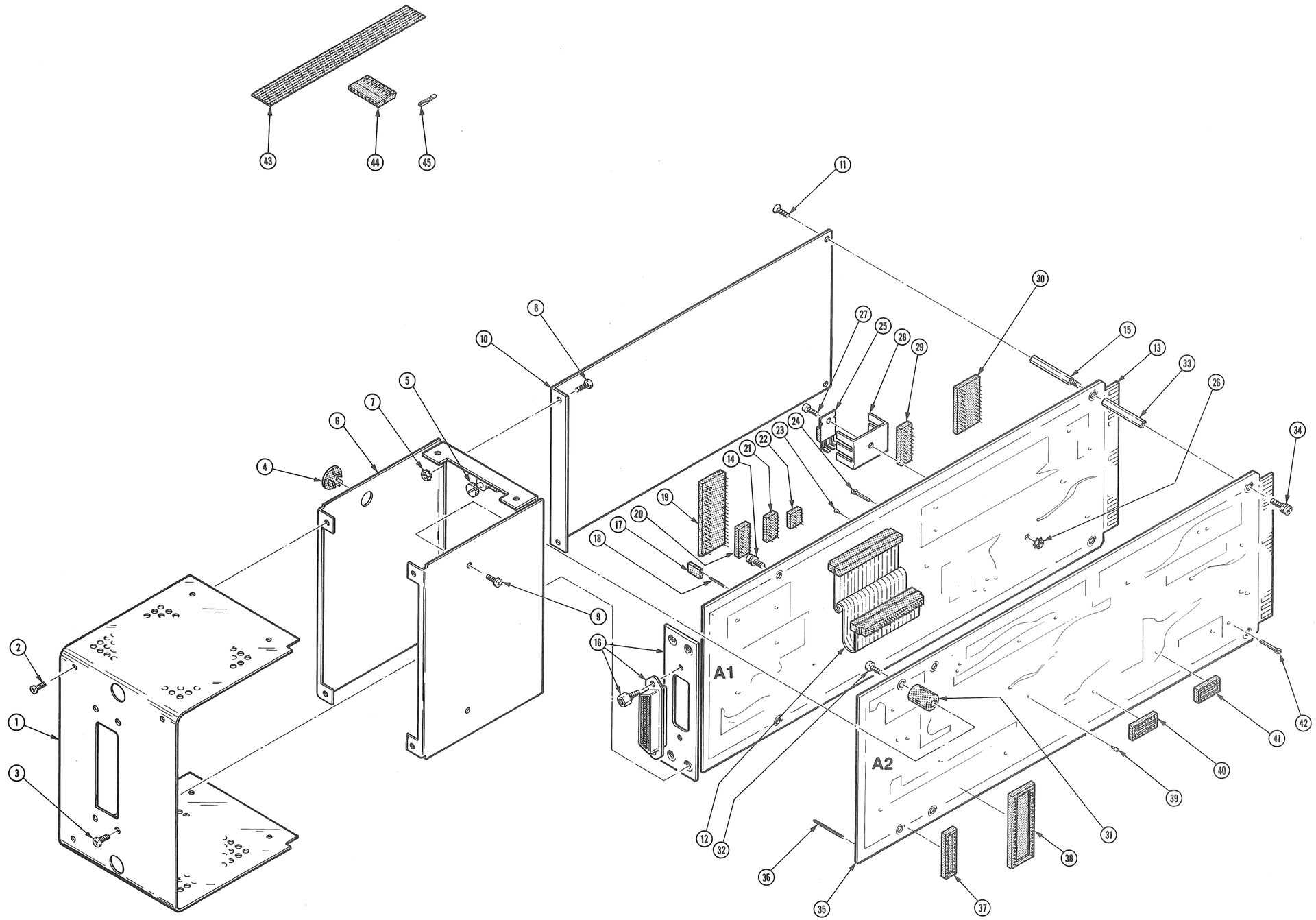
CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
04919	COMPONENT MFG SERVICE INC	1 COMPONENT PARK	WEST BRIDGEWATER MA 02379
05820	EG AND G WAKEFIELD ENGINEERING	60 AUDUBON RD	WAKEFIELD MA 01880
06540	WITE CORP AMATOM ELECTRONIC HARDWARE DIV	446 BLAKE ST	NEW HAVEN CT 06515
08261	SPECTRA-STRIP AN ELTRA CO	7100 LAMPSON AVE	GARDEN GROVE CA 92642
09922	BURNDY CORP	RICHARDS AVE	NORWALK CT 06852
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS	30 HUNTER LANE	CAMP HILL PA 17011
74868	AMPHENOL R F OPERATIONS AN ALLIED CO	33 E FRANKLIN ST	DANBURY CT 06810
77900	SHAKEPROOF DIV OF ILLINOIS TOOL WORKS	SAINT CHARLES RD	ELGIN IL 60120
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF DIVISION	ST CHARLES ROAD	ELGIN IL 60120
80009	TEKTRONIX INC	4900 S W GRIFFITH DR P O BOX 500	BEAVERTON OR 97077
93907	TEXTRON INC CAMCAR DIV	600 18TH AVE	ROCKFORD IL 61101
TK0435	LEWIS SCREW CO	4114 S PEORIA	CHICAGO IL 60609

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-1	380-0499-00			1	HSG HALF,CONN:FRONT,NYLON	80009	380-0499-00
					(ATTACHING PARTS)		
-2	211-0008-00			8	SCREW,MACHINE:4-40 X 0.25,PNH,STL	93907	ORDER BY DESCR
-3	211-0504-00			4	SCREW,MACHINE:6-32 X 0.250,PNH,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-4	134-0067-00			1	BUTTON,PLUG:0.5 HOLE,GRAY PLASTIC	80009	134-0067-00
-5	214-1573-00			2	THUMBSCREW:6-32 X 0.656,0.312 OD,SST	06540	6130-SS-0632
-6	380-0511-00			1	HSG HALF,CONN:REAR,ALUMINUM	80009	380-0511-00
					(ATTACHING PARTS)		
-7	210-0586-00			2	NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
-8	211-0097-00			2	SCREW,MACHINE:4-40 X 0.312,PNH,STL	TK0435	ORDER BY DESCR
-9	211-0008-00			2	SCREW,MACHINE:4-40 X 0.25,PNH,STL	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-10	386-3778-00			1	SUPPORT,CKT BD:GPIB INTERFACE	80009	386-3778-00
					(ATTACHING PARTS)		
-11	211-0101-00			2	SCREW,MACHINE:4-40 X 0.25,FLH,100 DEG,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-12	198-3057-00			1	WIRE SET,ELEC:	80009	198-3057-00
-13	----- -----			1	CKT BOARD ASSY:MPU/GPIB(SEE A1 REPL)		
					(ATTACHING PARTS)		
-14	211-0116-00			2	SCR,ASSEM WSHR:4-40 X 0.312,PNH,BRS,NP,POZ	77900	ORDER BY DESCR
-15	129-0661-00			2	SPACER,POST:1.213 L,4-40 INT/EXT,AL,0.188 H EX	80009	129-0661-00
					(END ATTACHING PARTS)		
					.CKT BOARD ASSY INCLUDES:		
-16	386-3370-01			1	.PLATE,CONN MTG:REAR,W/HARDWARE	80009	386-3370-01
-17	131-0993-00			1	.BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
-18	131-0608-00			54	.TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
-19	136-0623-00			4	.SKT,PL-IN ELEK:CMPNT,40 DIP,LOW PROFILE	09922	DILB40P-108
-20	136-0260-02			13	.SKT,PL-IN ELEK:MICROCKT,16 DIP,LOW CL	09922	DILB16P-108T
-21	136-0269-02			14	.SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP	09922	DILB14P-108T
-22	136-0514-00			2	.SKT,PL-IN ELEK:MICROCIRCUIT,8 DIP	09922	DILB8P-108
-23	136-0252-07			3	.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-24	214-0579-00			5	.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-25	----- -----			1	.MICROCIRCUIT:(SEE U312 REPL)		
					.(ATTACHING PARTS)		
-26	210-0586-00			1	.NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
-27	211-0097-00			1	.SCREW,MACHINE:4-40 X 0.312,PNH,STL	TK0435	ORDER BY DESCR
					.(END ATTACHING PARTS)		
-28	214-1967-00			1	.HEAT SINK,DIODE:(2)0.15 DIA HOLES,AL	05820	289-AB
-29	136-0634-00			1	.SKT,PL-IN ELEK:MICROCIRCUIT,20 DIP	09922	DILB20P-108
-30	136-0578-00			13	.SKT,PL-IN ELEK:MICROCIRCUIT,24 DIP,LOW PF	09922	DILB24P-108
-31	129-0466-00			2	SPACER,POST:0.575 L,4-40,NYLON,0.375 OD	80009	129-0466-00
					(ATTACHING PARTS)		
-32	211-0116-00			2	SCR,ASSEM WSHR:4-40 X 0.312,PNH,BRS,NP,POZ	77900	ORDER BY DESCR
					(END ATTACHING PARTS)		
-33	129-0662-00			4	SPACER,POST:1.188 L,4-40 EA END,AL,0.188 HEX	80009	129-0662-00
					(ATTACHING PARTS)		
-34	211-0116-00			4	SCR,ASSEM WSHR:4-40 X 0.312,PNH,BRS,NP,POZ	77900	ORDER BY DESCR
					(END ATTACHING PARTS)		
-35	----- -----			1	CKT BOARD ASSY:PIA/7001(SEE A2 REPL)		
-36	131-0608-00			42	.TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
-37	136-0578-00			4	.SKT,PL-IN ELEK:MICROCIRCUIT,24 DIP,LOW PF	09922	DILB24P-108
-38	136-0623-00			3	.SKT,PL-IN ELEK:CMPNT,40 DIP,LOW PROFILE	09922	DILB40P-108
-39	136-0252-07			6	.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-40	136-0260-02			8	.SKT,PL-IN ELEK:MICROCKT,16 DIP,LOW CL	09922	DILB16P-108T
-41	136-0269-02			20	.SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP	09922	DILB14P-108T
-42	214-0579-00			2	.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-43	175-0830-00			AR	CABLE,SP,ELEC:7,26 AWG,STRD,PVC JKT,RBN	08261	111-2699-972
-44	352-0166-00			2	HLDR,TERM CONN:8 WIRE,BLACK	80009	352-0166-00
-45	131-0707-00			16	CONTACT,ELEC:22-26 AWG,BRS,CU BE GLD PL	22526	47439-000
					STANDARD ACCESSORIES		
	070-2623-00			1	MANUAL,TECH:INSTR	80009	070-2623-00
	012-0630-01	B010100	B010273	1	CABLE,INTCON:2.0M L	04919	2024-2
	012-0630-03	B010274		1	CABLE,INTCON:2.0M L	74868	AC30147-102

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-	012-0630-01	B010100	B100795	1	CABLE,INTCON:2.0W L (OPTION 31 ONLY)	04919	2024-2
	012-0630-03	B100796		1	CABLE,INTCON:2.0W L (OPTION 31 ONLY)	74868	AC30147-102

FIG. 1 EXPLODED



MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC6800

(0 to 70°C; L or P Suffix)

MC6800C

(-40 to 85°C; L Suffix only)

MICROPROCESSING UNIT (MPU)

The MC6800 is a monolithic 8-bit microprocessor forming the central control function for Motorola's M6800 family. Compatible with TTL, the MC6800, as with all M6800 system parts, requires only one +5.0-volt power supply, and no external TTL devices for bus interface.

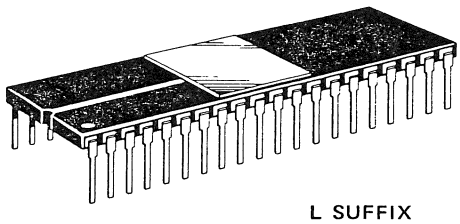
The MC6800 is capable of addressing 65K bytes of memory with its 16-bit address lines. The 8-bit data bus is bidirectional as well as 3-state, making direct memory addressing and multiprocessing applications realizable.

- Eight-Bit Parallel Processing
- Bi-Directional Data Bus
- Sixteen-Bit Address Bus — 65K Bytes of Addressing
- 72 Instructions — Variable Length
- Seven Addressing Modes — Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- Maskable Interrupt Vector
- Separate Non-Maskable Interrupt — Internal Registers Saved In Stack
- Six Internal Registers — Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Addressing (DMA) and Multiple Processor Capability
- Clock Rates as High as 1 MHz
- Simple Bus Interface Without TTL
- Halt and Single Instruction Execution Capability

MOS

(N-CHANNEL, SILICON-GATE)

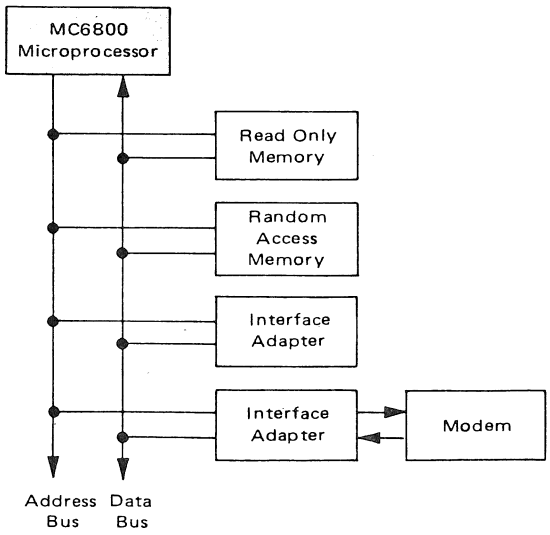
MICROPROCESSOR



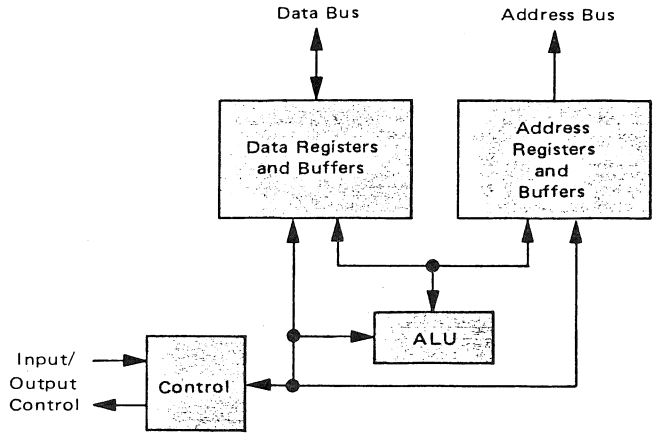
L SUFFIX
CERAMIC PACKAGE
CASE 715

NOT SHOWN: **P SUFFIX**
PLASTIC PACKAGE
CASE 711

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MC6800 MICROPROCESSOR BLOCK DIAGRAM



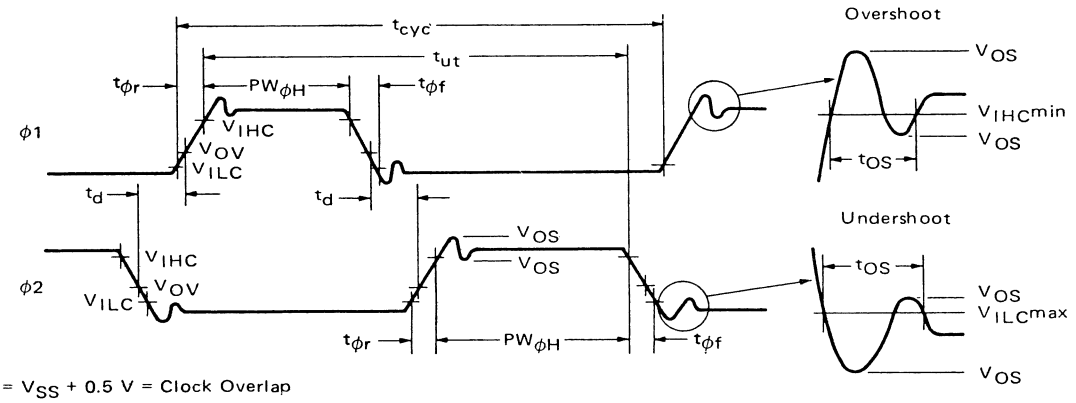
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	Logic	V_{IH}	V_{SS} + 2.0	–	V_{CC}	Vdc
	$\phi1,\phi2$	V_{IHC}	V_{CC} – 0.3	–	V_{CC} + 0.1	
Input Low Voltage	Logic	V_{IL}	V_{SS} – 0.3	–	V_{SS} + 0.8	Vdc
	$\phi1,\phi2$	V_{ILC}	V_{SS} – 0.1	–	V_{SS} + 0.3	
Clock Overshoot/Undershoot – Input High Level		V_{OS}	V_{CC} – 0.5	–	V_{CC} + 0.5	Vdc
– Input Low Level			V_{SS} – 0.5	–	V_{SS} + 0.5	
Input Leakage Current		I_{in}				μAdc
(V_{in} = 0 to 5.25 V, V_{CC} = max)	Logic*		–	1.0	2.5	
(V_{in} = 0 to 5.25 V, V_{CC} = 0.0 V)	$\phi1,\phi2$		–	–	100	
Three-State (Off State) Input Current	D0-D7	I_{TSI}	–	2.0	10	μAdc
(V_{in} 0.4 to 2.4 V, V_{CC} = max)	A0-A15,R/W		–	–	100	
Output High Voltage		V_{OH}				Vdc
(I_{Load} = –205 μAdc, V_{CC} = min)	D0-D7		V_{SS} + 2.4	–	–	
(I_{Load} = –145 μAdc, V_{CC} = min)	A0-A15,R/W,VMA		V_{SS} + 2.4	–	–	
(I_{Load} = –100 μAdc, V_{CC} = min)	BA		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mAdc, V_{CC} = min)		V_{OL}	–	–	V_{SS} + 0.4	Vdc
Power Dissipation		P_D	–	0.600	1.2	W
Capacitance #	$\phi1,\phi2$	C_{in}	80	120	160	pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	TSC		–	–	15	
	DBE		–	7.0	10	
	D0-D7		–	10	12.5	
	Logic Inputs		–	6.5	8.5	
	A0-A15,R/W,VMA	C_{out}	–	–	12	pF
Frequency of Operation		f	0.1	–	1.0	MHz
Clock Timing (Figure 1)						
Cycle Time		t_{cyc}	1.0	–	10	μs
Clock Pulse Width		$PW_{\phi H}$				ns
(Measured at V_{CC} – 0.3 V)	$\phi1$		430	–	4500	
	$\phi2$		450	–	4500	
Total $\phi1$ and $\phi2$ Up Time		t_{ut}	940	–	–	ns
Rise and Fall Times	$\phi1,\phi2$	$t_{\phi r}$, $t_{\phi f}$	5.0	–	50	ns
(Measured between V_{SS} + 0.3 V and V_{CC} – 0.3 V)						
Delay Time or Clock Separation		t_d	0	–	9100	ns
(Measured at V_{OV} = V_{SS} + 0.5 V)						
Overshoot Duration		t_{OS}	0	–	40	ns

*Except $\overline{IRQ}$ and $\overline{NMI}$, which require 3 kΩ pullup load resistors for wire-OR capability at optimum operation.

#Capacitances are periodically sampled rather than 100% tested.

FIGURE 1 – CLOCK TIMING WAVEFORM



V_{OV} = V_{SS} + 0.5 V = Clock Overlap measurement point

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Thermal Resistance	θ_{JA}	70	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

READ/WRITE TIMING Figures 2 and 3, f = 1.0 MHz, Load Circuit of Figure 6.

Characteristic	Symbol	Min	Typ	Max	Unit
Address Delay	t_{AD}	–	220	300	ns
Peripheral Read Access Time $t_{acc} = t_{ut} - (t_{AD} + t_{DSR})$	t_{acc}	–	–	540	ns
Data Setup Time (Read)	t_{DSR}	100	–	–	ns
Input Data Hold Time	t_H	10	–	–	ns
Output Data Hold Time	t_H	10	25	–	ns
Address Hold Time (Address, R/W, VMA)	t_{AH}	50	75	–	ns
Enable High Time for DBE Input	t_{EH}	450	–	–	ns
Data Delay Time (Write)	t_{DDW}	–	165	225	ns
Processor Controls*					
Processor Control Setup Time	t_{PCS}	200	–	–	ns
Processor Control Rise and Fall Time	t_{PCr}, t_{PCf}	–	–	100	ns
Bus Available Delay	t_{BA}	–	–	300	ns
Three State Enable	t_{TSE}	–	–	40	ns
Three State Delay	t_{TSD}	–	–	700	ns
Data Bus Enable Down Time During $\phi 1$ Up Time (Figure 3)	$t_{\overline{DBE}}$	150	–	–	ns
Data Bus Enable Delay (Figure 3)	t_{DBED}	300	–	–	ns
Data Bus Enable Rise and Fall Times (Figure 3)	t_{DBEr}, t_{DBEf}	–	–	25	ns

*Additional information is given in Figures 12 through 16 of the Family Characteristics – see pages 17 through 20.

FIGURE 2 – READ DATA FROM MEMORY OR PERIPHERALS

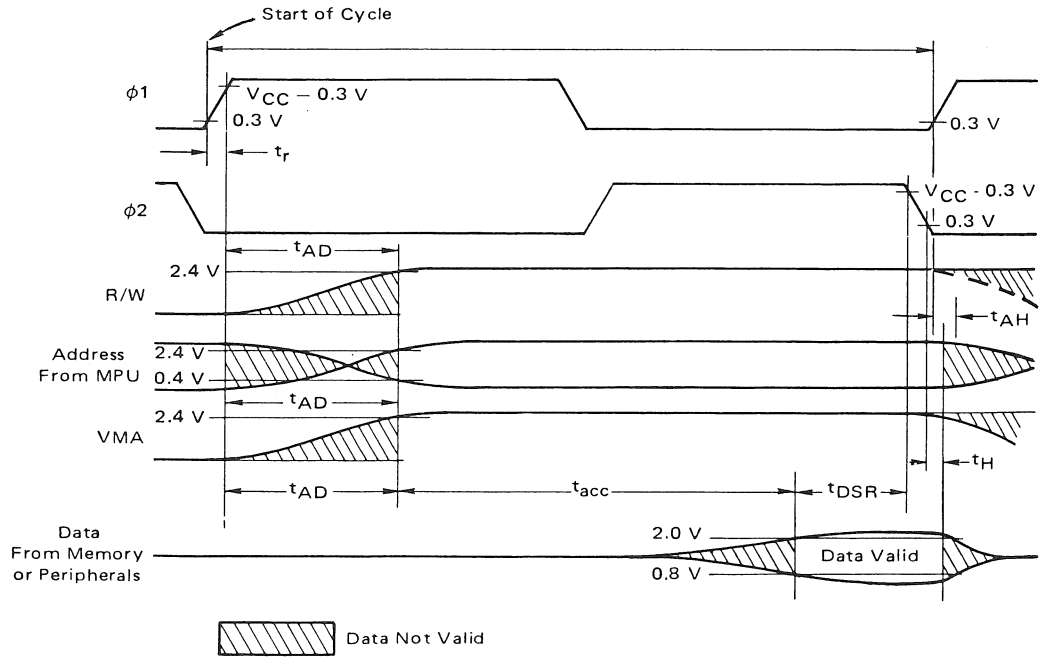


FIGURE 3 – WRITE IN MEMORY OR PERIPHERALS

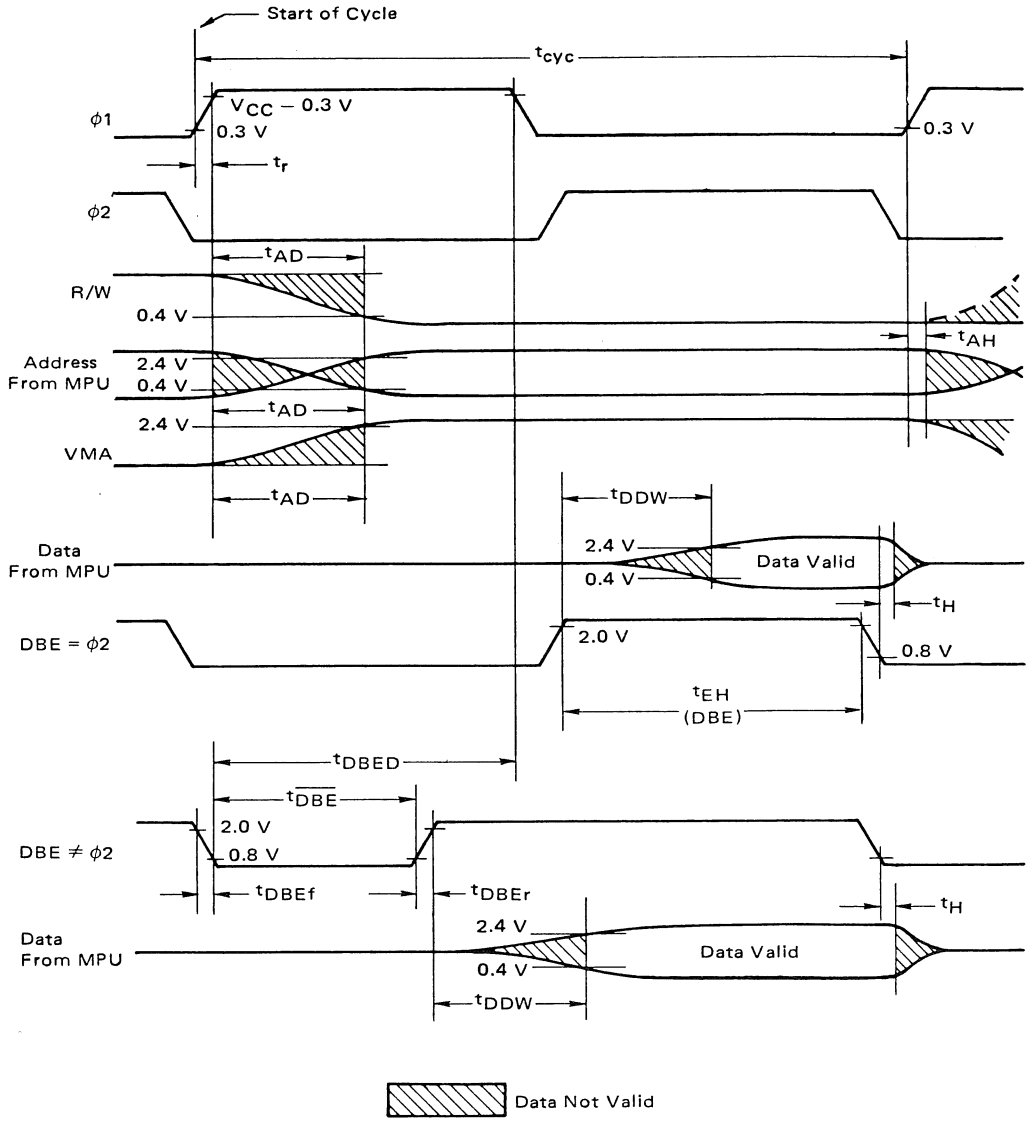


FIGURE 4 – TYPICAL DATA BUS OUTPUT DELAY versus CAPACITIVE LOADING

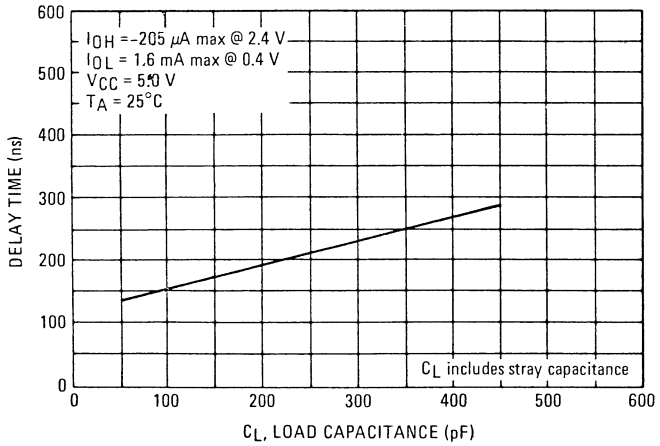


FIGURE 5 – TYPICAL READ/WRITE, VMA, AND ADDRESS OUTPUT DELAY versus CAPACITIVE LOADING

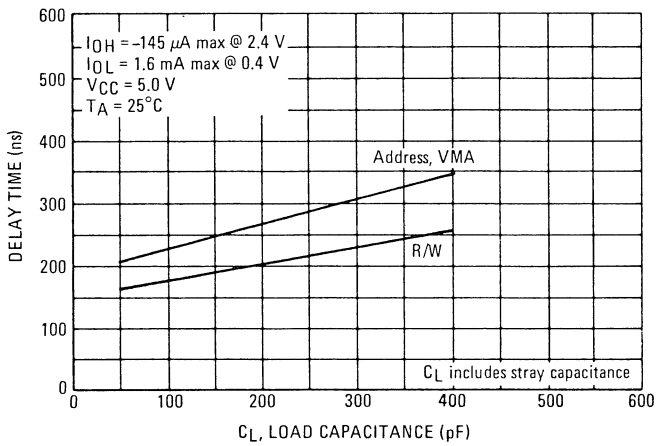
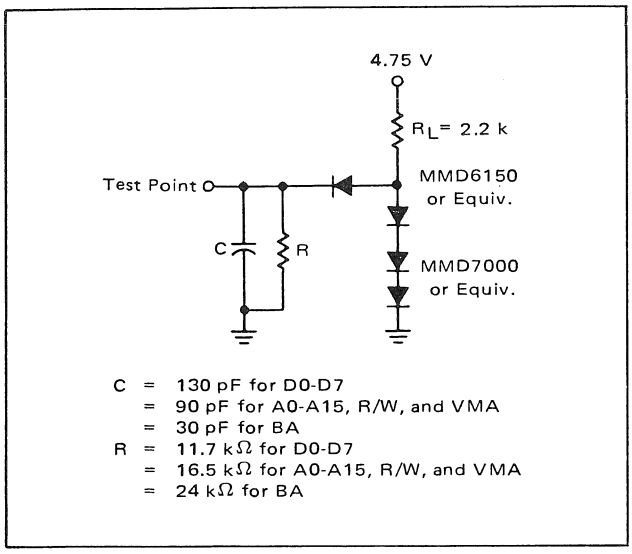


FIGURE 6 – BUS TIMING TEST LOAD



C = 130 pF for D0-D7
= 90 pF for A0-A15, R/W, and VMA
= 30 pF for BA
R = 11.7 kΩ for D0-D7
= 16.5 kΩ for A0-A15, R/W, and VMA
= 24 kΩ for BA

TYPICAL POWER SUPPLY CURRENT

FIGURE 7 – VARIATIONS WITH FREQUENCY

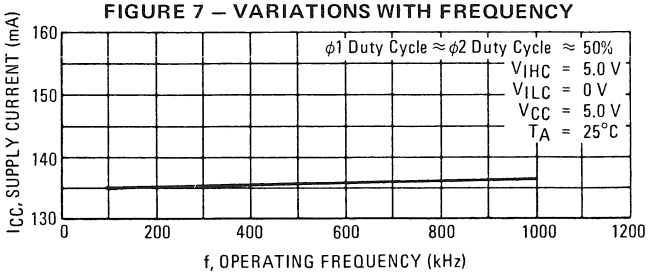
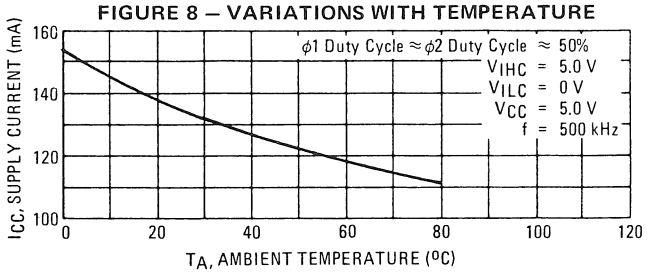
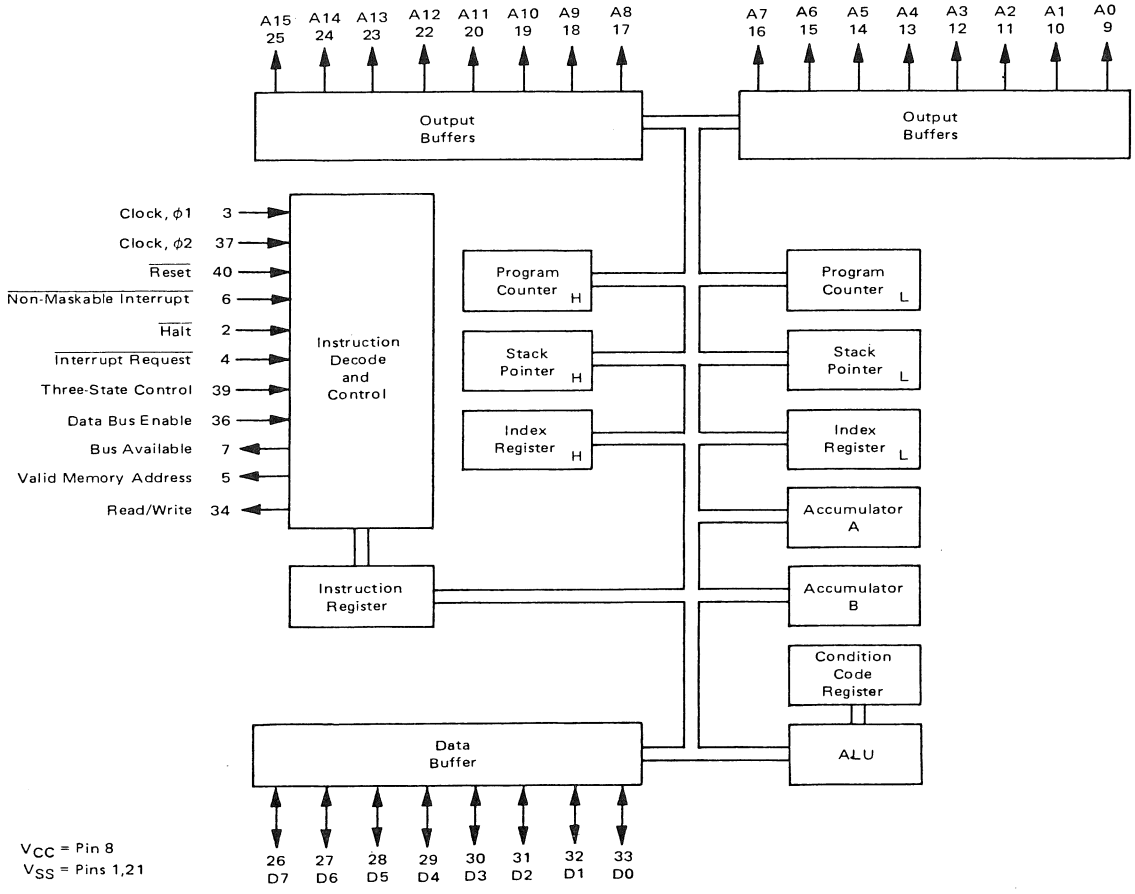


FIGURE 8 – VARIATIONS WITH TEMPERATURE



EXPANDED BLOCK DIAGRAM



V_{CC} = Pin 8
V_{SS} = Pins 1,21

MPU SIGNAL DESCRIPTION

Proper operation of the MPU requires that certain control and timing signals be provided to accomplish specific functions and that other signal lines be monitored to determine the state of the processor.

Clocks Phase One and Phase Two ($\phi 1, \phi 2$) — Two pins are used for a two-phase non-overlapping clock that runs at the V_{CC} voltage level.

Address Bus (A0-A15) — Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving one standard TTL load and 130 pF. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications.

Data Bus (D0-D7) — Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load and 130 pF.

$\overline{\text{Halt}}$ — When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a one level, Valid Memory Address will be at a zero, and all other three-state lines will be in the three-state mode.

Transition of the $\overline{\text{Halt}}$ line must not occur during the last 250 ns of phase one. To insure single instruction operation, the $\overline{\text{Halt}}$ line must go high for one Clock cycle.

Three-State Control (TSC) — This input causes all of the address lines and the Read/Write line to go into the off or high impedance state. This state will occur 700 ns after TSC = 2.0 V. The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The $\phi 1$ clock must be held in the high state and the $\phi 2$ in the low state for this function to operate properly. The address bus will then be available for other devices to directly address memory. Since the MPU is a dynamic device, it can be held in this state for only 4.5 μs or destruction of data will occur in the MPU.

Read/Write (R/W) — This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-State Control going high will turn Read/Write to the off (high impedance) state. Also, when the processor is halted, it will be in the off state. This output is capable of driving one standard TTL load and 90 pF.

Valid Memory Address (VMA) — This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 90 pF may be directly driven by this active high signal.

Data Bus Enable (DBE) — This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it would be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.

Bus Available (BA) — The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0) or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30 pF.

$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$) — This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The $\overline{\text{Halt}}$ line must be in the high state for interrupts to be serviced. Interrupts will be latched internally while $\overline{\text{Halt}}$ is low.

The $\overline{\text{IRQ}}$ has a high impedance pullup device internal to the chip; however a 3 kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

$\overline{\text{Reset}}$ — This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. If a high level is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$.

Figure 9 shows the initialization of the microprocessor after restart. $\overline{\text{Reset}}$ must be held low for at least eight clock periods after V_{CC} reaches 4.75 volts. If $\overline{\text{Reset}}$ goes high prior to the leading edge of $\phi 2$, on the next $\phi 1$ the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.

Non-Maskable Interrupt ($\overline{\text{NMI}}$) – A low-going edge on this input requests that a non-mask-interrupt sequence be generated within the processor. As with the $\overline{\text{Interrupt Request}}$ signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$.

The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory.

$\overline{\text{NMI}}$ has a high impedance pullup resistor internal to the chip; however a 3 kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupt lines that are sampled during $\phi 2$ and will start the interrupt routine on the $\phi 1$ following the completion of an instruction.

Figure 10 is a flow chart describing the major decision paths and interrupt vectors of the microprocessor. Table 1 gives the memory map for interrupt vectors.

FIGURE 9 – INITIALIZATION OF MPU AFTER RESTART

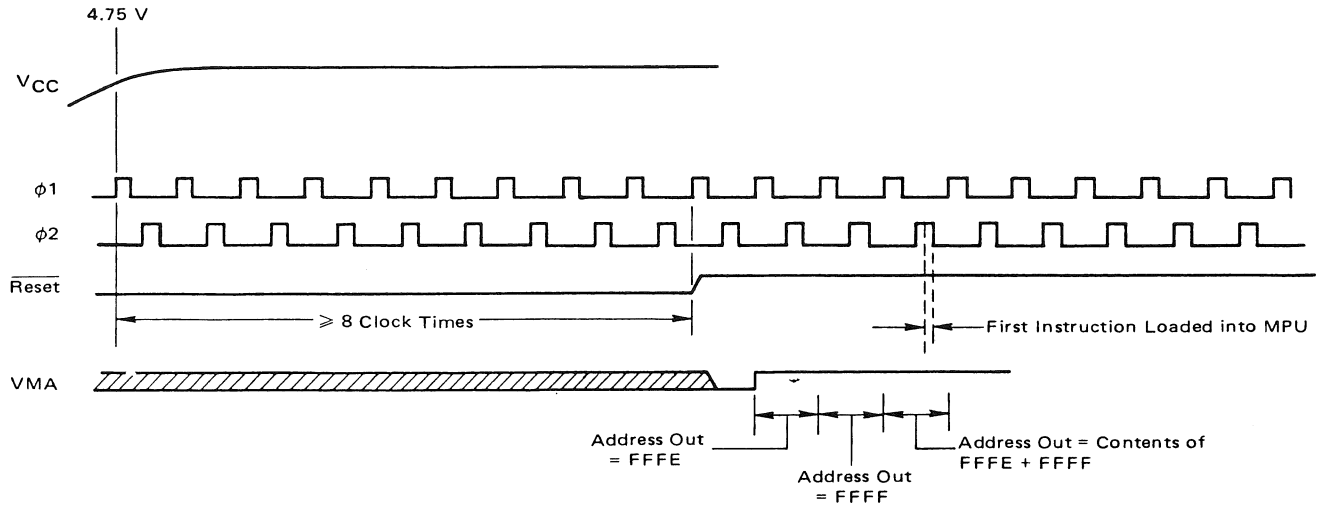
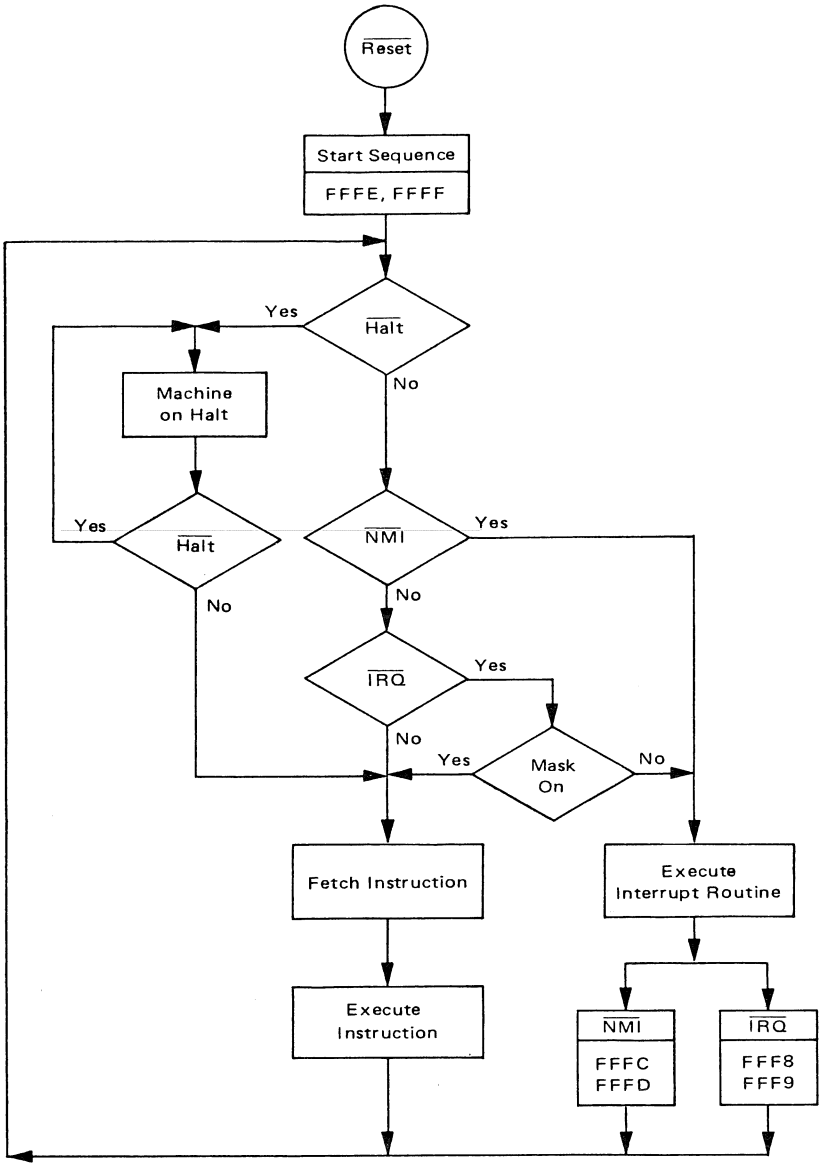


TABLE 1 – MEMORY MAP FOR INTERRUPT VECTORS

Vector MS	Vector LS	Description
FFFE	FFFF	Restart
FFFC	FFFD	Non-maskable Interrupt
FFFA	FFFB	Software Interrupt
FFF8	FFF9	Interrupt Request

FIGURE 10 – MPU FLOW CHART



MPU REGISTERS

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer (Figure 11).

Program Counter – The program counter is a two byte (16-bits) register that points to the current program address.

Stack Pointer – The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

Index Register – The index register is a two byte register that is used to store data or a sixteen bit memory address for the Indexed mode of memory addressing.

Accumulators – The MPU contains two 8-bit accumulators that are used to hold operands and results from an arithmetic logic unit (ALU).

FIGURE 11 – PROGRAMMING MODEL OF THE MICROPROCESSING UNIT

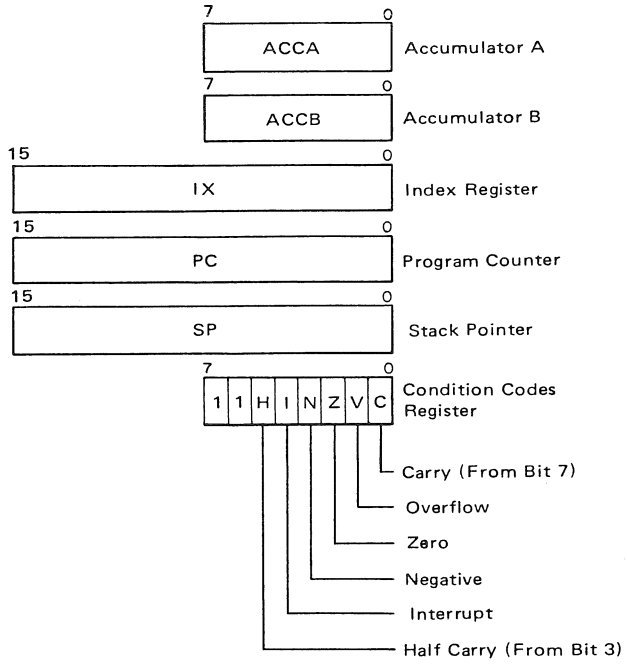
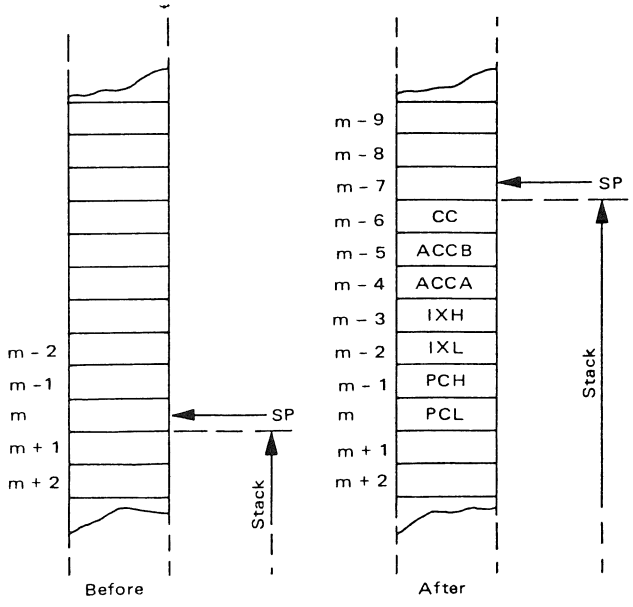


FIGURE 12 – SAVING THE STATUS OF THE MICROPROCESSOR IN THE STACK

SP = Stack Pointer
CC = Condition Codes (Also called the Processor Status Byte)
ACCB = Accumulator B
ACCA = Accumulator A
IXH = Index Register, Higher Order 8 Bits
IXL = Index Register, Lower Order 8 Bits
PCH = Program Counter, Higher Order 8 Bits
PCL = Program Counter, Lower Order 8 Bits



Condition Code Register — The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and half carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The unused bits of the Condition Code Register (b6 and b7) are ones.

Figure 12 shows the order of saving the microprocessor status within the stack.

MPU INSTRUCTION SET

The MC6800 has a set of 72 different instructions. Included are binary and decimal arithmetic, logical, shift, rotate, load, store, conditional or unconditional branch, interrupt and stack manipulation instructions (Tables 2 thru 6).

MPU ADDRESSING MODES

The MC6800 eight-bit microprocessing unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Table 7 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 1 MHz, these times would be microseconds.

Accumulator (ACCX) Addressing — In accumulator only addressing, either accumulator A or accumulator B is specified. These are one-byte instructions.

Immediate Addressing — In immediate addressing, the operand is contained in the second byte of the instruction except LDS and LDX which have the operand in the second and third bytes of the instruction. The MPU addresses this location when it fetches the immediate instruction for execution. These are two or three-byte instructions.

Direct Addressing — In direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in the machine i.e., locations zero through 255. Enhanced execution times are achieved by storing data in these locations. In most configurations, it should be a random access memory. These are two-byte instructions.

Extended Addressing — In extended addressing, the address contained in the second byte of the instruction is used as the higher eight-bits of the address of the operand. The third byte of the instruction is used as the lower eight-bits of the address for the operand. This is an absolute address in memory. These are three-byte instructions.

Indexed Addressing — In indexed addressing, the address contained in the second byte of the instruction is added to the index register's lowest eight bits in the MPU. The carry is then added to the higher order eight bits of the index register. This result is then used to address memory. The modified address is held in a temporary address register so there is no change to the index register. These are two-byte instructions.

Implied Addressing — In the implied addressing mode the instruction gives the address (i.e., stack pointer, index register, etc.). These are one-byte instructions.

Relative Addressing — In relative addressing, the address contained in the second byte of the instruction is added to the program counter's lowest eight bits plus two. The carry or borrow is then added to the high eight bits. This allows the user to address data within a range of -125 to +129 bytes of the present instruction. These are two-byte instructions.

TABLE 2 — MICROPROCESSOR INSTRUCTION SET — ALPHABETIC SEQUENCE

ABA	Add Accumulators
ADC	Add with Carry
ADD	Add
AND	Logical And
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
BCC	Branch if Carry Clear
BCS	Branch if Carry Set
BEQ	Branch if Equal to Zero
BGE	Branch if Greater or Equal Zero
BGT	Branch if Greater than Zero
BHI	Branch if Higher
BIT	Bit Test
BLE	Branch if Less or Equal
BLS	Branch if Lower or Same
BLT	Branch if Less than Zero
BMI	Branch if Minus
BNE	Branch if Not Equal to Zero
BPL	Branch if Plus
BRA	Branch Always
BSR	Branch to Subroutine
BVC	Branch if Overflow Clear
BVS	Branch if Overflow Set
CBA	Compare Accumulators
CLC	Clear Carry
CLI	Clear Interrupt Mask
CLR	Clear
CLV	Clear Overflow
CMP	Compare
COM	Complement
CPX	Compare Index Register
DAA	Decimal Adjust
DEC	Decrement
DES	Decrement Stack Pointer
DEX	Decrement Index Register
EOR	Exclusive OR
INC	Increment
INS	Increment Stack Pointer
INX	Increment Index Register
JMP	Jump
JSR	Jump to Subroutine
LDA	Load Accumulator
LDS	Load Stack Pointer
LDX	Load Index Register
LSR	Logical Shift Right
NEG	Negate
NOP	No Operation
ORA	Inclusive OR Accumulator
PSH	Push Data
PUL	Pull Data
ROL	Rotate Left
ROR	Rotate Right
RTI	Return from Interrupt
RTS	Return from Subroutine
SBA	Subtract Accumulators
SBC	Subtract with Carry
SEC	Set Carry
SEI	Set Interrupt Mask
SEV	Set Overflow
STA	Store Accumulator
STS	Store Stack Register
STX	Store Index Register
SUB	Subtract
SWI	Software Interrupt
TAB	Transfer Accumulators
TAP	Transfer Accumulators to Condition Code Reg.
TBA	Transfer Accumulators
TPA	Transfer Condition Code Reg. to Accumulator
TST	Test
TSX	Transfer Stack Pointer to Index Register
TXS	Transfer Index Register to Stack Pointer
WAI	Wait for Interrupt

TABLE 3 – ACCUMULATOR AND MEMORY INSTRUCTIONS

OPERATIONS	MNEMONIC	IMMED OP	IMMED ~	IMMED =	DIRECT OP	DIRECT ~	DIRECT =	INDEX OP	INDEX ~	INDEX =	EXTND OP	EXTND ~	EXTND =	IMPLIED OP	IMPLIED ~	IMPLIED =	BOOLEAN/ARITHMETIC OPERATION (All register labels refer to contents)	5 H	4 I	3 N	2 Z	1 V	0 C
Add	ADDA	8B	2	2	9B	3	2	AB	5	2	BB	4	3				A + M → A	↕	•	↕	↕	↕	↕
	ADDB	CB	2	2	DB	3	2	EB	5	2	FB	4	3				B + M → B	↕	•	↕	↕	↕	↕
Add Acmltrs	ABA													1B	2	1	A + B → A	↕	•	↕	↕	↕	↕
Add with Carry	ADCA	89	2	2	99	3	2	A9	5	2	B9	4	3				A + M + C → A	↕	•	↕	↕	↕	↕
	ADCB	C9	2	2	D9	3	2	E9	5	2	F9	4	3				B + M + C → B	↕	•	↕	↕	↕	↕
And	ANDA	84	2	2	94	3	2	A4	5	2	B4	4	3				A · M → A	•	•	↕	↕	R	•
	ANDB	C4	2	2	D4	3	2	E4	5	2	F4	4	3				B · M → B	•	•	↕	↕	R	•
Bit Test	BITA	85	2	2	95	3	2	A5	5	2	B5	4	3				A · M	•	•	↕	↕	R	•
	BITB	C5	2	2	D5	3	2	E5	5	2	F5	4	3				B · M	•	•	↕	↕	R	•
Clear	CLR							6F	7	2	7F	6	3				00 → M	•	•	R	S	R	R
	CLRA													4F	2	1	00 → A	•	•	R	S	R	R
	CLRB													5F	2	1	00 → B	•	•	R	S	R	R
Compare	CMPA	81	2	2	91	3	2	A1	5	2	B1	4	3				A – M	•	•	↕	↕	↕	↕
	CMPB	C1	2	2	D1	3	2	E1	5	2	F1	4	3				B – M	•	•	↕	↕	↕	↕
Compare Acmltrs	CBA													11	2	1	A – B	•	•	↕	↕	↕	↕
Complement, 1's	COM							63	7	2	73	6	3				M̄ → M	•	•	↕	↕	R	S
	COMA													43	2	1	Ā → A	•	•	↕	↕	R	S
	COMB													53	2	1	B̄ → B	•	•	↕	↕	R	S
Complement, 2's (Negate)	NEG							60	7	2	70	6	3				00 – M → M	•	•	↕	↕	①	②
	NEGA													40	2	1	00 – A → A	•	•	↕	↕	①	②
	NEGB													50	2	1	00 – B → B	•	•	↕	↕	①	②
Decimal Adjust, A	DAA													19	2	1	Converts Binary Add. of BCD Characters into BCD Format	•	•	↕	↕	↕	③
Decrement	DEC							6A	7	2	7A	6	3				M – 1 → M	•	•	↕	↕	4	•
	DECA													4A	2	1	A – 1 → A	•	•	↕	↕	4	•
	DECB													5A	2	1	B – 1 → B	•	•	↕	↕	4	•
Exclusive OR	EORA	88	2	2	98	3	2	A8	5	2	B8	4	3				A⊕M → A	•	•	↕	↕	R	•
	EORB	C8	2	2	D8	3	2	E8	5	2	F8	4	3				B⊕M → B	•	•	↕	↕	R	•
Increment	INC							6C	7	2	7C	6	3				M + 1 → M	•	•	↕	↕	⑤	•
	INCA													4C	2	1	A + 1 → A	•	•	↕	↕	⑤	•
	INCB													5C	2	1	B + 1 → B	•	•	↕	↕	⑤	•
Load Acmltr	LDAA	86	2	2	96	3	2	A6	5	2	B6	4	3				M → A	•	•	↕	↕	R	•
	LDAB	C6	2	2	D6	3	2	E6	5	2	F6	4	3				M → B	•	•	↕	↕	R	•
Or, Inclusive	ORAA	8A	2	2	9A	3	2	AA	5	2	BA	4	3				A + M → A	•	•	↕	↕	R	•
	ORAB	CA	2	2	DA	3	2	EA	5	2	FA	4	3				B + M → B	•	•	↕	↕	R	•
Push Data	PSHA													36	4	1	A → M_{SP}, SP – 1 → SP	•	•	•	•	•	•
	PSHB													37	4	1	B → M_{SP}, SP – 1 → SP	•	•	•	•	•	•
Pull Data	PULA													32	4	1	SP + 1 → SP, M_{SP} → A	•	•	•	•	•	•
	PULB													33	4	1	SP + 1 → SP, M_{SP} → B	•	•	•	•	•	•
Rotate Left	ROL							69	7	2	79	6	3				M	•	•	↕	↕	⑥	↕
	ROLA													49	2	1	A	•	•	↕	↕	⑥	↕
	ROLB													59	2	1	B	•	•	↕	↕	⑥	↕
Rotate Right	ROR							66	7	2	76	6	3				M	•	•	↕	↕	⑥	↕
	RORA													46	2	1	A	•	•	↕	↕	⑥	↕
	RORB													56	2	1	B	•	•	↕	↕	⑥	↕
Shift Left, Arithmetic	ASL							68	7	2	78	6	3				M	•	•	↕	↕	⑥	↕
	ASLA													48	2	1	A	•	•	↕	↕	⑥	↕
	ASLB													58	2	1	B	•	•	↕	↕	⑥	↕
Shift Right, Arithmetic	ASR							67	7	2	77	6	3				M	•	•	↕	↕	⑥	↕
	ASRA													47	2	1	A	•	•	↕	↕	⑥	↕
	ASRB													57	2	1	B	•	•	↕	↕	⑥	↕
Shift Right, Logic	LSR							64	7	2	74	6	3				M	•	•	R	↕	⑥	↕
	LSRA													44	2	1	A	•	•	R	↕	⑥	↕
	LSRB													54	2	1	B	•	•	R	↕	⑥	↕
Store Acmltr.	STAA				97	4	2	A7	6	2	B7	5	3				A → M	•	•	↕	↕	R	•
	STAB				D7	4	2	E7	6	2	F7	5	3				B → M	•	•	↕	↕	R	•
Subtract	SUBA	80	2	2	90	3	2	A0	5	2	B0	4	3				A – M → A	•	•	↕	↕	↕	↕
	SUBB	C0	2	2	D0	3	2	E0	5	2	F0	4	3				B – M → B	•	•	↕	↕	↕	↕
Subtract Acmltrs.	SBA													10	2	1	A – B → A	•	•	↕	↕	↕	↕
Subtr. with Carry	SBCA	82	2	2	92	3	2	A2	5	2	B2	4	3				A – M – C → A	•	•	↕	↕	↕	↕
	SBCB	C2	2	2	D2	3	2	E2	5	2	F2	4	3				B – M – C → B	•	•	↕	↕	↕	↕
Transfer Acmltrs	TAB													16	2	1	A → B	•	•	↕	↕	R	•
	TBA													17	2	1	B → A	•	•	↕	↕	R	•
Test, Zero or Minus	TST							6D	7	2	7D	6	3				M – 00	•	•	↕	↕	R	R
	TSTA													4D	2	1	A – 00	•	•	↕	↕	R	R
	TSTB													5D	2	1	B – 00	•	•	↕	↕	R	R
																		H	I	N	Z	V	C

LEGEND:

- OP Operation Code (Hexadecimal);
- ~ Number of MPU Cycles;
- = Number of Program Bytes;
- + Arithmetic Plus;
- – Arithmetic Minus;
- · Boolean AND;
- M_{SP} Contents of memory location pointed to be Stack Pointer;
- + Boolean Inclusive OR;
- ⊕ Boolean Exclusive OR;
- M̄ Complement of M;
- → Transfer Into;
- 0 Bit = Zero;
- 00 Byte = Zero;

Note – Accumulator addressing mode instructions are included in the column for IMPLIED addressing

CONDITION CODE SYMBOLS:

- H Half-carry from bit 3;
- I Interrupt mask
- N Negative (sign bit)
- Z Zero (byte)
- V Overflow, 2's complement
- C Carry from bit 7
- R Reset Always
- S Set Always
- ↕ Test and set if true, cleared otherwise
- • Not Affected

TABLE 4 – INDEX REGISTER AND STACK MANIPULATION INSTRUCTIONS

		IMMED			DIRECT			INDEX			EXTND			IMPLIED				COND. CODE REG.						
																		5	4	3	2	1	0
POINTER OPERATIONS	MNEMONIC	OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~	#	BOOLEAN/ARITHMETIC OPERATION	H	I	N	Z	V	C
Compare Index Reg	CPX	8C	3	3	9C	4	2	AC	6	2	BC	5	3				$X_H - M, X_L - (M+1)$	•	•	⑦	↕	⑧	•
Decrement Index Reg	DEX													09	4	1	$X - 1 \rightarrow X$	•	•	•	↕	•	•
Decrement Stack Pntr	DES													34	4	1	$SP - 1 \rightarrow SP$	•	•	•	•	•	•
Increment Index Reg	INX													08	4	1	$X + 1 \rightarrow X$	•	•	•	↕	•	•
Increment Stack Pntr	INS													31	4	1	$SP + 1 \rightarrow SP$	•	•	•	•	•	•
Load Index Reg	LDX	CE	3	3	DE	4	2	EE	6	2	FE	5	3				$M \rightarrow X_H, (M+1) \rightarrow X_L$	•	•	⑨	↕	R	•
Load Stack Pntr	LDS	8E	3	3	9E	4	2	AE	6	2	BE	5	3				$M \rightarrow SP_H, (M+1) \rightarrow SP_L$	•	•	⑨	↕	R	•
Store Index Reg	STX				DF	5	2	EF	7	2	FF	6	3				$X_H \rightarrow M, X_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Store Stack Pntr	STS				9F	5	2	AF	7	2	BF	6	3				$SP_H \rightarrow M, SP_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Indx Reg → Stack Pntr	TXS													35	4	1	$X - 1 \rightarrow SP$	•	•	•	•	•	•
Stack Pntr → Indx Reg	TSX													30	4	1	$SP + 1 \rightarrow X$	•	•	•	•	•	•

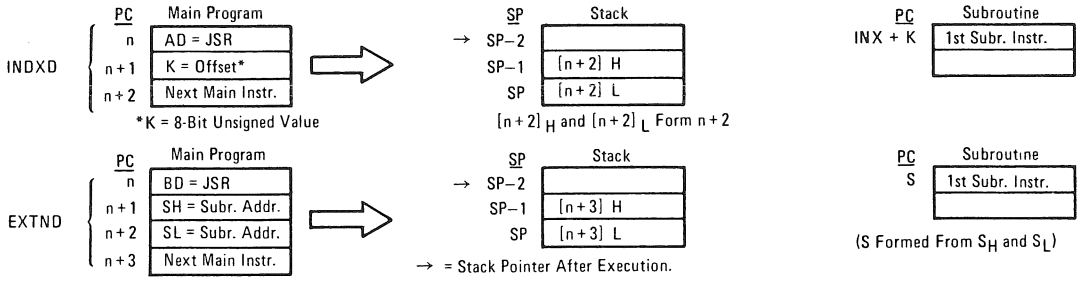
TABLE 5 – JUMP AND BRANCH INSTRUCTIONS

		RELATIVE			INDEX			EXTND			IMPLIED				COND. CODE REG.						
															5	4	3	2	1	0
OPERATIONS	MNEMONIC	OP	~	#	OP	~	#	OP	~	#	OP	~	#	BRANCH TEST	H	I	N	Z	V	C
Branch Always	BRA	20	4	2										None	•	•	•	•	•	•
Branch If Carry Clear	BCC	24	4	2										C = 0	•	•	•	•	•	•
Branch If Carry Set	BCS	25	4	2										C = 1	•	•	•	•	•	•
Branch If = Zero	BEQ	27	4	2										Z = 1	•	•	•	•	•	•
Branch If ≥ Zero	BGE	2C	4	2										$N \oplus V = 0$	•	•	•	•	•	•
Branch If > Zero	BGT	2E	4	2										$Z + (N \oplus V) = 0$	•	•	•	•	•	•
Branch If Higher	BHI	22	4	2										C + Z = 0	•	•	•	•	•	•
Branch If ≤ Zero	BLE	2F	4	2										$Z + (N \oplus V) = 1$	•	•	•	•	•	•
Branch If Lower Or Same	BLS	23	4	2										C + Z = 1	•	•	•	•	•	•
Branch If < Zero	BLT	2D	4	2										$N \oplus V = 1$	•	•	•	•	•	•
Branch If Minus	BMI	2B	4	2										N = 1	•	•	•	•	•	•
Branch If Not Equal Zero	BNE	26	4	2										Z = 0	•	•	•	•	•	•
Branch If Overflow Clear	BVC	28	4	2										V = 0	•	•	•	•	•	•
Branch If Overflow Set	BVS	29	4	2										V = 1	•	•	•	•	•	•
Branch If Plus	BPL	2A	4	2										N = 0	•	•	•	•	•	•
Branch To Subroutine	BSR	8D	8	2											•	•	•	•	•	•
Jump	JMP				6E	4	2	7E	3	3				See Special Operations	•	•	•	•	•	•
Jump To Subroutine	JSR				AD	8	2	BD	9	3					•	•	•	•	•	•
No Operation	NOP										01	2	1	Advances Prog. Cntr. Only	•	•	•	•	•	•
Return From Interrupt	RTI										3B	10	1		———			⑩	———	
Return From Subroutine	RTS										39	5	1		•	•	•	•	•	•
Software Interrupt	SWI										3F	12	1	See Special Operations	•	•	•	•	•	•
Wait for Interrupt*	WAI										3E	9	1		•	⑪	•	•	•	•

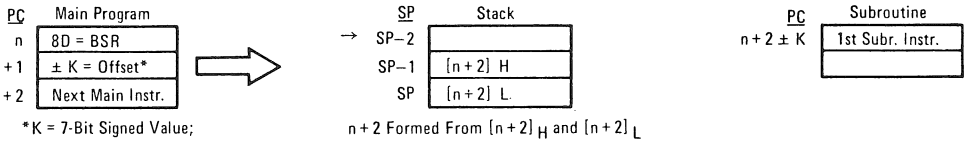
*WAI puts Address Bus, R/W, and Data Bus in the three-state mode while VMA is held low.

SPECIAL OPERATIONS

JSR, JUMP TO SUBROUTINE:

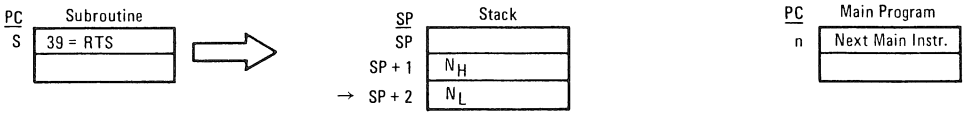


BSR, BRANCH TO SUBROUTINE:



JMP, JUMP:

RTS, RETURN FROM SUBROUTINE:



RTI, RETURN FROM INTERRUPT:

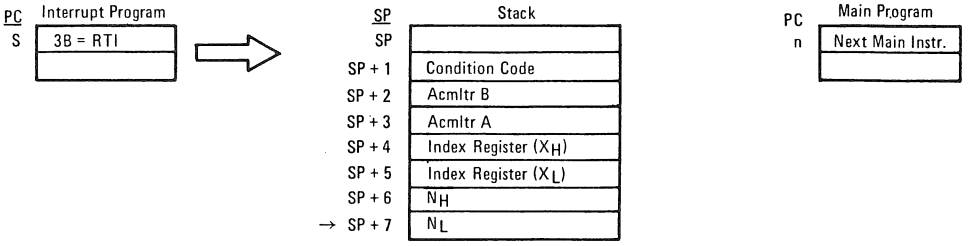


TABLE 6 – CONDITION CODE REGISTER MANIPULATION INSTRUCTIONS

OPERATIONS	MNEMONIC	IMPLIED OP	~	#	BOOLEAN OPERATION	COND. CODE REG. 5 H	4 I	3 N	2 Z	1 V	0 C
Clear Carry	CLC	0C	2	1	0 → C	•	•	•	•	•	R
Clear Interrupt Mask	CLI	0E	2	1	0 → I	•	R	•	•	•	•
Clear Overflow	CLV	0A	2	1	0 → V	•	•	•	•	R	•
Set Carry	SEC	0D	2	1	1 → C	•	•	•	•	•	S
Set Interrupt Mask	SEI	0F	2	1	1 → I	•	S	•	•	•	•
Set Overflow	SEV	0B	2	1	1 → V	•	•	•	•	S	•
Acmltr A → CCR	TAP	06	2	1	A → CCR	———		(12)			———
CCR → Acmltr A	TPA	07	2	1	CCR → A	•	•	•	•	•	•

CONDITION CODE REGISTER NOTES: (Bit set if test is true and cleared otherwise)

1 (Bit V) Test: Result = 10000000?
2 (Bit C) Test: Result = 00000000?
3 (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
4 (Bit V) Test: Operand = 10000000 prior to execution?
5 (Bit V) Test: Operand = 01111111 prior to execution?
6 (Bit V) Test: Set equal to result of N⊕C after shift has occurred.
7 (Bit N) Test: Sign bit of most significant (MS) byte = 1?
8 (Bit V) Test: 2's complement overflow from subtraction of MS bytes?
9 (Bit N) Test: Result less than zero? (Bit 15 = 1)
10 (All) Load Condition Code Register from Stack. (See Special Operations)
11 (Bit I) Set when interrupt occurs. If previously set, a Non-Maskable Interrupt is required to exit the wait state.
12 (All) Set according to the contents of Accumulator A.

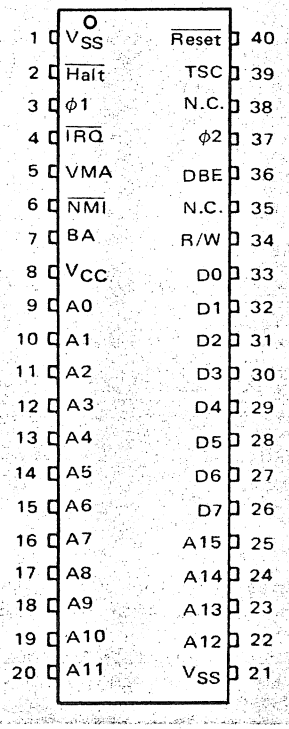
TABLE 7 – INSTRUCTION ADDRESSING MODES AND ASSOCIATED EXECUTION TIMES
(Times in Machine Cycles)

	(Dual Operand)	ACCX	Immediate	Direct	Extended	Indexed	Implied	Relative
ABA		•	•	•	•	•	2	•
ADC	x	•	2	3	4	5	•	•
ADD	x	•	2	3	4	5	•	•
AND	x	•	2	3	4	5	•	•
ASL		2	•	•	6	7	•	•
ASR		2	•	•	6	7	•	•
BCC		•	•	•	•	•	•	4
BCS		•	•	•	•	•	•	4
BEA		•	•	•	•	•	•	4
BGE		•	•	•	•	•	•	4
BGT		•	•	•	•	•	•	4
BHI		•	•	•	•	•	•	4
BIT	x	•	2	3	4	5	•	•
BLE		•	•	•	•	•	•	4
BLS		•	•	•	•	•	•	4
BLT		•	•	•	•	•	•	4
BMI		•	•	•	•	•	•	4
BNE		•	•	•	•	•	•	4
BPL		•	•	•	•	•	•	4
BRA		•	•	•	•	•	•	4
BSR		•	•	•	•	•	•	8
BVC		•	•	•	•	•	•	4
BVS		•	•	•	•	•	•	4
CBA		•	•	•	•	•	2	•
CLC		•	•	•	•	•	2	•
CLI		•	•	•	•	•	2	•
CLR		2	•	•	6	7	•	•
CLV		•	•	•	•	•	2	•
CMP	x	•	2	3	4	5	•	•
COM		2	•	•	6	7	•	•
CPX		•	3	4	5	6	•	•
DAA		•	•	•	•	•	2	•
DEC		2	•	•	6	7	•	•
DES		•	•	•	•	•	4	•
DEX		•	•	•	•	•	4	•
EOR	x	•	2	3	4	5	•	•

	(Dual Operand)	ACCX	Immediate	Direct	Extended	Indexed	Implied
INC		2	•	•	6	7	•
INS		•	•	•	•	•	4
INX		•	•	•	•	•	4
JMP		•	•	•	3	4	•
JSR		•	•	•	9	8	•
LDA	x	•	2	3	4	5	•
LDS		•	3	4	5	6	•
LDX		•	3	4	5	6	•
LSR		2	•	•	6	7	•
NEG		2	•	•	6	7	•
NOP		•	•	•	•	•	2
ORA	x	•	2	3	4	5	•
PSH		•	•	•	•	•	4
PUL		•	•	•	•	•	4
ROL		2	•	•	6	7	•
ROR		2	•	•	6	7	•
RTI		•	•	•	•	•	10
RTS		•	•	•	•	•	5
SBA		•	•	•	•	•	2
SBC	x	•	2	3	4	5	•
SEC		•	•	•	•	•	2
SEI		•	•	•	•	•	2
SEV		•	•	•	•	•	2
STA	x	•	•	4	5	6	•
STS		•	•	5	6	7	•
STX		•	•	5	6	7	•
SUB	x	•	2	3	4	5	•
SWI		•	•	•	•	•	12
TAB		•	•	•	•	•	2
TAP		•	•	•	•	•	2
TBA		•	•	•	•	•	2
TPA		•	•	•	•	•	2
TST		2	•	•	6	7	•
TSX		•	•	•	•	•	4
TSX		•	•	•	•	•	4
WAI		•	•	•	•	•	9

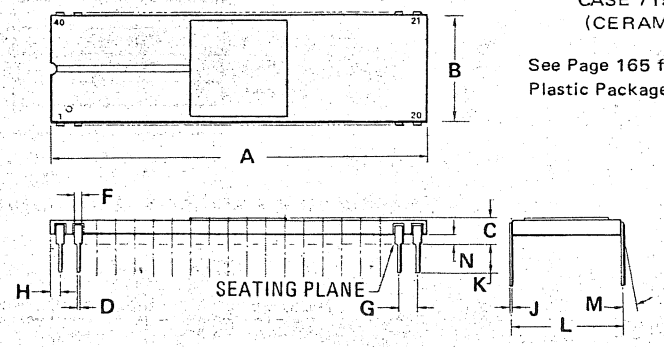
NOTE: Interrupt time is 12 cycles from the end of the instruction being executed, except following a WAI instruction. Then it is 4 cycles.

PIN ASSIGNMENT



PACKAGE DIMENSIONS
CASE 715-02
(CERAMIC)

See Page 165 for Plastic Package dimensions.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060

NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX. MAT'L CONDITION.

SUMMARY OF CYCLE BY CYCLE OPERATION

Table 8 provides a detailed description of the information present on the Address Bus, Data Bus, Valid Memory Address line (VMA), and the Read/Write line (R/W) during each cycle for each instruction.

This information is useful in comparing actual with expected results during debug of both software and hardware as the control program is executed. The information is categorized in groups according to Addressing Mode and Number of Cycles per instruction. (In general, instructions with the same Addressing Mode and Number of Cycles execute in the same manner; exceptions are indicated in the table.)

TABLE 8 – OPERATION SUMMARY

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
IMMEDIATE						
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	2	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Operand Data
CPX LDS LDX	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Operand Data (High Order Byte)
		3	1	Op Code Address + 2	1	Operand Data (Low Order Byte)
DIRECT						
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	1	Address of Operand	1	Operand Data
CPX LDS LDX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	1	Address of Operand	1	Operand Data (High Order Byte)
		4	1	Operand Address + 1	1	Operand Data (Low Order Byte)
STA	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Destination Address
		3	0	Destination Address	1	Irrelevant Data (Note 1)
		4	1	Destination Address	0	Data from Accumulator
STS STX	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	0	Address of Operand	1	Irrelevant Data (Note 1)
		4	1	Address of Operand	0	Register Data (High Order Byte)
		5	1	Address of Operand + 1	0	Register Data (Low Order Byte)
INDEXED						
JMP	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Operand Data
CPX LDS LDX	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Operand Data (High Order Byte)
		6	1	Index Register Plus Offset + 1	1	Operand Data (Low Order Byte)

TABLE 8 – OPERATION SUMMARY (Continued)

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
INDEXED (Continued)						
STA	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		6	1	Index Register Plus Offset	0	Operand Data
ASL LSR ASR NEG CLR ROL COM ROR DEC TST INC	7	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Current Operand Data
		6	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		7	1/0 (Note 3)	Index Register Plus Offset	0	New Operand Data (Note 3)
STS STX	7	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		6	1	Index Register Plus Offset	0	Operand Data (High Order Byte)
		7	1	Index Register Plus Offset + 1	0	Operand Data (Low Order Byte)
JSR	8	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer	0	Return Address (Low Order Byte)
		5	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		6	0	Stack Pointer – 2	1	Irrelevant Data (Note 1)
		7	0	Index Register	1	Irrelevant Data (Note 1)
		8	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
EXTENDED						
JMP	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Jump Address (High Order Byte)
		3	1	Op Code Address + 2	1	Jump Address (Low Order Byte)
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Operand Data
CPX LDS LDX	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Operand Data (High Order Byte)
		5	1	Address of Operand + 1	1	Operand Data (Low Order Byte)
STA A STA B	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Destination Address (High Order Byte)
		3	1	Op Code Address + 2	1	Destination Address (Low Order Byte)
		4	0	Operand Destination Address	1	Irrelevant Data (Note 1)
		5	1	Operand Destination Address	0	Data from Accumulator
ASL LSR ASR NEG CLR ROL COM ROR DEC TST INC	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Current Operand Data
		5	0	Address of Operand	1	Irrelevant Data (Note 1)
		6	1/0 (Note 3)	Address of Operand	0	New Operand Data (Note 3)

TABLE 8 – OPERATION SUMMARY (Continued)

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
EXTENDED (Continued)						
STS STX	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	0	Address of Operand	1	Irrelevant Data (Note 1)
		5	1	Address of Operand	0	Operand Data (High Order Byte)
		6	1	Address of Operand + 1	0	Operand Data (Low Order Byte)
JSR	9	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Subroutine (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Subroutine (Low Order Byte)
		4	1	Subroutine Starting Address	1	Op Code of Next Instruction
		5	1	Stack Pointer	0	Return Address (Low Order Byte)
		6	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		7	0	Stack Pointer – 2	1	Irrelevant Data (Note 1)
		8	0	Op Code Address + 2	1	Irrelevant Data (Note 1)
		9	1	Op Code Address + 2	1	Address of Subroutine (Low Order Byte)
INHERENT						
ABA DAA SEC ASL DEC SEI ASR INC SEV CBA LSR TAB CLC NEG TAP CLI NOP TBA CLR ROL TPA CLV ROR TST COM SBA	2	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
DES DEX INS INX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Previous Register Contents	1	Irrelevant Data (Note 1)
		4	0	New Register Contents	1	Irrelevant Data (Note 1)
PSH	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	1	Stack Pointer	0	Accumulator Data
		4	0	Stack Pointer – 1	1	Accumulator Data
PUL	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Operand Data from Stack
TSX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	0	New Index Register	1	Irrelevant Data (Note 1)
TXS	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Index Register	1	Irrelevant Data
		4	0	New Stack Pointer	1	Irrelevant Data
RTS	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 2)
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Address of Next Instruction (High Order Byte)
		5	1	Stack Pointer + 2	1	Address of Next Instruction (Low Order Byte)

TABLE 8 – OPERATION SUMMARY (Continued)

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
INHERENT (Continued)						
WAI	9	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	1	Stack Pointer	0	Return Address (Low Order Byte)
		4	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		5	1	Stack Pointer – 2	0	Index Register (Low Order Byte)
		6	1	Stack Pointer – 3	0	Index Register (High Order Byte)
		7	1	Stack Pointer – 4	0	Contents of Accumulator A
		8	1	Stack Pointer – 5	0	Contents of Accumulator B
		9	1	Stack Pointer – 6 (Note 4)	1	Contents of Cond. Code Register
RTI	10	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 2)
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Contents of Cond. Code Register from Stack
		5	1	Stack Pointer + 2	1	Contents of Accumulator B from Stack
		6	1	Stack Pointer + 3	1	Contents of Accumulator A from Stack
		7	1	Stack Pointer + 4	1	Index Register from Stack (High Order Byte)
		8	1	Stack Pointer + 5	1	Index Register from Stack (Low Order Byte)
		9	1	Stack Pointer + 6	1	Next Instruction Address from Stack (High Order Byte)
		10	1	Stack Pointer + 7	1	Next Instruction Address from Stack (Low Order Byte)
SWI	12	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 1)
		3	1	Stack Pointer	0	Return Address (Low Order Byte)
		4	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		5	1	Stack Pointer – 2	0	Index Register (Low Order Byte)
		6	1	Stack Pointer – 3	0	Index Register (High Order Byte)
		7	1	Stack Pointer – 4	0	Contents of Accumulator A
		8	1	Stack Pointer – 5	0	Contents of Accumulator B
		9	1	Stack Pointer – 6	0	Contents of Cond. Code Register
		10	0	Stack Pointer – 7	1	Irrelevant Data (Note 1)
		11	1	Vector Address FFFA (Hex)	1	Address of Subroutine (High Order Byte)
		12	1	Vector Address FFFB (Hex)	1	Address of Subroutine (Low Order Byte)
RELATIVE						
BCC BHI BNE BCS BLE BPL BEQ BLS BRA BGE BLT BVC BGT BMI BVS	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Branch Offset
		3	0	Op Code Address + 2	1	Irrelevant Data (Note 1)
		4	0	Branch Address	1	Irrelevant Data (Note 1)
BSR	8	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Branch Offset
		3	0	Return Address of Main Program	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer	0	Return Address (Low Order Byte)
		5	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		6	0	Stack Pointer – 2	1	Irrelevant Data (Note 1)
		7	0	Return Address of Main Program	1	Irrelevant Data (Note 1)
		8	0	Subroutine Address	1	Irrelevant Data (Note 1)

Note 1. If device which is addressed during this cycle uses VMA, then the Data Bus will go to the high impedance three-state condition. Depending on bus capacitance, data from the previous cycle may be retained on the Data Bus.
Note 2. Data is ignored by the MPU.
Note 3. For TST, VMA = 0 and Operand data does not change.
Note 4. While the MPU is waiting for the interrupt, Bus Available will go high indicating the following states of the control lines: VMA is low; Address Bus, R/W, and Data Bus are all in the high impedance state.

MOTOROLA Semiconductors
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

MC6820
(0 to 70°C; L or P Suffix)

MC6820C
(-40 to 85°C; L Suffix only)

PERIPHERAL INTERFACE ADAPTER (PIA)

The MC6820 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the MC6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

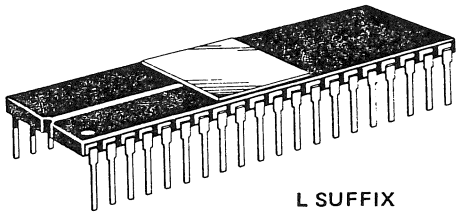
The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on Side A Peripheral Lines

MOS

(N-CHANNEL, SILICON-GATE)

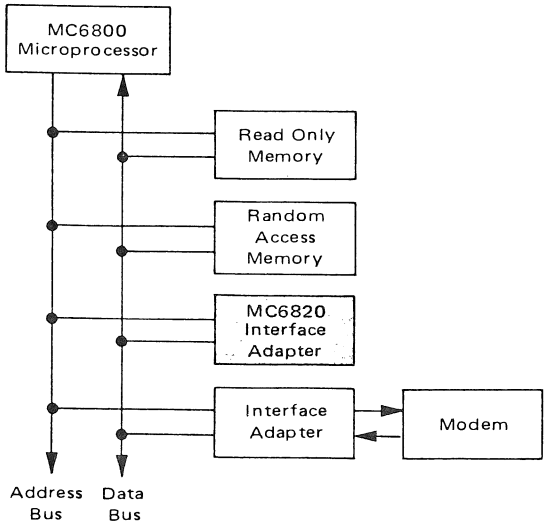
PERIPHERAL INTERFACE ADAPTER



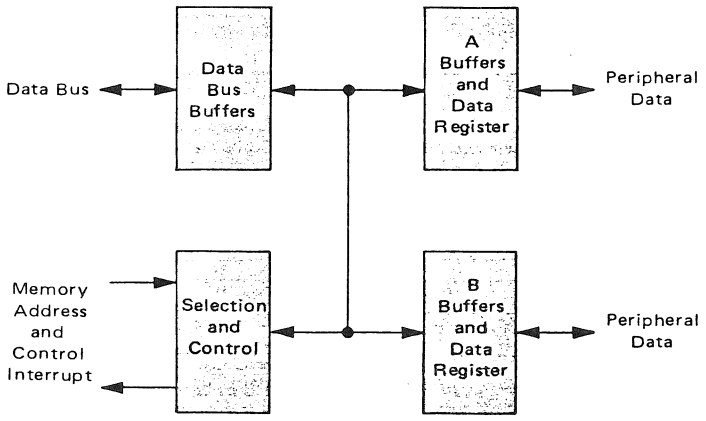
L SUFFIX
CERAMIC PACKAGE
CASE 715

NOT SHOWN: **P SUFFIX**
PLASTIC PACKAGE
CASE 711

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MC6820 PERIPHERAL INTERFACE ADAPTER BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage — Enable	V_{IH}	V_{SS} + 2.4	–	V_{CC}	Vdc
Input High Voltage — Other Inputs		V_{SS} + 2.0	–	V_{CC}	
Input Low Voltage — Enable	V_{IL}	V_{SS} -0.3	–	V_{SS} + 0.4	Vdc
Input Low Voltage — Other Inputs		V_{SS} -0.3	–	V_{SS} + 0.8	
Input Leakage Current (R/W, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, Enable) (V_{in} = 0 to 5.25 Vdc)	I_{in}	–	1.0	2.5	μAdc
Three-State (Off State) Input Current (D0-D7, PB0-PB7, CB2) (V_{in} = 0.4 to 2.4 Vdc)	I_{TSI}	–	2.0	10	μAdc
Input High Current (PA0-PA7, CA2) (V_{IH} = 2.4 Vdc)	I_{IH}	-100	-250	–	μAdc
Input Low Current (PA0-PA7, CA2) (V_{IL} = 0.4 Vdc)	I_{IL}	–	-1.0	-1.6	mAdc
Output High Voltage	V_{OH}				Vdc
(I_{Load} = -205 μAdc, Enable Pulse Width < 25 μs) D0-D7		V_{SS} + 2.4	–	–	
(I_{Load} = -100 μAdc, Enable Pulse Width <25 μs) Other Outputs		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mAdc, Enable Pulse Width < 25 μs)	V_{OL}	–	–	V_{SS} + 0.4	Vdc
Output High Current (Sourcing)	I_{OH}				
(V_{OH} = 2.4 Vdc) D0-D7		-205	–	–	μAdc
Other Outputs		-100	–	–	μAdc
(V_O = 1.5 Vdc, the current for driving other than TTL, e.g., Darlington Base) PB0-PB7, CB2		-1.0	-2.5	-10	mAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	I_{OL}	1.6	–	–	mAdc
Output Leakage Current (Off State) ($\overline{IRQA}$, $\overline{IRQB}$) (V_{OH} = 2.4 Vdc)	I_{LOH}	–	1.0	10	μAdc
Power Dissipation	P_D	–	–	650	mW
Input Capacitance — Enable	C_{in}	–	–	20	pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz) D0-D7		–	–	12.5	
PA0-PA7, PB0-PB7, CA2, CB2		–	–	10	
R/W, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1		–	–	7.5	
Output Capacitance ($\overline{IRQA}$, $\overline{IRQB}$)	C_{out}	–	–	5.0	pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz) PB0-PB7		–	–	10	
Peripheral Data Setup Time (Figure 1)	t_{PDSU}	200	–	–	ns
Delay Time, Enable negative transition to CA2 negative transition (Figure 2, 3)	t_{CA2}	–	–	1.0	μs
Delay Time, Enable negative transition to CA2 positive transition (Figure 2)	t_{RS1}	–	–	1.0	μs
Rise and Fall Times for CA1 and CA2 input signals (Figure 3)	t_r,t_f	–	–	1.0	μs
Delay Time from CA1 active transition to CA2 positive transition (Figure 3)	t_{RS2}	–	–	2.0	μs
Delay Time, Enable negative transition to Peripheral Data valid (Figures 4, 5)	t_{PDW}	–	–	1.0	μs
Delay Time, Enable negative transition to Peripheral CMOS Data Valid (V_{CC} – 30% V_{CC}, Figure 4; Figure 12 Load C) PA0-PA7, CA2	t_{CMOS}	–	–	2.0	μs
Delay Time, Enable positive transition to CB2 negative transition (Figure 6, 7)	t_{CB2}	–	–	1.0	μs
Delay Time, Peripheral Data valid to CB2 negative transition (Figure 5)	t_{DC}	20	–	–	ns
Delay Time, Enable positive transition to CB2 positive transition (Figure 6)	t_{RS1}	–	–	1.0	μs
Rise and Fall Time for CB1 and CB2 input signals (Figure 7)	t_r,t_f	–	–	1.0	μs
Delay Time, CB1 active transition to CB2 positive transition (Figure 7)	t_{RS2}	–	–	2.0	μs
Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$ (Figure 8)	t_{IR}	–	–	1.6	μs
Reset Low Time* (Figure 9)	t_{RL}	2.0	–	–	μs

*The Reset line must be high a minimum of 1.0 μs before addressing the PIA.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Thermal Resistance	θ_{JA}	82.5	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BUS TIMING CHARACTERISTICS

READ (Figures 10 and 12)

Characteristic	Symbol	Min	Typ	Max	Unit
Enable Cycle Time	t_{cycE}	1.0	–	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	–	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	–	μs
Setup Time, Address and R/W valid to Enable positive transition	t_{AS}	160	–	–	ns
Data Delay Time	t_{DDR}	–	–	320	ns
Data Hold Time	t_H	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	–	25	ns

WRITE (Figures 11 and 12)

Enable Cycle Time	t_{cycE}	1.0	–	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	–	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	–	μs
Setup Time, Address and R/W valid to Enable positive transition	t_{AS}	160	–	–	ns
Data Setup Time	t_{DSW}	195	–	–	ns
Data Hold Time	t_H	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	–	25	ns

FIGURE 1 – PERIPHERAL DATA SETUP TIME
(Read Mode)

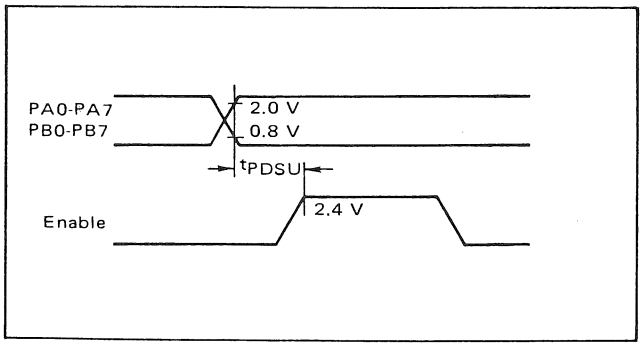


FIGURE 2 – CA2 DELAY TIME
(Read Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

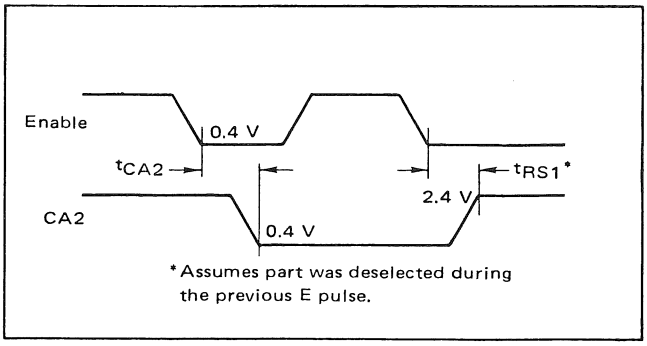


FIGURE 3 – CA2 DELAY TIME
(Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

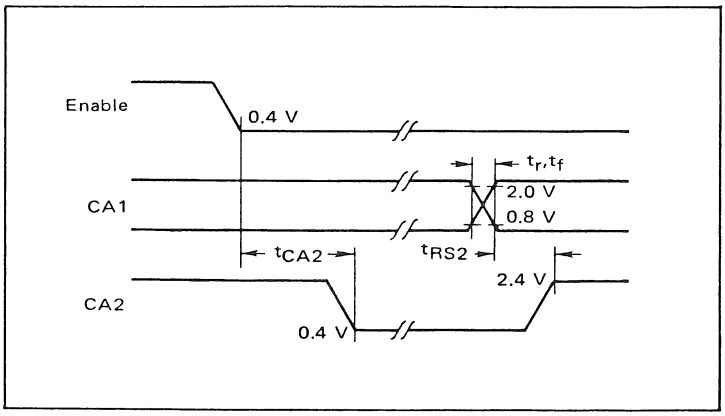


FIGURE 4 – PERIPHERAL CMOS DATA DELAY TIMES
(Write Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

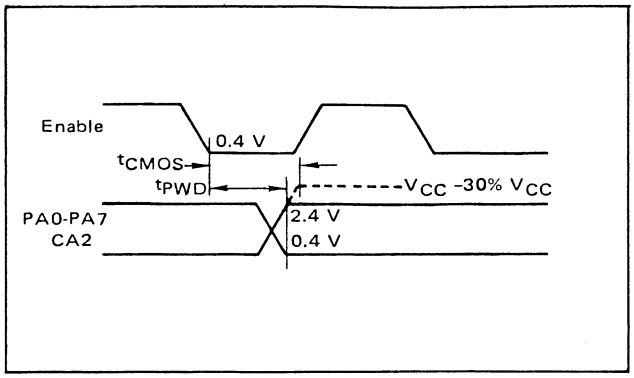
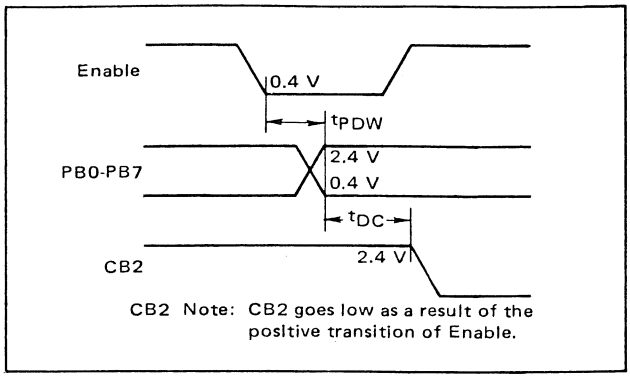
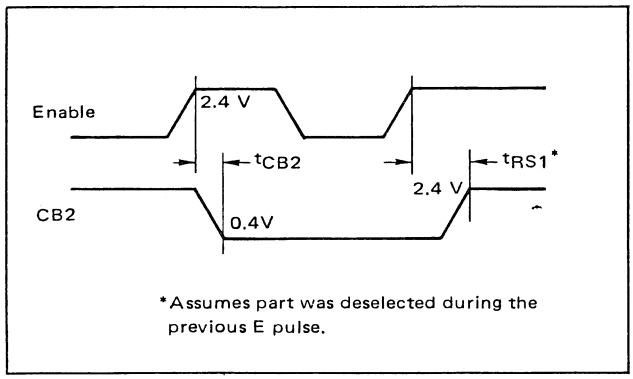


FIGURE 5 – PERIPHERAL DATA AND CB2 DELAY TIMES
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



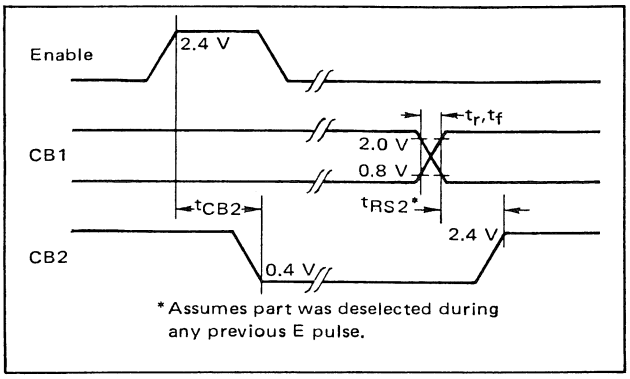
CB2 Note: CB2 goes low as a result of the positive transition of Enable.

FIGURE 6 – CB2 DELAY TIME
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



*Assumes part was deselected during the previous E pulse.

FIGURE 7 – CB2 DELAY TIME
(Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)



*Assumes part was deselected during any previous E pulse.

FIGURE 8 – $\overline{IRQ}$ RELEASE TIME

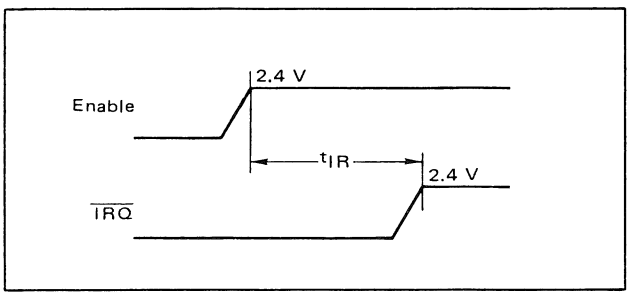
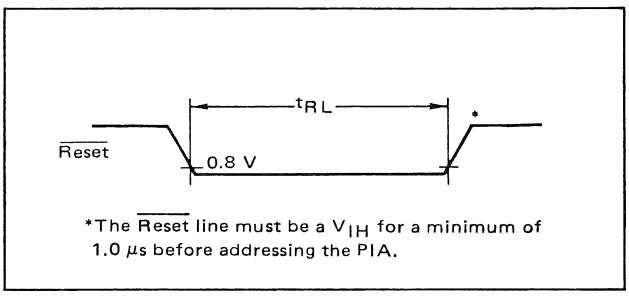


FIGURE 9 – $\overline{RESET}$ LOW TIME



*The $\overline{Reset}$ line must be a V_{IH} for a minimum of 1.0 μs before addressing the PIA.

FIGURE 10 – BUS READ TIMING CHARACTERISTICS
(Read Information from PIA)

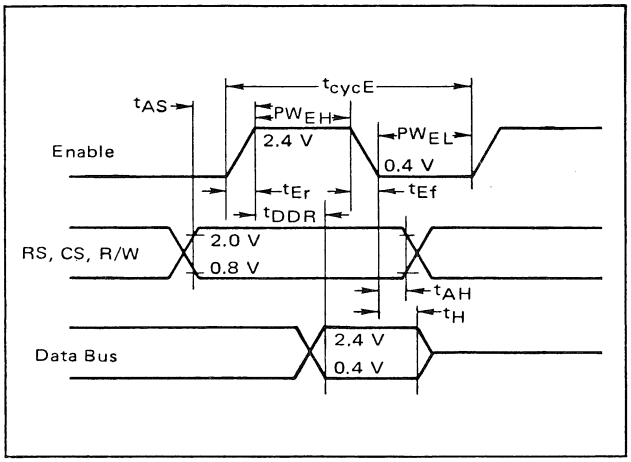


FIGURE 11 – BUS WRITE TIMING CHARACTERISTICS
(Write Information into PIA)

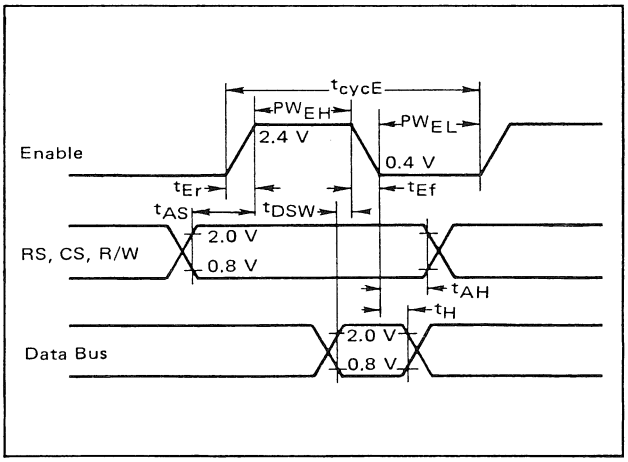
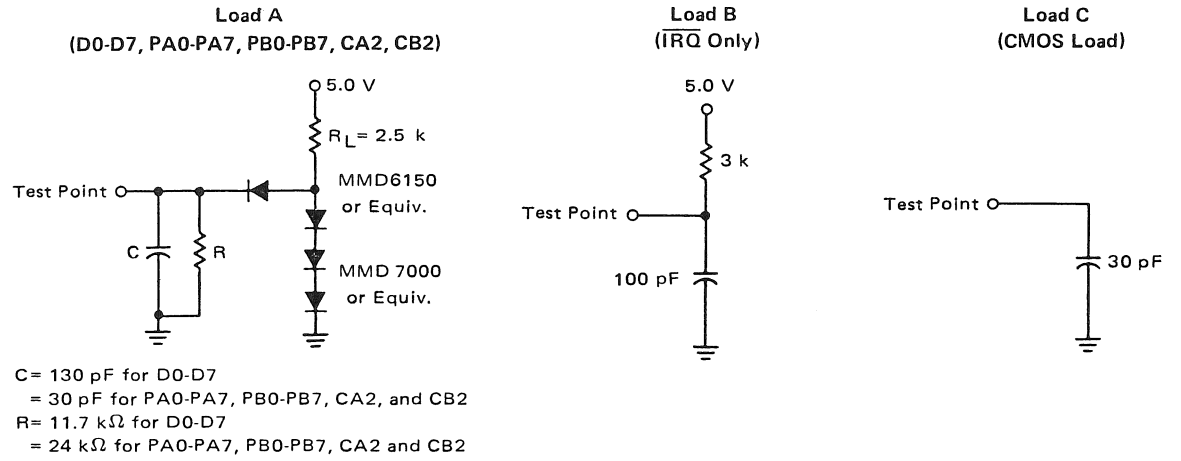


FIGURE 12 – BUS TIMING TEST LOADS



C= 130 pF for D0-D7
= 30 pF for PA0-PA7, PB0-PB7, CA2, and CB2
R= 11.7 kΩ for D0-D7
= 24 kΩ for PA0-PA7, PB0-PB7, CA2 and CB2

PIA INTERFACE SIGNALS FOR MPU

The PIA interfaces to the MC6800 MPU with an eight-bit bi-directional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with the MC6800 VMA output, permit the MPU to have complete control over the PIA. VMA should be utilized in conjunction with an MPU address line into a chip select of the PIA.

PIA Bi-Directional Data (D0-D7) – The bi-directional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The Read/Write line is in the Read (high) state when the PIA is selected for a Read operation.

PIA Enable (E) – The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal will normally be a derivative of the MC6800 $\phi 2$ Clock.

PIA Read/Write (R/W) – This signal is generated by the MPU to control the direction of data transfers on the Data Bus. A low state on the PIA Read/Write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the Read/Write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.

$\overline{\text{Reset}}$ – The active low $\overline{\text{Reset}}$ line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.

PIA Chip Select (CS0, CS1 and $\overline{\text{CS2}}$) – These three input signals are used to select the PIA. CS0 and CS1 must be high and $\overline{\text{CS2}}$ must be low for selection of the device. Data transfers are then performed under the control of the Enable and Read/Write signals. The chip select lines must be stable for the duration of the E pulse. The device is deselected when any of the chip selects are in the inactive state.

PIA Register Select (RS0 and RS1) – The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read.

The register and chip select lines should be stable for the duration of the E pulse while in the read or write cycle.

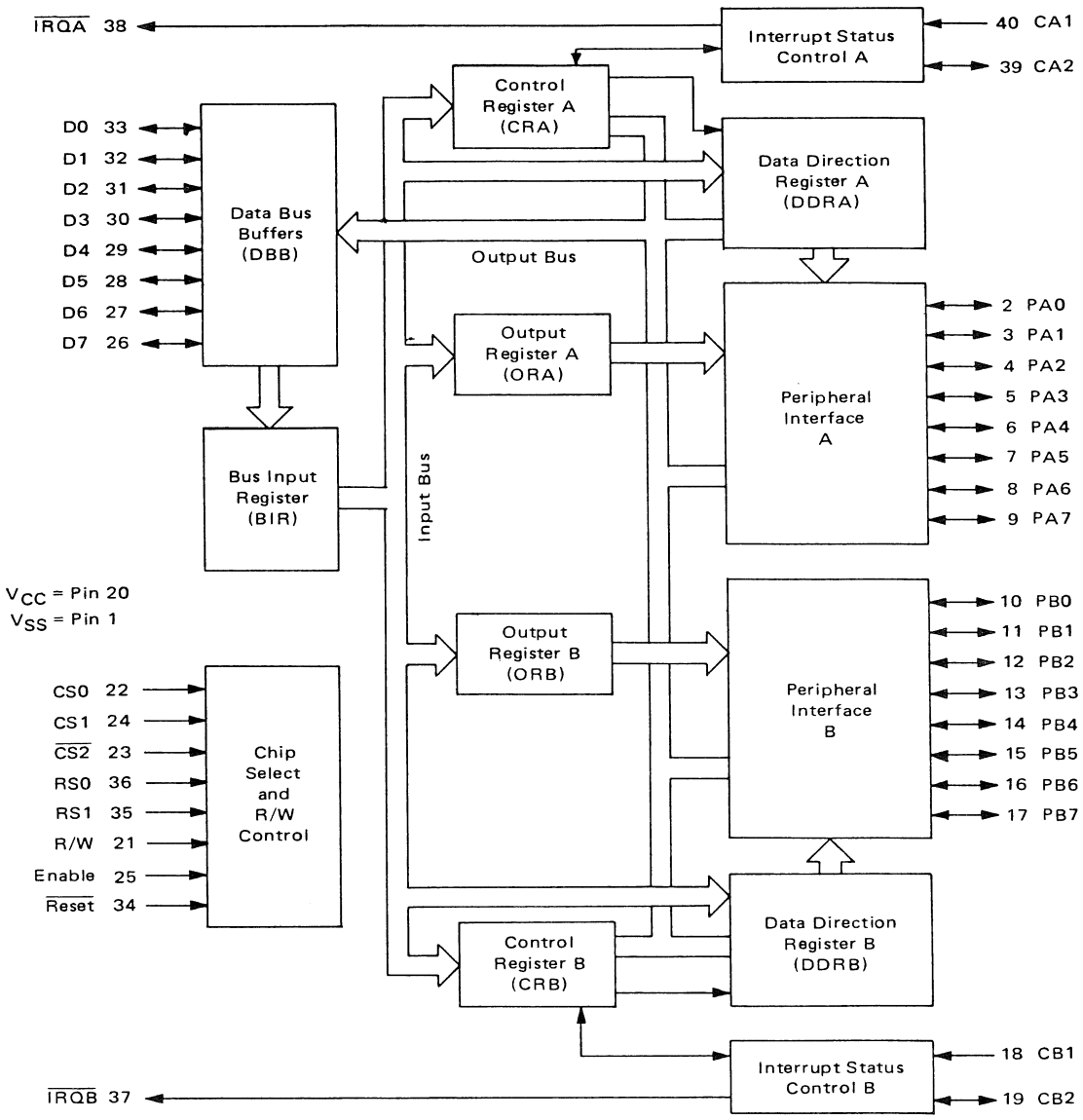
Interrupt Request ($\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$) – The active low Interrupt Request lines ($\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open drain" (no load device on the chip). This permits all interrupt request lines to be tied together in a wire-OR configuration.

Each Interrupt Request line has two internal interrupt flag bits that can cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU may be accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The interrupt flags are cleared (zeroed) as a result of an

EXPANDED BLOCK DIAGRAM



MPU Read Peripheral Data Operation of the corresponding data register. After being cleared, the interrupt flag bit cannot be enabled to be set until the PIA is deselected during an E pulse. The E pulse is used to condition the interrupt control lines (CA1, CA2, CB1, CB2). When these lines are used as interrupt inputs at least one E pulse must occur from the inactive edge to the active edge of the interrupt input signal to condition the edge sense network. If the interrupt flag has been enabled and the edge sense circuit has been properly conditioned, the interrupt flag will be set on the next active transition of the interrupt input pin.

PIA PERIPHERAL INTERFACE LINES

The PIA provides two 8-bit bi-directional data buses and four interrupt/control lines for interfacing to peripheral devices.

Section A Peripheral Data (PA0-PA7) — Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode the internal pullup resistor on these lines represents a maximum of one standard TTL load.

The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical "1" written into the register will cause a "high" on the corresponding data line while a "0" results in a "low". Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volt for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.

Section B Peripheral Data (PB0-PB7) — The peripheral data lines in the B Section of the PIA can be programmed to act as either inputs or outputs in a similar manner to PA0-PA7. However, the output buffers driving these lines differ from those driving lines PA0-PA7. They have three-state capability, allowing them to enter a high impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines PB0-PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a "high". As outputs, these lines are compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch.

Interrupt Input (CA1 and CB1) — Peripheral Input lines CA1 and CB1 are input only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.

Peripheral Control (CA2) — The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents one standard TTL load. The function of this signal line is programmed with Control Register A.

Peripheral Control (CB2) — Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output it is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.

NOTE: It is recommended that the control lines (CA1, CA2, CB1, CB2) should be held in a logic 1 state when $\overline{\text{Reset}}$ is active to prevent setting of corresponding interrupt flags in the control register when $\overline{\text{Reset}}$ goes to an inactive state. Subsequent to $\overline{\text{Reset}}$ going inactive, a read of the data registers may be used to clear any undesired interrupt flags.

INTERNAL CONTROLS

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

TABLE 1 – INTERNAL ADDRESSING

RS1	RS0	Control Register Bit CRA-2	Control Register Bit CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

INITIALIZATION

A low reset line has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

Details of possible configurations of the Data Direction and Control Register are as follows.

DATA DIRECTION REGISTERS (DDRA and DDRB)

The two Data Direction Registers allow the MPU to control the direction of data through each corresponding peripheral data line. A Data Direction Register bit set at "0" configures the corresponding peripheral data line as an input; a "1" results in an output.

CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1 and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1 or CB2. The format of the control words is shown in Table 2.

TABLE 2 – CONTROL WORD FORMAT

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

Data Direction Access Control Bit (CRA-2 and CRB-2) – Bit 2 in each Control register (CRA and CRB) allows selection of either a Peripheral Interface Register or the Data Direction Register when the proper register select signals are applied to RS0 and RS1.

Interrupt Flags (CRA-6, CRA-7, CRB-6, and CRB-7) – The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Control lines when those lines are programmed to be inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

TABLE 3 – CONTROL OF INTERRUPT INPUTS CA1 AND CB1

CRA-1 (CRB-1)	CRA-0 (CRB-0)	Interrupt Input CA1 (CB1)	Interrupt Flag CRA-7 (CRB-7)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	↓ Active	Set high on ↓ of CA1 (CB1)	Disabled — $\overline{IRQ}$ remains high
0	1	↓ Active	Set high on ↓ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high
1	0	↑ Active	Set high on ↑ of CA1 (CB1)	Disabled — $\overline{IRQ}$ remains high
1	1	↑ Active	Set high on ↑ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high

Notes:
1. ↑ indicates positive transition (low to high)
2. ↓ indicates negative transition (high to low)
3. The Interrupt flag bit CRA-7 is cleared by an MPU Read of the A Data Register, and CRB-7 is cleared by an MPU Read of the B Data Register.
4. If CRA-0 (CRB-0) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs after CRA-0 (CRB-0) is written to a "one".

Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1) – The two lowest order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1 (Table 3).

TABLE 4 – CONTROL OF CA2 AND CB2 AS INTERRUPT INPUTS
CRA5 (CRB5) is low

CRA-5 (CRB-5)	CRA-4 (CRB-4)	CRA-3 (CRB-3)	Interrupt Input CA2 (CB2)	Interrupt Flag CRA-6 (CRB-6)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	0	↓ Active	Set high on ↓ of CA2 (CB2)	Disabled — $\overline{IRQ}$ remains high
0	0	1	↓ Active	Set high on ↓ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high
0	1	0	↑ Active	Set high on ↑ of CA2 (CB2)	Disabled — $\overline{IRQ}$ remains high
0	1	1	↑ Active	Set high on ↑ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high

Notes: 1. ↑ indicates positive transition (low to high)
2. ↓ indicates negative transition (high to low)
3. The Interrupt flag bit CRA-6 is cleared by an MPU Read of the A Data Register and CRB-6 is cleared by an MPU Read of the B Data Register.
4. If CRA-3 (CRB-3) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs after CRA-3 (CRB-3) is written to a "one".

TABLE 5 – CONTROL OF CB2 AS AN OUTPUT
CRB-5 is high

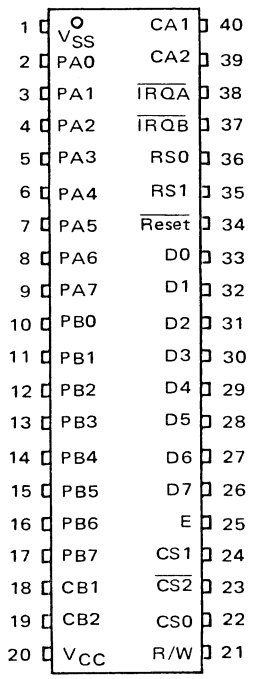
CRB-5	CRB-4	CRB-3	CB2 Cleared	CB2 Set
1	0	0	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High when the interrupt flag bit CRB-7 is set by an active transition of the CB1 signal.
1	0	1	Low on the positive transition of the first E pulse after an MPU Write "B" Data Register operation.	High on the positive edge of the first "E" pulse following an "E" pulse which occurred while the part was deselected.
1	1	0	Low when CRB-3 goes low as a result of an MPU Write in Control Register "B".	Always low as long as CRB-3 is low. Will go high on an MPU Write in Control Register "B" that changes CRB-3 to "one".
1	1	1	Always high as long as CRB-3 is high. Will be cleared when an MPU Write Control Register "B" results in clearing CRB-3 to "zero".	High when CRB-3 goes high as a result of an MPU Write into Control Register "B".

Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5) – Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1) (Table 4). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different characteristics (Tables 5 and 6).

TABLE 6 – CONTROL OF CA-2 AS AN OUTPUT
CRA-5 is high

CRA-5	CRA-4	CRA-3	CA2 Cleared	CA2 Set
1	0	0	Low on negative transition of E after an MPU Read "A" Data operation.	High when the interrupt flag bit CRA-7 is set by an active transition of the CA1 signal.
1	0	1	Low on negative transition of E after an MPU Read "A" Data operation.	High on the negative edge of the first "E" pulse which occurs during a deselect.
1	1	0	Low when CRA-3 goes low as a result of an MPU Write to Control Register "A".	Always low as long as CRA-3 is low. Will go high on an MPU Write to Control Register "A" that changes CRA-3 to "one".
1	1	1	Always high as long as CRA-3 is high. Will be cleared on an MPU Write to Control Register "A" that clears CRA-3 to a "zero".	High when CRA-3 goes high as a result of an MPU Write to Control Register "A".

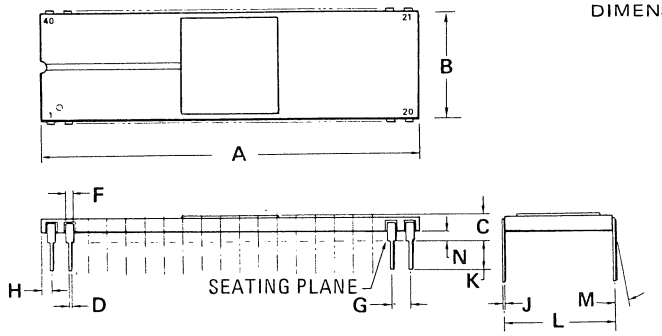
PIN ASSIGNMENT



PACKAGE DIMENSIONS

CASE 715-02
(CERAMIC)

SEE PAGE 165 FOR PLASTIC PACKAGE DIMENSIONS.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060

NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX. MAT'L CONDITION.

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MCM6810A

(0 to 70°C; L or P Suffix)

MCM6810AC

(-40 to 85°C; L Suffix only)

MOS

(N-CHANNEL, SILICON-GATE)

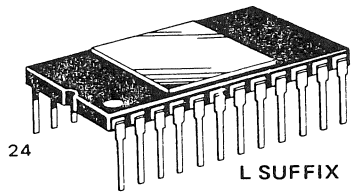
128 X 8-BIT STATIC RANDOM ACCESS MEMORY

128 X 8-BIT STATIC RANDOM ACCESS MEMORY

The MCM6810 is a byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing random storage in byte increments. Memory expansion is provided through multiple Chip Select inputs.

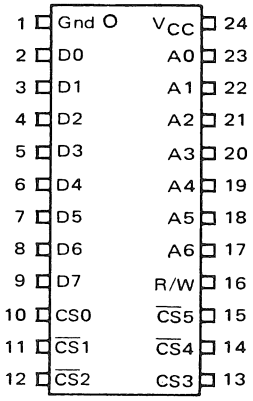
- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bi-Directional Three-State Data Input/Output
- Six Chip Select Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns — MCM6810AL1
  450 ns — MCM6810AL



L SUFFIX
CERAMIC PACKAGE
CASE 716

NOT SHOWN: P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT

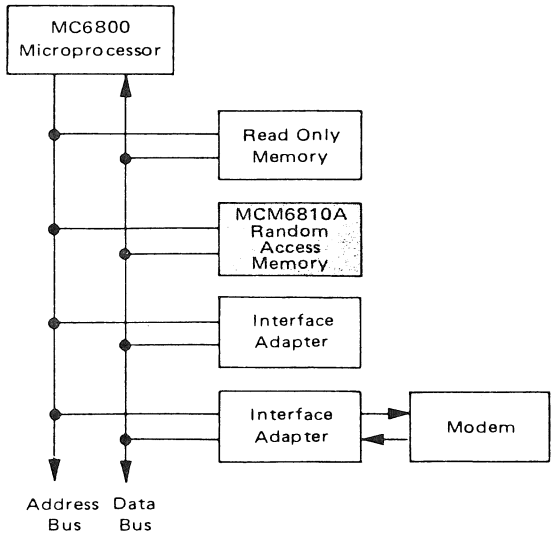


ABSOLUTE MAXIMUM RATINGS (See Note 1)

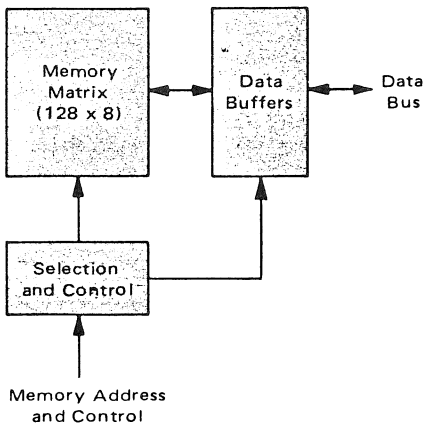
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM



MCM6810A RANDOM ACCESS MEMORY
BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

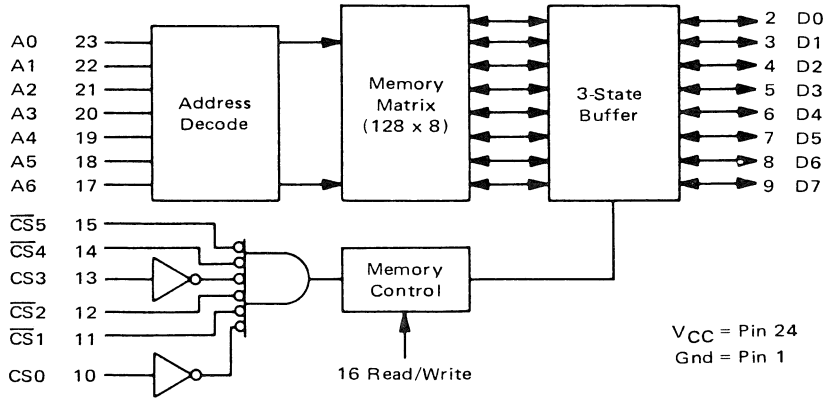
Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (A_n, R/W, CS_n, $\overline{CS}_n$) (V_{in} = 0 to 5.25 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = –205 μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) ($\overline{CS}$ = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current (V_{CC} = 5.25 V, all other pins grounded, T_A = 0°C) MCM6810AL MCM6810AL1	I_{CC}	– –	– –	70 80	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

BLOCK DIAGRAM



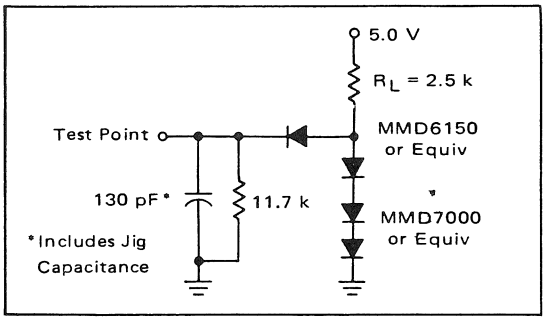
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	See Figure 1

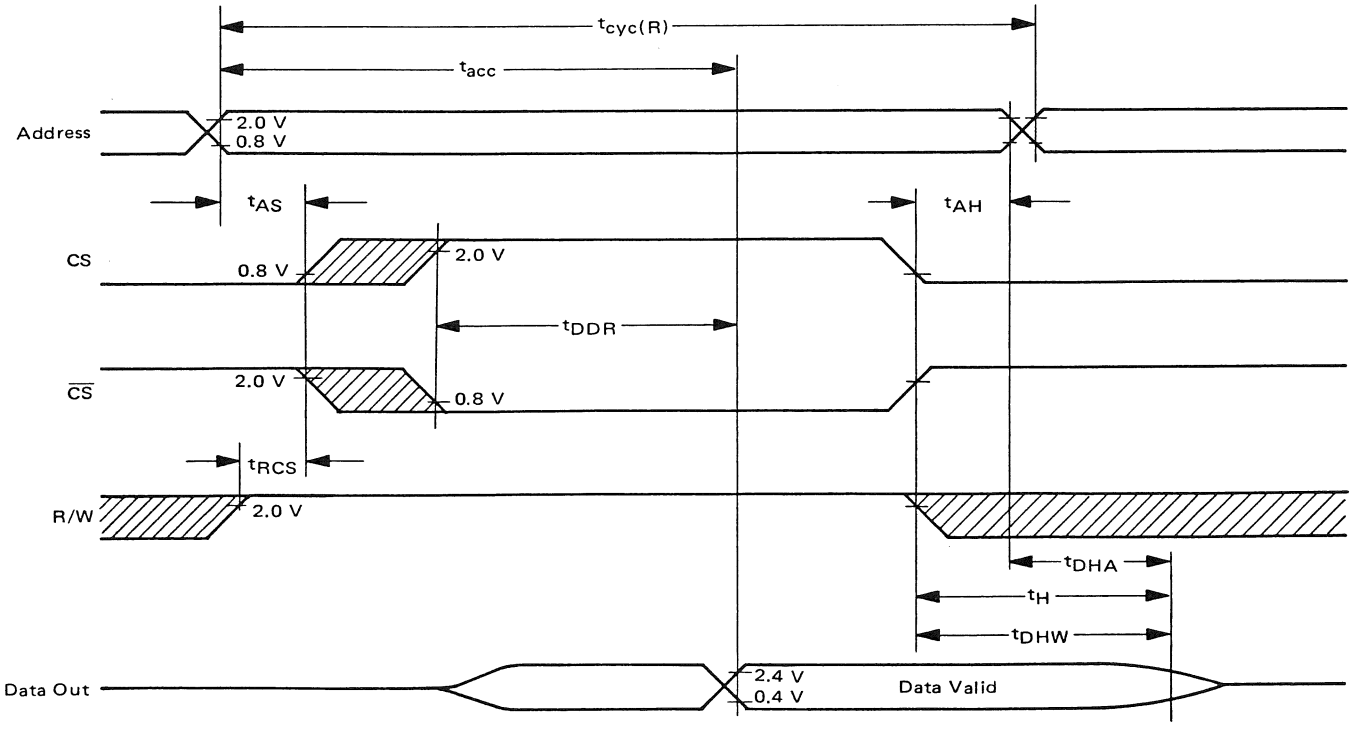
FIGURE 1 – AC TEST LOAD



READ CYCLE

Characteristic	Symbol	MCM6810AL		MCM6810AL1		Unit
		Min	Max	Min	Max	
Read Cycle Time	$t_{cyc(R)}$	450	–	350	–	ns
Access Time	t_{acc}	–	450	–	350	ns
Address Setup Time	t_{AS}	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	ns
Data Delay Time (Read)	t_{DDR}	–	230	–	180	ns
Read to Select Delay Time	t_{RCS}	0	–	0	–	ns
Data Hold from Address	t_{DHA}	10	–	10	–	ns
Output Hold Time	t_H	10	–	10	–	ns
Data Hold from Write	t_{DHW}	10	80	10	60	ns

READ CYCLE TIMING



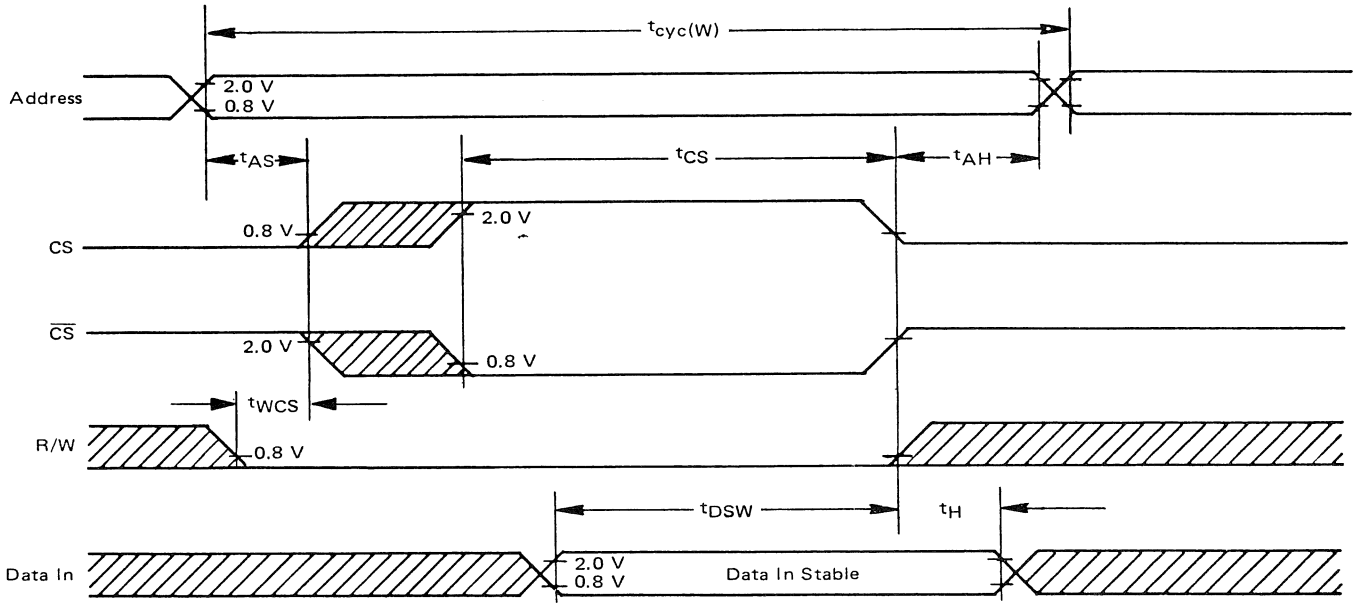
= Don't Care

Note: CS and $\overline{CS}$ can be enabled for consecutive read cycles provided R/W remains at V_{IH}.

WRITE CYCLE

Characteristic	Symbol	MCM6810AL		MCM6810AL1		Unit
		Min	Max	Min	Max	
Write Cycle Time	$t_{cyc(W)}$	450	–	350	–	ns
Address Setup Time	t_{AS}	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	ns
Chip Select Pulse Width	t_{CS}	300	–	250	–	ns
Write to Chip Select Delay Time	t_{WCS}	0	–	0	–	ns
Data Setup Time (Write)	t_{DSW}	190	–	150	–	ns
Input Hold Time	t_H	10	–	10	–	ns

WRITE CYCLE TIMING



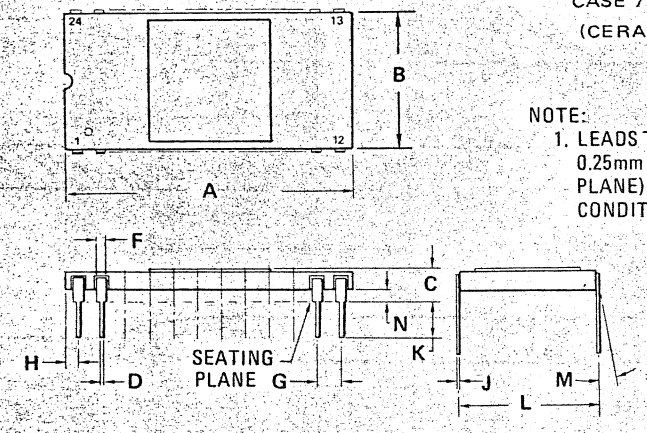
= Don't Care

Note: CS and $\overline{CS}$ can be enabled for consecutive write cycles provided R/W is strobed to V_{IH} before or coincident with the Address change, and remains high for time t_{AS}.

PACKAGE DIMENSIONS

CASE 716-02
(CERAMIC)

See Page 165 for Plastic Package dimensions.



NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	29.97	30.99	1.180	1.220
B	14.88	15.62	0.585	0.615
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.88	15.37	0.585	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060

Appendix B

H-P 9825 PROGRAMMING EXAMPLES

Controlling the DPO with the H-P 9825 is demonstrated in the following discussion. In addition to an understanding of the DPO, the P7001/IEEE 488 Interface, and the IEEE Standard 488-1975, familiarity with the 9825 and its 98034A HP-IB Interface is required.

Before operating the DPO with the 9825, ensure that the strap option on the P7001/IEEE 488 Interface is set for "Optional" operation (*i.e.*, in the strapped position), as explained on page 2-2 of this manual. Also make certain that the rotating switch on the 98034A HP-IB Interface is set to 7.

NOTE

When operating in the "optional" mode, the "Single Sweep Reset" (SSR) command and all of the DPO Front Panel PROGRAM CALL buttons should not be used.

The general format of the commands will be:

```
wrt 7Ø1,"cmd^"
      or
wrt 7Ø1,"cmd?"
```

where the '7' of '7Ø1' refers to the card setting on the 98034A HP-IB Interface; the 'Ø1' refers to the primary address set on the DPO/IEEE 488 Interface DIP switch (see page 2-1 of this manual); the ^ is used here for illustrative purposes only to indicate a mandatory blank space; and "cmd^" or "cmd?" is any of the commands described in Chapter 3 and shown in Tables 3-1 and 3-2 of this manual.

CLEARING THE INTERFACE AND SRQ LINE

The first command is usually to clear the interface and the SRQ line. This can be accomplished as follows:

```
wrt 701,"DCL "
```

STORE & HOLD

To Store and/or Hold a particular waveform, use the following examples as guides:

```
wrt 701,"STO A"
wrt 701,"HOL A"
```

Store and Hold may be accomplished for multiple waveforms as follows:

```
wrt 701,"STO D,B,A"
wrt 701,"HOL D,B,A"
```

READING DATA FROM THE DPO

Data may be read from the DPO into the 9825 as follows:

```
 0: dim A[512]
 1: wrt 701,"DPx?"
 2: for I=1 to 512
 3: red 701,A[I]
 4: next I
```

In the foregoing example, the variable A is first dimensioned to a 512-element array in line 0; line 1 prepares the DPO to transmit the data ('x' in "DPx?" represents any one of the DPO waveform arrays A, B, C or D); and lines 2 through 4 do the actual transfer.

WRITING DATA TO THE DPO

To transfer data from the 9825 to the DPO, use the following example as guide (remember that the data must be integers in the range 0 to 1023):

```
 0: dim A[512]
 .
 .
19:
20: fmt 1,x,f.0,z
21: wtb 701,"DPx "
22: for I=1 to 512
23: wrt 701.1,A[I]
24: next I
25: wrt 701,""
```

In the preceding example, lines 0 through 19 dimension and define the contents of variable A. Line 20 is a format statement referred to in line 23; in this format statement the 'x' suppresses leading spaces, to enhance transfer speed; the 'f.0' suppresses the decimal point, which if sent to the interface would cause a 113 error; and the 'z' suppresses the carriage return/line feed, thereby preventing the data stream from being prematurely terminated (since the DPO will terminate input upon receiving an <LF> character).

@

WRITING DATA TO THE DPO (Continued)

Line 21 prepares the DPO to receive data ('x' in "DPx " represents any one of the the DPO waveform arrays A, B, C or D). Lines 22 and 24 set up the output loop with line 23 actually effecting the transfer. In line 23, the '.1' in '701.1' is a referencing technique used by the 9825 to perform the write operation using format #1.

READING SCALE FACTORS

The following example may be used to read a scale factor from the DPO:

```
dim A$[10]
wrt 701,"CHL xx"
wrt 701,"SCL?"
red 701,A$
dsp A$
end
```

where 'xx' represents the channel to be read (see "Reading Scale Factors" on page 3-11 of this manual).

WRITING MESSAGES TO THE DPO

The following example may be used to write messages (or scale factors) to the DPO:

```
0: wrt 701,"ADR 3456"
1: wrt 701,"SCL THIS IS LOTS OF FUN"
2: wrt 701,"ADR 7296"    (Lines 2 & 3 are not necessary to write
3: wrt 701,"OCT 040100"   into Field 0, addresses 2048 - 2559.)
4: end
```

In the foregoing example, line 0 sets up the DPO address register to Field 2, waveform D. Line 1 transfers the message to Field 2, waveform D. Line 2 addresses the Readout Interface register in the DPO, and line 3 sets up the Readout Interface to display the message residing at Field 2, waveform D.

DPO DISPLAY SOURCE

The DPO Display Source may be changed as follows:

```
0: dim A$[6],B$[12]
1: wrt 701,"ADR 7040"
2: wrt 701,"OCT?"
3: red 701,A$
4: "x"→A$[2,2];"OCT "&A$→B$
5: wrt 701,B$
6: end
```

where "x" is 2 for plug-ins, 4 for memory, or 6 for both.

DPO DISPLAY SOURCE (Continued)

In the preceding example, line Ø dimensions two string variables; line 1 sets the interface Address Register to the decimal address of the Display Generator card within the DPO; lines 2 and 3 read the value of that card; line 4 modifies the status word according to which display mode is desired; and line 5 sends the modified status word back to the DPO, thus changing the display mode appropriately.

EXECUTING A SERIAL POLL

The following routine should be used to conduct a serial poll when the SRQ line is asserted (*i.e.*, when an interrupt occurs):

CAUTION

Do not attempt to use the standard HP mnemonic to perform the serial poll.

```
30: "ser":moct;rds(7,r1,r2,r3)→r4
31: band(2,shf(r3,5))→r1
32: band(37,r2)+40→r2
33: dtoA+100→r3
34: wti 0,7;wti 6,77;wti 6,r2;wti 6,30;wti 6,r3;rdi 4→r2;rdi 4→r2
35: wti 6,137;wti 6,31;wti 6,77;wti 7,r1
36: mdec;otdr2→r2;dsp r2
37: end
```

On entry to the above routine, the variable A should be set to the value of the primary address of the DPO. On exit, the status byte will be displayed on the 9825 in decimal. This routine could be made a subroutine by modifying line 36 by replacing the 'dsp r2' with 'ret', which would leave the decimal status byte in r2, then return to the calling routine.

The following detailed description will be useful to those who are interested in byte by byte transfers over the IEEE 488 bus. Line 3Ø labels the routine "ser" for serial poll; sets the calculator mode to octal so that all subsequent program values are to be interpreted as octal numbers; and finally the rds command interrogates the 98034A HP-IB Interface to determine its current status (note that the 7 here corresponds to the selector switch setting on top of the 98034A HP-IB Interface housing). Line 31 performs a binary 'AND' to mask all the line values on the IEEE 488 bus except the REN (Remote ENable) line. This is stored in r1 and is used later to ensure that the value (asserted or unasserted) of REN does not change during this sequence.

EXECUTING A SERIAL POLL (Continued)

Line 32 masks r2 to determine the primary address for the calculator interface itself. This value is added to 40_8 to create the listen address for the calculator which is then stored in r2. Line 33 performs a decimal to octal conversion of the variable A (the primary address of the DPO) which is then added to 100_8 to create the talk address of the DPO.

Lines 34 and 35 actually perform all the data transfers on the bus, as follows: wti 0,7 selects the 9825 interface with which the following transfers are to be made (again, the 7 corresponds to the selector switch setting); wti 6,77 places UNL (UNListen) on the IEEE 488 lines (ATN is asserted); wti 6,r2 tells the controller to listen; wti 6,3Ø issues the command SPE (Serial Poll Enable); wti 6,r3 tells the DPO to talk; rdi 4→r2 triggers the interface to read; and rdi 4→r2 reads the data and places status byte into r2.

In line 35: wti 6,137 performs UNT (UNTalk); wti 6,31 issues SPD (Serial Poll Disable); wti 6,77 executes another UNL; and wti 7,r1 unasserts the ATN line while leaving REN in the same condition that it was in upon entering the routine.

In line 36, the calculator mode is set back to decimal; the status byte collected in r2 is converted from octal to decimal; and the results are displayed on the calculator readout.

APPENDIX C

ASCII CODE CHART

B7 B6 B5 / BITS B4 B3 B2 B1	Ø Ø Ø	Ø Ø 1	Ø 1 Ø	Ø 1 1	1 Ø Ø	1 Ø 1	1 1 Ø	1 1 1
	CONTROL		HIGH X & Y GRAPHIC INPUT		LOW X		LOW Y	
Ø Ø Ø Ø	NUL 0 (0)	DLE 10 (16)	SP 20 (32)	0 30 (48)	@ 40 (64)	P 50 (80)	\ 60 (96)	p 70 (112)
Ø Ø Ø 1	SOH 1 (1)	DC1 11 (17)	! 21 (33)	1 31 (49)	A 41 (65)	Q 51 (81)	a 61 (97)	q 71 (113)
Ø Ø 1 Ø	STX 2 (2)	DC2 12 (18)	" 22 (34)	2 32 (50)	B 42 (66)	R 52 (82)	b 62 (98)	r 72 (114)
Ø Ø 1 1	ETX 3 (3)	DC3 13 (19)	# 23 (35)	3 33 (51)	C 43 (67)	S 53 (83)	c 63 (99)	s 73 (115)
Ø 1 Ø Ø	EOT 4 (4)	DC4 14 (20)	$ 24 (36)	4 34 (52)	D 44 (68)	T 54 (84)	d 64 (100)	t 74 (116)
Ø 1 Ø 1	ENQ 5 (5)	NAK 15 (21)	% 25 (37)	5 35 (53)	E 45 (69)	U 55 (85)	e 65 (101)	u 75 (117)
Ø 1 1 Ø	ACK 6 (6)	SYN 16 (22)	& 26 (38)	6 36 (54)	F 46 (70)	V 56 (86)	f 66 (102)	v 76 (118)
Ø 1 1 1	BEL 7 (7)	ETB 17 (23)	' 27 (39)	7 37 (55)	G 47 (71)	W 57 (87)	g 67 (103)	w 77 (119)
1 Ø Ø Ø	BS 8 (8)	CAN 18 (24)	(28 (40)	8 38 (56)	H 48 (72)	X 58 (88)	h 68 (104)	x 78 (120)
1 Ø Ø 1	HT 9 (9)	EM 19 (25)	) 29 (41)	9 39 (57)	I 49 (73)	Y 59 (89)	i 69 (105)	y 79 (121)
1 Ø 1 Ø	LF A (10)	SUB 1A (26)	* 2A (42)	: 3A (58)	J 4A (74)	Z 5A (90)	j 6A (106)	z 7A (122)
1 Ø 1 1	VT B (11)	ESC 1B (27)	+ 2B (43)	; 3B (59)	K 4B (75)	[5B (91)	k 6B (107)	{ 7B (123)
1 1 Ø Ø	FF C (12)	FS 1C (28)	, 2C (44)	< 3C (60)	L 4C (76)	\ 5C (92)	l 6C (108)	¦ 7C (124)
1 1 Ø 1	CR D (13)	GS 1D (29)	- 2D (45)	= 3D (61)	M 4D (77)	] 5D (93)	m 6D (109)	} 7D (125)
1 1 1 Ø	SO E (14)	RS 1E (30)	. 2E (46)	> 3E (62)	N 4E (78)	^ 5E (94)	n 6E (110)	~ 7E (126)
1 1 1 1	SI F (15)	US 1F (31)	/ 2F (47)	? 3F (63)	O 4F (79)	_ 5F (95)	o 6F (111)	RUBOUT (DEL) 7F (127)