Serial 002

11000-SERIES PLUG-IN TO MAIN FRAME INTERFACE MANUAL

Specification 42-008

6 Mar 1985

Approved by Representatives of the following Projects:

Equivalent Time Main Frame Les Larson — Les Larson

Plug-In Units Dave Dobak — Dave Dobak

Real-Time Main Frame Lee Jalovec — Lee Jalovec

Transient Digitizer Main Frames Kirk Wimmer — Kirk Wimmer

11000-SERIES PLUG-IN TO MAIN FRAME INTERFACE MANUAL

VOLUME 1 - HARDWARE

TABLE OF CONTENTS

SECTION 1 - CONNECTOR

11000-SERIES
AUXILIARY COMPARTMENT

A38	Ground	R Ch 3 Auxiliary Trigger In -	B38
A37	Ground	R Ch 3 Auxiliary Trigger In +	B37
A36	L Ch 3 Auxiliary Trigger In +	Calibration Voltage	B36
A35	L Ch 3 Auxiliary Trigger In -	Calibration Ground Sense	B35
A34	Ground	R Ch 4 Auxiliary Trigger In +	B34
A33	Ground	R Ch 4 Auxiliary Trigger In -	B33
A32	L Ch 1 Auxiliary Trigger In +	Ground	B32
A31	L Ch 1 Auxiliary Trigger In -	Ground	B31
A30	-5V Power	R Ch 1 Auxiliary Trigger In -	B30
A29	-5V Power	R Ch 1 Auxiliary Trigger In +	B29
A28	L Ch 4 Auxiliary Trigger In -	Ground	B28
A27	L Ch 4 Auxiliary Trigger In +	Shield	B27
A26	Ground	R Ch 2 Auxiliary Trigger In +	B26
A25	Ground	R Ch 2 Auxiliary Trigger In -	B25
A24	L Ch 2 Auxiliary Trigger In -	Ground	B24
A23	L Ch 2 Auxiliary Trigger In +	Ground	B23
A22	Shield	Ground	B22
A21	SDI Clock	SDI Data, PI to MF	B21
A20	SDI Data, MF to PI	11k Detector	B20
A19	+50V Power	-50V Power	B19
A18	+15V Power	-15V Power	B18
A17	Aux Z Axis	Ground	B17
A16	Mainframe Mode Info	Not Used	B16
no pin			no pin
A14	Ground	+5.1V Power	B14
A13	+Trigger	-Trigger	B13
A12	Ground	Ground	B12
A11	+Display	-Display	B11
A10	+5.1V Power	Shield	B10
A9	+5.1V Power	Load Stop	B9
A8	+5.0V Power	Not Used	B8
A7	Not Used	Mainframe Chan Switch	B7
A6	Ground	Sequence Sync	B6
A5	Sequence Clock	Sample Clock	B5
A4	Line Trigger	Not Used	B4
A3	Not Used	Not Used	B3
A2	Ground	Not Used	B2
A1	Sweep Gate	Not Used	B1

11000-SERIES

VERTICAL COMPARTMENTS

A38	Ground	Ch 1 Auxiliary Trigger Out +	B38
A37	Ground	Ch 1 Auxiliary Trigger Out -	B37
A36	Ch 2 Auxiliary Trigger Out +	Calibration Voltage	B36
A35	Ch 2 Auxiliary Trigger Out -	Calibration Ground Sense	B35
A34	Ground	Ch 3 Auxiliary Trigger Out +	B34
A33	Ground	Ch 3 Auxiliary Trigger Out -	B33
A32	Ch 4 Auxiliary Trigger Out +	Ground	B32
A31	Ch 4 Auxiliary Trigger Out -	Ground	B31
A30	-5V Power		no pin
A29	-5V Power		no pin
no pin			no pin
no pin			no pin
no pin			no pin
no pin			no pin
no pin			no pin
no pin			no pin
A22	Shield	Ground	B22
A21	SDI Clock	SDI Data, PI to MF	B21
A20	SDI Data, MF to PI	11k Detector	B20
A19	+50V Power	-50V Power	B19
A18	+15V Power	-15V Power	B18
A17	Aux Z Axis	Ground	B17
A16	Mainframe Mode Info	Not Used	B16
no pin			no pin
A14	Ground	+5.1V Power	B14
A13	+Trigger	-Trigger	B13
A12	Ground	Ground	B12
A11	+Display	-Display	B11
A10	+5.1V Power	Shield	B10
A9	+5.1V Power	Not Used	B9
A8	+5.0V Power	Not Used	B8
A7	Not Used	Mainframe Chan Switch	B7
A6	Ground	Sequence Sync	B6
A5	Sequence Clock	Not Used	B5
A4	Line Trigger	Not Used	B4
A3	Not Used	Not Used	B3
A2	Ground	Not Used	B2
A1	Not Used	Not Used	B1

SWEEP GATE (Aux Compartment only)

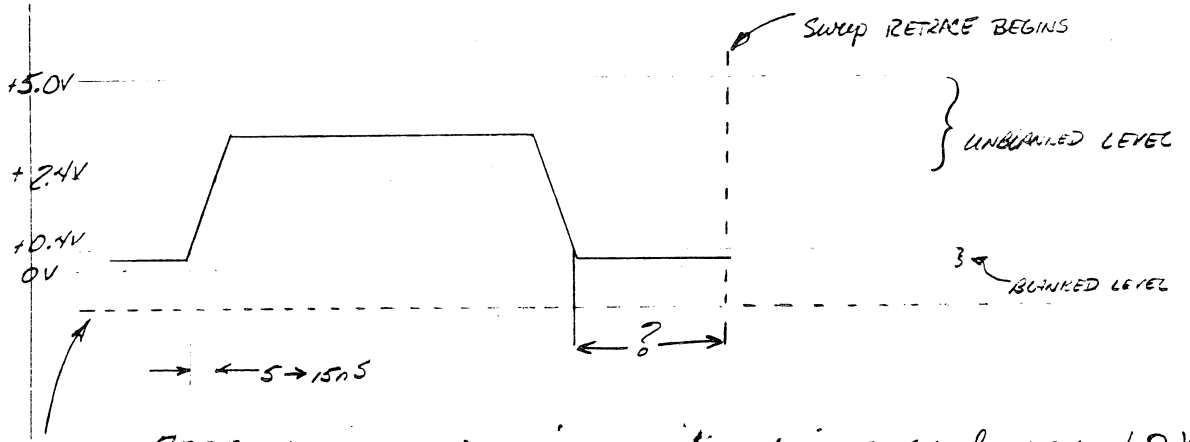
Sweep Gate, A1, is generated by the Aux plug-in unit and used by the main frame to generate crt unblanking signals and enable sampling in digitizing main frames. Sweep Gate is required only in the Aux plug-in compartment.

Special Considerations

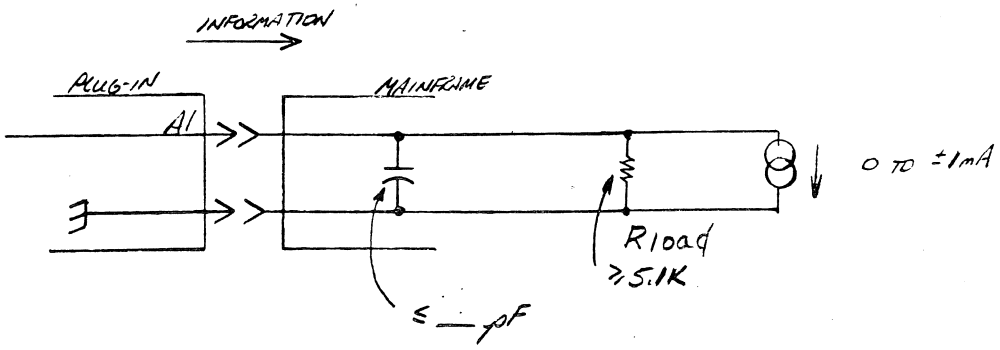
1. Plug-in units that generate no sweep and produce no display must tie pin A1 to ground, or leave pin A1 unconnected.

2. Plug-in units that produce no sweep but whose output should be displayed (vertical amplifiers) must connect pin A1 to pin A8 (+5 V) to unblank the crt.

3. Plug-in units that generate a sweep to be displayed on the crt or to indicate a "sweep time" must obey the specifications given below.



7000-series plug-in units drive as low as -1.0 V. 11000 main frames must withstand this input voltage. Maximum current is unknown.



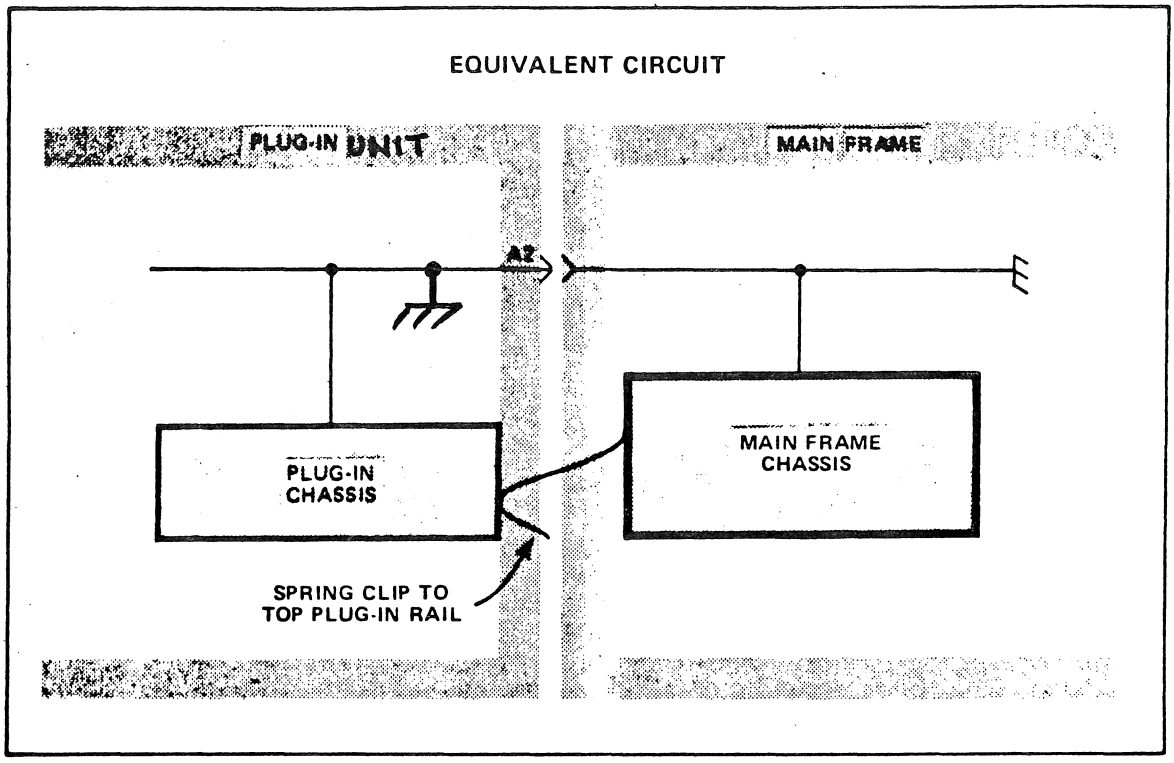
For all main frames, the voltage on A1 must meet the specifications for Blanked Level when no plug-in unit is installed. Rload may be connected to a negative supply to bring A1 within its required voltage range.

NOT USED

All 11k plug-in units and main frames are prohibited from making any connection to this contact.

GROUND

Ground, A2.



NOT USED

For details, see pin B1.

A3

NOT USED

For details, see pin B1.

NOT USED

For details, see pin B1.

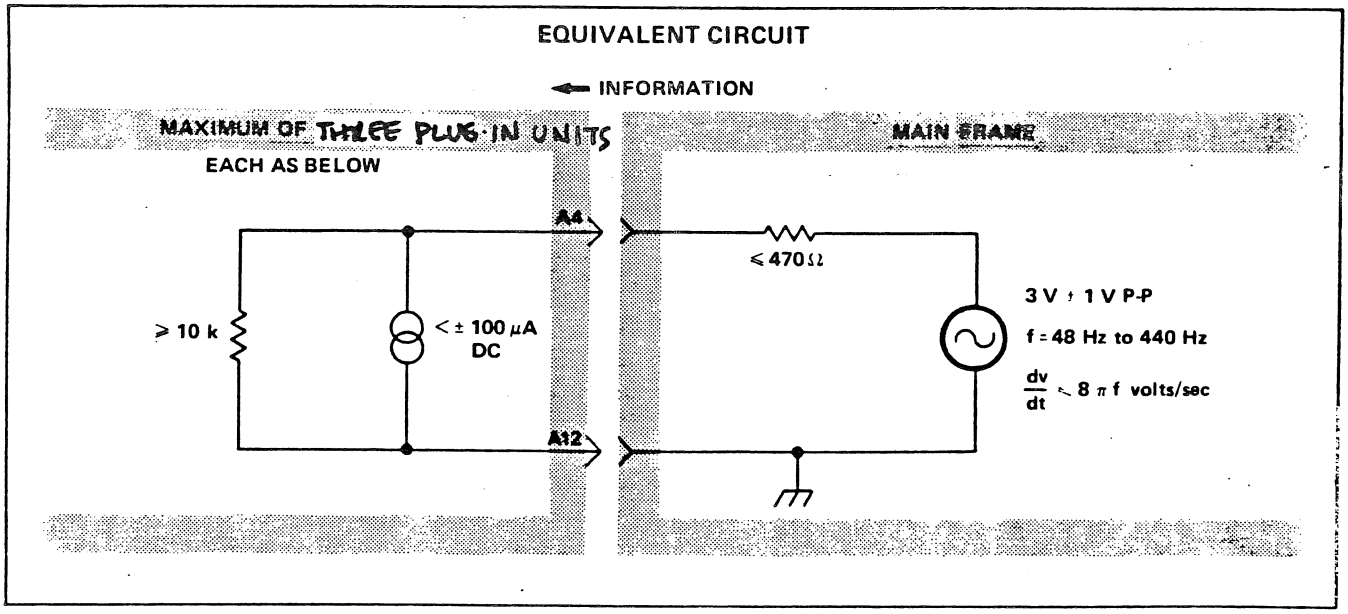
A4

LINE TRIGGER

Line Trigger, A4, supplies a line trigger signal to the plug-in units.

Main Frame Considerations:

Phasing	Line Trigger will be positive-going when the line, or phase, conductor is positive-going.
Maximum Noise	25 mV rms, measured tangentially, 20 Hz to 1 kHz.
Power Line Isolation	3750 V rms, at 60 Hz for one minute.



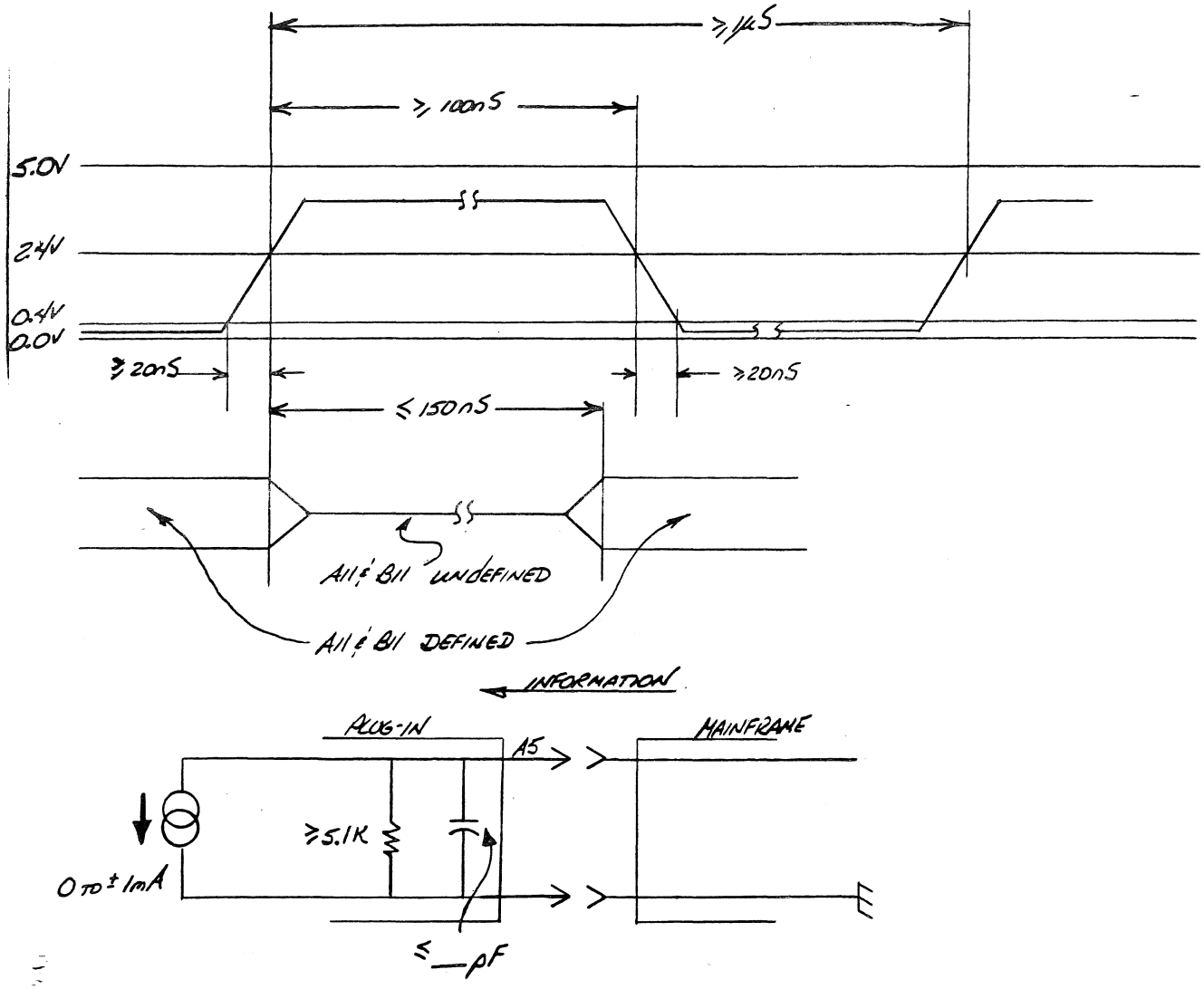
NOT USED

For details, see pin B1.

SEQUENCE CLOCK

Sequence Clock, A5, is generated by the main frame and used to advance multi-channel plug-in units through display sequences.

For details about the main frame switching, see Section 4, Channel Switching Logic.

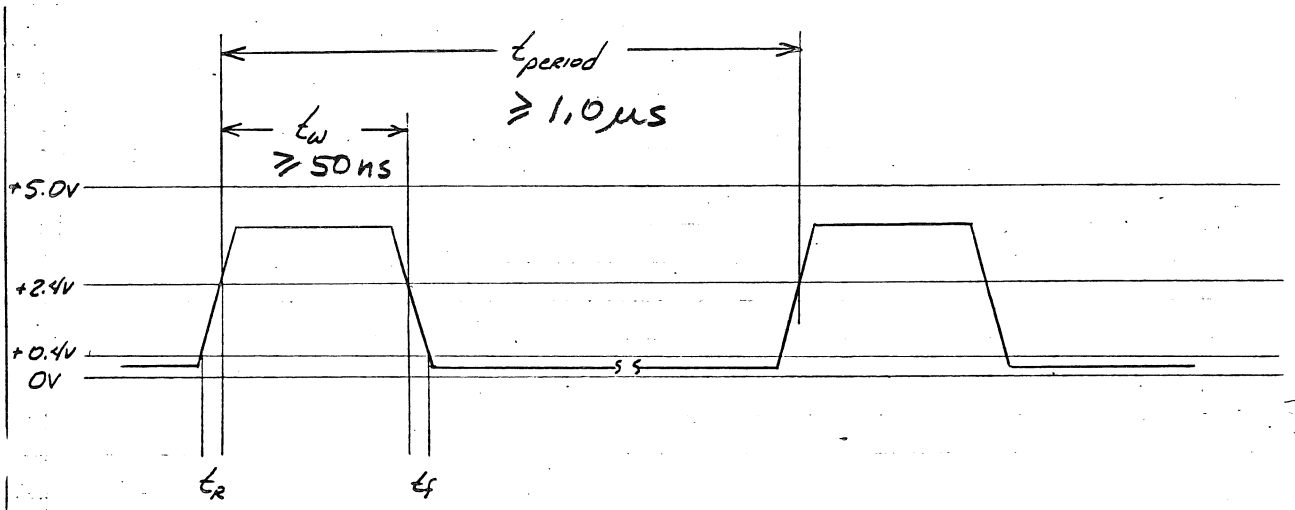


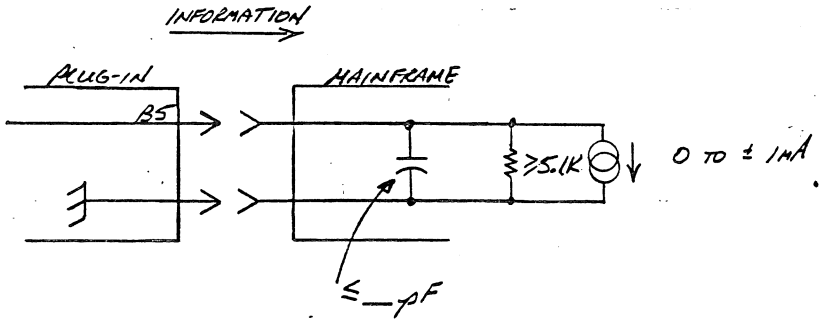
NOTE: MAINFRAME DRIVES A5 OF ALL PLUG-IN COMPARTMENTS IN PARALLEL.

SAMPLE CLOCK (Aux Compartment only)

Sample Clock, B5, originates in a plug-in unit in the Aux plug-in compartment.

The positive transition of Sample Clock initiates sampling activity in the main frame.





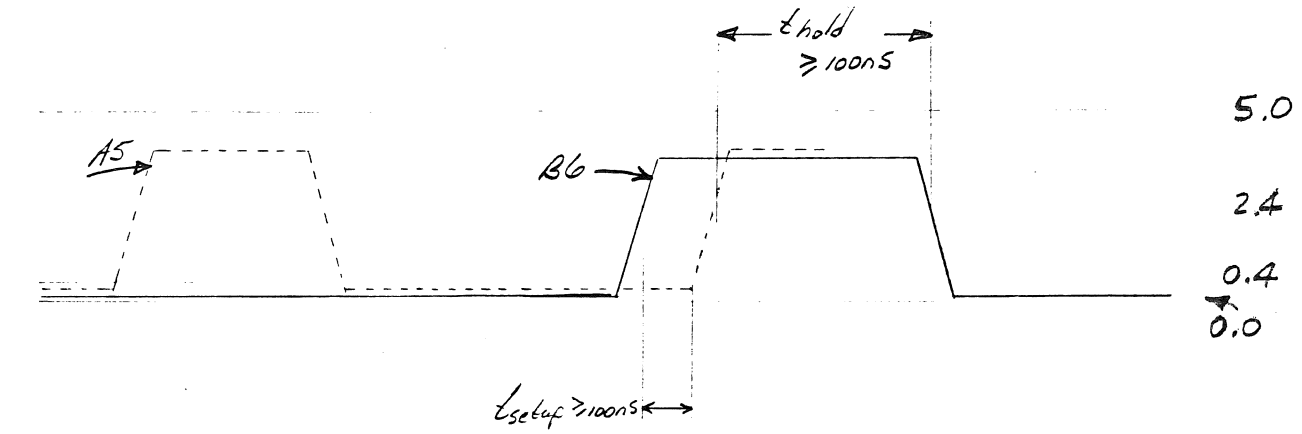
GROUND

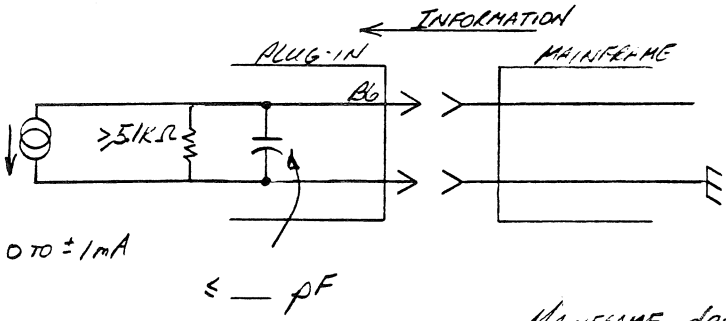
For equivalent circuit, see A2, Ground.

SEQUENCE SYNC

Sequence Sync, B6, is generated by the main frame. Multi-channel plug-in units use Sequence Sync to synchronize their display sequence with the main-frame display sequence.

For more detail about the Sequence Sync function, see Section 4, Channel Switching Logic.





MAINFRAME drives B6 of all plug-in units in parallel.

A7

NOT USED

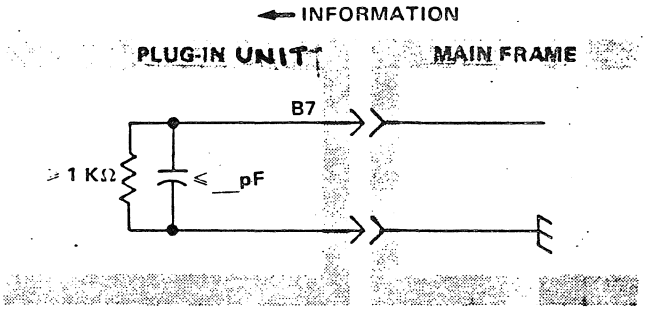
For details, see pin B1.

MAIN FRAME CHANNEL SWITCH SIGNAL

The Main Frame Channel Switch Signal, B7, is generated by the main frame logic; there are two versions of this signal. One version goes to the left and right vertical plug-in compartments; the other goes to the Auxiliary compartment.

For details about the Main Frame Channel Switching Signal, see Section 4, Channel Switching Logic.

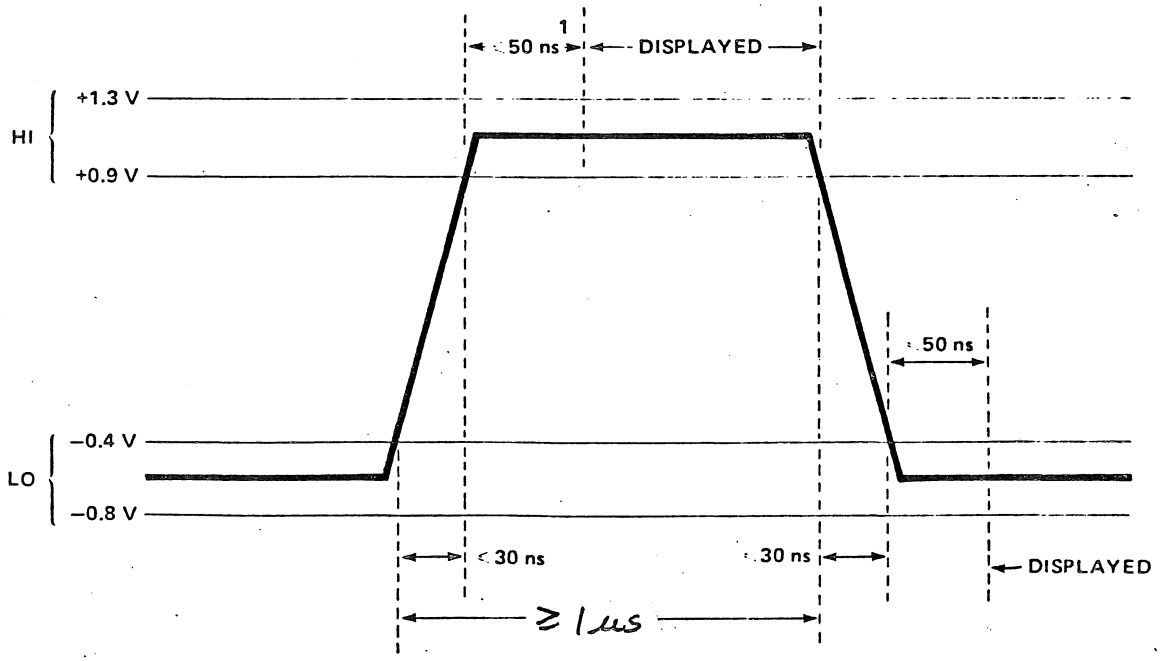
EQUIVALENT CIRCUIT



TRUTH TABLE

B7	A16	DISPLAY
Low	Low	No
Low	High	Yes
High	Low	Yes
High	High	No

WAVEFORM



[1] Some 7000-Series Amplifiers may not meet this specification.

+5.Ø V POWER

Refer to Section 2, Power Supplies, in this manual, for information about power-supply parameters.

NOT USED

For details, see pin B1.

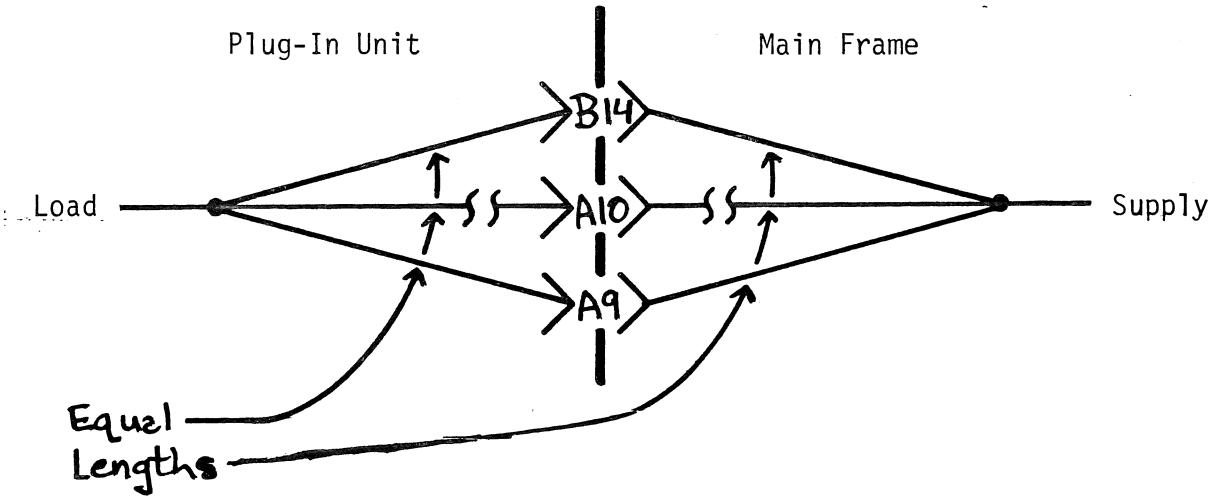
A9, A1Ø, B14

+5.1 V POWER

Refer to Power Supplies, in this manual, for information about power-supply parameters.

The +5.1 V Power is routed separately to each plug-in compartment. This contrasts with the other power supplies, which are bused to all three plug-in compartments.

Three pins furnish +5.1 V Power. It is essential that these pins share the load current equally. To accomplish this, both the main frame Interface Board and the plug-in unit must incorporate a "star" connection to these pins, with equal resistance from each pin to the center of the star. See illustration below.

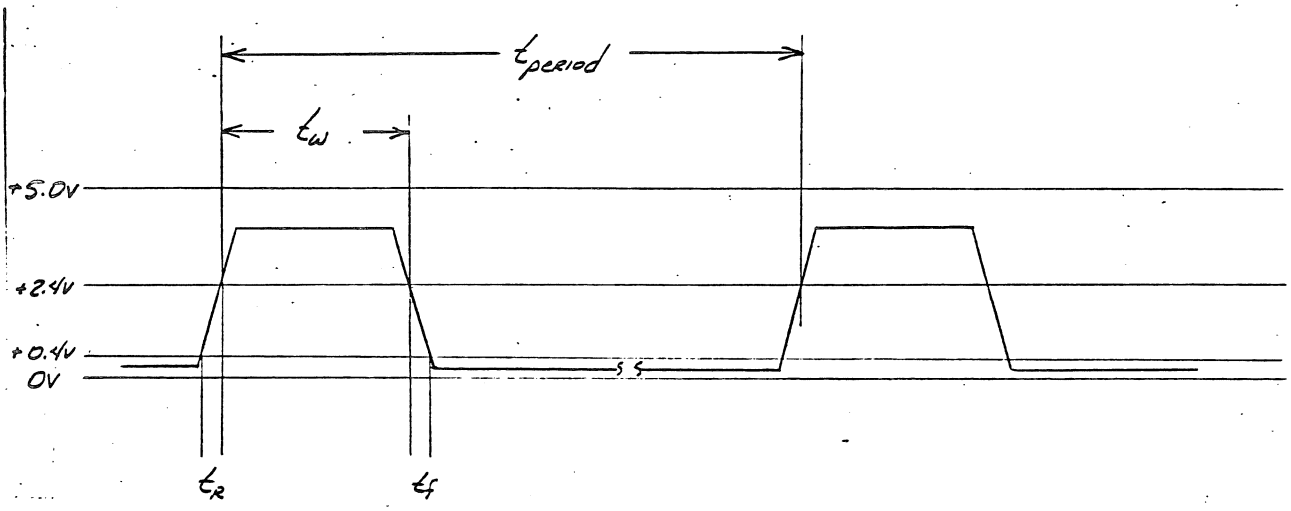


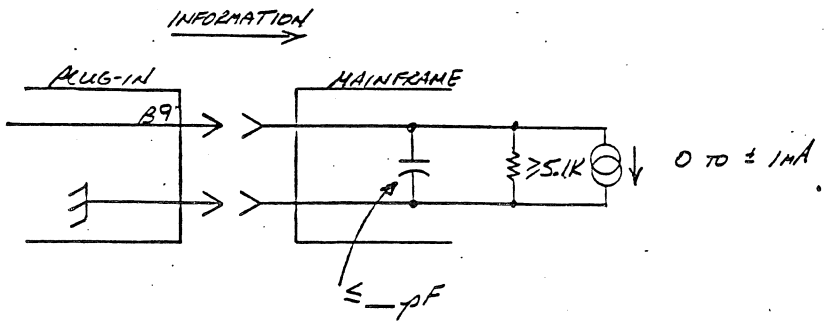
LOAD STOP (Aux Compartment only)

Load Stop, B9, originates in a plug-in unit in the Aux plug-in compartment.

Load Stop will be low during an acquisition (clocks enabled), and and high after an acquisition (clocks disabled).

7000-Series plug-in units drive as low as -1.0 V. 11000-Series main frames must withstand this input voltage. Maximum current is unknown.





+5.1 V POWER

See A9 for details.

SHIELD

Pin B1Ø provides shielding and constant impedance between adjacent pins. It will be grounded in any plug-in unit. Pin B1Ø will not be connected in any main frame.

A11

DISPLAY +

Display +, A11, provides signal input to the mainframe. A positive transition on A11 deflects the trace up or to the right.

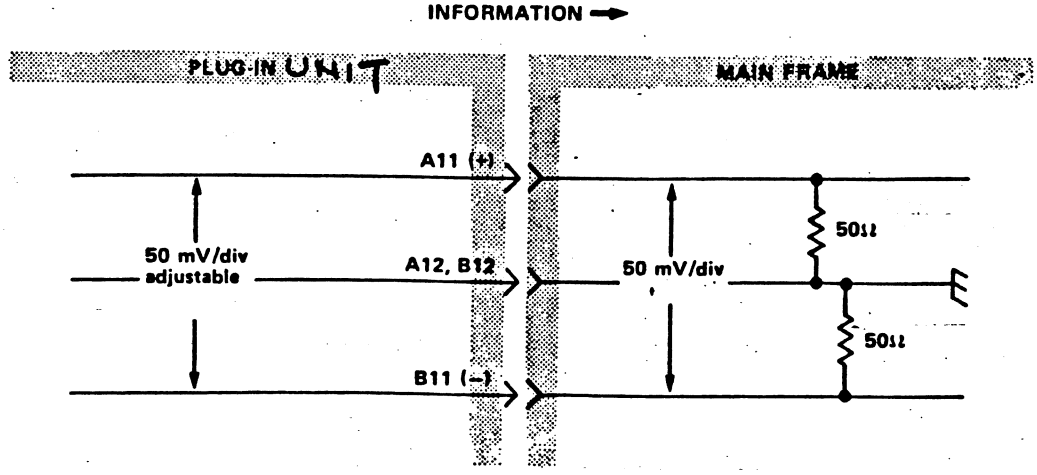
DC Considerations:

Deflection Factor	50 mV/div +/- 1% differential.
Input Resistance	
A11 to A12, B12	50 ohms +/- 1%.
B11 to A12, B12	50 ohms +/- 1%.
A11 to B11	100 ohms +/- 1%.
A11 shorted to B11 to A12, B12	25 ohms +/- 10%.
Usable Signal Limit (all ac & dc specs apply)	+/- 9 divisions.
Maximum Signal Limit	+/- 15 divisions.
DC Centering	+/- 0.2 division of graticule center.
Maximum Input DC Common Mode Component	75 mV or less. (7000-series plug-in units may provide up to 150 mV; 11000-series mainframes must withstand it.)

AC Considerations:

TDR (push-pull, t(sub)r equal to 0.35/1.5 times mainframe bandwidth)	<2% up to 250 MHz. <10% above 250 MHz.
CMRR to BW (for full-screen signal)	> 100:1 up to 250 MHz. > 50:1 above 250 MHz, with plug-in unit back-terminated.
Timing Match	See Section 5, Time Match of Display and Trigger Signals.

EQUIVALENT CIRCUIT



DISPLAY –

Display –, B11, provides signal input to the main frame. A negative transition on B11 deflects the trace up or to the right.

For specifications and equivalent circuit, see A11, Display +.

GROUND

For equivalent circuit see A2, Ground.

GROUND

For equivalent circuit see A2, Ground.

A13

+ TRIGGER

+ Trigger, A13, provides trigger input to the main frame.

DC Considerations:

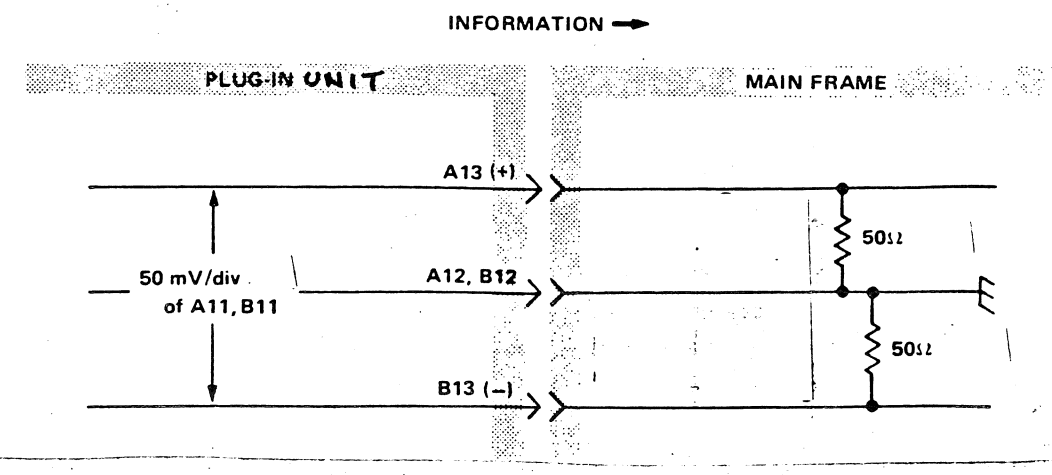
Main Frame:	
Deflection Factor	50 mV/div +/- 1% differential.
Input Resistance	
A13 to A12, B12	50 ohms +/- 1%.
B13 to A12, B12	50 ohms +/- 1%.
A13 to B13	100 ohms +/- 1%.
A13 shorted to B13 to A12, B12	25 ohms +/- 10%.
Usable Signal Limit (all specifications apply)	+/- 9 divisions.
Maximum Signal Limit	+/- 15 divisions.
DC Centering	+/- 0.2 division of signal on A11 & B11.
Maximum Input DC Common Mode Component	75 mV or less. (7000-series plug-in units may provide up to 150 mV; 11000-series main frames must withstand it.)
Plug-In Unit:	
Deflection Factor	Within 1% of signal on A11 and B11.
Variable Volts/Div	Varies with display channel.
Invert	Does not invert with display channel.
Bandwidth Limit	Limits with display channel.

AC Considerations:

TDR (push-pull, t(sub)r equal to 0.35/1.5 times main frame bandwidth)	<2% up to 250 MHz. <10% above 250 MHz. *
CMRR to BW (for full-screen signal)	> 100:1 up to 250 MHz. > 50:1 above 250 MHz. *
Timing Match	See Section 5, Time Match of Display and Trigger Signals.

* Plug-in unit should be back-terminated.

EQUIVALENT CIRCUIT



– TRIGGER

– Trigger, B13, provides trigger input to the main frame.

For specifications and equivalent circuit, see A13.

GROUND

For equivalent circuit see A2, Ground.

+5.1 V POWER

See A9 for details.

A15

NO PIN

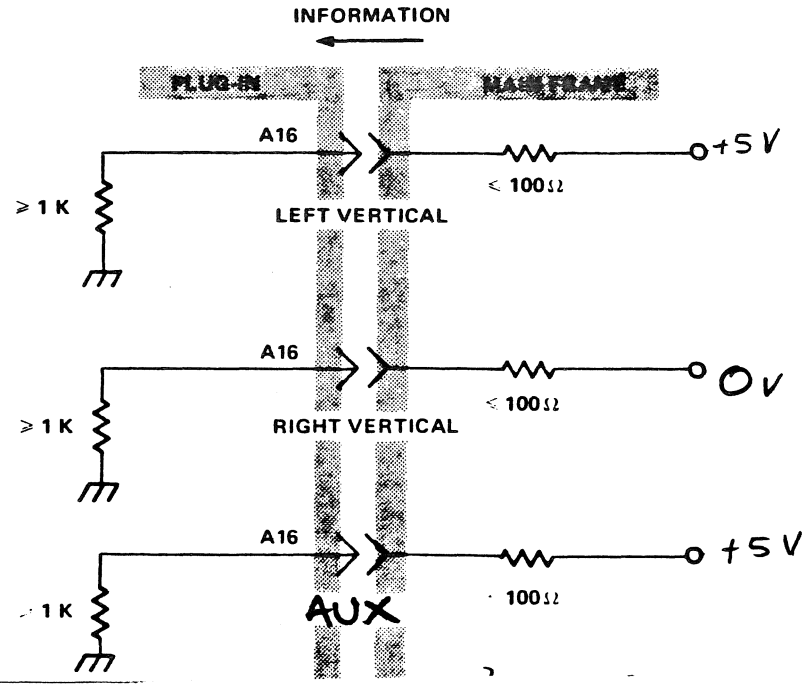
NO PIN

A16

MAIN FRAME MODE INFO

Main Frame Mode Info, A16 (with B7, Main Frame Channel Switch), permits the plug-in units to determine when their outputs are being displayed. This information is needed when Aux Z Axis, A17, is being used to ensure that only the displayed plug-in unit is modifying the Z Axis signal.

EQUIVALENT CIRCUIT



TRUTH TABLE

B7	A16	DISPLAY
Low	Low	NO
Low	High	Yes
High	Low	Yes
High	High	NO

High = +5 V ± 0.2 V

Low = 0 TO −1 V

NOT USED

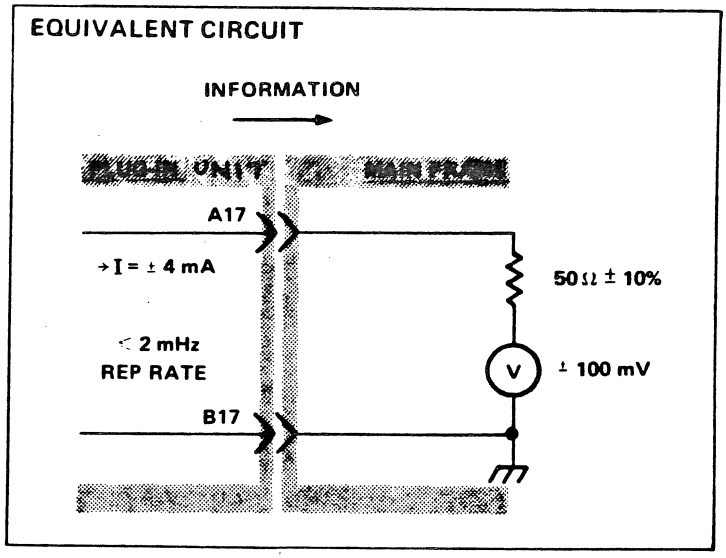
For details, see pin B1.

A17

AUX Z AXIS

Aux Z Axis, A17, is used by the plug-in unit to intensity modulate the display. The Aux Z Axis signal will dim (+i) or brighten (-i) the display from the level set by the main frame Intensity control (i.e., about +4 mA will extinguish a maximum intensity trace or invalidate a sample in a digitizing main frame). When no display is selected from a plug-in unit, the current in line A17 must be zero.

A17 is used in conjunction with Main Frame Mode Infr, A16, and Main Frame Channel Switch, B7.



GROUND

For equivalent circuit see A2, Ground.

+15 V POWER

+15 V Power. Refer to Section 2, Power Supplies, in this manual, for information about power supply parameters.

-15 V POWER

-15 V Power. Refer to Section 2, Power Supplies, in this manual, for information about power supply parameters.

+5Ø V POWER

+5Ø V Power. Refer to Section 2, Power Supplies, in this manual, for information about power supply parameters.

-5Ø V POWER

-5Ø V Power. Refer to Section 2, Power Supplies, in this manual, for information about power supply parameters.

A2Ø

SDI DATA, MAIN FRAME to PI

SDI Data, Main Frame to PI, consists of TTL levels which are transferred to the plug-in unit on the positive transition of SDI Clock (A21).

Most 7ØØØ-series plug-in units load pin A2Ø (SDI Data, Main Frame to PI) 5Ø ohms or less to ground. The main frame must be able to withstand a short to ground on pin A2Ø without hardware damage and without impairing the operation of any other plug-in unit.

The SDI is described in Section 3, Serial Data Interface.

11k DETECTOR

Each 11ØØØ-series plug-in unit will connect pin B2Ø through a 1Ø k ohm resistor to +5 or +5.1 volts.

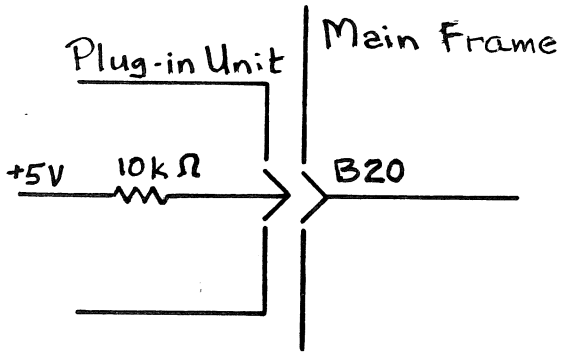
This feature provides a simple hardware detector. It allows the main frame to distinguish between two situations, as follows:

1. 11ØØØ-series plug-in unit, with defective SDI, installed in compartment; or
2. compartment contains either 7ØØØ-series plug-in unit or is empty.

In 7ØØØ-series plug-in units, pin B2Ø is connected directly to ground, connected to ground via 5Ø ohms, or left unconnected.

Any main frame may:

* use or ignore this information;
* sense as many other lines as needed to play the guessing game to determine which 7ØØØ-series plug-in unit is installed.



SDI CLOCK

SDI Clock, A21, is a 4 MHz, 50% duty cycle, TTL-level free-running signal.

In some 7k plug-in units, pin A21 (SDI Clock) is connected to ground. (The 7D10, 7D11, 7D14, 7S14, and possibly some others have pin A21 grounded.) The main frame must be able to withstand this ground without affecting the operation of any other plug-in unit(s). The means by which this is accomplished is left to the main frame designer.

Other 7k plug-in units have pin A21 connected to B21. No problem arises if A21 is connected to pin B21 but not to ground; the SDI Clock simply drives the data input.

The SDI is described in Section 3, Serial Data Interface.

SDI DATA, PI to MAIN FRAME

SDI Data, PI to Main Frame, consists of TTL levels which are transferred to the main frame on the positive transition of SDI Clock (A21).

Many 7k plug-in units ground pin B21 or connect it to pin A21, SDI Clock.

The SDI is described in Section 3, Serial Data Interface.

SHIELD

Pin A22 provides shielding and constant impedance between adjacent pins. Pin A22 will be grounded in any plug-in unit which uses the Auxiliary Trigger signal on pin A23. Pin A22 will not be connected in the main frame.

Pin A22 cannot be connected to ground in the main frame because the 7D15 and the 7D12 drive it with TTL levels.

GROUND

For equivalent circuit see A2, Ground.

A23

LEFT CH 2 AUXILIARY TRIGGER IN + (Aux Compartment only)

Pin A23 is Left Ch 2 Auxiliary Trigger In + in the Aux compartment only. There is no pin A23 in the L & R vertical plug-in compartments.

For specifications and equivalent circuit, see Section 5, Time Match of Display and Trigger Signals.

GROUND (Aux Compartment only)

Pin B23 is Ground in the Aux plug-in compartment only. There is no pin B23 in the L & R vertical compartments.

A24

LEFT CH 2 AUXILIARY TRIGGER IN - (Aux Compartment only)

Pin A24 is Left Ch 2 Auxiliary Trigger In - in the Aux compartment only. There is no pin A24 in the L & R vertical plug-in compartments.

For specifications and equivalent circuit, see Section 5, Timing of Display and Trigger Signals.

GROUND (Aux Compartment only)

Pin B24 is Ground in the Aux plug-in compartment only. There is no pin B24 in the L & R vertical compartments.

A25

GROUND (Aux Compartment only)

Pin A25 is Ground in the Aux plug-in compartment only. There is no pin A25 in the L & R vertical compartments.

RIGHT CH 2 AUXILIARY TRIGGER IN - (Aux Compartment only)

Pin B25 is Right Ch 2 Auxiliary Trigger In - in the Aux compartment only. There is no pin B25 in the L & R vertical plug-in compartments.

For specifications and equivalent circuit, see Section 5, Timing of Display and Trigger Signals.

GROUND (Aux Compartment only)

Pin A26 is Ground in the Aux plug-in compartment only. There is no pin A26 in the L & R vertical compartments.

RIGHT CH 2 AUXILIARY TRIGGER IN + (Aux Compartment only)

Pin B26 is Right Ch 2 Auxiliary Trigger In + in the Aux compartment only. There is no pin B26 in the L & R Vertical compartments.

For specifications and equivalent circuit, see Section 5, Time Match of Display and Trigger Signals.

A27

LEFT CH 4 AUXILIARY TRIGGER IN + (Aux Compartment only)

Pin A27 is Left Ch 4 Auxiliary Trigger In + in the Aux compartment only. There is no pin A27 in the L & R vertical plug-in compartments.

For specifications and equivalent circuit, see Section 5, Time Match of Display and Trigger Signals.

SHIELD (Aux Compartment only)

Pin B27 is Shield in the Aux plug-in compartment only. There is no pin B27 in the L & R vertical compartments.

Pin B27 provides shielding and constant impedance between adjacent pins. It will be grounded in any plug-in unit which uses the Auxiliary Trigger signal on pin B26. Pin B27 will not be connected in the main frame.

Pin B27 should not be connected to ground in the main frame, because it will short circuit the +5 V supply if a 7B90P or a 7A16P is installed.

A28

LEFT CH 4 AUXILIARY TRIGGER IN - (Aux Compartment only)

Pin A28 is Left Ch 4 Auxiliary Trigger In - in the Aux compartment only. There is no pin A28 in the L & R vertical plug-in compartments.

For specifications and equivalent circuit, see Section 5, Time Match of Display and Trigger Signals.

GROUND (Aux Compartment only)

Pin B28 is Ground in the Aux plug-in compartment only. There is no pin B28 in the L & R vertical compartments.

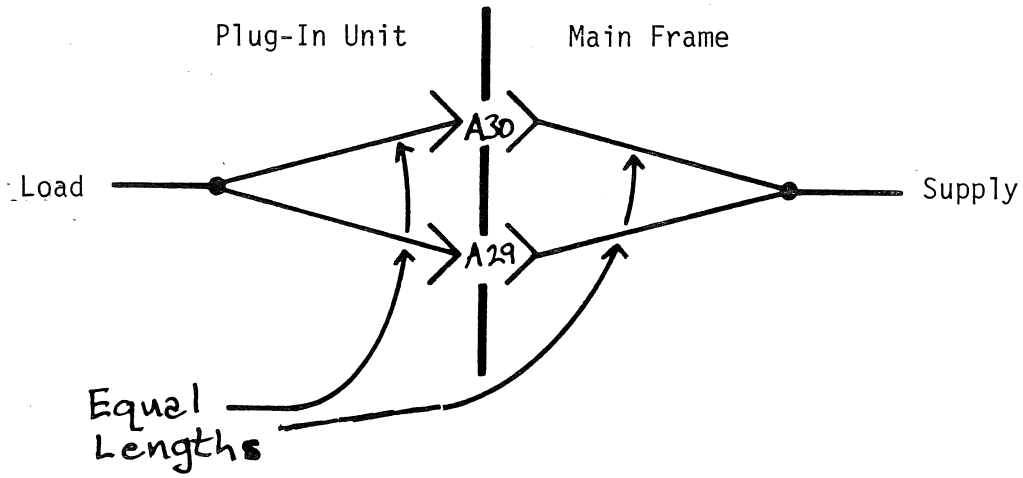
A29, A3Ø

-5.Ø V POWER

Pins A29 and A3Ø furnish -5.Ø V to the plug-in units.

It is essential that pins A29 and A3Ø share the load current equally. To accomplish this, both the main frame Interface Board and the plug-in unit must incorporate a "star" connection to pins A29 and A3Ø. The star must have equal resistance from pin A29 and A3Ø to the center of the star. The illustration below depicts a star connection.

For specifications and equivalent circuit, see Section 2, Power Supplies.



RIGHT CH 1 AUXILIARY TRIGGER IN + (Aux Compartment only)

Pin B29 is Right Ch 1 Auxiliary Trigger In + in the Aux compartment only. There is no pin B29 in the L & R vertical plug-in compartments.

For specifications and equivalent circuit, see Section 5, Time Match of Display and Trigger Signals.

A30, A29

-5.0 V POWER

See pin A29 for details.

RIGHT CH 1 AUXILIARY TRIGGER IN - (Aux Compartment only)

Pin B3Ø is Right Ch 1 Auxiliary Trigger In - in the Aux compartment only. There is no pin B3Ø in the L & R vertical plug-in compartments.

For specifications and equivalent circuit, see Section 5, Time Match of Display and Trigger Signals.

A31

CH 4 AUXILIARY TRIGGER OUT – (L & R Vert Compartments)
or
LEFT CH 1 AUXILIARY TRIGGER IN – (Aux Compartment only)

In the left and right vertical plug-in compartments, pin A31 accepts the Ch 4 Auxiliary Trigger Out – from the right or left vertical plug-in units.

In the Auxiliary plug-in compartment, pin A31 delivers the trigger outputs from the plug-in unit in the left vertical plug-in compartment.

For specifications and equivalent circuit, see Section 5, Time Match of Display and Trigger Signals.

GROUND

For equivalent circuit see A2, Ground.

A32

CH 4 AUXILIARY TRIGGER OUT + (L & R Vert Compartments)
or
LEFT CH 1 AUXILIARY TRIGGER IN + (Aux Compartment only)

In the left and right vertical plug-in compartments, pin A32 accepts the Ch 4 Auxiliary Trigger Out + from the right or left vertical plug-in units.

In the Auxiliary plug-in compartment, pin A32 delivers the trigger outputs from the plug-in unit in the left vertical plug-in compartment.

For specifications and equivalent circuit, see Section 5, Time Match of Display and Trigger Signals.

GROUND

For equivalent circuit see A2, Ground.

GROUND

For equivalent circuit see A2, Ground.

CH 3 AUXILIARY TRIGGER OUT - (L & R Vert Compartments)
or
RIGHT CH 4 AUXILIARY TRIGGER IN - (Aux Compartment only)

In the left and right vertical plug-in compartments, pin B33 accepts the Ch 3 Auxiliary Trigger Out - from the resident plug-in unit.

In the Auxiliary plug-in compartment, pin B33 delivers the trigger outputs from the plug-in unit in the right vertical plug-in compartment.

For specifications and equivalent circuit, see Section 5, Time Match of Display and Trigger Signals.

GROUND

For equivalent circuit see A2, Ground.

CH 3 AUXILIARY TRIGGER OUT + (L & R Vert Compartments)
or
RIGHT CH 4 AUXILIARY TRIGGER IN + (Aux Compartment only)

In the left and right vertical plug-in compartments, pin B34 accepts the Ch 3 Auxiliary Trigger Out - from the resident plug-in unit.

In the Auxiliary plug-in compartment, pin B34 delivers the trigger outputs from the plug-in unit in the right vertical plug-in compartment.

For specifications and equivalent circuit, see Section 5, Time Match of Display and Trigger Signals.

A35

CH 2 AUXILIARY TRIGGER OUT – (L & R Vert Compartments)
or
LEFT CH 3 AUXILIARY TRIGGER IN – (Aux Compartment only)

In the left and right vertical plug-in compartments, pin A35 accepts the Ch 2 Auxiliary Trigger Out – from the resident plug-in unit.

In the Auxiliary plug-in compartment, pin A35 delivers the trigger outputs from the plug-in unit in the left vertical plug-in compartment.

For specifications and equivalent circuit, see Section 5, Time Match of Display and Trigger Signals.

CALIBRATION GROUND SENSE

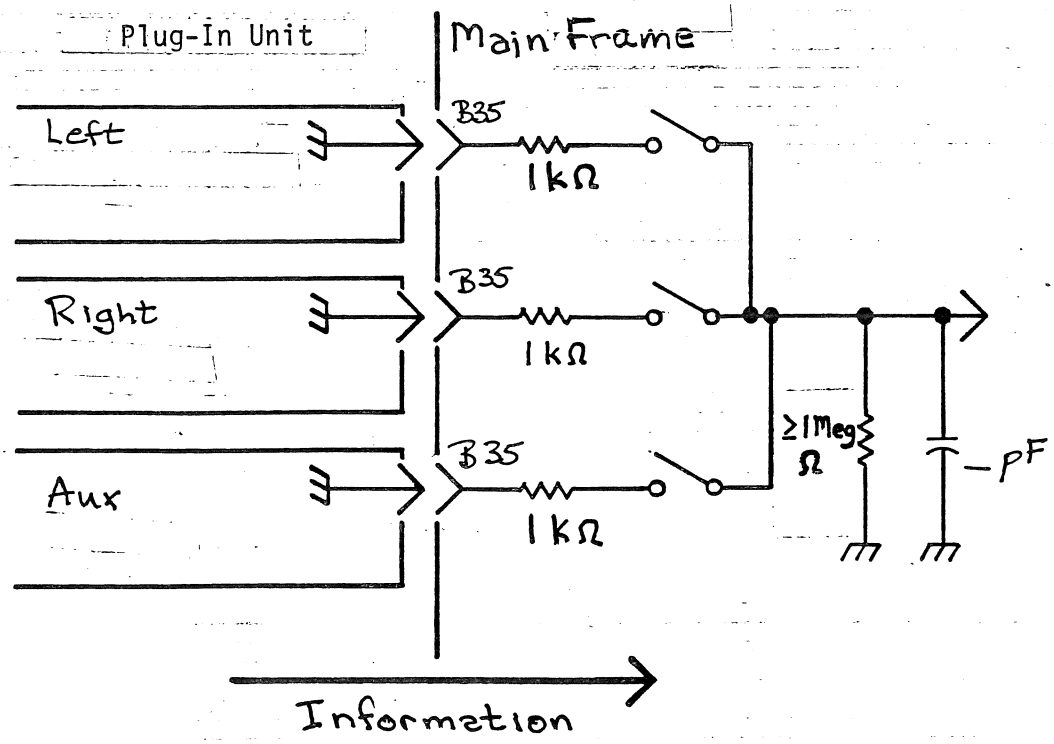
The Calibration Ground Sense line, B35, provides a means of sensing the actual voltage to which the Calibration Voltage is referenced.

When assigned to a plug-in compartment, the calibration voltage system will track Calibration Ground Sense over a range of +/-1ØØ mV.

When not assigned to a plug-in compartment, the calibration voltage system will isolate Calibration Ground Sense over a range of +/-5 V.

Some 7k plug-in units (7T11) connect +5 V to pin B35. The main frame must be able to withstand this without affecting the operation of any other plug-in unit. The main frame designers are solely responsible for accomplishing this.

The Calibration Ground Sense line can be connected to only one plug-in compartment at a time. Therefore, it follows that the Calibration Voltage is available, with specified accuracy, to only one plug-in compartment at any time.



A36

CH 2 AUXILIARY TRIGGER OUT + (L & R Vert Compartments)
or
LEFT CH 3 AUXILIARY TRIGGER IN + (Aux Compartment only)

In the left and right vertical plug-in compartments, pin A36 accepts the Ch 2 Auxiliary Trigger Out + from the resident plug-in unit.

In the Auxiliary plug-in compartment, pin A36 delivers the trigger outputs from the plug-in unit in the right vertical plug-in compartment.

For specifications and equivalent circuit, see Section 5, Time Match of Display and Trigger Signals.

CALIBRATION VOLTAGE

The Calibration Voltage provides accurate voltages for calibrating plug-in amplifiers, and for making other measurements which plug-in units may require.

Specifications:

Output Resistance:	50 ohms, +/-0.1%, at pin B36.
Full-Scale Voltages Available:	+/-25, 50, 100, 250, and 500 mV; and 1, 2.5, 5, and 10 V.
Voltage Range:	Negative full scale to positive full scale minus 1 LSB.
Resolution:	12 bits (1/4096th of full scale).
Settling Time (to 12-bit accuracy):	1 ms at pin B36.
Absolute Accuracy:	+/-0.2% of full scale at pin B36.
Voltage Output Limit:	+/-10 V into 1 MΩ; +/-5 V into 50 Ω.
Current Output Limit:	at least +/-100 mA.
Offset:	tbd
Noise:	tbd

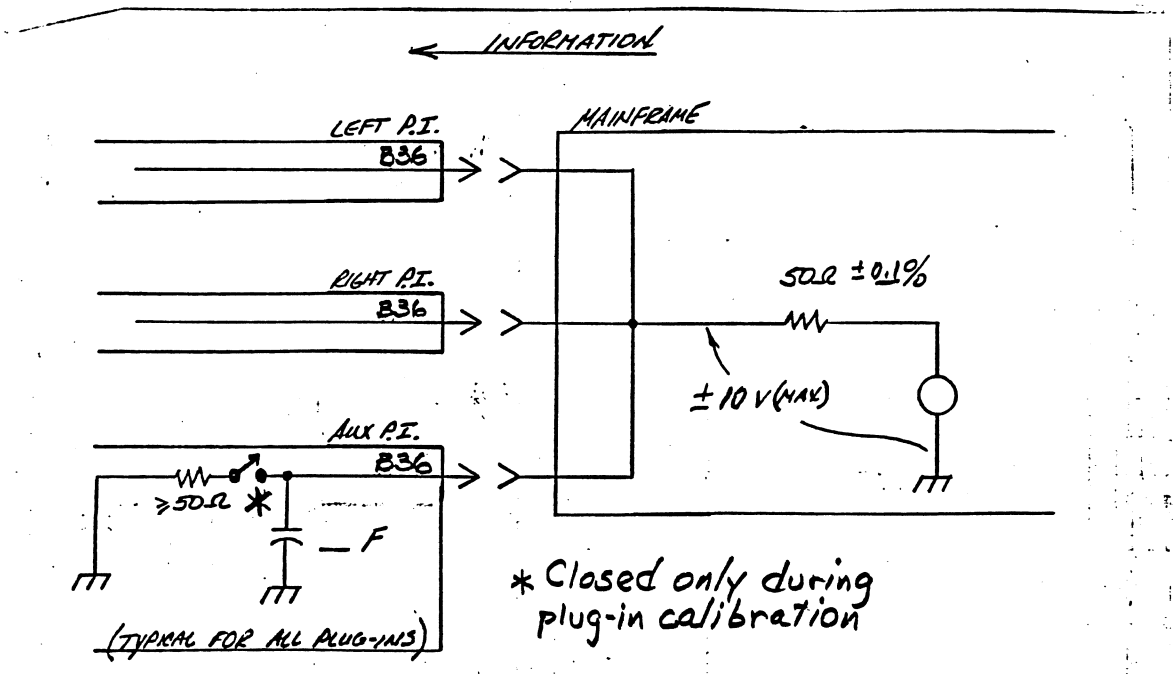
Although the Calibration Voltage is always connected to all three plug-in compartments, the accuracy specifications apply only to the compartment to which the Calibration Ground Sense is connected.

Resolution: The resolution of the Calibration Voltage, as stated previously, is at least 12 bits, and the range is at least +/-5 divisions, minus 1 LSB, for deflection factors up to 2 V/division.

Because the resolution of the Calibration Voltage might not be an even multiple of 100 points per division, the mainframe's behavior will follow this sequence:

Plug-in unit requests Calibration Voltage (floating-point value);
Mainframe rounds to nearest achievable value;
Mainframe sets Calibration Voltage accordingly; and
Mainframe notifies plug-in unit of floating-point value.

Rules for loading: TBD



GROUND

For equivalent circuit see A2, Ground.

CH 1 AUXILIARY TRIGGER OUT - (L & R Vert Compartments)
or
RIGHT CH 3 AUXILIARY TRIGGER IN + (Aux Compartment only)

In the left and right vertical plug-in compartments, pin B37 accepts the Ch 1 Auxiliary Trigger Out - from the resident plug-in unit.

In the Auxiliary plug-in compartment, pin B37 delivers the trigger outputs from the plug-in unit in the right vertical plug-in compartment.

For specifications and equivalent circuit, see Section 5, Time Match of Display and Trigger Signals.

GROUND

For equivalent circuit see A2, Ground.

CH 1 AUXILIARY TRIGGER OUT + (L & R Vert Compartments)
or
RIGHT CH 3 AUXILIARY TRIGGER IN - (Aux Compartment only)

In the left and right vertical plug-in compartments, pin B38 accepts the Ch 3 Auxiliary Trigger Out - from the resident plug-in unit.

In the Auxiliary plug-in compartment, pin B38 delivers the trigger outputs from the plug-in unit in the right vertical plug-in compartment.

For specifications and equivalent circuit, see Section 5, Time Match of Display and Trigger Signals.

POWER SUPPLIES

The power limits specified are absolute maximums, which account for component tolerances, variation in the component manufacturing process, and variation due to aging and temperature. The power limits apply to instantaneous values, measured with a time constant of no more than 10 seconds.

All current limits apply to instantaneous values, measured with a 50 MHz current probe. Using a dc meter to average time varying currents is not allowed.

Current limits may be exceeded only while the power supplies are turning on (from an off condition!). The amount of capacitance that a plug-in unit can apply to a power supply output is limited. Mainframes must be designed so that their dV/dt does not cause currents sufficient to damage or cause misbehavior of the power supply. When the power supply voltages have come within their specified tolerances, the plug-in currents must be within their specified maxima.

Every mainframe will supply up to 25 watts power per plug-in compartment.

Plug-in units designed for operation in any compartment are limited to 20 watts internal dissipation.

Plug-in units designed for operation in the Auxiliary compartment only are limited to 24 watts internal dissipation. Such a unit need not be locked out of Left or Right Vertical compartments; but software in the instrument must prevent it from operating in the Left or Right Vertical compartments.

UL testing is done with three load units, each dissipating 24 watts inside the plug-in unit and supplying 1 watt to an external load. (This rule is adopted because it is possible to plug in three "Aux only" type plug-in units, and they will dissipate power. The fact that the software prohibits useful operation does not reduce the temperatures that must be withstood.)

Probe Power

The amount of power by which the supply capability exceeds the allowed dissipation inside the plug-in unit is available for active probes through the "New Probe Interface" connector. It is also available for powering a device under test, as in the case of a curve tracer plug-in unit. Probes using the "New Probe Interface" connector are limited to 1.25 watts per probe; the plug-in unit need not monitor or limit the power transferred.

Les disagrees with this statement; he fears that available current will burn, melt, or otherwise destroy probes. Reasonable concern; what answer?

Plug-in units that provide power through any other port are responsible for limiting power appropriately to comply with the rules.

A three-wide plug-in unit is allowed to dissipate 64 watts internally, and transmit 11 watts to external loads.

A two-wide plug-in unit is allowed to dissipate 40 watts internally, and transmit 10 watts to external loads, if it is allowed to function normally in any compartment. It is allowed to dissipate 44 watts internally and transmit 6 watts to external loads, if it is allowed to function normally in the Right Vertical and Auxiliary compartments only.

The maximum number of "New Probe Interface" connectors which a plug-in unit may provide on its front panel is defined by:

$$N = [\ 25 - (\ \text{Internal Power Dissipation}\ )\ ] \ /\ 1.25$$

Rationale for Current Consumption

The +5, -5, +15, and -15 supplies were designed to power plug-in units and probes.

The "New Probe Interface" is defined as follows:

Maximum power in probe:	1.25 watts.
Maximum current:	
+5	75 mA.
-5	75 mA.
+15	25 mA.
-15	25 mA.

The current limit of 500 mA for the +15 and -15 supplies was chosen to support 7000-Series plug-in units. Every 11000-series plug-in unit must limit its internal consumption to 500 mA minus 25 mA times the number of "New Probe Interface" connectors on the front panel, and minus the maximum current made available through any other port.

The maximum currents for +5 and -5 were chosen to support the design needs of 11000-series plug-in units, and an addition was made for probes. Every 11000-series plug-in unit must limit its internal consumption to Imax minus 75 mA times the number of "New Probe Interface" connectors on the front panel, and minus the maximum current made available through any other port. For +5, Imax is 1.3 A; for -5, Imax is 1.8 A.

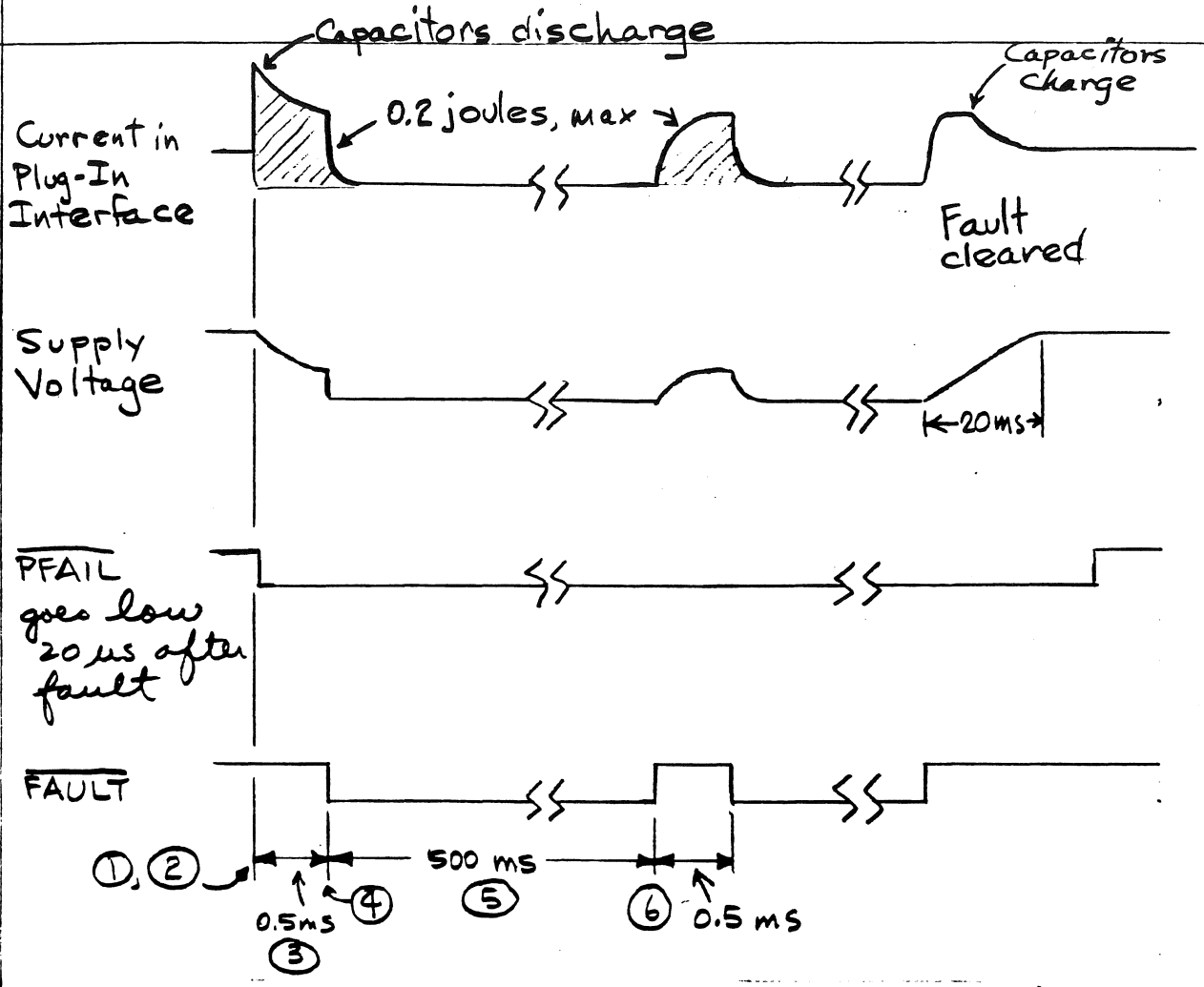


Figure PS-1 Fault definition.

Fault - a persistent condition of excessive current demand.

When a fault occurs, the following sequence of events occurs:

1. **The supply detects the fault within 20 microseconds.**
2. **A low level on the the PFAIL line signals that a fault has been detected, and a diagnostic LED is lit.**
3. **During a 0.5 ms delay, the peak power is limited to <400 W and the energy furnished to the faulty circuit is limited to 0.2 joules until the fault is cleared. The voltage begins to decay during this period.**
4. **If the fault persists, the entire converter will shut off, and the voltage and current outputs will decay to zero. The fault delay latch will set.**
5. **The converter will stay shut off for 500 ms.**
6. **After 500 ms, the converter will try to resume operation, and will deliver 0.2 joules to the faulty circuit. If the fault still exists, the converter will shut down again.**
7. **When the fault is cleared, the converter will be able to deliver 0.2 joules to the circuit without its producing a PFAIL signal. Normal operation then resumes.**

CHARACTERISTIC	SUPPLY VOLTAGE						
	+50	+15	+5.1	+5	-5	-15	-50
Maximum Single-Fault Voltage	+60	+18	+6.0	+7.0	-7.0	-18	-60
MAX CURRENT to Plug-In Unit (Amps)	0.1	0.5	3.0	1.3	1.8	0.5	0.1
MIN CURRENT to Plug-In Unit, in event of fault, after 0.5 ms dly (Amps) (1)	1.0	4.0	5.0	7.0	10.0	4.0	1.0
Max Capacitance, per plug-in unit, uF (2)	100	1000	1000	1000	1000	1000	100
Minimum Impedance @ 1 MHz, milohms (3)	50	100	--	100	100	100	50
Initial Setting Accuracy, +/-% (4)	0.5	0.5	4.9-5.2	0.5	0.5	0.5	0.5
Regulation, with respect to Line Voltage, Max., PPM (5)	5	5	100	5	5	5	5
Output Impedance, max, milohms (6)							
DC	.5	.08	20	.05	.05	.08	.5
1 MHz	500	500	500	500	500	500	500
Temperature Coefficient (max) ppm per degree C (7)	130	130	500	200	200	130	130
Drift, % per year, maximum	.3	.3	1.0	.5	.5	.3	.3
Total Regulation Envelope, % max (8)	2	2	4.8-5.25	2	2	2	2
Ripple, total, mV (9)	5	3	50	1	1	3	5
Transient Response, maximum recovery to within 5 mV, usec (10)	10	5	500	5	5	5	10
Maximum Recovery Time Constant, usec	5	2	200	2	2	2	5

1. Somewhat dependent on main frame. Fault current specified with main frame drawing nominal current. See Figure PS-1, Fault Definition.

2. Greater capacitance will cause a current limit during "hot switch."

3. Measured at terminals of Interface Board. Less impedance may cause instability in the regulator.

4. Measured at Interface Board sense points with:
   a. regulator connected to main frame,
   b. ambient temperature +20 to +30 degrees C, and
   c. 10.0 V Ref set within +/-25 mV.

5. Applies for line voltages between 90 V and 130 Vrms or 180 to 250 Vrms.

6. Measured at sense points on Interface Board, with load current anywhere from zero to rated maximum.

7. Ambient temperature from zero to +50 degrees C.

8. Includes line, load, temperature, and time variations. Measured at sense points on Interface Board.

9. Measured at sense points on Interface Board, with supplies furnishing 80% of their rated dc load current, with 500 kHz bandwidth with respect to Reference common.

10. Response to 35 mA step change in load; measured at Interface Board sense points, with 20 MHz bandwidth. (?)

CAMERA POWER

From Top Pin Crt Bezel Connector
(+15 V Regulated Supply)

	Power Light Off	Power Light On
Standby	30 μA or less at +20°C to +30°C	60 mA or less at +20°C to +30°C
Shutter Operation	90 mA peak*	130 mA peak*
Focus Operation	550 mA peak*; 190 mA steady state	600 mA peak*; 250 mA steady state

*Will vary with Main Frame.

SERIAL DATA INTERFACE (Jim Peterson)

The serial data interface (SDI) system is a means of transferring information serially, at a high bit rate, from the main frame to plug-in unit(s) or from plug-in unit(s) to the main frame. This allows a processor in the main frame to communicate with a processor in the plug-in unit.

The SDI consists of nine lines. Each plug-in unit has a clock line (supplied by the main frame), a dedicated data signal from the plug-in unit to the main frame, and a dedicated data signal from the main frame to the plug-in unit. The names of the lines are:

A_SDI_CLK - Clock to the Aux plug-in unit
A_TO_MFSDI - Data from the Aux plug-in to the main frame
MF_TO_ASDI - Data from the main frame to the Aux plug-in unit
L_SDI_CLK - Clock to the Left plug-in unit
L_TO_MFSDI - Data from the Left plug-in unit to the main frame
MF_TO_LSDI - Data from the main frame to the Left plug-in unit
R_SDI_CLK - Clock to the Right plug-in unit
R_TO_MFSDI - Data from the Right plug-in unit to the main frame
MF_TO_RSDI - Data from the main frame to the Right plug-in unit

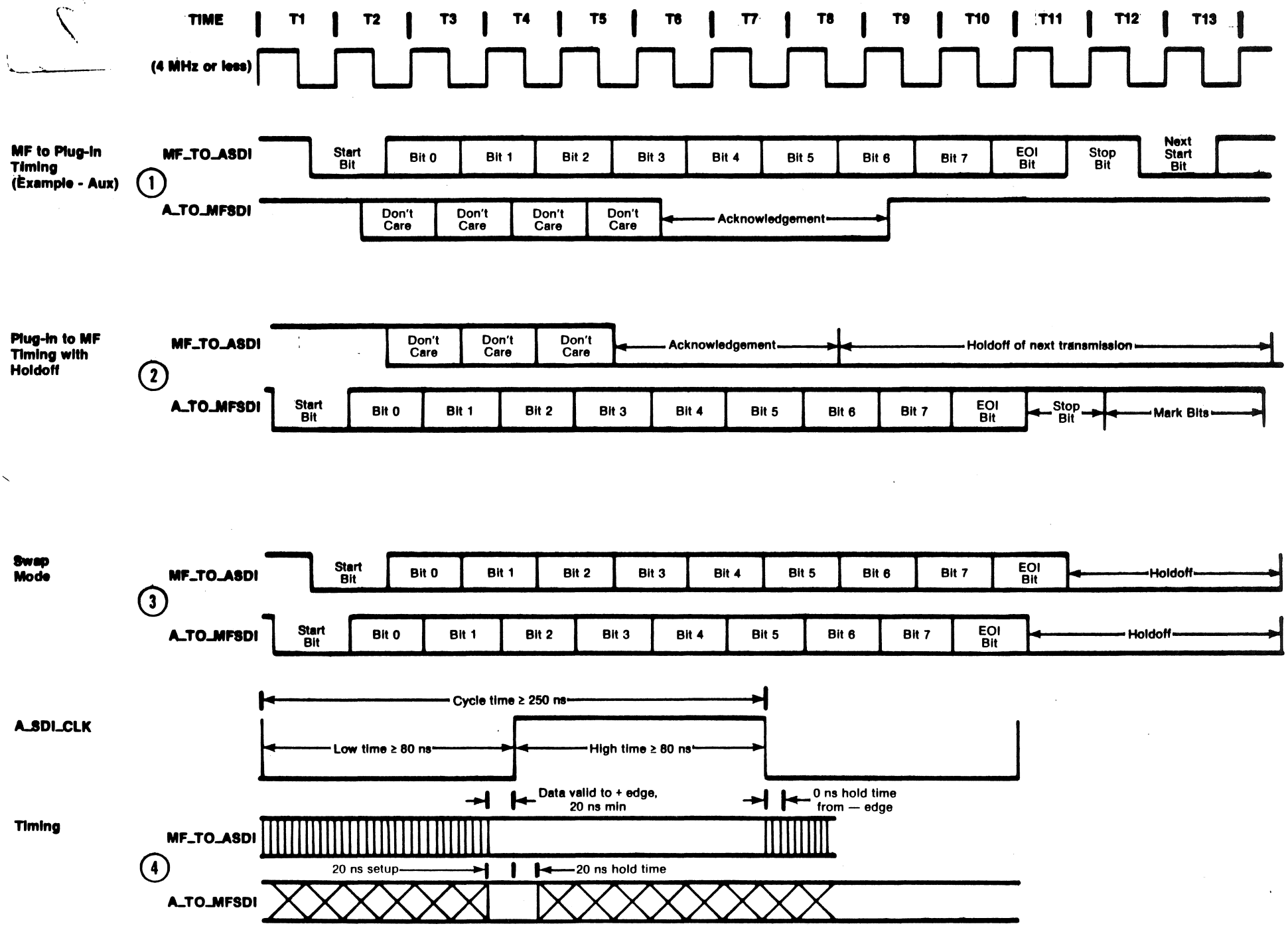
Any clock or data line can be shorted to ground without damaging the SDI hardware, although the SDI communication for that plug-in unit will not function. Data is clocked into both the main frame and plug-in units on the positive edge of the SDI clock. Data is clocked from the plug-in unit(s) on the positive edge of the clock, and from the main frame on the negative edge of the clock. Both the mainframe and the plug-in unit must have both a receiver and a transmitter to allow communication in either direction.

1. A simple example (refer to Figure SDI-1)

Only the signals for the Aux plug-in unit are shown; the signals for all the plug-in channels are identical.

1.1 Description of bits transmitted

When a SDI channel is not in use, the data signals are in the high (mark) state. To start a transmission (in this case, for the main frame to transmit a byte to the plug-in unit), a start bit (a low level) is sent first. The start bit causes a high-to-low transition on the data line. After the start bit is sent, eight data bits (LSB first) are transmitted, then an EOI bit is sent. If the EOI (End or Identify) bit is high, it also serves as a stop bit, and no stop bit needs to be transmitted. If the EOI bit is low, a stop bit will be transmitted after the EOI bit. This means that, to transmit one byte using the SDI system, either 10 (EOI bit high) or 11 (EOI bit low) clocks are required. With a 4 MHz clock a byte rate of 400 kbytes/sec may be achieved.


TIME
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
(4 MHz or less)
MF to Plug-in Timing (Example - Aux)
1
MF_TO_ASDI
Start Bit
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7
EOI Bit
Stop Bit
Next Start Bit
A_TO_MFSDI
Don't Care
Don't Care
Don't Care
Don't Care
Acknowledgement
Plug-in to MF Timing with Holdoff
2
MF_TO_ASDI
Don't Care
Don't Care
Don't Care
Acknowledgement
Holdoff of next transmission
A_TO_MFSDI
Start Bit
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7
EOI Bit
Stop Bit
Mark Bits
Swap Mode
3
MF_TO_ASDI
Start Bit
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7
EOI Bit
Holdoff
A_TO_MFSDI
Start Bit
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7
EOI Bit
Holdoff
A_SDI_CLK
Cycle time ≥ 250 ns
Low time ≥ 80 ns
High time ≥ 80 ns
Timing
Data valid to + edge, 20 ns min
0 ns hold time from — edge
4
MF_TO_ASDI
20 ns setup
20 ns hold time
A_TO_MFSDI

1.2 Acknowledgement

When the plug-in SDI senses a start bit, it needs to acknowledge that it is receiving the transmission. The SDI acknowledges reception by setting the data signal from the plug-in unit to the main frame low for three clocks after it receives bit 3. This notifies the mainframe that a real plug-in unit is installed; in other words, the slot is not empty. The acknowledgement is given with the same signal used to transmit data from the plug-in unit to the main frame. This means that, under normal circumstances (see Figure SDI-3 for the exception), the main frame and the plug-in unit cannot transmit data to each other at the same time.

The acknowledgement does not start until four clocks after the start bit. That is how the first SDI IC worked, and it set a precedent. The transmitting SDI must not mistake the acknowledgement as a stop-start bit combination.

1.3 Achieving maximum byte rate

In order to allow the maximum possible byte rate over the SDI, the data line to the main frame must go high again after bit 6 is received. This notifies the main frame that the plug-in unit is ready to receive another byte immediately after the one currently being transmitted. This requires first-in, first-out (FIFO) buffering of the received data because there are only two clock cycles to get the received data byte out of the receiver shift register. Without FIFO buffering in the receiver a method of holding off the next transmission is needed. This is explained in the next section.

2. SDI transfer with holdoff (Figure SDI-2)

This section concerns a transmission when the transmitted bytes are not transmitted back-to-back. Figure SDI-2 shows the details of an SDI transfer with holdoff.

One of the design goals for the SDI system was to allow fast and slow devices to be able to communicate. For example, suppose a plug-in unit could process a byte only once per second, but the main frame wanted to transmit to the plug-in unit at 1000 bytes/second. If the main frame sent the bytes at the faster rate, the plug-in unit would miss most of them.

To adapt the SDI system to this situation, we added a holdoff feature. As shown in Figure SDI-2, the plug-in unit is transmitting to the main frame. The timing is the same for transmission in either direction. The main frame can prevent the plug-in unit from sending another byte by leaving the data signal to the plug-in unit low after acknowledging the transmission from the plug-in unit. The data signal from the main frame will return high after the main frame reads the byte it receives, and this will allow the plug-in unit to send another byte, or permit the main frame to send a byte to the plug-in unit. A new transmission may start one clock after the holdoff period ends.

3. The swap mode

Another design goal of the SDI was to allow the main frame or the plug-in unit to start a transmission whenever the SDI system was idle. An idle state exists when no transmission or holdoff is occurring, and both data lines are in the high, or mark state. It is possible for both the main frame and plug-in unit to start transmitting simultaneously; that is, when the start bits are sent so that they are received on the same clock edge. This is called the "swap" mode.

In the swap mode, data is sent from the main frame to the plug-in unit at exactly the same time data is being sent from the plug-in unit to the main frame. In the swap mode, after the data and EOI bits have been sent, both data lines need to go into the holdoff mode for at least one clock cycle. This ensures that if the EOI bit is high, the EOI-to-holdoff transition will not be interpreted as a stop-to-start bit transition. In swap mode no acknowledge is sent because the data lines are busy transmitting data.

4. Timing specifications

4.1 SDI clock

The SDI clock (A_SDI_CLK, R_SDI_CLK, and L_SDI_CLK) signals should be 4 MHz or less. The slow speed allows for slow rise and fall times on the clock and data lines, which reduces noise generation. The clock should be close to symmetrical, with rise and fall times of about 20 to 40 nS. The SDI clock levels are TTL thresholds. If reduced bit rates are acceptable, slower clocks than 4MHz may be used. The main frame generates the clock.

4.2 MF to plug-in data

The main frame generates MF to plug-in data signals (MF_TO_ASDI, MF_TO_RSDI, MF_TO_LSDI) from the negative transition of the SDI clock. These signals are clocked into the plug-in receivers on the positive edge of the SDI clock. These signals must be valid (below a TTL low or above a TTL high) 20 nS before the positive transition of the SDI clock signal passes through the TTL low threshold. The hold time from the positive clock edge is also

20 nS, but because the data is clocked on the negative transition this is not a problem. If these signals were clocked out on the negative rather than positive clock transition, there would be a problem meeting the hold time specification of the data with respect to the clock.

4.3 Plug-in to MF data

The plug-in to main frame data signals (A_TO_MFSDI, R_TO_MFSDI, L_TO_MFSDI) are generated in the plug-in units. They are clocked out on the positive transition of the SDI clock in the plug-in unit, and received on the next positive transition of the SDI clock in the main frame. The setup and hold times are 20 nS with respect to the positive transition of the SDI clock. This data can be clocked out on the positive SDI clock transition because the SDI clock is generated in the main frame, and is guaranteed to get to the SDI chip in the main frame before it gets to the plug-in units.

14 Jan 1985
11000-SERIES CHANNEL-SWITCHING LOGIC (Tim Bennington)

The channel switching in the 11000-Series instrument line is performed by programmable sequencers residing in the main frame and in each plug-in unit. The main frame has the responsibility of interpreting information from the human interface and informing the plug-in units what to display, and the number of steps in the current sequence, during any given step of a sequence. The main frame supplies two communication lines, Sequence Clock (A5) and Sequence Sync (B6), to synchronize the plug-in units to the main frame.

The programmable sequencers in the main frame and plug-in unit must be capable of sequences of twelve steps; each step must be independent of all other steps. At any step, any possible channel or combination of channels must be available to direct to the crt or digitizing device.

The number of steps per sequence programmed into any plug-in unit must be equal to the number of steps per sequence in the mainframe. The steps must be displayed in order with a one-to-one correspondence with the main frame's sequence. A plug-in unit must account for a step in the sequence even though that plug-in unit is not furnishing the signal to the main frame for display or digitizing.

Plug-in units and main frames must advance to the next step in the sequence on the positive transition of every Sequence Clock when the Sequence Sync signal is low.

Plug-in units and main frames must reset to the first step in the sequence on the positive transition edge of Sequence Clock when the Sequence Sync signal is high.

Upon receiving a software reset command from the main frame, a plug-in unit will reset its programmable sequencer to the first step in the sequence. The main frame and plug-in unit(s) will always begin a display or digitizing cycle on the first step of the sequence.

Single-Sequence Mode

In single-sequence mode, the main frame has the responsibility of commanding the plug-in units to reset themselves to the first step in the sequence.

The main frame has the responsibility to initiate and to terminate the Single-Sequence Mode. The plug-in units have no special requirements to fulfill in this mode.

Synchronizing the Z-Axis Control

The main frame has the responsibility of generating one version of the Main Frame Channel Switching Signal (B7) for the two Vertical plug-in compartments and a second version for the Auxiliary plug-in compartment. The two signals are used in conjunction with Main Frame Mode Info (A16) to notify a plug-in unit that it may control the Z-Axis Amplifier via the Aux Z-Axis line (A17). The following rules must be followed:

1. When the exclusive-OR of signals A16 and B7 at any plug-in unit is true, that unit may modulate the Z-Axis intensity by applying a signal to A17.

2. When the exclusive-OR of signals A16 and B7 at any plug-in unit is false, that unit must not affect the signal present on A17.

3. When used in the Auxiliary plug-in compartment, plug-in units that generate a Sweep Gate (A1) may modulate A17 only when their Sweep Gate is high and the exclusive-OR of signals A16 and B7 is true.

4. Whenever channels of a plug-in unit in the Left compartment are added to channels of a plug-in unit in the Right compartment, the main frame need set the A16 and B7 signals true for only one of the those compartments.

5. Whenever a two-wide plug-in unit is installed, the compartment that houses the horizontal section of the two-wide unit should be the compartment used to supply the proper A16 and B7 signals.

TIME MATCH OF DISPLAY AND TRIGGER SIGNALS (Dave Dobak)
Skew Specification

The objective of the Auxiliary Trigger signals is to support a Triggering plug-in unit in the Auxiliary compartment. The Triggering unit discriminate the time relationship of signals as they appear at the input connectors of the Amplifiers.

Therefore, there needs to be a specification so that a plug-in unit operating in the Auxiliary Compartment, which uses Auxiliary Triggers, can make the signals time coincident.

This description defines the system configuration and requirements.

1. Amplifier Units

An Amplifier, by definition, includes channel-switched Display and Trigger outputs, and a continuously available Auxiliary Trigger output for each channel.

1.1 Display and Trigger Outputs

The Display (A11 - B11) and Trigger (A13 - B13) outputs will have the same electrical length from input to output. The overall propagation time is specified.

1.2 Auxiliary Trigger Outputs

The Auxiliary Trigger outputs (show pins numbers) must match each other (but they might not match the Display and Trigger outputs). The overall propagation time is specified.

2. MAIN FRAME

2.1 Display and Trigger Inputs

The display signal paths from each plug-in unit to each sampler, or to the display channel switch are matched. The trigger signal paths from each plug-in unit to the trigger channel switch are matched.

2.2 Auxiliary Trigger from Left and Right to Aux

All eight Auxiliary Trigger signal paths from Left and Right Vertical compartments to the Auxiliary compartment must be the same length. The overall delay is not specified.

This is done so that the overall delay can vary if necessary (for example, due to variation in ECB dielectric coefficient) but the propagation time will always be matched.

3. Auxiliary Trigger Plug-In Unit

An Auxiliary Trigger Plug-In unit is defined as a unit which operates only in the Auxiliary compartment, and uses the Auxiliary Trigger signals provided from amplifiers in the Left and Right Vertical compartments. Front panel inputs are optional.

3.1 Display and Trigger Outputs

No special rules apply to these outputs. Like amplifier outputs, they should be matched, but there is no overall specification unless the plug-in unit has bnc inputs with high bandwidth response as well as trigger-generation facilities.

3.2 Auxiliary Trigger Inputs

The Auxiliary Trigger Plug-In unit assumes that the signals it receives at the interface connector are matched in time as well as the signals at the Display outputs of the Amplifiers.

4. SPECIFICATIONS

4.1 Amplifier

The propagation delay for Amplifier plug-in units, from bnc input to each output is:

Display	Display Nominal ± 50 ps.
Trigger	Display Nominal ± 50 ps.
Aux Trig Ch 1	Aux Trig Nominal ± 50 ps.
Aux Trig Ch 2	Aux Trig Nominal ± 50 ps.
Aux Trig Ch 3	Aux Trig Nominal ± 50 ps.
Aux Trig Ch 4	Aux Trig Nominal ± 50 ps.

Note that these numbers are absolute. We do not use the concept of a loose tolerance nominal and a tight tolerance difference. This is because good match must occur between the channels of two plug-in units; there is no adaptive deskewing in the Auxiliary Trigger unit, so the amplifier design must provide for a close tolerance over all production.

4.2 Mainframe

The propagation delay across the Mainframe Interface Board from Left or Right Vertical compartment to Auxiliary compartment is:

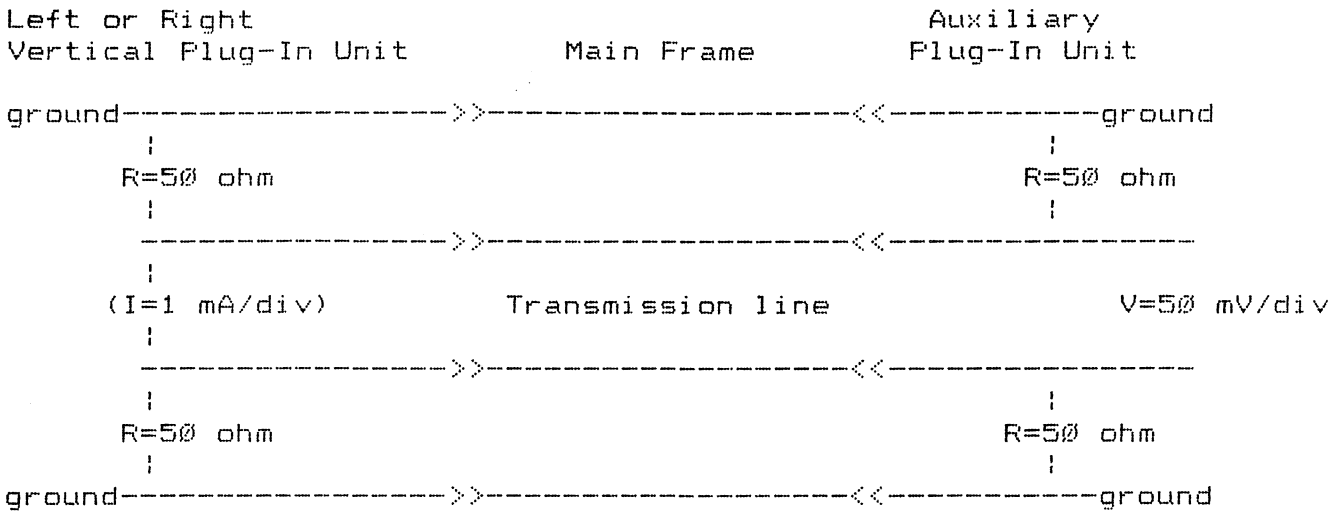
All channels match within ± 10 ps.

4.3 The Auxiliary Trigger Plug-In Unit

All channels match within ± 4Ø ps.

A tolerance of ± 4Ø ps is allowed for the Auxiliary Trigger Plug-In unit to achieve a system specification of ± 1ØØ ps.

Auxiliary Trigger equivalent circuit.



Main frame requirements:
Transmission line 1ØØ ohms side-to-side.

Maximum output of plug-in amplifiers: +/-15 divisions differential, 5Ø mV common mode component.

Specs apply over +/-6 divisions.

DC Centering: within Ø.2 divisions, referred to pins A11 and B11.

TDR of transmission lines,
measured with push-pull 5Ø ohm TDR:

Risetime:	tbd.
Aberrations:	tbd.
Reflections:	tbd.

Back termination is required in Amplifiers.

Current drive is shown in illustration. Voltage source behind 5Ø ohms is also acceptable.

The Amplifier is responsible for not being disturbed when the Auxiliary Compartment is empty and the transmission line terminations are absent.

When Amplifiers are installed in all three compartments, the Auxiliary Trigger Outputs from the Amplifiers in the Left and Right Vertical and Auxiliary Compartments drive each other. Amplifier plug-in units are responsible for not being disturbed when this condition exists.

Amplifier: This output follows Bandwidth Limit and Volts/Div (Coarse and Fine) and Offset of Display Channel. This output is never inverted; always +Up.

COMPATIBILITY OF 7000-SERIES WITH 11000-SERIES MAIN FRAMES

No 7000-series plug-in unit will suffer damage from being installed in an 11000-series main frame.

No 7000-series plug-in unit will produce a readout on an 11000-series main frame.

No 7000-series plug-in unit can be controlled through the 11000-series main frame's human interface.

7A-Series Amplifiers

The following plug-in units are fully compatible with 11000-series main frames, except that:

* No Tek readout will be displayed.
* Dual-channel units will operate in single-trace mode only (Ch 1, Ch 2, Add). Chop and Alt will not function. The Trigger and Display outputs will be available.
* Auxiliary Trigger signals are not provided to a plug-in unit in the Aux compartment.

7A11
7A12 (discontinued)
7A13
7A14 (discontinued)
7A15, 7A15A
7A16, 7A16A
7A17
7A18, 7A18A
7A19
7A22
7A24
7A26
7A29

The 7A16P will probably work, but we strongly discourage using it.

The 7A21N direct access unit is incompatible because the 11000 main frames have no provision for direct access.

The 7A42 Logic Triggered Vertical Amplifier is compatible, but functionally useless for display because 11000-series main frames do not enable the channel-switching function. The 7A42 could serve as a triggering source.

7B-Series Time Bases

7B-Series Time Bases can be used in any 11000-series compartment to provide a displayed ramp. They have the following limitations:

* No Tek readout is displayed.
* The 11000-series main frames provide no internal trigger signals.
* The sweep control signals (holdoff, lockout, and delay gate) are not supported in any 11000-series compartment, therefore there will be no interaction with the time bases in the 11000 main frame.

  When installed in the Aux compartment, 7B-Series Time Bases behave like amplifiers with built-in function generators, and with a sweep gate available; they can drive the z-axis amplifier.

These 7B-Series Time Bases are compatible with 11000-series main frames:

7B10	7B70
7B15	7B71
7B50, 7B50A	7B80
7B51	7B85
7B52	7B87
7B53, 7B53A	7B92, 7B92A *

* In the 7B92 and 92A, the Single Sweep Ready indicator on the front panel will always be on, because the 11000-series interface connector pin applies +5.1 V to pin A10.

  The1 7B90P will probably work like any other time base, but we strongly advise against using it.

7CT1N Curve Tracer

This unit is fully compatible. No Tek readout will be displayed because the 7CT1N generates none.

7D** Digital Units

The following units are functionally useless in all 11000-series main frames because the 11000-series main frames will not display their Tek readout.

7D10
7D11
7D12-M1
7D13
7D14
7D15

The 7D12-M2 is compatible, but no Tek readout will be displayed.

The 7D12-M3 is compatible, but no Tek readout will be displayed. This puts its rms-calculating beyond reach. This limits its usefulness to the ability to display a waveform derived from its nonground-referenced input.

The following plug-in units are functionally useless in ET 11ØØØ-series main frames, which are unable to unscramble waveforms and readout to produce an XY display. They are all compatible with real time 11k main frames, but no Tek readout will be displayed.

7DØ1
7DØ1DF1
7DØ1DF2
7DØ2
7D2Ø

In the 7D2Ø several GPIB lines will be connected to ground when it is plugged into an 11ØØØ-series main frame. No destruction will occur, but the bus will not work. Thus, to operate the 7D2Ø via the GPIB requires that its internal cable (P12Ø) be removed. Then GPIB hardware can be connected to the 7D2Ø only via its front-panel connector; there is never programmability through the main frame.

7S** and 7D** Sampling Units

All sampling equipment is fully compatible, except that:

1. Tek readout is not displayed, and

2. Old 7T11s, before SN B16Ø92Ø, March 5, 1973, have +5 V on pin A36. This means that installing a 7T11 adjacent to a 11A** or 11T** could damage the 11ØØØ-series unit (if installed simultaneously).

3. The 7S14 will work in dual-trace mode because its channel-switching is internally generated, and z-axis control is available.

4. Because a sweep gate is needed to unblank the display or qualify sampling, the sampling sweep must be installed in the Auxiliary plug-in compartment.

7M** Utility Units

The 7M11 Delay Line unit is fully compatible.

The 7M13 Readout Generator is useless because 11ØØØ-series main frames do not display Tek readout.

7K11 CATV Amplifier

The 7K11 is fully compatible, except for the lack of Tek readout.

7L** Spectrum Analyzers

The 7L5 is functionally useless because 11000-series main frames will not display Tek readout.

The 7L12 and 13 are compatible with all 11000-series main frames except for lack of Tek readout. Also, the Single Sweep Ready indicator on the front panel will always be on because the 11000-series Interface applies +5.1 V to pin A10.

The 7L14 and 7L18 are compatible with real time 11000-series main frames, except that no Tek readout will be displayed. They are functionally useless in ET 11000-series main frames because they cannot unscramble digital display waveforms to produce an XY display.

Because the Sweep Gate is needed to blank the display, the 7L-series spectrum analyzers should be installed in the Auxiliary plug-in compartment.

7J20 Spectrometer

The 7J20 is hereby declared to be incompatible, because no information is available about it. It was introduced in 1974 and promptly discontinued. (A resounding success; instant acclaim!)

Calibration Fixtures

The 067-0587-01 and-02 are fully compatible.

The Normalized Ramp Generator is not useful for 11000-series and has not been investigated.