REV	REF	DESCRIPTION OF CHANGE	CHK BY	DATE
OR		Initial Documentation as per ECN # 4102. All 13 pages changed.		Perkins 6-27-79

Linda Haney
Writer

David W. Perkins
Originator

REV OR

PART NUMBER 155-0217-00

Tektronix, Inc. M055D 155-0217-00

THE DRAWING TYPE DESIGNATION AND APPROVED SOURCES OF SUPPLY FOR THIS ITEM ARE LISTED ON THE PURCHASED ITEM SOURCE LIST (PISL) FOR THIS PART NUMBER.

TEKTRONIX, INC.
P. O. BOX 500
BEAVERTON, OREGON U.S.A. 97077

DWN/ WR	
COMP ENGR	
CHKR/ COORD	
INSTR DSGN	

DIMENSIONS ARE IN INCHES / MM
TOLERANCES: UNLESS OTHERWISE SPECIFIED

DEC	ANLR

SCALE	FIRST USED ON

MATERIAL

FINISH

TITLE

TRANSCONDUCTANCE AMPLIFIER WITH GAIN CONTROL; M055D

	SH 1 OF 13	CODE IDENT NO	SIZE	PART NUMBER	REV
		80009	A	155-0217-00	OR

1.0 PRODUCT PRECAUTIONS

Not applicable to this part.

2.0 DESCRIPTION

This component is a silicon, monolithic integrated circuit, which is fabricated using the 50/450 process. It is a transconductance amplifier with gain control, and provision is made for offset and positioning control. The component is packaged in a 16 pin dual-in-line package.

3.0 ABSOLUTE MAXIMUM RATINGS

3.1 Environmental

Storage Temperature (T_{stg}). . . . . -55 to +125°C

Operating Ambient Temperature Range (T_a). . . . 0 to 70°C

3.2 Electrical

Emitter-Base Breakdown Voltage (BV_{EBO}). . . . . 5.8 Volts

Collector-Emitter Voltage (V_{CE}) . . . . . 15 Volts

Positive Voltage on Pins 8, 9. and 11
W.R.I. Pin 5 (BV_{CS}) . . . . . 30 Volts

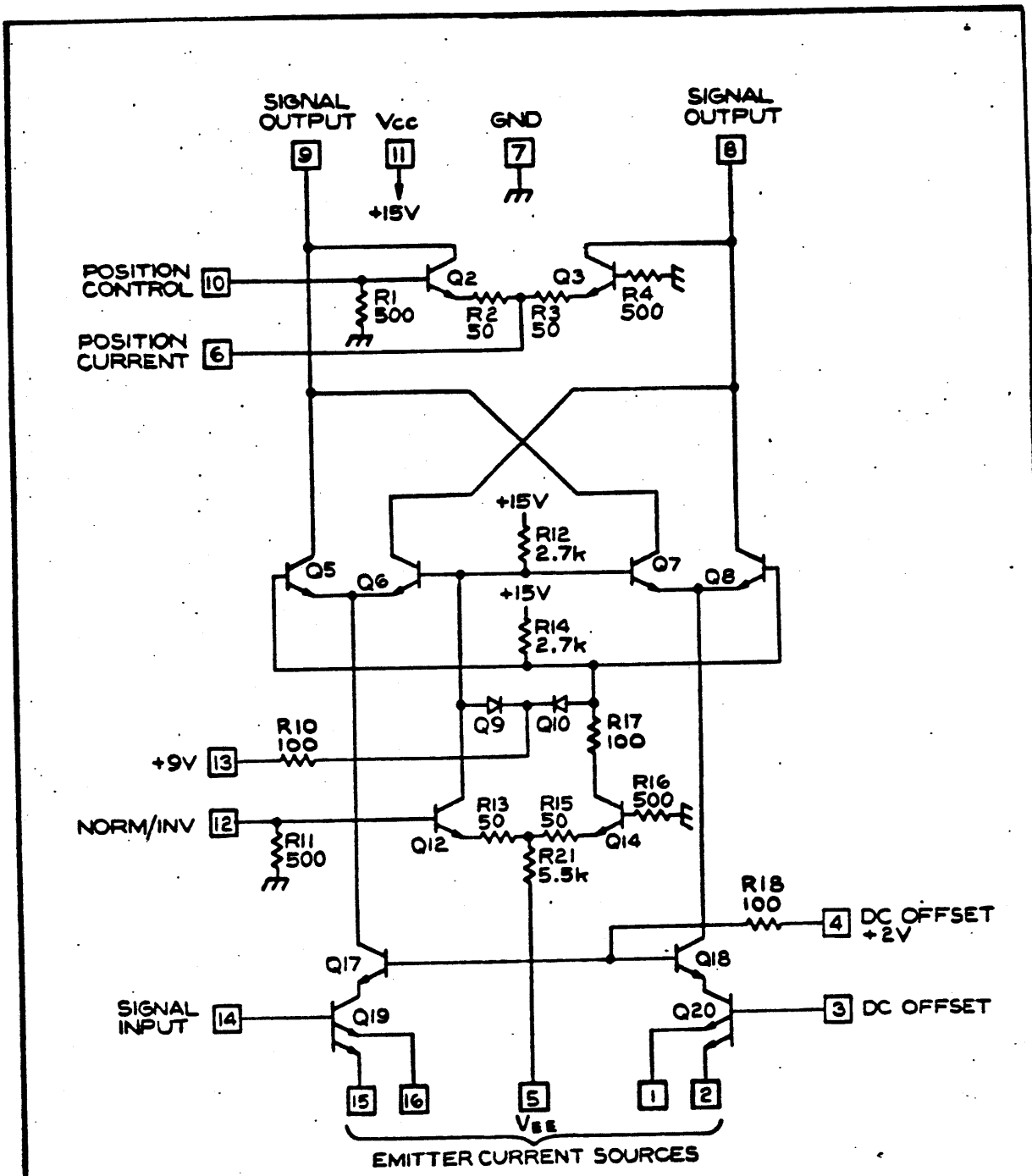
Pin 13 Voltage W.R.T. Pin 7 . . . . . 10 Volts

Voltage on Pins 10 & 12 W.R.T. Pin 7. . . . . 5 Volts

Total Current from Pin 8 or Pin 9 (I_{total}). . . 20 mA

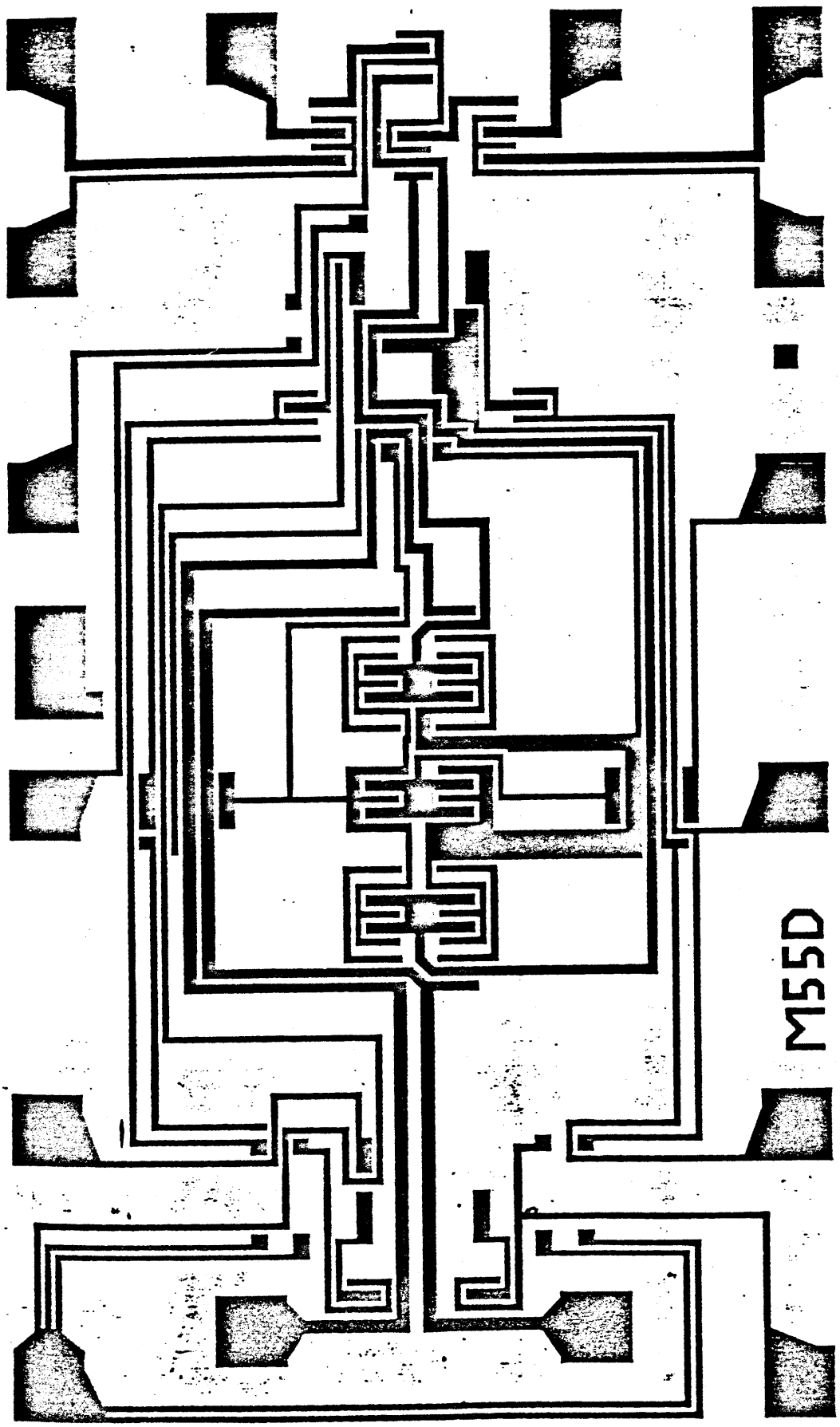
Total Device Power Dissipation (P_D) . . . . . 300 mW

4.0 SCHEMATIC DIAGRAM



ENGR	Evan Trail	7-1-76	PROCESS	50-450
DWN BY	J. Langley	6-29-76	PACKAGE	16 PIN DIP
CHK BY	Linda Boyer	7-13-76	DIE SIZE	60 mil X 40 mil
TYPE	MONOLITHIC	INPUT AMPLIFIER		MOSFET
INTEGRATED CIRCUIT ENG/MFG TEKTRONIX, INC. BEAVERTON, OREGON, U.S.A.		PART NO. 155-0217-00		

4.1 Layout Drawing



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000-7243-00D

DO NOT SCALE DRAWING

5.0 PARAMETRIC DEFINITIONS

5.1 Input Emitter Bulk Resistance

The bulk resistance seen from any input emitter contact to the emitter side of the emitter-base space charge level.

5.2 Input Offset Voltage

The voltage at the input required to set the differential output voltage to zero.

5.3 Input Offset Current

The input current required to set the differential output voltage to zero.

5.4 Common-Base Forward Current Gain

The sum of the output current divided by the sum of the input emitter current.

5.5 Risetime

The output response time (10% to 90%) of the component, when the input is subjected to an ideal step function.

5.6 Output-Current Differential at any Gain Setting

The output current differential measured with the inputs of the component such that a balanced condition exists. This parameter is commonly called "NULL SUPPRESSION".

5.7 Gain Control Current for Maximum Normal Gain

The current into the gain control node required to achieve maximum normal gain.

5.8 Gain Control Current for Maximum Inverted Gain

The current into the gain control node required to achieve maximum inverted gain.

5.0 PARAMETRIC DEFINITIONS (continued)

5.9 Zero Gain - Gain Control Current

The current into the gain control node when the potential at the node is zero volts.

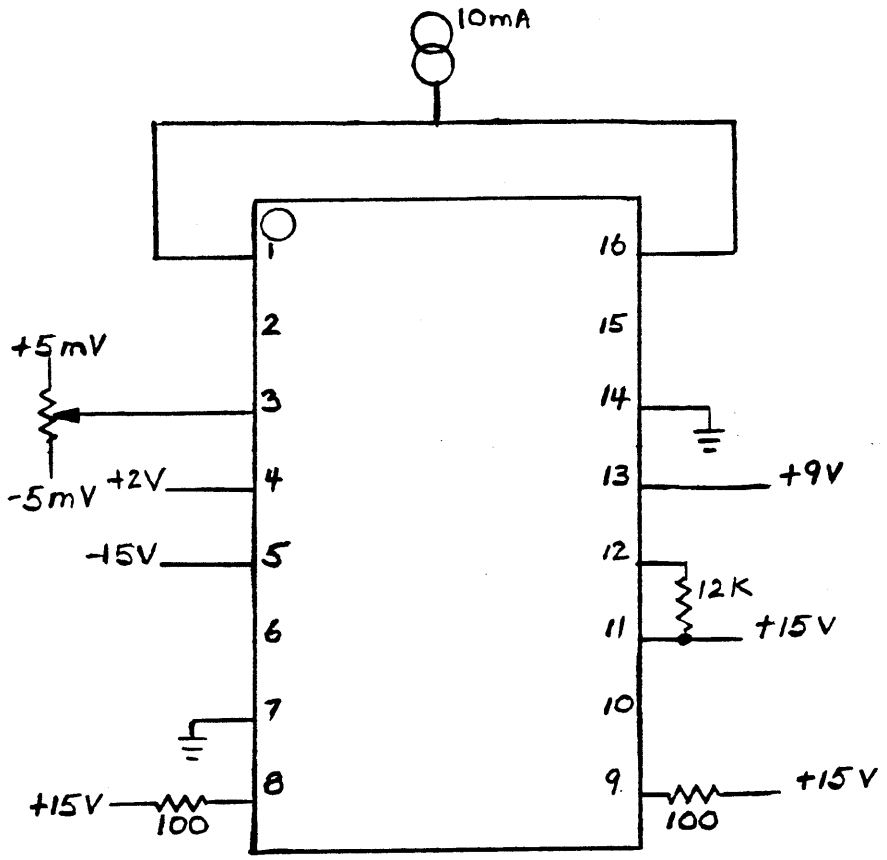
5.10 Position-Control Voltage for Zero Differential-Positioning Current

The voltage at the position control node, required to cause the outptu differential positioning current to go to zero.

6.0 PARAMETRIC SUMMARY

PARAMETER NAME AND CONDITIONS OF MEASUREMENT	PARAMETER SYMBOL	MINIMUM VALUE	MAXIMUM VALUE	UNIT OF MEAS.	PIN MEAS.
Emitter Bulk Resistance (typ. 3.5 ohm)	R_E			Ohms	1,2,15,16
Input Offset Voltage (see 6.1)	V_{IOS}		$\pm$5.0	mV	3
Input Offset Current (see 6.1)	I_{IOS}		50	µA	3,14
Common-Base Forward Current Gain	h_{fb}	0.95			8 & 9 Gnd. 1,16 or 2,15
Risetime (Typical 800 ps)	t_r			ps	
Output Current Differential (Null Supp.)	$I_{O.D.}$		$\pm$33.0	µA	8,9
Gain Control Current (Max. Norm.)	$I_{G.C.NORM}$	200	350	µA	12
Gain Control Current (Max. Inv.)	$I_{G.C.INV.}$	-350	-200	µA	12
Gain Control Current (Zero Gain)	$I_{Z.G.}$		$\pm$ 48	µA	12
Position Control Voltage	$V_{A.C.}$		$\pm$ 50	mV	10

6.1 Parametric Measurement Scheme



NOTES:

Input Offset Voltage

Set differential output voltage (Pins 8 & 9) to zero, measure Pin 3 voltage.

Input Offset Current

Insert current measuring devices in leads of Pins 3 & 14. Set differential output voltage to zero, measure ABSOLUTE current difference between Pin 3 and Pin 14.

Output Current Differential

Apply input offset voltage to Pin 3. Then measure output current differential at any gain setting (Pin 12).

Position Control Voltage

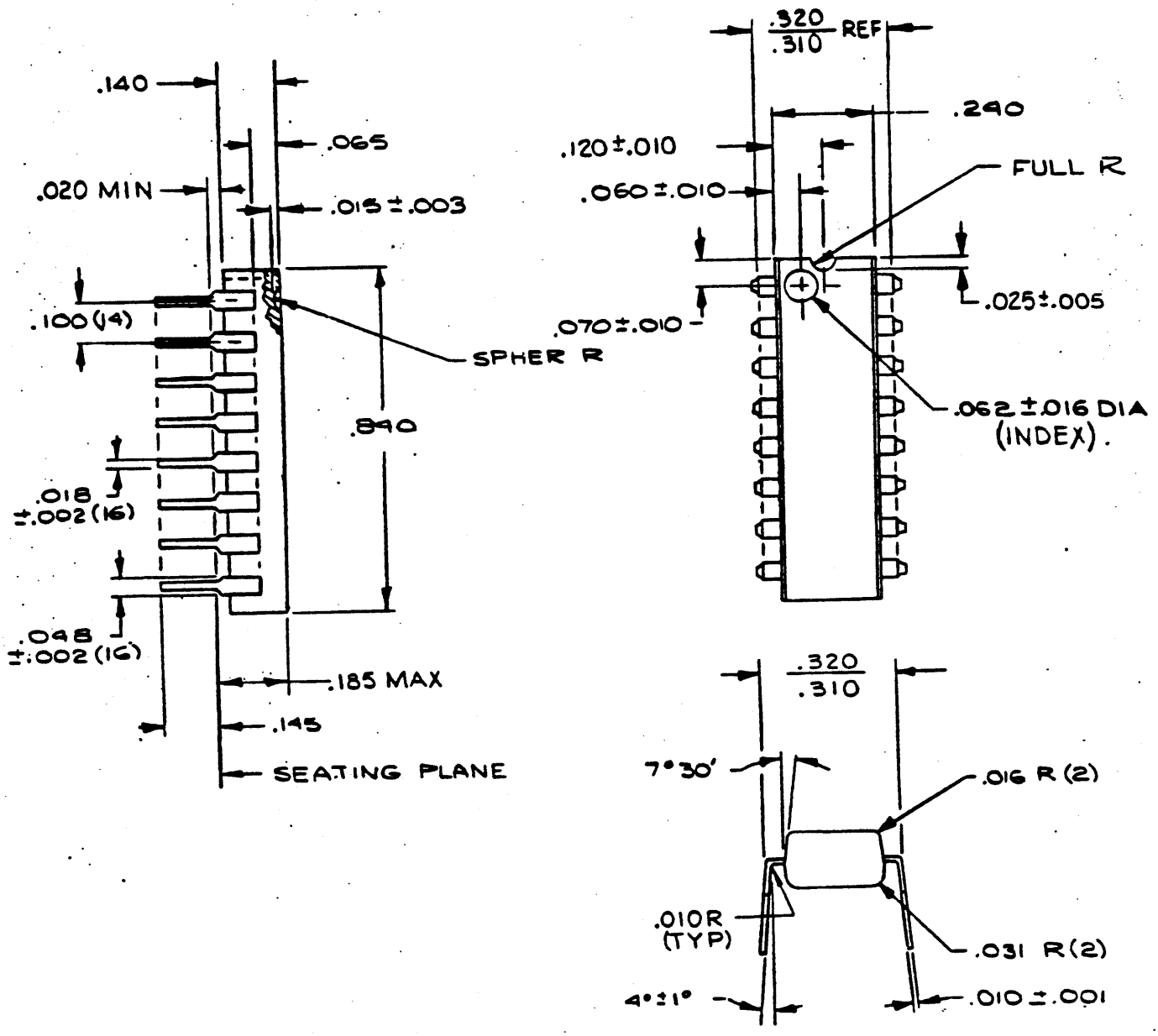
Source Pin 6 with 2 mA. Set voltage at Pin 10 such that differential output current is zero. Measure voltage at Pin 10.

7.0 PACKAGING

7.1 Terminal Identification

Pin Number	Name	Description
1	Input Emitter 1b	Sourcing Emitter
2	Input Emitter 2b	Sourcing Emitter
3	Input Base	Offset Control
4	Input Collector Voltage Return	Input Stage Bias
5	Substrate Node	Most Negative Supply
6	Positioning-Current Input	
7	Ground	
8	Signal Output	
9	Signal Output	Differential
10	Position Control Node	
11	Epitaxial Layer	Most Positive Supply
12	Normal/Invert Gain Control Node	
13	Multiplier Linearity Control - 9 Volt Bias	
14	Input Base	Signal Input
15	Input Emitter 2a	Sourcing Emitter
16	Input Emitter 1a	Sourcing Emitter

7.2 Outline Drawing



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7.3 Thermal Characteristics

Thermal Impedance

Junction to Case (θ_{jc}) . . . . . $50^{o}C/W$

Junction to Ambient (θ_{ja}). . . . . $99^{o}C/W$

8.0 RELIABILITY STATEMENT

8.1 Reliability Goal

λ, Failure Rate $\leq$ .16%/1K hours at 98^{o}C Tj.

λ, Failure Rate $\leq$ .02%/1K hours at 75^{o}C Tj.

MTTF $\geq$ 5 X 10^{6} hours at 75^{o}C Tj.

Expected Instrument Life: 10K Hours.

8.2 Life Test Results*

90% Confidence Level.

λ, $\leq$ .02%/1K hours at 98^{o}C Tj.

λ, $\leq$ .00002%/1K hours at 75^{o}C Tj.

Life Test Report #Rel-01 Date June 18, 1979

*These results are included for information about the component's capability at a particular time. Refer to manufacturing data for current failure rate data.

9.0 APPLICATIONS INFORMATION

Not applicable to this part.