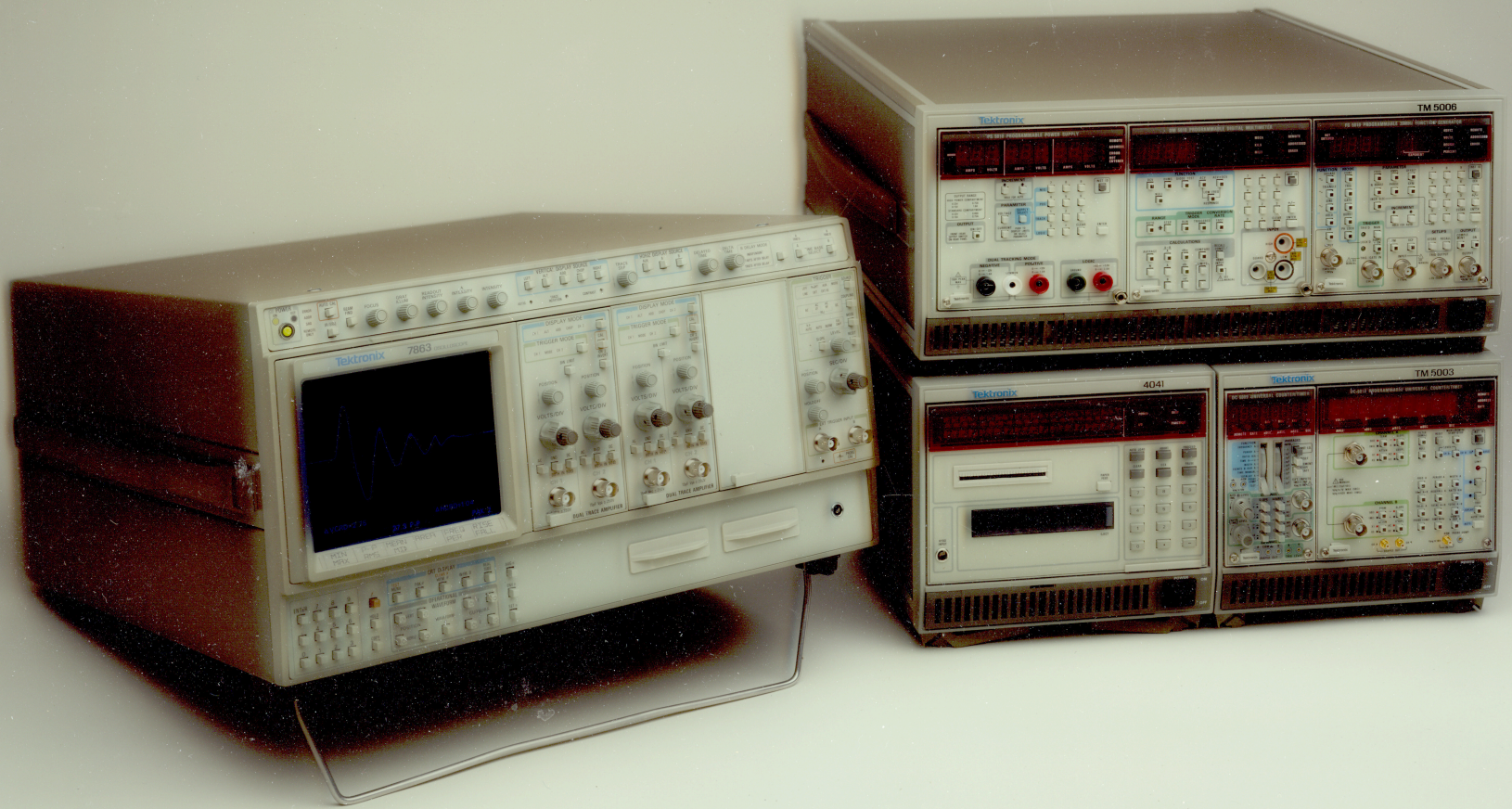
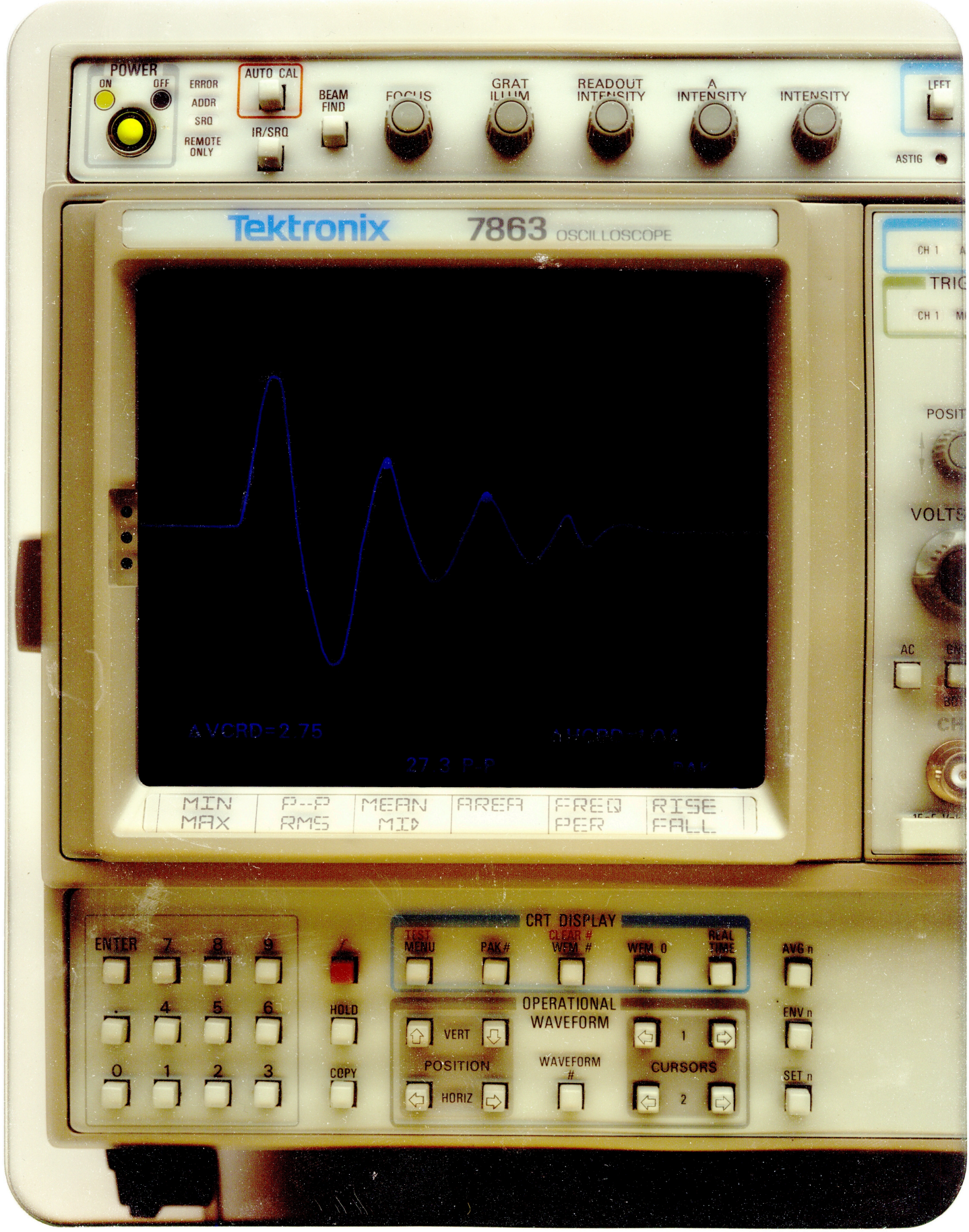
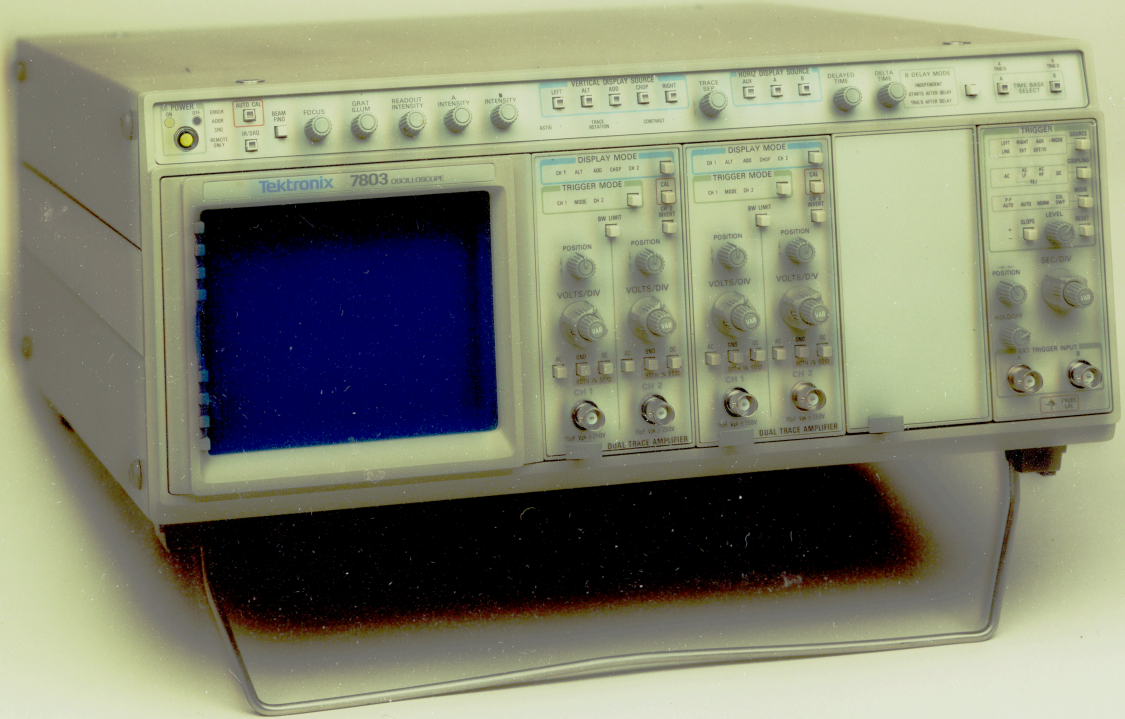
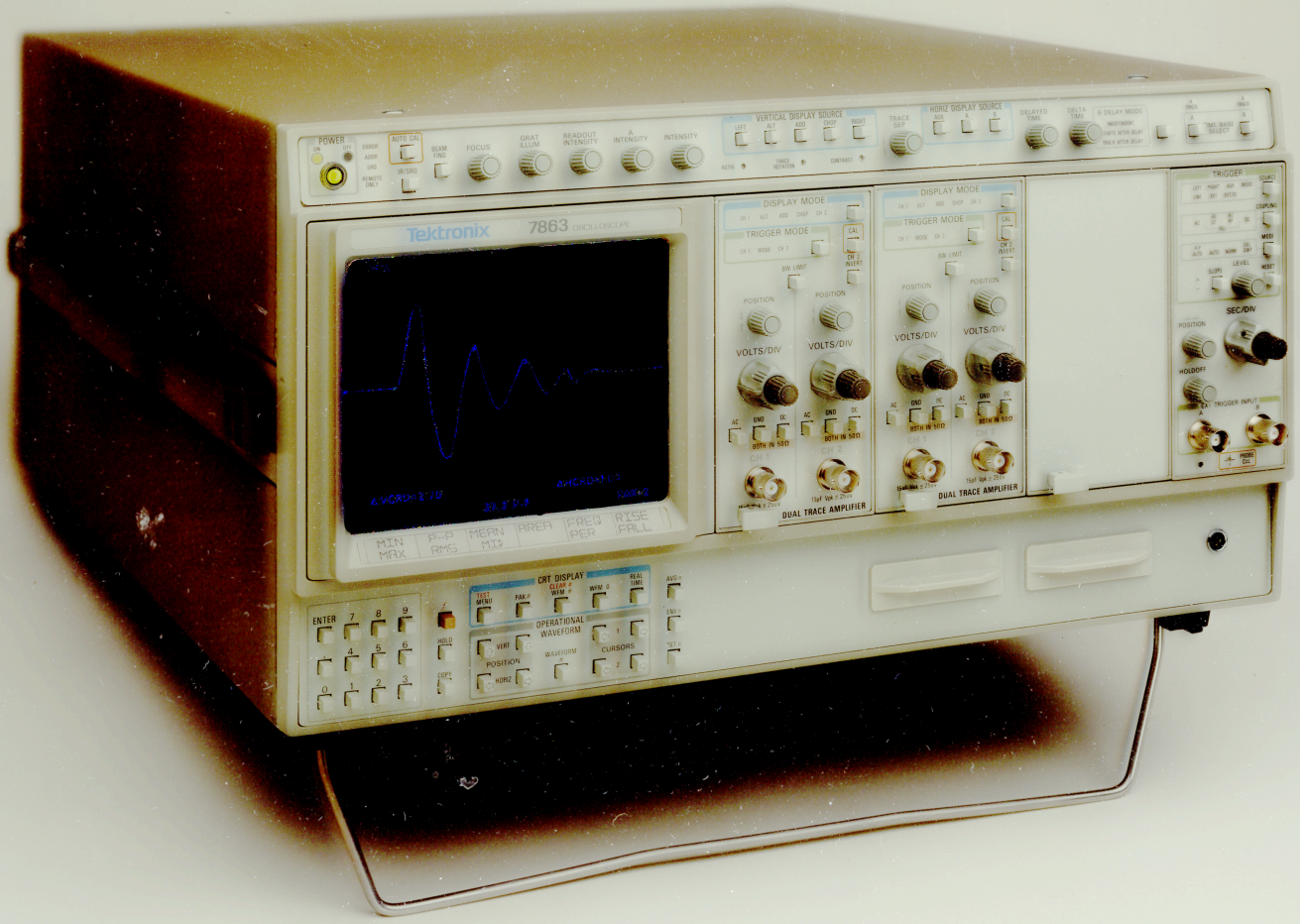
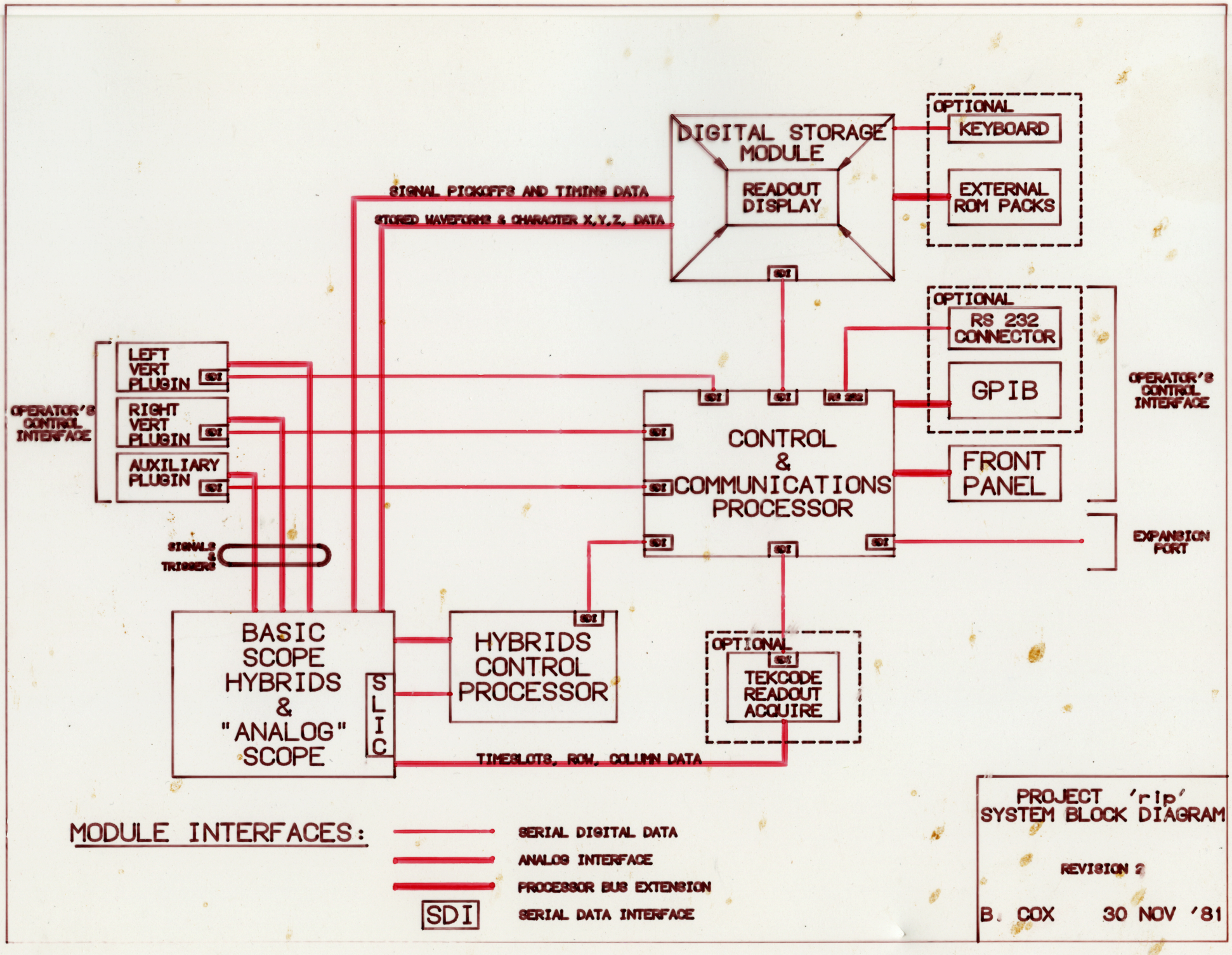

Tektronix
7863
Tektronix
TM 5006
Tektronix
4041
Tektronix
TM 5003

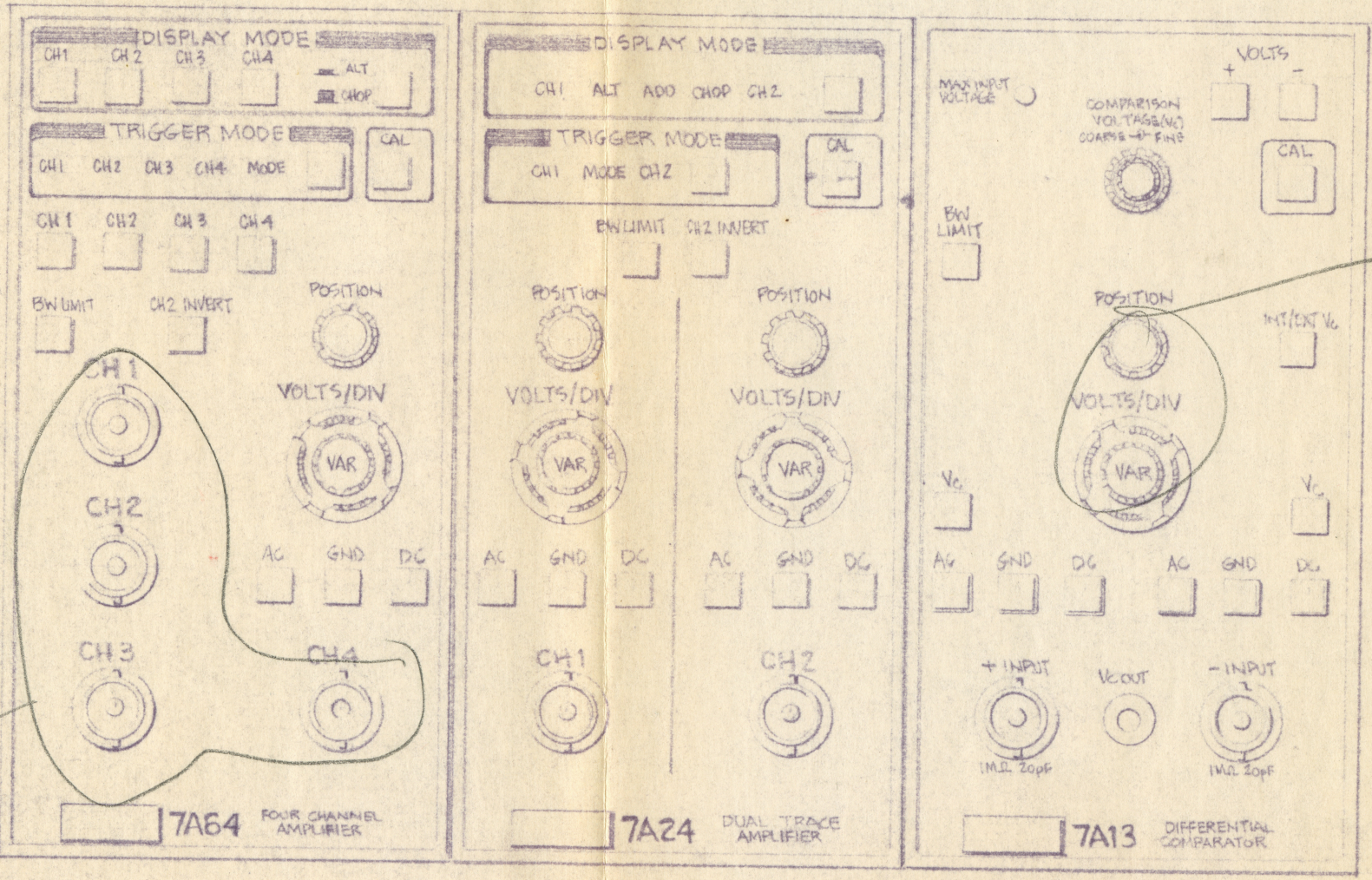

POWER
ON
OFF
ERROR
ADDR
SRQ
REMOTE ONLY
AUTO CAL
IR/SRQ
BEAM FIND
FOCUS
GRAT ILLUM
READOUT INTENSITY
A INTENSITY
INTENSITY
LEFT
ASTIG
Tektronix
7863 OSCILLOSCOPE
CH 1
TRIG
CH 1
POSIT
VOLTS
AC
MIN MAX
P-P RMS
MEAN MID
AREA
FREQ PER
RISE FALL
ENTER
7
8
9
4
5
6
0
1
2
3
HOLD
COPY
CRT DISPLAY
TEST MENU
PAK#
CLEAR # WFM #
WFM 0
REAL TIME
AVG n
OPERATIONAL WAVEFORM
VERT
POSITION
HORIZ
WAVEFORM #
CURSORS
1
2
ENV n
SET n


Tektronix 7803 OSCILLOSCOPE
DISPLAY MODE
TRIGGER MODE
POSITION
VOLTS/DIV
DUAL TRACE AMPLIFIER
TRIGGER
SEC/DIV


Tektronix
7863
DUAL TRACE AMPLIFIER
DUAL TRACE AMPLIFIER


DIGITAL STORAGE MODULE
READOUT DISPLAY
OPTIONAL
KEYBOARD
EXTERNAL ROM PACKS
SIGNAL PICKOFFS AND TIMING DATA
STORED WAVEFORMS & CHARACTER X,Y,Z, DATA
SDI
OPTIONAL
RS 232 CONNECTOR
GPIB
OPERATOR'S CONTROL INTERFACE
LEFT VERT PLUGIN
RIGHT VERT PLUGIN
AUXILIARY PLUGIN
OPERATOR'S CONTROL INTERFACE
CONTROL & COMMUNICATIONS PROCESSOR
FRONT PANEL
EXPANSION PORT
SIGNALS & TRIGGERS
BASIC SCOPE HYBRIDS & "ANALOG" SCOPE
SLIC
HYBRIDS CONTROL PROCESSOR
OPTIONAL
TEKCODE READOUT ACQUIRE
TIMESLOTS, ROW, COLUMN DATA
MODULE INTERFACES:
SERIAL DIGITAL DATA
ANALOG INTERFACE
PROCESSOR BUS EXTENSION
SDI
SERIAL DATA INTERFACE
PROJECT 'rip'
SYSTEM BLOCK DIAGRAM
REVISION 2
B. COX 30 NOV '81

ure welcome to bleed all over this, Cliff



unnecessarily crowded.

Looks funny. How do all the probe comp boxes fit?

JERRY WRISLEY
JAN 5 1982

20 minutes

Introduction

What I'm going to talk about

Program Overview

~~Status + Reasons~~ of 7DX & Reasons Changes are Needed

Clusters

Projects & 5 year Plan

This Project

This Project

Key Goals More Reliable Manufactureable Lower Cost Serviable

Describe Dupont Products

Digital Storage Scope Features

Realtime ~~Hurdle~~ Fallout

Architecture

Form Factor
3 Plug
Timebase
Programmability

Goals

Manufacturability, Reliability, Serviceability

—How

Time Line

Questions

Project rip Overview

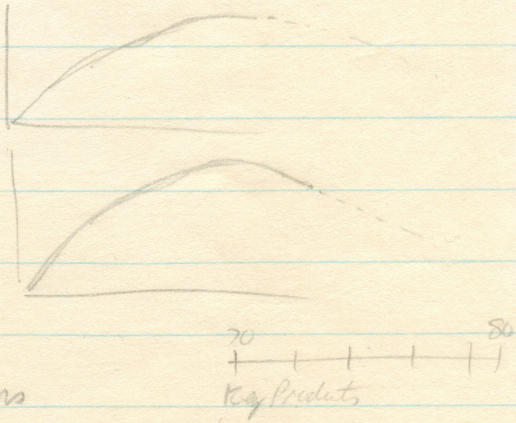
The purpose of this presentation is to familiarize you with the new mainframe project recently started in Lab Scopes — 7000 Series. Coded name "rip"

Agenda
- Lab Scopes Master Plan
- Project rip's relation to the plan
- Project Goals
- Product Descriptions
- Project Plan
- Questions

Lab Scopes is embarking on a major program to rejuvinate and replace the entire 7000 Series product line over the next 7 years.

Why bother?

Indicators for a Change
- Sales in dollars has flattened
- Sales in unit volume is declining
- Today, Lab Scopes contributes over 50% of the Company's profits



- Average age of the product line >8 yrs

70% revenue come products 8-10 years old

~~• Price/Performance ratio is not a good value to customers~~
~~- Old technology (discrete, small scale integration)~~
~~-~~

• Products beginning to fail to meet customer expectations
- Digital Storage
- Functional Programmability
- Poor Value — cost/performance
- Limited flexibility due to architecture.
- Automated System Applications

old technology
discrete
small scale integrat

Reasons that Corrections are worth our effort
- Customers are still basically interested in DK
  they're asking for corrections
- Inspite of deficiencies, sales are stronger than one might otherwise expect
- Continued high profits important for supplying cash for Teks other activities

~~• Price/Performance ratio is not a good value to customers~~
~~- Old technology (discrete, small scale integration)~~
~~-~~

• Products beginning to fail to meet customer expectations
- Digital Storage
- Functional Programmability
- Poor Value — cost/performance
- Limited flexibility due to architecture.
- Automated System Applications

old technology
discrete
small scale integrat

Reasons that Corrections are worth our effort
- Customers are still basically interested in 7K
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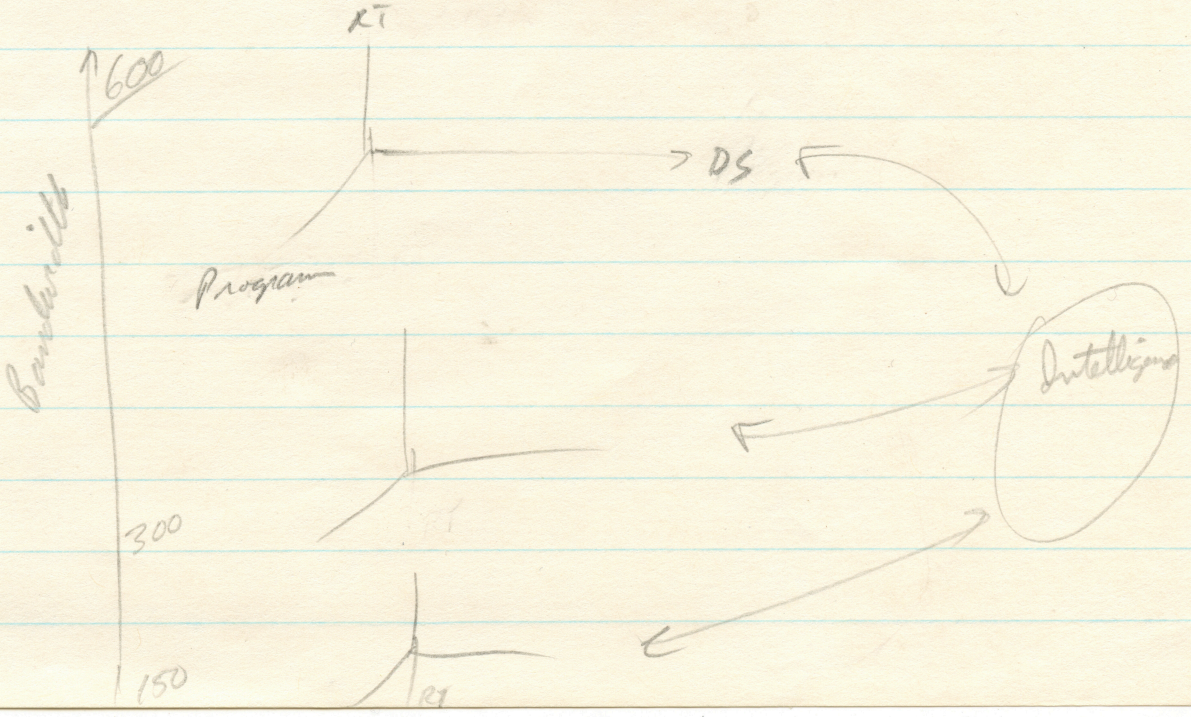
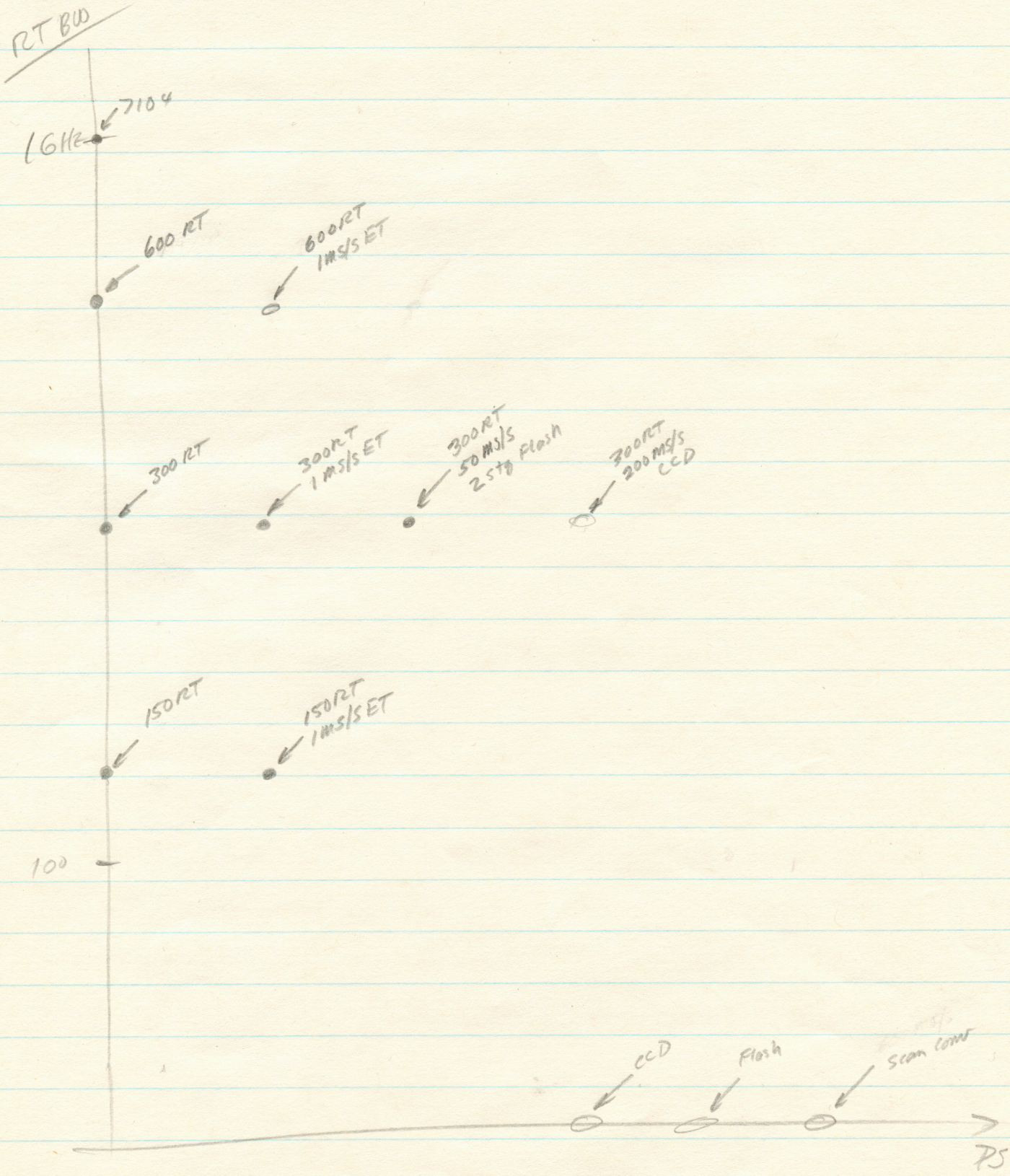
7 year plan

- rejuvinate conventional products
- establish full range of digitizer calability including technological superiority
- Upgrade the family architeture for new features & future flexibilty
- Utilize new component and manufacturing technologies, impove reliabilty, serviceabilty in order improve product value.

Multi dimension performance parameters.

key: Programmability
Systems vs Bench applications
Digital Storage
Level of Intelegence
Bandwidth (Sweep Speed, CRT)




RT BW
7104
1 GHz
600 RT
600 RT
1 MS/S ET
300 RT
300 RT
1 MS/S ET
300 RT
50 MS/S
2 Stg Flash
300 RT
200 MS/S
CCD
150 RT
150 RT
1 MS/S ET
100
CCD
Flash
Scan Conv
PS

Plug-ins

- Dual Trace - Hi Z Low-Z
- Differential
- 4-Trace
- Serial Word Recognizer
- Combinatorial Word Recognizer
- TV frame + Line trigger
- Fiber Optics TDR
- Sampling

Project Goals:

- Digital Storage Scope + Realtime on the market by early FY500
- 2 Stage Flash within a year after
- Realtime Scope cost within 20% of comparable 2465
- DS models to be the best value on the market, ~~two~~ very profitable
- Improved Manufacturing Process
- Quantum improvements in Reliability

Product Descriptions

Plain Scope

Form Factor — rack or bench
easier to build
" " Service
compatible with TM-5000
cart mobile measurment system

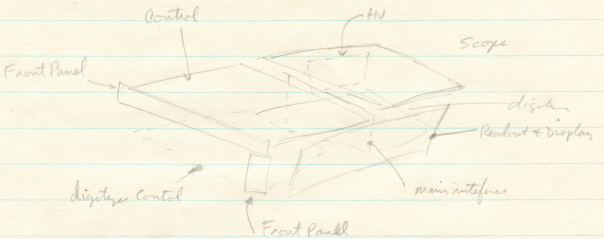
3 plug-ins with built in trimbars

AUX hole

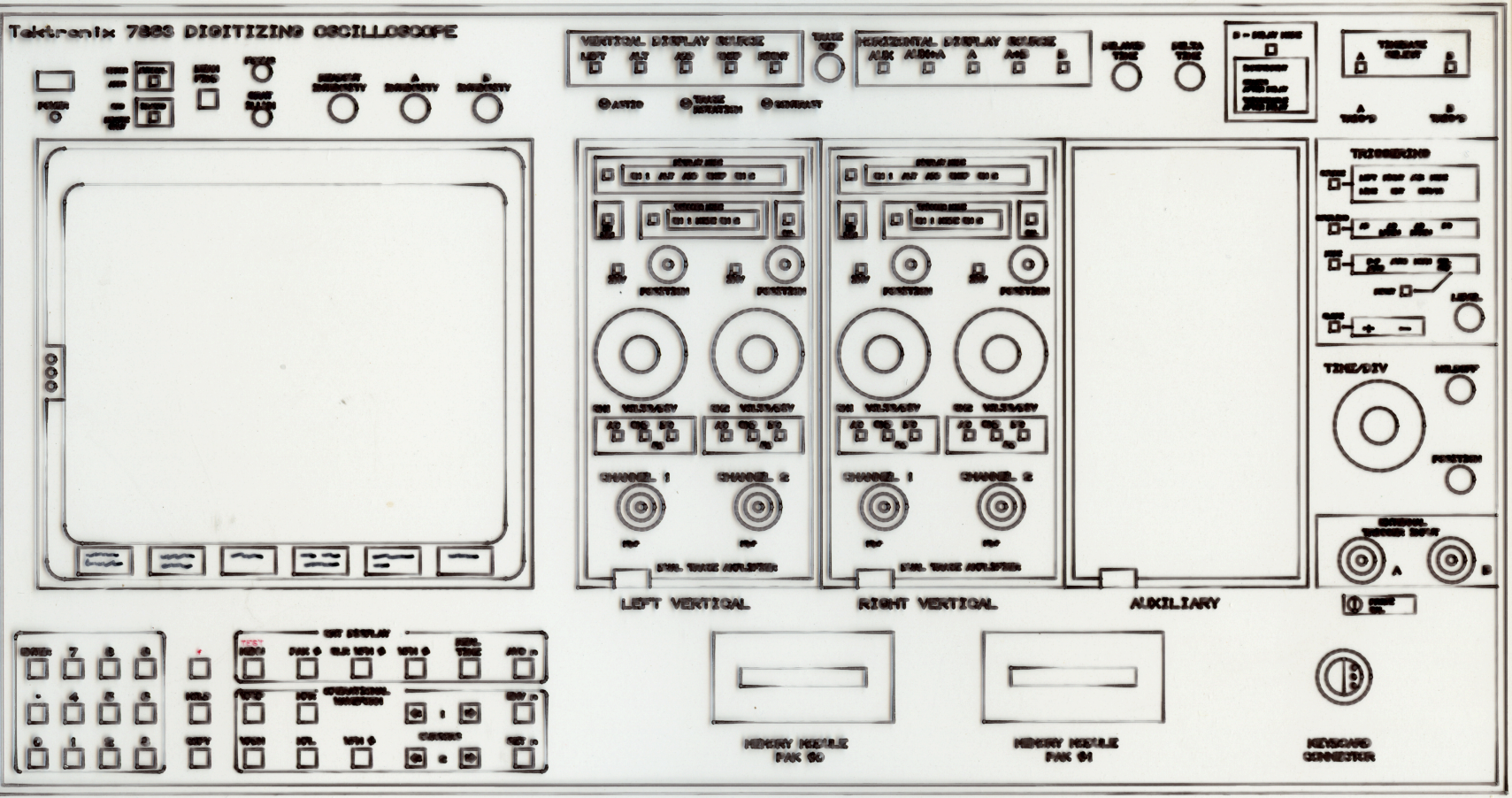
Large screen CRT

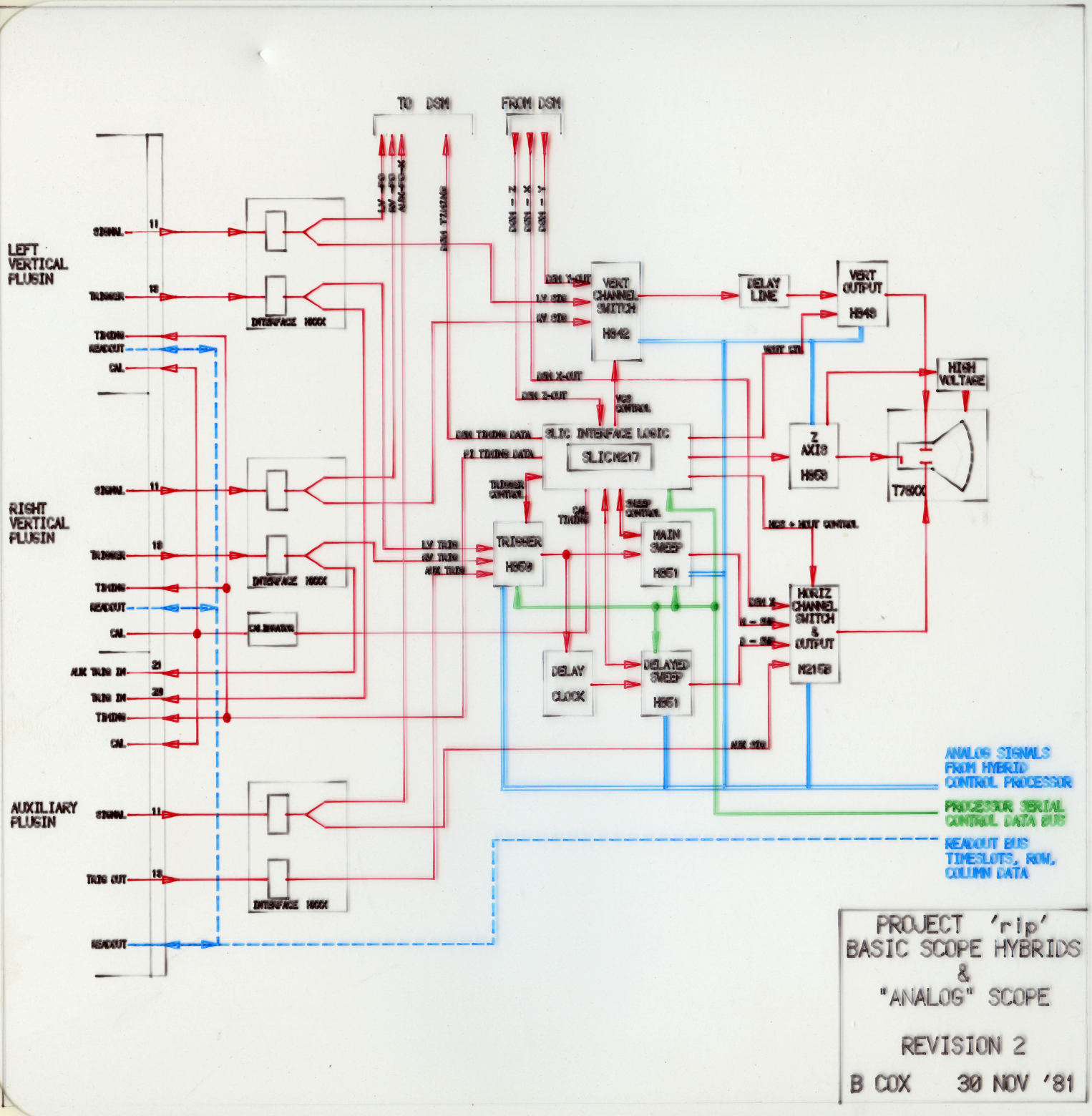
Digital Storage

Internal Layout



Block diagrams

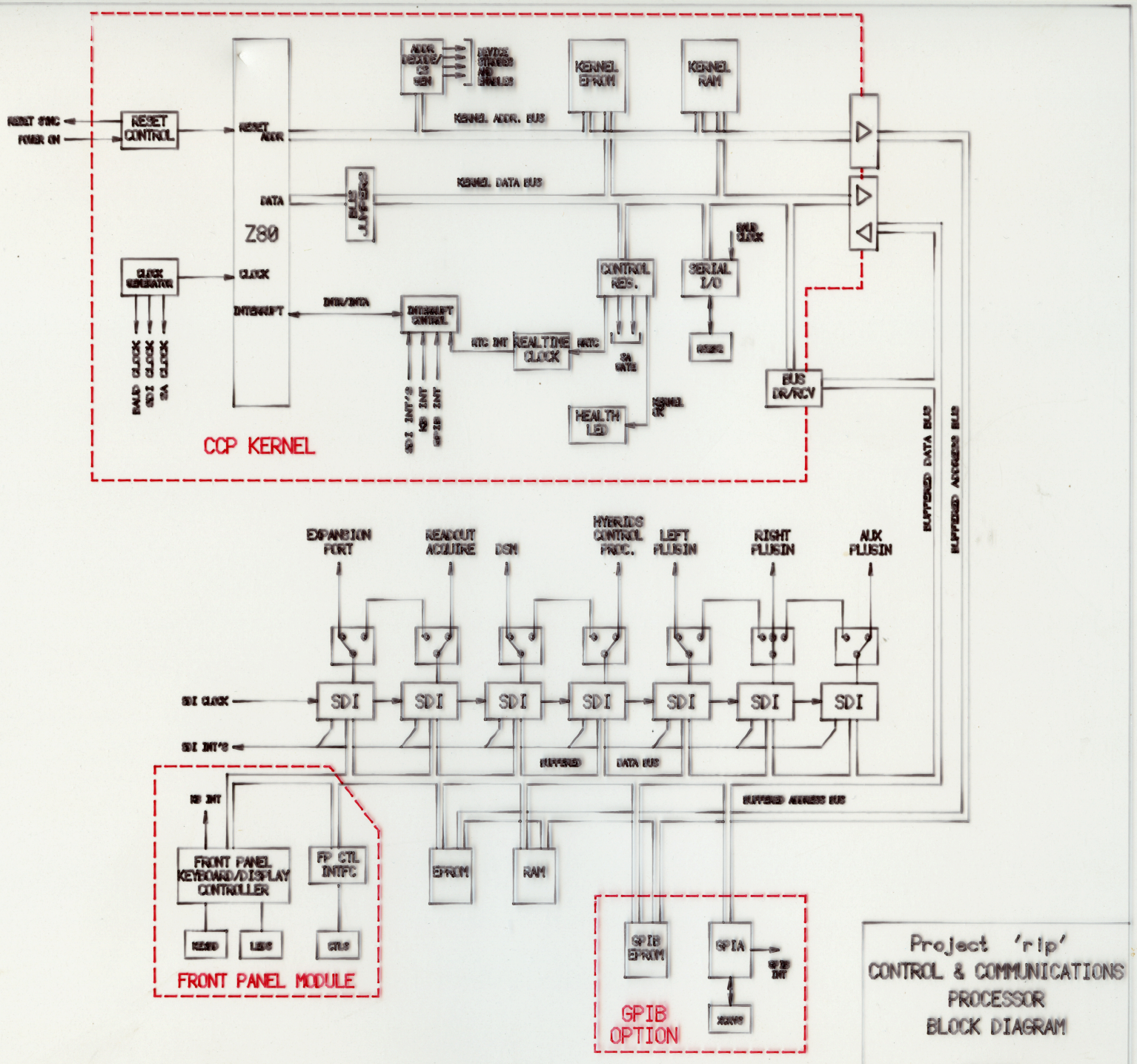

Tektronix 7603 DIGITIZING OSCILLOSCOPE
VERTICAL DISPLAY SOURCE
HORIZONTAL DISPLAY SOURCE
TRIGGERING
TIME/DIV
LEFT VERTICAL
RIGHT VERTICAL
AUXILIARY
MEMORY MODULE PAK 00
MEMORY MODULE PAK 01
KEYBOARD CONNECTOR



PROJECT 'rip'
BASIC SCOPE HYBRIDS
&
"ANALOG" SCOPE

REVISION 2

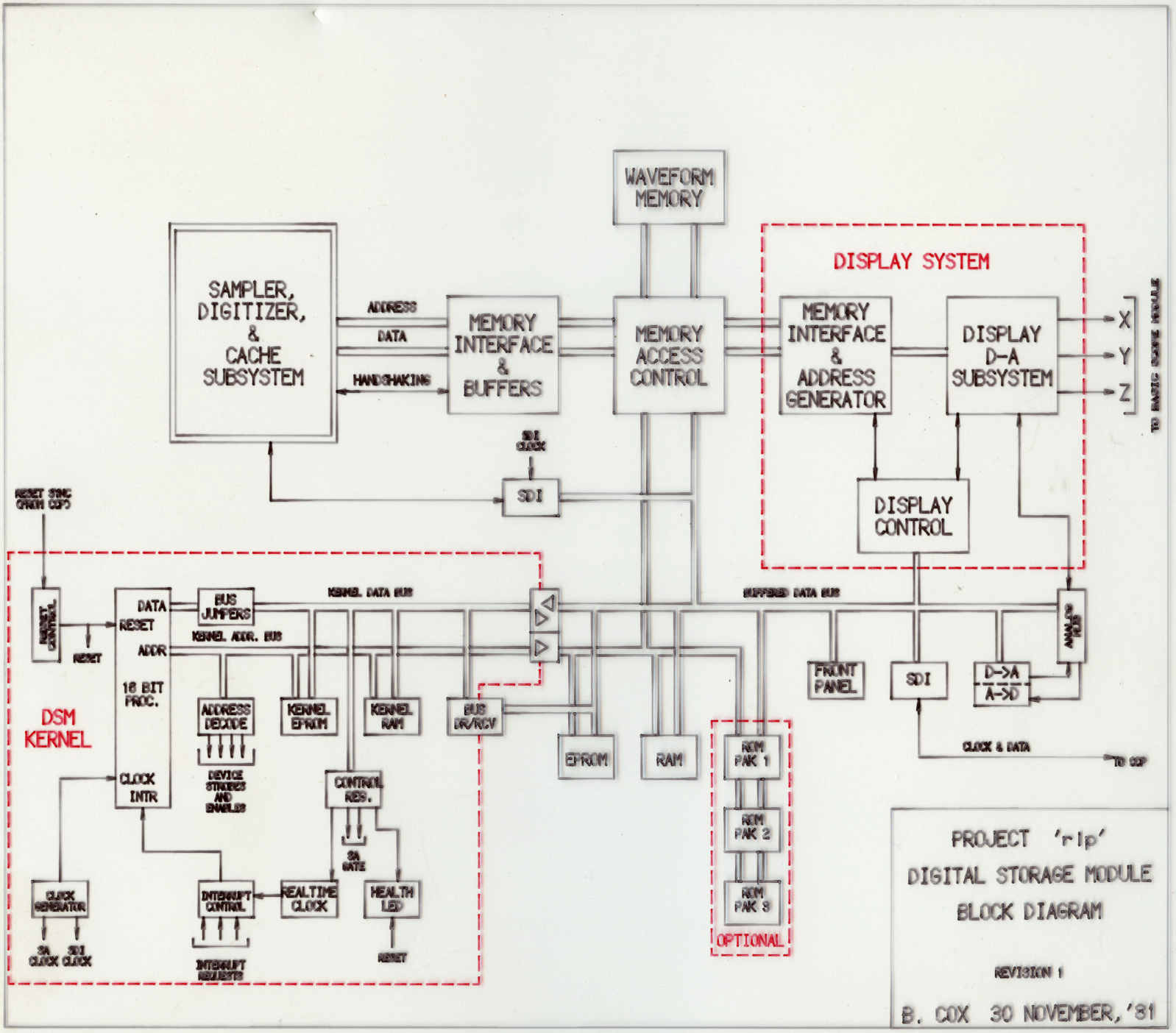
B COX 30 NOV '81

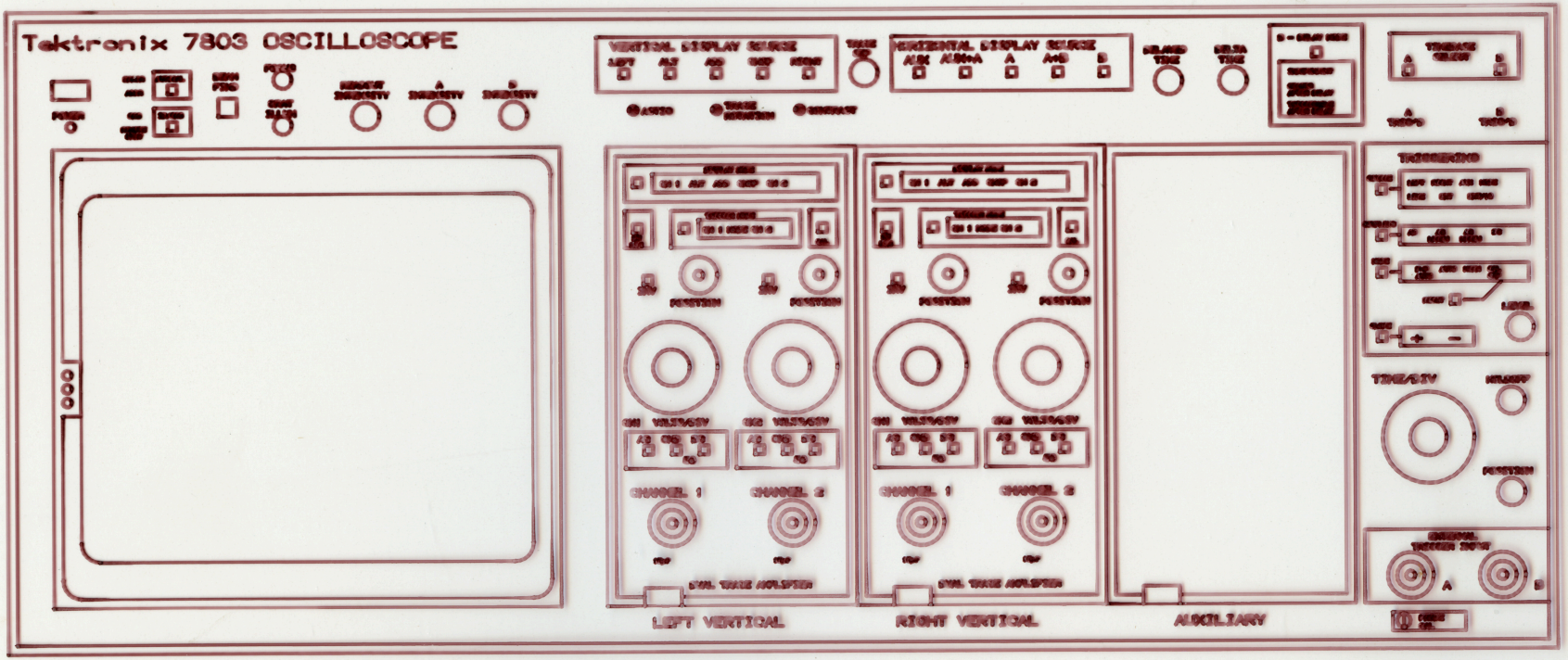


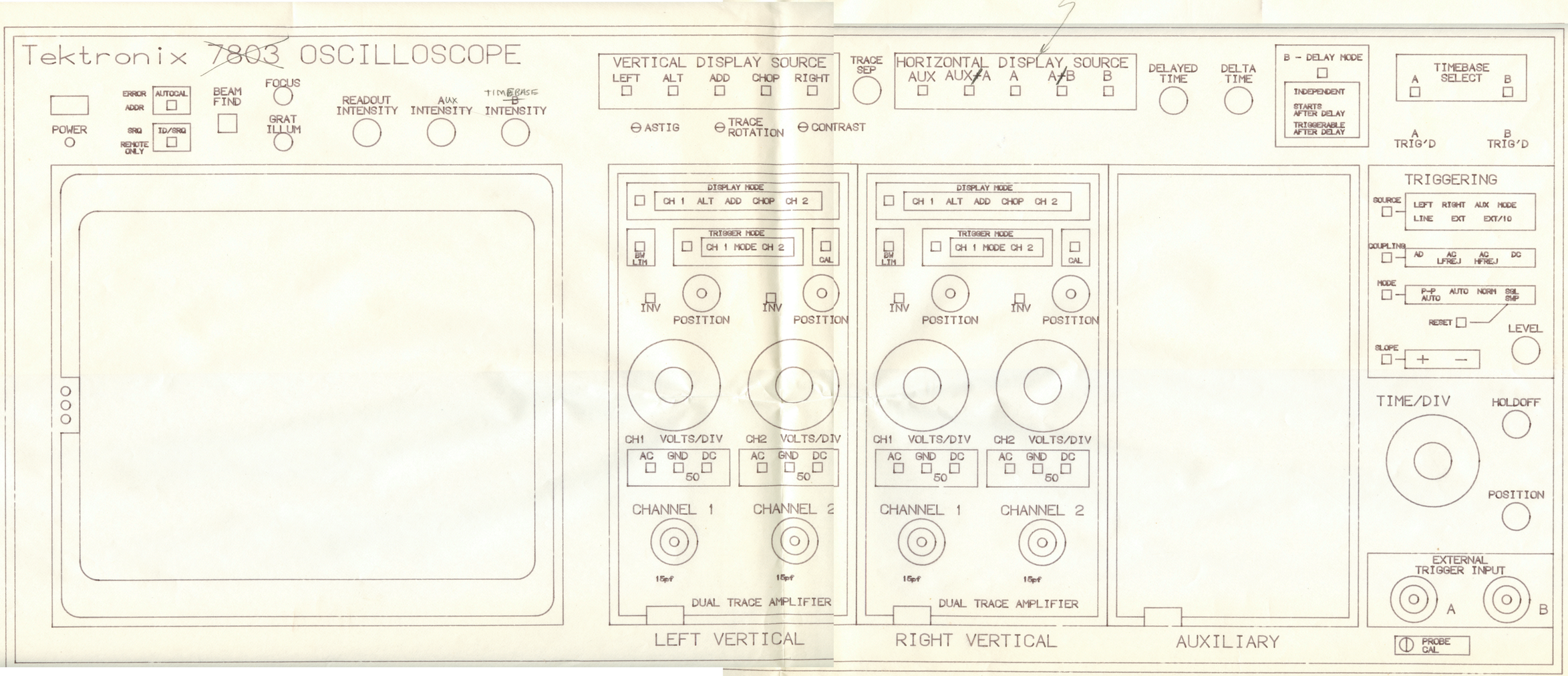
Project 'rip'
CONTROL & COMMUNICATIONS PROCESSOR
BLOCK DIAGRAM

REVISION 1

B. COX 30 NOVEMBER, '81

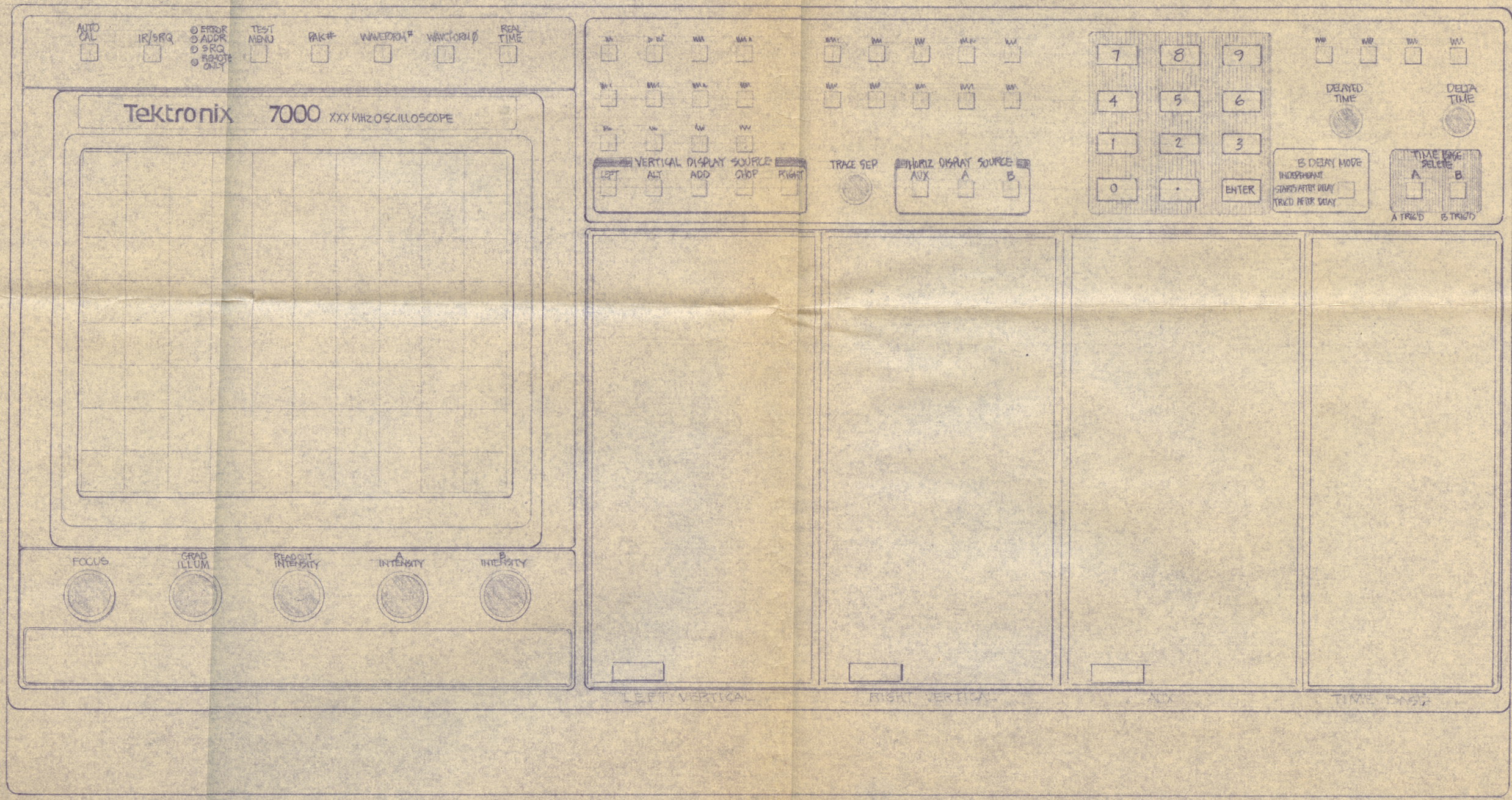

WAVEFORM MEMORY
SAMPLER, DIGITIZER, & CACHE SUBSYSTEM
ADDRESS
DATA
HANDSHAKING
MEMORY INTERFACE & BUFFERS
MEMORY ACCESS CONTROL
DISPLAY SYSTEM
MEMORY INTERFACE & ADDRESS GENERATOR
DISPLAY D-A SUBSYSTEM
X
Y
Z
TO BASIC SCOPE MODULE
SDI CLOCK
SDI
DISPLAY CONTROL
RESET SYNC (FROM CDP)
RESET CONTROL
RESET
DATA
RESET
ADDR
16 BIT PROC.
CLOCK
INTR
BUS JUMPERS
KERNEL DATA BUS
KERNEL ADDR. BUS
BUFFERED DATA BUS
ANALOG OUTPUTS
DSM KERNEL
ADDRESS DECODE
DEVICE STROBES AND ENABLES
KERNEL EPROM
KERNEL RAM
BUS DR/RCV
CONTROL REG.
3A GATE
CLOCK GENERATOR
INTERRUPT CONTROL
REALTIME CLOCK
HEALTH LED
3A CLOCK
3B1 CLOCK
INTERRUPT REQUESTS
RESET
EPROM
RAM
ROM PAK 1
ROM PAK 2
ROM PAK 3
OPTIONAL
FRONT PANEL
SDI
D->A
A->D
CLOCK & DATA
TO CDP
PROJECT 'rip'
DIGITAL STORAGE MODULE
BLOCK DIAGRAM
REVISION 1
B. COX 30 NOVEMBER, '81


Tektronix 7603 OSCILLOSCOPE
VERTICAL DISPLAY SOURCE
HORIZONTAL DISPLAY SOURCE
TRIGGERING
LEFT VERTICAL
RIGHT VERTICAL
AUXILIARY

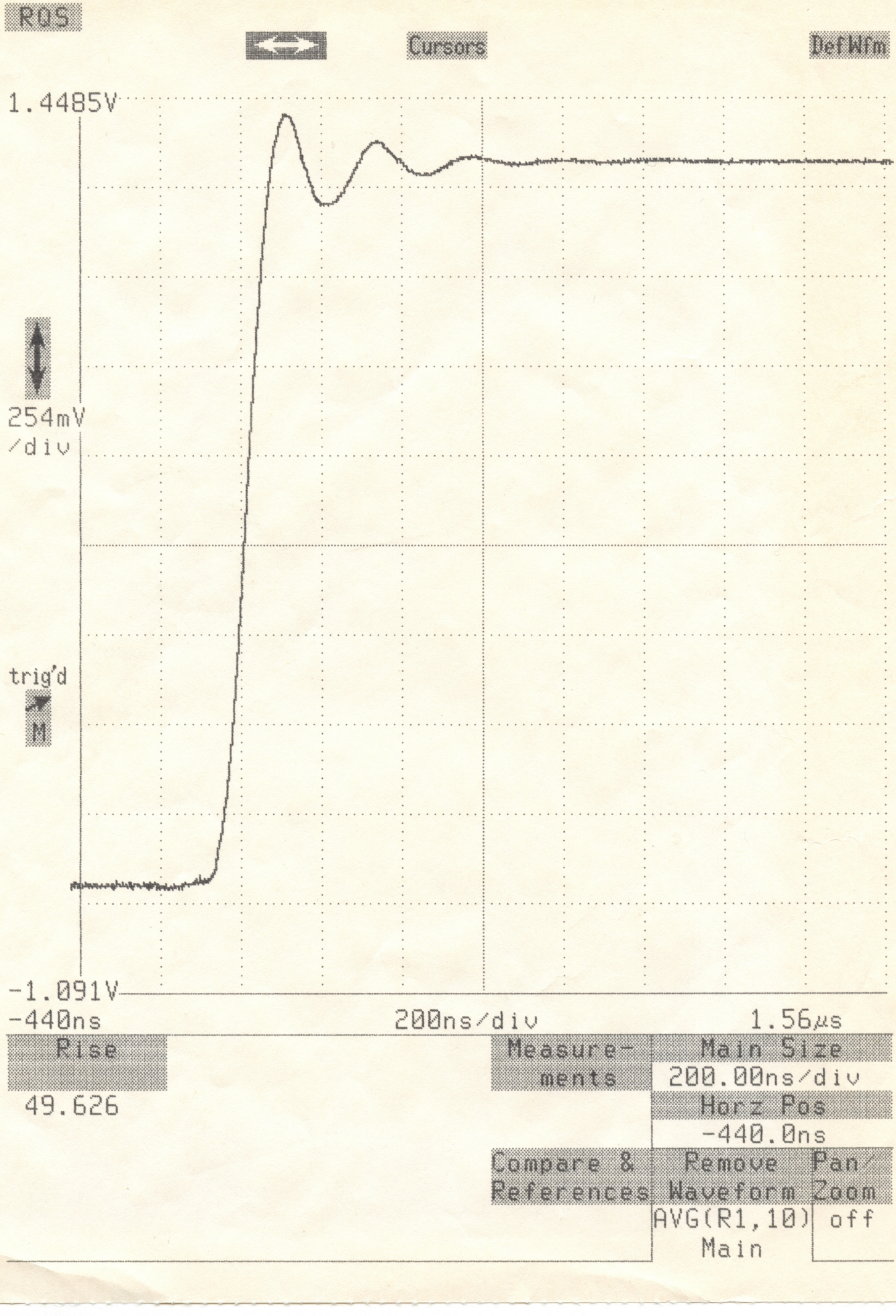


HORIZONTAL DISPLAY
AUX CHOP TIMEBASE
A ALT B

X10MAG?
Trace Seps?



J.WRISLEY MAY (1, 82


RQS
Cursors
DefWfm
1.4485V
254mV
/div
trig'd
M
-1.091V
-440ns
200ns/div
1.56µs
Rise
49.626
Measure-
ments
Main Size
200.00ns/div
Horz Pos
-440.0ns
Compare &
References
Remove
Waveform
Pan/
Zoom
AVG(R1,10)
Main
off

7 June 81

Tektronix 7XXX OSCILLOSCOPE

POWER

ERROR
ID
SRQ
REMOTE ONLY

CAL

ID/RQS

BEAM FIND

GRAT ILLUM

FOCUS

READOUT INTENSITY

WAVEFORM INTENSITY

VERTICAL DISPLAY MODE
LEFT ADD RIGHT AUX ALT CHOP

ASTIG

TRACE ROTATION

CONTRAST

VERT TRACE SEP

HORIZONTAL DISPLAY MODE
AUX A B ALT CHOP

DELAYED TIME

Δ TIME

TIMEBASE SELECT
A B

INTENSITY BALANCE

A TRIG'D

B TRIG'D

TRIGGERING
SOURCE: LEFT RIGHT AUX MODE / LINE EXT EXT ÷10
COUPLING: AC AC LFREJ AC HFREJ DC
MODE: PP AUTO AUTO NORM SGL SWP
RESET
SLOPE: + −
LEVEL

DISPLAY MODE
CH1 ALT ADD CHOP CH2

BW LIM

TRIGGER MODE
CH1 MODE CH2

CAL

INV

POSITION IDENTIFY

CH1 VOLTS/DIV

CH2 VOLTS/DIV

1MΩ DC
50Ω GND AC

CHANNEL 1

CHANNEL 2

20 pF
VPK < 250

DUAL TRACE AMPLIFIER

7AXX

LEFT VERT

RIGHT VERT

AUXILIARY
100 MHz MAX

TIME/DIV

HOLDOFF

POSITION

EXTERNAL TRIGGER INPUT
A B

0.4 Vpp
1 KHz

Tektronix 7XXXP DIGITIZING OSCILLOSCOPE

POWER

ERROR
ID
SRQ
REMOTE ONLY

CAL

ID/RQS

BEAM FIND

GRAT ILLUM

FOCUS

STORED INTENSITY

REALTIME INTENSITY

VERTICAL DISPLAY MODE
LEFT ADD RIGHT ALT CHOP

ASTIG

TRACE ROTATION

CONTRAST

VERT TRACE SEP

HORIZONTAL DISPLAY MODE
A B ALT CHOP

DELAYED TIME

Δ TIME

TIMEBASE SELECT
A B

INTENSITY BALANCE

A TRIG'D

B TRIG'D

DISPLAY MODE
CH1 ALT ADD CHOP CH2

TRIGGER MODE
CH1 MODE CH2

BW LIM

CAL

INV

IDENTIFY POSITION

CH1 VOLTS/DIV

CH2 VOLTS/DIV

IMP
DC
SRC GND AC

CHANNEL 1

CHANNEL 2

20pF
VPK ≤ 250

7AXXP DUAL TRACE AMPLIFIER

LEFT VERT

RIGHT VERT

AUXILIARY
100 MHZ MAX BW

TRIGGERING
SOURCE
LEFT RIGHT AUX MODE
LINE EXT EXT ÷10
COUPLING
AC AC LFREJ AC HFREJ DC
MODE
PP AUTO AUTO NORM SGL SWP
RESET
SLOPE
+ −
LEVEL

HOLDOFF

TIME/DIV

POSITION

EXTERNAL TRIGGER INPUT
A B

0.4 VPP 1 KHZ

6 7 8 9
2 3 4 5
WFM MEMORY DISPLAY COPY
0 1

ACQUISITION CONTROL
AVG ABR GND STOP

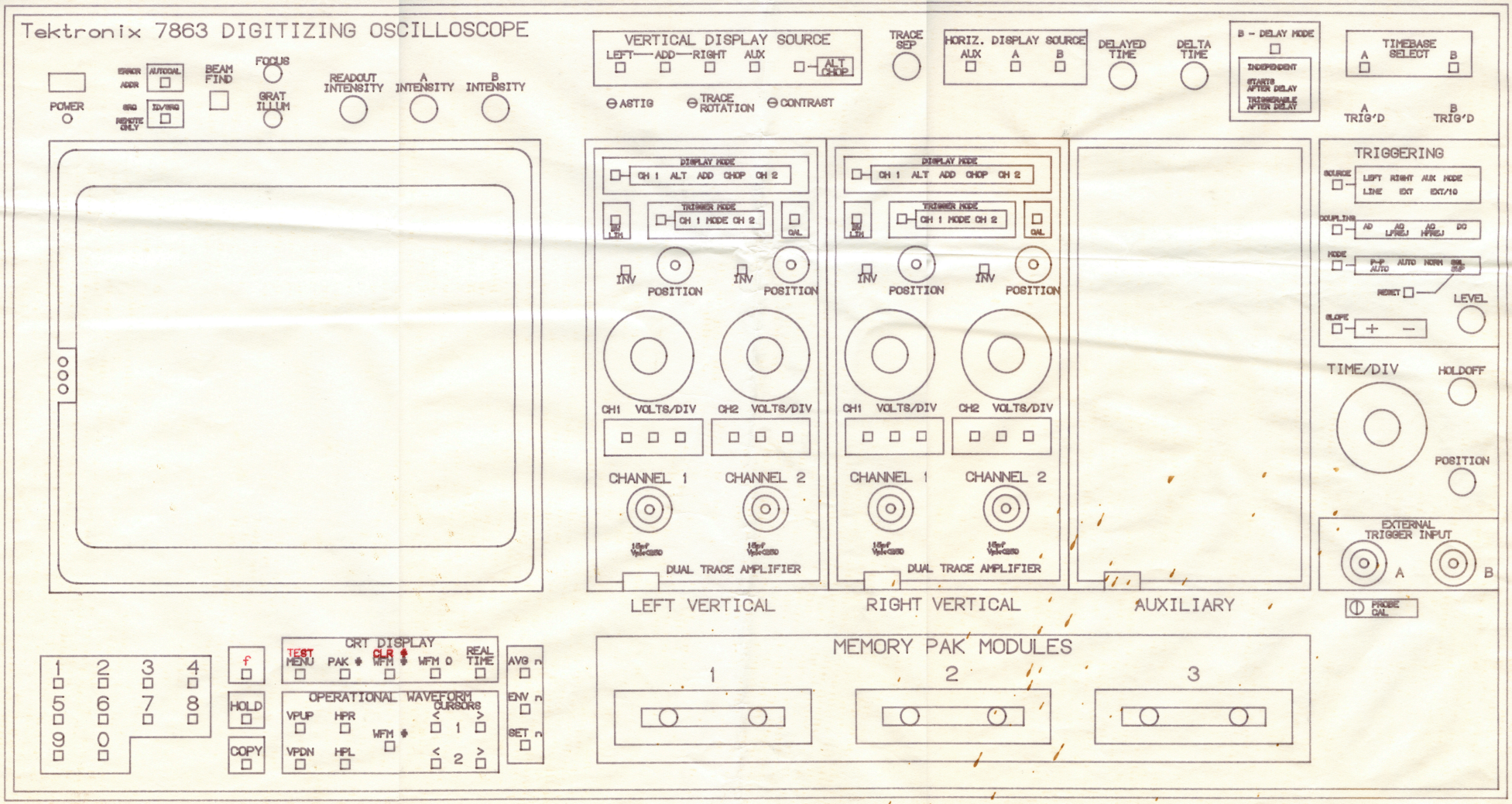
CRT DISPLAY
REALTIME STORED

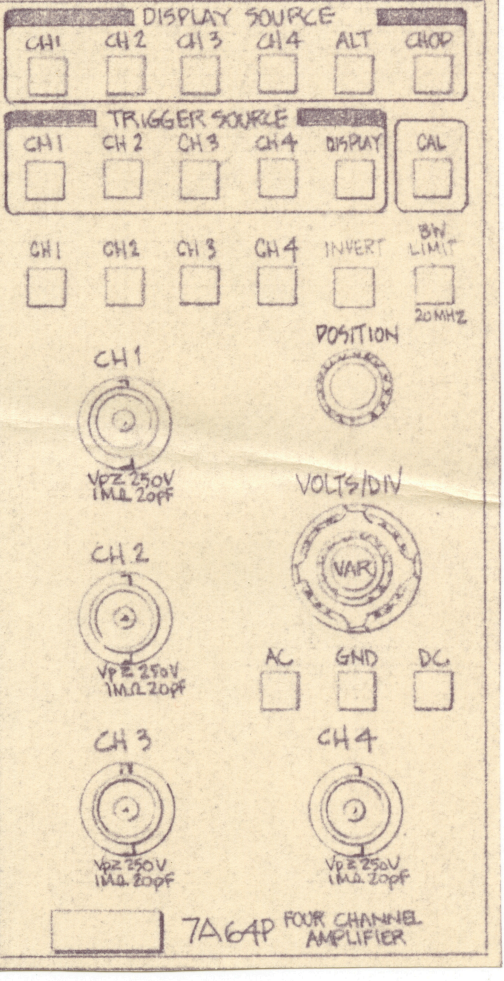
CURSORS
ONE DOT
TWO DOT
CURS 1 POS
CURS 2 POS

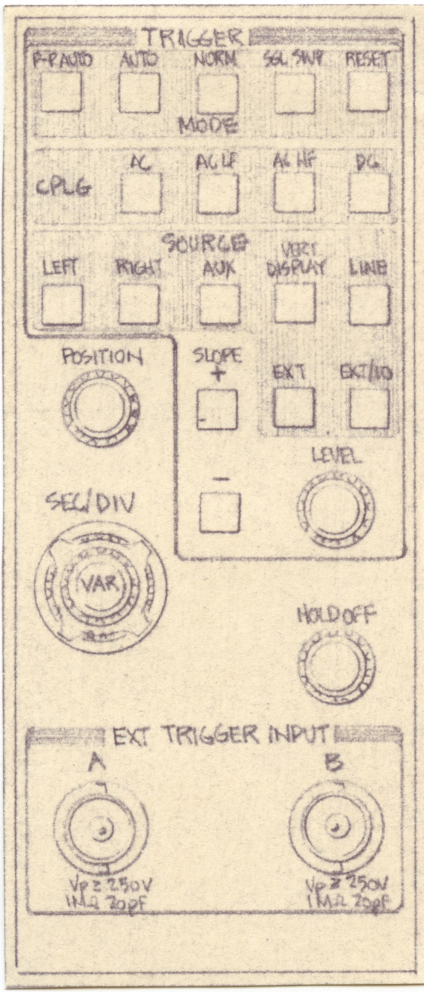
RESTART

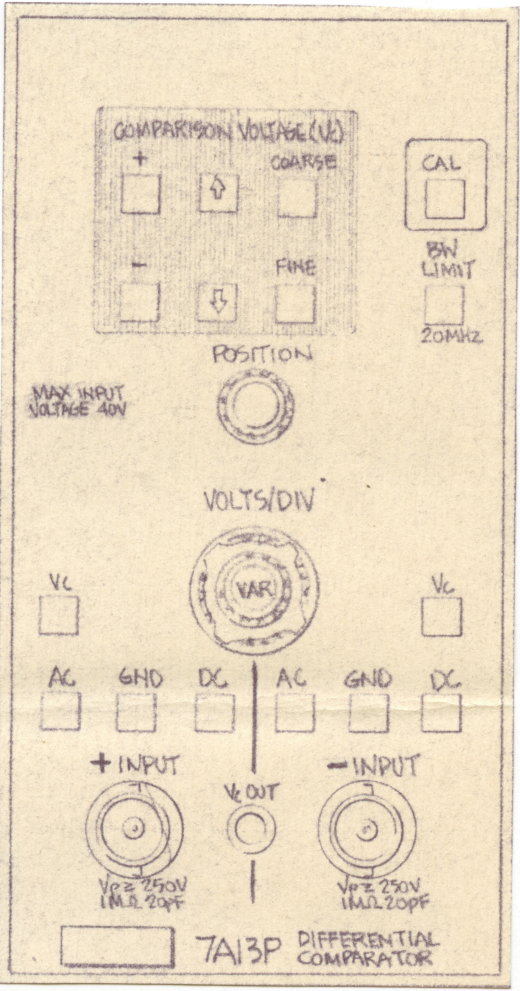
FP CONTROLS
SAVE RECALL

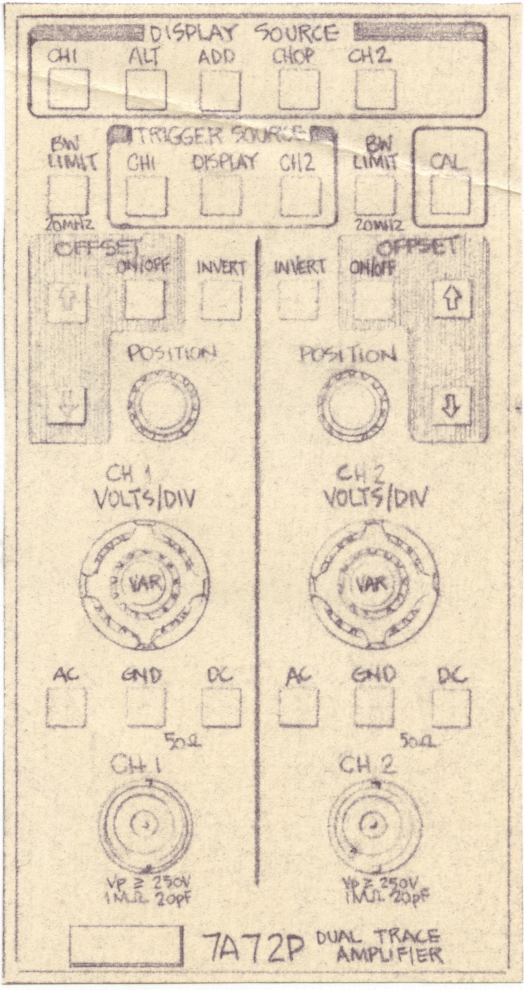
B. COX
6/5/81


Tektronix 7863 DIGITIZING OSCILLOSCOPE
POWER
ERROR
ADDR
ERR
REMOTE ONLY
AUTOCAL
ID/ERR
BEAM FIND
FOCUS
GRAT ILLUM
READOUT INTENSITY
A INTENSITY
B INTENSITY
VERTICAL DISPLAY SOURCE
LEFT
ADD
RIGHT
AUX
ALT CHOP
ASTIG
TRACE ROTATION
CONTRAST
TRACE SEP
HORIZ. DISPLAY SOURCE
AUX
A
B
DELAYED TIME
DELTA TIME
B - DELAY MODE
INDEPENDENT
STARTS AFTER DELAY
TRIGGERABLE AFTER DELAY
TIMEBASE SELECT
A
B
A TRIG'D
B TRIG'D
DISPLAY MODE
CH 1 ALT ADD CHOP CH 2
TRIGGER MODE
CH 1 MODE CH 2
INV
POSITION
CH1 VOLTS/DIV
CH2 VOLTS/DIV
CHANNEL 1
CHANNEL 2
DUAL TRACE AMPLIFIER
LEFT VERTICAL
RIGHT VERTICAL
AUXILIARY
TRIGGERING
SOURCE
LEFT RIGHT AUX MODE
LINE EXT EXT/10
COUPLING
AC LFREJ AC HFREJ DC
MODE
P-P AUTO AUTO NORM SGL SEQ
RESET
SLOPE
LEVEL
TIME/DIV
HOLDOFF
POSITION
EXTERNAL TRIGGER INPUT
A
B
PROBE CAL
1 2 3 4
5 6 7 8
9 0
f
HOLD
COPY
CRT DISPLAY
TEST MENU
PAK
CLR
WFM
WFM 0
REAL TIME
OPERATIONAL WAVEFORM CURSORS
VPUP
HPR
VPDN
HPL
AVG n
ENV n
SET n
MEMORY PAK MODULES
1
2
3


DISPLAY SOURCE
CH1
CH2
CH3
CH4
ALT
CHOP
TRIGGER SOURCE
CH1
CH2
CH3
CH4
DISPLAY
CAL
CH1
CH2
CH3
CH4
INVERT
BW LIMIT
20MHZ
POSITION
CH1
VPP 250V
1MΩ 20pF
VOLTS/DIV
VAR
CH2
VPP 250V
1MΩ 20pF
AC
GND
DC
CH3
VPP 250V
1MΩ 20pF
CH4
VPP 250V
1MΩ 20pF
7A64P FOUR CHANNEL AMPLIFIER


TRIGGER
P-P AUTO
AUTO
NORM
SGL SWP
RESET
MODE
CPLG
AC
AC LF
AC HF
DC
SOURCE
LEFT
RIGHT
ALT
VERT DISPLAY
LINE
POSITION
SLOPE
+
-
EXT
EXT/10
LEVEL
SEC/DIV
VAR
HOLDOFF
EXT TRIGGER INPUT
A
B
Vp ≥ 250V
1MΩ 20pF
Vp ≥ 250V
1MΩ 20pF


COMPARISON VOLTAGE (Vc)
+
COARSE
−
FINE
CAL
BW LIMIT
20MHz
POSITION
MAX INPUT VOLTAGE 40V
VOLTS/DIV
VAR
Vc
Vc
AC
GND
DC
AC
GND
DC
+ INPUT
Vc OUT
− INPUT
Vp-p ≤ 250V
1MΩ 20PF
Vp-p ≤ 250V
1MΩ 20PF
7A13P DIFFERENTIAL COMPARATOR


DISPLAY SOURCE
CH1
ALT
ADD
CHOP
CH2
BW LIMIT
TRIGGER SOURCE
CH1
DISPLAY
CH2
BW LIMIT
CAL
20MHZ
20MHZ
OFFSET
ON/OFF
INVERT
INVERT
ON/OFF
OFFSET
POSITION
POSITION
CH 1 VOLTS/DIV
CH 2 VOLTS/DIV
VAR
VAR
AC
GND
DC
AC
GND
DC
50Ω
50Ω
CH 1
CH 2
VP ≥ 250V 1MΩ 20pF
VP ≥ 250V 1MΩ 20pF
7A72P
DUAL TRACE AMPLIFIER