Tektronix
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1220/1225/1230
LOGIC ANALYZER

PM407

6800/6802 Microprocessor Probe

Operator's Manual

The PM407 has a software version number of 2.51. For use with the PM407, the 1220 and 1225 Logic Analyzers require software versions of 2.5 or above; the 1230 Logic Analyzer requires a software version of 3.03 or above.

Please check for change information at the back of this manual

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OVERVIEW

The PM407 6800/6802 Microprocessor Probe Personality Module consists of a 6800/6802 disassembly probe (with ribbon cable) and this user's manual. This manual shows you how to connect and use the PM407 with the 1220/1225/1230 Logic Analyzers. This manual does not teach you how to use analyzer keypads or menus. For information on using analyzers, refer to the operator's manual for your logic analyzer. For more information about the 6800/6802 microprocessor, refer to your microprocessor data book.

The PM407 Version 2.51 and above works with 1220/1225 Logic Analyzers having software version numbers 2.5 or higher and 1230 Logic Analyzers with software version numbers 3.04 or higher.

The PM407 gives you an interface between the 1220/1225/1230 Logic Analyzer and the 6800/6802-based systems under test (SUT). Along with regular logic analyzer features, the PM407 interface lets you sample data synchronously using the 6800/6802 clock, and display disassembly data in hardware and software formats.

Conventions. This manual uses these conventions:

- The term analyzer refers to the 1220, 1225, and 1230 Logic Analyzers unless otherwise specified.
- The term SUT refers to the 6800/6802 system under test.
- Active low signals are identified by a bar over the signal name, for example, $\overline{\text{NMI}}$.

ANALYZER CONFIGURATION

You must have at least 32 channels in the 1230 to use the PM407. This is because the probe uses 32 channels to acquire synchronous data from the 6800/6802-based SUT. You must also use a version 2.51 and above for the PM407 if you're using either a 1220/1225 version 2.5 (or higher) or a 1230 version 3.04 (or higher). Figure 1 shows the 1230 analyzer and expansion card configuration.

CONNECTING AND POWERING UP

The PM407 probe has two probe cables that connect to the analyzer. Figure 2 shows how the analyzer connects to your SUT.

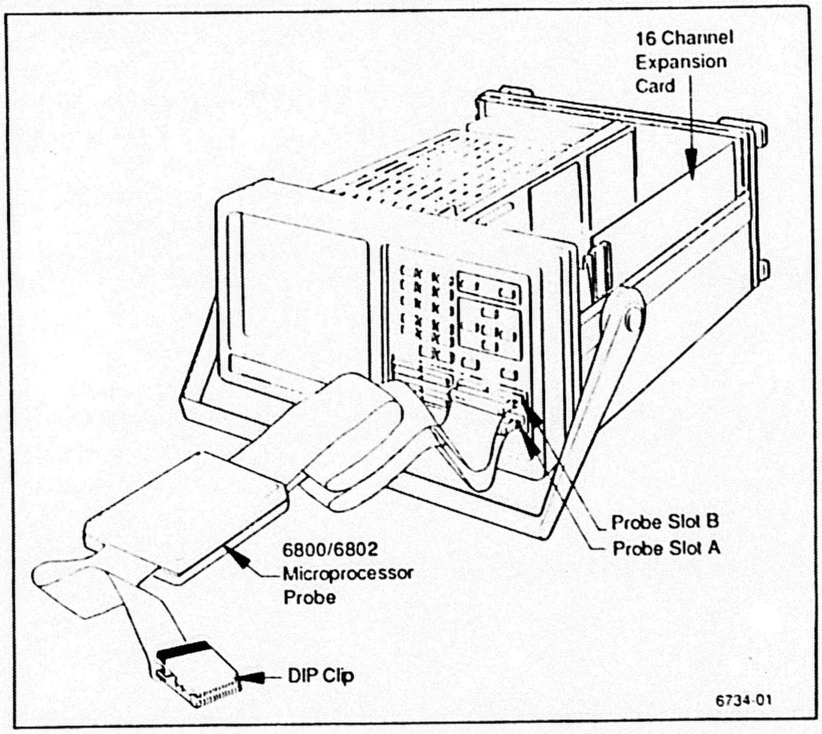

Figure 1. Analyzer configuration with PM407 probe.

Follow these steps to connect the PM407 to the analyzer.

1. Make sure that the power to the analyzer and SUT is off.

CAUTION

Do not connect the PM407 to the analyzer unless power to the a..alyzer is off. Do not connect the PM407 to the SUT unless power to the SUT is off. If you connect the disassembly probe to the SUT when power to the SUT is on and power to the analyzer is off, excessive power can flow through the probe's inputs and damage the probe.

2. Connect the bottom cable from the probe to input A on the front of the analyzer.

3. Connect the top cable from the probe to input B on the front of the analyzer.

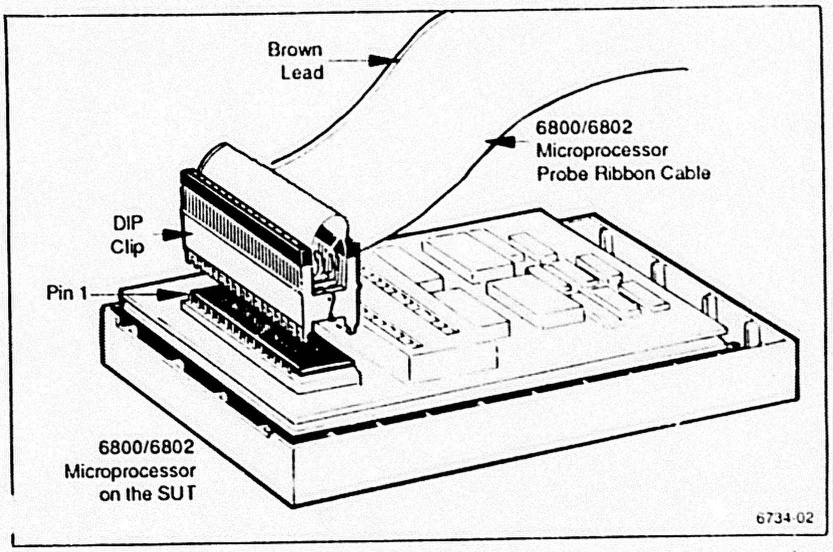

Figure 2. Connecting the DIP clip and SUT. The brown lead goes to pin 1 on the 6800/6802 microprocessor.

4. Connect the PM407 probe clip to the SUT as shown in Figure 2 (power to the SUT should be off). (Figure 3 shows the 6800 pinout, and Table 1 lists analyzer-to-6800/6802 signal line connections. Figure 3 and Table 1 are shown after this procedure.)

5. Turn on the analyzer; this also supplies power to the probe. The analyzer screen now displays the Initialization menu (Figure 4, shown after this procedure).

6. Press ENTER to upload the PM407 disassembly setup into the analyzer. Pressing ENTER overwrites the existing setup and changes the probe links, channel groups, and defined conditions for 6800/6802 disassembly. If you press MENU, the PM407 setup is not uploaded and your displayed disassembled data may be inaccurate.

7. Turn on power to the SUT.

After you press ENTER, the Main menu (Figure 5) is displayed. This menu lists setup, data, and utility features. Since the default disassembly setup defines the setup parameters for you (probe links, sampling rate and format, and conditions), you can press START at any time to acquire data from your SUT. Example 1, later in this manual, shows a data acquisition with the default setup.

Signal Name	6800 Pin Numbers		Signal Name
Vss	1	40	$\overline{\text{RESET}}$
$\overline{\text{HALT}}$	2	39	TSC
$\phi 1$	3	38	NC
$\overline{\text{IRQ}}$	4	37	$\phi 2$
VMA	5	36	DBE
$\overline{\text{NMI}}$	6	35	NC
BA	7	34	IO/R/$\overline{\text{W}}$
Vcc	8	33	D0
A0	9	32	D1
A1	10	31	D2
A2	11	30	D3
A3	12	29	D4
A4	13	28	D5
A5	14	27	D6
A6	15	26	D7
A7	16	25	A15
A8	17	24	A14
A9	18	23	A13
A10	19	22	A12
A11	20	21	Vss

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Figure 3. 6800 pinout. For a pinout of the 6802 refer to your 6800/6802 microprocessor data book.

Table 1
6800/6802 Signals and Analyzer Channels

6800/6802 Signals	122x/1230 Channels	Channel Groups	Description
A15-A00	B15-B00	ADD	Address bus
D07-D00	A15-A08	DAT	Data bus
VMA R/$\overline{W}$	A01 A00	STB	Strobes
$\overline{NMI}$ $\overline{IRQ}$	A03 A02	INT	Interrupts
DBE, RE * $\overline{HALT}$	A05 A04	CTL	Control

*DBE is for the 6800 and RE is for the 6802.

For more information about this table, press NOTES while the Disassembly menu is displayed on the screen.

```
TUE, MAY 31, 1988                                10:22 -DEFAULT

      Tektronix 1230/48 Channel Logic Analyzer, V3.05
      (C) Tektronix, Inc. 1987, 1988 All rights reserved.

   Use the NOTES key whenever information is needed,
          or consult the Operator's Manual.

          X represents DON'T CARE condition.

        OK to load setup from Personality Module?
       (Overwrites current setup and System Links!)
          Press ENTER to confirm, MENU to abort

          Press ENTER to confirm, MENU to abort.
```

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Figure 4. Initialization menu. When you turn the analyzer on with the PM407 plugged in, the Initialization menu includes a message telling you that you can now upload the disassembly setup by pressing ENTER.

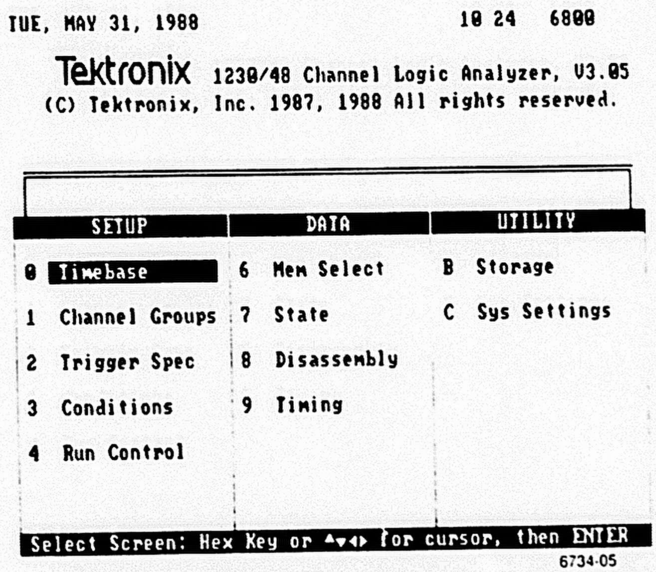

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Figure 5. Main menu. The Main menu always shows disassembly as a menu selection. However, you can display acquired data in disassembly format only when the PM407 is plugged in.

Loading Disassembly Setups. You are not required to upload the disassembly setup when you see the Initialization menu. However, if you don't, you must enter the disassembly setup manually or reset the analyzer so that the PM407 can upload the disassembly setup for you. You can reset the analyzer by pressing NOTES and ENTER at the same time.

Using Probes

The PM407 must always be plugged into slots A and B on the analyzer's front panel. If you have a fully loaded 1230, you can use slots C and D for acquisition probes. If you have a 1225, you can use slot C for an acquisition probe.

Acquisition and disassembly probes can be used together or separately with the 1230 and 1225 Logic Analyzers. The probe in slot A must always be connected to the clock in your SUT. If the probe in slot A is not connected to your SUT clock, the analyzer won't trigger when you press START. If you're using more than one probe and the probes are linked synchronously, each probe must be connected to the same clock point in your SUT. The PM407 DIP clip connects directly to the 6800/6802 microprocessor. Therefore, your connection to the SUT clock is assured.

Online Help

At the bottom of the disassembly screen, a one-line help message tells you which keys to press for disassembly functions. If you need more help, press NOTES. The analyzer then displays in-depth information about 6800/6802 disassembly, including the disassembler's software version number. You can press MENU at any time to exit NOTES and return to the previous display.

SETTING UP TO ACQUIRE DATA

This discussion shows you how the PM407 sets up the analyzer for 6800/6802 disassembly. The setups shown here are for an analyzer with 32 channels. *Example 1: A Simple Acquisition* later in this manual, shows a data acquisition using this 32-channel default setup.

A setup is a set of parameters that describes the current analyzer configuration for data acquisition and storage. For example, the setup includes information about probe links, acquisition rates, threshold voltage, and 6800/6802 trigger conditions.

Timebase

The acquisition timebase, probe links, and threshold voltage for 6800/6802 disassembly are shown in Figure 6. If you're using a 1230, the PM407 uses the synchronous clock rate of your SUT. If you're using a 1220 or 1225, the PM407 is set up for synchronous acquisition at 100 ns or slower.

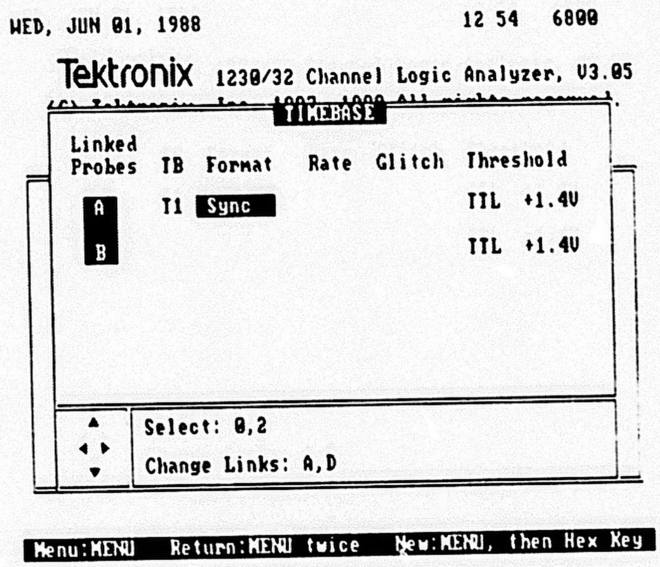

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Figure 6. Timebase menu.

Probe Links. The PM407 is a 32-channel disassembly probe which uses probe slots A and B. For 6800/6802 disassembly, probes A and B are linked together synchronously with the same timebase (T1) so that all disassembly is done with the same acquisition format and rate. If you're also using one or more acquisition probes, the acquisition probes are linked asynchronously in T2. This is the default setup. You can change links if you want to. However, to use the PM407 A and B slots must be linked together.

Clocking. The default disassembly clock format is synchronous so that you use the clock rate in your SUT as the data sampling rate. The PM407 probe automatically qualifies your SUT clock with software internal to the probe. There are no external clock qualifiers for the PM407.

For the 1230, the clock rate is set by your SUT. For the 1220/1225, the default clock rate is ⩾100 ns. For 6800/6802 disassembly, you must use a clock rate of ⩾100 ns if you're using a 1220/1225.

Glitch Capture. The 6800/6802 disassembly probe does not acquire glitches. Therefore, it is not possible to enter the Glitch field.

Channel Grouping

The PM407 sets up the analyzer's channel groups as shown in Figure 7. The Channel Grouping menu shows how the channel groups are named; for example, ADD for the address bus. If you have any acquisition probes connnected to connectors C and D, their channels will be listed under the UNUSED CHANNELS list. To acquire data on these channels you must add them to group GPF. *Example 3: Cross Triggering* later in this manual adds channels from connector C.

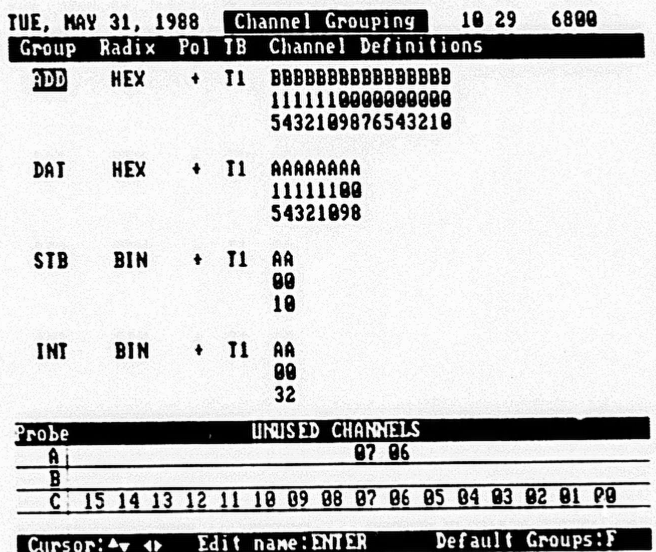

Figure 7. Channel Grouping menu. The control lines (CTL) are listed after the interrupt (INT) lines.

Trigger Conditions

The Conditions menu lets you define data conditions which the analyzer can recognize and trigger on. When you upload the 6800/6802 setup, the 6800/6802 input signals are grouped to correspond to the analyzer channels as listed earlier in Table 1. The conditions listed in Table 2 show the logic states corresponding to 6800/6802 operations.

Table 2
6800/6802 Cycle Types and Analyzer Conditions

Signal Line	ADD hex	DAT bin	STB bin	INT bin	CTL bin
MEM READ	XXXX	XX	11	XX	XX
MEM WRIT	XXXX	XX	10	XX	XX
$\overline{\text{RESET}}$	FFFE	XX	XX	XX	XX
$\overline{\text{NMI}}$	XXXX	XX	XX	0X	XX
$\overline{\text{IRQ}}$	XXXX	XX	XX	X0	XX
S/W INT	FFFA	XX	XX	XX	XX
/DBE6800	XXXX	XX	XX	XX	0X
/RE6802	XXXX	XX	XX	XX	0X
$\overline{\text{HALT}}$	XXXX	XX	XX	XX	0X

Figure 8 shows the default Conditions menu and Trigger Spec menu. You can change the conditions if you want to. The trigger statement shown in the figure is for a 1230. If you're using a 1220/1225, the default trigger action is START instead of TRIG.

```
TUE, MAY 31, 1988   Trigger Spec      10:30   6800
Level      Condition  Count        Action    Dest

1    IF     [MEM_READ]*[0001] THEN [ TRIG ] & [ FILL ]

2

                    CONDITIONS
Symbol      ADD  DAT STB INT CTL
            hex  hex bin bin bin
MEM_READ:   XXXX XX  11  XX  XX
MEM_WRIT:   XXXX XX  10  XX  XX
RESET   :   FFFE XX  XX  XX  XX
NMI     :   XXXX XX  XX  0X  XX

  ▲     Edit Symbol: ENTER
 ◀ ▶    Window Up  : F
  ▼     Window Down: C

Menu:MENU   Return:MENU twice   New:MENU, then Hex Key
```

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Figure 8. Conditions menu and Trigger Spec menu. The default condition window is large enough to show four of the defined conditions. Table 2 lists all signals/conditions defined for the PM407 probe. The default trigger statement is an if-then statement with the first condition, MEM READ, as the trigger condition. For the 1230, the trigger action is TRIG. For the 1220/1225, the trigger action is START.

Trigger Specification

The default trigger statement is an if-then statement. At initialization, the analyzer is set to trigger and fill memory when the condition MEM READ occurs. Figure 8 shows the Trigger Spec menu along with the Conditions menu.

Run Control

When you initialize the analyzer, the Run Control menu is set up as shown in Figure 9. The default display for acquired data is a disassembly display. The trigger position is set at memory location 1024, and the analyzer looks for the trigger after the pretrigger memory is full.

The Run Control menu also sets the memory-compare mode to Manual and tells you that the default channel mask for comparing memories is MEM READ, which is also the default trigger condition. A window (or viewport) at the bottom of the screen lists the value for MEM READ. Remember that channels set to X (don't care) are masked, or not compared, during a memory comparison.

```
TUE, MAY 31, 1988        Run Control        10 30    6800

 Update Memory    : [1]       Display: [Disassembly]
 Trigger Position: [1024]      0 ______________________ 2K
 Look for Trigger: [After Pre-Trigger Memory Full]
==========================================================
 Compare          : [Manual]
 Compare Memory 1 to Memory: [2]


 Compare Mem Locations: [0000] to [1747]
 Use Channel Mask     : [MEM_READ]
 Display Data at least: [5] seconds
==========================================================
            ADD  DAT STB INT CTL
 Symbol     hex  hex bin bin bin
 MEM_READ:  XXXX XX  11  XX  XX
==========================================================
 Cursor: ▲▼◀▶        Select: 0,2
```

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Figure 9. Run Control menu.

SETTING UP TO DISASSEMBLE CODE

Once you've set up the analyzer for disassembly, you can start to acquire and display data from your SUT. Your logic analyzer's operator manual tells how to display data in state and timing formats. This discussion shows you how to display disassembled 6800/6802 data, which you can do only when the PM407 is connected to the analyzer.

Regardless of how you set up timebases and channel groups, the PM407 will display disassembly data for your SUT.

Displaying in Hardware or Software Mode. With the PM407 attached, you can display disassembled data in hardware or software mode. In hardware display mode, the analyzer shows all bus operations and displays every acquired cycle. In software display mode, the analyzer shows only instructions; reads and writes are suppressed so that the display looks like an assembly listing. You can toggle between display modes by pressing DON'T CARE. For a complete discussion of these modes refer to *Using the Hardware* or *Software Display Mode* later in this manual.

Disassembly Mnemonics. The PM407 lets you display acquired data in disassembly mnemonics. Disassembly mnemonics are assembly-language instructions that have been disassembled from a machine language program. For example, 6800/6802 disassembly mnemonics include RTS, PSH, PUL, NOP, JMP, and LDA. An actual disassembly line might read LDAA 6002, which means "load accumulator A with the data at address 6002". Figure 10 shows an example of disassembly mnemonics.

```
TUE, MAY 31, 1988  Disasm: Memory 1   10:34   6800
Loc   Addr Data 6800   Disassembly   Operation  Status
2038  C448 48                        MEM READ   NOT VMA
2039  C449 00                        MEM READ
2040  E431 39   RTS                  OPC FETCH
2041  E432 86                        MEM READ
2042  C449 00                        MEM READ   NOT VMA
2043  C44A E4                        MEM READ
2044  C44B 3A                        MEM READ
2045  E43A 85  *BITA    #80          OPC FETCH
2046  E43B 80                        MEM READ
2047  E43C 27                        MEM READ

0000  0000 00   ???                  OPC FETCH  HALT
0001  E432 86   LDAA    #00          OPC FETCH
0002  C449 00                        MEM READ   NOT VMA
0003  C44A E4   ANDB    3A,X         OPC FETCH
0004  C44B 3A                        MEM READ
0005  E43A 85                        MEM READ
0006  E43B 80                        MEM READ
0007  E43C 27                        MEM READ
-0008-E43D-F9---ADCB---84BD----------OPC FETCH-----------
Func:F     Scroll: ⇄     Cursor: ◂▸     Jump: ENTER
```

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Figure 10. Disassembly mnemonics in hardware mode. In this hardware disassembly display, the curosr marks tl e current location in memory. The blank line separates the beginning and end of memory. The question marks indicate an invalid opcode. Figure 11 shows a software display that corresponds to this figure.

Displaying 6800 or 6802 Disassembly. You can set up your display for a 6800 or 6802 disassembly. Simply press C to switch from a 6800 disassembly display to a 6802 display. The name of the particular processor being displayed is located in the header line between Data and Disassembly.

Invalid Opcodes. The PM407 can display two different types of invalid opcodes. One occurs when the analyzer doesn't find a valid opcode. This type of invalid opcode is displayed with three question marks in the Disassembly column under the microproessor name. This usually occurs at the begining of memory as shown in Figure 10.

The other type of invalid opcode occurs when the opcode is not disassembled completely. In this case, the opcode is dimmed in the display and proceeded with an asterisk (*) as shown in Figure 10.

Mark Opcode Function. The 6800/6802 microprocessor doesn't indicate fetch cycles with control lines. However, the PM407 features a mark opcode function so you can determine which cycles are opcode fetches. This function disassembles again from a location you choose.

The mark-opcode function is most useful at the beginning of acquisition memory to get a correct disassembly started. Disassembly may not be correct if you started at the beginning or end of acquisition memory where instruction cycles may not all have been stored. If you suspect that the disassembly is incorrect, move the cursor bar to the location at which you want the second disassembly to begin. Then press 6. The PM407 changes the first possible location to an OPC FETCH operation and displays the new disassembled data from that point. This function only works in hardware mode.

Notes. The PM407 provides on-line help. Press the NOTES key while the Dissassembly menu is displayed on screen. There are five pages of notes available that discuss channel configuration, hardware and software modes, plus features that are specific to the PM407.

Searching for Events. Searching for events in the Disassembly menu works the same as searching for events in the State menu. Press 0 or 2 to cycle through the available conditions and the trigger event. Press 1 to execute the search.

When the analyzer finds the search event, it redraws the disassembly screen so that the cursor on the search event is in the middle of the screen. If you searched for an event that did not occur, the analyzer displays the message Not Found. The menu bars at the bottom of the screen lists the current search event. For more information about searching, refer to your logic analyzer's operator manual.

The analyzer can display and search for opcode fetches in software mode. However, since reads and writes (which are not opcode fetches) are suppressed in software mode, the analyzer cannot display or search for those instructions. If you're using software mode and you search for an event that is not an opcode fetch, the analyzer sets the cursor to the previous opcode fetch and displays the instruction where the previous valid search event occurred.

Using the Hardware Display Mode

For disassembly displays in hardware mode, the analyzer displays each sample location with address and data from the 6800/6802 bus cycle. Disassembled instructions are displayed at the beginning of each valid machine cycle. Figure 12, later in this discussion, shows a hardware disassembly display.

In the displays, the Loc column shows memory locations. The Address column shows the address, and the Data column displays data bus. When the PM407 recognizes the beginning of an instruction, the analyzer disassembles that instruction and displays it in the Disassembly column. The Disassembly column includes data listed under the name of the microprocessor as well as data listed under Disassembly.

The Operation column displays valid R/$\overline{W}$ cycles as MEM READ and MEM WRITE. Applicable bus operations are displayed in the order they occur; for example, an OPC FETCH and then a MEM READ.

The last column displays the status of control lines. In the Status column, the message with the highest priority is listed. For example, if a $\overline{\text{HALT}}$ and an $\overline{\text{IRQ}}$ occur at the same time, the $\overline{\text{HALT}}$ signal is listed in the display. Table 3 lists priorities.

Table 3
Active Control Line Priorities

Active Line	Description
$\overline{\text{HALT}}$	Halt all activity on processor
$\overline{\text{NMI}}$	Nonmaskable interrupt
$\overline{\text{IRQ}}$	Interrupt request
NOT VMA	Not valid memory address
DBE or RE	Data bus (6800); RAM enable (6802)

Pressing DON'T CARE while in the hardware display mode toggles the disassembly screen to the software display mode.

Using the Software Display Mode

The software display mode is useful because it displays only instructions; memory reads and writes are suppressed. The display resembles an assembly or program listing because it shows only one opcode fetch per line and each line must be the start of an instruction sequence. Because of this, the locations displayed are not contiguous. Figure 11 shows a software disassembly display.

```
TUE, MAY 31, 1988  Disasm:  Memory 1   10:36   6800
 Loc   Addr Data          6800   Disassembly  Operation

 1990  E42C 8117          CMPA   #17
 1992  E42E 2402          BCC    E432
 1996  E430 32            PULA                C449=00
 2000  E431 39            RTS                 C44A=E43A
 2005  E43A 8580          BITA   #80
 2007  E43C 27F9          BEQ    E437
 2011  E437 BDE426        JSR    E426         E439=26
 2020  E426 B66002        LDAA   6002         6002=00
 2024  E429 36            PSHA                C449=00
 2028  E42A 847F          ANDA   #7F
 2030  E42C 8117          CMPA   #17
 2032  E42E 2402          BCC    E432
 2036  E430 32            PULA                C449=00
 2040  E431 39            RTS                 C44A=E43A
 2045  E43A 8580         *BITA   #80

 0000  0000 00            ???
 0001  E432 8600          LDAA   #00
 0003  C44A E43A          ANDB   3A,X         E43B=8027
-0008--E43D-F984BD--------ADCB---84BD---------E437=BD----
 Func:F     Scroll Rate: 7,8 [20]    Mode: X [Software]
```

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Figure 11. Software disassembly display. Software mode suppresses memory reads and writes. This display corresponds to the hardware disassembly shown in Figure 10. Press DON'T CARE to toggle from software to hardware display mode.

The Data column displays bytes that make up the opcode and also displays any data fetches for the instruction. The Operation column lists the bus operations for the instruction sequence. For each instruction cycle, the analyzer uses the Operation column to tell you the memory address and I/O activity for that cycle. In this column, the address is displayed on the left of the equals sign; data is displayed on the right. Figure 11 shows address and data information.

Searching for Events. You can search for events in the software disassembly display the same as you search for events in the State table. However, because memory reads and writes are suppressed, if you search for an event that occurs on a memory read or write cycle, the analyzer searches instead for the previous opcode fetch displaying that instruction on the screen. To search for a memory read or write, press DON'T CARE to toggle to hardware mode, then select the search event, and then press 1 to search.

When you press DON'T CARE to switch back to software mode, the analyzer goes through memory to find the previous opcode fetch closest to the cursor position. When it finds the opcode fetch, the analyzer displays the disassembly in software mode; the cursor will be in the exact location on the screen as it was on the hardware disassembly. If it can't find an opcode fetch, the analyzer returns to hardware mode.

EXAMPLES

The next three examples show you how to acquire data for disassembly, how to display the data in hardware and software mode, and how to cross-trigger the disassembly probe from a different timebase (using an acquisition probe).

The first example uses the default setup for a simple acquisition. In the second example, you define specific conditions on which you want to trigger. The third example uses 48 channels to cross-trigger the 6800/6802 disassembly probe from the timebase used by an acquisition probe.

Example 1. A Simple Acquisition

This example uses the default 6800/6802 setup that was uploaded when you connected the analyzer to a SUT and initialized the analyzer.

This example shows you how to:

- acquire and disassemble data
- jump to a specific location
- search for a particular event
- toggle between display modes

Follow these steps to make a simple acquisition and begin manipulating data:

1. Make sure the analyzer is connected to your SUT and the analyzer is initialized with the default disassembly setup.
2. Press START to acquire data. The Acquisition Process screen is displayed, telling you the status of the acquisition. When the acquisition is complete, the analyzer stops and displays the data in disassembly format since

that is the default data format. Figure 12 shows the hardware display mode for the disassembly data.

3. Press DON'T CARE to toggle to software display mode. When you switch disassembly modes, the analyzer goes through memory to find the previous opcode fetch closest to the cursor. If it can't find an opcode fetch, it returns to hardware mode.

4. Press ENTER to tell the analyzer you want to enter a new location to be displayed, then enter 0000 to jump to the beginning of memory. As you finish entering the digits, the analyzer jumps to the selected memory address and displays the new information.

5. Press F until the search function is displayed at the bottom of the screen. Press 0 or 2 to cycle through available search functions and choose the trigger for the search event.

6. Press 1 to search for the trigger. Figures 12 shows the trigger event in hardware mode.

The scroll rate, jump, and search features for disassembly displays work the same as they do in the State table. For more information about these features, refer to your logic analyzer's operator manual.

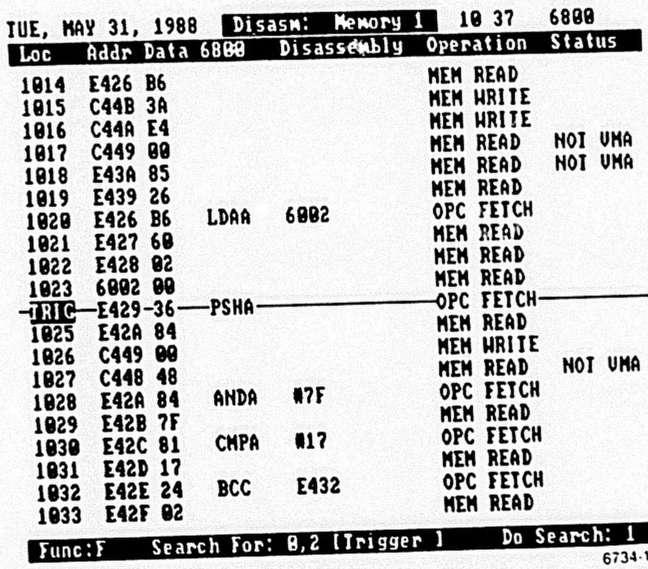


Figure 12. Hardware disassembly display. The search event in this example is the trigger event, which occurred at memory location 1024 as specified in the Run Control menu.

Example 2: Trigger on a Subroutine

This example shows you how to acquire specific data. In this example, a subroutine is located at address 1000. Assume that the subroutine has been incorrectly exiting a loop. You want the subroutine to loop, and you need the logic analyzer to help you determine where the error occurs. You want to acquire the beginning and end of the subroutine to determine why it is not looping. You need to define two conditions: the beginning of the subroutine (address 1000), and the end of the subroutine (address 100B).

This example uses the default setup except for defined conditions and trigger statements. You wouldn't need to change the timebase, channel grouping, or run-control information from the default 32-channel setup for this example. You would follow these steps to trace a subroutine and trigger at its conclusion:

1. Add two new conditions: SUBBEG and SUBEND.
3. Define SUBBEG to have a hexadecimal address of 1000 (the beginning of the subroutine) and SUBEND to have a

hexadecimal address of 100B (the end of the subroutine). Figure 13 shows the new condition words and also shows that the values for the data and control buses of both condition words are don't cares.

4. In the Trigger Spec menu, define two levels of if-then trigger statements as shown in Figure 13.

5. Press START. The analyzer acquires the subroutine, triggering and filling memory when SUBEND occurs. Figures 14 and 15 show the hardware and software disassembly for this example.

6. At address 100B a data value of 39 occurs. This value is an RTS (return from subroutine) command.

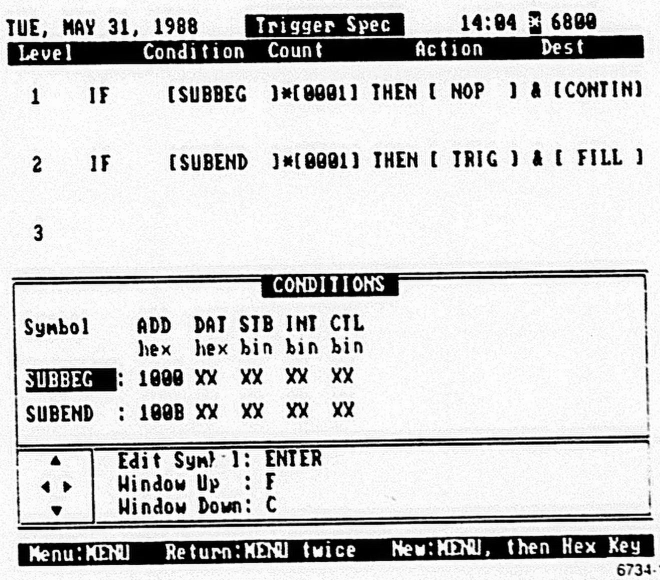


Figure 13. Subroutine setup. The two new conditions define the beginning and end of the subroutine you're tracing. The two levels of trigger statements tell the analyzer to store everything between the beginning and end of the subroutine and to trigger on the end.

TUE, MAY 31, 1988 **Disasm: Memory 1** 14:03 6800

Loc	Addr	Data 6800	Disassembly		Operation	Status
1014	0001	FF			MEM READ	NOT UMA
1015	0000	FF			MEM READ	NOT UMA
1016	1006	26	BNE	1005	OPC FETCH	
1017	1007	FD			MEM READ	
1018	1008	5A			MEM READ	NOT UMA
1019	1005	09			MEM READ	NOT UMA
1020	1008	5A	DECB		OPC FETCH	
1021	1009	26			MEM READ	
1022	1009	26	BNE	1002	OPC FETCH	
1023	100A	F7			MEM READ	
-TRIG-	100B	39			MEM READ	NOT UMA-
1025	1002	CE			MEM READ	NOT UMA
1026	1002	CE	LDX	#D700	OPC FETCH	
1027	1003	D7			MEM READ	
1028	1004	00			MEM READ	
1029	1005	09	DEX		OPC FETCH	
1030	1006	26			MEM READ	
1031	D700	FF			MEM READ	NOT UMA
1032	D6FF	FF			MEM READ	NOT UMA
1033	1006	26	BNE	1005	OPC FETCH	

Func:F Scroll: ↕ Cursor: ◂▸ Jump: ENTER

6734-14

Figure 14. Hardware display. The cursor marks the trigger which occurred at address 100B after the subroutine finished. The hardware display mode shows each memory read and write that occurred during the subroutine.

TUE, MAY 31, 1988 **Disasm: Memory 1** 14 43 6800

Loc	Addr	Data	6800	Disassembly	Operation
0984	1006	26FD	BNE	1005	
0988	1005	09	DEX		
0992	1006	26FD	BNE	1005	
0996	1005	09	DEX		
1000	1006	26FD	BNE	1005	
1004	1005	09	DEX		
1008	1006	26FD	BNE	1005	
1012	1005	09	DEX		
1016	1006	26FD	BNE	1005	
1020	1008	5A	DECB		
-1022-	1009	26F7	BNE	1002	
1026	1002	CED700	LDX	#D700	
1029	1005	09	DEX		
1033	1006	26FD	BNE	1005	
1037	1005	09	DEX		
1041	1006	26FD	BNE	1005	
1045	1005	09	DEX		
1049	1006	26FD	BNE	1005	
1053	1005	09	DEX		
1057	1006	26FD	BNE	1005	

Func:F Scroll Rate: 7,8 [20] Mode: X [Software]

6734-15

Figure 15. Software display. You can enter software mode by pressing DON'T CARE. You can see the subroutine sequence in a more compact form in software mode since only one instruction is displayed for each bus operation.

Example 3: Cross-Triggering

If you're using a 1225 or 1230 Logic Analzyer, you can acquire data on 16-channel acquisition probes at the same time you use the PM407. You can also set the PM407 to trigger off the acquisition probe, or vice versa. This example shows you how to set up the PM407 to trigger off the acquisition probe.

Configuration. This example uses a 1225/1230 with 48 channels. The PM407 is still plugged into probe slots A and B. The 16-channel acquisition probe (P6443 or P6444) is plugged into probe slot C.

What This Example Shows. This example first shows how to set up an acquisition probe to trigger on a condition, then shows how to set up the disassembly probe to automatically cross-trigger and show the acquired information in disassembly display.

In this example, you would want to know what will happen to your code if a particular I/O port receives a write signal from an external device. You would trigger the acquisition probe on a write from an external device to the I/O port. The analyzer then automatically cross-triggers the disassembly probe so that you could display the disassembly data for that acquisition.

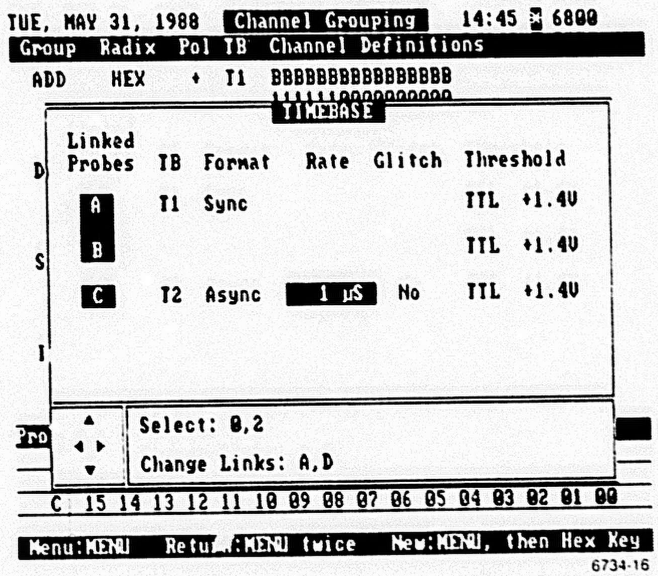
Figures 16 through 19 show the setup menus for this example. The menus show how to set up the 1225/1230 with the following values:

- Probes A and B are in T1; probe C is in T2.
- Channel group GPE is renamed to EXT and contains all 16 channels from probe C.
- The trigger condition EXT I/O is defined for the external write to the I/O port.
- The trigger timebase is T2 (the acquisition probe) so that the 1225/1230 recognizes the trigger condition EXT I/O and automatically cross-triggers the disassembly probe when EXT I/O occurs.

The Steps for Cross-Triggering. You would follow these steps to cross-trigger the 6800/6802 probe off the acquisition probe and search for the trigger event in the resulting disassembly display:

1. In the Timebase menu, link probes A and B in timebase T1 (separately from probe C, which should be in T2). The default setup automatically does this at power-up. Refer to Figure 16.
2. In the Channel Grouping menu, scroll to channel group GPF and change the channel group name to EXT. Insert all 16 data channels from probe C to the channel group. Refer to Figure 17.
3. In the Conditions menu, define a condition EXT I/O to the value of the WRITE signal; in this case, D4F0. Figure 17 shows the Trigger Spec menu and the value of the trigger condition EXT I/O.
4. In the Trigger Spec menu, set the trigger condition to EXT I/O. Figure 18 shows the Trigger Spec menu. In the 1225 the trigger action is START.
5. Look at the menu bar at the bottom of the Trigger Spec menu, and press D to toggle the trigger timebase to T2. Refer to Figure 18.
6. In the Run Control menu, make sure the 1225/1230 looks for the trigger EXT I/O after the pretrigger memory is full. The default data display format should still be set to Disassembly. Refer to Figure 19.
7. Press START. The 1225/1230 acquires data in both timebases, fills memory, and stops. The disassembly screen is displayed. Figure 20 shows a sample disassembly display.
8. Press 0 or 2 to cycle through available search events and select Trigger, then press 1 to locate the trigger. Figure 20 shows the trigger event in a hardware disassembly display.

Since you used two timebases to make the acquisition, you can call up state and timing displays for the acquired data from both timebases. Once you are in the State menu, press E and make sure the radix for the EXT group is set to HEX. Press 9 to toggle to each display to see what happened in T2 on the acquisition probe and T1 on the disassembly probe.



6734-16

Figure 16. Timebase for cross-trigger. Probes A and B (the 6800/6802 disassembly probe) are linked with T1, and probe C (the acquisition probe) is linked with T2. This lets you cross-trigger the disassembly probe on the data acquired in T2.

```
TUE, MAY 31, 1988  Channel Grouping   15 06   6800
Group  Radix  Pol TB  Channel Definitions
 SIB    BIN    +  T1  AA
                      00
                      10

 INT    BIN    +  T1  AA
                      00
                      32

 CTL    BIN    +  T1  AA
                      00
                      54

 EXT    HEX    +  T2  CCCCCCCCCCCCCCCC
                      1111110000000000
                      5432109876543210
Probe               UNUSED CHANNELS
  A|                     07 06
  B|
  C|
Cursor:▲▼ ◀▶   Edit name:ENTER   Default Groups:F
```

6734-17

Figure 17. Channel Grouping for cross-trigger. The channel group shows that the sixth channel group is renamed to EXT and contains all 16 channels for the acquisition probe (timebase T2).

```
TUE, MAY 31, 1988   Trigger Spec    15 24   6800
Level        Condition  Count       Action     Dest

 1   IF     [EXT I/O ]*[0001] THEN [ TRIG ] & [ FILL ]

 2

 3

 4

 5

CONDITION:
          ADD  DAT SIB INT CTL EXT
Symbol    hex  hex bin bin bin hex
EXT I/O :XXXX XX   XX  XX  XX  D4F0

Cur:▲▼◀▶ Sel:0,2 Instr:ENTER TrigTB:D[T2] Advanced:1
```

6734-18

Figure 18. Conditions and Trigger Spec for cross-trigger. The trigger condition EXT I/O is defined as the value of the external WRITE signal to the I/O port. The menu bar at the bottom of the Trigger Spec screen shows that the trigger timebase is T2.

```
TUE, MAY 31, 1988      Run Control       15:25 ▩ 6800

 Update Memory    : [1]      Display: [Disassembly]
 Trigger Position: [1024]    0 [      ·       ] 2K
 Look for Trigger: [After Pre-Trigger Memory Full]
═══════════════════════════════════════════════════
 Compare          : [Manual]
 Compare Memory 1 to Memory: [2]


 Compare Mem Locations: [0000] to [1747]
 Use Channel Mask     : [MEM_READ]
 Display Data at least: [5] seconds

            ADD  DAT STB INT CTL EXT
 Symbol     hex  hex bin bin bin hex
 MEM_READ:  XXXX XX  11  XX  XX  XXXX

 Cursor: ▲▼◄►      Select: 0,2
```

6734-19

Figure 19. Run Control for cross-trigger. The 1225/1230 looks for the trigger after the pretrigger memory is full. When the pretrigger memory is full and contion EXT I/O is found, the analyzer cross-triggers the disassembly probe (A and B) and fills the rest of memory, and displays the acquired data in disassembly format.

```
TUE, MAY 31, 1988   Disasm:  Memory 1    15 26 ▩ 6800
Loc   Addr Data 6800  Disassembly  Operation  Status
1014  E426 B6                      MEM READ
1015  C44B 3A                      MEM WRITE
1016  C44A E4                      MEM WRITE
1017  C449 00                      MEM READ    NOT VMA
1018  E43A 85                      MEM READ    NOT VMA
1019  E439 26                      MEM READ
1020  E426 B6     LDAA     6002    OPC FETCH
1021  E427 60                      MEM READ
1022  E428 02                      MEM READ
1023  6002 00                      MEM READ
TRIG--E429-36-----PSHA-------------OPC FETCH-----------
1025  E42A 84                      MEM READ
1026  C449 00                      MEM WRITE
1027  C448 48                      MEM READ    NOT VMA
1028  E42A 84     ANDA     #7F     OPC FETCH
1029  E42B 7F                      MEM READ
1030  E42C 81     CMPA     #17     OPC FETCH
1031  E42D 17                      MEM READ
1032  E42E 24     BCC      E432    OPC FETCH
1033  E42F 02                      MEM READ
Func:F    Scroll: ⮐    Cursor: ◄►    Jump: ENTER
```

6734-20

Figure 20. Hardware disassembly display. The cursor marks the location of the event on T1 when T2's trigger event EXT I/O occurred.