## TEKTRONIX®

## 550 MHz COUNTER

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\text { DC } 502
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## INTRODUCTION

## Description

The DC 502550 MHz Frequency Counter measures frequencies from 10 Hz to 550 MHz or totalizes events to $10^{7}$ at a maximum rate of 550 MHz . The DC 502 operates in a TEKTRONIX TM 500 Power Module only.

Frequency measurements are accomplished using one of two BNC inputs on the front panel. The DIRECT INPUT has a frequency range of 10 Hz to 110 MHz with a 300 mV peak-to-peak sensitivity, selectable attenuators, and an adjustable trigger level range. The $\div 10$ PRE-SCALE INPUT has a frequency range of 50 MHz to 550 MHz with a 500 mV peak-to-peak sensitivity and a $50 \Omega$ input impedance. The same four measurement interval times are selectable for each input.

Front panel controls reset the Counter and provide Start/Stop commands for the manual totalizing mode of each input.

Measurement display is accomplished with seven-segment LED's in a 7 -digit readout. The decimal point is automatically positioned by the MEASUREMENT INTERVAL selected, and leading zeros (to the left of the most significant digit or the decimal point) are blanked. LED's indicate when the GATE is open, when the kHz or MHz units are displayed, and when OVERFLOW occurs.

## Installation

The DC 502 is calibrated and ready to use as received. Referring to Fig. 1-1, install the DC 502 into the Power Module and turn on the power.


Fig. 1-1. Plug-in module installation/removal.

## OPERATIONAL CHECK

## Display Check

Press the RESET button to check the 7 character segments of each digit; the numerical display should be a row of eights. To check the decimal point position and the units indicators, set the MEASUREMENT INTERVAL switch as follows:

| Switch Position |  | Numerical Display | Units |
| :---: | :---: | :---: | :---: |
| . 01 SEC |  | . 0000 | MHz |
| . 1 SEC |  | . 00000 | MHz |
| 1 SEC | DIRECT | . 000 | kHz |
| 10 SEC |  | . 0000 | kHz |
| MANUAL |  | 000 |  |
| MANUAL |  | 000 |  |
| 10 SEC |  | . 000 | kHz |
| 1 SEC | PRE- | . 00000 | MHz |
| . 1 SEC | SCALE | . 0000 | MHz |
| . 01 SEC | INPUT | . 000 | MHz |

In the MANUAL position, no decimal point will be displayed. Press the START button and check that the GATE indicator lights, then release the button (STOP) and check that the GATE light goes out. To check the OVERFLOW indicator, set the MEASUREMENT INTERVAL switch to 10 s and apply 15 or $20-\mathrm{MHz}$ to the INPUT connector. The length of time a display can be held is determined by the DISPLAY TIME control, and will be discussed in the next few paragraphs.

## Frequency Measurements

Direct Input. The DC 502 provides direct measurement of the average frequency of signals from about 10 Hz to 110 MHz . The input sensitivity is 300 mV peak-to-peak, so select the proper attenuation ( $\mathrm{X} 1, \mathrm{X} 5, \mathrm{X} 10$, or X 50 ) for the given signal.


The input signal must not exceed 500 volts.

Apply a signal to the INPUT connector. Set the MEASUREMENT INTERVAL switch to the .01 SEC position and the DISPLAY TIME control fully CCW. Observe the numerical readout display. Adjust the TRIGGER LEVEL control for a stable reading. The zeroes leading the most significant digit in the display should be blanked.

Then turn the MEASUREMENT INTERVAL switch to the position that gives the desired reading. Generally, use the shorter measurement intervals for high-frequency, lowresolution measurements and the longer intervals for measurements requiring a high resolution.

NOTE
The OVERFLOW indicator can be lit for highresolution measurements, allowing the frequency to be indicated to 0.1 Hz . Refer to the Specifications at the end of this section for resolution and accuracy at each position of the MEASUREMENT INTERVAL switch.

The display is updated at a rate determined by the DISPLAY TIME control. Each time a sample of the input signal is taken, the GATE light will flash and the new reading will be displayed. To change the display time, which is continuously variable from about 0.1 second to 10 seconds, or to hold a display indefinitely, turn the DISPLAY TIME control.
$\div 10$ Pre-Scale Input. The DC 502 also provides a prescaled, $A C$-coupled input to measure the average frequency of signals from 50 MHz to 550 MHz . This input has a sensitivity of 500 mV , peak-to-peak, and a maximum input voltage limit of 10 V , peak-to-peak. Signals greater than 10 V may damage the diodes of the input circuit. The ATTEN controls do not apply to this input.

Apply a 50 MHz to 550 MHz signal of at least 500 mV amplitude to the $\div 10$ PRE-SCALE INPUT. Set the MEASUREMENT INTERVAL switch to .01 SEC and observe the readout. Leading zeros should be blanked. Select a MEASUREMENT INTERVAL which gives the best accuracy and resolution. As with the DIRECT INPUT, shorter measurement intervals give higher frequency, lower resolution measurements; longer intervals offer greater resolution, especially when overflow is employed.

## Totalizing

DIRECT INPUT. The DC 502 will count and display the accumulated number of signals (events) applied to the DIRECT INPUT connector up to the register capacity of 9,999,999 during the time interval between START/STOP commands from the front-panel pushbutton. Input signal rate should not exceed 110 MHz .

Set the MEASUREMENT INTERVAL switch to MANUAL, apply the signal, and push the START button. The GATE indicator will light and the progressing count will be displayed. Adjust the ATTEN and TRIGGER LEVEL controls as necessary for a steady count. To stop the counting, release the START button. The GATE light will go out and the displayed count will be held. The displayed count can continue when the START button is depressed again. The counter can be cleared to zero at any
time by pressing the RESET button or by moving the MEASUREMENT INTERVAL switch to another position.
$\div 10$ PRE-SCALE INPUT. In the MANUAL mode related to this input, the displayed count advances one count for every ten incoming events. The incoming events must have transition times and periods suitable for the $50 \Omega$ pre-scale input triggering requirements.

## USING THE COUNTER

## DIRECT INPUT Attenuation and Trigger Level Adjustment

Signals to be counted in the DIRECT INPUT channel may have a wide variety of shapes and amplitudes, many of which are unsuitable to drive the counting circuits. Because of this, the signal is first passed through an attenuator, then applied to a signal-shaping circuit which converts it to rectangular pulses of uniform amplitude. This circuit includes a reference level adjustable between + and -2 volts to which the incoming signal is compared, allowing the 300 -millivolt sensitivity window of the signal-shaping circuit to be adjusted to a convenient amplitude on the incoming waveform (see Fig. 1-2). Obtaining a steady, reliable reading is dependent upon the proper selection of input attenuation and proper adjustment of the TRIGGER LEVEL control.


Fig. 1-2. Two examples of triggering circuit output showing how proper adjustment of TRIGGER LEVEL control can avoid an erroneous count.

Generally, the best point on a waveform for triggering the counter is where the slope is steep and therefore usually free of noise. On a sine-wave signal, for example, the steepest slope occurs at the zero-crossing point. Noise pulses or other signal components of sufficient amplitude to produce unwanted trigger pulses will cause an erratic or incorrect count. Fig. 1-2 shows the TRIGGER LEVEL control adjusted to avoid error. In critical measurement applications, monitor the incoming signal with a test oscilloscope.

## Signal Connection

Coaxial cables and probes offer very convenient means of connecting the signals to the front-panel input BNC connectors. These devices are shielded to prevent pickup of electrostatic interference which can cause erroneous triggering and a faulty count. For the DIRECT INPUT, a $\times 10$ probe not only reduces the size of the signal, but also presents a high input impedance to allow the circuit under test to perform very close to normal operating conditions. For the $\div 10$ PRE-SCALE INPUT, the $50 \Omega$ input requires careful impedance matching. If the signal must be attenuated to avoid exceeding the maximum input limit of 10 V , use $50 \Omega$ attenuator pads terminated by the $50 \Omega$ input impedance of the DC 502.

## Measurement Interval and Display Time Controls

The MEASUREMENT INTERVAL switch selects the time interval (also called gate time) during which the DC 502 counts. The internal time-base circuit derives gate times from an accurate $1-\mathrm{MHz}$ reference signal to make frequency measurements. These gate times are $0.01 \mathrm{~s}, 0.1 \mathrm{~s}$, 1 s , or 10 s . The measurement interval selected determines the measurement range and resolution. Also, the displayed decimal point is positioned correctly and the correct measurement units ( MHz or kHz ) are indicated for the corresponding switch position.

The DISPLAY TIME control sets the length of time a measurement can be held in the counter and displayed. The HOLD detent position allows a measurement to be held indefinitely, or until the counter is reset to zero by the front-panel RESET button.


Fig. 1.3. Input/Output pin assignments at rear connector.

## Rear Connector I/O Assignments

Input and output data access to the DC 502 is available at the rear of the main circuit board. Fig. 1-3 identifies the contacts and their respective $1 / O$ assignments. A Power Module mainframe option is available which provides a rear-panel, multi-pin connector to which these data can be hard-wired for external access. Also possible are intracompartment connections with other plug-in modules when using a multi-compartment Power Module.

## Option 1-Precision Time Base

The DC 502 can be ordered with a temperaturecompensated $5-\mathrm{MHz}$ crystal oscillator to provide a highly stable ( 5 parts in $10^{7}$ ) and precise internal time base. This option includes a divide-by-five IC counter to produce the 1- MHz clock.

## SPECIFICATIONS

## Measurement Ranges, Resolution, and Accuracy

Frequency, 10 Hz to 550 MHz ; Gate times, $0.01 \mathrm{~s}, 0.1 \mathrm{~s}$, 1 s , and 10 s ; Display time, about 0.1 s to 10 s to HOLD; Totalizing capacity, 0 to $10^{7}$; Resolution (DIRECT INPUT), 100 Hz at 0.01 s gate time, 10 Hz at $0.1 \mathrm{~s}, 1 \mathrm{~Hz}$ at 1 s , and 0.1 Hz at 10 s ; Resolution $(\div \mathbf{1 0}$ PRE-SCALE INPUT), 1000 Hz at $0.01 \mathrm{~s}, 100 \mathrm{~Hz}$ at $0.1 \mathrm{~s}, 10 \mathrm{~Hz}$ at 1 s , and 1 Hz at 10 s ; Accuracy, $\pm 1$ count $\pm$ time base accuracy.

## Direct Input

Frequency, 10 Hz to 110 MHz ; Sensitivity, 300 mV peak-to-peak; Trigger level range, $\pm 2 \mathrm{~V}$; Attenuators, X 1 , $X 5, X 10$, and $X 50$; Coupling, $A C$; Input impedance, approximately $1 \mathrm{M} \Omega$ paralleled by about 20 pF ; Maximum input volts, 500 V ( $\mathrm{DC}+$ peak $A C$, or peak-to-peak $A C$ ).

## $\div 10$ Pre-Scale Input

Frequency, 50 MHz to 550 MHz ; Sensitivity, 500 mV peak to peak; Coupling, AC; Input impedance, approximately $50 \Omega$; Maximum input volts, 10 V peak-to-peak.

## Data Inputs and Outputs

Available via plug-in connector to multi-pin connector at rear of Power Module. Input lines are available for internal and external scan clock control. Output lines are available for BCD output (serial-by-digit), and to indicate status of timing, data good, reset, scale, decimal point and overflow.

## Internal Time Base

|  | Standard | Option 1 |
| :--- | :--- | :--- |
| Crystal Frequency | 1 MHz | 5 MHz |
| Stability $\left(0^{\circ} \mathrm{C}\right.$ to <br> $\left.+50^{\circ} \mathrm{C}\right)$, after $1 / 2$ <br> hour warm-up | Within 1 part in <br> $10^{5}$ | Within 5 parts in <br> $10^{7}$ |
| Long-term Drift | 1 part or less in <br> $10^{5}$ per month | 1 part in <br> $10^{7}$ per month |
| Accuracy | Adjustable to <br> within 1 part in <br> $10^{7}$ | Adjustable to <br> within 5 parts in <br> $10^{9}$ |

## Other

Temperature Range, Operating: $0^{\circ} \mathrm{C}$ to $+50^{\circ} \mathrm{C}$; Nonoperating: $-40^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$.

Altitude Range, Operating: to 15,000 feet; Nonoperating: 50,000 feet.

## SECTION 2 THEORY OF OPERATION

## INPUT CIRCUITS

## Direct Input

Attenuators. Signals to be counted are applied via front-panel DIRECT INPUT connector J100 to the attenuators. The attenuators are frequency-compensated voltage dividers consisting of resistors R102-R107 and capacitors C102-C107. Switches S100A and S100B allow front-panel selection of X1, X5, X10, or X50 attenuation of the input signal. C110 provides AC coupling.

FET source follower Q115 and emitter follower Q122 present a high impedance to the input signal. The diodes in the base circuit of E. F. Q128 form a series-limiter and clamping network, which reduces the input signal to limits suitable for driving the shaping circuits. The clamping diodes limit the voltage at the emitter of 0128 to a dynamic range of about 1.2 volts.

Signal-Shaping. U150B, an OR gate integrated circuit with push-pull outputs, is connected as a Schmitt trigger. It shapes the input signal into a square wave. Its "hysteresis window" is a width of about 200 mV . The output changes states when the signal voltage passes through the upper threshold, then reverts to its original state when the signal voltage passes through the lower threshold. For this reason, an input signal smaller in amplitude than the width of the hysteresis window cannot activate the counting circuits.

The quiescent level at the input of U150B can be adjusted to overcome some of the triggering difficulties arising from various input-signal shapes and frequencies. Integrated-circuit operational amplifier U135 and its associated discrete components are connected as a voltage follower. TRIGGER LEVEL potentiometer R135 selects a voltage between ground and about -2 volts and applies it to pin 3 of U135. This level is then established at pin 2, and hence, the input of U150B, through the action of the operational amplifier.

The output of U150B is applied to U150A, whose push-pull outputs drive Q160 and Q162, which are connected as a differential pair. This circuit provides a level shift to TTL level, and further shapes the signal to be counted. A waveform with fast rising and falling edges is produced at the collector of Q160. CR165 limits the amplitude of the count signal to 5 volts, clamping the negative-going portion of the signal to ground. The signal is then passed through emitter follower O170 to U160B, where it receives a final
phase inversion (to correspond with the input signal) and becomes the decade input.

## $\div \mathbf{1 0}$ Pre-Scale Input Circuit

50 MHz to 550 MHz signals applied to J 180 are AC-coupled into a $50 \Omega$ environment. A quiescent 10 mA current, set by R185 and R187, keeps CR185, 186, 187 and 188 in the diode clamping bridge turned on until the input signal amplitude reaches about $\pm 0.4 \mathrm{~V}$. While the bridge is turned on, the signal source sees about $20 \Omega$ equivalent resistance of the bridge in series with R189, $24 \Omega$, and the emitter resistance of $Q 190$, about $5 \Omega$. As the signal amplitude exceeds $\pm 0.4 \mathrm{~V}$, one pair of diodes (CR185, CR188) begins to turn off during positive-going excursions, while the other pair (CR186, CR187) turns off during negative-going excursions. As these diode pairs alternately turn off with signal amplitude changes, a matched pair of diodes (CR181A, CR181B) on the input side of the coupling capacitor, C182, alternately turn on to maintain the $50 \Omega$ input impedance. C181 prevents CR181A \& CR181B from being biased on or off by DC levels which may be part of the input signal.

The clamping action of the bridge diodes limits the changing DC level at the bridge output to a maximum 0.8 V peak-to-peak. This signal is then coupled by C188 to $\mathbf{Q 1 9 0}$ via the high-frequency peaking network, C189-R189. C192 couples the amplified signal to pin 10 , the high impedance input of the $\div 10$ counter, U190. C192 is mounted on the circuit board with special lead dress to aid high frequency response at minimum signal amplitudes. Bead L192 is mounted on one lead of C192 to suppress high frequency oscillations. R191 establishes a bias at pin 10 of U190. C191, 193, and 194 decouple pins 14, 13, and 12, respectively, right at the terminal connections to the circuit board. L199 and C199 suppress power supply noise and decouple the Vcc input, pin 14.

Pin 4 of U190 produces one output cycle, a level change of about 0.5 V , for every ten input events to pin 10 . The base of 0195 swings approximately between 3.4 V and 3.9 V . The emitter-follower action of Q195 provides a healthy current drive to the base of Q198, which would saturate in no-signal conditions except for CR196. The collector of Q 198 can, therefore, respond immediately to signal changes, producing a TTL-compatible output to drive pin 9 of U160B in the gating logic to the Decade Counting Units.

# TIME BASE AND CONTROL CIRCUIT 

## 1 MHz Clock

A precise one megahertz clock provides the reference for operation of the gate-generating circuits. The output of crystal oscillator Y200 is adjustable by C201 to exactly one megahertz. The four parts of U200 form a shaper-buffer stage to produce square-wave clock pulses and to isolate the oscillator from the $1-\mathrm{MHz}$ output line.

## Optional Clock

An optional 1 MHz clock is available, using a very stable 5 MHz crystal oscillator and a divide-by-five counter. This combination is shown on the schematic as Y201 and U201.

## Decade Divider Units (DDU's)

The DDU's consist of seven cascaded divided-by-ten counters, U209 through U215. They produce four gate times, $0.01 \mathrm{sec}, 0.1 \mathrm{sec}, 1 \mathrm{sec}$ and 10 sec , which are made available via the MEASUREMENT INTERVAL switch to the gate generator to establish the precise time interval the GATE is open. The 1-MHz clock signal is applied to pin 14 of U209, whose output is connected to the input of the
subsequent decade. Each decade is clocked with a negativegoing transition. The DDU's are reset by a CLEAR pulse, which places a 0 count in U209 and a 9 count in each subsequent decade.

## Gate Generator

The gate generator produces the GATE control signal and initiates the CLEAR, $\overline{C L E A R}$, and LATCH pulses. The generating portion consists of U220A, U222A, U220B, and U222B. The display time control portion consists of Q230, Q238, and 0240. The circuit will be described first in the normal gate mode (MEASUREMENT INTERVAL switch in one of the four gate time positions).

Assume that the $T_{0}$ conditions are as given in Fig. 2-1. The $Q$ outputs of U220A, U222A, U220B, and U222B are all LO. Q230 is off and the emitter of Q238 rises as C235 charges. At $\mathrm{T}_{1}, \mathrm{Q} 238$ reaches its firing potential and discharges the capacitor. This results in a short-duration LO pulse on the direct-set input (pin 2) of U220A, forcing its Q output HI and its $\overline{\mathrm{Q}}$ output LO. With two HI inputs on NAND gate U230A, its output goes LO and the output of


Fig. 2-1. Time Base generator normal gating mode ladder diagram.

NOR gate U230C goes HI, producing the CLEAR and CLEAR control signals. The next HI -to-LO transition from the $1-\mathrm{MHz}$ clock $\left(T_{2}\right)$ toggles U222A, causing its $Q$ output to go HI and its $\overline{\mathrm{O}}$ to go LO. With a LO applied to one of its inputs, U230A reverts to its original condition, terminating the CLEAR and CLEAR pulses. The DDU's then start counting from their 0999999 reset condition.

At the end of a 10 -microsecond delay (time for the DDU's to count the first digit, plus a propagation delay), a negative transition from the DDU's via the MEASUREMENT INTERVAL switch toggles U220B. This corresponds to $\mathrm{T}_{3}$ in Fig. 2-1. U220B's O output goes HI and its $\overline{\mathrm{Q}}$ output goes LO. The next negative transition from the $1-\mathrm{MHz}$ clock $\left(\mathrm{T}_{4}\right)$ toggles U 222 B , causing its Q output to go HI (GATE open) and its $\overline{\mathrm{Q}}$ output to go LO (supplying current to the front-panel GATE indicator LED, DS225). The GATE signal is also applied to the base of $\mathbf{Q} 230$, saturating the transistor and preventing C235 from charging.

The GATE remains open (HI) for the time duration selected by the MEASUREMENT INTERVAL switch. At the end of this time, which corresponds to $\mathrm{T}_{5}$ in Fig. 2-1, another negative transition from the DDU's toggles U220B. U220B's Q output goes LO and its $\overline{\mathrm{O}}$ output goes HI . The next negative transition from the $1-\mathrm{MHz}$ clock $\left(T_{6}\right)$ toggles U222B, causing its $Q$ output to go LO, closing the GATE. Simultaneously, the $\overline{\mathrm{Q}}$ output goes HI , removing current from the GATE indicator LED.

When the GATE output goes LO, the negative transition toggles U220A, switching Q LO and $\overline{\mathrm{Q}} \mathrm{HI}$. Now NAND gate U230D has two HI inputs, placing a LO at the input of OR gate U230B and activating the LATCH control signal (HI
state). One microsecond later ( $T_{7}$ ), a negative edge from the $1-\mathrm{MHz}$ clock toggles U222A, switching its outputs and placing a LO on the input of NAND gate U230D. U230D reverts to its original condition, terminating the LATCH signal.

The display time begins when the GATE signal ends ( $\mathrm{T}_{6}$ ). When 0230 turns off, C235 begins to charge through R232-R235 toward the Vcc supply. R235, DISPLAY TIME, provides an adjustable time constant to vary the display time from about 0.1 second to about 10 seconds. When the DISPLAY TIME control is fully clockwise (HOLD detent position), S235 opens, and C235 stops charging. When S 235 is closed and C 235 charges sufficiently to bring Q238 to its firing potential ( $T_{1}$ ), the display time ends and the next GATE-opening sequence begins.

## Manual Gate

The manual mode of operation is selected by placing the MEASUREMENT INTERVAL switch in the MANUAL position. The switch closure to ground (cam 5 of the switch) places a LO on the set inputs of U220B and U222A, and a LO on the clear input of U220A. This forces the Q outputs of U222A and U220B HI, and the Q output of U220A LO. With both inputs of U230D held HI, the LATCH output is held HI, allowing the counter to update the display continuously. The GATE is opened when the front-panel START button is pushed in, opening S210 and applying a HI to the clear input of U222B. As before, the GATE-open condition is HI at the Q output of U222B. The GATE is then closed when S210 is set to STOP (button out). To reset the counters in the manual mode, the RESET button must be pushed to activate to CLEAR, $\overline{\operatorname{CLEAR}}$ and RESET control signals.

## COUNTER CIRCUITS

## Decade Counter Units (DCU's)

The $10^{0}$ through $10^{6}$ DCU's are seven cascaded divide-by-ten counters. The first decade counter is made up of four individual J-K flip-flops to accept the high-speed decade input (up to 100 MHz ), and each subsequent DCU is a single IC. U165A, U165B, U167, and U169 comprise the first $\left(10^{\circ}\right)$ decade counter, and U235 through U240 make up the remaining six DCU's.

When the $J$ and $K$ inputs of U165B are HI (GATE open), the counter is enabled. The input signal is applied to the toggle input of U165B. On every tenth clock input counted by the first decade counter, the output of U169 goes LO, providing a carry signal which becomes the clock input for the second decade counter. Each subsequent decade divides
by ten in a similar manner. Four BCD output lines are connected from each DCU to its associated storage-register latch. When the CLEAR (HI) and CLEAR (LO) signals are activated, all of the decade counters are reset to the zero-count state.

## Storage Register

The seven IC latches (U250 through U256) comprise a storage register which stores the corresponding decade counter BCD output. The BCD output is applied to the data inputs at pins $1,5,7$, and $3\left(2^{0}, 2^{1}, 2^{2}\right.$, and $2^{3}$ bits respectively). The LATCH pulse is applied to the datastrobe input at pin 2 of each latch immediately upon closure of the GATE or when the MEASUREMENT INTERVAL switch is placed in the MANUAL position, as
described in the time base and control circuit. When the LATCH input goes HI , the logic levels at the data inputs are transferred to the associated BCD bit output to be scanned by the multiplexing circuit.

## Overflow Register

When the decade counters have counted to $9,999,999$, the counters are full. At the next count, the $2^{3}$ output of U240 goes LO, providing a toggle input to U241B. When this occurs, a LO is transferred from pin 10 to pin 8 of U241B, then when the LATCH pulse ends (goes LO), U241A is toggled and the LO is transferred to pin 13. When pin 13 of U241A goes LO, CR241 and DS242 conduct.

DS242 is an LED, and in its conduction state gives a front-panel OVERFLOW indication.

In the Manual counting mode, OVERFLOW indication is achieved via O 242 and CR244. The emitter of O242 is grounded by a switch closure, then when pin 9 of U241B goes HI on the first overflow count, Q242, CR244, and DS242 turn on.

U241 is reset by the $\overline{\text { CLEAR }}$ pulse. To prevent leadingzero suppression during the overflow condition, the displaycontrolling circuits are notified via U245A that the count is in excess of that displayed by the LED readout.

# DECODE AND DISPLAY MULTIPLEX 

## Scan Clock

The scan rate of the multiplexing circuit is determined by the scan clock. The scan clock is composed of U260B and U260D, which operate as a free-running multivibrator at an approximate 2 -kilohertz rate. The scan-clock output is passed through NOR gate U260A, which can also accept an externally applied scan-clock signal. Other input/output lines provide internal scan-clock disable and internal scanclock output. The scan clock drives an eight-state counter and a storage register for zero suppression.

## $\div 8$ Counter and Time-Slot Decoder

The divide-by-eight counter is made up of U262B, U263A, and U262A, which are three halves of SN7474 type D flip-flops. The output of this counter drives U265, an SN74145 BCD-to-decimal decoder. U265 provides eight output lines (designated $\mathrm{TS}_{0}$ through $\mathrm{TS}_{7}$ in the schematics and in Fig. 2-2) to simultaneously enable the output of each counter latch and its corresponding display LED sequentially. For example, when the $\mathrm{TS}_{1}$ line goes LO, Q280 is turned on to supply anode voltage to DS280 at the same time inverter U267C applies a HI to pin 6 of latch U256, enabling its output. Operation in a time sequence allows the latches to share a common set of output lines.

## Seven-Segment Decoder and Display LED's

U 270 is a BCD-to-seven decoder. It accepts the BCD output of the latches, then supplies current to the appropriate cathodes of the enabled LED to display the correct number. The display LED's are DS280 through DS286. When looking at the front panel of the DC 502, DS280 controls the numerical digit displayed at the far left $\left(10^{6}\right)$, DS281 controls the second ( $10^{5}$ ), etc. Each LED has seven segments, arranged so that a combination of lighted segments forms a number. When all of the segments are lighted, an " 8 " is formed.

## Leading Zero Suppression

Decoder driver U270 also has a zero-blanking feature which allows suppression of the zeroes leading the most significant digit (MSD) in the display. At $\mathrm{TS}_{0}$, a LO is applied to the direct-clear input of U263B, the zerosuppression storage register. This sets U263B to the zero-suppress state ( HI at pin 8), allowing the RippleBlanking Input (RBI, pin 5) of U270 to be LO. When the output of U265 advances to the next time slot $\left(\mathrm{TS}_{1}\right)$, the RBI of U270 remains LO for a few nanoseconds due to propagation delays, which allows the first digit to arrive from the latches while RBI is LO. If this first digit being decoded is a zero, the output to the display LED will be inhibited and the Ripple Blanking Output (pin 4) will be LO. If the digit is not a zero, the outputs are enabled and RBO goes HI. The . RBO is applied to the D input (pin 12) of U263B and is transferred to the output when the next scan-clock HI-to-LO transition occurs. Thus, if the first digit is a zero, pin 5 of U270 is held LO, inhibiting the output until the first non-zero digit comes through the decoder. When the first non-zero digit arrives, the outputs of U270 are enabled and the digit is displayed. Also, the RBO output at pin 4 is set HI , removing the RBI from pin 5 and allowing all succeeding digits to be displayed through the $\mathrm{TS}_{7}$ sequence.

When the scan gets past the decimal point in the display, or if the display overflows, any zeroes arriving at the decoder should be displayed. This is achieved as follows: $\mathrm{TS}_{5}$ is inverted by U267E and applied through OR gate U245B as a LO at the direct-set input of U263B. This holds pin 5 of U 270 HI , preventing zero-blanking during the $\mathrm{TS}_{5}$, $\mathrm{TS}_{6}$, and $\mathrm{TS}_{7}$ time slots. The location of the decimal point in the display is determined by the MEASUREMENT INTERVAL switch. The proper information is applied via the closed contacts of the switch to either NAND gate U 246 A or U 246 B . Then either $\mathrm{TS}_{3}$ or $\mathrm{TS}_{4}$ is enabled to the


Fig. 2-2. Multiplexing circuit ladder diagram showing timing with an all-zero display.
input of OR gate U245B via these NAND gates, setting U263B to the non-blank state at the appropriate time. In the case where the counter overflows, the HI output from U245A is applied to U245B, setting U263B to the non-blank state.

## POWER SUPPLIES AND INPUT/OUTPUT LINES

## Regulated Power Supplies

The DC 502 operating power is obtained from the power module mainframe and then electronically regulated to provide stable supplies of +15 volts, +5 volts, -5.2 volts, and -10 volts. The +15 -volt supply, whose active device is U300, provides the reference for the remaining supplies. Its output is set to +15 V by adjustment of R305.

Integrated circuit U320 regulates the +5 -volt supply, and transistors Q330 and Q340 regulate the -5.2 -volt and -10 -volt supplies respectively. The series-pass transistors for these supplies are located in the mainframe, where they can provide the proper heat dissipation.

## Input/Output Lines

The following inputs and outputs are available via the plug-in connector to external equipment. See Fig. 1-3, also.

When the front-panel RESET button is pushed, $\overline{\text { RESET }}$ goes LO, overriding the output of U263B, applying the non-blank and lamp-test functions to the decoder. This causes all seven segments in the display LED to be turned on.

OVERFLOW: This output is HI when the count overflows.

RESET: This is a dual-function input/output line. It provides a LO output during reset, or can be used as an external reset input.

Data Lines: $\overline{1}, \overline{2}, \overline{4}, \overline{8}$ provide BCD output, serial by digit, from the currently enabled storage-register latch. Other data lines include a LO when the MHz light is on, a LO when the second decimal point is lit, and a HI when the left-side digit (MSD) is enabled.

## DIAGRAMS, PARTS LISTS, AND ILLUSTRATIONS

## Symbols and Reference Designators

Electrical components shown on the diagrams are in the following units unless noted otherwise:

$$
\begin{array}{ll}
\text { Capacitors }= & \text { Values one or greater are in picofarads }(\mathrm{pF}) . \\
\text { Values less than one are in microfarad }(\mu \mathrm{F}) . \\
\text { Resistors }= & \text { Ohms }(\Omega)
\end{array}
$$

Symbols used on the diagrams are based on ANSI Y32.2-1970.
Logic symbology is based on MIL-STD-806B in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The following special symbols are used on the diagrams:

$\longrightarrow$

(7)


Refer to waveform number indicated in hexagon.

Connection soldered to circuit board.

Connection made to circuit board with interconnecting pin.

Blue tint encloses components located on circuit board.

PO circuit board

## ELECTRICAL PARTS LIST

Replacement parts should be ordered from the Tektronix Field Office or Representative in your area. Changes to Tektronix products give you the benefit of improved circuits and components. Please include the instrument type number and serial number with each order for parts or service.

## ABBREVIATIONS AND REFERENCE DESIGNATORS

| A | Assembly, separable or <br> repairable |
| :--- | :--- |
| AT | Attenuator, fixed or variable |
| B | Motor |
| BT | Battery |
| C | Capacitor, fixed or variable |
| Cer | Ceramic |
| CR | Diode, signal or rectifier |
| CRT | cathode-ray tube |
| DL | Delay line |
| DS | Indicating device (lamp) |
| Elect. | Electrolytic |
| EMC | electrolytic, metal cased |
| EMT | electrolytic, metal tubular |
| F | Fuse |


| FL | Filter |
| :--- | :--- |
| H | Heat dissipating device |
|  | (heat sink, etc.) |
| HR | Heater |
| J | Connector, stationary portion |
| K | Relay |
| L | Inductor, fixed or variable |
| LR | Inductor/resistor combination |
| M | Meter |
| Q | Transistor or silicon- |
|  | controlled rectifier |
| P | Connector, movable portion |
| PMC | Paper, metal cased |
| PT | paper, tubular |


| PTM | paper or plastic, tubular molded |
| :---: | :---: |
| R | Resistor, fixed or variable |
| RT | Thermistor |
| S | Switch |
| T | Transformer |
| TP | Test point |
| U | Assembly, inseparable or non-repairable |
| V | Electron tube |
| Var | Variable |
| VR | Voltage regulator (zener diode, etc.) |
| WW | wire-wound |
| $Y$ | Crystal |


| Ckt. No. |  | Tektronix Part No. | $\begin{aligned} & \text { Serial/M } \\ & \text { Eff } \end{aligned}$ | odel No. Disc | Description |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ASSEMBLIES |  |  |  |  |  |
| A1 ${ }^{1}$ |  | 670-2102-00 | B010100 | B039999 | MAIN Circuit Board Assembly |
| $\mathrm{Al}^{1}$ |  | 670-3409-00 | B040000 |  | MAIN Circuit Board Assembly |
| A1 ${ }^{2}$ |  | 670-3410-00 |  |  | MAIN Circuit Board Assembly |
| A2 |  | 670-2103-00 |  |  | DISPLAY Circuit Board Assembly |
| A3 |  | 670-2438-00 |  |  | $\div 10$ PRE-SCALER Circuit Board Assembly |
| A4 |  | 670-2708-00 |  |  | Protection Circuit Board Assembly |
| A5 |  | 670-3300-00 | XB040000 |  | $\div 5$ Circuit Board Assembly |
| CAPACITORS |  |  |  |  |  |
| C102 | M5 | 281-0510-00 |  |  | 22 pF, Cer, $500 \mathrm{~V}, 20 \%$ |
| C103 | M4 | 281-0605-00 |  |  | 200 pF , Cer, 500 V |
| C106 | L4 | 281-0509-00 |  |  | 15 pF, Cer, $500 \mathrm{~V}, 10 \%$ |
| ${ }^{C 107} 1$ | L5 | 281-0540-00 |  |  | $51 \mathrm{pF}, \mathrm{Cer}, 500 \mathrm{~V}, 5 \%$ |
| ${ }^{\text {C11 }} 101$ | L5 | 283-0068-00 | B010100 | B050499 | $0.01 \mu \mathrm{~F}$, Cer, $500 \mathrm{~V},+100 \%-0 \%$ |
| ${ }_{C 110}{ }^{2}$ | L5 | 283-0267-00 | B050500 |  | $0.01 \mu \mathrm{~F}, \mathrm{Cer}, 500 \mathrm{~V}, 20 \%$ |
| $\mathrm{Cl110}^{\text {C11 }}$ | L5 | 283-0068-00 | B010100 | B040502 | $0.01 \mu \mathrm{~F}, \mathrm{Cer}, 500 \mathrm{~V},+100 \%-0 \%$ |
| ${ }_{\text {Cl112 }}$ | L5 | 283-0267-00 | B040503 |  | 0.01 $10 \mathrm{~F}, \mathrm{Cer}, 500 \mathrm{~V}, 20 \%$ |
| C113 | L6 | 283-0003-00 |  |  | $0.01 \mu \mathrm{~F}$, Cer, 150 V , $+80 \%-20 \%$ |
| C122 | K5 | 283-0000-00 |  |  | $0.001 \mu \mathrm{~F}$, Cer, $500 \mathrm{~V},+100 \%-0 \%$ |
| C127 | K5 | 283-0000-00 |  |  | $0.001 \mu \mathrm{~F}$, Cer, $500 \mathrm{~V},+100 \%-0 \%$ |
| C139 | M5 | 283-0003-00 |  |  | $0.01 \mu \mathrm{~F}, \mathrm{Cer}, 150 \mathrm{~V},+80 \%-20 \%$ |
| C140 | L5 | 283-0177-00 |  |  | $1 \mu \mathrm{~F}$, Cer, $25 \mathrm{~V},+80 \%-20 \%$ |
| C141 | M5 | 283-0000-00 |  |  | $0.001 \mu \mathrm{~F}$, Cer, $500 \mathrm{~V},+100 \%-0 \%$ |
| C152 | J5 | 281-0589-00 |  |  | 170 pF, Cer, $500 \mathrm{~V}, 5 \%$ |
| C181 | R2 | 283-0219-00 |  |  | 1500 pF , Cer, $50 \mathrm{~V}, 20 \%$ |
| C182 | R3 | 283-0219-00 |  |  | 1500 pF , Cer, $50 \mathrm{~V}, 20 \%$ |
| C184 | R2 | 283-0219-00 |  |  | 1500 pF , Cer, $50 \mathrm{~V}, 20 \%$ |
| C187 | R3 | 283-0219-00 |  |  | 1500 pF , Cer, $50 \mathrm{~V}, 20 \%$ |
| C188 | Q3 | 283-0219-00 |  |  | 1500 pF , Cer, $50 \mathrm{~V}, 20 \%$ |
| C189 | Q3 | 283-0154-00 |  |  | 22 pF, Cer, $50 \mathrm{~V}, 5 \%$ |
| C191 | Q2 | 283-0204-00 |  |  | $0.01 \mu \mathrm{~F}, \mathrm{Cer}, 50 \mathrm{~V}, 20 \%$ |
| 122Standiond 1 only.only. |  |  |  |  |  |


|  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- |
| Ckt | Grid | Tektronix | Serial/Model No. |  |
| No. | Loc | Part No. | Eff | Disc |

ELECTRICAL PARTS LIST (cont)


Tektronix
Serial/Model No.



| Ckt No. | Grid Loc | Tektronix <br> Part No. | Serial/M <br> Eff | odel No. Disc |
| :---: | :---: | :---: | :---: | :---: |
| INTEGRATED CIRCUITS |  |  |  |  |
| INTEGRATED CIUl ${ }^{1}$ |  | 156-0118-00 | XE040000 |  |
| U2 ${ }^{1}$ |  | 156-0180-00 | XB040000 |  |
| U135 | L6 | 156-0067-00 |  |  |
| U150 | 14 | 156-0182-00 |  |  |
| U160 | H4 | 156-0180-00 |  |  |
| U165 | H4 | 156-0118-00 |  |  |
| U167 ${ }^{1}$ | 1 G4 | 156-0100-00 | B010100 | B039999X |
| $\mathrm{U} 167^{2}$ |  | 156-0100-00 | B010100 | B059999 |
| U167 ${ }^{2}$ |  | 156-0100-02 | B060000 |  |
| U169 ${ }^{1}$ | F4 | 156-0100-00 | B010100 | B039999X |
| U169 ${ }^{2}$ |  | 156-0100-00 | B010100 | B059999 |
| U169 ${ }^{2}$ |  | 156-0100-02 | B060000 |  |
| U190 | P3 | 156-0278-00 |  |  |
| U200 | F5 | 156-0030-00 |  |  |
| U201 ${ }^{2}$ |  | 156-0079-00 |  |  |
| U209 | E5 | 156-0079-00 |  |  |
| U210 | D4 | 156-0079-00 |  |  |
| U211 | E4 | 156-0079-00 |  |  |
| U212 | E4 | 156-0079-00 |  |  |
| U213 | F3 | 156-0079-00 |  |  |
| U214 | G3 | 156-0079-00 |  |  |
| U215 | H3 | 156-0079-00 |  |  |
| U220 | K2 | 156-0042-00 |  |  |
| U222 | L2 | 156-0174-00 |  |  |
| U230 | J2 | 156-0150-00 |  |  |
| U235 | D3 | 156-0079-00 |  |  |
| U236 | C2 | 156-0079-00 |  |  |
| U237 | B2 | 156-0079-00 |  |  |
| U238 | B1 | 156-0079-00 |  |  |
| U239 | C1 | 156-0079-00 |  |  |
| . U 240 | D1 | 156-0079-00 |  |  |
| $1_{S}$ <br> ${ }^{1}$ Standard only. <br> ${ }^{2}$ Option 1 only. |  |  |  |  |

Dual 100 MHz J-K master-slave flip-flop, replaceable by SN74S112N
Quad 2-input nand gate, replaceable by SN74S00N Operational amplifier, replaceable by UA741C
Type 2-3-2 input gate, replaceable by MCl0105
Quad 2-input nand gate, replaceable by SN74SOON
Dual 100 MHz J-K master-slave flip-flop, replaceable by SN74S112
Single $40 \mathrm{MHz} \mathrm{J}-\mathrm{K}$ edge-triggered flip-flop, replaceable by SN74H102
Single $40 \mathrm{MHz} \mathrm{J}-\mathrm{K}$ edge-triggered flip-flop, replaceable by SN74H102
Single $40 \mathrm{MHz} \mathrm{J}-\mathrm{K}$ edge-triggered flip-flop, replaceable by SN74H102
Single $40 \mathrm{MHz} \mathrm{J}-\mathrm{K}$ edge-triggered flip-flop, replaceable by SN74H102
Single $40 \mathrm{MHz} \mathrm{J}-\mathrm{K}$ edge-triggered flip-flop, replaceable by SN74H102
Single $40 \mathrm{MHz} \mathrm{J}-\mathrm{K}$ edge-triggered flip-flop, replaceable by SN74H102
Divide by 10 ctr , replaceable by SP630B
Quad 2-input positive nand gate, replaceable by SN7400N
Single 10 MHz divide-by-2- $\&-5$ ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $\&-5$ ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $\delta-5$ ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $8-5$ ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $8-5$ ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $\delta-5$ ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $\&-5$ ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $\&-5$ ripple counter, replaceable by SN7490N
Dual $15 \mathrm{MHz} \mathrm{J}-\mathrm{K}$ master-slave flip-flop,
replaceable by SN7476N
Dual $20 \mathrm{MHz} \mathrm{J}-\mathrm{K}$ master-slave flip-flop, replaceable by SN74111N
Quad 2-input positive nand buffer, replaceable by $\operatorname{SN} 7437 \mathrm{~N}$
Single 10 MHz divide-by-2- $8-5$ ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2-\&-5 ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $\&-5$ ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $\delta-5$ ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $\delta-5$ ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $\&-5$ ripple counter, replaceable by SN7490N

| Ckt. No. |  | Tektronix Part No. | Serial/Model No. Eff . Disc | Description |
| :---: | :---: | :---: | :---: | :---: |
| INTEGRATED CIRCUITS (cont) |  |  |  |  |
| U246 | F2 | 156-0043-00 |  | Quad 2-input positive nor gate, replaceable by SN7402N |
| U250 | E3 | 156-0198-00 |  | Quad 1atch, replaceable by MC4035P |
| U251 | D3 | 156-0198-00 |  | Quad latch, replaceable by MC4035P |
| U252 | C4 | 156-0198-00 |  | Quad latch, replaceable by MC4035P |
| U253 | B3 | 156-0198-00 |  | Quad latch, replaceable by MC4035P |
| U254 | B2 | 156-0198-00 |  | Quad latch, replaceable by MC4035P |
| U255 | C2 | 156-0198-00 |  | Quad latch, replaceable by MC4035P |
| U256 | D2 | 156-0198-00 |  | Quad latch, replaceable by MC4035P |
| U260 | M1 | 156-0030-00 |  | Quad 2-input positive nand gate, replaceable by SN7400N |
| U262 | K2 | 156-0041-00 |  | Dual 15 MHz D-type pos-edge-trig flip-flop, replaceable by SN7474N |
| U263 | L2 | 156-0041-00 |  | Dual 15 MHz D-type pos-edge-trig flip-flop, replaceable by SN7474N |
| U265 | E1 | 156-0111-00 |  | Single BCD-to-decimal decoder/driver, replaceable by SN74145N |
| U267 | E2 | 156-0058-00 |  | Hex. inverter, replaceable by SN7404N |
| U270 | H2 | 156-0128-00 |  | Single BCD-to-seven-segment decoder/driver, replaceable by SN7447N |
| U300 | C6 | 156-0071-00 |  | Voltage regulator, replaceable by UA723C |
| U320 | B6 | 156-0071-00 |  | Voltage regulator, replaceable by UA723C |
| CRYSTALS |  |  |  |  |
| $\mathrm{Y}_{2} 00$ | F5 |  |  |  |
| $Y 201^{1}$ | F6 | 119-0262-00 |  | Oscillator, RF, 5 MHz |

## CONTROLS AND CONNECTORS

## Display Readout

LED readout, seven 7 . segment digits with automatically placed decimal point. The leading zeroes are suppressed unless an overflow is indicated.

## Overflow Indicator

 LED indicates overflow of leading digits when readout attempts to display more than seven digits.
## DISPLAV TIme Control

Variable control concentric with MEASUREMENT IN TERVAL switch sets the length of time the reading will be displayed after the count is made and before the next measurement is taken. Display time can be varied from 0.1 second (MIN) to about 10 seconds. HOLD position (clockwise) provides continuous display until reset by pressing the RESET button.
$M H Z$ and $k H z$ Units Indicators
LED indicates that readout displayed number should be multiplied by $10^{6}$ be multiplied by
$(\mathrm{MHz})$ or $10^{3}(\mathrm{kHz})$.


Relocated on back
of board SN B07000

PARTS LOCATION GRID


## INTERNAL ADJUSTMENTS PROCEDURE

## Services Availab

Tektronix, Inc. provides complete instrument repair and adjustment at local Field Service Centers and at the Factor Service Center. Contact your local TEKTRONIX Field Office or representative for further information

## Test Equipment

For measurement of the power supply voltages, a 20,000 ohms/volt VOM will give satisfactory measurements. Fo example, Triplett 630 NA multimeter.

For $1-\mathrm{MHz}$ frequency measurement, a secondary frequency standard or other frequency source having measuring optional 5 MHz crystal output) is recommended for accuracy. Also recommended is a test oscilloscope with a bandwidth of at least 1 MHz and a stable triggering circuit for frequency-comparison measurement.

## Procedure

## note

The performance of this instrument can be check at any temperature within the $0^{\circ} \mathrm{C}$ to $+50^{\circ} \mathrm{C}$ range. $+20^{\circ} \mathrm{C}$ and $+30^{\circ} \mathrm{C}\left(+68^{\circ} \mathrm{F}\right.$ and $\left.+86^{\circ} \mathrm{F}\right)$.

The DC 502 can be operated either fully installed in a TM 500 Series Power Module or connected to a plug-in extender (TEKTRONIX Part No. 067-0645-01).

Power Supply Checks and Adjustment. Connect the oltmeter between the +15 -volt test point and ground. 5 -volt, -5.2 -volt, and -10 -volt supplies to be within $5 \%$.

NOTE
f the instrument is operated on the plug-in extender, the +5 -volt supply may not regulate.


Time-Base Frequency Check and Adjustment. Connect the DC $5021-\mathrm{MHz}$ time base reference and the secondary standard to the oscilloscope as shown. Adjust the oscillo scope to display several complete cycles.

To determine oscillator error, observe the rate of horizontal drift of the displayed waveform. Waveform moving to the right indicates that the time-base frequency is $<1 \mathrm{MHz}$; to the left, $>1 \mathrm{MHz}$. The period in seconds for he waveform to move the width of one cycle is equal to the frequency difference in parts in $10^{6}$. For example, if the waveform drifts to the right at a rate of one cycle's in $10^{6}$ low. Maximum allowable frequency difference is 1 part in $10^{5}$ ( 5 parts in $10^{7}$ for the optional 5 MHz crystal). Adjust C201 for no drift.

## DC 502 BLOCK DIAGRAM





# MECHANICAL PARTS LIST 

Replacement parts should be ordered from the Tektronix Field Office or Representative in your area. Changes to Tektronix products give you the benefit of improved circuits and components. Please include the instrument type number and serial number with each order for parts or service.

## ABBREVIATIONS

| BHB | binding head brass | $h$ | height or high | OHB | oval head brass |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BHS | binding head steel | hex. | hexagonal | OHS | oval head steel |
| CRT | cathode-ray tube | HHB | hex head brass | PHB | pan head brass |
| csk | countersunk | HHS | hex head steel | PHS | pan head steel |
| DE | double end | HSB | hex socket brass | RHS | round head steel |
| FHB | flat head brass | HSS | hex socket steel | SE | single end |
| FHS | flat head steel | ID | inside diameter | THB | truss head brass |
| Fil HB | fillister head brass | 1 g | length or long | THS | truss head steel |
| Fil HS | fillister head steel | OD | outside diameter | w | wide or width |


| Fig. 8 Index No. | Tektronix Part No. | Serial/Model No. Eff Disc | $\begin{aligned} & Q \\ & t \\ & y \end{aligned}$ | $12345 \quad$ Description |
| :---: | :---: | :---: | :---: | :---: |
| 1-1 | 366-0494-00 |  | 1 | KNOB, gray--TRIGGER LEVEL |
|  | - - - - |  | - | knob includes: |
|  | 213-0153-00 |  | 1 | SETSCREW, 5-40 x 0.125 inch, HSS |
| -2 | 366-1031-00 |  | 1 | KNOB, red--DISPLAY TIME |
|  | - - - - |  | - | knob includes: |
|  | 213-0153-00 |  | 1 | SETSCREW, 5-40 x 0.125 inch, HSS |
| -3 | 366-1165-00 |  | 1 | KNOB, gray--MEASUREMENT INTERVAL |
|  | - - - - |  | - | knob includes: |
|  | 213-0153-00 |  | 2 | SETSCREW, 5-40 x 0.125 inch, HSS |
| -4 | 366-1422-00 |  | 1 | KNOB, latch |
| -5 | 366-1257-30 |  | 1 | PUSHBUTTON--RESET |
|  | 366-1402-01 |  | 1 | PUSHBUTTON--START |
| -6 | 366-1402-00 |  | 1 | PUSHBUTTON--X5 |
|  | 366-1257-87 |  | 1 | PUSHBUTTON--X10 |
| -7 | 131-0955-00 |  | 2 |  |
|  | - - |  | - | J180 electrical list) |
|  | ---- |  | - | mounting hardware for each: (not included w/connector) |
| -8 | 210-0255-00 |  | 1 | TERMINAL, lug, 0.391 inch ID, SE |
| -9 | - - - - |  | 1 | RESISTOR, variable (See R135 electrical list) |
|  | ---- |  | - | mounting hardware: (not included with resistor) |
| -10 | 210-0583-00 |  | 1 | NUT, hex., 0.25-32 x 0.312 inch |
| -11 | 210-0940-00 |  | 1 | WASHER, flat, 0.25 ID x 0.375 inch OD |
| -12 | 426-0681-00 |  | 4 | FRAME, pushbutton |
| -13 | 426-0916-00 |  | 1 | FRAME, readout window |
| -14 | 331-0314-00 |  | 1 | WINDOW, readout |
| -15 | 337-1399-00 |  | 2 | SHIELD, electrical, side |
| -16 | 333-1653-00 |  | 1 | PANEL, front |
|  | - - - |  | - | mounting hardware: (not included with panel) |
| -17 | 211-0159-00 |  | 2 | SCREW, 2-56 x 0.375 inch, PHS |
| -18 | 210-0405-00 |  | 2 | NUT, hex., 2-56 x 0.188 inch |

FIGURE 1 EXPLODED (cont)

| Fig. \& Index No. | Tektronix Part No. | Serial/Model No. Eff Disc | $Q$ | $12345 \quad$ Description |
| :---: | :---: | :---: | :---: | :---: |
| 1-19 | 214-1513-00 |  | 1 | LATCH, plug-in retaining |
|  | ----- |  | - | mounting hardware: (not included with latch) |
| -20 | 213-0254-00 |  | 1 | SCREW, thread forming, 2-56 x 0.25 inch, $100^{\circ} \mathrm{csk}$, FHS |
| -21 | 386-2292-00 |  | 1 | SUBPANEL, front |
|  | - - - |  | - | mounting hardware: (not included w/subpane1) |
| -22 | 213-0229-00 |  | 4 | SCREW, thread forming, 6-20 $\times 0.375$ inch, $100^{\circ} \mathrm{csk}$, FHS |
| -23 | ---- |  | 1 | CIRCUIT BOARD ASSEMBLY--DISPLAY (See A2 electrical list) |
| -24 | 337-1719-00 |  | 1 | SHIELD, electrical, subpanel |
| -25 | - - - - |  | 1 | CIRCUIT BOARD ASSEMBLY--PRESCALER (See A3 electrical list) |
|  | 136-0269-02 |  | - | circuit board assembly includes: |
| -26 | 136-0269-02 |  | 1 | SOCKET, integrated circuit, 14 pin |
| -27 | 136-0252-04 |  | 6 | SOCKET, pin connector |
|  | - |  | - | mounting hardware: (not included w/circuit board assy) |
| -28 | 211-0001-00 |  | 2 | SCREW, 2-56 x 0.25 inch, PHS |
| -29 | - - - - - |  | 1 | CIRCUIT BOARD ASSEMBLY--MAIN (See A1 electrical list) |
|  | ----- |  | - | circuit board assembly includes: |
| -30 | 131-0604-00 |  | 13 | CONTACT, electrical (For repair, see maint. section) |
| -31 | 136-0252-04 |  | 16 | SOCKET, pin connector |
|  | 136-0234-00 |  | 2 | SOCKET, pin connector |
|  | 131-0566-00 |  | 2 | LINK, terminal connecting |
| -32 | 376-0051-00 |  | 1 | COUPLING, shaft |
|  | - - |  | - | coupling includes: |
|  | 213-0022-00 |  | 4 | SETSCREW, 4-40 x 0.188 inch, HSS |
|  | 354-0251-00 |  | 2 | RING, coupling |
|  | 376-0049-00 |  | 1 | COUPLING, plastic |
| -33 | 384-1146-00 |  | , | SHAFT, extension |
| -34 | 260-1425-00 |  | 1 | SWITCH, push--START-STOP (S235) |
| -35 | 361-0382-00 |  | 8 | SPACER, switch, brown |
| -36 | 260-1353-01 |  | 1 | SWITCH, push--ATTEN (S100A \& S100B) |
| -37 | - - - |  | 1 | RESISTOR, variable (See R235 electrical list) |
|  | - - - - |  | - | mounting hardware: (not included w/resistor) |
| -38 | 210-0583-00 |  | 1 | NUT, hex., $0.25-32 \times 0.312$ inch |
| -39 | 210-0046-00 |  | 1 | WASHER, lock, internal, 0.261 ID x 0.40 inch OD |
| -40 | 407-0803-00 |  | 1 | BRACKET, component mounting |
|  | ------ |  | 3 | mounting hardware: (not included w/circuit board assy) |
| -41 | 213-0146-00 |  | 3 | SCREW, thread forming, 6-20 $\times 0.312$ inch, PHS |

## FIGURE 1 EXPLODED (cont)

| Fig. \& Index No. | Tektronix Part No. | Serial/Model No. Eff Disc | $\begin{aligned} & Q \\ & t \\ & y \end{aligned}$ | $12345 \quad$ Description |
| :---: | :---: | :---: | :---: | :---: |
| 1-42 | 426-0724-00 |  | 1 | FRAME SECTION, bottom |
| -43 | 426-0725-00 |  | 1 | FRAME SECTION, top |
| -44 | 179-1767-00 |  | 1 | WIRING HARNESS |
|  | 105-0406-00 |  | 1 | ACTUATOR ASSEMBLY, cam switch (S200) |
|  | - - - |  | - | actuator assembly includes: |
| -45 | 200-1391-00 |  | 1 | COVER |
|  | - - - - |  | - | mounting hardware: (not included with cover) |
|  | 211-0022-00 |  | 2 | SCREW, 2-56 x 0.188 inch, PHS (Discard \& use ref 非8) |
| -46 | 210-0001-00 |  | 2 | WASHER, lock, internal, 0.092 ID x 0.18 inch OD |
| -47 | 354-0219-00 |  | 1 | RING, retaining |
| -48 | 401-0057-00 |  | , | BEARING, front |
| -49 | 214-1139-001 |  | - | SPRING, flat, gold |
|  | 214-1139-02 ${ }^{1}$ |  | - | SPRING, flat, green |
|  | 124-1139-03 ${ }^{1}$ |  | - | SPRING, flat, red |
| -50 | 214-1127-00 |  | 1 | ROLLER, detent |
| -51 | 105-0405-00 |  | 1 | DRUM ASSEMBLY |
| -52 | 401-0057-00 |  | 1 | BEARING, rear |
| -53 | 210-0405-00 |  | 2 | NUT, hex., 2-56 x 0.188 inch |
| -54 | 210-0406-00 |  | 4 | NUT, hex., 4-40 x 0.188 inch |
|  | ----- |  | - | mounting hardware: (not included w/actuator assembly) |
| -55 | 211-0116-00 |  | 3 | SCREW, sems, 4-40 x 0.312 inch, PHB |
| -56 | - - - - |  | 1 | CIRCUIT BOARD ASSEMBLY--PROTECTION (See A4 elect. list) |
|  | - - - |  | - | circuit board assembly includes: |
| -57 | 344-0154-00 |  | 2 | CLIP, electrical, fuse |
|  | ----- |  | - | mounting hardware: (not included w/circuit board assy) |
| -58 | 213-0206-00 |  | 1 | SCREW, thread forming, 6-32 $\times 1.25$ inches, PHS |
| -59 | 361-0516-00 |  | 1 | SPACER, sleeve, 0.986 inch long |

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DC 502550 MHz FREQUENCY COUNTER

## MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Sections of the manual are often printed at different times, so some of the information on the change pages may already be in your manual. Since the change information sheets are carried in the manual until ALL changes are permanently entered, some duplication may occur. If no such change pages appear in this section, your manual is correct as printed.

## TEXT CORRECTION

The upper limit frequency response specifications has been changed to 110 MHz . Any reference to a 100 MHz should be changed to read: 110 MHz .

DC 502 EFF SN B040000-up

## ELEGTRICAL PARTS LIST AND SCHEMATIC CHANGES

## REMOVE :

| U167 | 156-0100-00 | Single $40 \mathrm{MHz} \mathrm{J-K} \mathrm{edge-triggered} \mathrm{flip-flop}$, <br> replaceable by SN74H102 |
| :--- | :--- | :--- |
| U169 156-0100-00 | Single $40 \mathrm{MHz} \mathrm{J-K} \mathrm{edge-triggered} \mathrm{flip-flop}$, <br> replaceable by SN74H102 |  |

CHANGE TO:
A1
670-2102-01
MAIN Circuit Board Assembly
ADD :

670-3300-00

U1

U2
156-0180-00

DIVIDE BY 5, Circuit Board Assembly
Dual $100 \mathrm{MHz} \mathrm{J}-\mathrm{K}$ master-s lave flip-flop, replaceable by SN74S112

- Quad 2-input nand gate, replaceable by SN74S00N



## DC 501 EFF SN BO60000-up

DC 502 EFF SN BO70000-up

## ELECTRICAL PAR'TS LIST AND SCHEMATIC CHANGE

ChANGE TO:
R137
311-1554-00
200 k $\Omega$, Var

ADD :
C121 283-0111-00 $0.1 \mu \mathrm{~F}$, Cer, 50 V
(R137 and C121 are located on Diagram $\langle 1\rangle$ COUNTER TIME BASE \& CONTROL)



[^0]:    ${ }^{1}$ Replace only with part bearing the same color code as the original part in your instrument.

