component news

April 25, 1980 COMPANY CONFIDENTIAL Issue 280

Intel 2118 — Below expectation

The introduction of the Intel 2118 marks the beginning of a new era in dynamic RAM design. Because this was the first 5V-only dynamic RAM, Memory and I/O Component Engineering undertook an extensive analysis and evaluation. Results of the preliminary circuit analysis and testing of D mask samples, both furnished to us and purchased directly, are outlined in this article.

General impressions

In analyzing this device, a few overall impressions of the circuit design have been formulated:

1. An attempt was made to minimize the number of internal clocks. This is evident in the design of the address input circuit where two control clocks and their complements are used to control internal address latching operations.

2. Attempts were also made to reduce the amount of internal interconnnections. Many of the internal clocks appear to have a self-timing circuit to restore the initial state of the clock generator (see Figure 1). This eliminates the need to route clock signals around the chip for restoration purposes.

3. Thought was given to minimizing internal delays. An obvious difference between the Intel 2118 and the 2117 is the use of a single data bus sensing circuit. This means the proper data bus is selected before actual sensing occurs. The 2117 uses two separate data bus sensing circuits and a combiner before the output buffer circuit. The 2118 scheme should improve speed, but timing overlap can cause internal bus contentions.

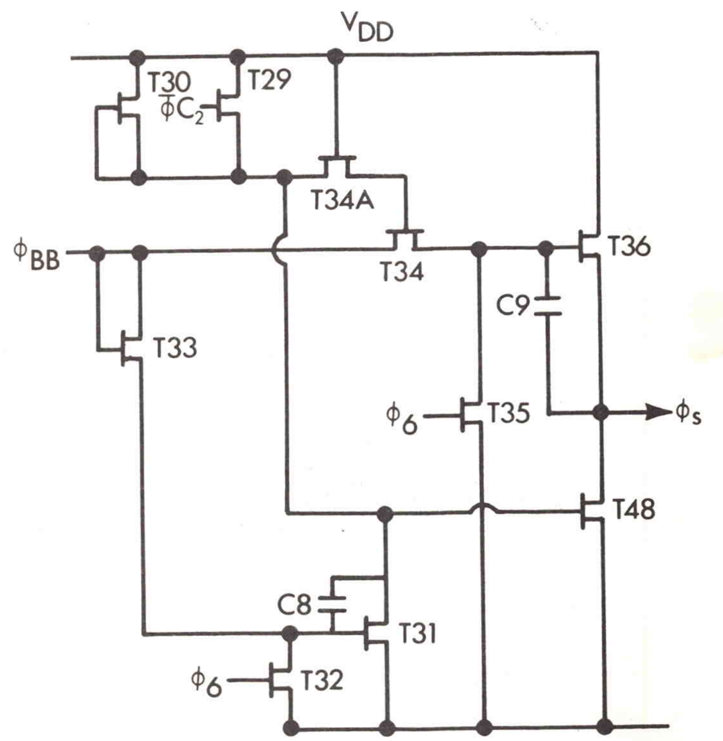


Figure 1 — ϕ_s clock

continued on page 2

Also in this issue

Problems uncovered

Early testing was devoted to investigating pattern sensitivity and timing constraints. This was done for two reasons: (1) on the sample opened for circuit analysis, a large poly-II misalignment was present. This tends to cause functional data sensing problems. Although no pattern sensitivities were discovered in the samples tested, the amount of misalignment is significant and would effect the sensing operation.

(2) It was felt that timing overlap caused by process variations and circuit design abnormalities might cause a timing specification problem. Two problems were noticed. Values of t_{RAH} and t_{CAH} were out of specification over the operating voltage range at 70°C. The component became non-functional at 4.3V as indicated in the schmoo plot (Figure 2). This seemed rather close to the 4.5V lower limit specification.

Intel's response

Our concerns were communicated to Intel. The response was that the 2118 did indeed have some problems, and was undergoing some circuit design changes. Specifically, Intel stated three areas where changes were being made:

1. In the dummy cell circuit.
2. In the output sense and buffer circuits to rectify and output delay problem.
3. Changes in layout to make the device conform to present design rules.

It is my opinion that further circuit changes have been made to produce a better performing device.

User considerations

One side of the charge storage cell plates on the 2118 is connected through a conditional desensitizing circuit to the 5V supply. The circuit is an attempt to reduce sensitivity to noise on the 5V line. The attempt seems inadequate for its designed purpose. It will smooth out noise spikes on the supply line, but a better design would have shown a gounded cell plate. This means the user must continue to minimize noise on the supply line.

As was the case with the 4116, the 2118 part may be susceptible to spurious noise on the address and control inputs. Efforts must be made to reduce noise on these inputs.

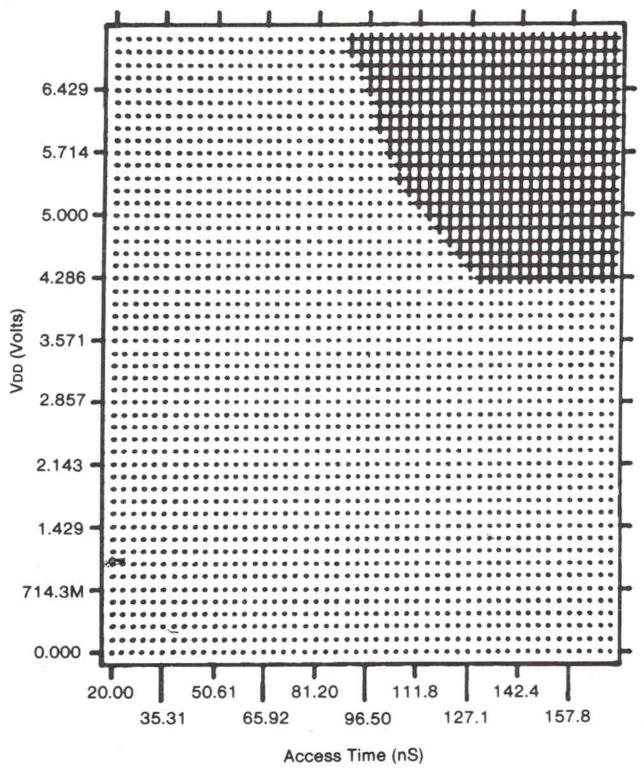


Figure 2 — Schmoo plot, Intel 2118

It appears the first version of a 5V-only dynamic RAM has failed to meet design expectations. Although care was taken to reduce coupling (holding off unselected word lines) and to improve sensing margins (active bit line restoration), the component did not achieve desired performance. Intel has made changes to the design (D-A mask) and these changes will be evaluated as samples become available.

For more information, please contact me on ext. 2543.

Bob Goetz
78-557

Preliminary evaluation report

TI's 92K bit bubble memory

Texas Instruments' 92K bit bubble memory was the first commercially available device supported by a set of custom ICs designed to interface the memory with external systems. Since its introduction in 1976, TI has been continually improving its internal design, which has made possible both better performance and lower prices (through improved yield).

Initially the 92K bit bubble memory was used primarily on projects internal to TI (e.g. the Silent 700 terminal), but in the past couple of years it has been incorporated into some systems developed by external parties as well. The design iterations of the 92K bit device are:

TBM0100 — 1976
TBM0103 — February 1977
TIB0203 — May 1978
TIB0203S — September 1979

Within the past year at least a dozen companies have announced bubble memories at technical meetings, and four major US companies (Intel, TI, National & Rockwell) have announced **commercial** bubble memory devices with support ICs. These chips range in capacity from 92K to 1M bit.

Although the TBM0103 has become an obsolete part, there are still reasons for investigating it technically. When opened up the device gives a first-hand view of all the pieces in a bubble memory package (see Figure 1). But, to evaluate the device we needed to develop a technique for opening bubble memory packages nondestructively. (Intel said it was impossible.)

Secondly, technical knowledge derived from this effort would give a reference for comparing other bubble memories. This aids in correlating device performance with internal design.

Evaluation results

We first developed a technique for nondestructively opening a bubble memory package. The method consists of using a Dremel tool to cut away first the magnetic shield, then the bias magnets, followed by sectioning the drive coils. At this point all that remains is the bubble chip embedded in a thermally conductive epoxy mounted on a lead frame. Because the epoxy does not bond too strongly to the lead frame, a sharp X-acto knife can be wedged between the layers and the epoxy pried off, leaving the exposed garnet chip ready for microscopic examination.

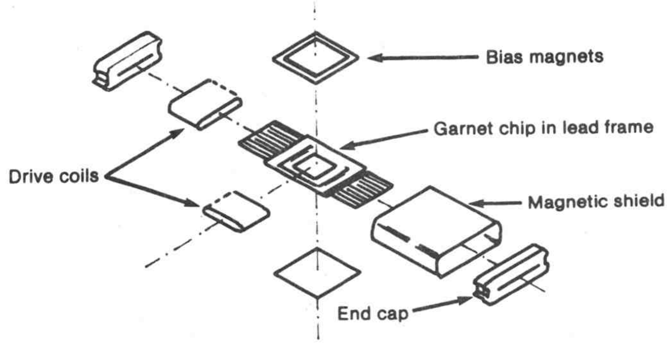


Figure 1 — Exploded view of bubble memory package

Our preliminary evaluation has been limited to photomicrographs of the surface of the garnet chip. The first observation made was that the architecture was of the "major/minor loop" type (see Figure 2, page 4). This type of architecture is typified by data being generated and detected on a closed propagation path called the "major loop," while data is stored in several "minor loops" (see Figure 3, page 5). This architecture is still used in the newer version of the 92K bit device, but is being replaced by the "block replicate" architecture in larger capacity devices now coming on the market.

It is of greater interest to look in detail at the various structures, which perform the basic functions (generate, replicate, annihilate, transfer, detect, corner turns) because these structures determine critical operating margins and hence, driving performance.

continued on page 4

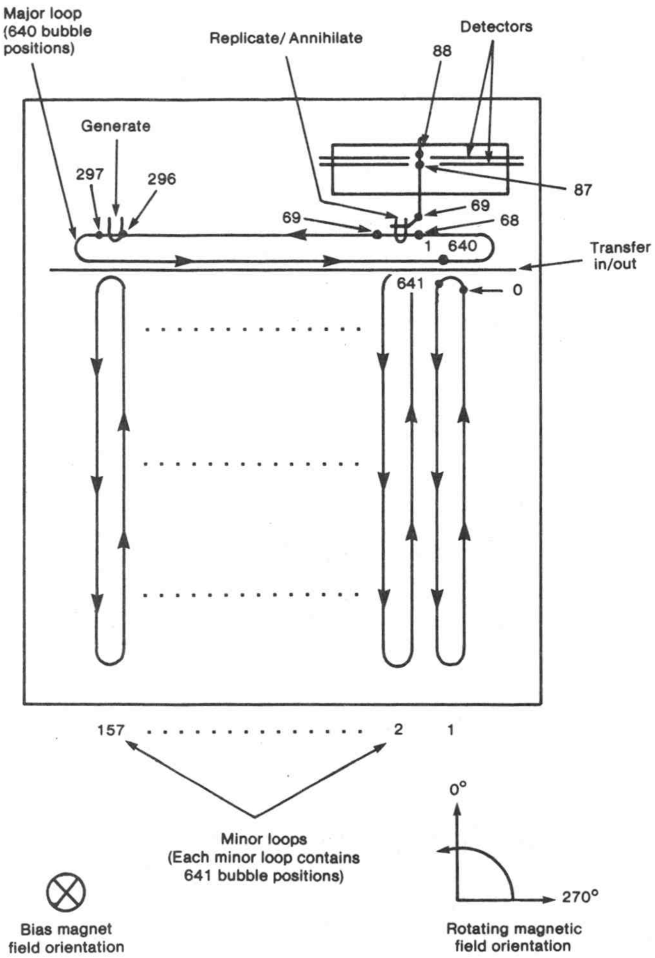


Figure 2 — TBM0103 architecture

Generator

The gross structure of the bubble generator is shown in Figure 4. The bubble is generated when a pulse of current is passed through the V-shaped conductor, causing a highly localized magnetic field in the groove at the end of the conductor. This field causes a magnetic domain or bubble to be formed in the garnet layer just beneath the conductor. If the timing is correct this bubble can now be moved to the left along the T-I (major loop) propagation path.

The important observation here is that the generator makes a bubble from scratch. This can be contrasted with the newer and more efficient method of generation where a permanent "seed" bubble is stretched and cut into two pieces to form a new bubble.

Another interesting observation is the "step" in the legs of the generator, see Figure 4. The length of this step is exactly equal to one propagation period (distance between I's on the TI pattern in the major loop). It appears that Texas Instruments found it necessary to alter their original design and move the generator one step closer to the detector. This may have been done to improve the capability to modify a page of data (speculation only).

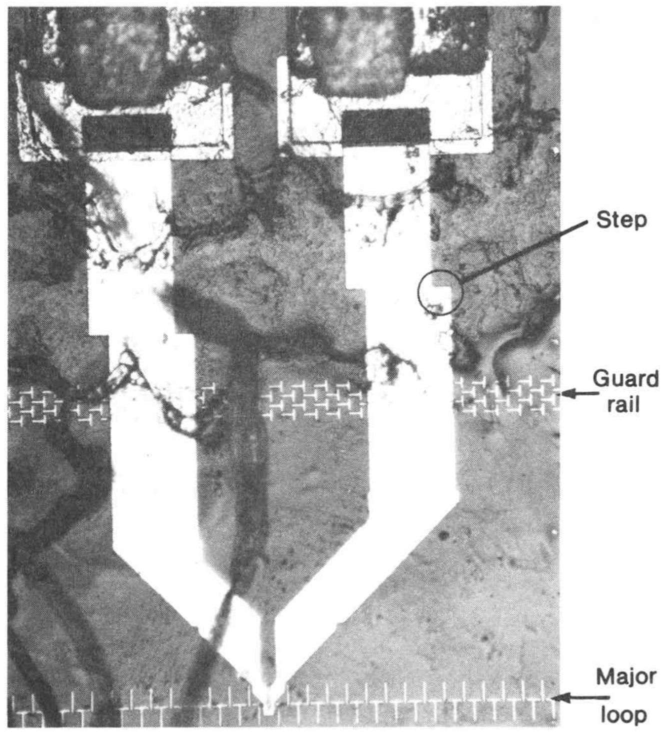


Figure 4 — Bubble generator (Mag. 112X)

Transfer gate

The transfer gate structure is shown in Figure 5, page 6. The gate was identified as the "dollar sign" type, due to the shape of the permalloy (gray colored) structure. Data is transferred in or out of the major loop by application of a suitably timed current pulse through the conductor (light colored) when the bubble is in position at the transfer gate.

continued on page 5

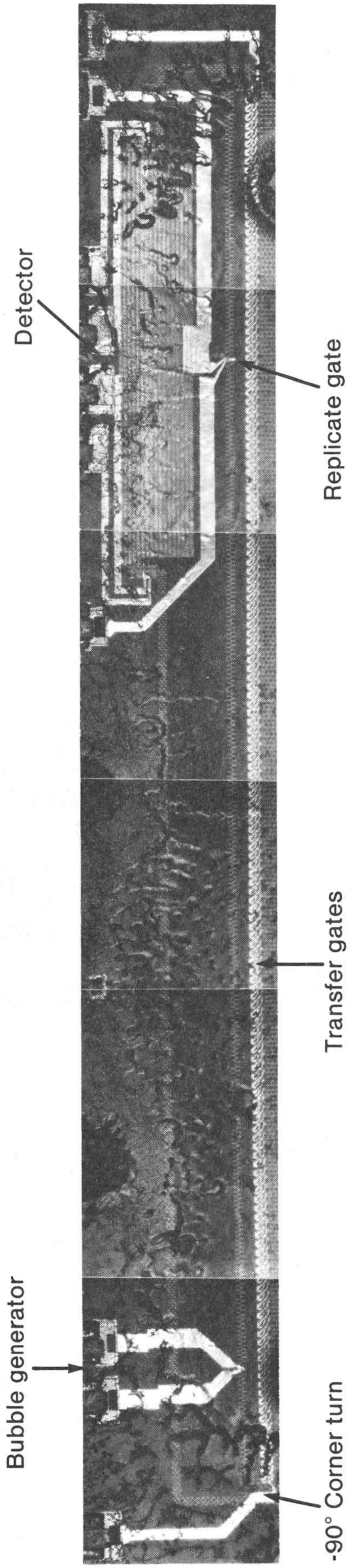


Figure 3 — Major/minor loop architecture
(Mag. — 27X)

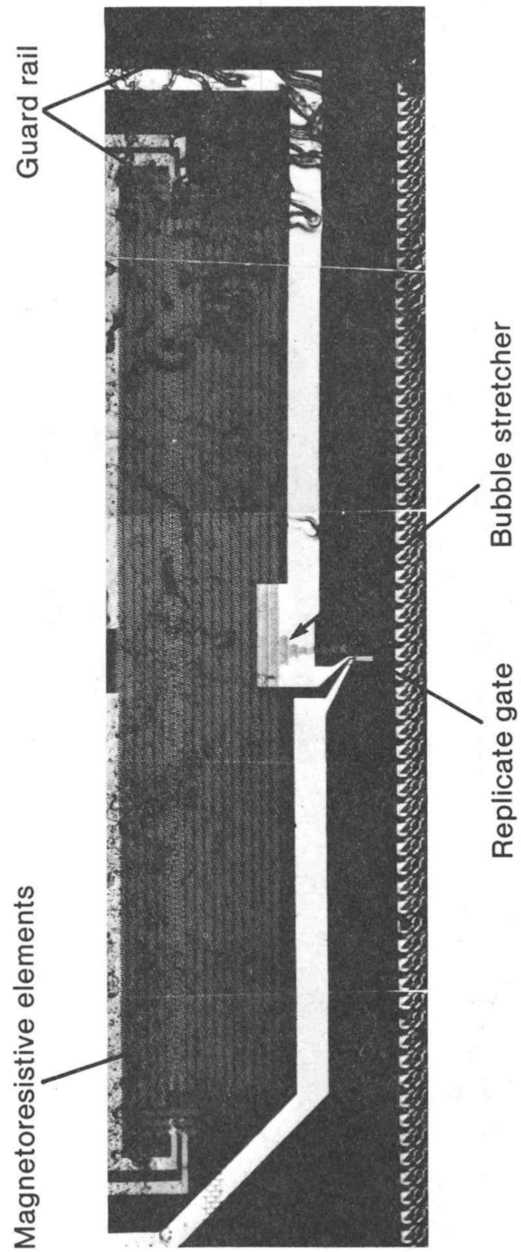


Figure 6 — Detector
(Mag. — 56X)

continued on page 6

Note the defect in the permalloy structure just below the transfer gate of the second minor loop from the left. The diagonal bar does not extend far enough to make contact with the rest of the permalloy structure, which diminishes device performance.

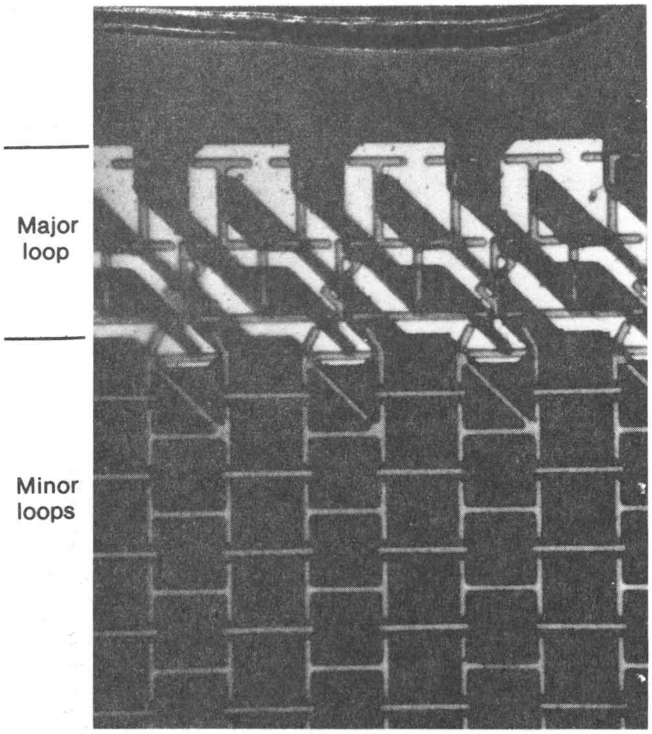


Figure 5 — Transfer gate (Mag. 452X)

Detector

The entire detector is shown in Figure 6, page 5. The four principle regions of the detector are:

1. Replicate gate — where the bubble is removed from the major loop.
2. Stretcher — where the bubble's size is increased by stretching it along the chevron overlay.
3. Magnetoresistive element — when the bubble passes under this "zig-zag" pattern its magnetic field causes the electrical resistance of the zig-zag conductor to be altered. Notice that there are two conductors in the detector structure — the second is used as a dummy to cancel out the effect of the rotating drive field which also affects the conductor's resistance.
4. Guard rail — after the bubble passes the zig-zags it is marched upward to the last row of chevron elements where it passes on to "bubble heaven."

A detailed view of the replicate gate is shown in Figure 7. It is identified to be a "pick ax" type gate. This gate makes three distinct functions possible:

1. Read destructively — read data and clear that memory location.
2. Clear memory location — clear memory location without reading data.
3. Read non-destructively — read data and return it to the same memory location for later use.

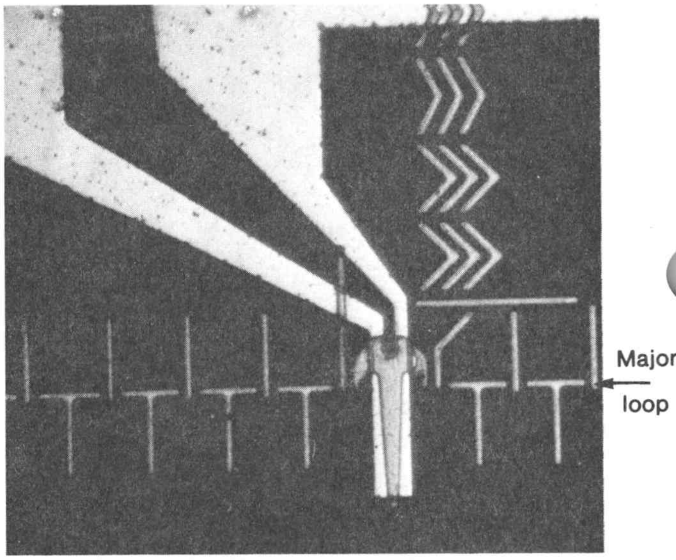


Figure 7 — Replicate gate detail (Mag. 452X)

In a destructive read-out, the bubbles in the major loop approach the gate from the right. When they reach the gate, they are transferred out of the major loop and into the detector where they are stretched and detected as they pass under the magnetoresistive element. Because the bubbles are transferred out of the major loop, that memory location is cleared for new data.

continued on page 7

If you want only to clear a memory location, the data is transferred into the detector area as before, but this time the signal from the detector is ignored by the controlling circuitry. It is also possible to cut the bubbles into two pieces at this gate and send one to the detector and the other along the major loop and back into its original storage area in the minor loops. In this way data can be read non-destructively.

Future investigations

Although the work done so far on the TBM0103 has been illuminating, it has also raised several new questions which will be addressed in the next few weeks. Presently work is being done on the Intel 7110 1M bit bubble memory, which has proved to be much more complicated internally. (A report on this work will be presented at a later date.) After the preliminary work has been completed on the Intel device, more detailed "autopsies" including process analysis and materials characterization will be performed on both devices.

Anyone wishing further information on bubble memories can contact **Dick Green, Memory and I/O Component Engineering, ext. 2557.**

Free HEXFETs

International Rectifier has given me 55 of their HEXFETs to distribute around Tek.

All of these devices are in plastic TO-220 packages. Most are 400V parts. If you can put them to good use, give me a call and I'll send you a few. Because demand will probably exceed supply, I'll give them out on a priority basis.

Jerry Willard
78-557, ext. 2539

Correction

In the last issue of **Component News** the delivery station for Dale Vanderzanden (ME New Product Introduction group) was in error. Dale's delivery station should have been 78-575.

Manufacturing Engineering Announcement

Because of reorganization, Manufacturing Engineering Process Support no longer designs and builds special purpose jigs, fixtures, machines and machine "marriages" for business units throughout Tek. For this kind of work, please contact the machine shop that supports your particular business unit, or farm it out.

We do, however, retain the capability of building small tools and dies for your special applications. If you have any questions please contact me at 78-544, ext. 2517.

Jim Mumm
ME Process Support

Wrong number causes problems

Dennis Johnson, Electromechanical Component Engineer, reports that his phone extension is incorrectly listed in the Tek phone directory. The number that is listed is extension 2466. The correct phone number is extension **2471.** Please make this note in your phone directory.

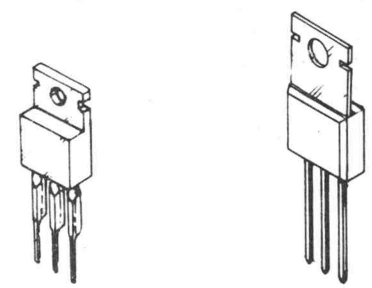
Bad news for voltage regulator users

Texas Instruments is discontinuing production of all voltage regulators housed in TO-202 packages. This will affect three Tek part numbers and leave National Semiconductor as the only available source.

The Tek part numbers affected are:

Tek P/N	Vendor P/N	Output voltage
156-1262-00	78M15	+15V
156-1263-00	78M05	+5V
156-1264-00	79M12	−12V

The TO-202 is pin compatible with the TO-220 package and was originally developed to replace the TO-220 for low-cost, sensitive applications requiring less output current. The TO-202 is easier to fabricate, making it less expensive than the TO-220. However, industry users have not standardized using the TO-202, which is reflected by Texas Instruments' decision to drop low usage voltage regulators.



TO-220 package **TO-202 package**

National is a front-runner in the development of regulators, and they have recently discontinued all odd-voltage regulators in all package styles. The only fixed voltage regulators available from National are the ±15, ±12 and ±5 volt parts. National is hoping the industry will standardize using the LM317 (positive) and LM337 (negative) adjustable regulators.

In addition, the news that Signetics is dropping their entire voltage regulator line due to low profitability suggests and reinforces the trend of semiconductor manufacturers to discontinue low volume, low profit regulators.

Designers should use caution in implementing the affected part numbers in any new designs. Also, when part numbering any new voltage regulator, I suggest you confer with me about the future of the device.

Chris Martinez
78-557, ext. 2540

3rd "technology fair" scheduled

On Thursday and Friday, May 8 and 9, Tek Labs' Component Development Group will present the third technology fair in Building 50 auditorium. The hours will be from 10 am to 4 pm Thursday, and from 10 am to 1 pm Friday. The objective of the fair is to show Tek engineers and managers recent developments from the Component Development Group.

The technology fair will present working demos of new and continuing developments that have not had wide exposure; component "product lines" with which Tek engineers should become familiar; and new components, ideas and analytical tools. Component Development Group engineers and managers will be on hand to answer questions. The format will be an "open house," with no formal papers presented.

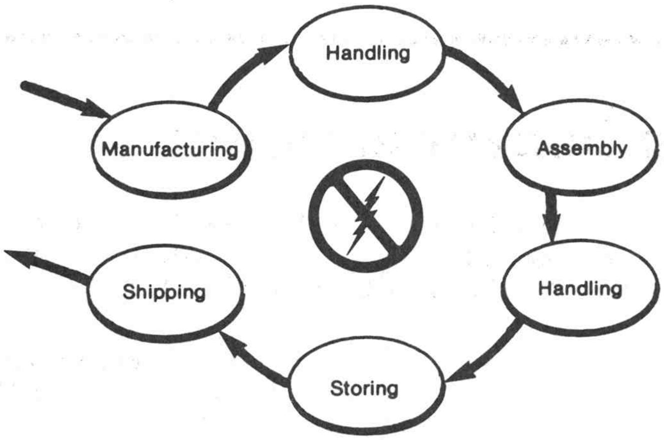
Because some of the material presented will be company confidential, each person attending should wear their name tag for easy identification.

For more information about the CDG technology fair, call **Sally Jo Smith on ext. 5736.**

Materials for ESD protection

In the past, engineers didn't have to be concerned with what type of floor they were walking on, or what kinds of polishes, cleansers and coatings they used. However, as solid state circuitry becomes faster and more sophisticated, the need for proper electrostatic discharge (ESD) control is imperative.

Static in varying intensities not only causes shock discomfort or damage due to its charge, it attracts and holds dirt and other airborne contaminants to surrounding surfaces. This in turn can result in scrambled computer data, errant signals, erratic machine behavior and component damage. In an industrial plant ESD causes poor quality parts, waste rejects, unscheduled downtime, increased maintenance due to latent failures and the need for more intensive environmental control.



ESD occurs when a concentration of electrical charges creates a voltage and thus an electric field between the charge and the reference point, such as ground. As long as a body is isolated from ground and there is a relative motion of a contacting medium (such as air), a charge will develop on any surface — conductive or not. The potential level of this charge on any body depends on how fast the electrostatic charge is bled off.

Static-safe operating and handling techniques are particularly important because many devices are damaged by potentials that the discharging person can't even feel (<3000 volts). Yet, potentials as high as 40,000 volts have been measured on people (see Figure 1). Just by walking a few steps on a dielectric floor, an individual can easily generate 10,000 volts from their body. Very sensitive devices zap and are degraded with just 100 volts or less static charge.

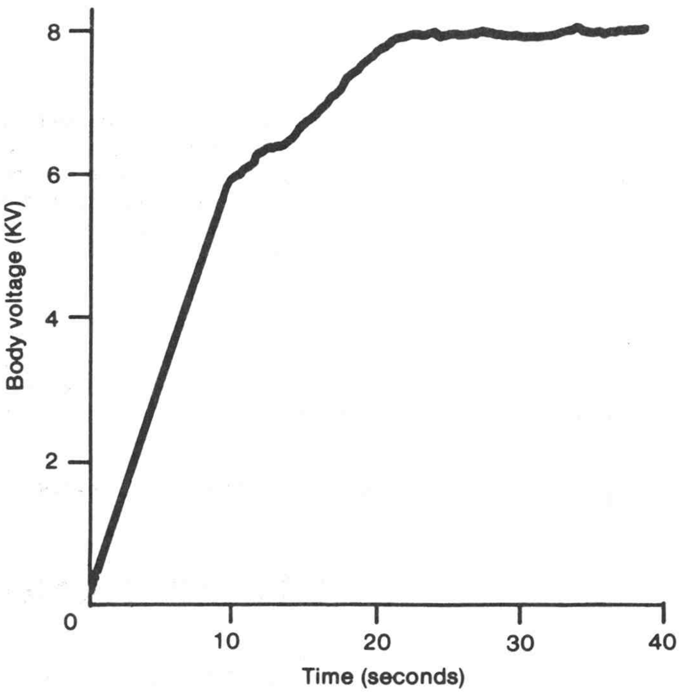


Figure 1 — Body voltage vs. distance walked
(stroll test, acrylic carpet, 20%RH, leather-soled shoes)

There are at least four ways of controlling ESD:

1. Make materials more electrically conductive by adding metallic oxides or metal particles to a monomer mix.
2. Copolymerization of an anti-static resin with the base polymer.
3. Use of topical additives such as fatty amines and high molecular weight alcohols.
4. Use of static eliminating devices such as static free work station, deionizing air blowers, static monitoring devices, etc. Refer to the table at the end of this article for a more complete listing of anti-static materials.

In addition to using anti-static materials it is also important to develop preventive handling procedures that are understood by everyone who

continued on page 10

works with discrete components. An ESD program might begin by flagging or categorizing static sensitive parts, followed by a comprehensive, user-oriented set of handling procedures.

Commonly available anti-static materials for handling, shipping and storing static sensitive components include:

Work Station and Accessories:

1. Work stations – Portable or individual type; industrial type
2. Accessories – Wrist straps, sleeve protection, seat or stool covers, leg/foot grounding device, heel protector, grounding carts, floor mats, table tops, gloves, conductive shoe covers, work surface cleaners and topical antistats.

Packaging and Shipping Devices

DIP shipping tubes, vials/bottles, shorting bars, styro-coated boards, conductive shipping boxes, document elements, masking film, tote boxes, antistatic carriers for microcircuits, bucket and drum liners, and conductive rollers.

Static Monitoring Devices

Static meters, static scanners (unichannel and multichannel audio-visual alarm systems), portable static locators, static decay meters, electrostatic voltmeters, high-voltage power supply/amplifier/controller (monitors corona charging and discharging techniques and closed loop charge control systems) and electrostatic discharge simulators.

Static Eliminating Devices

Ionizing air blowers, guns and nozzles, conductile (static conductive floor tiles), static free desoldering tools and static protected carpets.

For more information about ESD protection devices, contact **Bella Geotina (78-552), ext. 2471.**

Multitone ceramic buzzer element

A new **multitone** piezoelectric ceramic buzzer element is now available from the Electronic Components Division of Panasonic Company. Designated as "EFB-S19A01CE," the new element represents a state-of-the-art advance in buzzers because it can generate a number of tones, depending on the applied signal frequency. Previously, similar buzzers offered a single tone output.

The new element will produce an SPL (sound pressure level) between 80 and 95 dB over a frequency range of 500 to 5000 Hz when driven by a 10-volt peak-to-peak square wave at a point 10 cm away from the element. Other specifications include resonant frequency of 1.9 KHz, resonant impedance of 480 ohms maximum, electrostatic capacitance of 70,000 pF (at 0.12 KHz), and it can be operated by a 6-volt peak-to-peak input voltage. The dimensions of the new element are: 35 mm (1.378 inches) diameter and thickness of just 1 mm (0.0394 inches).

The deliveries of the EFB-S19A01CE buzzer elements are 60 to 90 days. In production quantities, the elements sell for 40 to 50¢ each.

Byron Witt
78-552, ext. 2479

Universal DC motor mass test system

In the past, mass testing of DC motors was a difficult task. Individual drive circuits, supplies and control circuits were set up for each motor tested. This was usually accomplished by acquiring an instrument to drive each motor — a costly and sometimes impossible feat. To overcome this problem a mass test system was set up in Electromechanical Component Engineering to life test DC motor assemblies.

This system was made as flexible as possible to allow a variety of different DC motors to be operated from it. The complete system consists of a control module, drive circuits and test motor monitor circuit.

The control module is the heart of the test system. It produces the control signal which will represent the actual test motor velocity profile. The motor velocity will follow this control signal, given the proper supply voltage and current to the system. The module can produce up to three different velocity profile modes in a repetitious sequence. Two of the modes cause the motor to operate in a forward direction while the remaining mode forces it to run in a reverse direction. Any or all of these velocity profile modes may be manually programmed in sequence for life testing or evaluation procedures.

The test motors can be manually programmed to operate in each mode for a period of one to one thousand seconds before proceeding to the next velocity mode. After all the programmed modes have been completed, the cycle is automatically repeated until the system is shut down. The control signal amplitude, which is directly related to motor velocity, can be varied for all modes simultaneously or one mode can be decreased by itself, allowing two speeds per cycle.

Each of the three modes can be individually programmed to operate motors continuously or intermittently. On/off times in the intermittent mode may be manually programmed for periods of ten to one thousand milliseconds (see Figure 1). The rise and fall times of the forward and reverse intermittent velocity profile may each be manually programmed between ten and one thousand milliseconds.

The idea behind the variable control module is to easily simulate (at worst case conditions) the majority of DC motor operating modes that would be required for any instrument application.

The second part of the testing station, the drive circuit assembly, forces all test motors to follow a velocity profile equal to that of the

continued on page 12

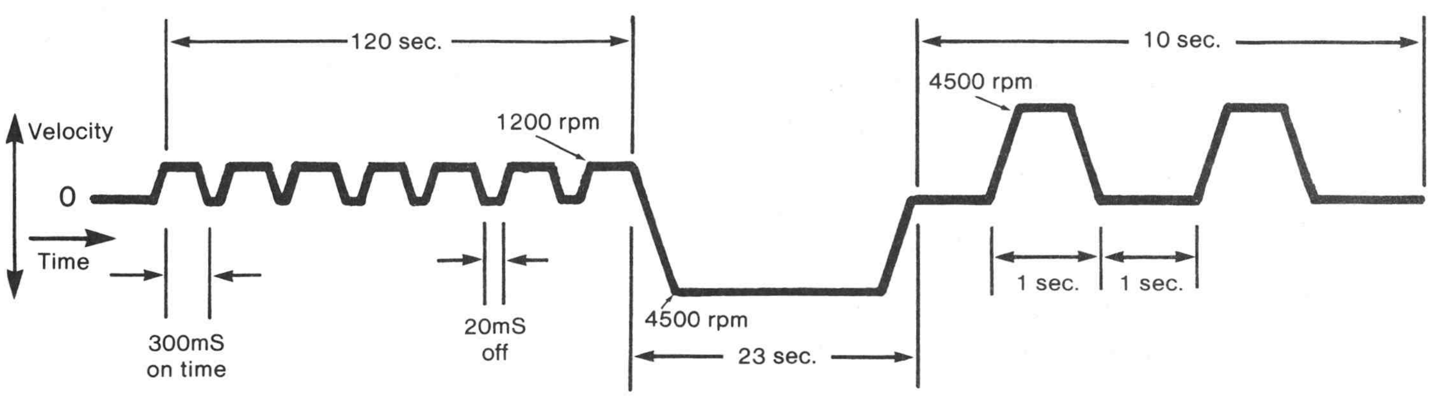


Figure 1 — Typical velocity vs. time cycle used to life test DC Servo motors

control module signal, regardless of torque loading on motor output shaft. Each circuit has the capability of driving a 25 volt DC motor requiring a maximum of five amps current. The current limit can be adjusted per the individual motor requirements. The circuits are built on removable vector boards allowing easy replacement and troubleshooting of components without affecting other drives.

It was necessary to use a closed loop bipolar drive scheme for the circuit design to force fast acceleration and deceleration of the high speed Servo motors. The back electromotive force (BEMF) of each test motor was used for feedback, allowing virtually unlimited flexibility in the type of DC motor that can be driven, whether it has an external feedback system or not. Minor manual adjustment of the voltage and BEMF feedback gains and circuit bandwidth characteristics will allow basically any DC motor to be driven. At present the drivecard cage assembly will allow ten motors to be driven per control signal.

The third part of the test station is the motor monitoring portion, which consists of a circuit that separates the BEMF voltage from the supply voltage. The BEMF is used for monitoring purposes because it is directly proportional to motor velocity. The BEMF along with motor supply voltage and control signal are the major waveforms necessary to monitor the complete test system (see Figure 2).

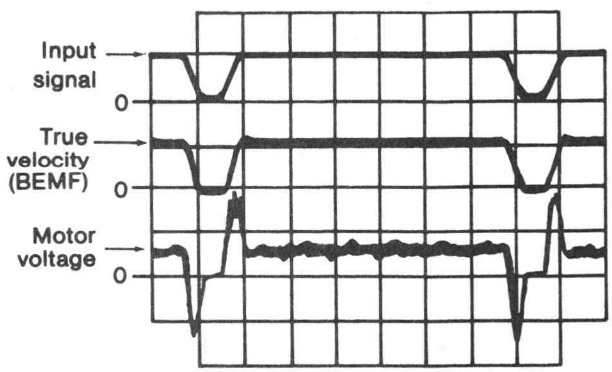
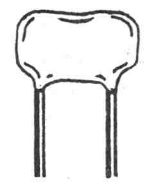


Figure 2 — Typical test monitor curves

This system is presently being used for life testing DC micromotors. Work is also underway to develop another test system to determine galvanometer (Penmotor) linearity specs. If you would like more details concerning motor evaluation and testing, please contact **Bill Stadelman (78-552), ext. 2466.**

Mica capacitor availability

Through the years Tek has had two main suppliers of mica capacitors. About 18 months ago one of those suppliers went out of business causing serious availability problems — a delivery time of 33 weeks was not unusual. Molded mica capacitors (which Tek still uses) were in even higher demand than dipped micas. In the last year and a half many suppliers have been evaluated, and the availability is considerably better today. Wherever possible, the use of molded mica capacitors at Tek has been converted to dipped mica. We now have four suppliers approved, and others are still being considered.



Users of dipped mica capacitors should be aware that silver is used in the construction of these parts, and that makes us subject to silver price adders. At least one company is imposing silver price adders on their mica capacitors today.

If you have any questions concerning molded mica capacitor replacements or dipped mica capacitor suppliers (present or future), please call **Alan LaValle at 78-552, ext. 2538.**

COMPONENT CHECKLIST

The "Component Checklist" is intended to draw attention to problems or changes that affect circuit design. This listing includes: catalog and spec changes or discrepancies; availability and price changes; production problems; design recommendations; and notification of when and how problems were solved. For those problems of a continuing nature, periodic reminders with additional details will be included as needed.

Tek P/N	Vendor	Description of part	Who to contact, ext.
✓ **290-0425-00**	**Union Carbide**	**100μF, 20V tantalum cap**	**Don Anderson, 2545**

This part is a hermetically sealed, axial lead tantalum capacitor that is built to have low ESR at high frequencies. We use many of these as filters in switching power supplies. The 100KHz ESR spec is 0.06Ω maximum, and for the last year (and perhaps longer) most of the parts we received were between 0.06Ω and 0.08Ω. It appears that the manufacturers cannot meet the original ESR spec. We are considering raising our ESR spec to 0.08Ω maximum to make it correspond with reality. If this will cause any problems, please contact me.

We now pay close to $3 for this part, and it could approach $4 by the end of this year. It is possible to replace this tantalum cap with an aluminum that is slightly larger, has about the same ESR and costs about $0.45. Two good prospects are the 290-0800-00 (250μF, 20V) and the 290-0932-00 (390μF, 15V).

Tek P/N	Vendor	Description of part	Who to contact, ext.
✓ **290-0726-00**	**Sprague**	**220 μF, 10V dipped tantalum cap**	**Don Anderson, 2545**

This capacitor has been used in filter and bypassing applications because its 100KHz ESR was typically under 0.10Ω. Recently, tantalum cap manufacturers started using higher CV tantalum powder which makes smaller and cheaper caps that also have higher ESR. These caps are now arriving with 0.20Ω to 0.40Ω high-frequency ESRs. The chances of getting caps with the original low ESRs are finite, but small. This part could be replaced with the 290-0932-00 (390μF, 15V, 0.5" X 1"), or the 290-0800-00 (250μF, 20V, 0.5" X 1") which are larger aluminum electrolytics, but have a lower ESR.

This problem of worsening ESRs may show up in many other tantalum parts, so you should look at all tantalum applications where low ESR is critical and consider replacing them with low-ESR aluminums (listed as "high ripple" is the Resistor/Capacitor Parts Catalog).

Tek P/N	Vendor	Description of part	Who to contact, ext.
✓ **175-1020-00** **175-0284-00**	**ITT Surprenant**	**50Ω coaxial cable**	**Elizabeth Doolittle, 2550**

These 50Ω coax cables are UL Style 1354, which is rated for 60°C and 30V RMS. This temperature rating is not high enough for many applications where the instrument will be UL approved.

A good substitute for these part numbers is 175-1020-09, a 50Ω coax, UL Style 1435. This coax is rated at 80°C, 300V RMS. It also has the same electrical properties but slightly larger diameter than those listed above.

continued on page 14

Tek P/N	Vendor	Description of part	Who to contact, ext.
No Tek P/N	Texas Instruments	9914 GPIB chip	Jim Howe, 2566

An earlier Component Checklist note about the 9914 (CN#275 page 10) outlined a potential problem with disabling an ACDS-holdoff function by masking the associated interrupt status bit. The suggested procedure is not guaranteed to prevent problems on the bus, however.

The ACDS-holdoff interrupt status bits are set whenever the appropriate command is on the bus and the chip is in ACDS. The interrupt status bits are set even though the interrupt status bit is set while the interrupt mask bit is one. The ACDS-holdoff will not be released by clearing the interrupt mask bit.

If the ACDS-holdoff function is to be disabled by masking the interrupt, it is essential that the 9914 be in ACDS-holdoff when the change in the interrupt mask is to be made. The reason is that the chip may already have reached ACDS-holdoff for a certain function when that function is disabled; however, the chip will remain in ACDS-holdoff because masking the interrupt does not allow the bus to proceed. Also, once a particular function is masked, it is not possible to determine from reading the 9914 registers whether or not the chip is in ACDS-holdoff for that function.

Therefore, the two choices for using the interrupt mask register for disabling an ACDS-holdoff function are as follows:

a. Establish the mask bits for the ACDS-holdoff functions once only, during initialization.

b. Alternatively, the mask bits may be cleared, but **only** when the bus is known to be frozen; for example, when servicing an ACDS-holdoff interrupt, or 'B1,' or 'B0.'

The ACDS-holdoff functions may be enabled at any time without chip malfunction.

ComponentNews **NewComponents**

Vendor	No.	Description	When Available	P/N	Approx. Cost	Engineer to contact
		analog devices				
Analog Devices	—	AD542J, Precision BiFET op amp, V_{OS} = 2mV max.	now	156-1492-00	$ 2.00	Willie Rempfer, 2539
PMI, Micro Power Systems	—	OP-10, dual matched instrumentation op amp	now	—	11.00	Willie Rempfer, 2539
		optoelectronic and passive devices				
TEC LITE	SS1L-C05-EL12-Y	LED, lamp, green, shielded w/hardware	now	150-1085-00	—	Betty Anderson, 2549
TEC LITE	SS1L-A05-EL02-Y	LED, lamp, red, shielded w/hardware	now	150-1086-00	—	Betty Anderson, 2549
Dialight	559-0201-003	LED, lamp, green, T1 size, with snap-in housing, wire leads	now	150-1089-00	—	Betty Anderson, 2549
Dialight	550-2406	LED, lamp, high brite red, looks around corners P.C. mount	now	150-1090-00	—	Betty Anderson, 2549

IMPORTANT NOTICE: New FCC Regulations

The Computer Business Equipment Manufacturer's Association (CBEMA) legal staff has advised us that the FCC commissioners have agreed to the following changes to the Docket No. 20780 FCC regulations recently imposed on our products.

1. Exemption of Products

All industrial test equipment, medical equipment, household appliances and process control equipment have been removed from this docket and will be covered under future FCC rule making sometime in the next three to five years.

All Tektronix test and measurement products are presently considered industrial test equipment.

IDG products are presently the only class of equipment covered by this regulation.

2. Extension of compliance date (for products covered by this regulation)

Products in production prior to October 1981, and produced before September 1983, are not required to be in compliance.

New products introduced after October 1981, must be in compliance.

All applicable products produced after September 1983, must be in compliance.

Equipment covered by this regulation that does not comply by January 1, 1981, must be labeled as such, even though compliance is not required.

3. Label Changes

The word "harmful" has been replaced with the word "undesirable."

4. Marketing Rules

Computing devices are exempt from FCC marketing rules.

For additional information please contact me on ext. 7887.

Herb Zajac
Environmental Laboratories

Implosion shield quality problems

Due to increasingly high scrap dollar costs encountered during the manufacture of implosion shields (approximatley $7,100 in AP009), it has become increasingly necessary to establish company-wide standards for allowable contamination and specks. Several product groups have indicated the CRT faceplate quality specifications would be a reasonable guideline for implosion shields. Therefore, the following specifications (CRT Process Spec. No. 8-0458) are in-line with our present inspection criteria and will be used as plastics quality standard for the manufacture of implosion shields.

Defect	Equivalent Diameter	Inside quality area		Outside quality area*	
		Maximum Number Allowed	Minimum Separation	Maximum Number Allowed	Minimum Separation
Black specks, contaminants, spots	0.015" - 0.020"	0	——	6	0.250"
	0.010" - 0.015"	0	——	6	0.500"
	0.005" - 0.010"	3	0.500"	10	0.500"
	Max. #over 0.005"	3	0.500"	10	0.500"
	Under 0.005"	Disregard unless of such density to be considered a cloud.			

*This area is not visible with shield installed in instrument.

New inspection equipment will be purchased to standardize the inspection procedures according to the above specifications.

Please direct any comments or questions to **Bob Luka, ext. 7216 (Vancouver).**

component news

Component News is published by Technical Communications (58-122)

Jacquie Calame, editor
Lola Janes, typesetting
Loretta Clark, paste-up/graphics

To submit an article, contact Jacquie on ext. 6867.
For mailing list changes, contact Kelly Turner on ext. 5502.