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Instructions

12RM01
8080 MNEMONICS ROM PACK

The 8080 Mnemonics ROM Pack configures a 1240 Logic Analyzer to acquire and disassemble data from an 8080 microprocessor. A Probe Interface (Option 01) makes connection to the microprocessor easy and arranges the lines for use with the setup from the ROM Pack.

NOTE

To use this ROM Pack, your 1240 Logic Analyzer must be equipped with at least two 1240D2 cards.

Insert this manual at the back of your *1240 Logic Analyzer Operator's Manual*, or in the 1240 Optional Accessories binder.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL

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OVERVIEW

THIS MANUAL

This manual describes how the 8080 Mnemonics ROM Pack configures the 1240 Logic Analyzer for use with 8080 microprocessors, how to connect the 1240 to the 8080, and how to acquire data and display it. It also describes the four data display formats available when an 8080 Mnemonics ROM Pack is installed in your 1240 and how you can get a printout of these state table displays.

OTHER MANUALS

To use the 8080 Mnemonics ROM Pack, you should be familiar with the operation of the 1240 Logic Analyzer and the 8080 microprocessor. Refer to the *1240 Logic Analyzer Operator's Manual* and the operator's manual for any communication packs that you may be using, as well as the manufacturer's 8080 microprocessor manual.

OPTIONAL PROBE INTERFACE

Option 01 to the 8080 Mnemonics ROM Pack is a Probe Interface, that allows the 1240 to be easily connected to the 8080. An unconfigured probe interface can be ordered as a 40-pin Universal Probe Interface Kit (UPIK40).

ROM PACK INSTALLATION

MINIMUM CONFIGURATION

In order to acquire data from an 8080 microprocessor using the 8080 Mnemonics ROM Pack, it is necessary to have a 1240 Logic Analyzer equipped with at least two 1240D2 18-channel Data Acquisition Cards.

NOTE

The 8080 Mnemonics ROM Pack will not set up the 1240 or disassemble data when it is installed in a 1240 with less than two 1240D2 acquisition cards.

INSTALLING THE ROM PACK

CAUTION

Static Discharge can damage the semiconductor devices in a Mnemonics ROM Pack. Discharge static from a pack before installing it by momentarily laying the pack, label side up, on the top of the 1240.

To install the 8080 Mnemonics ROM Pack in your 1240 Logic Analyzer, locate the slot on the right side of the instrument, beneath the probe connectors. Insert the connector end of the ROM Pack, with the label up, past the hinged slot cover and into the memory pack connector. (The mechanical design of the pack ensures that it cannot be installed incorrectly.) Refer to Figure 1.

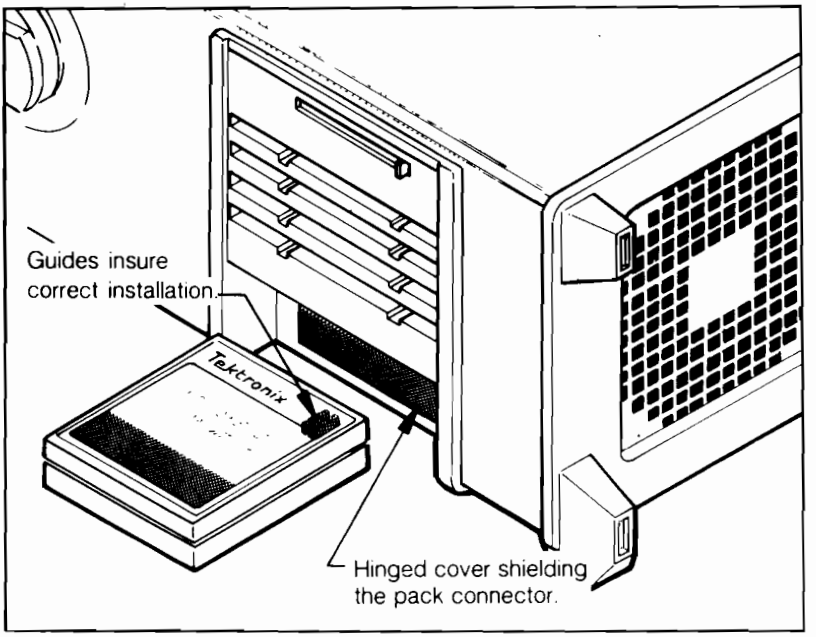

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Figure 1. Installing the ROM Pack in a 1240.

LOADING THE ROM PACK CONTENTS

NOTE

The 1240 should use the same power ground as the system under test. Otherwise, differences between system grounds may cause inconsistent acquisition.

If the 1240 has not been powered up, the contents of the ROM Pack will be loaded automatically at power-up. If the 1240 is on, enter the Storage Memory Manager menu, remove any other ROM Pack, install the 8080 Mnemonics ROM Pack, and press the LOAD NEW PACK soft key. The ROM Pack is now loaded.

CAUTION

Do not remove the ROM Pack while you are in any menu other than Storage Memory Manager. Removing it at any other time may cause complete disruption of the 1240's internal memory. To restore the 1240, turn it off and back on.

REMOVING THE ROM PACK

To unload the ROM Pack from the 1240, enter the Storage Memory Manager menu, pull the ROM Pack straight out of the 1240 (it is not necessary to power-down), and press LOAD NEW PACK.

CAUTION

After removing the ROM Pack, do not leave the Storage Memory Manager menu without pressing the LOAD NEW PACK soft key. Doing so may cause complete disruption of the 1240's internal memory. To restore the 1240, turn it off and back on.

CONNECTING TO THE 8080

CONNECTION OVERVIEW

Table 1 provides an overview of the connections between the 1240 Logic Analyzer equipped with an 8080 Mnemonics ROM Pack and your 8080 microprocessor.

NOTE

*Regardless of the connection scheme, be sure to connect a **USER'S GND** lead from each acquisition probe to the microprocessor ground (pin 2). Otherwise, invalid data may be acquired.*

TABLE 1
1240 SCREEN TO 8080 PINOUT MAP

1240 SCREEN			CONNECTIONS		8080	
GROUP	BIT	C/Q	POD*	CHAN	SIGNAL	PIN
CNTL	7	-	0	7	D7 (MEMR)	6
	6	-	0	6	D6 (INP)	5
	5	-	0	5	D5 (M1)	4
	4	-	0	4	D4 (OUT)	3
	3	-	0	3	D3 (HLTA)	7
	2	-	0	2	D2 (STACK)	8
	1	-	0	1	D1 (/WO)	9
	0	-	0	0	D0 (INTA)	10
ADDR	15	-	3	7	A15	36
	14	-	3	6	A14	39
	13	-	3	5	A13	38
	12	-	3	4	A12	37
	11	-	3	3	A11	40
	10	-	3	2	A10	1
	9	-	3	1	A9	35
	8	-	3	0	A8	34
	7	-	2	7	A7	33
	6	-	2	6	A6	32
	5	-	2	5	A5	31
	4	-	2	4	A4	30
	3	-	2	3	A3	29
	2	-	2	2	A2	27
	1	-	2	1	A1	26
	0	-	2	0	A0	25
DATA	7	-	0	7	D7	6
	6	-	0	6	D6	5
	5	-	0	5	D5	4
	4	-	0	4	D4	3
	3	-	0	3	D3	7
	2	-	0	2	D2	8
	1	-	0	1	D1	9
	0	-	0	0	D0	10
(none)	-	P0	0	C/Q	SYNC	19
	-	P1	1	C/Q	DBIN	17
	-	P2	2	C/Q	/WR	18
	-	P3	3	C/Q	HLDA	21

* Pod numbers are shown for a 1240 with a total of two acquisition cards installed. For each additional acquisition card installed, add 2 to the pod numbers given.

The first two of the following subsections are for those who purchased an Option 01 with their 8080 Mnemonics ROM Pack (12RM01 Option 01). The third subsection is intended for those who did not purchase an 8080 Probe Interface along with their ROM Pack, while the fourth is for those who have subsequently purchased a 40-pin Universal Probe Interface Kit (UPIK40).

CONNECTING THE PROBE INTERFACE TO THE 8080

If you ordered Option 01, your 8080 Mnemonics ROM Pack came with an 8080 Probe Interface. Connect the 40-pin DIP clip end of the 8080 Probe Interface to the 8080 microprocessor. Be sure to connect pin 1 of the DIP clip to pin 1 of the microprocessor. Pin 1 of the 8080 Probe Interface DIP clip is identified with an arrow.

NOTE

Failure to connect pin 1 of the Probe Interface to pin 1 of the 8080 will result in acquisition of meaningless data.

CONNECTING THE 1240 TO THE PROBE INTERFACE

Connect two data acquisition probes to each of the two 18-channel data acquisition cards used by the 8080 Mnemonics ROM Pack. (The ROM Pack uses the 1240D2s in the highest-numbered slots of the 1240.) Remove the lead sets from these probes.

NOTE

The 1240 should use the same power ground as the system under test. Otherwise, differences between system grounds may cause inconsistent acquisition.

Now attach these probes to the 8080 Probe Interface. Turn on the 1240 (if it is not already on) and use the ID button to identify one of the probes connected to the two highest-numbered 18-channel cards. Connect that probe to the 8080 Probe Interface lead set with the correct label as indicated by Table 2. Repeat this procedure for each probe. Also, connect the ground leads from all four probes to the ground ring on the black wire.

TABLE 2
PROBE TO 8080 PROBE INTERFACE CONNECTIONS

8080 Probe Interface Lead Set Identifiers		1240 Pod I.D. Number for various configurations		
1240	(DAS)	2 Acq. Cards	3 Acq. Cards	4 Acq. Cards
0	(1A)	0	2	4
1	(1B)	1	3	5
2	(1C)	2	4	6
3	(2A)	3	5	7

NOTE

Be sure to connect a USER'S GND lead from each acquisition probe to the black wire with the ring on it (microproceesor ground). Otherwise, invalid data may be acquired.

IF YOU DO NOT HAVE A PROBE INTERFACE

If your 8080 Mnemonics ROM Pack does not include an Option 01 Probe Interface, connect the pins from the microprocessor to the 1240D2 pod channels as shown in Table 3.

NOTE

Be sure to connect a USER'S GND lead from each acquisition probe to the microprocessor ground (pin 2). Otherwise, invalid data may be acquired.

TABLE 3
8080 PINOUT WITH POD AND CHANNEL ASSIGNMENTS

1240 Pod*-Channel	Signal Name	8080 Pin Numbers		Signal Name	1240 Pod*-Channel
P3-2	A10	1	40	A11	P3-3
USER'S GNDs	GND	2	39	A14	P3-6
P0-4	D4	3	38	A13	P3-5
P0-5	D5	4	37	A12	P3-4
P0-6	D6	5	36	A15	P3-7
P0-7	D7	6	35	A9	P3-1
P0-3	D3	7	34	A8	P3-0
P0-2	D2	8	33	A7	P2-7
P0-1	D1	9	32	A6	P2-6
P0-0	D0	10	31	A5	P2-5
n.c.	−5 V	11	30	A4	P2-4
n.c.	RESET	12	29	A3	P2-3
n.c.	HOLD	13	28	+12 V	n.c.
n.c.	INT	14	27	A2	P2-2
n.c.	$\phi 2$	15	26	A1	P2-1
n.c.	INTE	16	25	A0	P2-0
P1-Q/C	DBIN	17	24	WAIT	n.c.
P2-Q/C	$\overline{WR}$	18	23	READY	n.c.
P0-Q/C	SYNC	19	22	$\phi 1$	n.c.
n.c.	+5 V	20	21	HLDA	P3-Q/C

* Pod numbers are shown for a 1240 with a total of two acquisition cards installed. For each additional acquisition card installed, add 2 to the pod numbers given.

IF YOU BUY A UPIK40

If you purchase a 40-pin Universal Probe Interface Kit (UPIK40), it should be assembled so the connections correspond to the information shown in Table 4. You should label the lead sets in the UPIK40 with pod numbers appropriate to your 1240. Note that Table 4 contains pod numbers that are only appropriate if your 1240 has two 18-channel cards and no others. If your 1240 has more acquisition cards, add 2 to the pod number for each additional card.

TABLE 4
PROBE INTERFACE CONNECTIONS*

1	Pod 3 — red	Pod 3 — orange	40
2	Ground ring	Pod 3 — blue	39
3	Pod 0 — yellow	Pod 3 — green	38
4	Pod 0 — green	Pod 3 — yellow	37
5	Pod 0 — blue	Pod 3 — violet	36
6	Pod 0 — violet	Pod 3 — brown	35
7	Pod 0 — orange	Pod 3 — black	34
8	Pod 0 — red	Pod 2 — violet	33
9	Pod 0 — brown	Pod 2 — blue	32
10	Pod 0 — black	Pod 2 — green	31
11		Pod 2 — yellow	30
12		Pod 2 — orange	29
13			28
14		Pod 2 — red	27
15		Pod 2 — brown	26
16		Pod 2 — black	25
17	Pod 1 — white		24
18	Pod 2 — white		23
19	Pod 0 — white		22
20		Pod 3 — white	21

* Pod numbers are shown for a 1240 with a total of two cards installed. For each additional card installed, add 2 to the pod numbers given. Connections are shown from the wire insertion side of the male-to-female harmonica adapter.

THE SETUP SUPPLIED BY THE ROM PACK

When the 8080 Mnemonics ROM Pack is loaded into a 1240 with two or more 1240D2 cards, several things happen:

- The 1240 enters Operation Level 2, ADVANCED STATE ANALYSIS. If you manually leave level 2 for levels 0 or 1, you will ruin the setup supplied by the ROM Pack. (Using level 3 will not cause a problem.)
- All 1240D2 chaining is turned off.
- The thresholds are set to TTL on the two 1240D2s used by this ROM Pack.
- All polarities are set to 1 (positive - true) on the two 1240D2s used by this ROM Pack.
- T2 is redefined as DEMUX. See *Timebase Definitions* later in this manual.
- The lowest-numbered pod (of the first 1240D2 being used by the ROM Pack) is clocked by T2 F and used to acquire the CNTL group. These control signals are demultiplexed from the microprocessor's data lines. Both the input radix and the display radix for the CNTL group are set to BINary.
- The other three pods used by the ROM Pack are clocked by T2 L and their radices are set to HEXadecimal. These pods are used to acquire the ADDR and DATA groups.
- Channel 8 of the lowest-numbered pod used by the ROM Pack is reserved for use by the 1240 in postprocessing the acquired data. Do not attempt to use or reassign this channel.

NOTE

If you attempt to use the 8080 Mnemonics ROM Pack in a 1240 that does not have at least two 1240D2s, the 1240 setup will not be modified.

Table 5 summarizes the way the 8080 ROM Pack sets up the last two 18-channel cards in the 1240.

TABLE 5
HOW THE 8080 ROM PACK SETS UP THE 1240

GROUP	TIME BASE	INPUT RADIX	DISPLAY RADIX	THRESHOLD, POLARITY	POD*: CHANNELS
CNTL	T2 F	BIN	BIN	TTL, all +	**0**: 7-0
ADDR	T2 L T2 L	HEX HEX	HEX HEX	TTL, all + TTL, all +	**3**: 7-0 **2**: 7-0
DATA	T2 L	HEX	HEX	TTL, all +	**1**: 7-0

* Pod numbers are shown for a 1240 with a total of two acquisition cards installed. For each additional acquisition card installed, add 2 to the pod numbers given.

MENU AND DATA DISPLAY DIFFERENCES

- The Timebase, Memory Config, and Channel Grouping menus are set up as shown in Table 5. Do not change these settings except as described in the subsection, *What You May Change*.
- Every menu that uses groups contains the CNTL, ADDR, and DATA groups set up by the ROM Pack.
- If a 1200C01 RS232C or a 1200C11 Parallel Printer COMM Pack is installed, the COMM PORT CONTROL menu is replaced by the LINE PRINTER OUTPUT menu. Line printer operation is described later in this manual.
- The STATE TABLE soft key label changes to 8080 STATE TABLE while you are in the State Table display menu.
- Also in the State Table display, GLITCHES ON/OFF is replaced by a FORMAT select field. This is where you choose a data display format. The choices are STATE, ABSOLUTE, HARDWARE, and SOFTWARE. The differences between these formats are discussed in detail later in this manual. You can still make the choice of GLITCHES ON or GLITCHES OFF in the Timing Diagram menu; the State Table display will reflect that choice.
- In the Timing Diagram display, the active cursor value at the bottom of the display is shown in STATE, ABSOLUTE, or HARDWARE format depending on the selection made in the State Table display menu. (If you select SOFTWARE disassembly in the State Table display menu, readouts in the Timing Diagram will appear in HARDWARE format.)

TIMEBASE DEFINITIONS

The 8080 ROM Pack sets up the 1240 to use Timebase 2 in the DEMUXed mode. T2 F is then used to store the 8080 status byte in the CNTL group, and T2 L is used to store the information for the ADDR and DATA groups. Timebase T2 F is set up to be the *falling* edge of SYNC qualified by ANDing with HLDA = 0. Timebase T2 L is set up to be the ORed *falling* edges of /WR and DBIN qualified by ANDing with HLDA = 0. Refer to Table 6.

TABLE 6
DEFAULT SETUP OF CLOCK QUALIFIERS

Clock Qualifier	Pod Number			T2 F		T2 L	
	2 Acq. Cards	3 Acq. Cards	4 Acq. Cards	ORed Clock	ANDed Qual.	ORed Clock	ANDed Qual.
SYNC	0	2	4	falling			
DBIN	1	3	5			falling	
/WR	2	4	6			falling	
HLDA	3	5	7		low		low

DMA Cycles. The default Timebase definitions just described prevent the acquisition of Direct Memory Access cycles by the AND HLDA = 0 qualification. If you want to store DMA cycles, you may change the qualification of the T2 F and T2 L timebases in the TIMEBASE menu. Qualification on HLDA = 1 causes only DMA cycles to be stored, while no qualification on HLDA (blank, don't care), allows both DMA and non-DMA cycles to be stored. *HOWEVER*, DMA cycles are not distinquished from memory reads and writes by the ROM Pack, so correct disassembly is not guaranteed when you make any change from the default values.

Additional User Qualification. If your 1240 has more data acquisition cards than the required two 18-channel cards, you may use the additional clock/qualifier channels to further qualify Timebase 2. *HOWEVER,* correct disassembly is not guaranteed when you do this.

WHAT YOU MAY CHANGE

Much of the setup provided by the 8080 ROM Pack cannot be disturbed without seriously impairing the disassembly of your data, but you can safely make the following modifications:

- You may change radices anywhere, but your choices will be ignored in some display formats.
- You may reorganize the CNTL group; the ROM Pack will retain its own internal grouping for processing purposes.
- You may change the qualification of timebases T2 F and T2 L, but correct mnemonic disassembly will no longer be guaranteed.
- You may change anything having to do with timebase T1; the 8080 Mnemonics ROM Pack only uses T2.
- You may change the configuration or grouping of any acquisition cards not used by the ROM Pack (as long as you do not chain any of the 1240D2s). The 8080 Mnemonics ROM Pack uses only the two highest-numbered 1240D2 (18-channel) acquisition cards.

NOTE

Do not chain any 18-channel cards. Doing so disrupts the setup supplied by the ROM Pack.

STORING AND USING A MODIFIED SETUP

When you have created and verified a modified setup for your 1240 that is compatible with the Mnemonics ROM Pack, you can store it and retrieve it using the following procedures:

Storing a Modified Setup

- Go to the Storage Memory Manager menu (UTILITY key).
- Remove the Mnemonics ROM Pack.
- Install a RAM Pack, press LOAD NEW PACK, and store your setup (FILETYPE: SETUP, STORED IN: PACK).

Using a Modified Setup

- Go to the Storage Memory Manager menu (UTILITY key).
- Install your RAM Pack, press LOAD NEW PACK, and load the file containing the modified setup.
- Store that setup in the 1240's internal RAM (FILETYPE: SETUP, STORED IN: RAM).
- Remove the RAM Pack, install the Mnemonics ROM Pack, and press LOAD NEW PACK.
- Retrieve your modified setup from the 1240's internal RAM and proceed.

DATA QUALIFICATION AND TRIGGERING

IDENTIFYING CYCLE TYPES

To use either the Global or Sequential Event Recognizers effectively, you need to be able to identify cycle types. Cycle types are decoded from the channels of the CNTL group according to the relationships shown in Table 8. Table 7 gives the names of the signals in the CNTL group. These signals are output as the 8080 status byte and are demultiplexed from the data lines using the T2 F timebase.

TABLE 7
CNTL GROUP SIGNALS

CHAN.	SIGNAL NAME
7	MEMR
6	INP
5	M1
4	OUT
3	HLTA
2	STACK
1	/WO
0	INTA

TABLE 8
IDENTIFYING CYCLE TYPES

CYCLE TYPE	CNTL GROUP 7654 3210	HEX	NOTES
MEM WRITE	0000 0000	00	
STACK WRITE	0000 0100	04	
HALT ACK	0000 1010	0A	NEC 8080A only
I/O WRITE	0001 0000	10	
INT ACK	0010 0010	22	NEC 8080A only
INT ACK	0010 0011	23	INTEL 8080 only
I/O READ	0100 0010	42	
MEM READ	1000 0010	82	
STACK READ	1000 0110	86	
HALT ACK	1000 1010	8A	INTEL 8080 only
FETCH	1010 0010	A2	
* ? *	All Others	??	

SPECIFYING CYCLE TYPES

To specify a particular cycle type as a condition for data qualification or triggering, enter the values shown in Table 8 for that cycle type in the CNTL field of the event recognizer.

CNTL Group Modification. You may split up the CNTL group, or rearrange its channels, or change its radix, without affecting disassembly. The ROM Pack maintains for its internal use a version of the group as it originally set it up. This allows you to take individual channels out of the CNTL group or create your own sub-groups with names that suggest the sub-set of channels you include or the way you are using them. (Of course, reorganization of the CNTL group means that you can no longer use the values given in Table 8.)

8080 CYCLE TYPE DEFINITIONS

FETCH A memory read cycle in which an instruction opcode (the first byte of an 8080 instruction) is fetched for execution.

HALT ACK Indicates that the 8080 is in a halt state. No instructions are being executed. Neither the data nor address buses contain useful information during this type of cycle.

I/O READ A cycle in which data is read from an I/O port in response to an IN instruction. The port number appears on the lower 8 bits of the address bus. (The higher 8 bits of the address bus contain meaningless data.)

I/O WRITE A cycle in which data is written to an I/O port in response to an OUT instruction. The port number appears on the lower 8 bits of the address bus. (The higher 8 bits of the address bus contain meaningless data.)

INT ACK An interrupt acknowledge cycle. The value on the data bus is the opcode supplied by the external circuitry to cause handling of the interrupt. The address bus does not contain useful information during this cycle.

MEM READ Any cycle, other than an opcode FETCH or a STACK READ cycle, in which data is read from memory. An event recognizer set for MEM READ cycles can be modified to include stack operations by entering an X (don't care) in bit 2 of the default CNTL group. Similarly, FETCH cycles can be included by entering an X (don't care) in bit 5 of the default CNTL group.

MEM WRITE Any cycle, other than a STACK WRITE cycle, in which data is written to memory. An event recognizer set for MEM WRITE cycles can be modified to include stack operations by entering an X (don't care) in bit 2 of the CNTL group.

STACK READ A memory read cycle in which data is retrieved from the system stack.

STACK WRITE A memory write cycle in which data is placed on the system stack.

*** ? *** An illegal cycle type; an unrecognized combination of control channels. This may indicate a misconnected or defective 8080 Probe Interface, or a setup which has been modified from what the ROM Pack created, or a real problem in your prototype.

DISPLAYING DISASSEMBLED DATA

INSTRUCTION MNEMONICS

This ROM Pack disassembles in the Intel 8080 mnemonics syntax used in the *MCS-80 USER'S MANUAL* by Intel Corporation (1977). Operands in disassembled instructions are always displayed in hexadecimal.

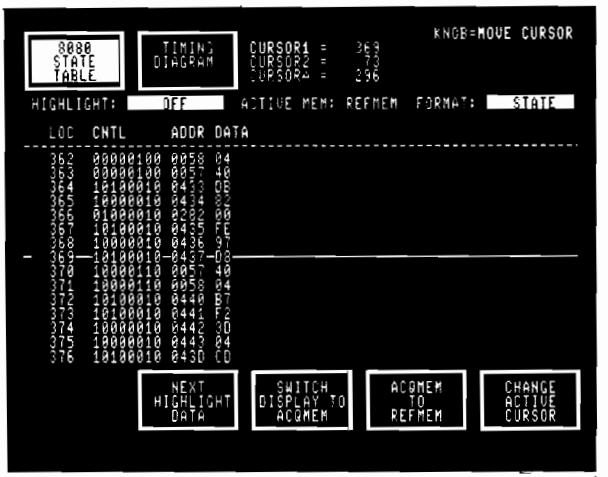
DISPLAY FORMATS

The mnemonics and cycle type information generated by the 8080 ROM Pack is available in the STATE TABLE display (accessed by pressing the DATA key). You have three choices of disassembly formats in addition to the standard state table display. You select the display format by placing the blinking field cursor in the FORMAT field and using the SELECT keys to indicate your choice.

NOTE

If you attempt to use the 8080 Mnemonics ROM Pack in a 1240 that does not have at least two 1240D2s, you will get an INSUFFICIENT 1240D2 CARDS TO SUPPORT DISASSEMBLY message in the State Table menu and only the (standard) STATE display format will be available.

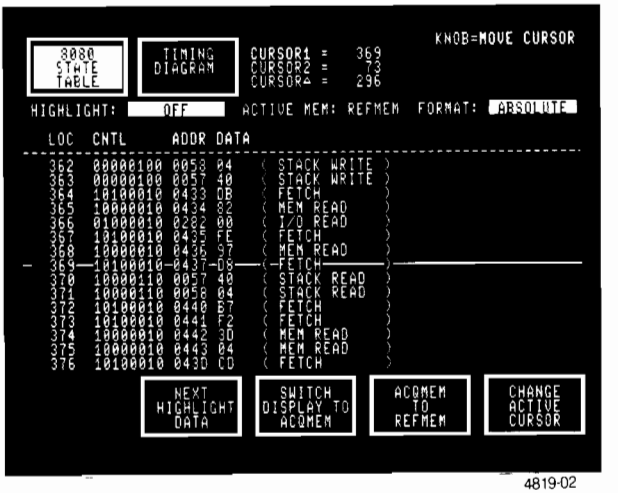
STATE. This is the standard 1240 State Table format that you get without the 8080 ROM Pack installed. This format is also the only one available in AUTO-RUN, when no T2 data is acquired, or when you have less than two 1240D2 cards installed (FORMAT field is not present). Look at Figure 2.



4819-01

Figure 2. STATE format is standard without the ROM Pack.

ABSOLUTE. This format is like the STATE format, but is enhanced by the addition of cycle type information. Look at Figure 3.



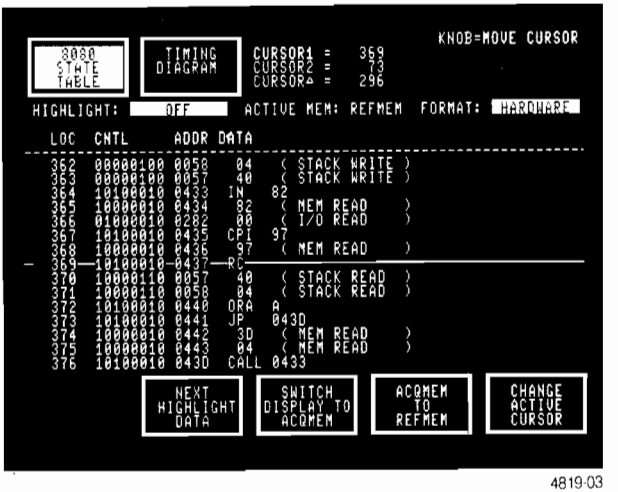
4819-02

Figure 3. ABSOLUTE format adds cycle type information.

HARDWARE. In this format, instruction mnemonics are displayed in the DATA group on opcode fetch cycles, and cycle type information is provided on all other cycles. Look at Figure 4.

NOTE

User choices of display radix are overridden in the HARDWARE display format. The ADDR and DATA groups are always shown in HEX. To see the data in these groups in your choice of radix, use the FORMAT select field to switch back and forth between this format and ABSOLUTE or STATE.



4819-03

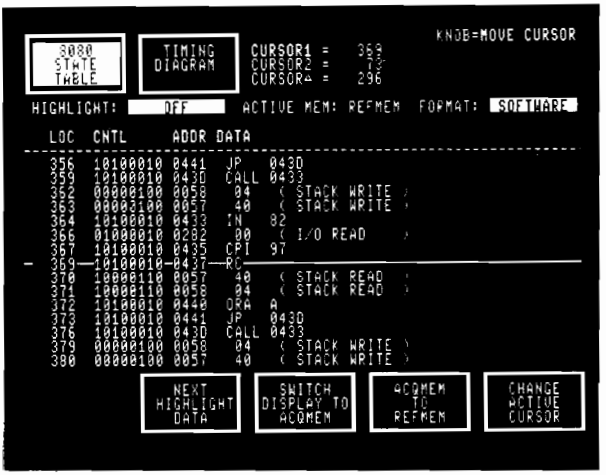
Figure 4. HARDWARE format shows instruction mnemonics.

SOFTWARE. This display format is designed to look like a source code listing and thus make analysis of the program flow easier. It is similar to HARDWARE except that the data for instruction read cycles that are not opcode fetches is suppressed and only the CNTL, ADDR, and DATA groups are available. (T1 groups and T2 groups from 18-channel cards that are not being used by the ROM Pack are suppressed.) Look at Figure 5.

Notice that the suppression of cycles resulting from the transition from any other format to SOFTWARE may cause the data cursors to move.

NOTE

User choices of display radix are overridden in the SOFTWARE display format. The ADDR and DATA groups are always shown in HEX. To see the data in these groups in your choice of radix, use the FORMAT select field to switch back and forth between this format and ABSOLUTE or STATE.



4819-04

Figure 5. SOFTWARE format suppresses non-fetch instruction reads.

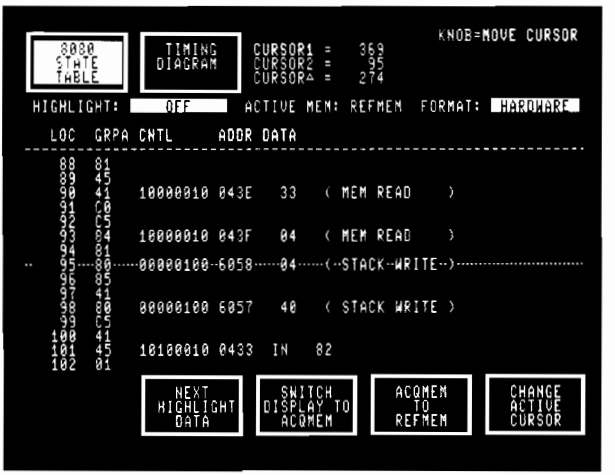
TIMING DISPLAYS

In the Timing Diagram menu, the active cursor value readout at the bottom of the data display reflects your choice of disassembly FORMAT in the State Table menu, with one exception: When you select SOFTWARE in the State Table menu, the readout in the Timing Diagram will be in HARDWARE format.

DUAL TIMEBASE DISPLAYS

As noted earlier in this manual, you may use T1 with any acquisition cards in your 1240 that are not used by the 8080 Mnemonics ROM Pack. The ROM Pack only uses the two 18-channel cards with the highest pod numbers, so you may use any lower-numbered 18-channel cards and any 9-channel cards in the instrument with T1.

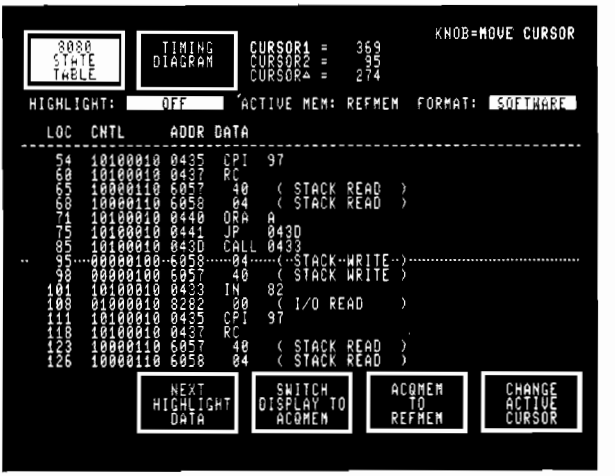
In the STATE, ABSOLUTE, and HARDWARE formats, the data acquired on T1 is correlated with the T2 F and T2 L data acquired from the 8080. Refer to Figure 6 to see T1 data correlated with 8080 data.



4819-05

Figure 6. T1 data correlated with 8080 data.

When you select SOFTWARE as the data display format, T1 data is suppressed in the interest of giving you the best possible overview of the 8080 program flow. Refer to Figure 7 and contrast it with Figure 6.



4819-06

Figure 7. T1 data is suppressed in SOFTWARE format.

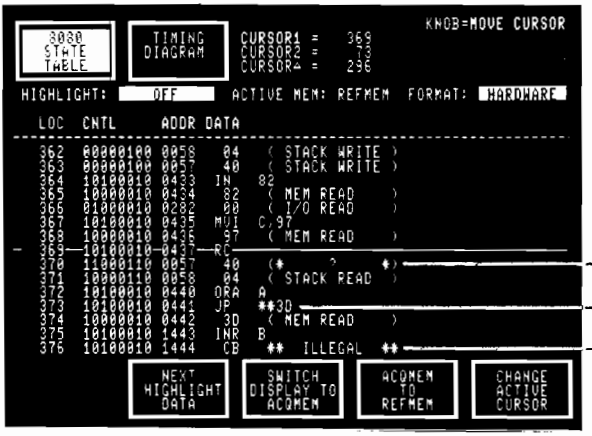
EDITING THE REFERENCE MEMORY

If you wish to edit the reference memory, you need to understand how the reserved channel (channel 8 of the first pod used by the 8080 Mnemonics ROM Pack) is used by the post-acquisition disassembly program. This channel will have a 1 stored in it only on cycles where the processor was reading the second or third bytes of a multi-byte instruction. By looking for these 1s, the 8080 Mnemonics ROM Pack program is able to locate instruction operands for disassembly and to suppress these non-opcode instruction reads in the SOFTWARE data display format.

If you edit your reference memory, and you want valid disassembly of the new memory that results, you may need to assign the reserved channel to a group and use the same rules for putting a 1 on this channel that the 8080 Mnemonics ROM Pack uses. The ROM Pack puts a 1 only on memory read cycles on consecutive addresses after an opcode fetch.

NON-STANDARD DISASSEMBLIES

When the 8080 Mnemonics ROM Pack encounters an unexpected combination of data, or when part of the data is missing, one of the indications shown in Figure 8 appears.



1 ***Illegal cycle type*** arises from an unexpected combination of control channel values. This indication can occur in every display format type except STATE. It can be caused by a misconnected or defective 8080 Probe Interface (or UPIK40), or a setup which has been modified and is no longer correct, or a problem with your system under test.

2 ***Missing data indication*** signals that part of the instruction was not stored in the acquisition memory. This can arise at the end of memory or when some sort of data qualification has prevented the complete storage of an instruction. This can also arise when the condition in a conditional call or return instruction was not satisfied. Whatever the cause, a single asterisk is displayed for each missing hexadecimal digit.

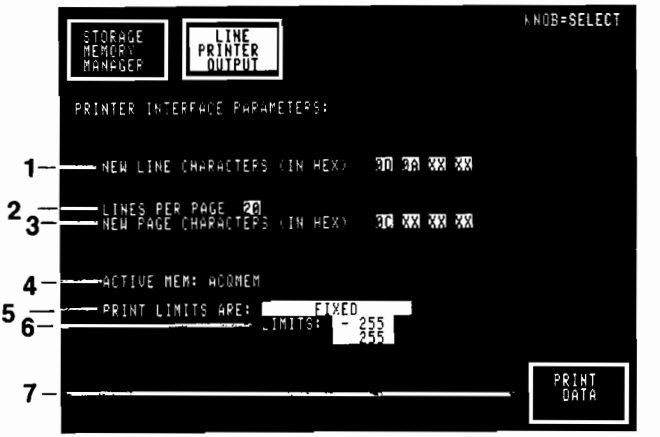
3 ***Illegal opcode fetch*** arises from an unexpected data bus value on an opcode FETCH cycle. This indication can occur in either HARDWARE or SOFTWARE display format. The erroneous opcode in the acquisition memory appears to the left of this label in the DATA group. This indication usually occurs when a problem in your software has caused an attempted execution at an erroneous address.

4819-07

Figure 8. Non-standard Disassemblies.

LINE PRINTER OUTPUT

When the 8080 ROM Pack is installed in a 1240 that also has a 1200C01 RS232C or 1200C11 Parallel Printer COMM Pack installed, the UTILITY menu presents a soft key labeled LINE PRINTER OUTPUT replacing the COMM PORT CONTROL key. The menu accessed by this key allows you to send your state data displays to a line printer in the current format. Refer to Figures 9 and 10.



1 NEW LINE CHARACTERS: Use these hexadecimal fields to define a string of from one to four characters that will be appended to each line. The first field must have an entry, but the last three fields can be filled with **X**s (don't cares).

2 LINES PER PAGE: Use this decimal field to specify the number of lines that will be printed on each page. Valid values range from 1 to 99.

3 NEW PAGE CHARACTERS: Use these hexadecimal fields to define a string of from one to four characters that will follow the end of every page. The first field must have an entry, but the last three fields can be filled with **X**s (don't cares).

4 ACTIVE MEM: This field is for information only. Change the active memory in the State Table or Timing Diagram menus.

5 PRINT LIMITS ARE: Use this field to indicate whether the area of active memory to be printed will be defined by FIXED LIMITS or BETWEEN CURSORS. When BETWEEN CURSORS is selected, the area of the active memory that will be printed is defined by the data cursors (inclusive).

6 LIMITS: This field becomes active when FIXED LIMITS is selected in the PRINT LIMITS ARE field. Entries here specify the first and last line of memory to be printed. When PRINT LIMITS ARE: BETWEEN CURSORS, this field displays the locations of the cursors.

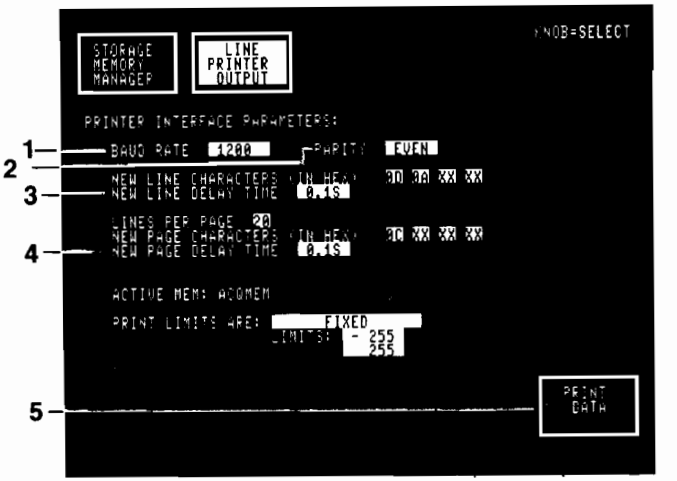
7 PRINT DATA: Touch this soft key to start the transmission of data. It will remain lighted during the transfer. Use the STOP key to interrupt the transmission, if necessary.

4819-08

Figure 9. LINE PRINTER OUTPUT menu when 1200C11 is installed.

NOTE

Do not attempt to control the 1240 remotely while any Mnemonics ROM Pack is installed.



1 BAUD RATE: Use this field to specify the baud rate at which the 1240 will supply data to the printer. The available choices are: 110, 134.5, 150, 300, 600, 1200, 2400, 4800, and 9600.

2 PARITY: Use this field to make parity choices of ODD, EVEN, and NONE.

3 NEW LINE DELAY TIME: Use this field to specify the minimum amount of time delay between the transmission of successive lines by the 1240. The choices range from NONE to 9.9 SEC in 100 ms steps.

4 NEW PAGE DELAY TIME: Use this field to specify the minimum amount of time delay between the transmission of the last line of one page and the first line of the next page. The choices range from NONE to 9.9 SEC in 100 ms steps.

5 PRINT DATA: Touch this soft key to start the transmission of data. Use the STOP key to interrupt the transmission, if necessary. This key places the 1240 ONLINE when the 1200C01 RS232C COMM Pack is installed. If the device being transmitted to is capable of transmitting back, spurious remote commands can affect the operation of the 1240. Also, during a PRINT DATA operation, the 1200C01 parameters are modified. Therefore, do not attempt to control the 1240 remotely while any Mnemonics ROM Pack is installed.

4819-09

Figure 10. LINE PRINTER OUTPUT menu when 1200C01 is installed. Refer to Figure 9 for a description of the fields that are the same in both menus. Refer to the *RS232C COMM Pack 1200C01 Operator's Manual* for information on handshaking protocols and the use of null modems.

ERROR MESSAGES

When used with an 8080 Mnemonics ROM Pack, the 1240 Logic Analyzer uses some error messages that are different from those it normally displays. Also, some of the normal error messages have additional meanings when they are used with this ROM Pack.

APPLYING SEARCH PATTERN - PLEASE WAIT — This message occurs briefly twice during a data acquisition with the 8080 Mnemonics ROM Pack installed, unless PATTERN SEARCH DISABLED is selected.

CONFIG ERROR — This message always appears in the State Table display after power-up with an 8080 Mnemonics ROM Pack installed. It indicates that the setup used to acquire the current acquisition memory and the current setup from the 8080 Mnemonics ROM Pack are inconsistent. Acquiring new data should make this message go away. (Refer to the *Reference Information* section of the *1240 Logic Analyzer Operator's Manual* for a complete discussion of this message.) This message also appears in the LINE PRINTER OUTPUT menu if the current configuration does not permit a PRINT DATA operation to be performed.

INSUFFICIENT 1240D2 CARDS TO SUPPORT DISASSEMBLY — This message indicates that your instrument does not have enough 18-channel cards to support the use of this Mnemonics ROM Pack.

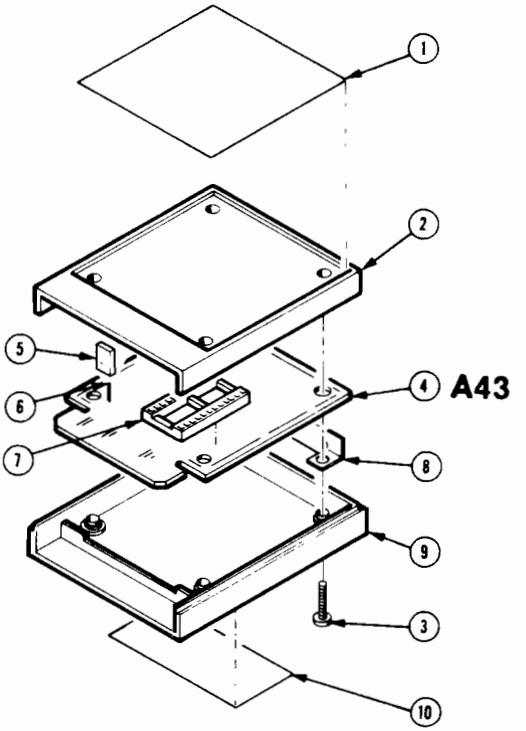
NO VALID DATA ACQUIRED — This message indicates that either no T2 data was acquired or that the acquired data was so heavily qualified that what was left of it disappeared during (SOFTWARE) disassembly.

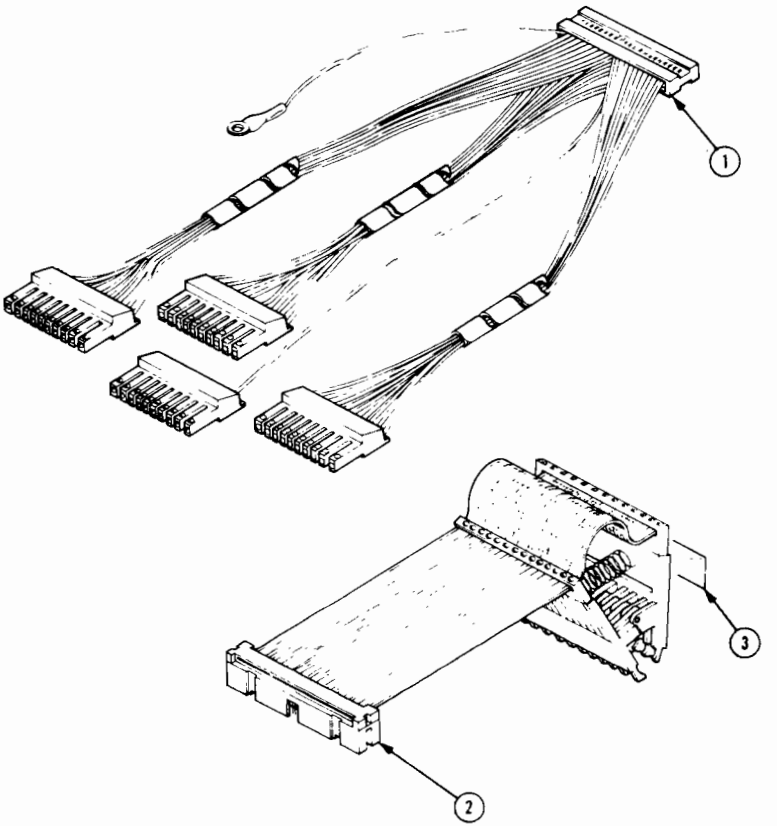
PRESS "STOP" TO TERMINATE OPERATION — This message tells you the correct way to stop a PRINT DATA operation. Since letting the printing operation finish or stopping it are your only choices once a printout is in progress, the 1240 assumes that you want to stop printing if you touch any key.

MEMORY TIMEBASE ASSIGNMENTS WILL NOT SUPPORT DISASSEMBLY — The memory being displayed cannot be disassembled because it was acquired with a setup that does not support disassembly. Go to the Storage Memory Manager menu and press LOAD NEW PACK to get a setup that will support disassembly. Then, acquire new data using that setup.

REPLACEABLE PARTS LIST
8080 MNEMONICS ROM PACK — 12RM01

NUMBER	TEK. P/N	DESCRIPTION
ELECTRICAL (REFER TO SCHEMATIC IN 1240 SERVICE MANUAL)		
A43	670-8172-00	CRT. BOARD ASSY: 32/64K MEMORY ROM PACK (U200, U300 EPROMs ARE NOT PART OF A43)
A43C100	281-0775-00	CAP, FIXED, CER, DI: 0.1 uF, 20%, 50V
A43C400	281-0775-00	CAP, FIXED, CER, DI: 0.1 uF, 20%, 50V
		CHASSIS PARTS
U200	160-2417-00	MICROCKT, DGTL: 16384 x 8 EPROM, PRGM
U300	160-2418-00	MICROCKT, DGTL: 16384 x 8 EPROM, PRGM
MECHANICAL (REFER TO EXPLODED VIEW DRAWING)		
1	334-0115-00	1 MARKER, IDENT: MKD 8080 ROM PACK
2	200-2503-01	1 COVER, ROM PACK: TOP
		(ATTACHING PARTS)
3	211-0012-00	4 SCREW, MACHINE: 4.40 x 0.375, PHD, STL
		— — * — —
4	- - - - -	CKT BOARD ASSY: 32/64K MEMORY ROM PACK (SEE A43 REPL)
5	131-0993-00	2 • BUS CONDUCTOR: 2 WIRE, BLACK
6	131-0608-00	6 • TERMINAL, PIN: 0.365 L x 0.025 PH BRZ GOLD
7	136-0755-00	2 • SKT, PL-IN ELEC: MICROCIRCUIT, 28 DIP
8	337-3122-00	1 SHIELD, ELEC: STATIC
9	200-2504-01	1 COVER, ROM PACK: BOTTOM
10	334-4727-00	1 MARKER, IDENT: MKD PROM PROGRAM IDENT
		STANDARD ACCESSORIES
	070-4819-00	MANUAL, TECH: INSTRUCTION


1
2
5
6
7
4
A43
8
9
3
10



REPLACEABLE PARTS LIST
8080 PROBE INTERFACE — 12RM01 OPTION 01

NUMBER	TEK. P/N		DESCRIPTION
MECHANICAL (REFER TO EXPLODED VIEW DRAWING)			
1	012-0998-00	1	LEAD SET, ELEC: 9.75 IN. LONG.
2	015-0015-00	1	TEST CLIP ASSY: 5.5 IN. LONG, 40 PIN
3	334-5328-00	1	MARKER, IDENT: MKD 8080