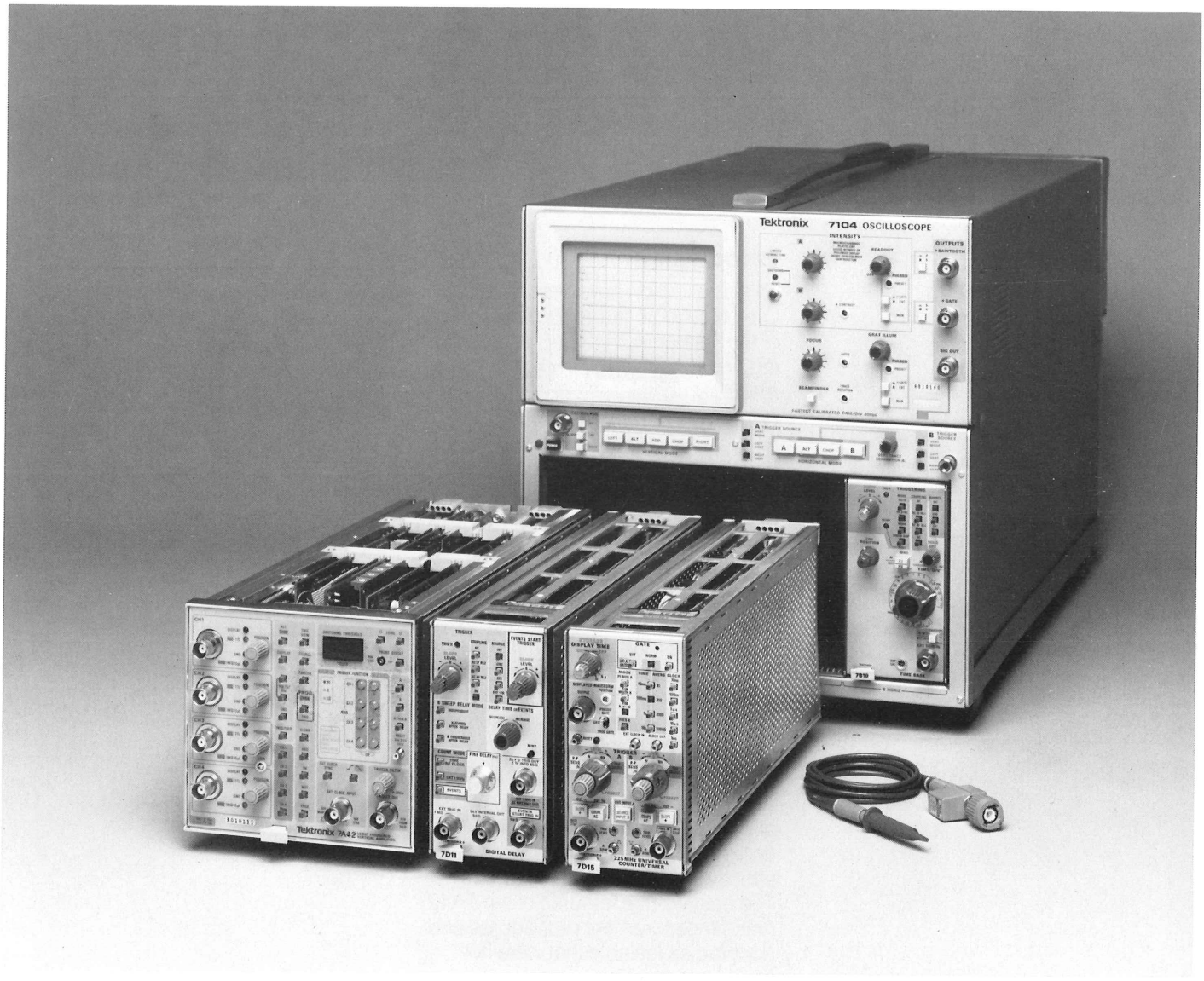
ADVANCED TRIGGERING TECHNIQUES



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Introduction

This application note describes the use of the logic triggering functions of the Tektronix 7A42 Logic Triggering Vertical Amplifier in digital timing measurements.

Limitations of conventional techniques

In digital systems, signal timing relationships are of the utmost importance. Traditional measurement techniques, using such instruments as logic analyzers and oscilloscopes do not, in many instances, offer the flexibility required in designing, evaluating, and maintaining these systems. The high or low information of the logic analyzer and the level and slope triggering of the oscilloscope limit the usefulness of both.

The 7A42 solution

Adding the flexible triggering system of the 7A42 to the high-resolution analog display of the oscilloscope effectively alleviates the problems. The easy-to-use features of the 7A42 make measurement procedures and accuracies feasible that were not previously possible.

Logic triggering techniques

The 7A42 is a two-wide, 350-MHz amplifier plug-in for the Tektronix 7000 series line of laboratory oscilloscopes. It permits the display of digital signals in analog form using logic triggering techniques—a capability that brings together oscilloscope and high-speed logic analyzer technologies.

General Background

Logic Triggering

By adding flexible word recognition functions much like those of logic analyzers, the 7A42 overcomes the limitations of traditional triggering techniques. It generates a trigger when a programmed Boolean equation is satisfied. The equation describes a set of logic conditions that must be present at the vertical inputs for a trigger to be generated by the 7A42 and sent to the time base to initiate a sweep.

For example, if an application requires triggering and viewing a logic combination in which the channel 1 signal is high, the channel 2 signal is low, the channel 3 signal is low, and the channel 4 signal changes from high to low, the user can set up the 7A42 to recognize the event. This is done very simply by pressing the appropriate front-panel keys as in Example 1.

Example 1:
CH1 AND CH2 NOT AND CH3 NOT AND CH4 NOT EDGE

A simplified equivalent logic diagram and timing diagram for this example are shown in Figure 1.

Entry flexibility

Note that the channel (CH1, CH2, CH3, or CH4), EDGE, and NOT selections may be entered in any order. For instance, key stroke sequences CH1 NOT EDGE, NOT CH1 EDGE, and EDGE NOT CH1 are equivalent. However, for purposes of this application note, the entry sequence employed is channel number, logic level, then transition, as applicable.

Boolean functions

In the 7A42, the AND function of two or more variables is termed the "product". For example, the product at the flip-flop D input in Figure 1 is CH1•$\overline{CH2}$•$\overline{CH3}$. Triggering products may be OR'ed together so that a triggering function may consist of the sum of two products, as in Example 2.

Example 2:
FUNCTION A = CH1 AND CH2 NOT OR CH1 NOT AND CH2

A simplified equivalent logic diagram for this example is shown in Figure 2.

In this instance, triggering function A consists of the Boolean sum of each of the products, CH1 AND CH2 NOT and CH1 NOT AND CH2. This is an implementation example of the 7A42 EXCLUSIVE-OR gate, a powerful general application feature. In using that feature, the 7A42 generates a trigger only when the two signals differ.

Independent vs dependent functions

The 7A42 memory can include two completely independent triggering functions: A and B. Each may in turn be called up and implemented immediately at the touch of a button. This offers important flexiblity, but the 7A42 can also operate in a nested triggering mode. This is called the A THEN B mode.

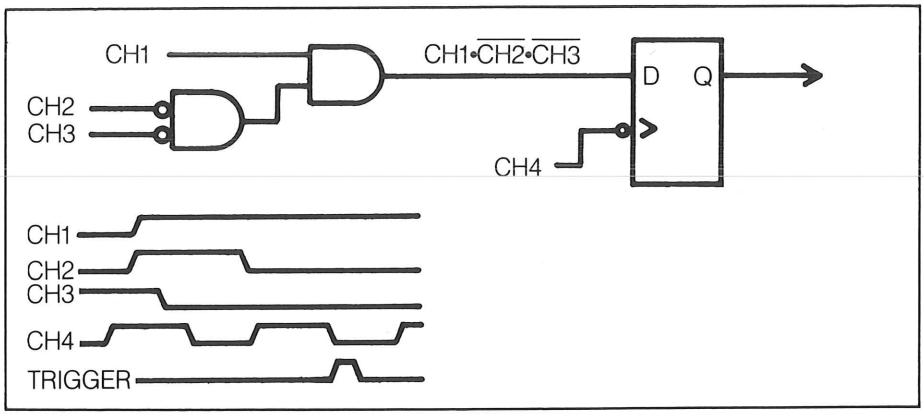


Figure 1. Example 1 Logic and Timing Diagrams

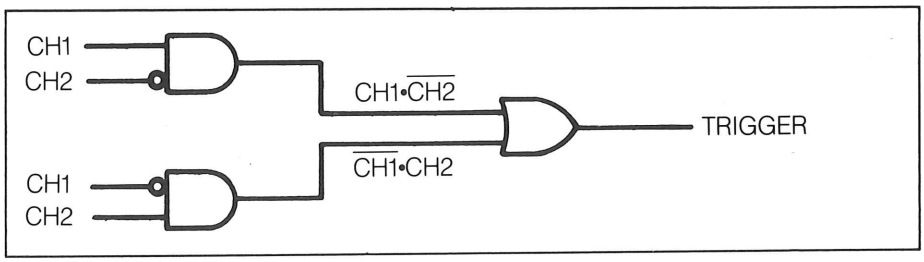


Figure 2. Example 2 Logic Diagram

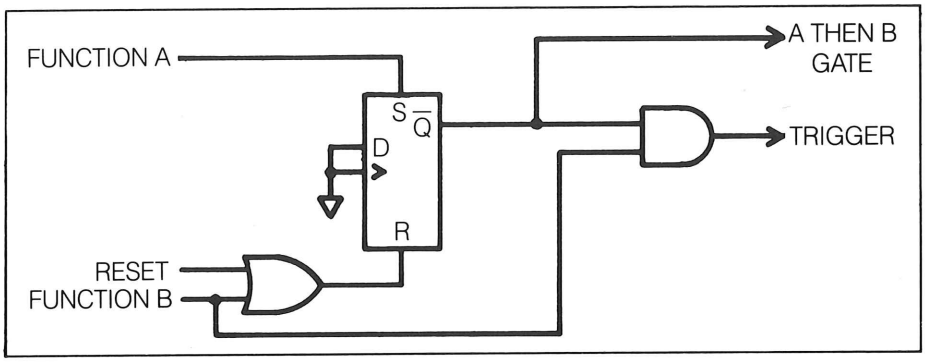


Figure 3. Simplified Nested Triggering Equivalent Diagram

Nested Triggering

In the nested triggering mode (A THEN B), trigger function A arms the circuitry and trigger function B causes the trigger to be generated at its next occurrence. An equivalent logic diagram is shown in Figure 3.

Gate generation

During nested triggering operation, the 7A42 generates a gate signal called A THEN B GATE, which becomes high when trigger function A is recognized and stays high until trigger function B is recognized (or until A THEN B GATE is reset). Thus, the duration of the A THEN B GATE signal represents the elapsed time between the occurrence of triggering function A and the following occurrence of triggering function B.

This gate signal is routed directly to the mainframe interface and can be internally strapped to the TRIGGER OUT connector on the front panel. The output signals, TRIGGER OUT and A THEN B GATE, allow the use of special purpose plug-ins to greatly extend the capabilties of the 7A42.

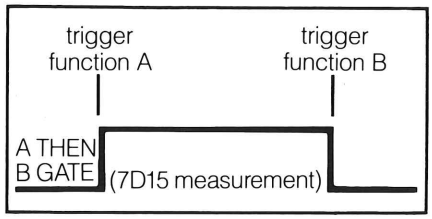
7A42/7D15 Combined features

When the nested triggering features of the 7A42 are combined with the time, frequency, and events measurement capabilties of the 7D15 Universal Counter/Timer plug-in, a powerful evaluation and troubleshooting system is created. The 7A42 A THEN B GATE signal can be used to gate the counting and timing functions of the 7D15 to easily accomplish previously difficult measurements.

The 7D15 can measure the duration of the 7A42 A THEN B GATE signal to indicate to the user the elapsed time between functions A and B. Or, the 7D15 can operate as a gated events counter to count the number of machine cycles between functions A and B. Or, the 7D15 can be used as a simple events counter to provide a total count of trigger events over extended time periods for reliability testing. These are only three of the practically limitless range of applications of these plug-ins.

7A42/7D15 Applications

To use the A THEN B GATE signal, the 7A42 A and B functions must be programmed. Function A becoming true arms the 7A42 and causes the A THEN B GATE signal to become high and remain so until function B becomes true. This generates a sweep trigger and also causes the A THEN B GATE signal to be reset low.



These programmed functions can be simple, such as CH1 AND CH2, or more complex, such as CH1 AND CH2 NOT OR CH1 AND CH2 NOT EDGE. Note that no external connections are necessary to the 7D15. With the 7A42 in the left-hand two compartments of a four-compartment mainframe and the 7D15 in the "A" Horizontal compartment, the 7A42 trigger outputs are sent directly to the 7D15 through the mainframe internal trigger path.

Note: CH1 and CH2 signals may not necessarily be synchronous. The display shows the actual signals of CH1 and CH2 during the A THEN B GATE time.

For these applications, the 7A42 trigger set-up is as follows:

Function A- CH1 NOT
Function B- CH1 NOT AND CH2 EDGE OR CH1 NOT AND CH2 NOT EDGE

Measuring Time From A To B

In digital design, the time between the occurrence of one event and the occurrence of a second can be used to determine design correctness or identify areas of concern. Propagation delay through a series of gates can be determined using the 7A42 A THEN B GATE signal to trigger a 7D15. The internal clock of the 7D15 can be used to determine the elapsed time from the recognition of function A (gate input) to the recognition of function B (gate output). The duration of the 7A42 A THEN B GATE signal represents this time and can be measured by the 7D15 and the results displayed on the mainframe crt.

Setup

To measure the elapsed time, make the necessary connections from the unit under test to the 7A42 input channels; program the 7A42 trigger functions; set up each channel for the desired logic family, impedance, threshold, and display characteristics; and set up the 7D15 as follows:

Gate to NORMAL
Mode to TIM WIDTH A
Average to x10
Clock to 10 ns
Trigger A source to TRIGGER SOURCE
slope to + (plus)
coupling to DC
level to PRESET

Then, set the mainframe trigger source for the 7D15 compartment to RIGHT VERTICAL MODE.

Measurement

The 7D15 will count the time between occurrences of functions A and B. As shown in Figure 4, the time for this example is 194 ns. The width of A THEN B GATE is wider than the elapsed time between events A & B by 5 ns ± 2 ns.

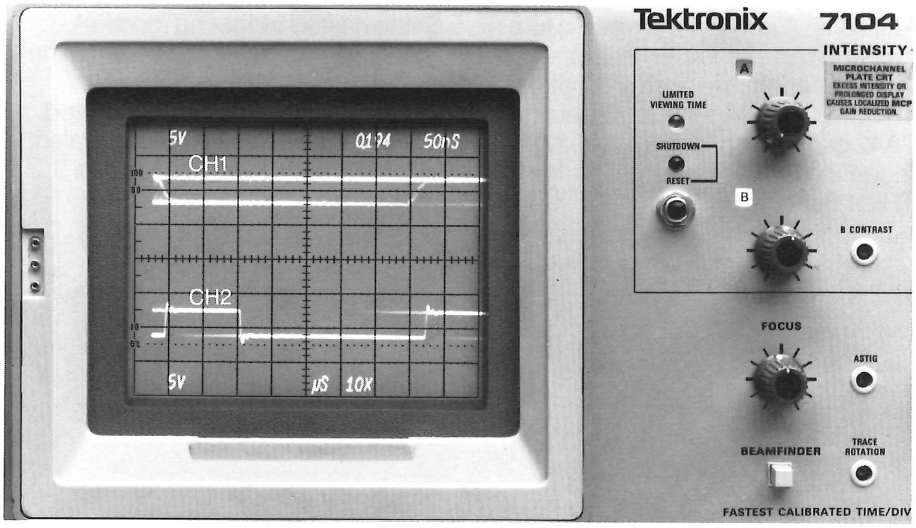


Figure 4. A to B Timing

Counting Clock Cycles Between Events

In microprocessor design and service, intermittent failures are difficult to identify and locate. The number of clock cycles between an event (set up as trigger function A) and an error condition (set up as trigger function B) can both simplify and speed fault location. The 7A42 trigger functions, A and B, can be programmed to recognize two such independent events and, with an external system clock connected to the 7D15, the 7D15 can count the number of clock cycles occurring between the events. The 7A42 A THEN B GATE signal low-to-high transition initiates the 7D15 count of the system clock and the high-to-low transition terminates the count.

Setup

To count clock cycles, make the proper connections from the unit test to the 7A42 input channels; program the 7A42 trigger functions; set up each channel for the desired logic family, impedance, threshold, and display characteristics; connect the system clock signal to the 7D15 B input; and set up the 7D15 as follows:

Gate to CH A GATE
Mode to FREQ B
Display time to 5 S
Storage to OFF
Trigger A source to TRIGGER SOURCE
slope to + (plus)
coupling to DC
level to PRESET
Trigger B source to INPUT b
slope to + (plus)
coupling to DC
level to PRESET
sensitivity as required

Then, set the mainframe trigger souce for the 7D15 compartment to RIGHT VERTICAL MODE.

Measurement

The 7D15 will count the clock cycles between the occurrence of function A and B. As shown in Figure 5, the count in this example is 195 clock cycles.

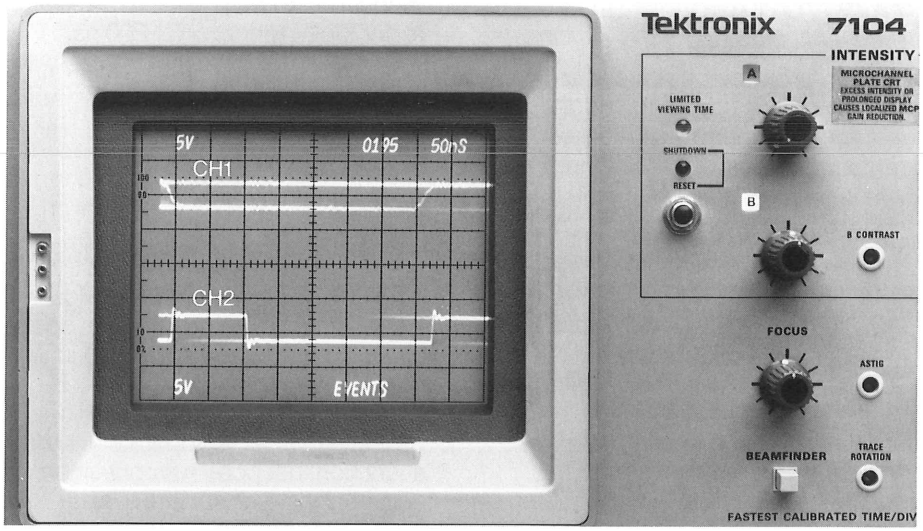


Figure 5. Clock Cycles between A and B

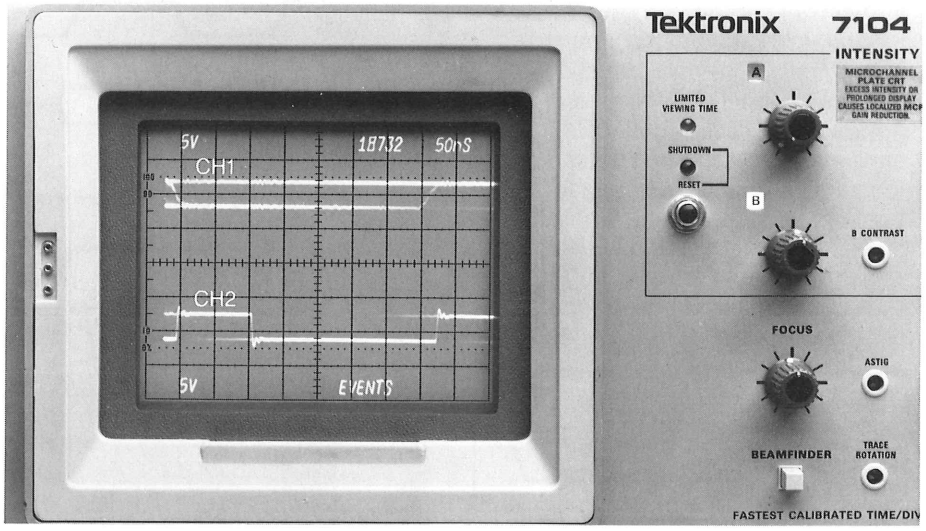


Figure 6. Triggers Generated

Counting Events

In the evaluation of digital systems, it is often necessary to monitor for specific conditions such as intermittent or aperiodic errors. The combination capabilities of the 7A42 and 7D15 can count the number of triggers (errors or other events) occurring during any set period.

Setup

To count the number of errors, make the necessary connections from the unit under test to the 7A42 input channels; program the 7A42 trigger functions to recognize the error condition; set up each channel for the desired logic family, impedance, threshold, and display characteristics; and set up the 7D15 as follows:

Mode to FREQ B
Gate to ON
Display time to infinite
Trigger B source to TRIGGER SOURCE
slope to + (plus)
coupling to DC
level to PRESET

Then, set the mainframe trigger source for the 7D15 compartment to LEFT VERTICAL MODE.

Measurement

The 7D15 will keep a running count of the number of triggers generated by the 7A42 and display the total on the mainframe crt as shown in Figure 6. The user can either turn off the test unit, or monitor the reading during operation after a predefined time has elapsed.

7A42/7D11 Application

Extra Background

To verify microprocessor system read operation timing, the edge-sensitive triggering, trigger delay, and trigger reset capabilities of the 7A42 are most helpful.

Edge-Sensitive Triggering

The 7A42 allows the user to recognize and trigger on the rising or falling step of a signal. It is similar to the + and − slope triggering of a standard oscilloscope plug-in. Basic information to this application is that CHI NOT EDGE means that the trailing edge of a pulse is the "true" condition.

Trigger Delaying

To examine the conditions toward the end of the read pulse, the variable trigger filter can be used to prevent trigger arming before the time window of the actual read operation. For example, if the trigger filter is set for approximately 200 ns, the READ strobe line must remain low for longer than 200 ns for trigger function A to be satisfied and the 7A42 sweep trigger output to be armed. Timing diagrams with the trigger filter off and on are shown in Figures 7 and 8, respectively.

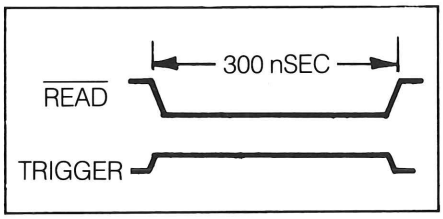


Figure 7. Non-Delayed Trigger Arming Timing Diagram

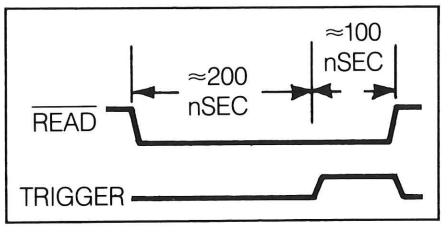


Figure 8. Delayed Trigger Arming Timing Diagram

Trigger delay setup

To set the trigger filter for 200 ns, select 7A42 function A (CH1 not) with the trigger filter off and note the duration of the READ strobe signal. Then, turn the trigger filter on, continuing to turn the control clockwise until the displayed duration of the signal on screen is reduced by 200 ns. By turning on the trigger view function of the 7A42, a display similar to Figures 7 and 8 can be attained. In this operation, the oscilloscope triggers at the point in the read cycle after which the date lines must remain stable. (The trigger filter will operate only on a function that does not contain an edge-sensitive channel.)

Trigger Reset

When using the A THEN B GATE with the 7D11, the 7D11 can be used to reset the 7A42 if function B does not occur within a predetermined time. This allows the 7A42 to be armed again by the next occurrence of function A. For this purpose, the 7D11 is used in the delay-by-time mode. It begins counting when function A is recognized and times out some set time after that event.

Locating Illegal Data Transitions

In developing a microprocessor based system, it is important to ensure that data being read from or written into memory remain stable at specified times during memory read

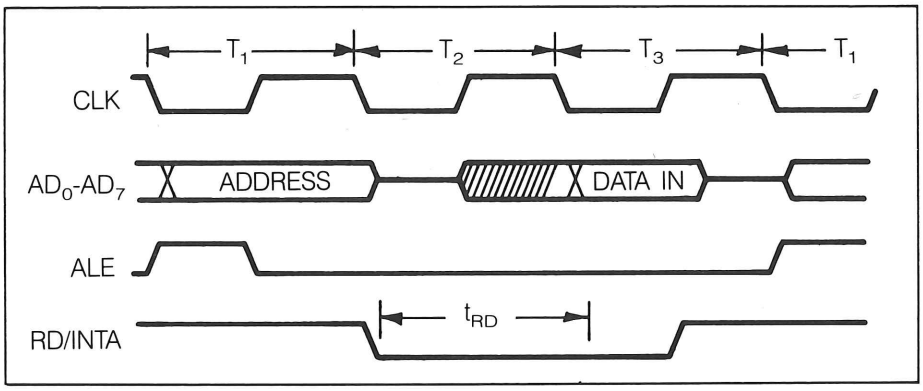


Figure 9. 8085A Read Cycle Timing Diagram

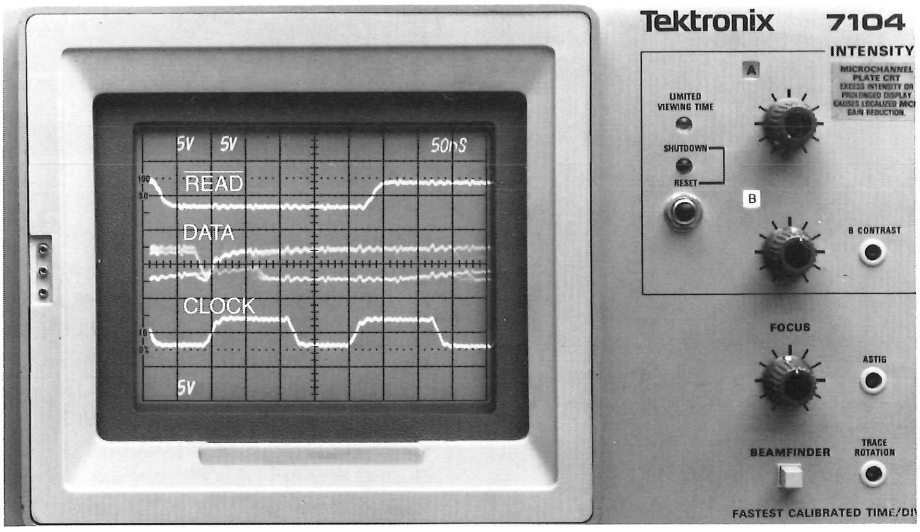


Figure 10. Read Cycle Timing

and write cycles. This timing is critical to transferring only valid data. The 7A42 can monitor the data lines and trigger on an error condition through its level- and edge-sensitive trigger functions.

Verifying Read/Write Timing

A timing diagram of a read cycle for the 8085A microprocessor is shown in Figure 9.

Figure 10 is an example of a data line display during a typical read cycle in a functioning microprocessor system. In this example, the 7A42 trigger source is the READ pulse alone (CH1 NOT). The READ pulse is applied to channel 1, the data line (AD03) is applied to channel 2, and the clock signal is applied to channel 3. The trigger selected is CH1 NOT.

Making the Measurement

In searching for illegal data transition, the tests must examine each data line to isolate timing problems. Using the 7A42, this is done by defining a timing window during which a Boolean triggering function must be recognized, and stepping through the data lines. This technique allows displaying only events of interest and eliminates double triggering and confusing displays. With it, the user is assured that triggers are generated only upon recognition of specific error conditions and that those errors can be positively identified. The following tests search for illegal data transitions in the 8085A microprocessor operations.

To perform the tests requires a 7D11 Digital Delay Unit and a suitable time base such as a 7B80 Delayed Time Base.

Setup

First, program the 7A42 triggering functions as follows:

Function A—CH1 NOT
Function B—CH1 NOT AND CH 2 EDGE OR CH1 NOT AND CH2 NOT EDGE

Second, set up the 7B80 and 7D11 controls as follows:

7B80—Mode to NORM
Coupling to DC
Source to INT
Time/div to 50 ns
Trigger source to VERT MODE

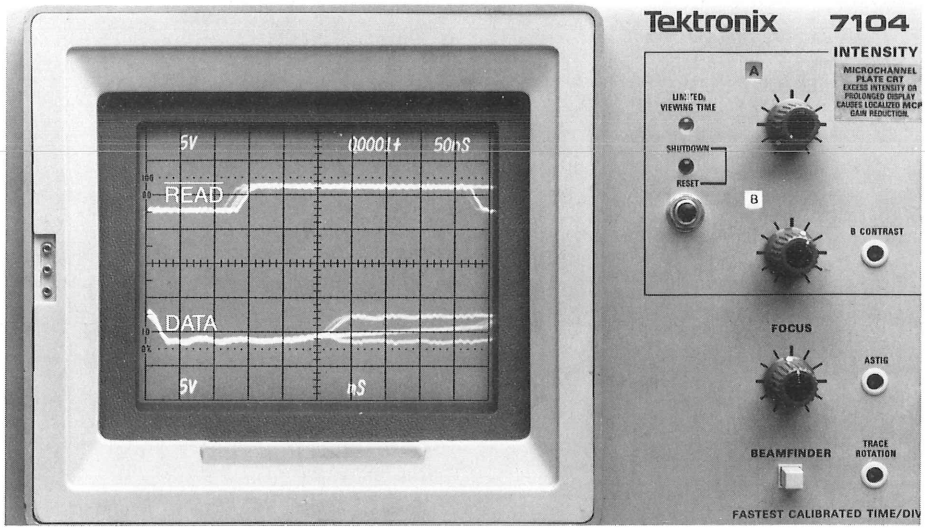


Figure 11. Non-Spec Data Transition

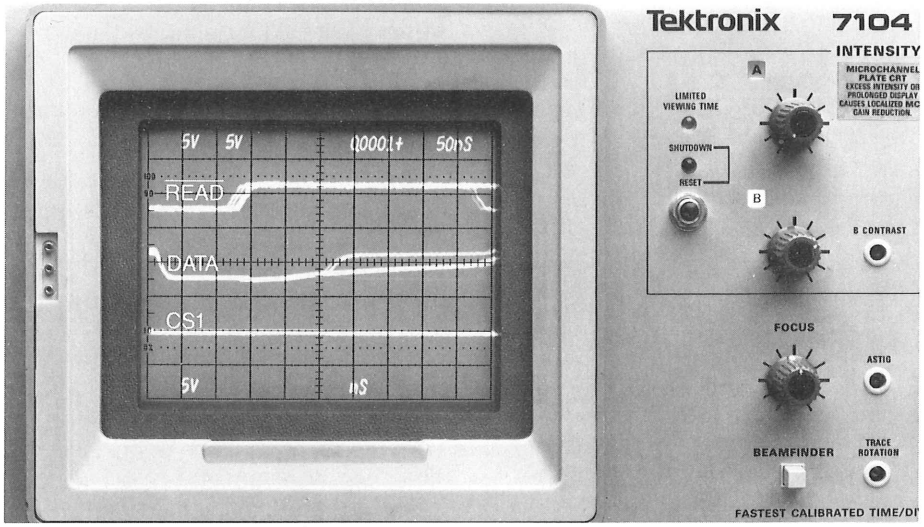


Figure 12. Chip Select High, Chip Not Enabled

7D11—Coupling to DC
Source to INT
B sweep delay mode to INDEPENDENT
Count mode to TIME INTERNAL CLOCK
Delay time or events to 0.0001 + ms

Third, connect a cable from the 7D11 DLY INTERVAL OUT connector to the 7A42 RESET input connector.

Fourth, set the 7A42 trigger filter to delay approximately 200 ns before arming the 7D11 (see the paragraph on edge-sensitive triggering). The delay time of the 7D11 resets the 7A42 100 ns after the trigger signal is received.

Measurement

This setup will cause the 7A42 to arm 200 ns after the beginning of a low level READ strobe signal. Function B will cause the 7A42 to generate a trigger if, during a low level state of the READ strobe signal, either a positive-going or negative-going transition occurs on the data line. Figure 11 shows a data transition outside the 8085A specifications.

In this instance, the test 8085A runs at a 4.5-MHz internal clock rate. The data must be valid approximately 210 ns after the READ strobe signal becomes low (according to the 8085A data sheet for this clock rate).

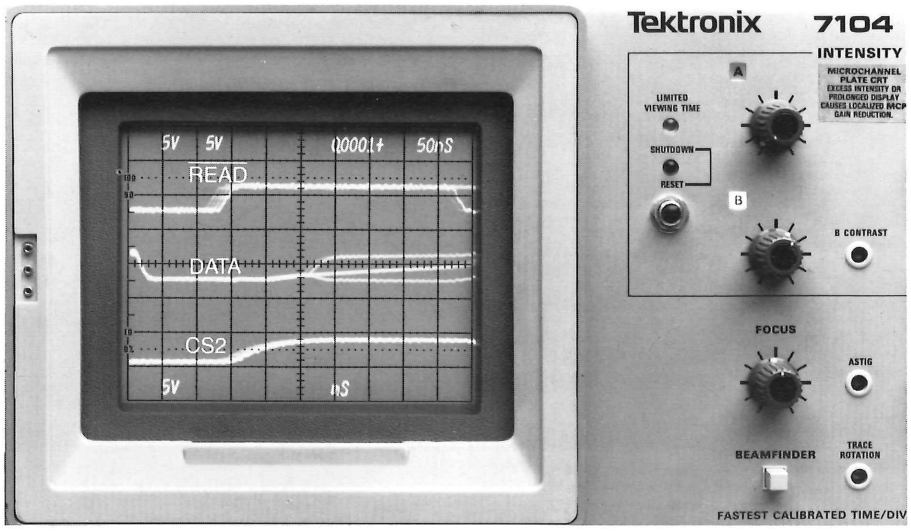


Figure 13. Chip Enable, Chip Selected, Producing Data

Locating the Fault

Examining the chip enable lines of the two 2764 memory devices in this design indicates that the second chip enable is causing the problem. This is shown in Figure 12 (chip select high, chip not enabled) and Figure 13 (chip enable low, chip selected and producing data). In this particular instance, excessive capacitance on the chip enable line to the second device was found to be the problem.

Error detection and recording

If no triggers are generated by the 7A42, the user is assured of the timing stability of the design. If a trigger does occur, the error condition can be seen in analog form and the timing error can be measured. If this event occurs at a very slow repetition rate, or occurs rarely or at random, a storage oscilloscope such as the 7834 can be used to view it. A fast writing real-time oscilloscope, such as the 7104 or 7904A, can also be used in conjunction with a crt camera to record the event.

Summary

When the logic triggering features of the 7A42 are combined with the delay and counting features of the 7D11 and 7D15, the result is a test and troubleshooting system that makes previously difficult fault identification both efficient and practical. The capability to set up a triggering function and wait for a fault condition using the 7D11, or to measure the time, number of events, or number of faults using the 7D15, is invaluable to the digital designer or evaluator.

The ability to quickly and easily set up a triggering function without the time, expense, and trouble of finding a suitable gate, wiring the proper levels to that gate, and then using the gate output to trigger an oscilloscope to capture an error condition, is a significant advantage to the user of this system.

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