Tektronix®

COMMITTED TO EXCELLENCE

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

PM 101
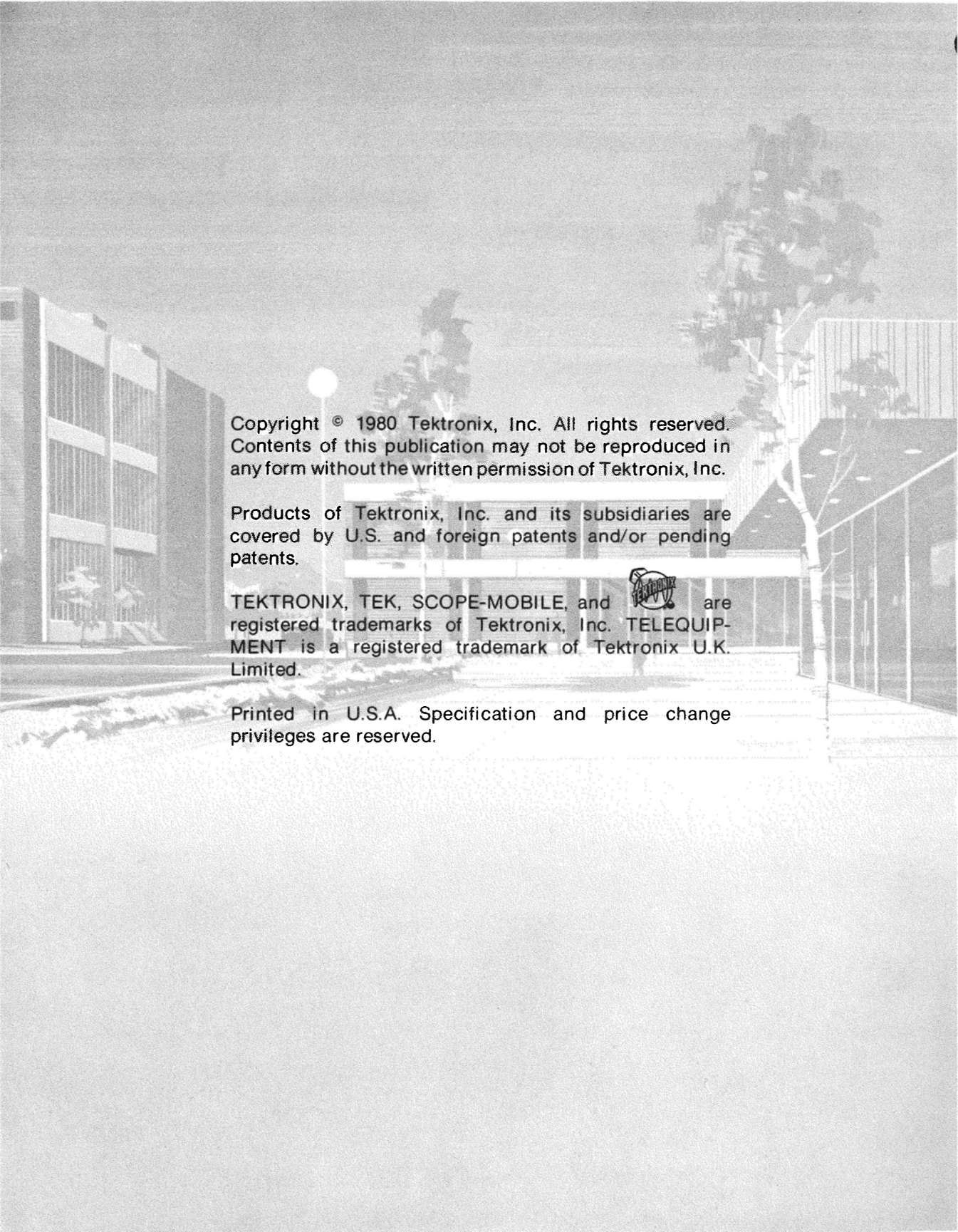## GENERAL PURPOSE
PERSONALITY MODULE

INSTRUCTION MANUAL

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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

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NOTE

The following illustrations are located in the diagrams foldout section at the rear of this manual.

LIST OF TABLES

NOTE

The following tables are located in the diagrams foldout section at the rear of this manual.

OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

In This Manual

⚠ This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment

⚡ DANGER — High voltage.

⏚ Protective ground (earth) terminal.

⚠ ATTENTION — refer to manual.

Power Source

This product is intended to operate from a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power module power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power module power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Fuse

To avoid fire hazard, use only the fuse of correct type, voltage rating and current rating as specified in the parts list for your product.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Operate Without Covers

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.

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SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

Dangerous voltages may exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate in a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

PM 101 General Purpose Personality Module.

INTRODUCTION

About This Manual

This manual describes the operation and servicing of the PM 101 General Purpose Personality Module. The first part of this manual, the operator's portion, provides an overview of the module, instructions on how to connect it to Systems-Under-Test and the Logic Analyzer, and other information on operation. The second part of the manual, the service portion, is found after the colored divider page. It contains maintenance information, circuit descriptions, diagnostics, schematics, and parts lists, and is intended to be used only by qualified service personnel. Refer to the table of contents for the specific location of information.

This manual frequently refers to the "Logic Analyzer"; this means the 7D02 Logic Analyzer. It is assumed that the reader has access to Operator's and Service manuals for the 7D02.

Overview of the General Purpose Personality Module

The PM 101 General Purpose Personality Module attaches to a TEKTRONIX 7D02 Logic Analyzer allowing it to be used with virtually any system-under-test which has 16 or less data lines and 24 or less address lines. The rest of the PM 100 series of Personality Modules built by Tektronix are microprocessor-specific. The PM 101 is intended to allow a user to analyze systems for which a specific probe does not exist.

Physically, the PM 101 consists of a plastic pod containing the electronic circuitry on two circuit boards. A four foot ribbon cable and connector is attached to one end, and a set of 54 leads is connected to the other end. The ribbon cable and connector attach to the Logic Analyzer, while the leads are used to connect the Personality Module to the System-Under-Test or the Self Test Stimulus Circuitry of the PM 101 itself. Grabber tips for these leads (Tektronix Part No. 206-0222-00) are provided as a standard accessory.

Electrically, the General Purpose Personality Module buffers up to 16 Data lines, 24 Address lines, 10 Control or Qualifier lines and a clock. It also contains Read-Only-Memory Circuitry and Control Circuitry which allows the Logic Analyzer to read the ROM or halt the system under test. Self Test Stimulus Circuitry, used in diagnostics and troubleshooting, is on a second board.

OPERATING INSTRUCTIONS

Storing the General Purpose Personality Module

Keep the General Purpose Personality Module in a clean area where the temperature remains between −62°C and 85°C. Humidity should not exceed 95%, non-condensing. The PM 101 should not be taken above 50,000 feet.

Connecting the Personality Module to the Logic Analyzer

> CAUTION

Always be certain to turn off the mainframe (logic analyzer) power before connecting or disconnecting any Personality Module.

Turn off the mainframe power and insert the ribbon cable connector labeled "PERSONALITY MODULE—PM 100 SERIES" into the receptacle labeled "PERSONALITY MODULE—PM 100 SERIES" on the front of the Logic Analyzer.

Connecting the PM 101 to the System-Under-Test

The leads on the other end of the Personality Module are Data, Address, Control and Clock input lines, and one System-Under Test Stop Not output line. The input lines are buffered by the Personality Module for transmission to the Logic Analyzer. The STOP output is a signal from the Logic Analyzer to halt the System-Under-Test. The Data, Address, and some of the Control lines (C0—C5) are used for Word Recognizer event definition. Control lines C4—C9 may be used in acquisition strobe (state clock) qualification.

The PM 101 has 24 Address lines, 16 Data lines, 10 Control lines, a Clock input and a Stop output. This allows it to be used with a 7D02 having the Expansion Option (Opt. 3, Field Opt. 03). The leads from the General Purpose Personality Module are grouped into bunches of eight or ten color-coded wires, each of which is fitted with a single 0.025 inch square connector. This allows connection to almost any circuit. The wires are color-coded using the standard resistor color-code scheme which is shown on the Personality Module cover. Only the second digit of two-digit numbers is used in the color coding. The heavy black leads are Ground (GND). The grey lead next to the end is the Clock (CLK) line. The remaining single red lead is Stop System-Under-Test Not (/STOP S.U.T.). Refer to the cover of the Personality Module.

NOTE

A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies

0 — Write
1 — Read

Because the PM 101 Personality Module buffers signals with very fast rise times, it is important that procedures be followed which minimize delay and prevent cross-talk and other noise.

Always connect the input leads as closely as possible to the signal source to minimize signal degradation.

Keep individual leads separated as much as possible beyond the identification labels; closely bundled lines increase cross-talk.

Connect the ground leads directly to the ground pin of the signal driver wherever possible. Do not add any additional lead length to the ground path. This probe will only work correctly at high frequencies with systems which have an effective system of grounds.

When used without the Expansion Option, only Address lines 0—15 and Data lines 0—7 are functional. Everything else about hook-up remains the same.

If the Expansion Option is present in the Logic Analyzer, but the additional lines are unused, the displays will show all "1"s in binary, or all "F"s in hex, wherever there are lines without data. These can be inverted to appear as all "0"s by inversion in the Format mode.

Control lines. When connecting the PM 101 to a system, the control lines are used primarily for two things: qualification of data and qualification and synthesis of clocks. Control lines C0 through C3 are stored and displayed with each word. This makes them useful in the acquisition of processor lines which are not on the address or data busses, but which may be essential in establishing the status of the system under test. If not needed as control lines, C0—C3 may also be used as additional address or data lines, but they will still appear in

the CONTROL column. Control lines C4 and C5 may also be used in word recognizer event definition, though they are not stored. C4 through C9 can be used for clock qualification, which makes them useful for state clock generation, where the logical ANDing of the selected qualifiers and the input clock edge selects acquisition strobes (the State Clock) from the input clock signals and thereby limits the data collected. C6—C9 also have a role in USER CLOCK SYNTHESIS; see that subsection below.

NOTE

All clock qualifiers must meet set-up and hold time specifications relative to the PM 101 clock input. Refer to Sections 3 and 5.

When using USER CLOCK QUALification and USER CLOCK SYNTHESIS, the clock qualifier must be true when the clock synthesizer enables an Acquisition Strobe. It is possible to enter contradictory program instructions. If all clocks are disqualified, a NO CLOCK message will be displayed. If all data is disqualified, a NO DATA AC-QUIRED message appears when the program is stopped.

Instruction Fetch and Demultiplexing. The PM 101 does not have circuitry for decoding Instruction Fetch cycles or demultiplexing busses because it is not specific to any particular protocol. Nonetheless, appropriately connected control lines can provide qualification information which allows the Logic Analyzer to derive Instruction Fetch cycles or demultiplexing timing. Knowledge of the workings of the system under test and appropriate qualification can be used to identify almost any state of the system and to collect data only while the system is in that state. The data collected may be limited by either clock qualification in the trigger command or word recognizer event definition.

Clock. The Clock input line to the PM 101 is used to detect the basic timebase of the system under test. This clock is transmitted by the PM 101 for use as the data acquisition timebase after any desired polarity selection and qualification have been applied. The 7D02 Logic Analyzer has the ability to divide the clock or delay the clock from the system-under-test by two, three, or four, to select the rising or falling edge, and to AND the selected clock edge with a control word selected from C4—C9. Without user intervention, the default values imbedded in the PM 101's ROM are: no division, positive edge, and all "Don't Cares" (Xs) for C4—C9. These default values may be varied by entries in the User Clock Qualification field in the Program mode.

User Clock Synthesis. ESYNC (C6 or C8) allows synchronization of the 7D02 Clock Synthesizer to the timebase of the system-under test. The ESYNC signal is the reference for both the DIVIDE BY N mode and the DELAY BY N mode.

If USER CLOCK SYNTHESIS is selected in the 7D02, the user then has a choice between DELAY CLOCK BY N, where N may be 0, 1, 2, 3, or 4, and DIVIDE CLOCK BY N, where N may equal 1, 2, 3, or 4. A delay of 0 or a divide by 1 correspond to the inactivated states of these modes.

NOTE

Do not use the ESYNC or WAIT lines when dividing by 1 or delaying by 0.

If the user selects DELAY CLOCK BY N, one acquisition strobe (State Clock) will occur for every ESYNC, delayed by N input clock pulses. Refer to Fig. 2-1 and 2-3.

If the user selects DIVIDE CLOCK BY N, however, the Acquisition Strobe will occur on the N-1th input clock pulse after the end of the ESYNC signal, and at one Nth of the frequency of the input clock. The clock will continue at that frequency without further ESYNC signals. Refer to Fig. 2-2 and 2-3. In this mode it is assumed that ESYNC is asserted on the first phase of a multi-phase clock system and that it is desired to generate the 7D02 acquisition strobe (State Clock) on the last phase.

If ESYNC is repetitive, it should be regular and asserted at the same place in the input clock cycle of a system with a multiphase clock. If these conditions are not met, the clock phase may become un-synchronized or extra acquisition strobes (State Clocks) may be generated. Normally, when a repetitive ESYNC signal is available, the delay-by mode is most useful. Where no repetitive ESYNC is available, the divide-by mode is most useful, with ESYNC connected to some signal such as "Power-up Reset".

WAIT (C7 or C9) signals in both modes simply delay the next acquisition strobe (State Clock) by one input clock pulse for every input clock pulse that occurs while WAIT is asserted. See Fig. 2-1 and 2-2.

WAIT also qualifies acquisition strobes (the State Clock), inhibiting them even when all the ANDed Clock Qualifiers are true. Refer to Fig. 2-3.

NOTE

If both WAIT and ESYNC are asserted at the same time, only the WAIT signal will be effective. See Fig. 2-3.

@
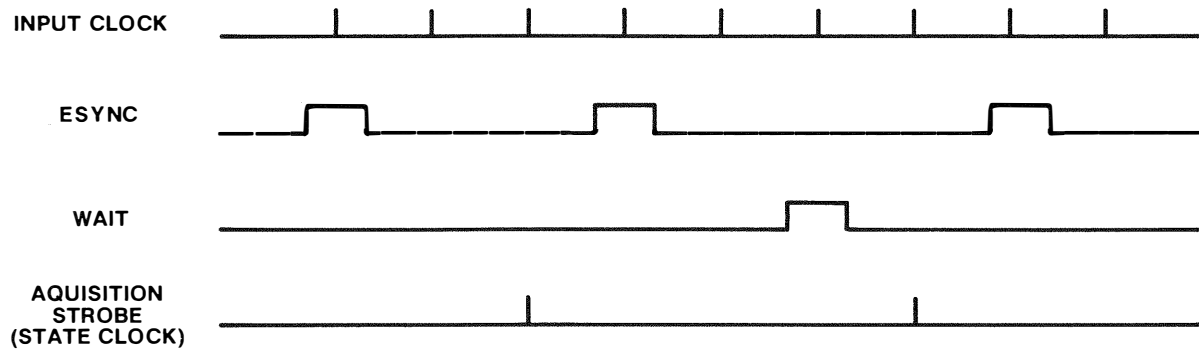
Fig. 2-1. User Clock Synthesis—Delay by 2.
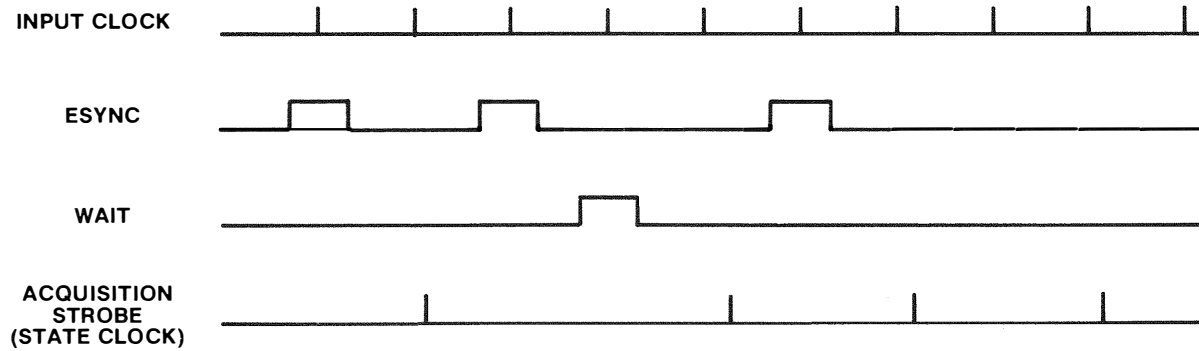
Fig. 2-2. User Clock Synthesis—Divide by 2.
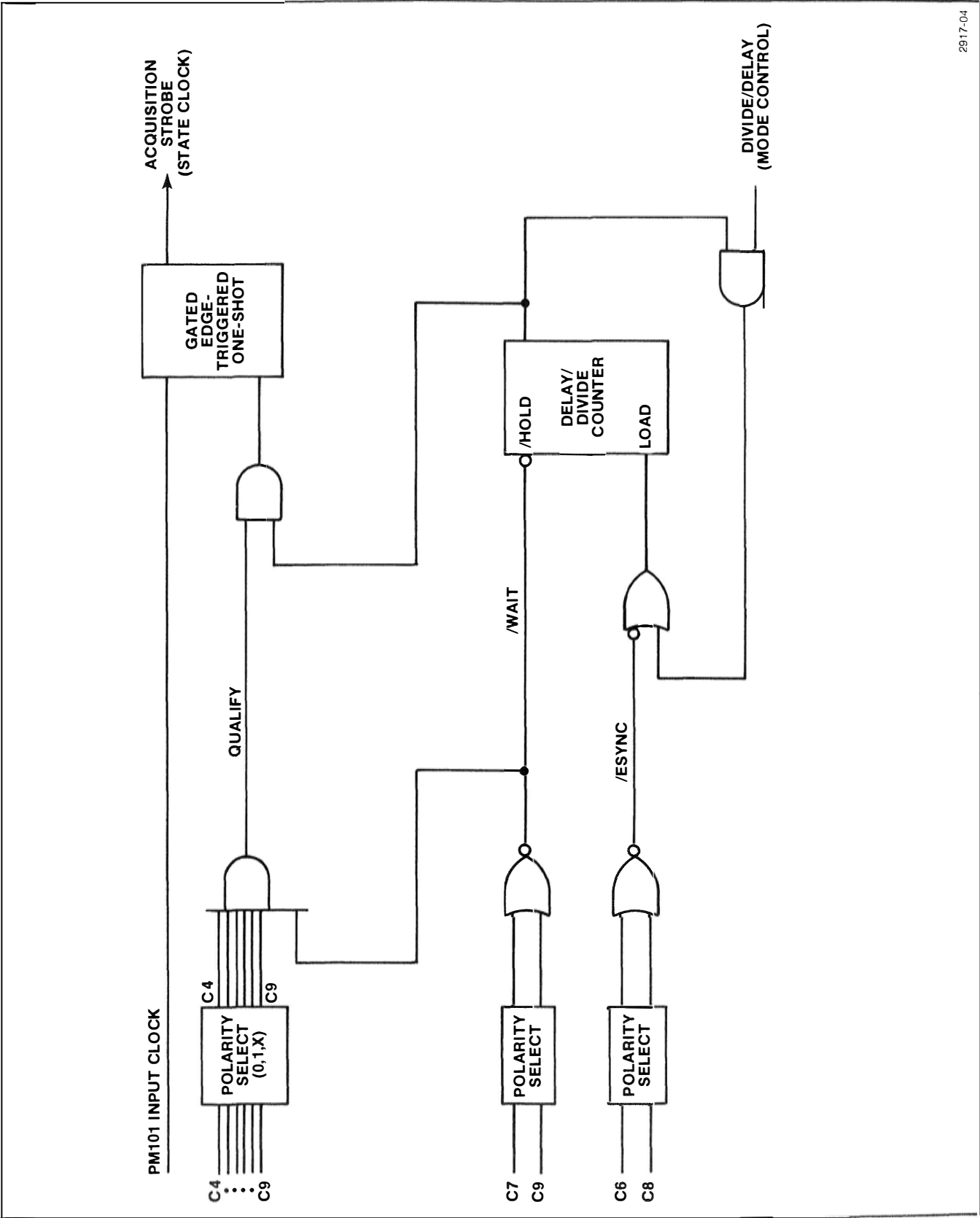
Fig. 2-3. 7D02 Clock Synthesis and Qualification Circuitry—Functional Block Diagram.

Inversion. Unless a bus inversion has been defined in the Format mode, all field selections are positive-true logic. A "1" selection in a clock qualification field is a selection of the clock edge when that qualifier is in a high, logic "1" state. If negative or mixed logic is to be analyzed, either the choices made while programming in the Word Recognizer may be inverted or the Format Mode may be entered and appropriate bus inversions performed.

The Bus Inversion display in the Format mode is most usable when binary is selected as the radix in the Word Recognizer Address Field and the Word Recognizer Data Field. This is the Bus Inversion display with binary radices selected and default "0"s shown:

```
BUS INVERSION
DATA=0000000000000000
AD=000000000000000000000000
C0=0        C1=0        C2=0        C3=0
C4=0        C5=0        EXT TRIG IN=0
```

/STOP. Stop System-Under-Test Not (/STOP S.U.T.) is the single output from the Logic Analyzer system back to the system-under-test. It is used by the Logic Analyzer to halt the system-under-test if "SYSTEM UNDER TEST HALT" is selected in the Main Trigger program. The STOP line can only be asserted low, i.e., the program runs with "STOP high; it is asserted low when main memory acquisition is complete. Since the STOP line cannot be set to low and then be asserted high, the system-under-test must be capable of responding to a low-true halt command.

NOTE

A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies

0 — Write
1 — Read

Application Examples

One typical use of the PM 101 General Purpose Personality Module is to analyze a system based on a microprocessor which is not currently supported by Tektronix. Others include analyzing systems which are not microprocessor based and analyzing bus networks generally.

The PM 101 does not perform mnemonic disassembly because it has been designed for these non-specific applications. All bus transactions can be monitored in the absolute mode if the user has a means of identifying instructions and data. Demultiplexing can be accomplished if a system control line indicating the bus status is used to qualify clocks or define word recognizer

events. Systems which include their own demultiplexing circuitry can be analyzed either from points where the signals of interest are separate or from points where they are multiplexed by the use of appropriate qualification.

6502. The MOS Technology 6502 is a good example of a microprocessor whose operation can conveniently be analyzed using the PM 101. It is an 8-bit processor with internal clock generation and an instruction SYNC line output. The SYNC line makes it much easier to distinguish Instruction Fetch cycles; the Logic Analyzer can use it as a direct control line input to monitor and index bus transactions. The 6502 has another feature which aids in monitoring its bus—all data on the bus is defined for every cycle.

Connecting the General Purpose Personality Module to the 6502 involves identifying the address and data lines and connecting the correct leads from the PM 101 to them. Depending on the availability of these lines the Grabber Tips (Tektronix Part No. 206-0222-00) which are standard accessories to the PM 101 may be required.

Connect the two black leads with the alligator clips to system ground. Connect the CLK connector, the grey lead next to the ground lead, to the Phase 2 clock output of the system-under-test.

The remaining single red wire is Stop System-Under-Test Not, /STOP S.U.T. The /STOP S.U.T. line must be used with discretion in the 6502 system. Conflict between the PM 101 circuitry and the system halt controls can cause improper system operation.

While particular applications might require monitoring other control lines, the following control lines are generally useful in most applications: SYNC, RDY, /NMI, /IRQ, S.O., and R/W. Only four of these lines can be stored and displayed, since only C0 through C3 receive this treatment in the Logic Analyzer. This example assigns C0 to R/W, C1 to /NMI, C2 to /IRQ, and C3 to SYNC (fetch). The two control lines which can be used for either word recognizer event recognition or clock qualification, C4 and C5, will be assigned to RDY and S.O., respectively.

The Format Mode can be used to invert any signals which are only available in negative logic. But remember, while bus inversions in the Format mode affect word recognizer event definition and the display of acquired data, they do not affect the trigger command or Timing Option areas.

It may be helpful to make notes in table form of which control lines go to which signals, what form those signals are in (normal or inverted), and whether an inversion

decision was made in the Format Mode. Such a table may be of great assistance in correctly programming the word recognizer.

Intel's Multibus®. The Intel MULTIBUS consists of a network of signal lines in the following categories: 20 address lines, 16 bidirectional data lines, 8 multilevel interrupt lines, and several bus control, timing and power supply lines. The data and address lines are driven by 3-state devices. The interrupt and some other control lines are open-collector driven.

The MULTIBUS is compatible with 8- or 16-bit processors with data rates up to 5 MHz. While data is transferred asynchronously, XACK, the Transfer Acknowledge Signal, can be used as clock for bus traffic.

Table 2-1 gives a typical monitoring example for a user primarily interested in address and data information:

TABLE 2-1

TYPICAL CONNECTIONS

PM101/7D02 Channels	Pin #	Signal Name
Address 0	57	ADR0
1	58	ADR1
2	55	ADR2
3	56	ADR3
4	53	ADR4
5	54	ADR5
6	51	ADR6
7	52	ADR7
8	49	ADR8
9	50	ADR9
10	47	ADRA
11	48	ADRB
12	45	ADRC
13	46	ADRD
14	43	ADRE
15	44	ADRF
16	28	ADR10
17	30	ADR11
18	32	ADR12
19	34	ADR13
20	27	BHEN
21	spare	
22	spare	
23	spare	

TABLE 2-1 (cont)

PM 101/7D02 Channels	Pin #	Signal Name
DATA 0	73	DAT0
1	74	DAT1
2	71	DAT2
3	72	DAT3
4	69	DAT4
5	70	DAT5
6	67	DAT6
7	68	DAT7
8	65	DAT8
9	66	DAT9
10	63	DAT10
11	64	DAT11
12	61	DAT12
13	62	DAT13
14	59	DAT14
15	60	DAT15
CLOCK CLK	23	XACK
CONTROL 0	19	MRDC
1	20	MWTC
2	21	IORC
3	22	IOWC
4	spare	
5	spare	
/STOP S.U.T.	not used	

In the Main Trigger section, choose the USER CLOCK QUAL. and FALLING EDGE OF CLOCK alternatives. Leave all other choices in their default states.

The data gathered will include all reads and writes to memory, all reads and writes to input-output devices and the Interrupt Response/Acknowledge cycle.

This set-up does not provide information about which cycle is an Instruction Fetch, which master is controlling the bus, or when an interrupt occurs. The spare channels can be used to ascertain which master is controlling and when interrupts occur, if desired.

The example given was for a 16-bit system. The extra lines available when the PM 101 is used with an 8-bit system can be used to derive much more system status and control line information. Particular choices vary with the user's needs and perspective.

How this Personality Module Affects the Logic Analyzer

Part of the display of the Logic Analyzer and the choices that it offers are Personality Module dependent. The PM 101 General Purpose Personality Module contains 2k words of ROM (Read Only Memory) which, when read by the Logic Analyzer, provide it with a variety of information which it needs to appropriately format displays, etc. This sub-section provides information about the ways in which the PM 101 ROM modifies the performance of the 7D02.

Word Recognizer Format

The General Purpose Personality Module produces the following display format in the Word Recognizer:

```
DATA=nn
ADDRESS=nnnn
C0=b     C1=b     C2=b     C3=b
C4=b     C5=b     EXT TRIG IN=b
```

where   "b" is a binary digit or "X",
         "n" is a binary, hex or octal digit, or "X"
         (default hex is shown), and
         "X" is "Don't care".

Radix Selection. To vary the radix of "n" in the above example, enter the Format mode by pressing the FORMAT key and move the cursor to the Word Recognizer Address Field. The display looks like this:

```
WORD RECOGNIZER ADDRESS FIELD
   2-HEX
      0 BINARY
      1 OCTAL
      2 HEX
```

indicating that if the user wishes to select an alternative radix to the default hexadecimal, the "0" or "1" key should be depressed.

Note: While the Data and Address field radices may be varied by selections made in the Format mode, the Control lines must always be binary.

Expansion Option. If the Expansion Option (Opt. 3, Field Opt. 03) is present, the following display is defined by the PM 101 for the Word Recognizer:

```
DATA=nnnn
AD=nnnnnn
C0=b     C1=b     C2=b     C3=b
C4=b     C5=b     EXT TRIG IN=b
```

where   "b" is a binary digit or "X",
         "n" is a binary, hex or octal digit or "X"
         (default hex is shown), and
         "X" is "Don't care".

As above, the choices for "n" are varied by selections made in the Format mode.

Data Display Format

Since the PM 101 is not specific to any particular system, it does not include any mnemonic display capability. The Mnemonic Mode, if selected, is the same as the Absolute Mode and produces an identical display. In both modes, if all radices are non-binary, the header in the display field is:

```
LOC     ADDRESS     DATA     CONTROL
```

In the LOCation column, "000" is the oldest stored data and "255" is the most recent. In the CONTROL column, C∅ is on the right and C3 is on the left.

Radix Selection. After the FORMAT key on the 7D02 Logic Analyzer is pressed and the cursor is appropriately positioned, the display offers the following choices:

```
ADDRESS FIELD DISPLAY
   2 HEX
      0 BINARY
      1 OCTAL
      2 HEX
      3 ASCII
```

indicating that if the user wishes to select an alternative radix to the default hexadecimal, the "0", "1" or "3" key should be depressed.

When the cursor is moved down, the display becomes:

```
DATA FIELD DISPLAY
   2 HEX
      0 BINARY
      1 OCTAL
      2 HEX
      3 ASCII
```

If the user chooses anything other than a binary output for the Address Field Display and Data Field Display radices, and the Expansion Option is not present, the data in the Acquisition Memory is displayed in the following format:

```
ddd       nnnnnn       nnn       bbbb
dddT      nnnnnn       nnn       bbbb
```

where   "b" is a binary digit,
         "n" is a binary, hex, octal, or ASCII digit
         (default hex is shown),
         "d" is a decimal digit, and
         "T" indicates where the trigger occurred.

Note: While the user may define the radices for the Address and Data fields, the Location and Control fields' radices are fixed.

Binary Address—Binary Data. If binary is chosen for the output radix for the Data and Address display fields, and the Expansion Option is not present, no header as such appears and the format is:

```
LOC:ddd CNTL:bbbb DATA:bbbbbbbb
ADDRESS:bbbbbbbbbbbbbbbb
LOC:ddd CNTL:bbbb DATA:bbbbbbbb
ADDRESS:bbbbbbbbbbbbbbbb TRIG
```

where   "b" is a binary digit,
         "d" is a decimal digit, and
         "TRIG" indicates the trigger value.

Expansion Option. If the user chooses non-binary output radices for the Address and Data fields, but the Expansion Option is present, the data is output in the following format:

```
ddd        nnnnnnnnn    nnnnnn     bbbb
dddT       nnnnnnnnn    nnnnnn     bbbb
```

where   "b" is a binary digit,
         "n" is a binary, hex, octal, or ASCII digit
         (default hex is shown),
         "d" is a decimal digit, and
         "T" indicates where the trigger occurred.

If both the Data Field Display and Address Field Display radices are selected to be binary and the Expansion Option is present, the output is in the following format:

```
LOC:ddd          CONTROL:bbbb
AD:bbbbbbbbbbbbbbbbbbbbbbbb
DATA:bbbbbbbbbbbbbbbb
LOC:dddT         CONTROL:bbbb
AD:bbbbbbbbbbbbbbbbbbbbbbbb
DATA:bbbbbbbbbbbbbbbb
```

where   "d" is a decimal digit,
         "b" is a binary digit, and
         "T" indicates where the trigger occurred.

SPECIFICATIONS

TABLE 3-1

ELECTRICAL SPECIFICATIONS

Characteristics	Description			
Signal Inputs				
Maximum number of channels with Option 03	Total 50		Data 16 Address 24 Control 10	

	Control Line	Stored	Word Rec. Input	Clock Qualifier
	C∅	X	X	
	C1	X	X	
	C2	X	X	
	C3	X	X	
	C4		X	X
	C5		X	X
	C6			X
	C7			X
	C8			X
	C9			X

Characteristics	Performance Requirements	Supplemental Information
General Purpose Data Input Channels		
TTL Input Levels		1/2 LSTTL load 0 V—7 V signal swings max
Input Capacitance		25 pF nominal
Voltage in low limits	Minimum 0.0 V, Maximum 0.5 V	
Voltage in high limits	Minimum 2.4 V, Maximum 7.0 V	
Hysteresis		0.2 V minimum
Current in low limits (V in low = 0.4 V)		−0.2 mA maximum

TABLE 3-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
Current in high limits (V in high = 7.0 V)		+0.1 mA maximum
Current in high limits (V in high = +2.7 V)		+0.02 mA maximum
Maximum voltage in Non-operating, Non-destructive		−7 to +15 continuous. Limited to any two inputs simultaneously on negative voltages.
Threshold voltage		Fixed +1.4 V, nominal. TTL compatible
Halt Output Drive		
V_{OH}		2.4 V, I_o = 1 mA
V_{OL}		0.5 V, I_o = −2 mA
Clock Input		
Input resistance		50 kΩ typical
Input capacitance		15 pF nominal
Clock period	100 ns minimum	
Clock pulse width minimum	25 ns high, 25 ns low	
Voltage in low limits (operating)	0.0 V minimum, 0.5 V maximum	
Voltage in high limits	2.4 V, 7.0 V minimum	
Hysteresis		0.4 V nominal
Threshold voltage		Fixed 1.4 V nominal
Maximum voltage in, Non-operating, non-destructive		−15 V to +15 V
Propagation delays through Personality Module		
Delay through ECL clock		10.5 ns minimum, 14.5 ns maximum
Data channel delay (Address and Control)		21.5 ns minimum, 31 ns maximum
Test Clock		
Clock Period		100 ns ± 10 ns
Clock Pulse Width, minimum		25 ns

Table 3-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
General Purpose System Specification with Logic Analyzer		
Clock/Qualifier Data (Channels C4—C9)	Setup time = 55 ns maximum Hold time = 0.0 ns maximum	35 ns typical measured according to manual performance check
Data (Channels A0—A23, D0—D15, C0—C3)	Setup time =45 ns maximum Hold time = 0.0 ns maximum	25 ns typical
C6—C9, when used to generate /ESYNC and /WAIT	Setup time = 55 ns maximum Hold time = 0.0 ns maximum	35 ns typical
Data acquisition period between qualified clocks	100 ns minimum	
Data pulse width	50 ns minimum	

TABLE 3-2

MECHANICAL SPECIFICATIONS

Characteristics	Performance Requirements	Supplemental Information
Size		4.7" x 8" x 1.7" (12 cm x 20.3 cm x 4.3 cm)
Weight		Approx. 2 lbs. w/cables (Approx. 1 kg w/cables)
Cable length Logic Analyzer to Pod		4 ft. ±1.0 in.) (122 cm ±2.5 cm)

TABLE 3-3

ENVIRONMENTAL SPECIFICATIONS

Characteristics	Performance Requirements	Supplemental Information
Temperature		Operating: +15° C to 55° C Non-operating: −62° C to 85° C
Relative Humidity		95% to 97%, non-condensing
Altitude		Operating: 4.5 km (15,000 feet) Non-operating: 15 km (50,000 feet)

TABLE 3-4
LOGIC ANALYZER CONNECTOR INTERFACE

Pin	Signal	Electrical Description
1	AI1	STTL output, back terminated into 68 Ω
2	CLK	Differential ECL: HI = −0.8 V, LO = −1.7 V; differentially terminated into 124 Ω
3	/CLK	Differential ECL: HI = −0.8 V, LO = −1.7 V; differentially terminated into 124 Ω
4	AI3	STTL output, back terminated into 68 Ω
5	AI0	STTL output, back terminated into 68 Ω
6	AI5	STTL output, back terminated into 68 Ω
7	AI2	STTL output, back terminated into 68 Ω
8	AI6	STTL output, back terminated into 68 Ω
9	AI4	STTL output, back terminated into 68 Ω
10	GND	Ground
11	AI7	STTL output, back terminated into 68 Ω
12	AI8	STTL output, back terminated into 68 Ω
13	AI9	STTL output, back terminated into 68 Ω
14	AI11	STTL output, back terminated into 68 Ω
15	AI10	STTL output, back terminated into 68 Ω
16	AI13	STTL output, back terminated into 68 Ω
17	AI12	STTL output, back terminated into 68 Ω
18	AI15	STTL output, back terminated into 68 Ω
19	AI14	STTL output, back terminated into 68 Ω
20	GND	Ground
21	AI16	STTL output, back terminated into 68 Ω
22	AI17	STTL output, back terminated into 68 Ω
23	AI18	STTL output, back terminated into 68 Ω
24	AI19	STTL output, back terminated into 68 Ω
25	AI21	STTL output, back terminated into 68 Ω
26	AI20	STTL output, back terminated into 68 Ω
27	AI23	STTL output, back terminated into 68 Ω
28	AI22	STTL output, back terminated into 68 Ω
29	DI1	STTL output, back terminated into 68 Ω
30	GND	Ground
31	DI3	STTL output, back terminated into 68 Ω
32	DI0	STTL output, back terminated into 68 Ω
33	DI4	STTL output, back terminated into 68 Ω
34	DI2	STTL output, back terminated into 68 Ω
35	DI6	STTL output, back terminated into 68 Ω
36	DI5	STTL output, back terminated into 68 Ω
37	DI9	STTL output, back terminated into 68 Ω
38	DI7	STTL output, back terminated into 68 Ω
39	DI10	STTL output, back terminated into 68 Ω
40	GND	Ground
41	DI12	STTL output, back terminated into 68 Ω
42	DI8	STTL output, back terminated into 68 Ω
43	DI14	STTL output, back terminated into 68 Ω
44	DI11	STTL output, back terminated into 68 Ω
45	+5 V	STTL output, back terminated into 68 Ω
46	DI13	STTL output, back terminated into 68 Ω
47	C0	STTL output, back terminated into 68 Ω
48	DI15	STTL output, back terminated into 68 Ω
49	C2	STTL output, back terminated into 68 Ω

TABLE 3-4 (cont)

Pin	Signal	Electrical Description
50	GND	Ground
51	C5	STTL output, back terminated into 68 Ω
52	C1	STTL output, back terminated into 68 Ω
53	C7	STTL output, back terminated into 68 Ω
54	C3	STTL output, back terminated into 68 Ω
55	C9	STTL output, back terminated into 68 Ω
56	C4	STTL output, back terminated into 68 Ω
57	+5 V	STTL output, back terminated into 68 Ω
58	+15 V	Power Supply
59	−15 V	Power Supply
60	C6	STTL output, back terminated into 68 Ω
61	/HALT S.U.T.	1/2 LSTTL input load
62	C8	STTL output, back terminated into 68 Ω
63	/SEL P	4 LSTTL input loads
64	LOOK	4 LSTTL input loads

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

THEORY OF OPERATION

General Theory of Operation

The primary function of a Personality Module is to collect data from the System-Under-Test and transfer it to the Logic Analyzer along with appropriate format and display information.

In the PM 101 General Purpose Personality Module this result is achieved by circuitry in one of five functional areas:

— Data Transfer Circuitry, including data, address, and control lines,

— Clock Transmission Circuitry, which converts the TTL "CLK IN" to ECL for rapid and buffered differential transmission to the Logic Analyzer,

— ROM Circuitry, which consists of 2k of Personality ROM with provision for a 2k, 4k, or 8k Custom ROM developed for custom disassembly,

— Control Circuitry, which interprets the status of the LOOK and /SEL P lines and buffers /HALT S.U.T. into /STOP S.U.T.,

— Self Test Stimulus Circuitry, which generates signals for the module-analyzer system diagnostics.

NOTE

A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies

0 — Write
1 — Read

Figure 4-1 is a Circuit Block Diagram which organizes the circuitry and shows the signal flow. It should be useful in gaining an overview of circuit operation, in troubleshooting certain problems, and understanding the Detailed Circuit Descriptions which follow.

DETAILED CIRCUIT DESCRIPTION

Data Transfer Circuitry

The data transfer circuitry is on board A1 and appears on schematic 1A.

All Data (DIØ—DI15), Address (AIØ—AI23), and Control (CIØ—CI9) lines are protected against static discharge, which could damage the Personality Module or Logic Analyzer circuitry, by hybrid ICs containing spark-gaps, series resistors, and clamp diodes. Each hybrid protects four input lines. The Control lines pass through A1U5045, A1U4050, and A1U4043. The Data lines pass through A1U2033, A1U1052, A1U2043, and A1U1041. The Address lines are protected by A1U4036, A1U4032, A1U3034, A1U3042, A1U3044 and A1U3040.

After passing through the protection hybrids, the Data, Address, and Control inputs are buffered by 74LS244 Octal Buffer ICs, so that the System-Under-Test is only subjected to a small amount of loading. The Control lines are buffered by A1U5041 and A1U4041. The Data lines are buffered by A1U2031 and A1U2041. The Address lines are buffered by A1U5031, A1U3031, A1U3041, and A1U4041.

When these buffers are in a "0" state and the voltage is increasing, they require approximately 1.6 V of input to switch them to a "1" state. However, when they are in a "1" state and the input voltage is decreasing, it must go as low as approximately 1.2 V before being interpreted as a "0". This hysteresis effect provides enhanced protection against noise and glitches on the line.

The buffers are matched to the impedance of the lines they drive by 68 Ω series terminating resistors.

Clock Transmission Circuitry

The clock transmission circuitry is on board A1 and appears on schematic 1B.
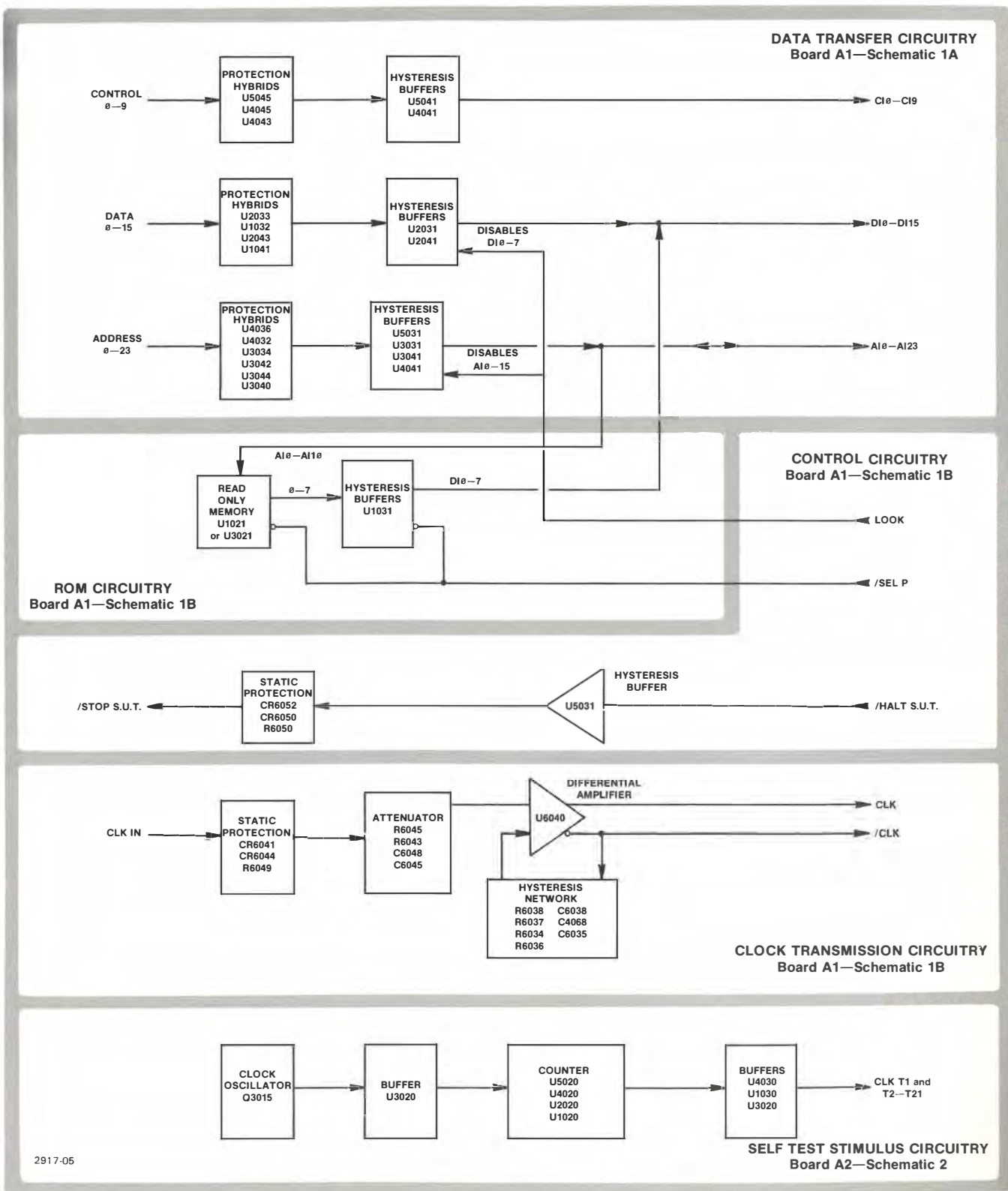
Fig. 4-1. PM 101 Circuit Block Diagram.

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4-2

The CLK IN signal is protected against static discharge by a spark gap, a series resistor (A1R6049) and clamping diodes (A1CR6041 and A1CR6044). The series RC network (A1R6045 and A1C6048) and the RC network to ground (A1R6043 and A1C6045) attenuate this signal (4:1), while presenting a high impedance to the system under test.

The circuitry between pin 8 and pin 3 of differential amplifier A1U6040 provides hysteresis for enhanced noise immunity. Resistors A1R6037, A1R6034, and A1R6036 comprise a voltage divider which couples part of the differential amplifier's negative output signal on pin 8 back to its negative input on pin 3. The voltage output of A1U6040 varies a total of 800 mV between a logical "1" and a logical "0". Only 120 mV of this variation reaches the series input resistor A1R6038 and pin 3 of A1U6040. This voltage swing is multiplied by a factor of four as a result of the effect of A1R6045 and A1R6043 in attenuating the input voltage. The result is about 500 mV of effective DC hysteresis on pin 2 of A1U6040.

The capacitors parallel to these resistors provide frequency compensation so that rapid transitions are subject to a similar hysteresis effect.

Delay through the Clock Transmission Circuitry is less than the delay through the Data Transfer Circuitry, ensuring that the Logic Analyzer has clock information in advance of changes on the Data, Address and Control lines.

ROM Circuitry

The Read-Only-Memory is on board A1 and appears on schematic 1B.

The Read-Only-Memory, A1U1021, contains information with which the Logic Analyzer will format data displays and set up the word recognizer formats for different radix selections, decode the data from the system-under-test and interpret the personality module diagnostics.

The ROM is first read by the Logic Analyzer before actual data acquisition to help format the Logic Analyzer's word recognizer, set up the acquisition hardware, and determine whether the user will be able to define clock qualifications. Then it is read again, after data acquisition, to format the data for disassembly and display.

The standard 2k version of this ROM is accessed by eleven Address lines (AIØ through AI1Ø), although two additional Address lines (AI11 and AI12) may be strapped in for use with 4k or 8k custom ROMs. Refer to Table 4-1

for specific strapping configurations, and to the page in front of schematic 1B for a component location diagram.

TABLE 4-1
ROM Straps—A1 Board

ROM	P3032	P3034	P3036
G.P. 2k	3-4	3-4	4-5
G.P. 4k	3-4	2-3	2-3
G.P. 8k	4-5	1-2	1-2
Custom 2k	2-3	3-4	4-5
Custom 4k	2-3	2-3	2-3
Custom 8k	1-2	1-2	1-2

Control Circuitry

The control circuitry is on board A1. Refer to schematic 1A and 1B.

Normally the Address and Data lines carry information originating in the System-Under-Test. But, before and after data acquisition, the Logic Analyzer shuts off part of this information in the Personality Module and reads the Personality Module ROM over these lines instead. When the Logic Analyzer wants data from the Personality Module ROM, it first causes LOOK to go to its "1" state, which forces Address buffers AI0 through AI15 (A1U3041, A1U3031, and A15031) and Data buffers DI0 through DI7 (A1U2031) in the Data Transfer Circuitry of the Personality Module to go to their "High-Z" state (neither "1" nor "0" asserted). Refer to Fig. 4-2.

NOTE

A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies

0 — Write
1 — Read

The Logic Analyzer next causes /SEL P to go low and applies the address of the information it wants to the Address lines. When the resulting data has settled, the Logic Analyzer reads the Data lines and simultaneously returns /SEL P to its high ("1") state. The Address lines from the Logic Analyzer are also returned to their "High-Z" state at this time.

Last, LOOK goes back to "0" and the Address and Data buffers are no longer inhibited. The information going to the Logic Analyzer is again the information from the system-under-test rather than the Personality Module ROM.
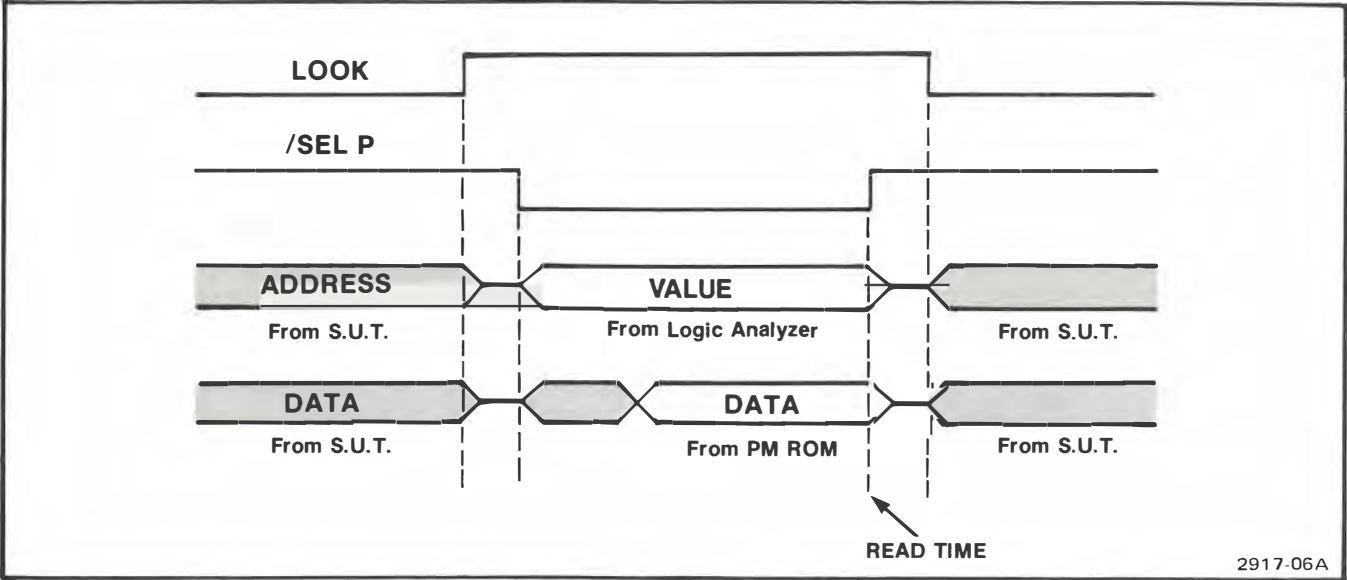
Fig. 4-2. How the Logic Analyzer reads the ROM.

/STOP S.U.T. is a buffered (A1U5031) output version of the input /HALT S.U.T. from the Logic Analyzer. It is protected by a spark-gap, a 100 Ω series resistor (A1R6050), and clamping diodes (A1CR6052 and A1CR6050). (This signal is labeled "HALT" on the Personality Module cover.)

Self Test Stimulus Circuitry

The Self Test Stimulus Circuitry is located on board A2 and appears on schematic 2.

The Self Test Stimulus Circuitry consists of a free running 16-bit counter (A2U5020, A2U4020, A2U2020, and A2U1020) whose input, T1 (A2U3020-4) is oscillating at a frequency of approximately 10 MHz.

T1 through T17 are the free-running counter outputs. T1 is the approximately 10 MHz clock rate generated by the A2Q3015 circuitry and buffered by A2U3020, while T17 is the slowest bit, running at about 76 Hz. T2 through T17 and T21 are buffered by A2U4030 and A2U1030.

T18, T19 and T20 are ripple carry outputs from A2U5020, A2U4020, and A2U2020, the first three ICs in the four-IC counter. These outputs are buffered by A2U3020.

See Sections 5 and 6 for information on how to use the Self Test Stimulus outputs.

PERFORMANCE CHECK

Introduction

This section provides a procedure for verifying that the PM 101 General Purpose Personality Module is operating correctly. It is assumed that the Logic Analyzer has already passed its performance check. If it has not, it should be checked first; refer to Section 3 of the 7D02 Service manual.

A technician familiar with running this test will probably be able to run it in about two hours. Someone using this procedure for the first time should expect it to take approximately twice that long. When a module passes this check, it is meeting all of the electrical performance specifications listed in Section 3 of this manual.

Test Equipment Required

The test equipment listed in Table 5-1 is required for a complete performance check of the PM 101. Detailed operating instructions for use of the test equipment are not included in the Performance Check Procedure. Refer to the appropriate test equipment manuals for more information.

Test Fixtures

Refer to Fig. 5-1 and assemble two test fixtures as follows: loosen the binding post screws on a BNC to binding post adapter, insert a separate piece of 22-gauge wire through each post, tighten the screws, and bend the wires in opposite directions. (For most effective use, insert the wires so that all of the excess length is to one side.)
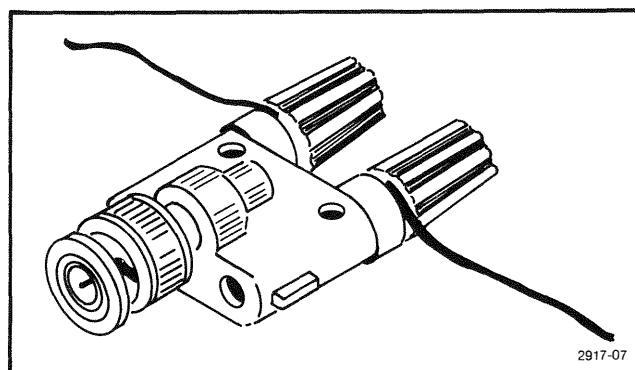
Fig. 5-1. An Assembled Test Fixture.

TABLE 5-1

TEST EQUIPMENT REQUIRED

Item (w/ Tek. Number)	Familiar Name	Purpose
Logic Analyzer (7D02) w/Opt. 3 (Expansion)	7D02	To provide a system for the PM 101 to be a part of.
Oscilloscope mainframe (7603, 7704A, or other appropriate mainframe)	Mainframe	To provide the facilities necessary to operate the 7D02.
Oscilloscope, 200 MHz bandwidth, dual-trace, calibrated 1 ns/div resolution	Test oscilloscope	Examination of pulse generator signals.
P6106 Passive probe 250 MHz, 10X, 10 MΩ (Tektronix Part No. 010-6106-03)	Oscilloscope probe	Oscilloscope input (2 required)
Pulse Generator (PG 502)	PG 502	To provide clock pulses to the PM 101.
Pulse Generator (PG 508)	PG 508	To provide data pulses to the PM 101 and triggering for the PG 502.
Test Equipment Mainframe (TM 504)	TM 504	To provide facilities necessary to operate the above two items.
Coaxial cable, 50 Ω	Coax cable	Signal connection.
Bnc male to dual binding post adapter (Tektronix Part No. 103-0035-00)	Bnc to Binding Post Adapter	To make test fixtures (2 required)
50 Ω Feedthrough termination (Tektronix Part No. 011-0049-01)	50 Ω Termination	Signal termination
Test lead, black (Tektronix Part No. 012-0426-01)	Black test lead	Signal connection
Test lead, red (Tektronix Part No. 012-0426-00)	Red test lead	Signal connection.

Connecting the Self-Test Stimulus

a. Turn off power to the Logic Analyzer at the oscilloscope mainframe.

b. Remove the plastic cover on the back of the Personality Module using a small screwdriver or Allen wrench.

c. Move the strapping connector from the power-off position to the power-on position as shown in Fig. 5-2.

d. Connect the Data, Address, Control and Clock leads on the PM 101 to the Self-Test Stimulus pins, as indicated in Table 5-2 and shown in Fig. 5-3.

TABLE 5-2

SELF-TEST STIMULUS CONNECTION

Connector	PM 101 Individual Test Leads					
	Data	Address	Address	Qualifiers	Timing	Other
T2	D0	A0			Black	
T3	D1	A1			Brown	
T4	D2	A2			Red	
T5	D3	A3			Orange	
T6	D4	A4			Yellow	
T7	D5	A5			Green	
T8	D6	A6			Blue	
T9	D7	A7			Violet	
T10	D8	A8	A16	Q0		
T11	D9	A9	A17	Q1		
T12	D10	A10	A18	Q2		
T13	D11	A11	A19	Q3		
T14	D12	A12	A20	Q4		
T15	D13	A13	A21	Q5		
T16	D14	A14	A22			
T17	D15	A15	A23			
T18				Q6		
T19				Q7		
T20				Q8		
T21				Q9		
Clock						Grey
TS						Red
GND					White	Black

OFF   ON

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Fig. 5-2. Power Strapping—Self Test Stimulus Circuitry.

2917-09
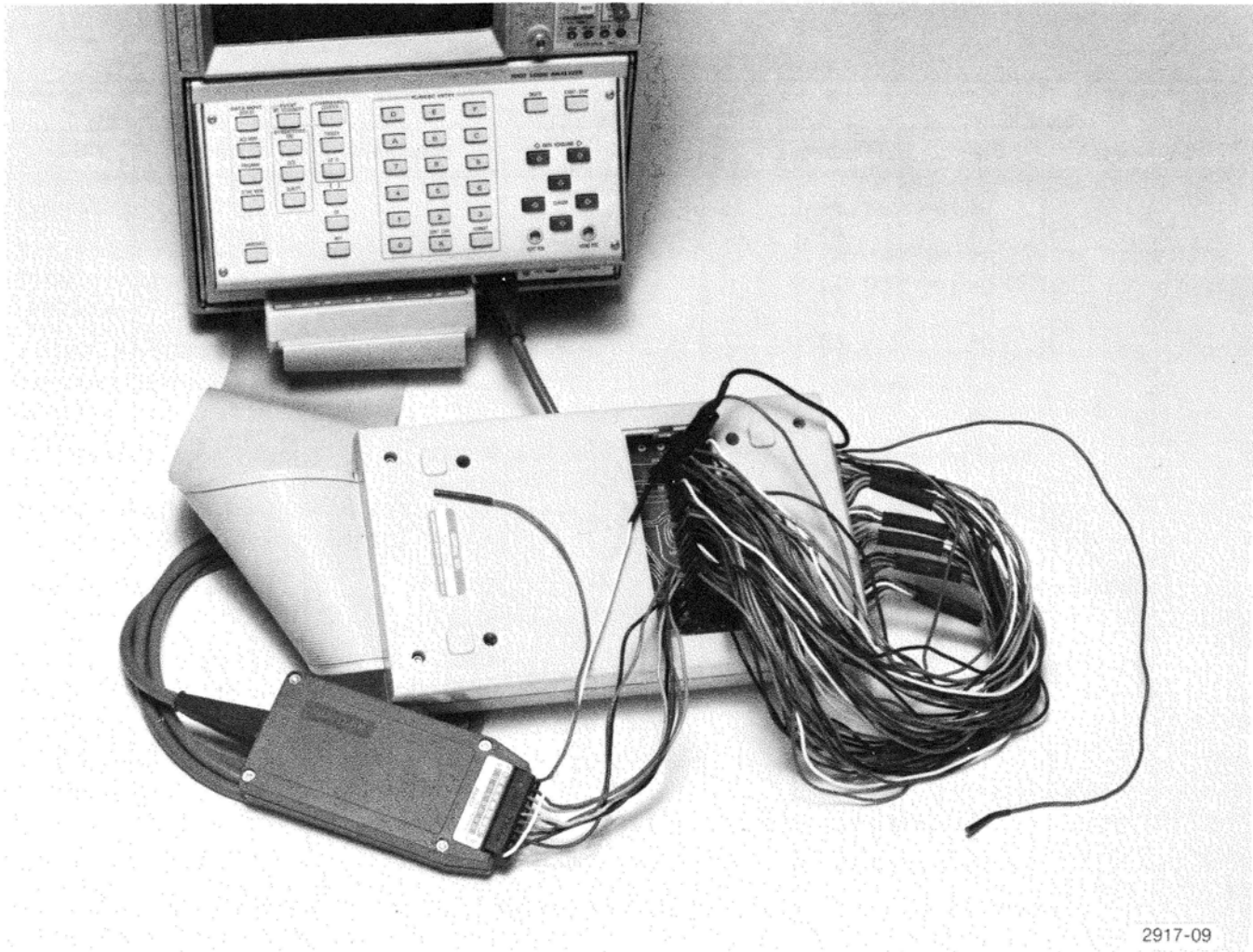
Fig. 5-3. Self Test Stimulus Connection.

PERFORMANCE CHECK

1. Diagnostics. Run the "PER. MOD. — SYSTEM" Diagnostic Module with LOOPING ENABLED for at least five seconds for each of the eight individual tests using the following procedure:

⚠️ { *CAUTION* }

Always be certain to turn off the mainframe (logic analyzer) power before connecting or disconnecting any Personality Module.

a. Turn off the mainframe power and insert the ribbon cable connector "PERSONALITY MODULE — PM 100 SERIES" into the receptacle labeled "PERSONALITY MODULE — PM 100 SERIES" on the front of the Logic Analyzer.

b. Turn on the mainframe power and depress any front panel key within two seconds. Keep the key depressed for at least five seconds to simulate a keyboard failure, bring up the POWER-UP VERIFICATION display and allow entry into the DIAGNOSTIC MONITOR.

c. Press "X" to get a menu of the Diagnostic Monitor.

d. Press "9" to run the "PER. MOD. — SYSTEM" Diagnostic Monitor.

e. Press "E" to ENABLE LOOPING. (The Self-Test Stimulus was connected in an earlier procedure.)

@

f. Press the START/STOP key to run the first test. Wait five seconds. A number such as 0853-XX associated with a "PASS" of Test #1 is normal. The number is the part number of the ROM package.

g. Press the START/STOP key to run the next test. Wait five seconds.

h. Repeat step "g" until all eight tests have been completed.

i. Check to verify that all tests passed. Note the messages associated with any errors. A number associated with any test other than Test #1 is an error indication. A number associated with a "PASS" indicates that the error was transient. Record these numbers and refer to Section 6, Maintenance and Troubleshooting.

j. Press the START/STOP key and the "X" key to return to the Diagnostic Monitor menu.

k. Press "B" to run the TIMING OPTION test.

l. Press "E" to ENABLE LOOPING.

m. Press the START/STOP button three times to enter test #3.

n. Wait five seconds and press the START/STOP button.

o. Check to verify that Test B3 passes. Record any error messages. A number associated with a PASS indicates a transient error. (Failures of sub-tests other than sub-test 3 probably are not Personality Module failures; refer to the 7D02 Logic Analyzer Service manual, Maintenance and Troubleshooting section, for the "Pers. Mod.—Sys." diagnostic flowchart.)

p. Press the START/STOP key and the "X" key to RETURN TO MENU.

q. Press the "X" key again to return to normal operation.

2. HALT Circuit Functional Check

a. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

b. Move the CURSOR to the end of any existing program and hold the DELETE key until the entire program is deleted.

c. Press the TRIGGER key.

d. Move the CURSOR to the Trigger Delay Field and enter a "3" to select ZERO DELAY.

e. Enter a "1" to select SYSTEM UNDER TEST HALT.

f. Move the CURSOR to the bottom of the program and press the WD RECOGNIZER key.

g. Enter all "0"s in the Data Field.

h. Press the TRIGGER and END keys. Check that the program is as shown in Fig. 5-4.
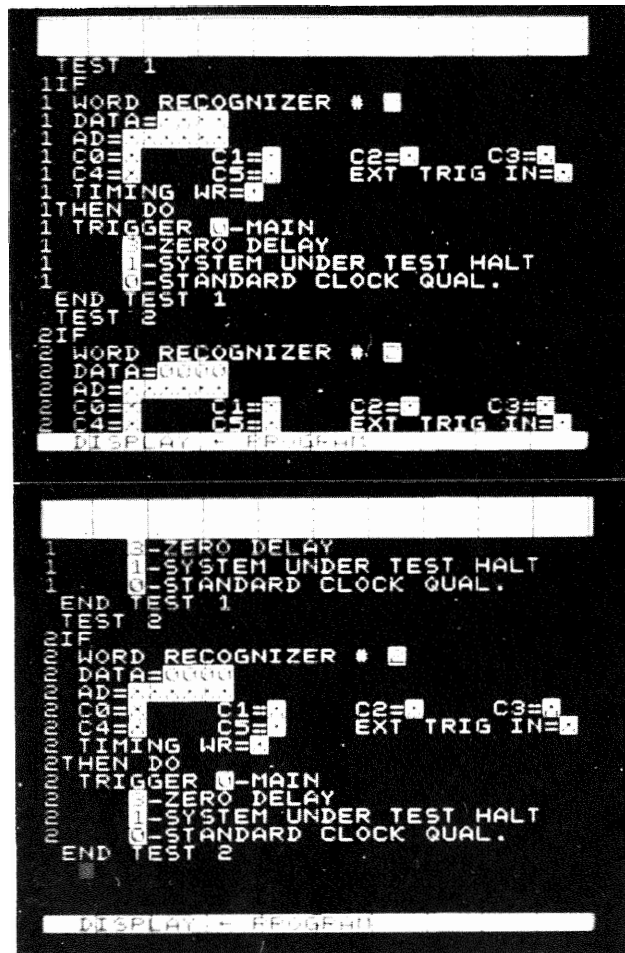
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Fig. 5-4. HALT Check Program.

i. Press the IMMEDIATE, GO TO, and "2" keys, and then move the CURSOR to the right (EXECUTE).

j. Check that the trigger occurs on DATA 0000.

k. Press the START/STOP key.

l. Check that the trigger occurs on DATA 0003.

m. Press the START/STOP key at least four more times.

n. Verify that the DATA increments by 3 on each occasion.

3. Clock Checks. This procedure checks minimum clock pulse width (25 ns), minimum clock period (100 ns), minimum data acquisition period (100 ns) and minimum interval between qualified clocks.

a. Move the Self-Test Circuitry power jumper from its power-on to its power-off position. Refer to Fig. 5-2.

b. Turn on power to the mainframe oscilloscope, the test oscilloscope, and the TM 504. Allow 20 minutes for the equipment to warm up.

c. Set the PG 508 TRANSITION TIME and DELAY controls fully counterclockwise to their minimum positions.

d. Set the PG 508 LEADING and TRAILING edge controls fully counterclockwise to their minimum, "X1" position.

e. Set all three PG 508 TRIGGERING switches to their out positions.

f. Set the PG 508 MODE switches for the DELAYed mode by pushing the lower switch to its latched-in position.

g. Connect a 50 Ω feed-thru termination to the PG 508 OUTPUT connector. Refer to Fig. 5-5.

h. Connect a test fixture to the 50 Ω feed-thru termination on the PG 508 OUTPUT connector.

i. Connect the test oscilloscope Channel 1 probe to the test fixture; ground to black, tip to red. See Fig. 5-5.

j. Set the PG 508's PERIOD control to 20 ns and adjust the PERIOD-CAL control for a 100 ns period as measured on the test oscilloscope, Channel 1. (It may be necessary to set the DURATION control to its minimum position.)

k. Set the test oscilloscope Channel 1 POSITION controls so that the center graticule line represents +1.4 V, by setting the VOLTS/DIV switch to 1 VOLT/DIV, switching the AC-GND-DC switch to its GND position, and positioning the trace 1.4 divisions below the center graticule line. Return the AC-GND-DC switch to its DC position.

l. Using Channel 1 on the test oscilloscope to measure the signal voltage, adjust the PG 508 OUTPUT (VOLTS) control for a pulse with a high level of 2.4 V and a low level of +0.5 V.

m. Adjust the PG 508 DURATION-CAL control for 45 ns with the DURATION switch in the "10 ns" position.

n. Connect one of the PM 101 ground leads to the PG 508 Test Fixture's black terminal.

o. Connect Data lines 3 through 0 from the PM 101 to the Test Fixture's red terminal using the Grabber Tips which are standard accessories to the PM 101. Refer to Fig. 5-5.

p. Using coaxial cable, connect the PG 508 + TRIG OUT connector to the + TRIG/DURATION INPUT connector on the PG 502.

q. Connect the other Test Fixture to the PG 502 OUTPUT connector.

r. Connect the test oscilloscope Channel 2 probe ground to the PG 502 Test Fixture's black terminal.

s. Connect the test oscilloscope's Channel 2 probe tip to the red side of the PG 502 Test Fixture.

t. Pull out the BACK TERM switch on the PG 502.

u. Press the NORM/COMPLEMENT switch on the PG 502 to invert its output.

v. Turn the PG 502 PERIOD control fully clockwise to the EXT TRIG position.

w. Set the PULSE DURATION control on the PG 502 to the "5 ns" position and adjust the PULSE DURATION-VARIABLE control for a 25 ns pulse on Channel 2 of the Test Oscilloscope.

x. Using Channel 1 on the test oscilloscope to measure the signal voltage, set the PG 502 output pulse for a high level of 2.4 V and a low level of +0.5 V.

y. Connect one of the PM 101 ground leads to the PG 502 Test Fixture's black terminal.
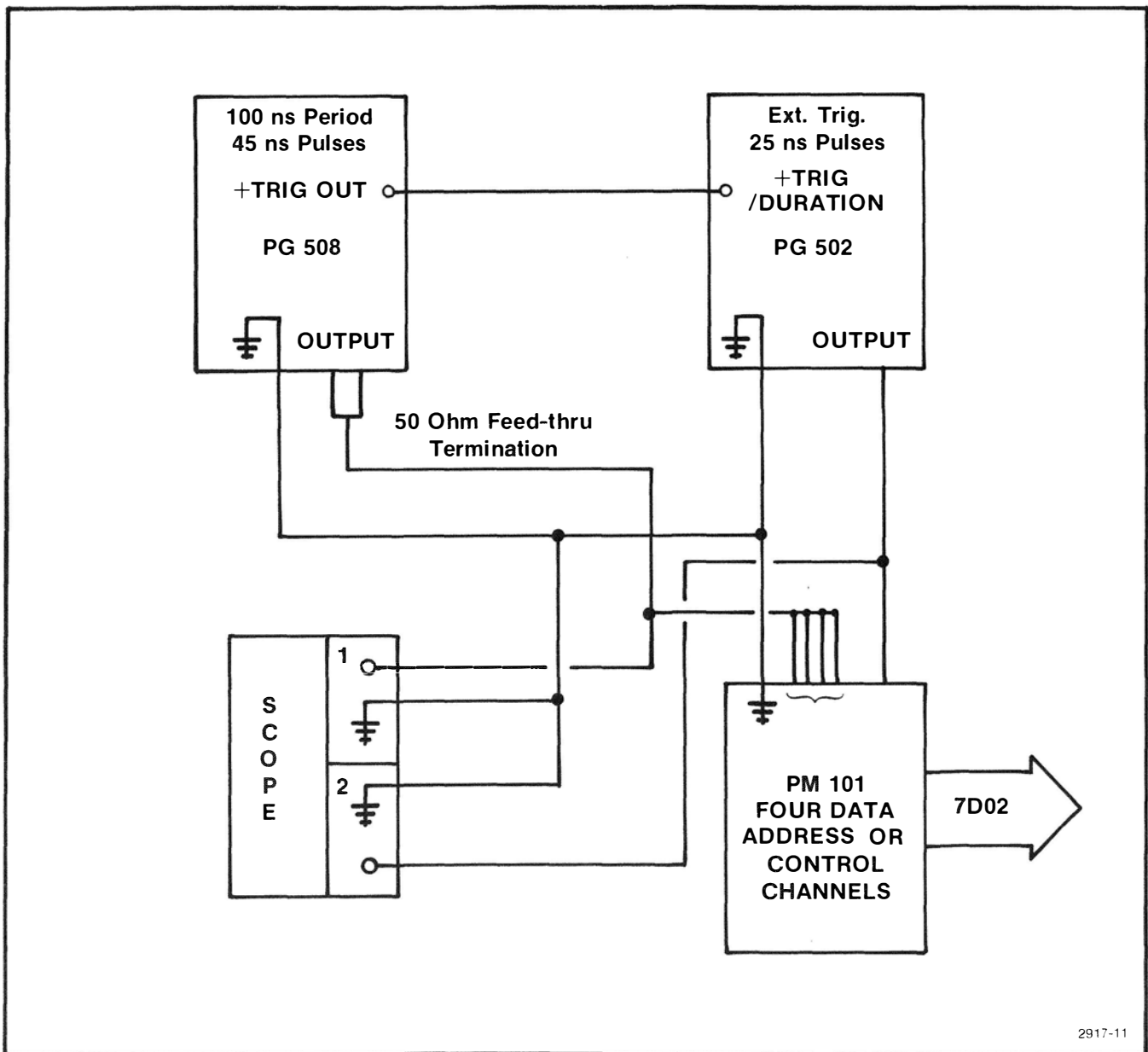
Fig. 5-5. Equipment Set-up—Clock Checks.

z. Connect the PM 101 Clock line (single grey lead) to the PG 502 Test Fixture's red terminal.

aa. Adjust the PG 508 DELAY controls so that trailing edge of the inverted PG 502 pulse is coincident with the trailing edge of the non-inverted PG 508 pulse at the center graticule line of the test oscilloscope. (Trigger on channel 2.)

ab. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

ac. Move the CURSOR to the end of any existing program.

ad. Press and hold the DELETE key until the entire program is deleted.

ae. Press the COUNTER key and enter 10,000 events.

af. Press the [ ] (brackets) key.

ag. Press the COUNTER key, move the CURSOR to the left, and enter 2 to select Counter #2.

ah. Enter "1" twice to select "μs" and the STOP command.

ai. Press the GOTO key.

aj. Press the [ ] (brackets) key twice.

ak. Press the NOT key and the WD RECOGNIZER key.

al. Enter a hexadecimal "F" in the rightmost Word Recognizer Data position.

am. Press the [ ] (brackets) key twice.

an. Press the TRIGGER key.

ao. Move the CURSOR down once to the Trigger Position field and enter a "3" to select ZERO DELAY and another "0" to select SYSTEM UNDER TEST CONTinue.

ap. Enter a "0" to select STANDARD CLOCK QUALification.

aq. Press the GOTO key and enter a "3".

ar. Press the [ ] (brackets) key.

as. Press the ELSE key.

at. Press the [ ] (brackets) key.

au. Press the COUNTER key.

av. Press the COUNTER key, move the CURSOR to the left, and enter "2" to select Counter #2.

aw. Press the [ ] (brackets) key twice.

ax. Press the COUNTER key, move the CURSOR to the left, and enter "2" to select Counter #2.

ay. Enter 01050 μs.

az. Press the OR key.

ba. Press the NOT key.

bb. Press the WD RECOGNIZER key, move the CURSOR up and enter "1" as its number.

bc. Move the CURSOR to the bottom of the program and press the [ ] (brackets) key.

bd. Press the GOTO key. (Default "3" is correct.)

be. Press the ELSE key.

bf. Press the [ ] (brackets) key.

bg. Press the COUNTER Key.

bh. Move the CURSOR down and enter "1" to select the RESET command.

@

bi. Press the COUNTER key, move the CURSOR to the left and enter a "2" to select Counter #2.

bj. Move the CURSOR down and enter "2" to select the RESET AND RUN command.

bk. Press the GOTO key and enter "1".

bl. Press the [ ] (brackets) key.

bm. Press the END key twice to end Test 2 and to create and end Test 3.

bn. Check that the program is as shown in Fig. 5-6.

bo. Press START/STOP key to run program.

bp. Check that the program runs continuously with no trigger.

bq. Wait approximately 15 seconds and press the START/STOP key.

br. The display should show LOCation 254, indicating that 255 data groups were stored.

bs. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

bt. Move the CURSOR to the Clock Qualification field in Test 1 and enter "1" to select USER CLOCK QUALification.

bu. Enter "1" to select FALLING EDGE OF CLOCK.

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Fig. 5-6. Clock Checks Program.

bv. Set the PG 502 COMPLEMENT/NORM switch to its out position to return the output to its normal, non-inverted form.

bw. Check that the PG 502 output pulse on the Test Oscilloscope display is positive-going and of 25 ns duration and that the trailing edges of the pulses are coincident.

bx. If the pulse duration is not 25 ns, adjust the PG 502 PULSE DURATION-VARIABLE control. Adjust the PG 508 DELAY-CAL control if the trailing edges are not coincident.

by. Press the START/STOP key to run the program.

bz. Check that the program runs continuously for at least 15 seconds.

ca. Press the START/STOP key to stop the program and verify that the last LOCation stored was 254.

cb. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

cc. Move the CURSOR to the Word Recognizer Data field and enter a hexadecimal "0" in the least significant digit.

cd. Set the PG 508 COMPLEMENT/NORM switch to its in position to invert the output.

ce. Check that the PG 508 output pulse on Test Oscilloscope display is negative-going and of 45 ns duration and that its trailing edge is coincident with the trailing edge of the positive-going PG 502 output pulse.

cf. If the pulse duration is not 45 ns, adjust the PG 508 DURATION-CAL control. Adjust the PG 508 DELAY-CAL control if the trailing edges are not coincident.

cg. Press the START/STOP key to run the program.

ch. Check that the program runs continuously for at least 15 seconds.

ci. Press the START/STOP key to stop the program and verify that the last LOCation stored is 254.

cj. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

ck. Move the CURSOR to the Clock Edge field and enter "0" to select RISING EDGE OF CLOCK.

cl. Set the PG 502 COMPLEMENT/NORM switch to its in position to invert its output.

cm. Check that the PG 502 output pulse on the Test Oscilloscope display is negative-going and of 25 ns duration and that its trailing edge is coincident with the trailing edge of the negative-going pulse from the PG 508.

cn. If the pulse duration is not 25 ns, adjust the PG 502 PULSE DURATION-VARIABLE control. Adjust the PG 508 DELAY-CAL control to make the trailing edges coincident.

co. Press the START/STOP key to run the program.

cp. Check that the program runs continuously for at least 15 seconds.

cq. Press the START/STOP key and verify that the last LOCation stored is 254.

4. Setup and Hold Check—Main Section. This routine checks all of the Data channels, all of the Address channels, and Control channels C0 through C3.

a. The PG 502 will not be used again. Use the same setup as in Check 3 above for the PG 508 with the following changes:

b. Connect the PM 101 Clock line and the test oscilloscope Channel 1 probe tip, as well as the first four data channels from the PM 101, to the red terminal of the Test Fixture connected to the PG 508.

c. Set the PG 508 PERIOD control to .2 μs and the center CAL control fully counterclockwise.

d. Press the PG 508 COMPLEMENT/NORM switch to its out position for a normal output.

e. Set the PG 508 DURATION control to 10 ns and adjust the DURATION-CAL control for a positive-going 45 ns pulse as displayed on the test oscilloscope.

@

f. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

g. Move the CURSOR to the end of the existing program.

h. Press and hold the DELETE key until the entire program is deleted.

i. Press the NOT key.

j. Press the WD RECOGNIZER key.

k. Move the CURSOR to the Word Recognizer Data field and enter a hexadecimal "F" in the location corresponding to the channels connected to the PG 508 in part "b" above or part "ad" below.

l. Press the [ ] (brackets) key.

m. Press the TRIGGER key.

n. Move the CURSOR to the Clock Qualification field and enter "1" to select USER CLOCK QUALification.

o. Enter "1" to select FALLING EDGE OF CLOCK.

p. Check that the display of the program is as shown in Fig. 5-7.

2917-27

Fig. 5-7. Main Section Setup and Hold Program.

q. Press the START/STOP key to run the program.

r. Check that the program continues to run for at least 15 seconds.

s. Press START/STOP key to stop the program.

t. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

u. Move the CURSOR to the Clock Qualification field and enter "0" to select RISING EDGE OF CLOCK.

v. Move the CURSOR to the appropriate Word Recognizer field and enter a "0" in the position corresponding to the channels being checked.

w. Set the PG 508 COMPLEMENT/NORM switch to the in position to invert the output.

x. Check that the pulse on the test oscilloscope display is negative-going and of 45 ns duration.

y. If the pulse duration is not 45 ns, adjust the PG 508 DURATION-CAL control.

z. Move the CURSOR to the Word Recognizer Data field and enter a hexadecimal "0" in the position of the lines being checked.

aa. Press the START/STOP key to run the program.

ab. Check that the program continues to run.

ac. Wait approximately 15 seconds, then press the START/STOP key.

ad. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

ae. Connect four different PM 101 channels to the Test Fixture and repeat parts "d", "e", "k", "n", "o", and "q" through "ad". Do this for the rest of the Data channels, all of the Address channels, and the four Control channels, CØ through C3.

@

5. Setup and Hold Check—ANDed Clocks

a. Perform parts "a" through "i" of Check 4 except parts "b", "d", and "e". Instead of those parts, connect Control lines C4, C5, and C6 and the test oscilloscope probe to the Test Fixture's red terminal and set the PG 508 PERIOD switch to 20 μs with the center CAL control fully counterclockwise. Adjust the DURATION-CAL control for a 55 ns pulse.

b. Press the ELSE and [ ] (brackets) keys.

c. Press the COUNTER key.

d. Enter a "1" to select μs.

e. Press the GOTO key.

f. Press the [ ] (brackets) key.

g. Press the ELSE key.

h. Press the GOTO key.

i. Press the [ ] (brackets) key.

j. Press the NOT and COUNTER keys.

k. Enter 00050 μs.

l. Press the [ ] (brackets) key twice.

m. Press the COUNTER key.

n. Move the CURSOR down to the Counter command field and enter a "2" to select the RESET AND RUN command.

o. Press the GOTO key and enter a "2".

p. Press the [ ] (brackets) key, then the ELSE key, and then the [ ] key again.

q. Press the TRIGGER key.

r. Move the CURSOR to the Trigger Delay field and enter a "3" to select ZERO DELAY.

s. Move the CURSOR to the Clock Qualification field, enter a "1" to select USER CLOCK QUALIFICATION, then another "1" to select FALLING EDGE OF CLOCK.

t. Move the CURSOR to the C9-C4 ANDed Clocks field and enter "1"s in the rightmost bit positions C6, C5, and C4 (the rest are "don't care").

u. Press the GOTO key and enter a "4".

v. Press the [ ] (brackets) key.

w. Press the END key to end Test 3, then again to end Test 4.

x. Check that the program is as shown in Fig. 5-8, Part A.
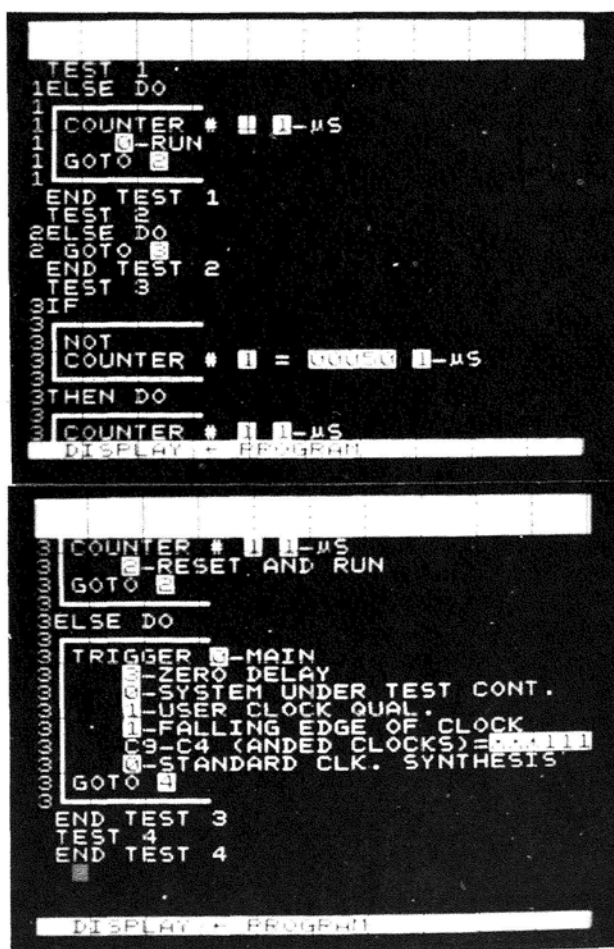
2917-28

Fig. 5-8. Part A. ANDed Clocks Setup and Hold Program.

y. Press the START/STOP key to run the program.

z. Check that the program continues to run, with no trigger and no SLOW CLOCK indication.

aa. Wait approximately 15 seconds and press the START/STOP key to stop the program.

ab. Check that 255 data words were stored in memory. (The last LOCation shown should be 254.)

ac. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

ad. Move the CURSOR to the Clock Edge Selection field and enter a "0" to select RISING EDGE OF CLOCK.

ae. Move the CURSOR to the C9-C4 ANDed Clocks field and enter 0's in bit positions C6, C5, and C4.

af. Check that the program is as shown in Fig. 5-8, Part B.
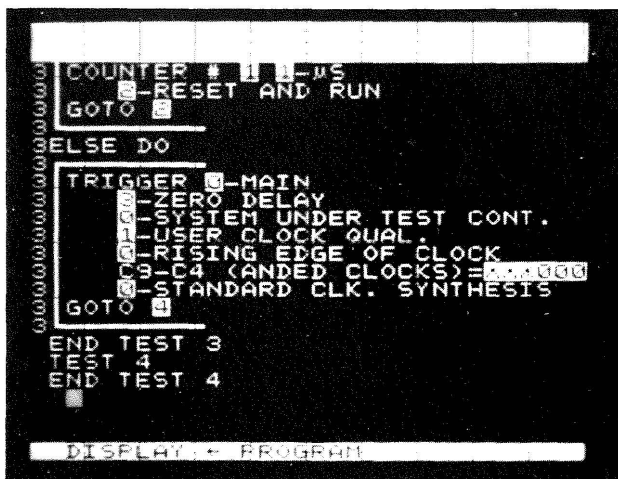
2917-29

Fig. 5-8. Part B. ANDed Clocks Setup and Hold Program.

ag. Set the PG 508 COMPLEMENT/NORM switch to its in position to invert the signal output.

ah. Check that the pulse on the test oscilloscope display is negative-going and of 55 ns duration.

ai. If the pulse duration is not 55 ns, adjust the PG 508 DURATION-CAL control.

aj. Press the START/STOP key to run the program.

ak. Check that the program continues to run with no trigger and no SLOW CLOCK indication.

al. Wait approximately 15 seconds and press the START/STOP key to stop the program.

am. Check that 255 data words were stored in memory. (The last LOCation shown should be 254.)

an. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

ao. Move the CURSOR to the C9-C4 ANDed Clocks field and enter "0"s in the leftmost bit positions C9, C8, and C7; enter "X"s in bit positions C6, C5, and C4.

ap. Check that the program is as shown in Fig. 5-8, Part C.

2917-30

Fig. 5-8. Part C. ANDed Clocks Setup and Hold Program.

aq. Disconnect PM 101 Control lines C6, C5, and C4 from the Test Fixture's red terminal and connect PM 101 control lines C9, C8, and C7 instead.

ar. Press the START/STOP key to start the program.

as. Check that the program continues to run with no trigger and no SLOW CLOCK indication.

at. Wait approximately 15 seconds and press the START/STOP key to stop the program.

@

5-13

au. Check that 255 data words were stored in memory. (The last LOCation stored should be 254.)

av. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

aw. Move the CURSOR to the Clock Qualification field and enter "1" to select FALLING EDGE OF CLOCK.

ax. Enter "1"s in C9-C4 ANDed Clocks field bit positions C9, C8, and C7.

ay. Check that the program is as shown in Fig. 5-8, Part D.

2917-31
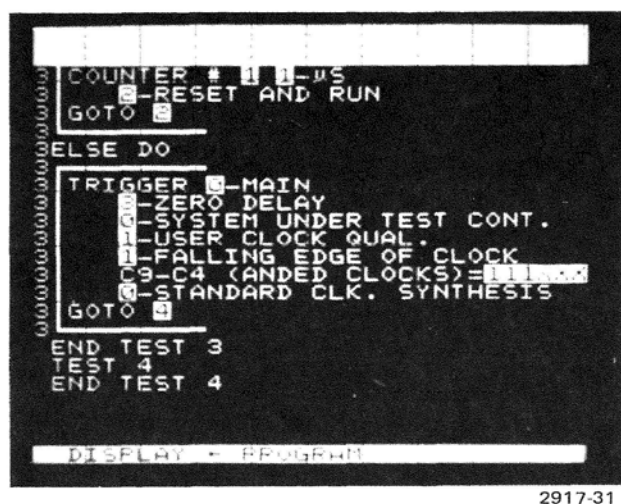
Fig. 5-8. Part D. ANDed Clocks Setup and Hold Program.

az. Set the PG 508 COMPLEMENT/NORM switch to its out position for a non-inverted output.

ba. Check that the pulse on the test oscilloscope display is positive-going and of 55 ns duration.

bb. If the pulse duration is not 55 ns, adjust the PG 508 DURATION-CAL control.

bc. Press the START/STOP key to start the program.

bd. Check that the program continues to run with no trigger and no SLOW CLOCK indication.

be. Wait approximately 15 seconds and press the START/STOP key to stop the program.

bf. Check that 255 data words were stored in memory. (The last LOCation stored should be 254.)

6. Setup and Hold Check—ESYNC and WAIT

ESYNC Section

a. Leave the test setup as it was at the end of the preceding check except Control lines C6 and C8 (ESYNC) and the test oscilloscope probe are connected to the Test Fixture's red terminal.

b. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

c. Move the CURSOR to the end of any existing program and DELETE it.

d. Press the COUNTER key, move the CURSOR to the left, and enter a "2" for the counter #.

e. Enter "00999" and a "0" to select EVENTS.

f. Press the [ ] (brackets) key and the TRIGGER key.

g. Move the CURSOR down and enter "3" to select ZERO DELAY.

h. Move the CURSOR down once to the Clock Qualification field and enter a "1" to select USER CLOCK QUALIFICATION.

i. Enter a "1" to select FALLING EDGE OF CLOCK.

j. Enter "X"s (don't cares) in C4 through C9.

k. Move the CURSOR to the Clock Synthesis field and enter a "1" to select USER CLOCK SYNTHESIS.

l. Enter "1" to select DIVIDE CLOCK BY 2 and a "2" as the divisor.

m. Enter a "1" in the ESYNC bit 6 position and press the COUNTER key.

n. Move the CURSOR down and enter a "1" to select the STOP mode for Counter #1.

o. Press the GOTO key.

p. Press the [ ] (brackets) key.

q. Press the ELSE key.

r. Press the [ ] (brackets) key.

s. Press the COUNTER key.

t. Press the COUNTER key and enter a "2" for the Counter #.

u. Press the [ ] (brackets) key.

v. Press the END key twice to end Tests 1 and 2.

w. Check that the program is as shown in Fig. 5-9.

x. Press the START/STOP key to run the program.

y. Check that the count stored in Counter #1 is between 19,000 and 21,000 μs.

z. Repeat parts x and y three or more times.

aa. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

ab. Move the CURSOR to the Divide Clock field and enter "3" to select DIVIDE CLOCK BY 3.

ac. Press the START/STOP key.

ad. Check that the program runs continuously with a SLOW CLOCK indication.

ae. Wait approximately 15 seconds and press the START/STOP key to stop the program.

af. Check that the display reads "NO DATA AC-QUIRED".

ag. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

ah. Move the CURSOR to the Clock Qualification field and enter a "0" to select RISING EDGE OF CLOCK.

ai. Move the CURSOR to the ESYNC C6 bit position and enter a "0".

aj. Set the PG 508 COMPLEMENT/NORM switch to its in position to invert the signal output.

ak. Check that the pulse on the test oscilloscope display is negative-going and of 55 ns duration.
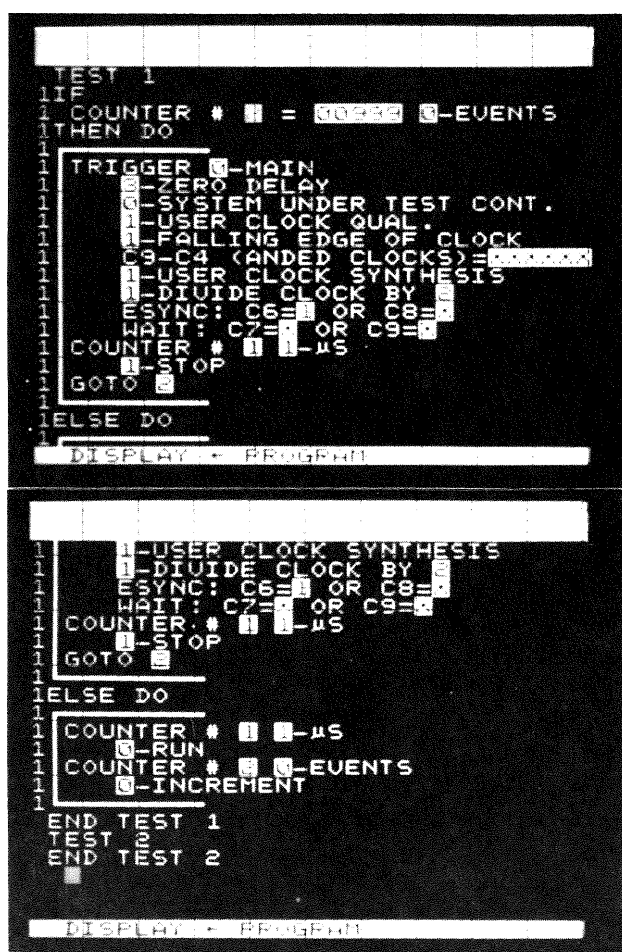
2917-32

Fig. 5-9. ESYNC Setup and Hold Program.

al. If the pulse duration is not 55 ns, adjust the PG 508 DURATION-CAL control.

am. Press the START/STOP key to run the program.

an. Check that the program runs continuously with a SLOW CLOCK indication.

ao. Wait approximately 15 seconds and press the START/STOP key to stop the program.

ap. Check that the display reads "NO DATA AC-QUIRED".

aq. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

ar. Move the CURSOR to the Divide Clock field and enter a "2" to select DIVIDE CLOCK BY 2.

as. Press the START/STOP key to run the program.

at. Check that the count stored in Counter #1 is between 19,000 and 21,000 μs.

au. Repeat parts as and at three or more times.

av. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

aw. Enter an "X" in the C6 bit position and a "0" in the C8 bit position.

ax. Press the START/STOP key to run the program.

ay. Check that the count stored in Counter #1 is between 19,000 and 21,000 μs.

az. Repeat parts ax and ay three or more times.

ba. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

bb. Move the CURSOR to the Divide Clock field and enter a "3" to select DIVIDE CLOCK BY 3.

bc. Press the START/STOP key to run the program.

bd. Check that the program runs continuously with a SLOW CLOCK indication.

be. Wait approximately 15 seconds and press the START/STOP key to stop the program.

bf. Check that the display indicates "NO DATA AC-QUIRED".

bg. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

bh. Move the CURSOR to the Clock Qualification field and enter a "1" to select FALLING EDGE OF CLOCK.

bi. Move the CURSOR to the ESYNC C8 bit position and enter a "1".

bj. Set the PG 508 COMPLEMENT/NORM switch to its out position to make the output non-inverted.

bk. Check that the pulse on the test oscilloscope display is positive-going and of 55 ns duration.

bl. If the pulse duration is not 55 ns, adjust the PG 508 DURATION-CAL control.

bm. Press the START/STOP key to run the program.

bn. Check that the program runs continuously with a SLOW CLOCK indication.

bo. Wait approximately 15 seconds and press the START/STOP key to stop the program.

bp. Check that the display reads "NO DATA AC-QUIRED".

bq. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

br. Move the CURSOR to the Divide Clock field and enter "2" to select DIVIDE CLOCK BY 2.

@

bs. Press the START/STOP key to run the program.

bt. Check that the count stored in Counter #1 is between 19,000 and 21,000 μs.

bu. Repeat parts bs to bt three or more times.

WAIT Section

bv. Disconnect PM 101 Control lines C6 and C8 (ESYNC) from the Test Fixture's red terminal and connect Control lines C7 and C9 (WAIT) to the red terminal.

bw. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

bx. Move the CURSOR to the ESYNC C8 bit position and enter an "X"; then enter a "1" in the WAIT C7 bit position.

by. Check that the program is as shown in Fig. 5-10.

bz. Check that the pulse in the test oscilloscope display is positive-going and of 55 ns duration.

ca. If the pulse duration is not 55 ns, adjust the PG 508 DURATION-CAL control.

cb. Press the START/STOP key to run the program.

cc. Check that the program runs continuously with a SLOW CLOCK indication.

cd. Wait approximately 15 seconds and press the START/STOP key to stop the program.

ce. Check that the display reads "NO DATA ACQUIRED".

cf. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

cg. Move the CURSOR to the ESYNC C7 bit position and enter an "X"; then enter a "1" in the C9 bit position.

ch. Press the START/STOP key to run the program.

ci. Check that the program runs continuously with a SLOW CLOCK indication.

cj. Wait approximately 15 seconds and press the START/STOP switch to stop the program.

ck. Check that the display reads "NO DATA ACQUIRED".

cl. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

cm. Move the CURSOR to the Clock Qualification field and enter a "0" to select RISING EDGE OF CLOCK.

cn. Move the CURSOR to the WAIT C9 bit position and enter a "0".
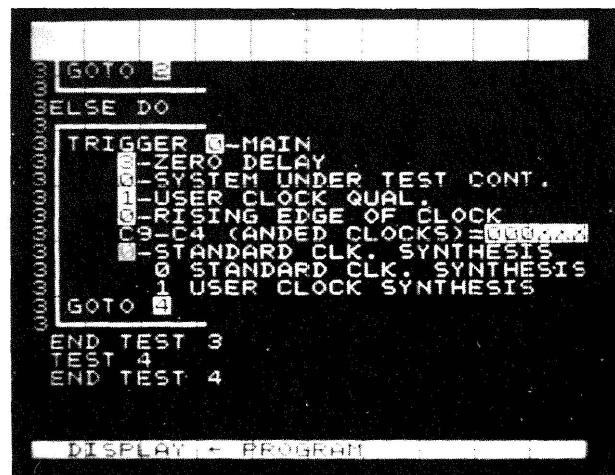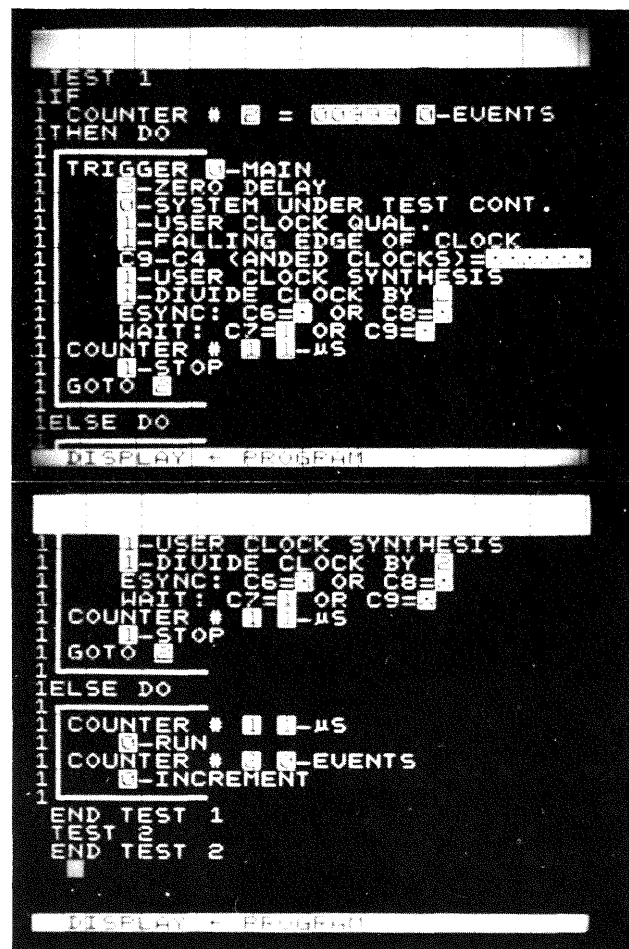

2917-33

Fig. 5-10. WAIT Setup and Hold Program.

co. Set the PG 508 COMPLEMENT/NORM switch to its in position to invert the signal output.

cp. Check that the pulse on the test oscilloscope display is negative-going and of 55 ns duration.

cq. If the pulse duration is not 55 ns, adjust the PG 508 DURATION-CAL control.

cr. Press the START/STOP key to run the program.

cs. Check that the program runs continuously with a SLOW CLOCK indication.

ct. Wait approximately 15 seconds and press the START/STOP key to stop the program.

cu. Check that the display reads "NO DATA ACQUIRED".

cv. Press the IMMEDIATE, DISPLAY, and PROGRAM keys.

cw. Move the CURSOR to the WAIT C7 bit position and enter a "0".

cx. Enter an "X" in the C9 bit position.

cy. Press the START/STOP key to run the program.

cz. Check that the program runs continuously with a SLOW CLOCK indication.

da. Wait approximately 15 seconds and press the START/STOP key to stop the program.

db. Check that the display reads "NO DATA ACQUIRED".

This completes the PM 101 Performance Check.

MAINTENANCE AND TROUBLESHOOTING

Cleaning and Periodic Maintenance

The PM 101 requires no periodic maintenance. Refer to Section 5 of this manual for a Performance Check if performance is in doubt. Operating circumstances will determine when the following cleaning procedure should be followed.

Exterior. Dust the Personality Module with a soft brush or cloth. Dirt should be removed with a cloth dampened in a mild solution of detergent and water.

CAUTION

DO NOT use chemical cleaning agents on the pod covers as they may damage the plastic. In particular, avoid solutions containing acetone, benzene, xylene or other organic solvents.

DO NOT use a cloth which is too damp or touch the connectors with the cloth.

Interior. Use a jet of low pressure air to remove dust from the interior of the pod and the circuit boards. A soft brush may be required. After soldering, or when otherwise required, use isopropyl alcohol with a soft cloth or cotton swab to remove flux, resin or dirt.

Service

The PM 101 Personality Module is a complex electronic instrument containing static sensitive components. It should only be serviced by qualified service personnel.

Tektronix, Inc. provides complete instrument service at local Field Service Centers and at the Factory Service Center in Beaverton, Oregon. Contact your local Tektronix representative or Field Office for additional information.

Ordering Parts

Most electrical and mechanical parts can be ordered through your local Tektronix Field Office or representative. However, you should be able to obtain many of the standard electronic components from a local commercial source in your area. Before you purchase or order a part from a source other than Tektronix, Inc., please check the Replaceable Mechanical Parts list, Section 9, for the proper value, rating, tolerance, and description.

When ordering parts from Tektronix, Inc. it is important to include the following information for each part ordered to ensure receipt of the correct parts:

1.   Instrument type (including modification and option numbers).

2.   Serial number of the instrument.

3.   A descriptive name or number; especially circuit and assembly numbers if it is an electrical part.

4.   Tektronix part number.

Disassembly

Remove the four middle screws from the top cover and lift it off. The top board (A1) is now accessible.

To gain access to the bottom board (A2), completely remove the two screws on the 64-pin connector end of the pod. Loosen, but do not remove, the two screws on the other end of the pod.

Gently lift the top board part way out of the pod at the free end. Grasp the bottom board and lift it gently out from under the top board. Refer to Fig. 6-1.

Turn the bottom board (A2) over and plug A2J1015 into A1P1015. Protect A2 from shorting and static discharge by placing appropriate materials between it and the environment. Figure 6-2 shows a PM 101 Personality Module in the accessible position with the Self Test Stimulus connected.

Self Test Stimulus

While the Logic Analyzer Power-Up Verification tests do not require any Self Test Stimulus, Tests 0, 9, and B of the more extensive Diagnostic Monitor do require that the operator make these connections.
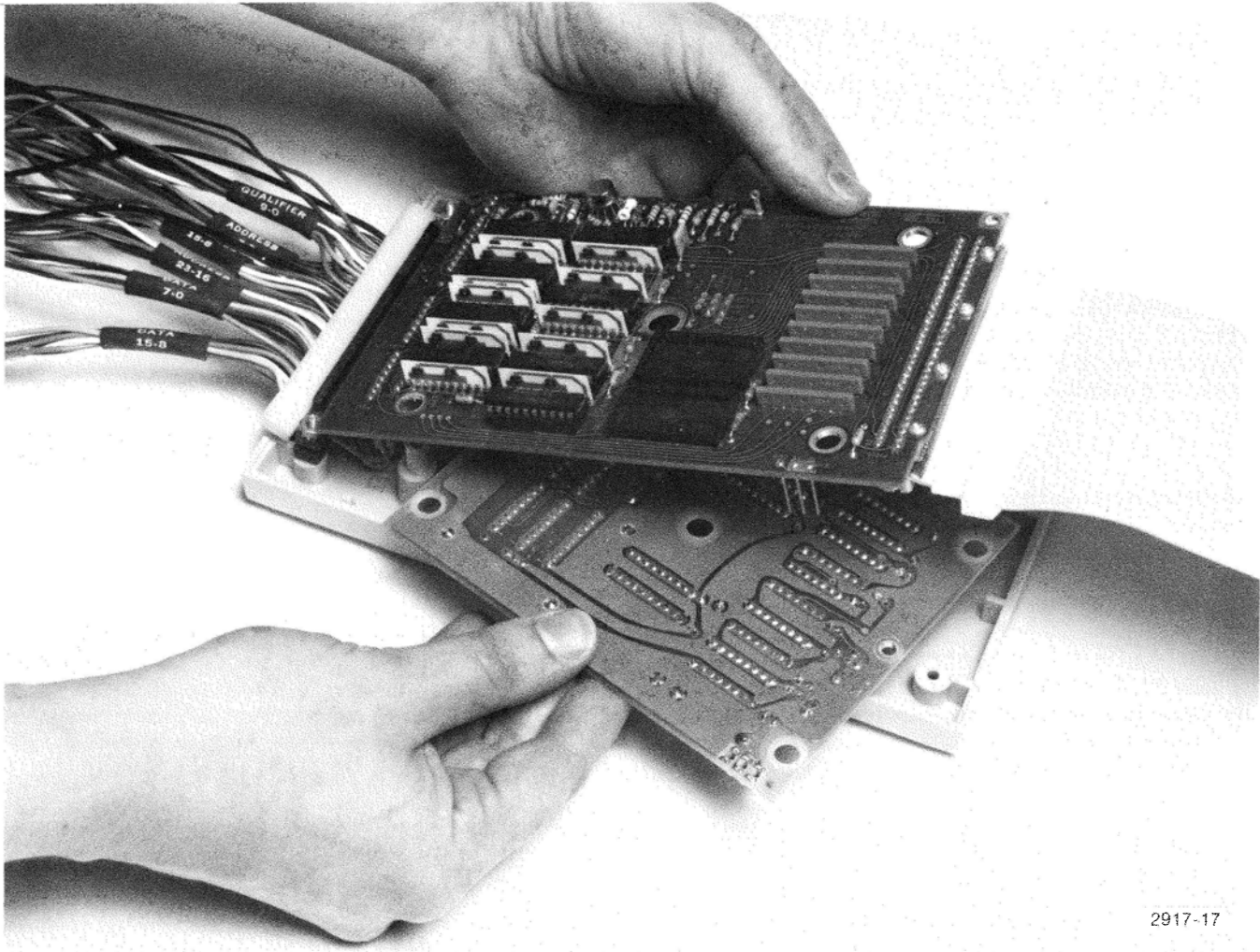
2917-17

Fig. 6-1. Removing Board A2.

Connect the Self Test Stimulus as indicated in Table 6-1 and the following procedure:

a. Turn off power to the Logic Analyzer and Personality Module with the mainframe power switch.

b. Remove the access cover on the bottom of the pod by inserting a small screwdriver into the slot and prying gently.

@

c. Connect all of the individual test leads to the Self Test Stimulus connectors as indicated in Table 6-1 and shown in Fig. 6-2.

d. Move the Self Test Circuitry power strap, A2J5050, from its power-off position (2-3) to its power-on position (1-2) as shown in Fig. 6-3.

e. Apply power to the Logic Analyzer and Personality Module by turning on the mainframe power switch.

f. To disconnect the Self Test Stimulus, perform steps a, c (in reverse), d (in reverse), b (in reverse), and e.

2917-18
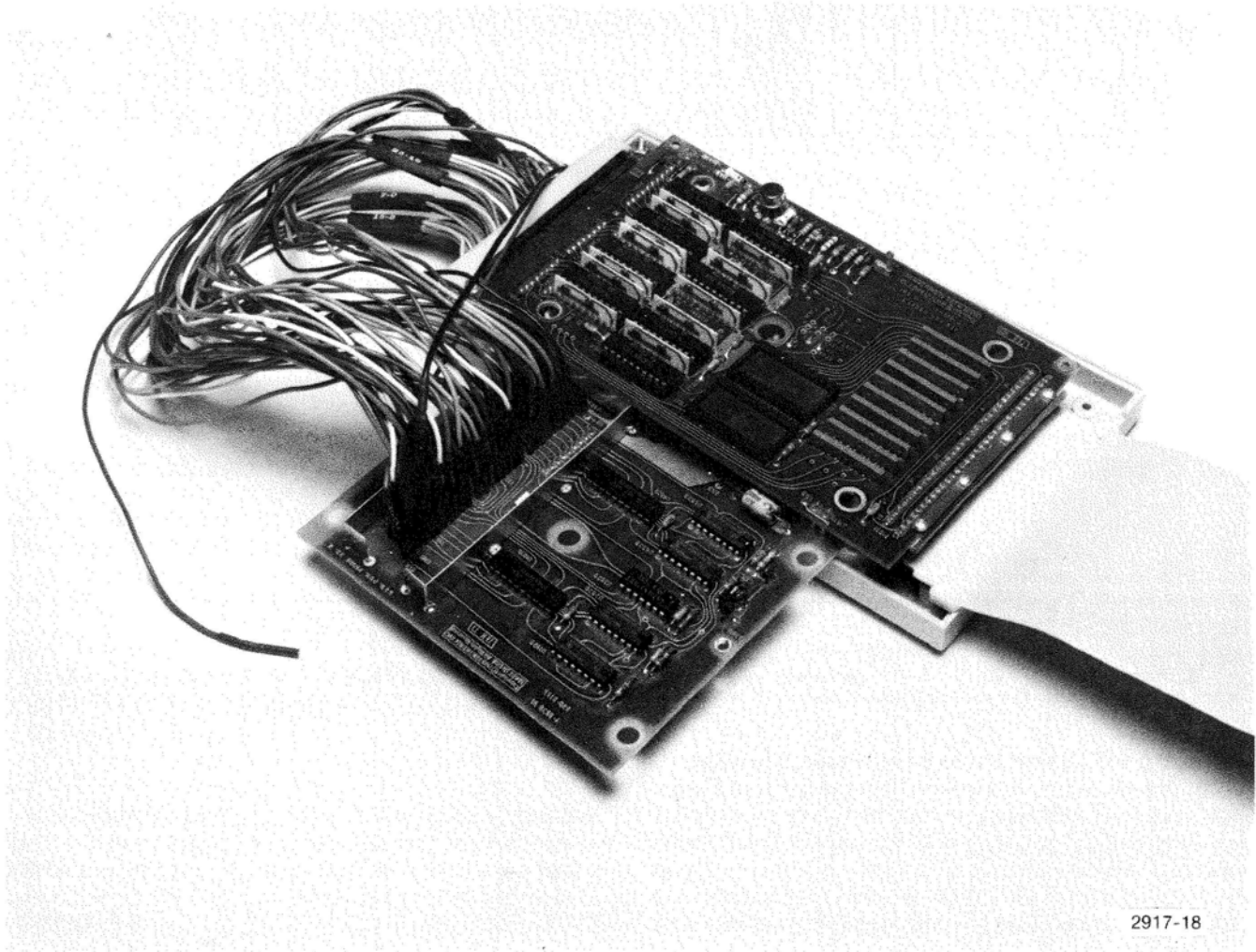
Fig. 6-2. Accessible Position—Self Test Stimulus Connected.

OFF   ON
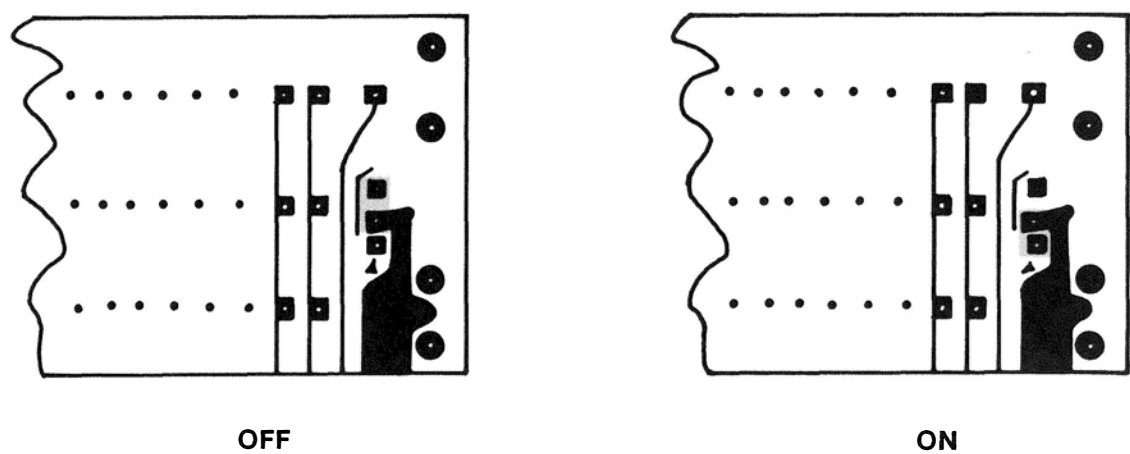
2917-08

Fig. 6-3. Power Strapping—Self Test Stimulus Circuitry.

TABLE 6-1

SELF-TEST STIMULUS CONNECTION

| Connector | PM 101 Individual Test Leads | | | | | |
	Data	Address	Address	Qualifiers	Timing	Other
T2	DØ	AØ			Black	
T3	D1	A1			Brown	
T4	D2	A2			Red	
T5	D3	A3			Orange	
T6	D4	A4			Yellow	
T7	D5	A5			Green	
T8	D6	A6			Blue	
T9	D7	A7			Violet	
T10	D8	A8	A16	QØ		
T11	D9	A9	A17	Q1		
T12	D1Ø	A1Ø	A18	Q2		
T13	D11	A11	A19	Q3		
T14	D12	A12	A2Ø	Q4		
T15	D13	A13	A21	Q5		
T16	D14	A14	A22			
T17	D15	A15	A23			
T18				Q6		
T19				Q7		
T20				Q8		
T21				Q9		
Clock						Grey
TS						Red
GND					White	Black

@

Timing Option. The Self Test Stimulus Circuitry also provides stimulus for the Timing Option probe, P6451. This stimulus is the reference for the TIMING OPTION test (Test B) on the Diagnostic Monitor menu. Sub-test 1 is internal to the 7D02 and runs even without the Timing Option Probe connected.

Troubleshooting

While the Logic Analyzer—Personality Module system is quite complex, it has built in diagnostic routines which simplify troubleshooting. Power-up Diagnostics, which are a limited version of the full diagnostic program, run every time the instrument is turned on. If a failure is detected, the "Power-up Verification" test results are displayed. This display offers the operator the choice between beginning operation or displaying the Diagnostic Monitor menu. That menu in turn offers the operator the choices of running any or all of the Module Tests, or of exiting the Diagnostic Monitor, or displaying the Signature Exerciser menu within the Diagnostic Monitor.

Depressing and holding any keyboard button within approximately three seconds of pulling the POWER switch on will simulate a failure and allow the operator to access the Diagnostic Monitor.

NOTE

Some problems may only occur when the instrument is fully warmed up. Allow 20 minutes for this purpose.

Diagnostic Flow Charts. When the diagnostic routines detect a failure these flow charts will help the technician isolate a particular IC or group of IC's for signature analysis or conventional troubleshooting. Refer to Figs. 6-4 through 6-9.

Substitution—the easiest test. If other Logic Analyzers or Personality Modules are available, try substituting them and running the diagnostics again.

CAUTION

Exercise caution with power supply problems, since a seriously out of tolerance power supply could cause secondary damage in more than one unit.

"Check . . .". The word "check" as used in the Diagnostic Flow Chart means:

A VISUAL INSPECTION for damage, connection continuity, or shorts.

SIGNATURE ANALYSIS—See the signature analysis subsection below.

VOLTAGE CHECK of local power supply line(s).

WAVEFORM ANALYSIS of the signal quality. For example, rise and fall times, amplitude, ringing, noise or glitches, as applicable.

Intermittent Problems. A whole section of the flow chart deals with intermittent failures. If the problem is known to occur infrequently, skip ahead in the Flow Chart and begin LOOPING the test most likely to exercise the affected area.

Setup and Hold Performance Checks. The Diagnostic Flow Chart sometimes directs the reader to PM 101 or 7D02 Setup and Hold Performance Checks. These tests check the response speed of portions of the system and may be useful in finding some intermittent problems. Performing them requires additional equipment and considerable time, however. Refer to Section 5 of this manual.

NOTE: "GO TO" SYMBOLS WITH QUOTES INSIDE REFER TO OTHER DIAGNOSTIC FLOW CHARTS. E.G.,

GO TO INSTRUMENT "DIAG. FLOWCHART"

PM101 START - 1

7D02 KNOWN TO BE GOOD ?

NO → GO TO 7D02 "PER.MOD.-SYS."

YES

CONNECT THE SELF TEST STIMULUS AND 7D02

RUN THE 7D02 DIAGNOSTIC MONITOR-ALL (TEST 0)

DO ALL TESTS PASS?

YES → GO TO PM101 "C6-C9" FIG. 6-6.

NO

IS THIS THE 1ST TIME THROUGH?

YES → CHECK ALL SELF TEST STIMULUS CONNECTIONS AND GROUND

NO

DID ANY OTHER TESTS THAN 9-1,2,3,4,7,8, OR B-3 FAIL ?

YES → GO TO 7D02 "PER.MOD.-SYS."

NO

DID TEST B-3 FAIL ?

YES → CHECK ALL THE TIMING OPTION SELF TEST STIMULUS CONNECTORS.

WAS A PROBLEM DISCOVERED AND CORRECTED ?

YES

NO → GO TO PM101 "CLOCK CIRCUITS" FIG. 6-7.

NO

DID TEST 9-1 OR 9-2 FAIL ?

YES → CHECK A1U1031, A1U1021, /SEL P, LOOK, AND ASSOCIATED CIRCUITRY AND CONNECTORS.

NO

GO TO PM101 "START- 2" FIG. 6-5

2917-19

Fig. 6-4. PM 101 Start-1.
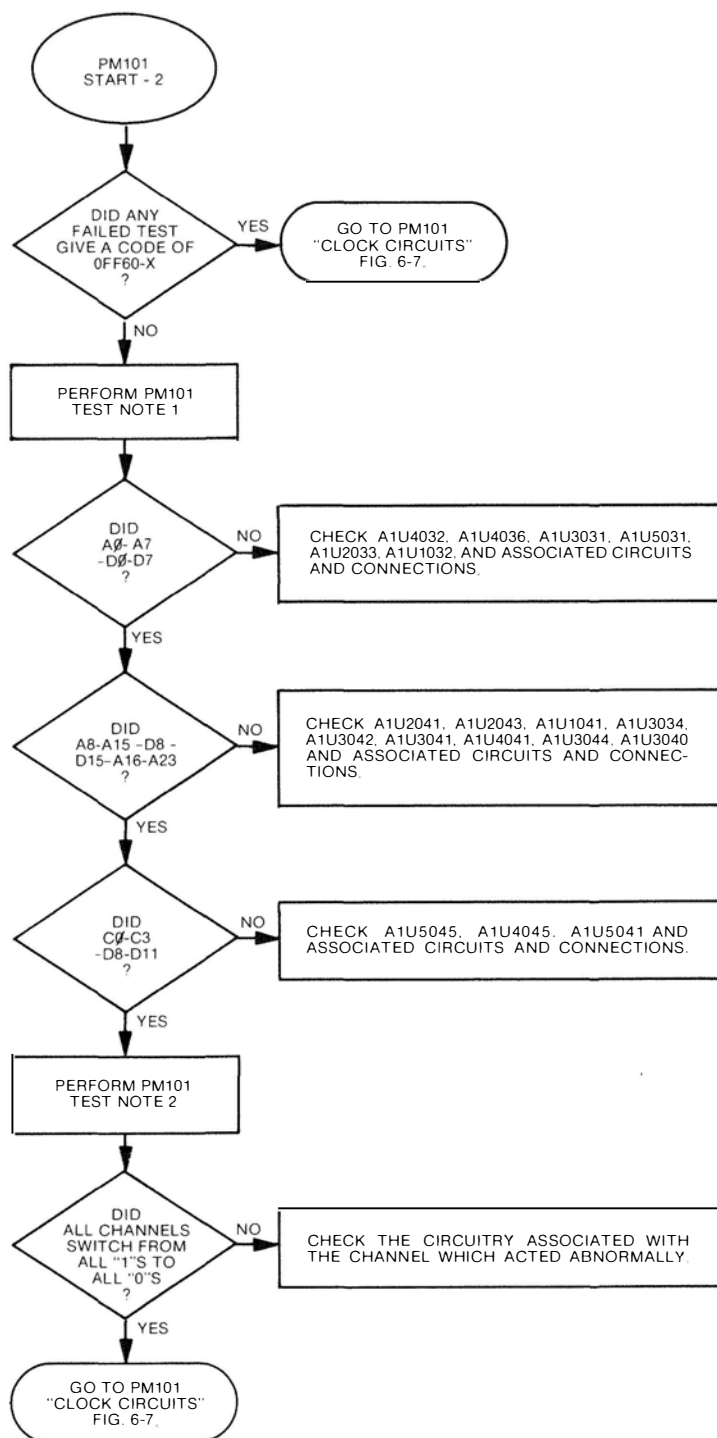
Fig. 6-5. PM 101 Start-2.
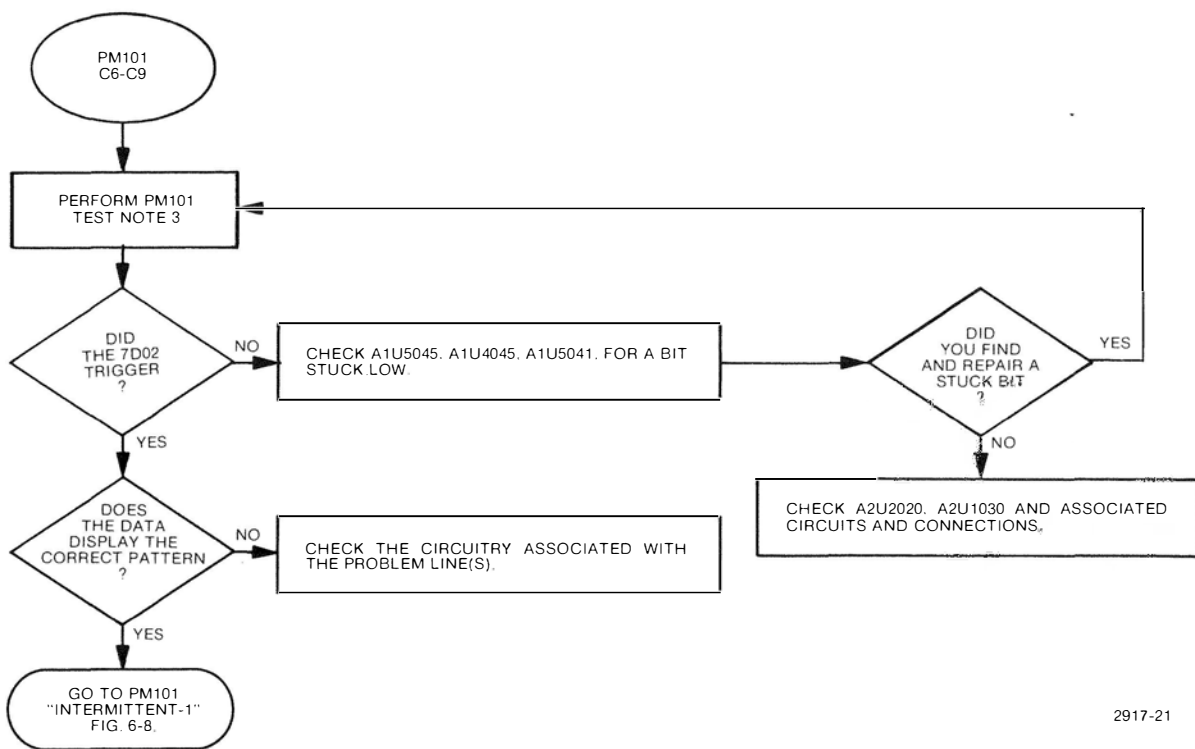
Fig. 6-6. PM 101 C6—C9.
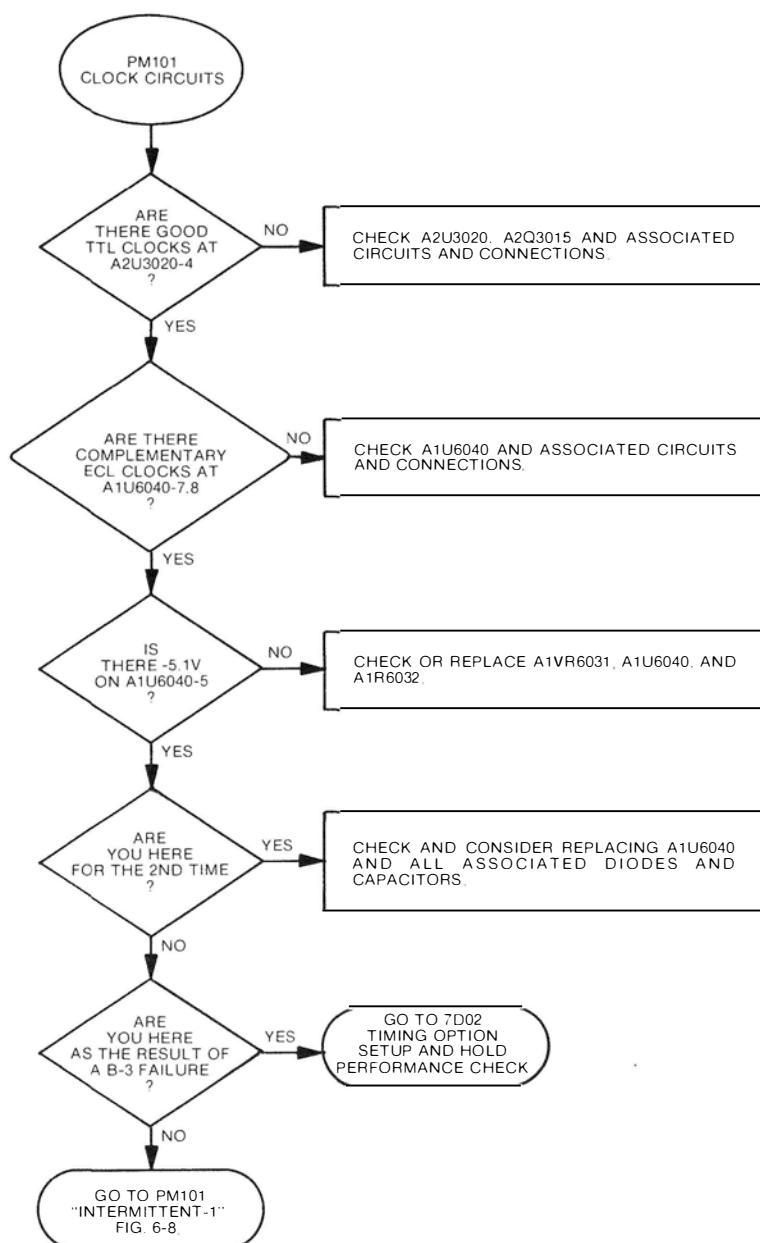
Fig. 6-7. PM 101 Clock Circuits.
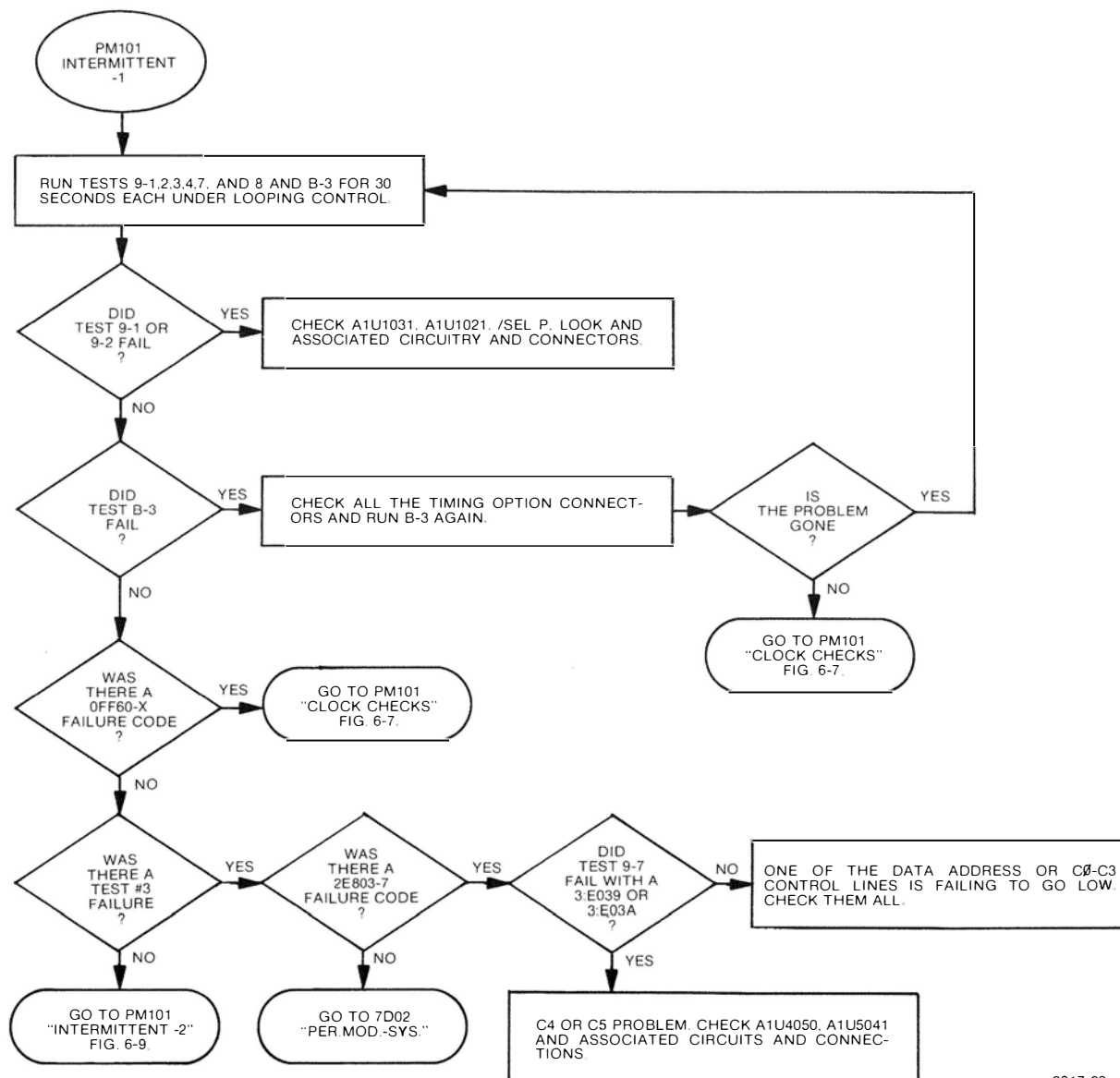
2917-22

Fig. 6-8. PM 101 Intermittent-1.
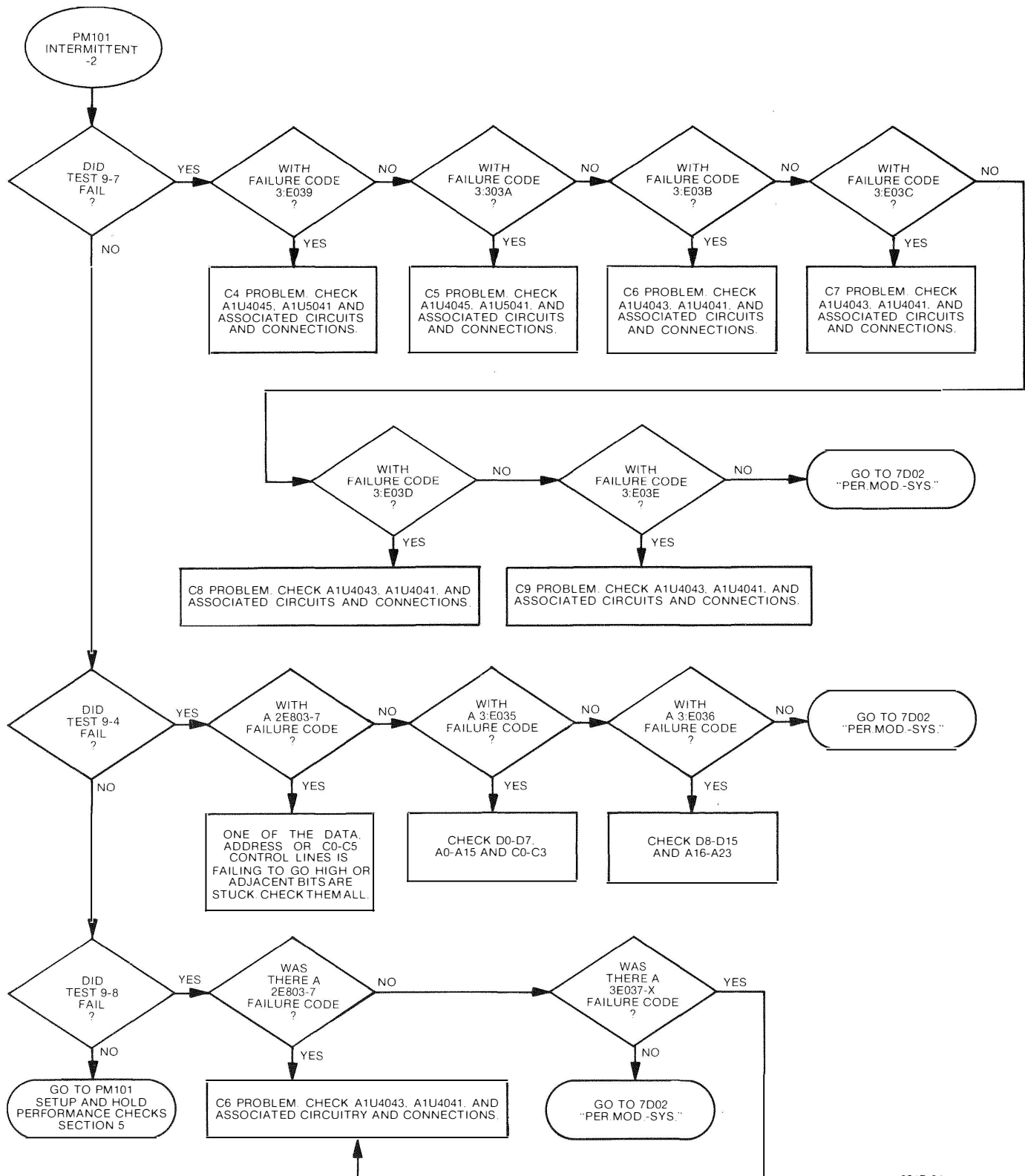
Fig. 6-9. PM 101 Intermittent-2.

2917-24

Test Notes

Test Note 1. Turn the 7D02 off and on to initialize default conditions. After the Powerup Diagnostics have run, press the TRIGGER key and the START/STOP button. Check that the two leftmost DATA and ADDRESS characters and the center pair of ADDRESS characters are all the same, and that the two rightmost characters in the DATA and ADDRESS columns are the same, e.g.:

LOC	ADDRESS	DATA	CONTROL
000T	3636FE	36FE	0110
001	3636FF	36FF	0110
002	373700	3700	0111
003	373701	3701	0111
004	373702	3702	0111

Test Note 2. Change the default program to all "0"s as follows: Press the IMMEDIATE, DISPLAY, and PROGRAM keys. Move the CURSOR to the Word Recognizer Data field and enter sixteen "0"s. Press the START/STOP button and press the DATA SCROLLING (up) key. The display should look like this:

LOC	ADDRESS	DATA	CONTROL
013	FFFFFE	FFFE	1111
014	FFFFFF	FFFF	1111
015T	000000	0000	1111
016	000001	0001	0000
017	000002	0002	0000

Test Note 3. Change the default program as follows: Press the IMMEDIATE, DISPLAY, and PROGRAM keys. Move the CURSOR to the Word Recognizer Data field and enter a hexadecimal "2" in the rightmost place. Also enter a hexadecimal "2" in the rightmost place of the Address field. Leave CØ through C5 all "0"s. Move the CURSOR down and enter a "1" in the Clock Qualification field to select USER CLOCK QUALification. Move the CURSOR down again and enter four ones in the leftmost places of the ANDED CLOCKS field. Press the START/STOP button to run this program. A trigger should occur and the data should look like this:

LOC	ADDRESS	DATA	CONTROL
013	FFFFFB	FFFB	1111
014	FFFFFE	FFFE	1111
015T	000002	0002	1111
016	000003	0003	0000
017	000006	0006	0000
018	000007	0007	0000
019	00000A	000A	0000
020	00000B	000B	0000
021	00000E	000E	0000
022	000012	0012	0000

Diagnostic Monitor—Test Modules

Module Test 9-1. This sub-test reads a byte at 3:E010 in the Personality Module ROM to read the ROM length. Using this, it locates the ROM trailer and reads the value at 3:YYFC (where YY is the value read from 3:E010). The value read at 3:YYFC is compared with the value at 3:YYFD, which should be its complement. If the two bytes are not complementary, an error message is printed as follows:

1   FAIL   3E7FD-X   ; 2K ROM

1   FAIL   3YYFD-X   ; INCORRECT   VALUE @ 3:E010

Where: X signifies the first non-complementary data bit when the two bytes are compared on a bit-by-bit basis (starting with the LSB).

If the ROM part number is correct the following message is printed:

1   PASS   0853-XX

Note that this is the only time that any data follows a true PASS indication. In other cases where a number follows a PASS signal, there was actually an intermittent failure.

Module Test 9-2. This sub-test calculates a 16-bit checksum on the Personality Module ROM. If the calculated value does not match the expected value, the calculated value is reported as an error as follows:

2   FAIL   F113

If the first part of sub-test 9-1 failed, it is likely that this test will also fail. However, if the first part of sub-test 9-1 failed and the second part also failed, this test still might pass since the checksum is location independent.

NOTE

The Self Test Stimulus Circuitry on the Personality Module must be connected for the remaining sub-tests in Module Test 9.

Module Test 9-3. Before this test is run, the four Word Recognizers are programmed according to data stored in the Personality Module ROM:

	D15—DØ	A23—A0	C5	C4	C3	C2	C1	CØ
WR1	0000	000000	0	0	0	0	0	0
WR2	55555	555555	0	1	0	1	0	1
WR3	AAAA	AAAAAA	1	0	1	0	1	0
WR4	FFFF	FFFFFF	1	1	1	1	1	1

@

If the Expansion Option is not present, Address lines A16—A23 and Data lines D8—D15 are set to "X" (don't care). The External Trigger is always set to "X" (don't care).

The State Machine in the 7D02 is programmed to execute a test sequence:

1 IF WR1, THEN TRIGGER MAIN AND TIMING

1 IF WR2 OR WR3 OR WR4, THEN DON'T TRIGGER

1 ELSE GOTO 1

The Acquisition Memory board in the 7D02 is set for Zero Delay. The Front End Qualifiers and the Clock Shifter/Divider are programmed to default values of all "X"s (don't cares) according to data stored in the Personality Module ROM. After all setups are complete, a Display command is sent and the Slow Clock Detector is checked. A slow clock indication results in the following error:

3 FAIL   0FF60-1   ;   SLOW OR NO CLOCK

This error can be caused by an erratic or missing PM 101 clock.

If the clock appears to be running, the Personality Module ROM is read to determine how long to wait for a trigger to occur. A Store command in the 7D02 is sent next. After waiting the specified length of time, the Activity Monitor on the Acquisition Memory board is examined to see if the Main Section has triggered and returned to the Display mode. (All of this is occurring in the 7D02.) If the Main Section is still in the Store mode, the following error is generated:

3 FAIL   2E803-7   ;   MAIN SECTION FAILED TO TRIGGER

Failure to trigger can be caused by a failure of the Personality Module to generate the WR1 value.

Module Test 9-4. This test involves all four Word Recognizers, both Counters, the State Machine, and the Acquisition Memory. The Word Recognizers remain programmed as in sub-test 3. The State Machine is programmed with the following test program:

The State Machine begins in state 1 and advances to the next state as each of the four Word Recognizers occur in order. While in state 1, the two Counters are reset. While in state 2, Counter 1 is incremented, and while in state 3, Counter 2 is incremented. While all of this is going on, the Acquisition Memory is acquiring data. When Word Recognizer 4 occurs, that single data sample is not stored and the Main Section and the Timing Option are both

triggered. At that point, the Acquisition Memory contains the last 16 words generated before Word Recognizer 4 and the 240 words generated immediately after Word Recognizer 4. If the Qualify RAM works correctly, the Word Recognizer 4 value was not stored. Counter 1 contains the number of clocks that occurred between Word Recognizer 1 and Word Recognizer 2, and Counter 2 contains the number of clocks that occurred between Word Recognizer 1 and Word Recongizer 3.

The Acquisition Memory board is set for a delay of 240 clocks and the Memory Address Counter is pre-set to 0FDH. The Front End Qualifiers and the Clock Shifter/Divider are programmed with default values according to data stored in the Personality Module ROM. After all steps are completed, a Display command is sent and the Slow Clock Detector is checked. A Slow Clock indication results in the following error message:

4 FAIL   0FF60-1   ;   SLOW OR NO CLOCK

If the clock appears to be running, the Personality Module ROM is read to determine how long to wait for a trigger. Then, a Store command is sent. After waiting 2 ms, the Activity Monitor on the Acquisition Memory board is examined to see if the Main Section has triggered and returned to the Display mode. If still in the Store mode, the following error message is generated:

4 FAIL   2E803-7   ;   MAIN SECTION FAILED TO TRIGGER

Failure to trigger can be caused by a failure of the Personality Module to generate any one of the Four Word Recognizer values.

Another part of sub-test 4 checksums the Acquisition Memory. All bytes between 2:E000 and 2:E3FF are summed and the result stored. The Expansion Option Acquisition Memory is then checksummed by summing all bytes between 2:E400 and 2:E7FF. The results of these checksums are compared with the expected values stored in the Personality Module ROM, and one of the following error messages is displayed if they do not compare correctly:

4 FAIL   3E035-X   ;   MAIN ACQ. MEM. FAILS CHECKSUM

4 FAIL   3E036-X   ;   EXP. OPT. ACQ. MEM. FAILS CHECKSUM

These messages may indicate that the PM 101 is not always generating the correct data pattern, i.e., that one or more channels are intermittent.

Module Test 9-5. Failure of this test indicates that the problem is in the 7D02; consult that Service manual.

Module Test 9-6. Failure of this sub-test indicates that the problem is in the 7D02; consult that Service manual.

Module Test 9-7. This test checks the Control (Qualifier) lines C4 to C9 on the 7D02 Front End board. The State Machine is programmed with the test sequence:

```
1    IF WR1, THEN TRIGGER MAIN
1    ELSE GOTO 1
```

Word Recognizer 1 was programmed to all "0"s in sub-test 3. This sub-test checks the operation of control lines C4 through C9 by qualifying out the value to which Word Recognizer 1 has been programmed. This is accomplished by placing, one at a time, the requirement for a "1" on C4, C5, and C9, and the requirement for a "0" on C6, C7, and C8. In each case these lines are used to qualify out the value in Word Recognizer 1. If a particular control line works correctly, the State Clock that occurs with WR1 is inhibited because the State Clocks never occur when the Word Recognizer value is present, so the State Machine will not see the Word Recognizer output. A PASS is indicated by a failure of the Main Section to trigger. A byte in the Personality Module ROM specifies that the Processor wait 2 ms for the trigger to occur.

Six bytes in the Personality Module ROM specify what value to send to the Front End board for each of the control lines. The following sequence is repeated six times, once for each control line or until a failure occurs:

Read value from Personality Module ROM
Write value to Front End Latch
Send Store command
Wait a specified length of time
Check Activity Monitor on Acquisition Memory board
If in Display mode, print FAIL and stop

The test results are interpreted as follows:

```
7    FAIL   3E039; C4 DID NOT INHIBIT TRIGGER

7    FAIL   3E03A; C5 DID NOT INHIBIT TRIGGER

7    FAIL   3E03B; C6 DID NOT INHIBIT TRIGGER

7    FAIL   3E03C; C7 DID NOT INHIBIT TRIGGER

7    FAIL   3E03D; C8 DID NOT INHIBIT TRIGGER

7    FAIL   3E03E; C9 DID NOT INHIBIT TRIGGER
```

Module Test 9-8. This test exercises the Programmable Shifter/Divider on the 7D02 Front End Board in the delay-by-one and divide-by-two modes. A byte in the General Purpose Personality Module tells the 7D02 that this test can be run using this Module.

For this test the State Machine is programmed with the following test sequence:

```
1 IF WR1
1 THEN
1 GOTO 4

4 IF WR1
4 THEN
4 TRIG MAIN
```

The PM 101 ROM sets the 7D02 Front End to its default status, except that it is set to divide-by-two and the low state of C6 is used to generate ESYNC. A Display command is sent and the Slow Clock Detector is checked. If no clock is present, the following error message is displayed:

```
8    FAIL   0FF60-1   ;   SLOW OR NO CLOCK
```

This error can be caused by an erratic PM 101 Clock Signal or a C6 problem.

If the clock is determined to be running, a Store command is sent and the Processor waits 2 ms. At the end of that delay, the Acquisition Memory Activity Monitor is checked and, if the Main Section has not returned to the Display mode (triggered), the following error message is displayed:

```
8    FAIL   2E803-7   ;   MAIN SECTION FAILED TO
TRIGGER
```

This failure could be caused by a failure of the Personality Module to generate the all "0"s pattern of Word Recognizer 1 or by a C6 problem.

If the Main Section did trigger, the Acquisition Memory should now be full. All of the bytes between 2:E000 and 2:E3FF are checksummed and the result is compared to the expected value stored in the Personality Module ROM. If the values do not match, the following error message is displayed:

```
8    FAIL   3E037-X   ;   DIVIDE BY 2 CHECKSUM
FAILED
```

This error message may indicate an intermittent PM 101 channel, since the pattern being generated is not perfect.

If the divide-by-two test passes, the entire test is repeated with the Front End set to delay-by-one instead of divide-by-two. (C6 generates ESYNC as before.) If the test fails under these conditions, the following error is displayed:

```
8    FAIL   3E038-X   ;   SHIFT BY 1 CHECKSUM
FAILED
```

@

This test also may indicate that a PM 101 channel is intermittent.

Module Test B-3. In this sub-test, the Timing Option Word Recognizer is set to trigger on the occurrence of a hexadecimal 55 (specified by the Personality Module ROM) and the State Machine is programmed with the following test program:

1 IF TIM OPT WR=55 (WR1=TIM.OPT.WR)
  AND WR2,3,4=DON'T CARE
1 THEN
1 GOTO 4
  END

4 IF TIM OPT WR=55 (TIM.OPT.WR.=WR1)
  AND WR2,3,4=DON'T CARE
4 THEN
4 TRIG MAIN AND TIMING
  END

Also, the Timing Option Memory Address Counter is set to "0". All Word Recognizers except the Timing Option Word Recongizer are set to all "X" (don't care).

The Slow Clock Indicator is checked for the presence of a clock. If none is detected, the following error is reported:

3 FAIL 0FF60-1 ; SLOW OR NO CLOCK DETECTED

If the clock appears to be running, a byte is read from the Personality Module ROM which specifies that the Processor wait 2 ms for a trigger. Then a Store command is sent. After waiting the specified 2 ms, the Acquisition Memory Activity Monitor is examined to see if the Main Section has triggered. If it has not, the following error message is displayed:

3 FAIL 2E803-7 ; MAIN SECTION FAILED TO TRIGGER

This error may be caused by a failure of the Personality Module to generate a hexadecimal 55 on the Timing Option pins of the Self Test Stimulus Circuitry.

If the trigger did occur, the Timing Option Memory Address Counter is examined to determine the last data location, and the trigger location is calculated. This value is then compared to a value stored in the Personality Module ROM. If the two are not complementary, the following error message is displayed:

3 FAIL 3E03F-X ; TRIGGER VALUE IN-CORRECT

This error may indicate an improper timing relationship between the Clock signal from the PM 101 and the data from the Self Test Stimulus Circuitry of the PM 101.

If the trigger test passes, the Timing Option Acquisition Memory at address 2:F000—2:F0FF is checksummed and the result compared with the expected value stored in the Personality Module ROM. If the values are not the same, the following error message is displayed:

3 FAIL 3E040-X ; CHECKSUM ERROR 2:F000—2:F0FF

Where:"X" indicates the bit that didn't match.

This error may be caused by a failure of the Self Test Stimulus Circuitry to consistently generate the correct pattern or an intermittent Timing Option Probe.

Signature Tables—Boards A1 and A2

All signatures in the following tables were taken with a SONY/TEKTRONIX 308 Data Analyzer.

Configuration: Invalid signatures occur if the configuration is not as specified. The PM 101 Self Test Stimulus Circuitry provides stimulus for Test 7, the "PER. MOD. - SYSTEM" test, of the DIAGNOSTIC MONITOR - SIGNATURE EXERCISER routine. The probe must be connected to the 7D02. The Self Test Stimulus is connected normally except the Control lines (Q6, Q7, and Q8) on T18, T19, and T20·must be moved to the T2, T3, and T4 connections used by the Timing Option. Refer to Table 6-1.

Software: 160-0361-00 Diagnostic ROM

Analyzer: SONY/TEK 308

Table 6-2

SIGNATURES

	Location	S/W	SIG
Clock	CLK	↑	N/A
Start	T17	↓	0000
Stop	T17	↓	0000
Power	**SIG**		
+5	755U		
Gnd	0000		

TABLE 6-2 (cont)

SIGNATURES

A1U1021	SIG
1	A3C1
2	7211
3	AA08
4	C4C3
5	0772
6	7050
7	C113
8	H335
18	755U
19	HH86
20	0000
21	755U
22	577A
23	7707

A1U1031	SIG
3	AA08
5	C4C3
7	A3C1
9	7211
12	7050
14	0772
16	C113
18	H335

A1U2031	SIG
2	H335
3	AA08
4	C113
5	C4C3
6	0772
7	A3C1
8	7050
9	7211
11	7211
12	7050
13	A3C1
14	0772
15	C4C3
16	C113
17	AA08
18	H335
19	0000

A1U2041	SIG
2	89F1
3	1180
4	HH86
5	0000
6	7707
7	7050
8	577A
9	AC99
11	AC99
12	577A
13	PCF3
14	7707
15	0000
16	HH86
17	1180
18	89F1

A1U3021	SIG
1	A3C1
2	7211
3	AA08
4	C4C3
5	0772
6	7050
7	C113
8	H335
18	755U
19	HH86
20	0000
21	755U
22	577A
23	7707

A1U3031	SIG
2	AA08
3	89F1
4	7211
5	HH86
6	A3C1
7	7707
8	C4C3
9	577A
11	577A
12	C4C3
13	7707
14	A3C1
15	HH86
16	7211
17	89F1
18	AA08
19	0000

A1U3041	SIG
2	0000
3	AC99
4	1180
5	PCF3
6	PCF3
7	1180
8	AC99
9	0000
11	0000
12	AC99
13	1180
14	PCF3
15	PCF3
16	1180
17	AC99
18	0000
19	0000

A1U4041	SIG
2	H335
3	89F1
4	C113
5	HH86
6	7050
7	7707
8	C113
9	577A
11	577A
12	C113
13	7707
14	7050
15	HH86
16	C113
17	89F1
18	H335

A1U5031	SIG
3	0772
5	H335
7	7050
9	C113
11	C113
13	7050
15	H335
17	0772
19	0000

A1U5041	SIG
3	HH86
5	89F1
6	7707
7	AC99
8	577A
9	PCF3
11	PCF3
12	577A
13	AC99
14	7707
15	89F1
17	HH86

A2U1020	SIG
7	HHH4
10	UFAA
11	0000
12	1180
13	PCF3
14	ACC9

A2U1030	SIG
2	7707
3	7707
4	577A
5	577A
6	HH86
7	HH86
8	89FC
9	89FC
11	AC99
12	AC99
13	PCF3
14	PCF3
15	1180
16	1180
17	0000
18	0000

A2U2020	SIG
7	HHH4
10	9908
11	89F1
12	0000
13	57AA
14	7707
15	UFAA

@

TABLE 6-2 (cont)
SIGNATURES

A2U3020	SIG
5	HHH4
6	A88C
8	PF57
9	9908
10	89U5
11	UFAA

A2U4020	SIG
	HHH4
10	HHH4
11	A3C1
12	7211
13	AA08
14	C4C3
15	9908

A2U4030	SIG
2	H335
3	H335
4	C113
5	C113
6	7050
7	7050
8	0772
9	0772
11	C4C3
12	C4C3
13	AA08
14	AA08
15	7211
16	7211
17	A3C1
18	A3C1

A2U5020	SIG
7	755U
10	755U
11	0772
12	7050
13	C113
14	H335
15	HHH4

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.   component number

A23R1234   A23   R1234

Assembly number   Circuit number

Read: Resistor 1234 of Assembly 23

Example b.   component number

A23A2R1234   A23   A2   R1234

Assembly number   Subassembly number   Circuit number

Read: Resistor 1234 of Subassembly 2 of Assembly 23
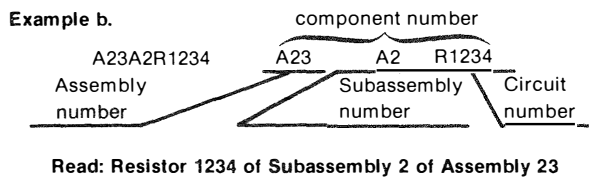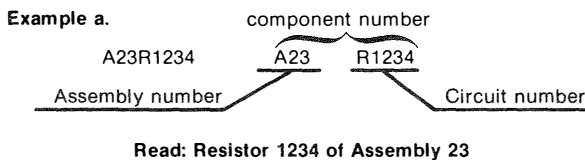
Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD, PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
52648	PLESSEY SEMICONDUCTORS	1641 KAISER	IRVINE, CA 92714
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
55210	GETTIG ENG. AND MFG. COMPANY	PO BOX 85, OFF ROUTE 45	SPRING MILLS, PA 16875
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-6154-00			CKT BOARD ASSY:GENERAL PURPOSE 1	80009	670-6154-00
A2	670-6155-00			CKT BOARD ASSY:GENERAL PURPOSE 2	80009	670-6155-00
A3	670-6149-00			CKT BOARD ASSY:PROBE CONNECTOR	80009	670-6149-00
	----- -----			(NO ELECTRICAL PARTS)		
A1	----- -----			CKT BOARD ASSY:GENERAL PURPOSE 1		
A1C1001	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C1040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2045	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C3031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C3032	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C3045	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C4031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C4034	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C4044	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C5032	283-0346-00			CAP.,FXD,CER DI:0.47UF,+80-20%,100V	72982	8131-M100F474Z
A1C5042	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C6030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C6033	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C6035	283-0136-00			CAP.,FXD,CER DI:10PF,5%,50V	51642	A100050-NP0-100J
A1C6038	281-0615-00			CAP.,FXD,CER DI:3.9PF,+/-0.5PF,200V	72982	374001C0J0399D
A1C6039	283-0330-00			CAP.,FXD,CER DI:100PF,5%,50V	72982	8111N068C0G0101J
A1C6045	283-0186-00			CAP.,FXD,CER DI:27PF,5%,50V	72982	8121B070A270J
A1C6048	281-0663-00			CAP.,FXD,CER DI:10.4PF,1%,500V	72982	374005C0G01049F
A1CR6041	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR6044	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR6050	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A1CR6052	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A1R1021	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R2010	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R2015	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R2021	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R3010	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R3011	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R3012	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R3014	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R4012	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R4013	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R5010	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R5011	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R6032	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A1R6034	321-0282-00			RES.,FXD,FILM:8.45K OHM,1%,0.125W	91637	MFF1816G84500F
A1R6036	321-0208-00			RES.,FXD,FILM:1.43K OHM,1%,0.125W	91637	MFF1816G14300F
A1R6037	321-0268-00			RES.,FXD,FILM:6.04K OHM,1%,0.125W	91637	MFF1816G60400F
A1R6038	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A1R6043	321-0631-00			RES.,FXD,FILM:12.5K OHM,1%,0.125W	91637	MFF1816G12501F
A1R6045	321-0344-00			RES.,FXD,FILM:37.4K OHM,1%,0.125W	91637	MFF1816G37401F
A1R6049	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A1R6050	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1TP6030	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A1U1021	160-0853-00			MICROCIRCUIT,DI:2048 X 8 EPROM	80009	160-0853-00
A1U1031	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3	80009	156-0956-04
A1U1032	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U1041	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Dscont	Name & Description	Mfr Code	Mfr Part Number
A1U2031	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3	80009	156-0956-04
A1U2033	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U2041	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3	80009	156-0956-04
A1U2043	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U3031	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3	80009	156-0956-04
A1U3034	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U3040	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U3041	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3	80009	156-0956-04
A1U3042	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U3044	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U4032	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U4036	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U4041	156-0956-04			MICROCIRLUIT,DI:OCTAL BFR W/3	80009	156-0956-04
A1U4043	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U4045	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U5031	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3	80009	156-0956-04
A1U5041	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3	80009	156-0956-04
A1U5045	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U6040	156-1344-00			MICROCIRCUIT,LI:COMPARATOR ECL	52648	SP9685CM
A1VR6031	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755
A2	----- -----			CKT BOARD ASSY:GENERAL PURPOSE 2		
A2C1020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C1030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C3020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C4015	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	72982	8121N130C0G0511G
A2C4020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C4030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C5015	283-0193-00			CAP.,FXD,CER DI:510PF,2%,100V	72982	8121N130C0G0511G
A2C5020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C6015	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A2L4015	108-0683-00			COIL,RF:900MH	80009	108-0683-00
A2Q3015	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A2R2015	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R3015	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A2R3020	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A2R5015	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A2U1020	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	80009	156-0844-02
A2U1030	156-0916-02			MICROCIRCUIT,DI:8-2 INP 3-STATE BFR,BURN	27014	DM81LS97
A2U2020	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	80009	156-0844-02
A2U3020	156-0645-02			MICROCIRCUIT,DI:SCHMITT-TRIG POS-NAND	01295	SN74LS14
A2U4020	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	80009	156-0844-02
A2U4030	156-0916-02			MICROCIRCUIT,DI:8-2 INP 3-STATE BFR,BURN	27014	DM81LS97
A2U5020	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	80009	156-0844-02

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).

Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.

@
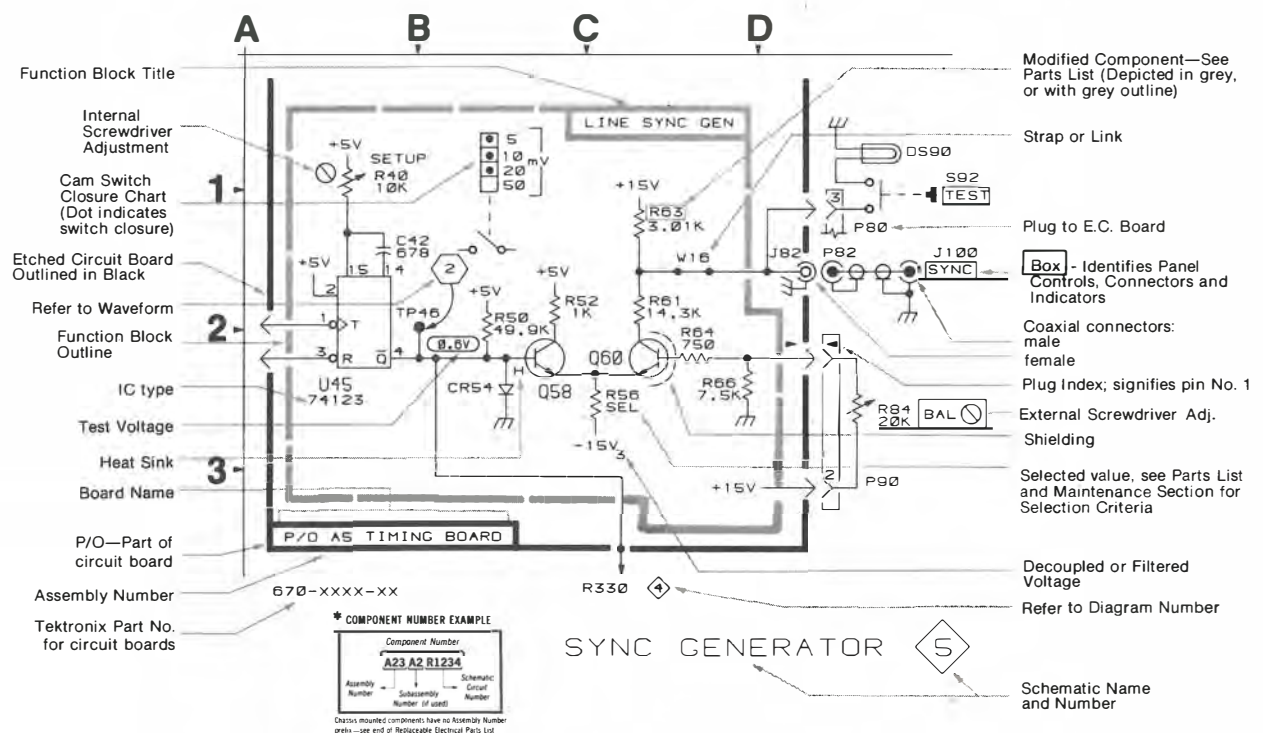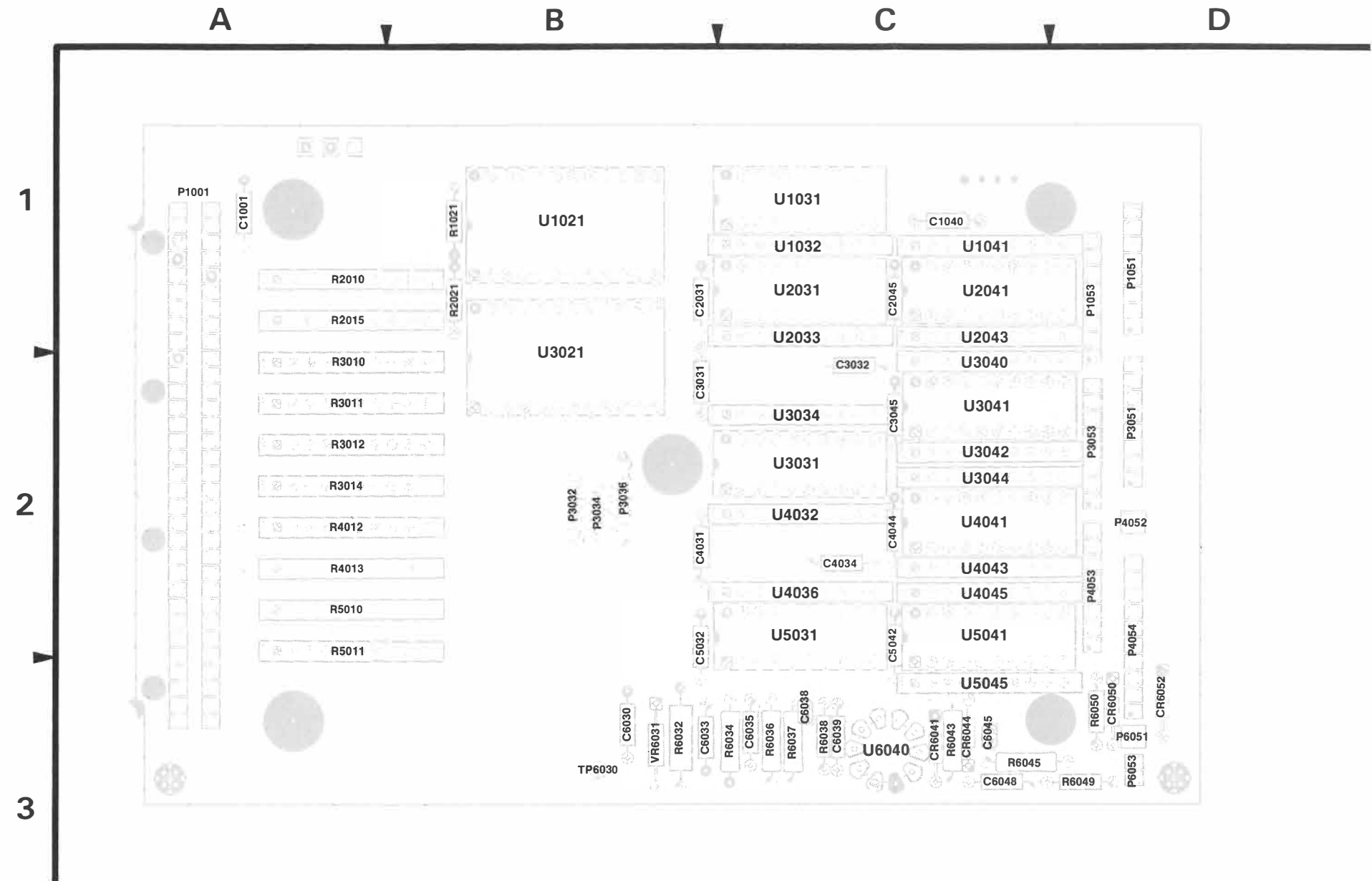
Figure 8-1A. A1 Upper Board Component Locations.

Table 8-1

IC Pin Information

Device Type	VCC	GND
2716	24	12
7414	14	7
74LS161	16	8
74LS244	20	10
81LS97	20	10
H1023	1	2

Table 8-2

ASSEMBLY A1					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P1001	A3	A1	U1041	C5	C1
P1001	F1	A1	U2031	B4	C1
P1051	A4	D1	U2033	B4	C1
P1053	A4	D1	U2041	D4	C1
P3051	A3	D2	U2043	C4	C1
P3053	A2	D2	U3031	B2	C2
P4053	A1	D2	U3034	B3	C2
P4054	A5	D2	U3040	E3	C2
			U3041	D1	C2
R2010	F5	A1	U3041	F3	C2
R2015	F5	A1	U3042	C1	C2
R3010	F4	A2	U3044	C2	C2
R3011	F4	A2	U4032	B2	C2
R3012	F4	A2	U4036	B1	C2
R3014	F3	A2	U4041	D2	C2
R4012	F2	A2	U4041	F5	C2
R4013	F2	A2	U4043	E5	C2
R5010	F1	A2	U4045	E4	C2
R5011	F1	A2	U5031	B1	C2
			U5041	F4	C2
U1032	B5	C1	U5045	E4	C3

Partial A1 also shown on diagram 1B.
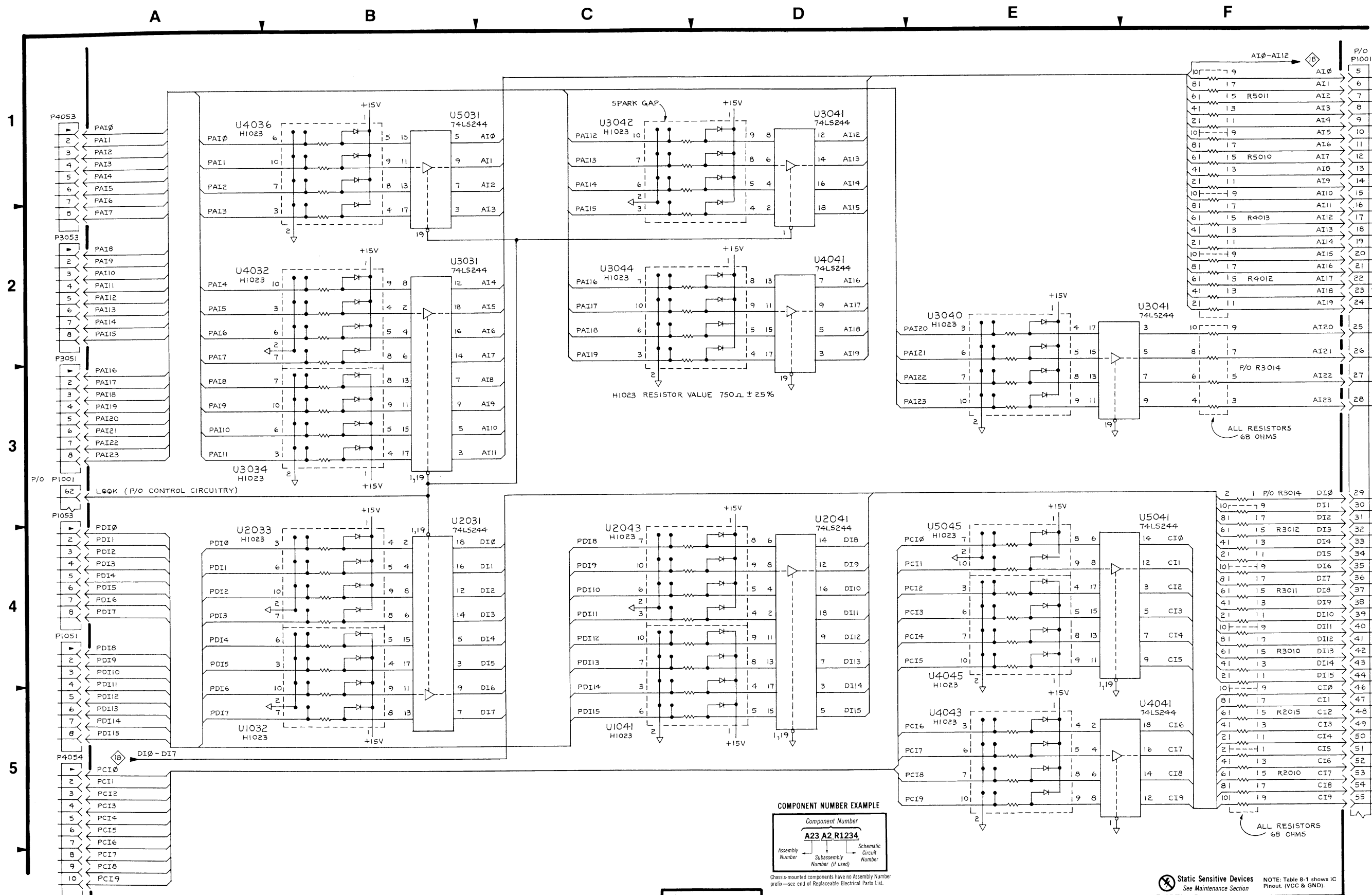
PM101 GENERAL PURPOSE PERSONALITY MODULE

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DATA TRANSFER CIRCUITRY ⟨1A⟩

A1 DATA TRANSFER CIRCUITRY
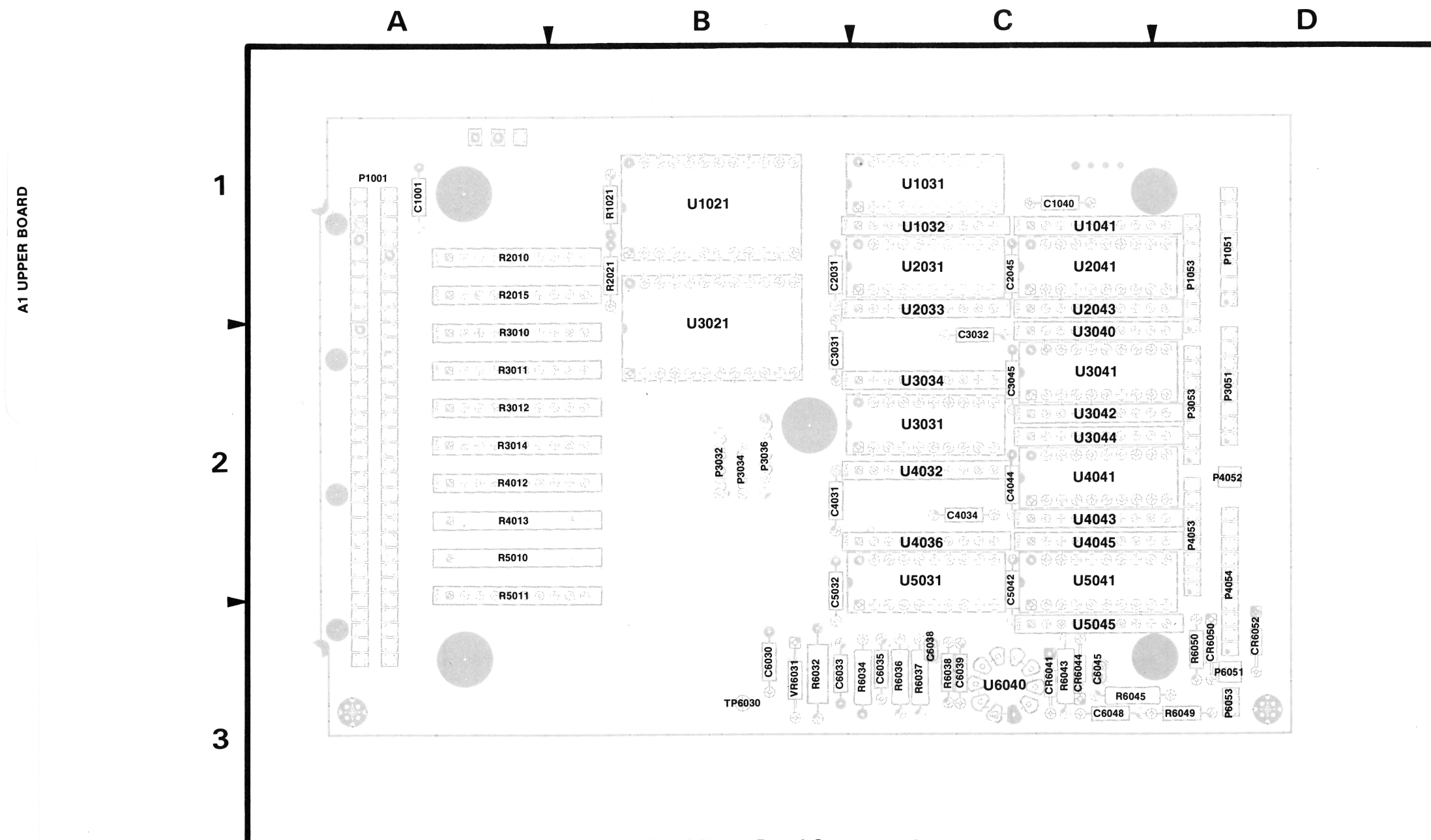
A1 UPPER BOARD

Figure 8-1B. A1 Upper Board Component Locations.

Table 8-3

ASSEMBLY A1					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1001	A3	A1	P3032	B2	B2
C1040	B3	C1	P3034	B2	B2
C2031	A3	B1	P3036	B2	B2
C2045	A3	C1	P4052	A4	D2
C3031	B3	B2	P6051	A4	D3
C3032	B3	C2	P6053	A3	D3
C3045	A3	C2	P6053	F1	D3
C4031	B3	B2			
C4034	B3	C2	R1021	C2	B1
C4044	A3	C2	R2021	D2	B1
C5032	B3	B2	R6032	C4	B3
C5042	A3	C2	R6034	C4	C3
C6030	A3	B3	R6036	C4	C3
C6033	A3	B3	R6037	C4	C3
C6035	C4	C3	R6038	C4	C3
C6038	C4	C3	R6043	C4	C3
C6039	C4	C3	R6045	B3	C3
C6045	B4	C3	R6049	B3	D3
C6048	B4	C3	R6050	E1	D3
CR6041	B3	C3	TP6030	A3	B3
CR6044	B4	C3			
CR6050	D1	D3	U1021	C2	B1
CR6052	D1	D3	U1031	F2	C1
			U3021	E2	B1
J1010	A4	A1	U5031A	D1	C2
			U6040	C3	C3
P1001	A1	A1			
P1001	C3	A1	VR6031	C4	B3

Partial A1 also shown on diagram 1A.

A   B   C   D   E   F

CONTROL CIRCUITRY

1   P/O P1001   61   /HALT SUT   U5031A
                                                                 74LS244
                                                                 2   18   +5V
                                                                         CR6052   R6050
                                                                                  100   /STOP SUT   P/O P6053   2
                                                                         CR6050

    63   /SEL P

                                        G.P. 8K G.P. CUST CUST 8K
                                        5   4   3   2   1   P3032

                                   8K 2 4K 3 2K   P3034   GP ROM   CUSTOM ROM
                                   1   U1021   U3021
2   6831B   2716,(2732)
                AI11 3   R1021 +5V   R2021 +5V   U1031
                AI12 1   4K 5 2K 6   P3036   4.7k   24   4.7k   24   74LS244
                          2   8K   20   OE   20   OE,(CE)   DIØ 2   18   DIØ
          IA   AIØ-AI12   18   CE   21   Vpp,(A12)   DI1 4   16   DI1
                                                                         21   Vpp   18   CE,(A11)   DI2 8   12   DI2
                                                                                                                                        DI3 6   13   DI3
                                                            AIØ 8 AØ 0Ø 9   DIØ   AI1 8 AØ 0Ø 9   DIØ   DI4 15 5   DI4
                                                            AI1 7 A1 01 10 DI1   AI2 7 A1 01 10 DI1   DI5 17 3   DI5
                                                            AI2 6 A2 02 11 DI2   AI3 6 A2 02 11 DI2   DI6 11 9   DI6
                                                            AI3 5 A3 03 13 DI3   AI4 5 A3 03 13 DI3   DI7 13 7   DI7
                                                            AI4 4 A4 04 14 DI4   AI5 4 A4 04 14 DI4
3   58   +15V   AI5 3 A5 05 15 DI5   AI6 3 A5 05 15 DI5
    45   +5V   +5V   +15V   AI6 2 A6 06 16 DI6   AI7 2 A6 06 16 DI6   DIØ-DI7   IA
    56   C5032   0.1   C1040   AI7 1 A7 07 17 DI7   AI8 1 A7 07 17 DI7
    57   GND   C1001 .47µF   C3031   AI8 23 A8   AI9 23 A8
    4   C2031 C4044   C3032   AI9 22 A9   AI10 22 A9
    60   C2045 C5042   C4031   AI10 19 A10   AI11 19 A10
    64   TP6030 C6030 C3045 C6033   C4034
    59   -15V   .01   ROM CIRCUITRY
                           -15V

    P/O P6053   +5V
4   CLK IN   R6049   R6045   CR6041   +5V U6040
                  470   37.4k   5P9685
                                                                       2 7   CLK   P/O P1001
                         C6048   CR6044   C6045   R6043   4,9,10   /CLK   3
    J1010   10.4pF   27pF   12.5k   3 8
    2   +5V   +5V   5   R6032
    3   GND   C6039 R6038   270 -15V
    3   -15V -15V   100pF 8.2k
                                                           VR6031
                                                    R6034   5.1V
    P6051   9.09k
    GND   R6037
                                              R6036   10pF 6.04k
    P4052   1.43k C6035
    GND

    CLOCK TRANSMISSION CIRCUITRY

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly   Subassembly   Schematic
Number   Number (if used)   Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

NOTE: Table 8-1 shows IC Pinout. (VCC & GND).

PM101 GENERAL PURPOSE PERSONALITY MODULE

P/O A01 PM101 BD.1

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ROM, CLOCK, AND CONTROL CIRCUITRY   1B

A1 ROM CLOCK AND CONTROL CIRCUITRY   1B

A2 LOWER BOARD

A   B   C

1

2
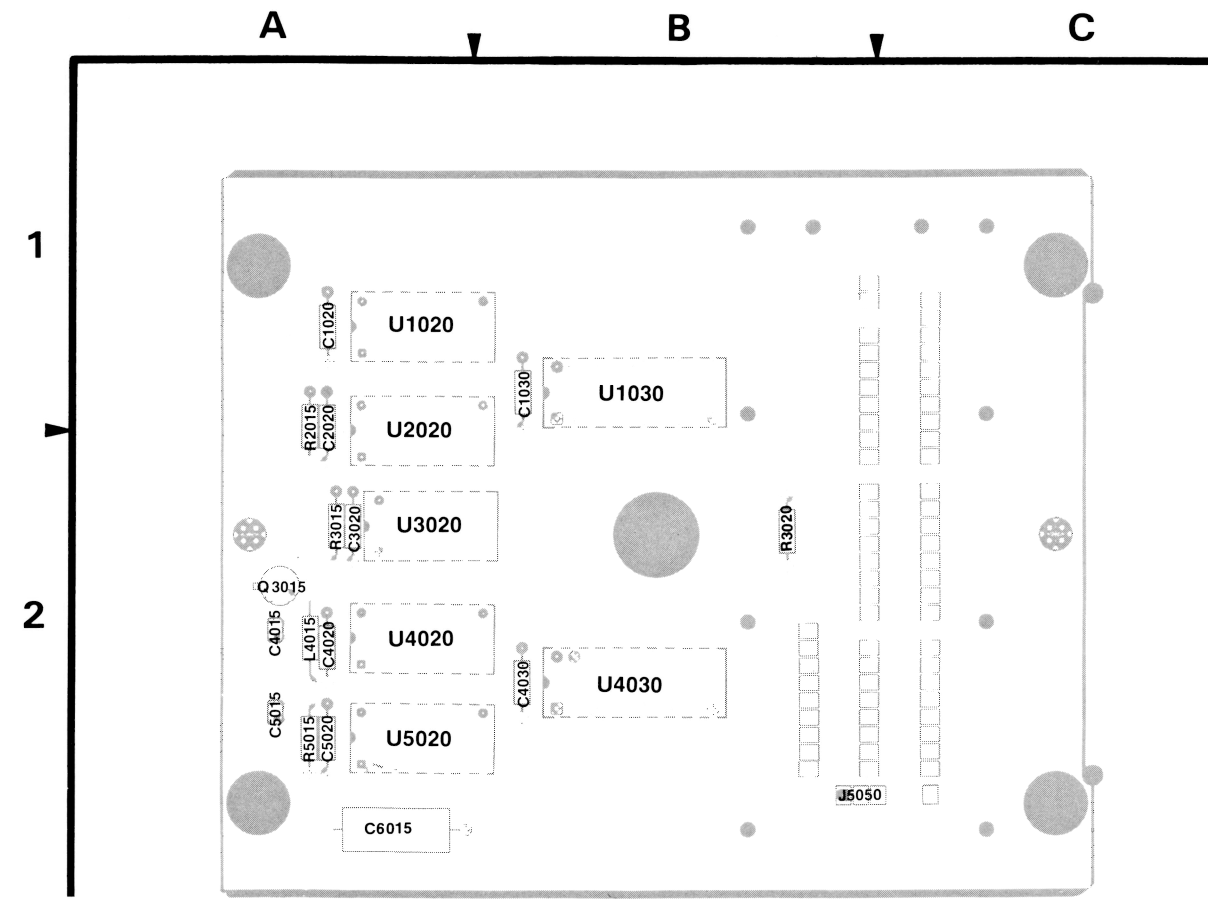
Figure 8-2. A2 Lower Board Component Locations.

U1020

U1030

U2020

U3020

U4020

U4030

U5020

C6015

J5050

C1020

C1030

R2015
C2020

R3015
C3020

R3020

Q 3015

C4015
L4015
C4020

C4030

C5015
R5015
C5020

Table 8-4

ASSEMBLY A2		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1020	B3	A1
C1030	B3	A1
C2020	B3	A1
C3020	B3	A2
C4015	A2	A2
C4020	B3	A2
C4030	B3	A2
C5015	A2	A2
C5020	B3	A2
C6015	A3	A2
J1012	A3	A3
J5050	B2	B2
L4015	A2	A2
Q3015	B2	A2
R2015	B2	A1
R3015	B1	A2
R3020	B1	B2
R5015	B2	A2
U1020	D1	A1
U1030	F2	B1
U2020	D1	A1
U3020	D2	A2
U3020A	B1	A2
U3020B	B1	A2
U4020	C1	A2
U4030	E1	B2
U5020	C1	A2

CLK T1

U5020
16 74LS161A

U4020
16 74LS161A

U2020
16 74LS161A

U1020
6 74LS161A

U4030
20 81LS97

U1030
20 81LS97

U3020A
7414

U3020B
7414

R3015
3.3K

R3020
ZERO
OHM

R2015
4.7K

Q3015

C4015
510PF

L4015
900nH

C5015
510PF

R5015
12K

-15V

+5V

T HALT

U3020
7414

J5050

OFF   ON

+5V

+5V

0.1

C1020
C1030
C2020
C3020
C4020
C4030
C5020

J1012

2   +5V

3   GND

-15V

C6015
47µF

COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly
Number

Subassembly
Number (if used)

Schematic
Circuit
Number

Chassis-mounted components have no Assembly Number
prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

NOTE: Table 8-1 shows IC
Pinout. (VCC & GND).

A02 PM101 BD. II

PM101 GENERAL PURPOSE PERSONALITY MODULE

2917-82

SELF TEST STIMULUS CIRCUITRY ◇2

2

A   B   C

1

P7020

2

J1010

Figure 8-3. A3 Connector Board Component Locations.
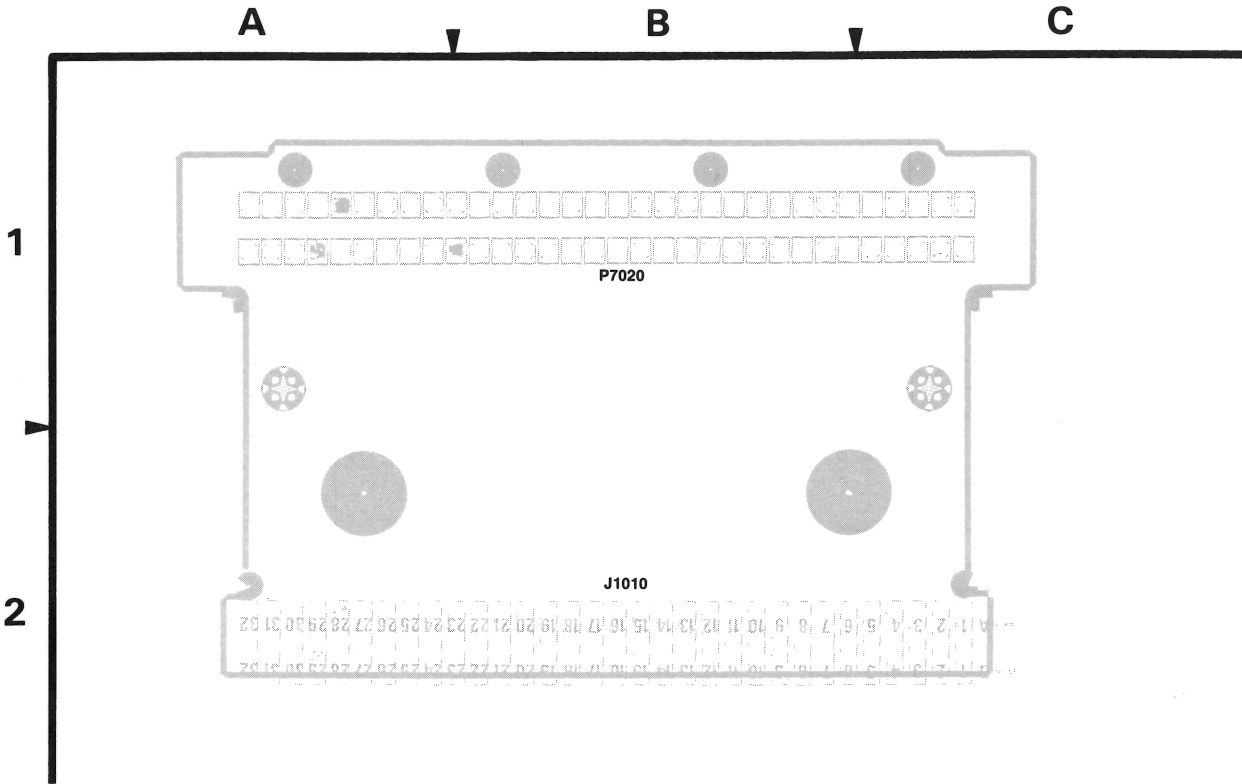
REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000   Part first added at this serial number

00X   Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5   *Name & Description*

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

#	INCH	ELCTRN	ELECTRON	IN	INCH	SE	SINGLE END
#	NUMBER SIZE	ELEC	ELECTRICAL	INCAND	INCANDESCENT	SECT	SECTION
ACTR	ACTUATOR	ELCTLT	ELECTROLYTIC	INSUL	INSULATOR	SEMICOND	SEMICONDUCTOR
ADPTR	ADAPTER	ELEM	ELEMENT	INTL	INTERNAL	SHLD	SHIELD
ALIGN	ALIGNMENT	EPL	ELECTRICAL PARTS LIST	LPHLDR	LAMPHOLDER	SHLDR	SHOULDERED
AL	ALUMINUM	EQPT	EQUIPMENT	MACH	MACHINE	SKT	SOCKET
ASSEM	ASSEMBLED	EXT	EXTERNAL	MECH	MECHANICAL	SL	SLIDE
ASSY	ASSEMBLY	FIL	FILLISTER HEAD	MTG	MOUNTING	SLFLKG	SELF-LOCKING
ATTEN	ATTENUATOR	FLEX	FLEXIBLE	NIP	NIPPLE	SLVG	SLEEVING
AWG	AMERICAN WIRE GAGE	FLH	FLAT HEAD	NON WIRE	NOT WIRE WOUND	SPR	SPRING
BD	BOARD	FLTR	FILTER	OBD	ORDER BY DESCRIPTION	SQ	SQUARE
BRKT	BRACKET	FR	FRAME or FRONT	OD	OUTSIDE DIAMETER	SST	STAINLESS STEEL
BRS	BRASS	FSTNR	FASTENER	OVH	OVAL HEAD	STL	STEEL
BRZ	BRONZE	FT	FOOT	PH BRZ	PHOSPHOR BRONZE	SW	SWITCH
BSHG	BUSHING	FXD	FIXED	PL	PLAIN or PLATE	T	TUBE
CAB	CABINET	GSKT	GASKET	PLSTC	PLASTIC	TERM	TERMINAL
CAP	CAPACITOR	HDL	HANDLE	PN	PART NUMBER	THD	THREAD
CER	CERAMIC	HEX	HEXAGON	PNH	PAN HEAD	THK	THICK
CHAS	CHASSIS	HEX HD	HEXAGONAL HEAD	PWR	POWER	TNSN	TENSION
CKT	CIRCUIT	HEX SOC	HEXAGONAL SOCKET	RCPT	RECEPTACLE	TPG	TAPPING
COMP	COMPOSITION	HLCPS	HELICAL COMPRESSION	RES	RESISTOR	TRH	TRUSS HEAD
CONN	CONNECTOR	HLEXT	HELICAL EXTENSION	RGD	RIGID	V	VOLTAGE
COV	COVER	HV	HIGH VOLTAGE	RLF	RELIEF	VAR	VARIABLE
CPLG	COUPLING	IC	INTEGRATED CIRCUIT	RTNR	RETAINER	W/	WITH
CRT	CATHODE RAY TUBE	ID	INSIDE DIAMETER	SCH	SOCKET HEAD	WSHR	WASHER
DEG	DEGREE	IDENT	IDENTIFICATION	SCOPE	OSCILLOSCOPE	XFMR	TRANSFORMER
DWR	DRAWER	IMPLR	IMPELLER	SCR	SCREW	XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000AH	STANDARD PRESSED STEEL CO., UNBRAKO DIV.	8535 DICE ROAD	SANTA FE SPRINGS, CA 90670
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
93907	CAMCAR SCREW AND MFG. CO.	600 18TH AVE.	ROCKFORD, IL 61101

@

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	334-3727-00			1		PLATE,IDENT:MKD GENERAL PURPOSE PROBE	80009	334-3727-00
-2	380-0608-00			1		HSG HALF,CKT BD:TOP	80009	380-0608-00
						(ATTACHING PARTS)		
-3	211-0093-00			4		SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
						- - - * - - -		
-4	200-2415-00			1		DOOR,ACCESS:PLASTIC	80009	200-2415-00
-5	380-0594-00			1		HSG HALF,CKT BD:BOTTOM	80009	380-0594-00
						(ATTACHING PARTS)		
-6	211-0093-00			4		SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
-7	210-0586-00			4		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
-8	343-0836-00			4		CLAMP,CABLE:3.72 L,ALUMINUM	80009	343-0836-00
-9	361-0998-00			4		SPACER,CKT BD:0.245 ID X 0.38 OD X 0.23	80009	361-0998-00
	131-2613-00			1		CONN,RCPT ELEC:CABLE	80009	131-2613-00
-10	334-3722-00			1		. SLEEVE,MKR,CA:MKD-15	80009	334-3722-00
-11	380-0591-00			1		. HSG HALF,CKT BD:TOP	80009	380-0591-00
						(ATTACHING PARTS)		
-12	211-0225-00			2		. SCR,CAP,SOC HD:4-40 X 0.312 INCH,STL	000AH	OBD
-13	210-0551-00			4		. NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	83385	OBD
-14	211-0093-00			2		. SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
						- - - * - - -		
-15	380-0590-01			1		. HSG HALF,CKT BD:TOP	80009	380-0590-01
-16	343-0836-00			2		. CLAMP,CABLE:3.72 L,ALUMINUM	80009	343-0836-00
-17	200-2412-00			2		. CABLE NIP,ELEC:3.45 L X 0.05 ID	80009	200-2412-00
-18	175-3537-01			1		. CA ASSY,SP,ELEC:64,28 AWG,48.0 L	80009	175-3537-01
-19	213-0055-00			4		. SCR,TPG,THD FOR:2-32 X 0.188 INCH,PNH STL	93907	OBD
-20	----- -----			1		. CKT BOARD ASSY:PROBE CONNECTOR(SEE A3 EPL)		
-21	131-0608-00			64		. . TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-22	213-0055-00			4		SCR,TPG,THD FOR:2-32 X 0.188 INCH,PNH STL	93907	OBD
-23	----- -----			1		CKT BOARD ASSY:GENERAL PURPOSE 1(SEE A1 EPL)		
-24	131-0590-00			3		. CONTACT,ELEC:0.71 INCH LONG	22526	47351
-25	131-1857-00			1		. TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
-26	----- -----			1		. TERM,TEST POINT:SEE A1TP6030 EPL)		
-27	131-0608-00			92		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-28	136-0252-07			10		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-29	131-0589-00			2		. TERM,PIN:0.46 L X 0.025 SQ.PH BRZ GL	22526	47350
-30	136-0634-00			8		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-31	136-0578-00			2		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-32	----- -----			1		CKT BOARD ASSY:GENERAL PURPOSE 2(SEE A2 EPL)		
-33	136-0263-04			3		. SOCKET,PIN TERM:FOR 0.025 INCH SQUARE PIN	22526	75377-001
-34	131-0993-00			1		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-35	131-0608-00			66		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-36	337-2722-00			1		. SHIELD,ELEC:ACCESS DOOR,BRASS	80009	337-2722-00
-37	175-2736-00			1		LEAD ASSY,ELEC:2,23 AWG,14.0 L	80009	175-2736-00
	352-0169-02			1		. CONN BODY,PL,EL:2 WIRE RED	80009	352-0169-00
-38	175-2737-00			1		LEAD ASSY,ELEC:8,23 AWG,14.0 L	80009	175-2737-00
	352-0166-07			1		. CONN BODY,PL,EL:8 WIRE VIOLET	80009	352-0166-07
-39	175-2738-00			1		LEAD ASSY,ELEC:8,23 AWG,14.0 L	80009	175-2738-00
	352-0166-04			1		. CONN BODY,PL,EL:8 WIRE YELLOW	80009	352-0166-04
-40	175-2739-00			1		LEAD ASSY,ELEC:8,23 AWG,14.0 L	80009	175-2739-00
	352-0166-08			1		. CONN BODY,PL,EL:8 WIRE GRAY	80009	352-0166-08
-41	175-2740-00			1		LEAD ASSY,ELEC:8,23 AWG,14.0 L	80009	175-2740-00
	352-0166-05			1		. CONN BODY,PL,EL:8 WIRE GREEN	80009	352-0166-05
-42	175-2741-00			1		LEAD ASSY,ELEC:8,23 AWG,14.0 L	80009	175-741-00
	352-0166-06			1		. CONN BODY,PL,EL:8 WIRE BLUE	80009	352-0166-06
-43	175-2742-00			1		LEAD ASSY,ELEC:10,23 AWG,14.0 L	80009	175-2742-00
	352-0168-03			1		. CONN BODY,PL,EL:10 WIRE ORANGE	80009	352-0168-03
	195-0957-01			2		LEAD ELECTRICAL:18 AWG,9.0 L,0-N	80009	195-0957-01
-44	200-2412-00			2		CABLE NIP,ELEC:3.45 L X 0.05 ID	80009	200-2412-00
-45	334-3797-00			1		SLEEVE,MKR,CA:MKD ADDRESS 7-0	80009	334-3797-00
-46	334-3798-00			1		SLEEVE,MKR,CA:MKD ADDRESS 23-16	80009	334-3798-00
-47	334-3799-00			1		SLEEVE,MKR,CA:MKD ADDRESS 15-8	80009	334-3799-00
-48	334-3800-00			1		SLEEVE,MKR,CA:MKD DATA 7-0	80009	334-3800-00
-49	334-3801-00			1		SLEEVE,MKR,CA:MKD DATA 15-8	80009	334-3801-00
-50	334-3802-00			1		SLEEVE,MKR,CA:MKD CONTROL 9-0	80009	334-3802-00

FIG. 1 EXPLODED
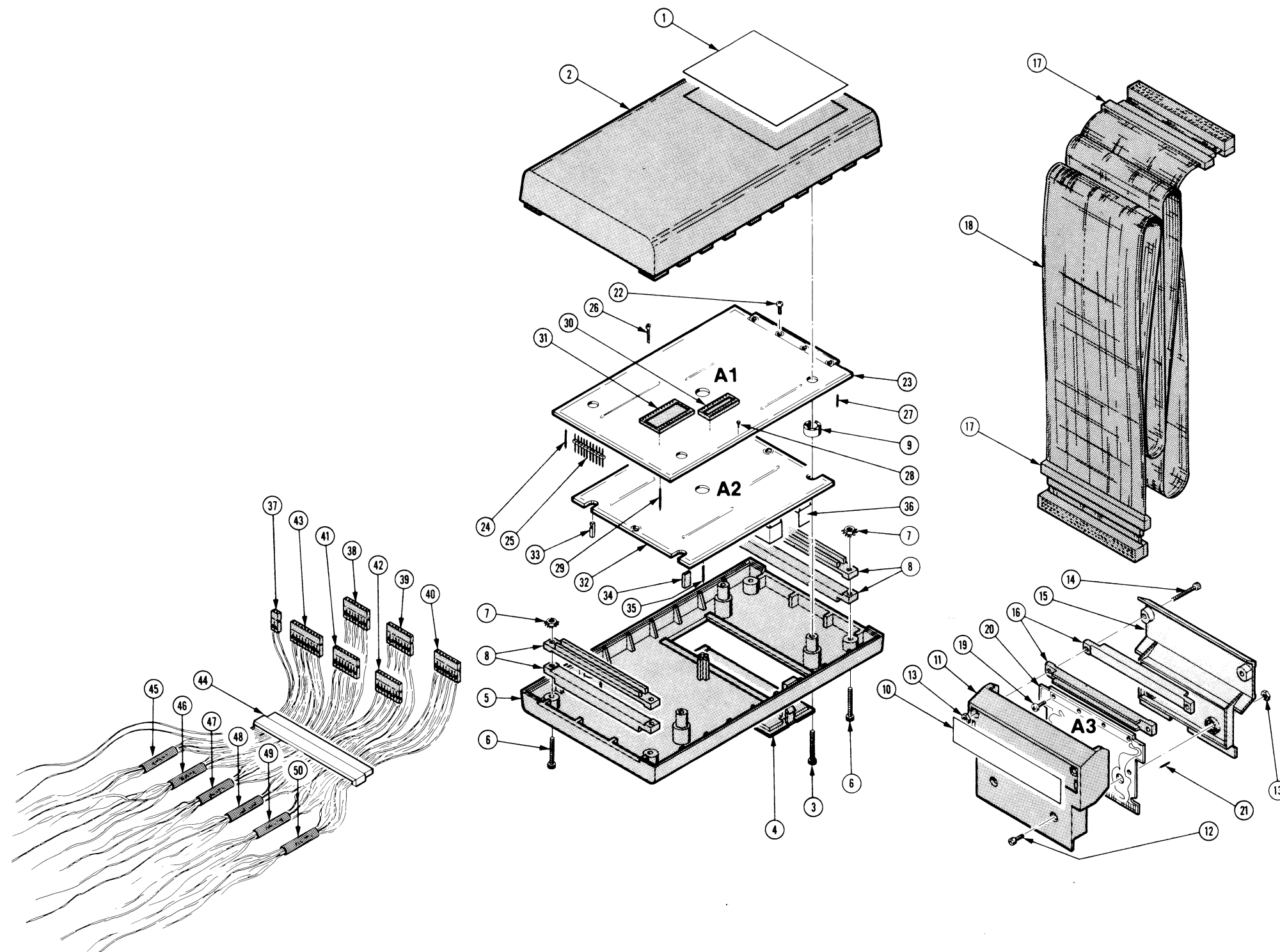
Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
	070-2917-00			1		MANUAL,TECH:INSTR,010-6460-04	80009	070-2917-00

PM 101 GENERAL PURPOSE PERSONALITY MODULE

SIGNAL GLOSSARY

This section contains an alphabetical listing of all the signals which go to or from the PM 101 General Purpose Personality Module as well as a brief explanation of what each signal does.

Signal	Description	Signal	Description
AIØ—AI23	Address lines from the Personality Module to the Logic Analyzer, except Ø thru 7 which are bidirectional.	DIØ—DI15	Data lines going from the Personality Module to the Logic Analyzer.
CIØ—CI3	Control lines from the Personality Module to the Logic Analyzer. These lines are stored and are available for event recognition in the Word Recognizer.	/HALT S.U.T.	A low-going halt command from the Logic Analyzer to the Personality Module. After buffering, this signal becomes /STOP S.U.T. which goes to the System-Under-Test.
CI4—CI5	Control lines from the Personality Module to the Logic Analyzer. These lines are available for event definition in the Word Recognizer.	PAIØ—PAI23	Address lines from the System-Under-Test to the Personality Module. (See AIØ—AI23.)
CLK	Non-inverted ECL clock signal from the Personality Module to the Logic Analyzer. This signal is generated by CLK IN from the S.U.T.	PCIØ—CPI9	Control lines from the System-Under-Test to the Personality Module. (See CIØ—CI9.)
/CLK	Inverted ECL clock signal from the Personality Module to the Logic Analyzer. This signal is derived from CLK IN from the S.U.T.	PDIØ—DPI15	Data lines from the System-Under-Test to the Personality Module. (See DIØ—DI15.)
	NOTE	QØ—Q9	The same as PCIØ—PCI9.
	A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies	/STOP S.U.T.	A low-going halt command from the Personality Module to the System-Under-Test. This signal is a buffered version of /HALT S.U.T. from the Logic Analyzer.
	0 — Write *1 — Read*		

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

DESCRIPTION

REPLACEABLE ELECTRICAL PARTS LIST CORRECTION

CHANGE TO:

A2U3020   156-0462-00   MICROCIRCUIT,DI:HEX SCHMITT TRIGGER

The above part is located on the A2 GENERAL PURPOSE 2 circuit board assembly and shown on the A2 SELF TEST STIMULUS CIRCUITRY diagrm 2.

DESCRIPTION

TEXT CHANGES

SECTION 3 SPECIFICATIONS

Table 3-1 page 3-2

Delay through ECL clock specification under Supplemental Information

CHANGE TO:

       12.0 ns min

       15.5 ns max

Table 3-3 page 3-3

Temperature specification under Supplemental Information

CHANGE TO:

       Operating: -15° C to 55° C

DIAGRAM CHANGE

Diagram 1B ROM, CLOCK, AND CONTROL CIRCUITRY

R6049

CHANGE TO: 330 ohm

R6034

CHANGE TO: 8.45 kohm

DESCRIPTION

TEXT ADDITION

SECTION 9 REPLACEABLE MECHANICAL PARTS

ACCESSORIES

ADD:

    206-0222-00   53 HOOK TIP,RETRACTABLE