

These are the major points that I'd like to touch on.

Agenda

I'd like to share my group's philosophy with you because
general framework
forms a ~~basis~~ for guiding development

PHILOSOPHY

Harry Poston →

COMPARISONS TO 7854

Extension from 7854
Successful product for 3yrs

MAJOR CHARACTERISTICS

Some primary
Specs

HUMAN INTERFACE EXAMPLE

and then an
example of what
to give a feel
we're thinking
to make the ET
Box
easy to use

DESIGN CONCEPTS

How we plan to build the ET

Peter's Note: 7854

Last 2 yrs 1472 units

Life (3yrs) 2500 units

W/O calculator 4 units!

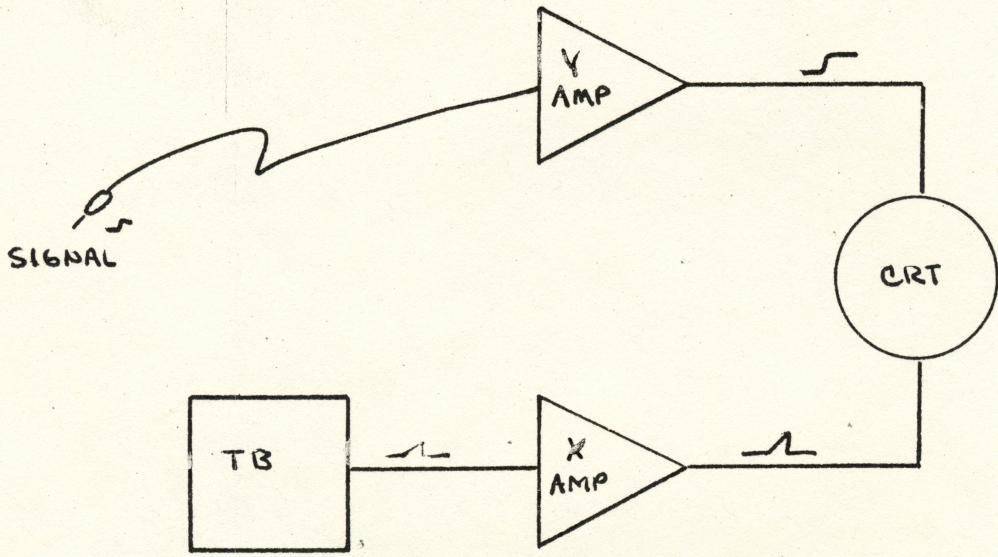
Agenda

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INTRODUCTION	1
DIGITAL SCOPES	2
ET PROGRAM	2
PROJECT DESCRIPTION	18
CRITICAL COMPONENTS	4
QUESTIONS	3

TR/hk (CPM/125/DOGNPONY)

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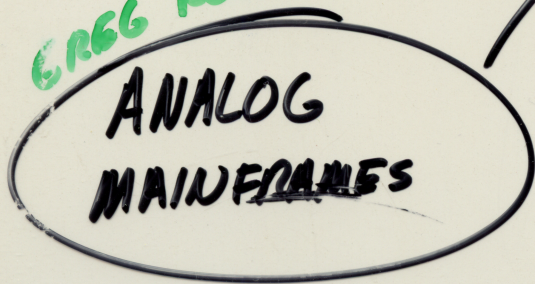
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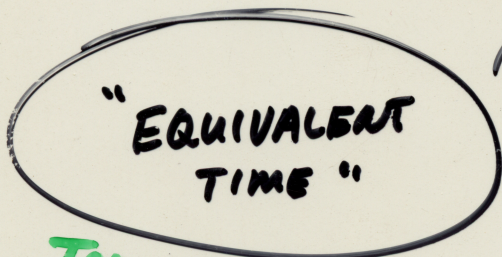
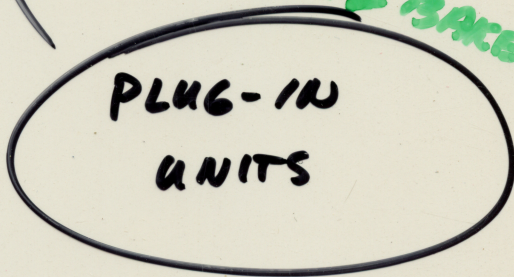
LAB SCOPES

THOR
HALLEN

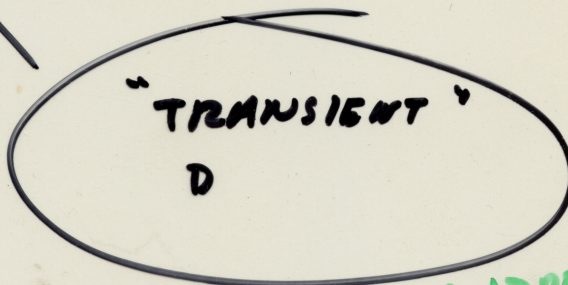
EREG ROBBERS



CLIFF BAKER



TOM DOUSSEAN



GENE ANDREWS

7853DP DIGITAL OSCILLOSCOPE**"EQUIVALENT TIME" MAINFRAME****GENERAL DESCRIPTION**

The 7853DP is a digital oscilloscope offering many features which make it a versatile instrument for general purpose waveform measurements:

- * Digital-only design (without HF analog display path) provides significantly improved measurement accuracy and flexibility at a much lower cost, when compared to conventional scopes.
- * 20 MS/s, 10 bit, 500 MHz digitizer satisfies most general purpose needs.
- * "Live" operation for normal scope-like viewing of signals.
- * "Storage" operation for retention and recall of signals.
- * Friendly manual operation from the front panel.
- * 100% functionally programmable for complete remote control of all functions and controls (ideal for system applications).
- * High speed data and control I/O ports, including IEEE-488 and RS-232C, with expansion capabilities to others.
- * Extensive waveform parameter measurement and processing functions for accurate and repeatable answers.
- * Signal Averaging and Envelope acquisition capabilities.
- * User selectable Auto-ranging feature simplifies operation, allowing the user to focus attention on the measurements rather than driving the scope.
- * Automatic Self-cal (internal time/temp algorithm) for high accuracy measurements...even from a cold start.
- * Soft-labeled functions significantly reduce front panel clutter and simplify operation...for the novice and expert alike.

26 July 83

*Changes of
June 84*

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- * Soft-labeled functions significantly reduce front panel clutter and simplify operation...for the novice and expert alike.

- * Three hardware plug-in compartments allow the user to configure the acquisition front-end for specific measurements (LEFT and RIGHT for vertical signals, and AUX for trigger conditioning as well as vertical signals); these compartments also allow for possible future analog/digital special purpose plug-ins.
- ~~* Two software plug-in compartments allow the user to add more measurement/processing power as Tek develops new applications (ROM-Paks).~~
- * Built-in timebases for improved accuracy.
- * Modular construction of both hardware and software means the scope never becomes obsolete, since the basic mainframe can be added to or updated as technology evolves (specifically applies to the digitizer, display, and measurement/processing capabilities).
- * Hardcopy and Mass Storage capabilities when coupled to appropriate external devices via one of the I/O ports. → PC
- * Simplified construction techniques for ease of manufacture and high reliability.
- * Fully compatible with 7K+ plug-ins: limited compatibility with selected 7K plug-ins when equipped with downgrade option.

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CHARACTERISTICS:

Signal Acquisition:

Sampling Rate:	20MS/s.
A/D Resolution:	10 bits.
Equivalent Time Bandwidth:	500 MHz, mainframe only. 300 MHz, with popular plug-in.
Equivalent Time Transient Response:	700 ps risetime with less than 3% aberrations, mainframe only.
Vertical Accuracy:	0.4% DC to 1 MHz, 1.4% 1 MHz to 30 Mhz, mainframe only.
Analog Input Channels:	Three plug-in compartments, all equivalent (allows for up to 12 input channels with 4-trace plug-ins).
Record Length:	501 points to 10,001 points, user selectable in a 1-2-5 sequence.
Timebases:	Two identical built-in timebases allow for independent or delaying/delayed operation; input BNC provided for external source.
Record Durations:	5 ns to 1000 s, user selectable in a 1-2-5 sequence (no variable timebase).
Timebase Accuracy:	0.01%.
Acquisition Memory:	1001 points standard, optionally expandable to 10,001 ^{16K} points.
Trigger:	Allows viewing/storage of signals, + to - 100% of the trigger point.
Trigger Source:	Any plug-in compartment (A13/B13) or external BNC.

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Displays

CRT: 4.3 inch (Horiz) x 5.3 inch (Vert) useable display area, monochrome, P-31 phosphor, crisp spot, electromagnetically deflected.

Technique: Vertical Raster Scan, non-interlaced; bit-mapped static display with vertical scan dynamic display; 550 horiz by 704 vert pixels.

Color: Not available on base product at initial introduction. Architecture allows for LCCS or shadow mask color to be added later, though technical problems remain to be solved in either case.

Intensity: Four programmable levels: off, low, med, high.

Scanning Freq: 36.6 kHz horiz, 60 Hz vert.

Composite Video: Available option; odd ball rate, workable with Tek 690SR.

Display Modes: Waveform, Program, Help, Status, Utilities,...

Characters: 7 x 12 dot matrix; 55 characters per row, 44 rows; full ASCII set plus Tek specials.

Waveforms: Fixed display at ~~501~~⁵¹² points per waveform (other resolution records are compressed/expanded for display purposes only...retain full resolution in main memory); maximum of 8 waveforms displayed at a time; X-Y and Y-T

Graticule: Electronic; linear ~~and log~~^{possible} standard (others available as option...as market applications are identified)

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Storage:

Waveform Memory: ~~10,001~~ ^{~50k} points standard, optionally expandable to ~~50,001~~ ^{~220k} points.

"Front Panel" Set-ups: 10 configurations, maximum (internally).

~~Programs: Up to 1000 commands (internally).~~

Power down: ~~All waveforms, programs,~~ configuration and front panel settings are retained for two weeks or more.

Mass Storage: External, for waveforms, panel set-ups, ~~programs.~~ ^{on PC}

Waveform Processing:

Cursors: One or two per waveform, absolute or relative measuring.

Acquisition: Average, Envelope, Ground, Readout.

Waveform Parameters: Amplitude: Max, Min, P-P, RMS, Mean, Mid;
Pulse: Rise, Fall, Width, Delay, Freq, Per, Energy, Area.

Waveform Functions: Diff, Integ, Interp, Smooth.

Arithmetic Operators: +, -, /, *, Sqrt, Log, Exp, Abs, Sin, Cos, Signum.

Numeric Entry: 0 thru 9, ., exponent, change sign.

~~Alpha Entry: A thru Z, upper and lower case.~~

Storage:

Waveform Memory:	10,001 points standard, optionally expandable to 50,001 points.
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~~Programming:~~

~~Simple sequences of linked commands can be programmed to be associated with each waveform; complex programs require external optional Waveform Programmer keyboard.~~

Other:

Plug-in compatibility:

Fully compatible with all programmable 7K+ plug-ins; downward compatible with selected 7K plug-ins ~~when equipped with optional downgrade kit:~~ 7D20, 7A15A, 7A16A, 7A18A, 7A26, 7A17, 7A13, 7A22, 7A11, 7A24, 7A19, 7A29, 7S11, 7T11, 7M11, 7S12, 7S14, 7L14, 7L18, 7L5, 7L12, 7K11 (non-programmable).

Power:

110/220 VAC, 50/60 Hz; 400 Hz operation with fan option.

~~300~~³¹⁵ Watts maximum line, fully loaded mainframe under worst case load conditions.

Size:

8.75 (H) x 16.75 (W) x 20 (D) cubic inches (bench);
8.75 (H) x 19.00 (W) x 20 (D) cubic inches (rack).

Reliability:

10,000 Hrs MTBF at 25°C, mainframe only.

Hardcopy:

Device drivers optional for output to specified hardcopy units via standard Centronics interface (possibly a Tek ink-jet copier with Tek interface will be amongst the offerings...from Wilsonville)

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PC

Mass Storage:

~~Device drivers optional to interface with specified mass storage units via GPIB port (possibly a Tek dual floppy drive unit with Tek interface...from Wilsonville)~~

Self-cal:

Invoked automatically to present settings whenever time and/or temperature change beyond specified limits, or when a setting is changed. Total self-cal time is less than 100 ms. Mainframe controls process, calibrating mainframe and plug-in DC balances, offsets, and low frequency gains.

Auto-ranging:

At the users selection, provides automatic ranging of acquisition vertical and/or horizontal scale factors, and/or triggering.

Options:

~~Waveform Programmer Keyboard:~~

~~Extends programming capability from simple linked sequences to complex programs.~~

Expansion Acquisition Memory:

~~Extends digitizer to 5001 or 10,001 points.~~ 16k

Main Memory:

~~Extends waveform storage to 20,001 or 50,001 points.~~
~50k ~220k

Device Drivers:

~~Disk driver for xxxx model disk drive unit(s), via GPIB and/or proprietary ports.~~

Printer driver(s) xxxx for model hardcopy unit(s), via Centronics port.

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Main Memory: Extends waveform storage to 20,001 or 50,001 points.

Device Drivers: Disk driver for xxxx model disk drive unit(s), via GPIB and/or proprietary ports.
Printer driver(s) xxxx for model hardcopy unit(s), via Centronics port.

Color:

Adds 3 or 8 color display (LCCS and/or shadow mask). (Not available at product introduction. ~~Will~~ ^{MAY} be developed as separate engineering project).

~~Rom Paks:~~

~~Mass Storage and Hardcopy Drivers.
Amplifier gain correction.
New Applications, as determined by our market needs.~~

Option ROMs:

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Plug-in Downgrade:

Provides limited compatibility with selected 7K plug-ins.

~~400 Hz Fans~~

~~Substitutes 50/60 Hz fan with 400 Hz fan.~~

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	TITLE	CONTACT
1	7853DP Digital Oscilloscope General Description	Rousseau
2	Responsibilities (people)	Rousseau
3	External Specification	Fladstol
4	Hardware Specification	Fladstol
5	7853DP Oscilloscope Primer	Fladstol
6	7853DP Oscilloscope Measurement Techniques	Fladstol
7	7853DP FW Project Plan	Hinrichs
8	"C" Coding Standard	Austin
9	7853DP Display Controller HW/SW Interface Spec	Diehm
10	7853DP Memory Management Unit HW/SW Interface Spec	Gupta
11	7853DP Software Quality Assurance Plan	Hinrichs
12	7853DP Hardware Architecture Overview	Stanley
13	ET Firmware Architecture	Stanley
14	Operating System Functional Specification for the ET Digitizer Processor	Schakel
15	7853DP Executive Processor Prototype Firmware Spec	Batson
16	ET Mainframe Interrupt Controller HW/SW Interface Spec	Hastings
17	ET Standard I/O Board RS-232 Port HW/SW Interface Spec	Hastings
18	ET Mainframe SDI HW/SW Interface Spec	Hastings
19	ET Temperature Sensor and Tone Generator HW/SW Interface Spec	Hastings
20	ET Mainframe Programmable Interval Timer HW/SW Interface Spec	Hastings
21	ET Printer Port HW/SW Interface Spec	Hastings
22	ET User Input HW/SW Interface Spec	Hastings

Engineering recommends changes to the ET program in order to reduce risks and schedule slippages. The recommendations are:

- * eliminate some product features;
- * slightly increase engineering personnel, staged over the next year;
- * clearly establish ET project priority;
- * adjust target PSR to first quarter of FY 700.

Details of this recommendation and associated risks and contingencies follow.

Several alternatives were considered while working towards this recommendation. They were rejected primarily based on time to market, product viability and risks, although their discussion contributed to the final recommendation. These alternatives are summarized following the recommendation.

Please see Tom Rousseau for further information.

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RECOMMENDATIONS:

Features: Eliminate instrument programming language and limit programming composite processing to one operator.

Eliminate dedicated mass storage capability.

Limit Auto-scope to be the same as the HP1980.

Limit Waveform Compressor performance to min/max display only.

Resources: Add one HWE III/IV to Digitizer control/DAG circuit by the end of AP 502.

Add two SWE I/II at the beginning of SW coding stage, last quarter FY 500.

Support: Establish ET priority relative to other projects to insure that ECBs, evaluation, prototype, and technician requirements are not in the critical path. Make corrective adjustments if they come into the critical path.

Schedule: Target PSR is first quarter FY 700, with 50% confidence factor; second quarter FY 700, with 80% confidence factor.

Program will be managed to the following targets:

HDC	510
HPR	603
HER	609
FDC	513
FIR	608
FER	613
PSR	701

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DISCUSSION OF RECOMMENDATIONS:

Features:

Elimination of programming language and mass storage reflect the change of attitude towards this requirement. In the instrument's target user environment, the pervasiveness of personal computers is expected to obviate the need for self-contained programming and mass storage. It is now expected that a user can more effectively have these capabilities via his pc connected to the ET via a GPIB or RS-232 port. This change in attitude requires that Marketing identify and support specific pc's.

Programming of composite functions has diminishing value with multiple operators. One operator allows for composite functions such as: "wfm1 * wfm2", "wfm3 - wfm6", "wfm3/5"

Elimination of these features very significantly reduces the SW specification and design task; these features are not well defined, nor were they expected to be for several months due to conflicts of expectations and manpower restrictions.

Auto-scope becomes a fairly small task if it is expected to have the same characteristics as the HP1980. Beyond this, Auto-scope becomes a difficult task to resolve due to conflicts of performance expectations.

Limiting the waveform compressor to min/max eliminates uncertainty about algorithms for a variety of "averaging" schemes. The situation is that the averaging schemes have several potential pitfalls which have not been sorted out; min/max has been built and demonstrated...it has no design problems. The only reason for considering averaging is that it potentially could provide a more pleasing display to the eye when in the compressed display mode. However, the latter point is somewhat moot, in that a user can avoid the compressed waveform mode by selecting horizontal scrolling.

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DISCUSSION OF RECOMMENDATIONS (cont):

Resources: Three people are added to critical path items.

The control logic and DAG gate array designs tasks were previously under estimated; combined, they are proving to be a two person job with only one person working on them.

The two software people coming on line just before the coding phase helps to reduce coding time in the waveform manager and operating system areas. These can be college hires. They are not needed nor wanted during the specification and design phases.

Support: The revised schedules were established with the assumption that long ques would be avoided for ECBs. Most boards expected to go around 4-5 times before ER, except the Acquisition and Timebase boards at 7-8 times (due to critical analog circuits and interactions with new ICs).

The assumption ~~was made~~ that minor changes (eg, metal only) to ICs could go around within a month and major ones within three months.

If ET is judged to be high priority to management, then commensurate support is needed.

Schedule: Confidence factor means a 50/50 chance, or 80/20 chance of occurring as stated. There is certainly a risk that we won't hit first quarter, though the chance that we will is reasonable. If all goes reasonably well, then we'll make it. If there are unexpectedly severe IC, or system integration problems (including SW, plug-ins, and Manufacturing) then slips may occur.

Scheduling does not include the impact of the HMOS problem (disappearing vendor...Tek). If a solid resolution is not reached by the end of AP 501, then we can expect as much as a 2 for 1 slip until it is. We run the risk of having to start from scratch on the two HMOS parts.

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MAJOR RISKS AND CONTINGENCIES:

AREA	RISK	CONTINGENCIES
IC Turn around time	More than three go arounds. Longer than 3 months for a go around. Loss of HMOS increases dependencies on outside.	For Tek ICs, install Lab Scope IC champion in Bldg 59. Add experienced IC designers to ET team. Delay project.
Digitizer Performance	Difficulty achieving satisfactory Equivalent Time speed. Satisfactory Sample and Hold Hybrid. Time Interpolator IC: performance and functionality on schedule.	Highly experienced engineers on parts; high priority in IC and Hybrid support areas. Reduce performance expectations.
Power/Cooling	Too much power = inadequate cooling.	Convert more TTL farms to VLSI. Higher CFM and noisier fan. Lower reliability expectations.
Human Interface	Unacceptable error rates. User acceptance.	Lower expectations. Redefine and delay project.
HW/SW Integration	Severe problems.	Delay project and/or lower performance expectations.
Mainframe/Plug-in Integration	Severe problems. Inadequate quantities of hardware, software, people to test.	Delay project and/or lower performance expectations.
Technicians	Lack of sufficient quality and quantity.	Engineers do work.
Prototype FW	Insufficient support for HW. Too much demand on SW group.	HW engineers write prototype code. Delay product and/or diagnostics code.
Thru-put performance "Live"	Too slow.	Depend more heavily on assembly coding. Accept performance as is.
SW Evaluation	Insufficient resources.	Reduce expectations. More black box less White box testing.
SW Development Tools	Adequate C compiler not available in time. No toolsmith.	Convert to a VAX/VMS environment and use Intel tools. Purchase Intel NRM and several Series IV's.
Morale	Could become low under heavy project stress. Could create family problems for employees.	Provide extraordinary incentives with benefits shared by spouse and family.

MAJOR RISKS AND CONTINGENCIES:

AREA	RISK	CONTINGENCIES
IC Turn around time	More than three go arounds. Longer than 3 months for a go around. Loss of HMOS increases dependencies on outside.	For Tek ICs, install Lab Scope IC champion in Bldg 59. Add experienced IC designers to ET team. Delay project.
Digitizer Performance	Difficulty achieving satisfactory Equivalent Time speed. Satisfactory Sample and Hold Hybrid. Time Interpolator IC: performance and functionality on schedule.	Highly experienced engineers on parts; high priority in IC and Hybrid support areas. Reduce performance expectations.
Power/Cooling	Too much power = inadequate cooling.	Convert more TTL farms to VLSI. Higher CFM and noisier fan. Lower reliability expectations.
Human Interface	Unacceptable error rates. User acceptance.	Lower expectations. Redefine and delay project.
HW/SW Integration	Severe problems.	Delay project and/or lower performance expectations.
Mainframe/Plug-in Integration	Severe problems. Inadequate quantities of hardware, software, people to test.	Delay project and/or lower performance expectations.
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ALTERNATIVES:

ALTERNATIVE	FEATURES	RESOURCES	TIME	CONFIDENCE	COMMENTS
#1 So called "Optimum" ET	Full feature set as described 2 Jun 84.	No additional engineers.	PSR AP 710	80%	Unacceptable because takes too long.
#2	Same as #1.	Add 3 engineers, 1 Digitizer, 2 SW	PSR AP 706	65%	Unacceptable because takes too long.
#3 First Quarter Plan	Eliminate pro- gramming; simple autoscope	Add 3 engineers, 1 Digitizer, 2 SW	PSR 1st Qtr FY 700 PSR 2nd Qtr FY 700	50% 80%	Requires clear project priority. This is the recommendation.
#4 "Minimum" DSO	Digital Storage & Display; not extensible; no programming or measurements		PSR AP 610	20-80%	Major project reset. Likely loose key people. Would still take longer than #3.
#5 Add digitizer to RT	Same as RT with 7854 style digitizer; No live digital dsy; No processing.	Same as RT + 4	PSR 613	40-70%	Requires ET Sample and Hold; not much enhancement over 7854. Very expensive.
#6 7854 Upgrade	Same as 7854 with functional program- ability added.	5 engineers	PSR 610	80%	Not much product enhance- ment over 7854; Very expensive (\$7K af + 1.5K per plug). Only dual trace, no delayed sup.

NOTES:

Given that shortest time to market is important, alternative #3 is viewed as the minimum risk. All others, except #6, are expected to either take longer or offer much less return for about the same time and effort. #6 does not provide a viable product to base our future on; at best, it is a stop gap product which would consume resources (about 13-15 people with support).

In the terms of #4, "minimum DSO", #3 is already the minimum we can do within time constraints. #4 would take longer for less product, due to being a major reset.

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NOTES:

PSR is the time Manufacturing is ready to output first products.
PSR is not the same as customer availability, unless Marketing
demo requirements are zero. CA will typically lag PSR by the
amount of time required to fill demo requirements at the
Manufacturing output rate.

TR/hk (CPM/130/RECOMEND.ET)

NOTES:

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PSR is not the same as customer availability, unless Marketing
demo requirements are zero. CA will typically lag PSR by the
amount of time required to fill demo requirements at the
Manufacturing output rate.

IV. PHASED RELEASES.

It was decided that there would be three Phased Releases of the Product Firmware, with the following schedule:

RELEASE	AREA	FEATURES
Release I AP 605	DIG	All except Autocal, Autoscope, and limited set of plugins only.
	DSY	YT Waveforms; Lines; Graticules
	EXP HL	Menu processor; ASCII Parser
	EXP LL	D/S (minus some calls); Internal Comm; External Comm; 'Easier' GPIB
	HIM	Waveforms w/o windows; Major menus; Icons; Axes
	LLCmd	Simple waveforms (single wfm only); Parameter setting/changing
	DIAG	Self-test (Power-up)
	WFM MGR	To be determined
	GENERAL	Error detection, but no error recovery
	Release II AP 608	DIG
DSY		Recovery from temporary items (Popups); Everything else.
EXP LL		Autocal; Autoscope; Touchscreen; RS232 Comm; 'Tricky' GPIB
HIM		All else: Meters, Knobs, etc.
LLCmd		Functions added to sources; multiple wfms; Cursors; Windows
DIAG		Interactive diagnosis
WFM MGR		To be determined
Release III AP 610	GENERAL	Error Recovery
	EXP LL	Hard copy interface
	LLCmd	Vertical Source functions and Measurement commands; Error detection.
	WFM MGR	To be determined

Wendy Wanlass, M.D.
Internal Medicine

4855 S.W.
Western
Avenue
Beaverton,
Oregon
97005
503 643-7565

1
39
20
26
52
80

219 Knobs/buttons

44
20
30
58
115

267 Commands/functions

7854

2 knobs
38 Hand buttons
24 Status indicators

NORTHWEST
Permanente
P.C. / PHYSICIANS & SURGEONS

Transparent Touch Panel

Custom ICs

<i>SH3</i>	Quantizer Comparator Buffer/Multiplexer Time Interpolator
<i>HMOS</i>	Timebase Digitizer Control MMU Waveform Compressor
<i>NEC CMOS</i>	Vertical Raster Scan

Hybrids	Sampler Buffer/Multiplexer
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Color Shutter (Option)

Critical Components

Transparent Touch Panel

Custom ICs

SH3	Quantizer Comparator Buffer/Multiplexer Time Interpolator
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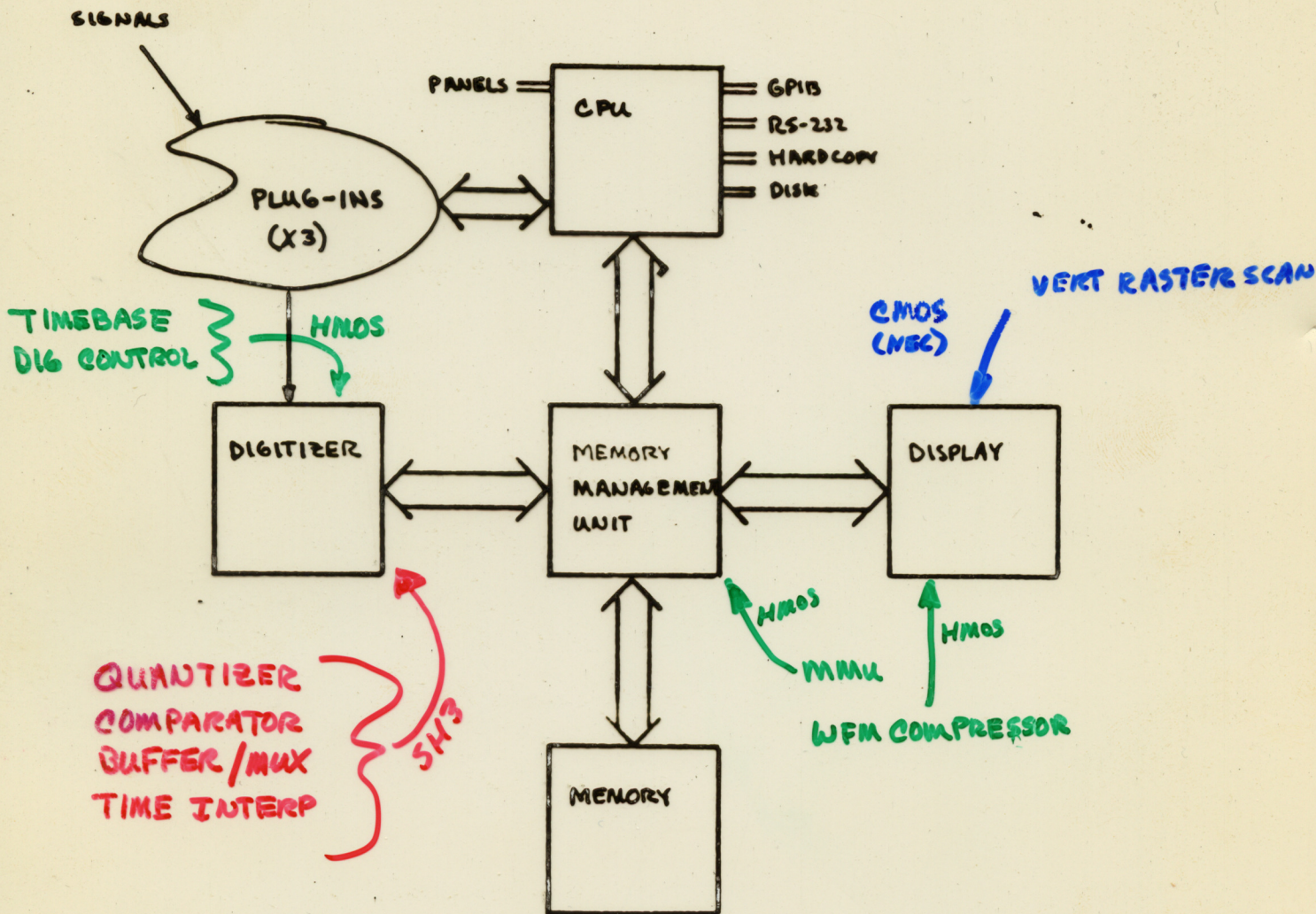
HMOS	Timebase Digitizer Control MMU Waveform Compressor
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NEC CMOS	Vertical Raster Scan
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Hybrids	Sampler Buffer/Multiplexer
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Color Shutter (Option)

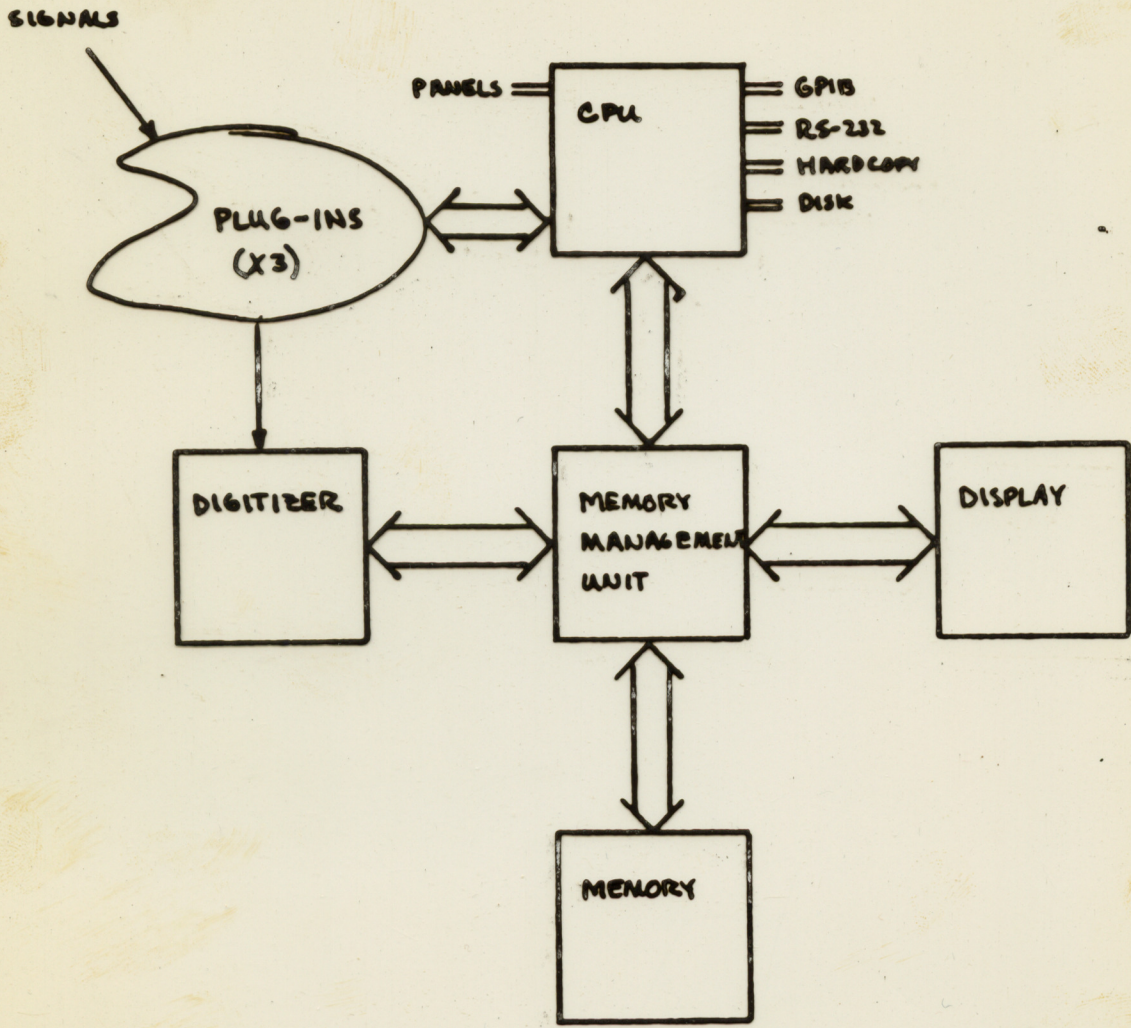
Custom ICs + Hybrids



⇔ DIGITAL

→ ANALOG

Architecture



⇔ DIGITAL
→ ANALOG

18 Oct 83
TR

• FOR THE USER:

More Performance for the \$

- FLEXIBILITY TO ADAPT TO CURRENT/FUTURE NEEDS
 - * PLUG-INS (HW)
 - * OPTION ROMS (FW)
- EASIER TO USE
- ENHANCED MEASUREMENTS
 - * MORE ACCURATE
 - * FASTER
 - * AUTOMATED

• FOR TEKTRONIX:

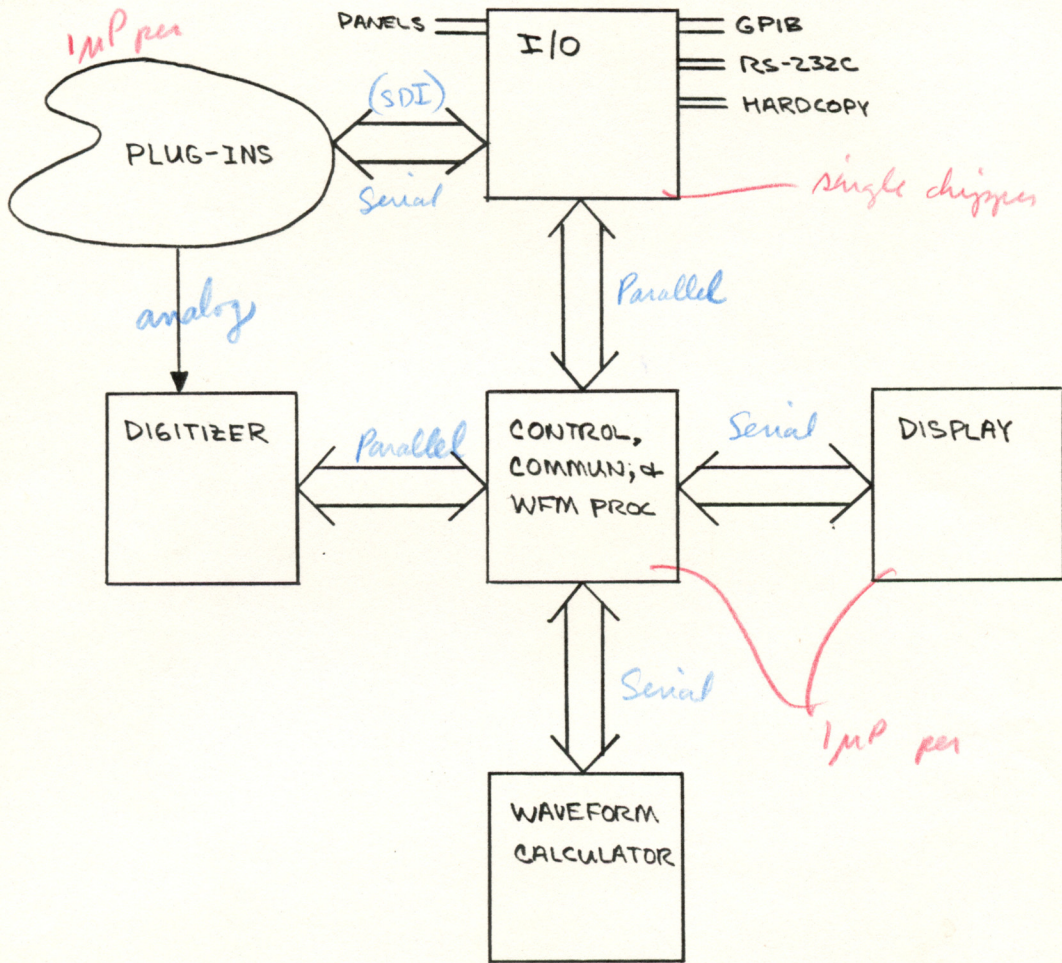
New, Powerful, Flexible Architecture

- COMPLETELY NEW
- MODULAR HW & FW
- MUCH GREATER FLEXIBILITY TO CONFIGURE NEW PRODUCTS
- FASTER TIME TO MARKET FOR FUTURE PRODUCTS



Difficult
Barrier for
Competition
to Overcome

Architecture



7854 Sales

I'm going to describe the ET mainframe to you.

Addressing the more sophisticated user who demands greater accuracy and efficiency with ^{general} measurements, but is still sensitive to cost.

It means our foremost goal is to provide the best balance of solutions to measurement problems.

Every feature we put into the box has real value ~~towards improving measurements.~~

The human interface is not precisely defined at this time, but we do have some general concepts thought out.

Our goal is to minimize the user's concern with setting up the scope, allowing him to concentrate on his measurements, instead.

TEK INTER-OFFICE COMMUNICATION

LAB SCOPES PRESENTATION SCHEDULE

TO: Distribution List
FROM: George Kersels
SUBJECT: Meeting Agenda

for
Wed 19 Oct

DATE: Oct. 5, 1983

I have asked Thor Hallen of ISD to have his organization give us a presentation. The time, place and agenda are listed below. I would like everyone in ECO from 2nd level managers and up to plan to attend this session.

If you have any questions give Vikki (x5431) a call.

DATE: Wednesday
October 19th

TIME: 1:00pm - 5:00pm

PLACE: PGE Building (Auditorium)
Corner of Old Scholls Ferry Road
and Murry Blvd.

PLEASE CARPOOL WITH SOMEONE ELSE
IF YOU POSSIBLY CAN... THEIR PARKING
IS VERY MINIMAL

AGENDA:

- 1) Introductions - George Kersels (5 mins.)
- 2) ISD/Lab Instruments Engineering - Thor Hallen, Engr, Manager (10 mins.) *go to the manager*
- 3) Greg Rogers - Real Time Manager (30 mins.) *unique features; TCB; SWH; MCP 600 MHz CAT*
- 4) Break (15 mins.)
- 5) Tom Rousseau - Equivalent Time Manager (30 mins.) *Human & tube - examples
Trade Panel; color settle;*
- 6) Gene Andrews - Transient Mainframe Manager (30 mins.) *common to family*
- 7) Break (15 mins.)
- 8) Cliff Baker - Next Generation Plug Ins Manager (15 mins.) *real both LBT & Sam Common
Noise/PS benefits*
- 9) Stu McNaughton - Current Generation Manager (30 mins.)
- 10) Questions/Answers/Discussion (30 mins.)

Distribution List

Chris Curtin
Fred Engstrom
Lisa Schultz
Aris Silzars
Wayne Spencer
Mike Swink

ECO Secretaries: NOTE: Please make sure this notice gets to the 2nd line managers and above.

TEK INTER-OFFICE COMMUNICATION

TO: Distribution

DATE: February 2, 1983

FROM: Thor Hallen

SUBJECT: **Change Of Schedules**

Phil Robinson has requested the opportunity to provide feedback on our development plans, presented to him last week.

He will be available at the beginning of our presentation this Friday. We have moved the speaking schedule back 15 minutes for his presentation.

8:15 - 8:30	Presentation by Phil Robinson
8:30 - 8:45	Introduction / Jim
8:45 - 9:15	Market Dynamics / Peter
9:15 - 9:30	Family Overview / Thor
9:30 - 10:00	Conventional Mainframes / Greg
10:00 - 10:30	E.T. Mainframes / Tom
10:30 - 10:45	BREAK - Coffee in cafeteria
10:45 - 11:15	T.D. Mainframes / Gene
11:15 - 11:30	Plug-Ins / Cliff
11:30 - 11:45	H.R. Sampling / Stu
11:45 - 12:00	Project Estimates / Thor (as needed)
12:00 - 12:15	Firmware Plan / Don (as needed)
12:15 - 12:45	Discussion / All

lcw

Tektronix
COMMITTED TO EXCELLENCE

February 2, 1988

DISTRIBUTION: Jim Cavoretto
 Peter Schot
 Greg Rogers
 Tom Rousseau
 Gene Andrews
 Cliff Baker
 Stu McNaughton
 Don Williams
 Thor Hallen

Distribution

Thor Hallen

Project Schedules

Phil Robinson has requested the opportunity to present his development plans, presented to him last week. He will be available at the beginning of our presentation on this Friday. We have moved the speaking schedule back.

8:15 - 8:30	Presentation by Phil Robinson
8:30 - 8:45	Introduction / Jim
8:45 - 9:15	Market Dynamics / Peter
9:15 - 9:30	Facility Overview / Thor
9:30 - 10:00	Conventional Maintenance / Greg
10:00 - 10:30	E.T. Maintenance / Tom
10:30 - 10:45	BREAK - Coffee in cafeteria
10:45 - 11:15	T.D. Maintenance / Gene
11:15 - 11:30	Plug-ins / Cliff
11:30 - 11:45	H.R. Sampling / Stu
11:45 - 12:00	Project Estimates / Thor (as needed)
12:00 - 12:15	Trimware Plan / Don (as needed)
12:15 - 12:45	Discussion / All

104

TEK INTER-OFFICE COMMUNICATION

TO: Distribution

DATE: February 2, 1983

FROM: Thor Hallen

SUBJECT: Reschedule of 7K+ Presentations to
Lab Scopes Engineering

The Presentation on the 7K+ Family of Instruments has been moved:

DATE: February 4, 1983, Friday

TIME: 8:15 - 12:30

PLACE: PGE AUDITORIUM

(End of Murray Rd at Scholls Ferry Rd)

Please carpool from Tektronix, as PGE has limited parking space.

Below is the schedule of presentations:

8:15 - 8:30	Introduction / Jim
8:30 - 9:00	Market Dynamics / Peter
9:00 - 9:15	Family Overview / Thor
9:15 - 9:45	Conventional Mainframes / Greg
9:45 - 10:15	E.T. Mainframes / Tom
10:15 - 10:30	BREAK - Coffe in cafeteria
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11:00 - 11:15	Plug-Ins / Cliff
11:15 - 11:30	H.R. Sampling / Stu
11:30 - 11:45	Project Estimates / Thor (as needed)
11:45 - 12:00	Firmware Plan / Don (as needed)
12:00 - 12:30	Discussion / All

The auditorium is booked until 1:00 in case of overflow.

lcw

Tektronix
COMMITTED TO EXCELLENCE

February 2, 1983

Distribution

- DISTRIBUTION:
- Jim Cavoretto
 - Peter Schot
 - Greg Rogers
 - Tom Rousseau
 - Gene Andrews
 - Cliff Baker
 - Stu McNaughton
 - Don Williams
 - Thor Hallen

Schedule of XK Presentations to Lab Scope Engineering

The presentation on the XK Family of Instruments will be held on:

DATE: February 4, 1983

TIME: 8:15 - 12:30

PLACE: PGE AUDITORIUM

(End of Xerox Job at Schott's Party)

Please respond from Tektronix, as PGE has limited parking space.

Below is the schedule of presentations:

8:15 - 8:30	Introduction / Jim
8:30 - 9:00	Market Dynamics / Peter
9:00 - 9:15	Family Overview / Thor
9:15 - 9:45	Conventional Mixtures / Greg
9:45 - 10:15	E.T. Mixtures / Tom
10:15 - 10:30	BREAK - Coffee in cafeteria
10:30 - 11:00	E.D. Mixtures / Gene
11:00 - 11:15	Plug-ins / Cliff
11:15 - 11:30	H.R. Sampling / Stu
11:30 - 11:45	Project Estimates / Thor (as needed)
11:45 - 12:00	Primeval Plan / Don (as needed)
12:00 - 12:30	Discussion / All

The auditorium is booked until 1:00 in case of overflow.

Jim

TEKTRONIX Inter-Office
Communication

To: List

Date: 1/21/83

Subject: Yesterday's Presentation to
Wim Velsink and Phil Robinson

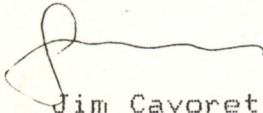
Based on comments from Phil Robinson I would classify our presentation yesterday a success.

I know there are still a lot of unanswered questions but I think we have come a long way toward gaining the additional support from Phil and Wim that this program requires.

This doesn't mean the road is "clear ahead" from now on. Resources are, and will continue to be tight. But I'm sure we will be funded to a reasonable level.

So, let's get moving!!

Best Regards,


Jim Cavoretto
Business Unit General Manager
Laboratory Instruments

List: Thor Hallen, Gene Andrews, Tom Rousseau, Greg Rogers,
Cliff Baker, Stu McNaughton, Don Williams, Peter Schot.

MANUFACTURING COST ESTIMATE

- ET Mainframe with
Mono Display, 20/10 Dig,
Waveform Calculator \$3600

- Color Option \$400

- Compares to 7854 \$4500

Based on FY300 Frozen standards

BREAKDOWN OF ET COST ESTIMATE:

	<u>Parts + Non IDC</u>
Digitizer	615
CPU	429
Display	417
Diagnostics	24
Auto-Cal	18
Option Hooks	24
Plug-in Interfacing	290
External Keyboard	120
Mechanical Pkg	240
Power Supply	150
Front Panel	134
Other	406
SUB-TOTAL	2867
ISD Labor @ 20%	717
TOTAL	<u>3584</u>

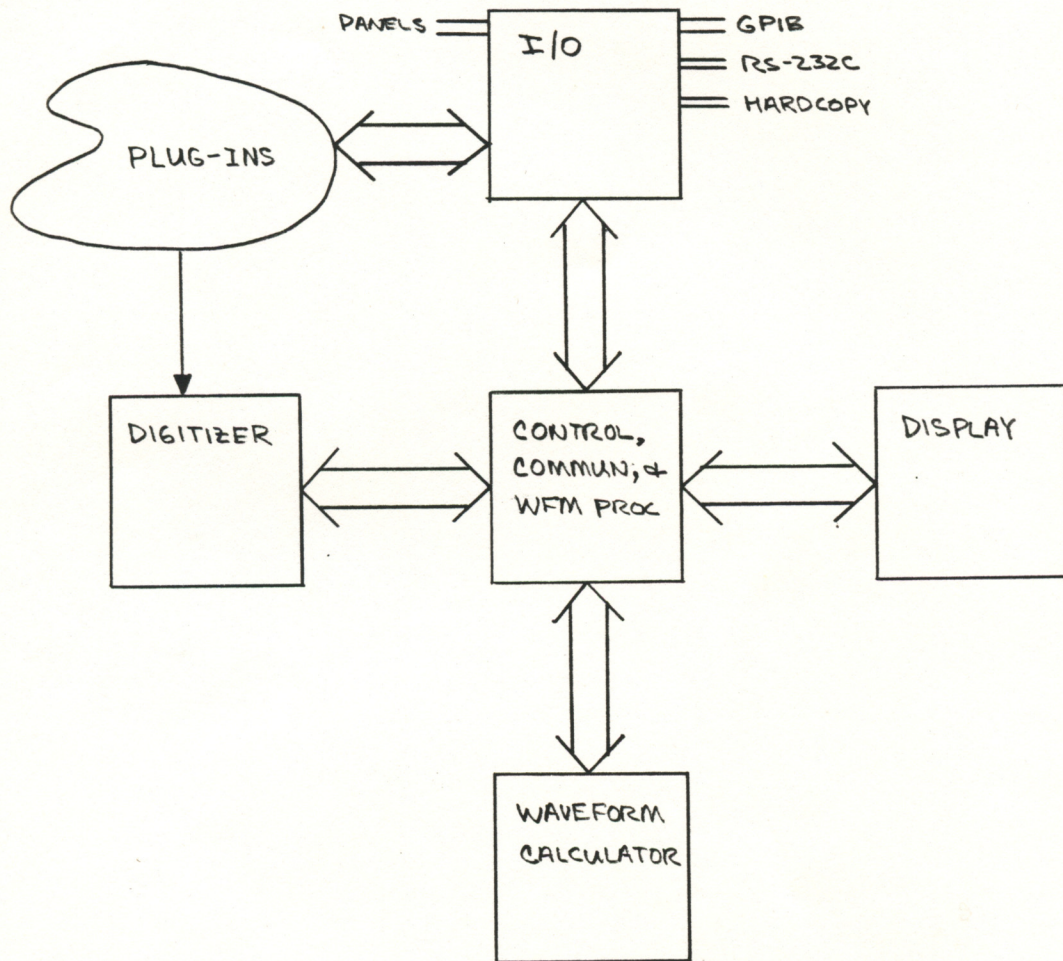
SHF III Quantizer
 Comparator
 Sampler Buffer

HMOS Custom Gate Arrays and IC's
 Digitizer Timebase and Control
 Display Vector Generator and Control

ITO Transparent Touch Keys

Color Shutter on high resolution raster display

Hybrids



PHILOSOPHY

COMPARISONS TO 7854

MAJOR CHARACTERISTICS

HUMAN INTERFACE EXAMPLE

DESIGN CONCEPTS

WE WANT...

**TO MAKE THE WORLD'S BEST VALUED LABORATORY
GRADE OSCILLOSCOPES FOR GENERAL WAVEFORM
MEASUREMENTS.**

TO THAT END...

**WE WILL PROVIDE FEATURES WHICH CLEARLY AND
DIRECTLY ENHANCE WAVEFORM MEASUREMENTS:**

- INCREASE MEASUREMENT ACCURACY**
- REDUCE INSTRUMENT IMPOSED COMPLEXITIES.**

ATTRIBUTE	7854	ET
WAVEFORM ACQUISITION	Integral A/D 250KS/s, 10 bit ET BW 475 MHz Linear Ramp TB	Modular A/D 20MS/s, 10 bit ET BW 475MHz Digital TB
DIGITAL STORAGE	5120 points, max 1024 pt, max rec	10,001 points, max 10,001 pt, max rec
MEASUREMENTS/ PROCESSING	Waveform Parameters Waveform Calculator	Waveform Parameters Waveform Calculator Extended Functions (via ROM Paks, I/O)

ATTRIBUTE	7854	ET
DISPLAY	Analog, DC-400MHz Digital (from memory only) Text 40 char, 16 lin 5 inch diagonal	Digital (from memory or continuous acquire - emulates realtime display) Text 50 char, 27 lines 7.5 inch diagonal Color Option
ACCURACY	2%, Vert & Horiz	<0.5%, Vert 0.02% or 20ps max, Horiz
FUNCTIONAL PROGRAMABILITY	Vert & Horiz Modes (MF only; nothing in plug-ins)	All functions, including plug-ins
I/O PORTS	GPIB	GPIB RS-232C Hardcopy Expandable

<u>ATTRIBUTE</u>	<u>7854</u>	<u>ET</u>
EASE OF USE		Fewer Controls Auto-Scope Thoughtful Menus
SELF-CAL	No	DC Gains, Offsets
DIAGNOSTICS	Extensive - external Simple PUP Self-test	Extensive - internal Complete PUP Self-test (reports specific failures; allows override)
MODULARITY	Plug-ins Memory Waveform Calculator Power Supply	Plug-ins Memory Waveform Calculator ROM-Paks Digitizer Display I/O Ports Power Supply
PHYSICAL	Upright, Bench only	Low-Profile, Bench & Rack
COST	\$4500	\$3600

20MS/s, 10 bit, 2-stage flash converter

475MHz ET BW (300MHz @ probe tip)

Adjustable Record Length to 10,001 points

1001 Standard; Option up to 10,001

Accuracies < 0.5% Vert, 0.02% or 20ps Horiz

Signal Averaging and Envelope acquisition modes

Continuous Acquire or Roll modes, with acquire stop

Waveform Parameters

Min, Max, P-P, RMS, Mean, Risetime,
Falltime, Width, Freq, Period, Area,
Cursors.

Waveform Calculator

Parameters
Functions (Diff, Intg, Interp, Smooth)
Operators (+, -, /, *, Sqrt, Log, Exp,
Abs, Sin, Cos)
Programming linked sequences of commands

*Opt ROMS
or
ROM Paks
Programming KB*

Extended Processing

FFT, Amplifier Error Correction, Hardcopy
Driver, Special Applications

*Opt ROMS
or
ROM Paks*

Display up to eight waveforms at one time

"Soft" key labeling

Text: ASCII and special Tek characters

50 characters per line, 27 lines

640 X 480 pixels

Electronic Graticule

Zooming, panning

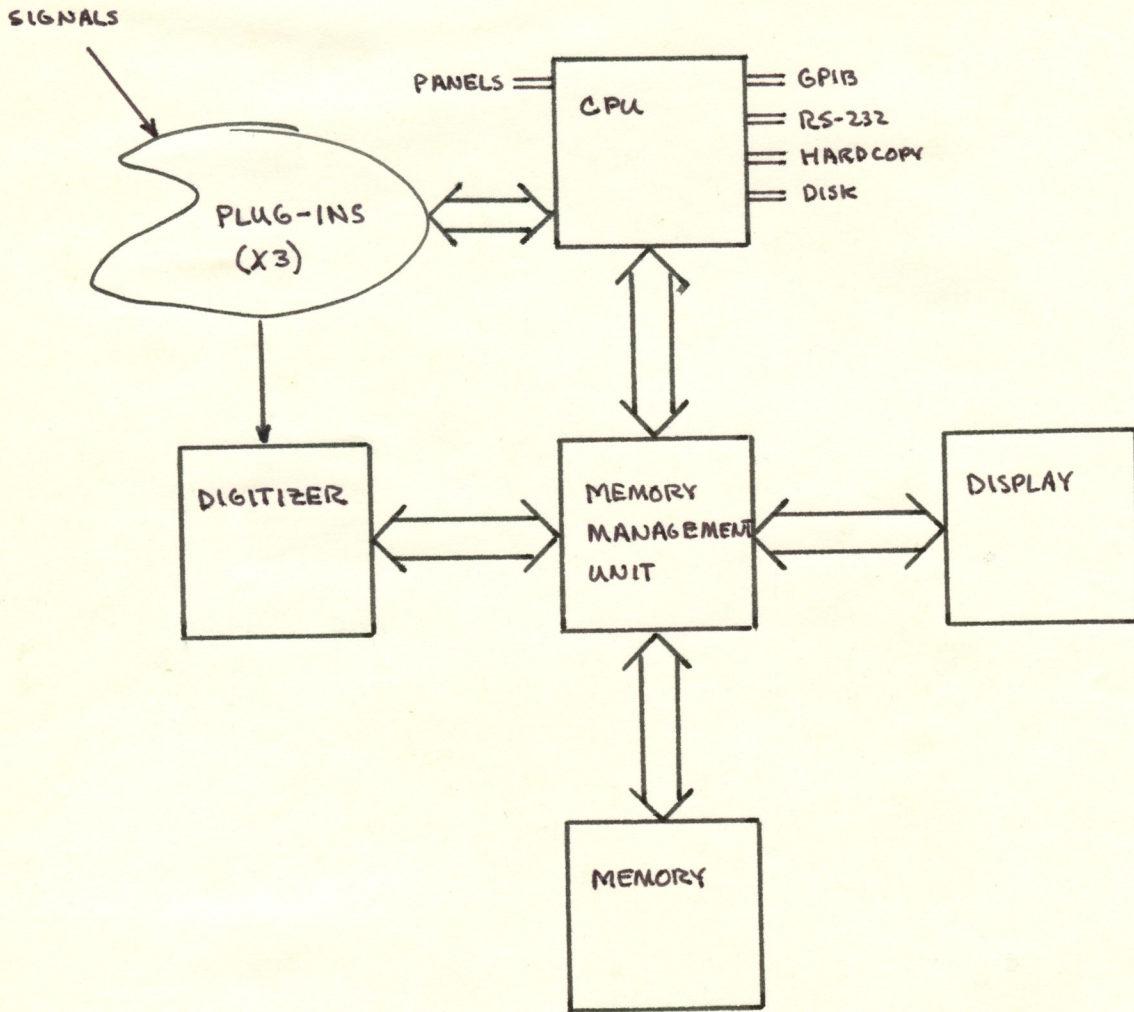
Auto-scaling of display

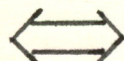

Continuous display of selected parameters

Color option (red, green, yellow) with shading

Normal and Reverse video

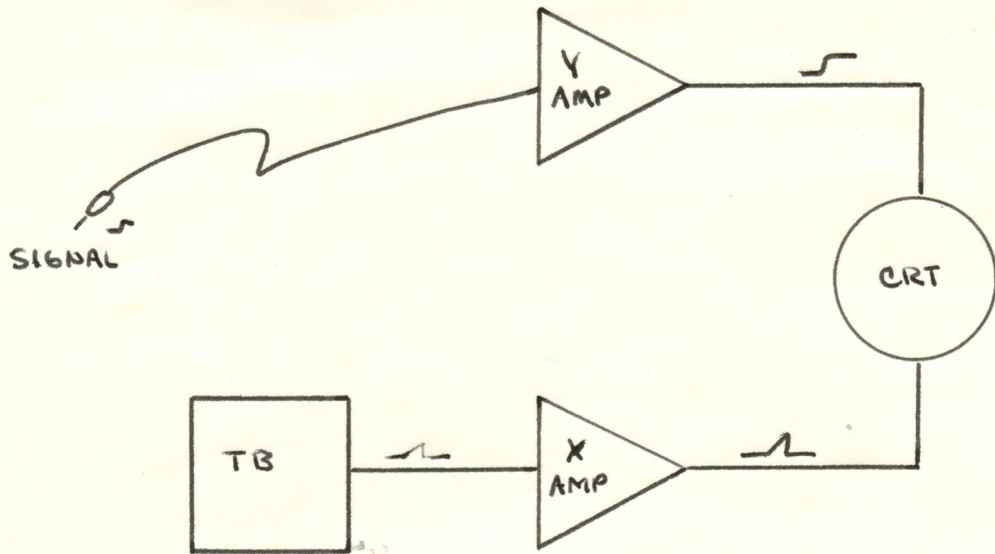
Interactive Display



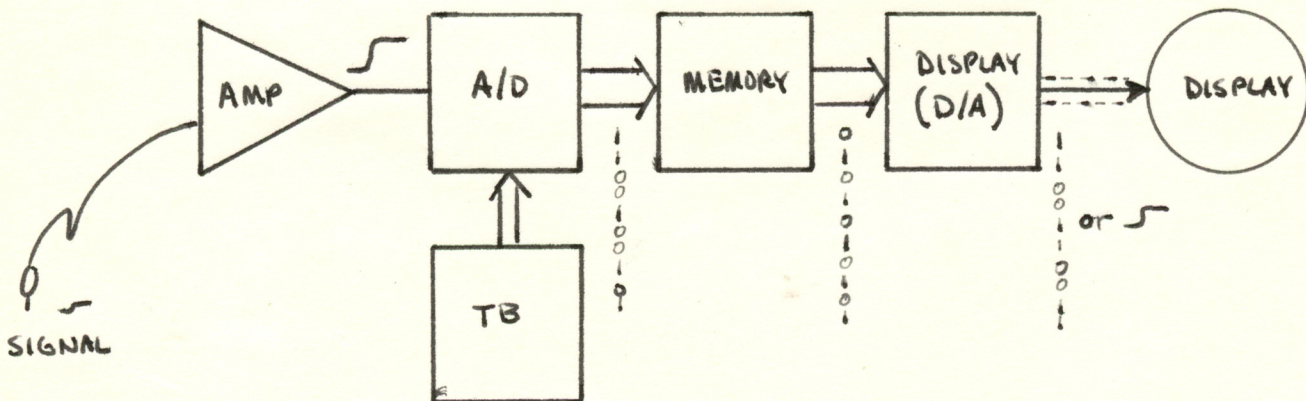
 DIGITAL
 ANALOG

18 Oct 83
TR

ANALOG SCOPE:



DIGITAL SCOPE:



INTRODUCTION

DIGITAL SCOPES

ET PROGRAM

PROJECT DESCRIPTION

CRITICAL COMPONENTS

TR/hk (CPM/125/DOGNPONY)

INTRODUCTION

DIGITAL SCOPES

ET PROGRAM

PROJECT DESCRIPTION

CRITICAL COMPONENTS

QUESTIONS

DEVELOP SALABLE PRODUCTS

ET Mainframe (20 MS/s Digitizer)
100 MS/s Digitizer
Color Option
SW Applications

GET ET MAINFRAME TO MARKET BY AP 610

DEVELOP MODULAR ARCHITECTURE FOR DIGITAL SCOPES

UPGRADE 7K CAPABILITIES

Fully Programmable Hardware
Digital Data/Control Communications
Modular SW/FW
Simplified Human Interface

DEVELOP MODULAR ARCHITECTURE FOR 7K DIGITAL SCOPES

Design Flexibility
Manufacture Flexibility
Product Configuration Flexibility
SW and HW

IMPROVE AND EXTEND MEASUREMENT CAPABILITIES

Accuracy
Local Processing
Remote Control
SW Applications

SIMPLIFY THE HUMAN INTERFACE

Reduce Unnecessary Clutter
Friendly to the Neophyte
Effective for the Expert
Instrument should be Helpful

Transparent Touch Panel

Custom ICs

<i>SH3</i>	Quantizer Comparator Buffer/Multiplexer Time Interpolator
<i>HMOS</i>	Timebase Digitizer Control MMU Waveform Compressor
<i>NEC CMOS</i>	Vertical Raster Scan

Hybrids	Sampler Buffer/Multiplexer
----------------	-------------------------------

Color Shutter (Option)

R05



Cursors

Def Wfm

5.0349U



100mV /div

trig'd



4.0349U

-10ns

1ns/div

-060as

Vertical Desc	Horizontal Desc	Axes	Condition Acquisition	Vert Mag: Wfm
L+0	Main	Linear	Continuous	-----V/div
Impedance	Coupling	BW Limit	Page to	Remove Wfm 2
	@1024 pts		All Wfms Status	L+0 Main
				Chan Sel
				Calcd Wfm

FIRMWARE BUDGET

DIAGNOSTICS	16K
WAVEFORM PROCESSING	32K
CONTROL + COMMUNICATIONS	4K
DISPLAY	16K
I/O	20K
DIGITIZER	4K
AUTOSCOPE	4K
AUTO CAL	4K
	<hr/>
	100K

DEVELOPMENT SCHEDULE

PA	313
DC	409
ER	513
PSR	606

DEVELOPMENT COST

DC

\$1.5M

PSR

4.1M