Tektronix
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1220/1225/1230
LOGIC ANALYZER

PM403

6502, 65C02, 65C802 Microprocessor Probe

Operator's Manual

PM403
65XX DISASSEMBLY

*The PM403 has a software version number of 2.52.
For use with the PM403, the 1220 and 1225 Logic Analyzers require software versions of 2.5 or above; the 1230 Logic Analyzer requires a software version of 3.03 or above.*

Please check for change information at the back of this manual

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PM403
65XX DISASSEMBLY

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OVERVIEW

The PM403 6502/65C02/65C802 Microprocessor Probe Personality Module consists of a disassembly probe (with ribbon cables) and this user's manual. This manual shows you how to connect and use the PM403 disassembly probe with the 1220/1225/1230 Logic Analyzers. This manual does not teach you how to use analyzer keypads or menus. For information on using the logic analyzer refer to your logic analyzer operator's manual. For more information about the 6502/65C02/65C802 microprocessor, refer to your microprocessor data book.

The PM403 Version 2.52 firmware works with 1220/1225 Logic Analyzers having software version numbers 2.5 or higher and 1230 Logic Analyzers with software version numbers 3.03 or higher. If you're using a 1220/1225 version 2.5 or higher or a 1230 version 3.03 or higher, you must use the version 2.52 PM403. You can see what version of analyzer system software you are using by reading the opening menu when you turn the unit on.

The PM403 gives you an interface between the 1220/1225/1230 Logic Analyzer and 6502/65C02/65C802-based systems under test (SUT). Along with regular analyzer features, the PM403 interface lets you sample data synchronously using the SUTclock, and display disassembly data in hardware and software formats.

Conventions. This manual uses these conventions:

- The term analyzer refers to the 1220, 1225, and 1230 Logic Analyzers unless otherwise specified.
- The term 65x refers to the 6502, 65C02, and 65C802 8-bit microprocessors.
- The term SUT refers to the 65x system under test.
- Active low signals are identified by a bar over the signal name, for example, $\overline{\text{NMI}}$.

ANALYZER CONFIGURATION

You must have at least 32 channels in the 1220/1225/1230 to use the PM403. This is because the probe uses 32 channels to acquire synchronous data from the 65x-based SUT. You must also use a version 2.52 PM403 if you're using a 1220/1225 version 2.5 or higher or a 1230 version 3.03 or higher. Figure 1 shows the analyzer and expansion card configuration.

CONNECTING AND POWERING UP

The PM403 has two probe cables that connect to the analyzer. Follow these steps to connect the PM403to the analyzer. Figures 1 and 2 show how the analyzer connects to your SUT.

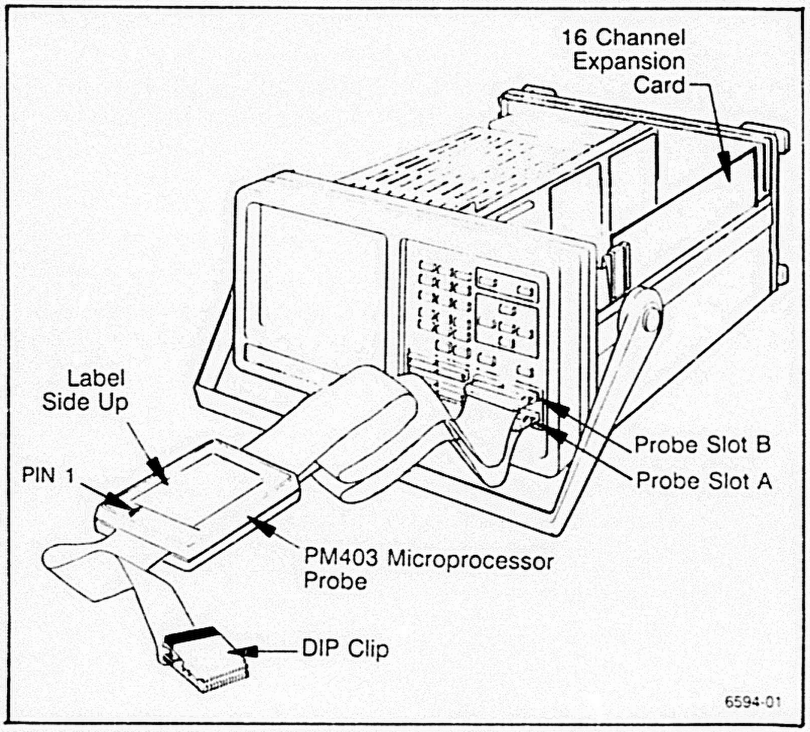


Figure 1. Analyzer configuration with PM403 probe. Note that the bottom cable plugs into probe slot A and the top cable plugs into probe slot B.

To connect the PM403 to your SUT, follow these steps:

1. Make sure that the power to the analyzer and SUT is off.

CAUTION

Do not connect the PM403 to the analyzer unless power to analyzer is off. Do not connect the PM403 disassembly probe to the SUT unless power to the SUT is off. If you connect the disassembly probe to the SUT when power to the SUT is on and power to the analyzer is off, too much power can flow through the probe's inputs and damage the probe.

2. With the PM403 label side up, connect the bottom cable from the probe to input A on the front of the analyzer.
3. Connect the top cable from the probe to input B on the front of the analyzer.

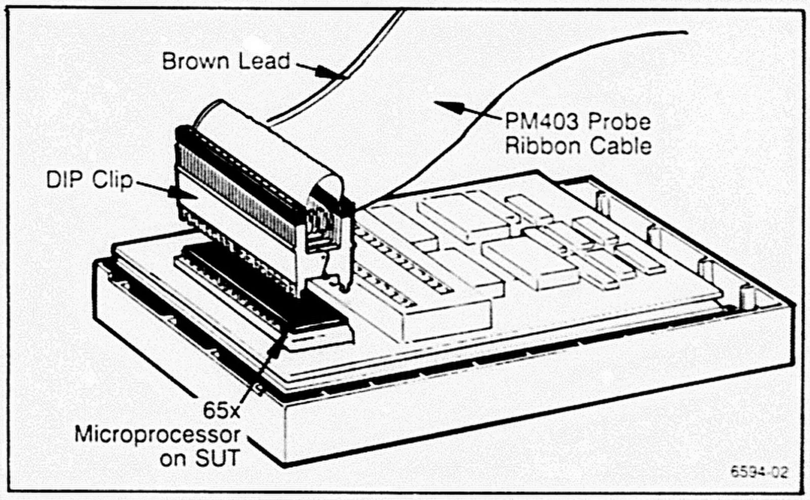


Figure 2. Connecting the DIP clip and SUT.

4. Connect the PM403 probe clip to the SUT as shown in Figure 2 (power to the SUT should be off). The brown lead labeled PIN 1 on the PM403 goes to pin 1 on the 65x microprocessor. Figure 3 shows the 65x pinout, and Table 1 lists analyzer-to-65x signal line connections. Figure 3 and Table 1 are shown after this procedure.

5. Turn on the analyzer which also supplies power to the probe. The analyzer screen now displays the Initialization menu (Figure 4, shown after this procedure).

6. Press ENTER to upload the PM403 disassembly setup into the analyzer. Pressing ENTER overwrites the existing setup and changes probe links, channel groups, and defined conditions for 65x disassembly. If you press MENU, the PM403 setup is not uploaded and the analyzer's current setup is saved.

7. Turn on power to the SUT.

At this point the analyzer displays the Main menu (Figure 5), which lists setup, data, and utility menus. Since the default disassembly setup defines the setup parameters for you (probe links, sampling rate and format, conditions, and so on), you can press START at any time to acquire data from your SUT. Example 1, later in this manual, shows a data acquisition with the default setup.

Signal Name	6502 Pin Numbers		Signal Name
Vss	1	40	$\overline{RES}$
RDY	2	39	OUT
OUT	3	38	$\overline{S0}$
$\overline{IRQ}$	4	37	IN
NC	5	36	NC
$\overline{NMI}$	6	35	NC
SYNC	7	34	R/$\overline{W}$
Vcc	8	33	D0
A0	9	32	D1
A1	10	31	D2
A2	11	30	D3
A3	12	29	D4
A4	13	28	D5
A5	14	27	D6
A6	15	26	D7
A7	16	25	A15
A8	17	24	A14
A9	18	23	A13
A10	19	22	A12
A11	20	21	Vss

6594-03

Figure 3. 6502 pinout.

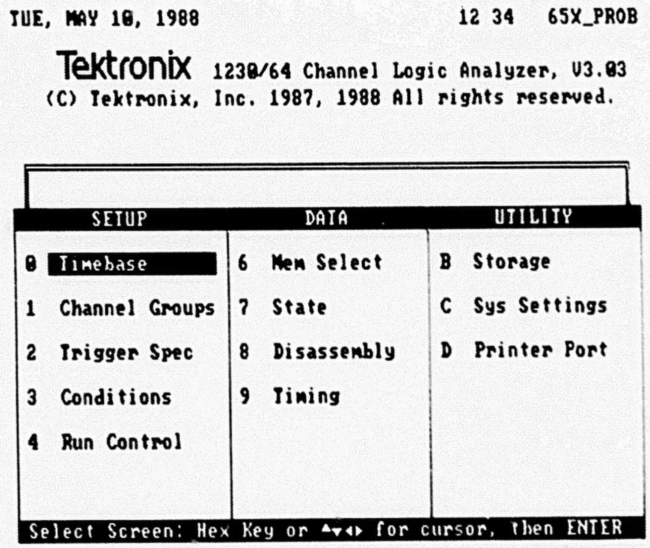
Table 1
65x Signals and Analyzer Channels

65x Signals	122x/1230 Channels	Channel Groups	Description
A15-A00	B15-B00	ADD	Address bus
D07-D00	A15-A08	DAT	Data bus
SYNC R/$\overline{W}$	A01 A00	STB	Strobes
$\overline{NMI}$ $\overline{IRQ}$ RESET	A03 A02 A05	INT	Interrupts

```
TUE, MAY 10, 1988                              12:32   -DEFAULT

Tektronix 1230/64 Channel Logic Analyzer, V3.03
(C) Tektronix, Inc. 1987, 1988 All rights reserved.

    Use the NOTES key whenever information is needed,
            or consult the Operator's Manual.

           X represents DON'T CARE condition.

          OK to load setup from Personality Module?
        (Overwrites current setup and System Links!)
           Press ENTER to confirm, MENU to abort

           Press ENTER to confirm, MENU to abort.
```

6594-04

Figure 4. Initialization menu. When you turn the analyzer on with the PM403 plugged in, the Intialization menu includes a message telling you that you can now upload the disassembly setup by pressing ENTER.



6594-05

Figure 5. Main menu. The Main menu always shows disassembly as a menu selection. However, you can display acquired data in disassembly format only when the PM403 is plugged in. As long as the channel groups are in the default definitions and the acquisition memory is valid, you can display valid disassembly data.

Loading Disassembly Setups. You don't have to upload the disassembly setup when you see the Initialization menu. However, if you don't, you must enter the disassembly setup manually or reset the analyzer so that the PM403 can upload the disassembly setup for you. You can reset the analyzer by pressing NOTES and ENTER firmly at the same time.

Using Probes

The PM403 must always be plugged into slots A and B on the analyzer front panel. If you have a 1220/12255 Logic Analyzer, you can use slot C for an acquisition probe. If you have a 1230 Logic Analyzer, you can use slots C and D for acquisition probes.

You may use an acquisition probe as well as the disassembly probe. The acquisition and disassembly probes may be used together or separately without unplugging either. You can always run the trigger specification on either timebase.

The probe cable in slot A must always be connected to the clock in your SUT. If the probe in slot A is not connected to your SUT clock, the analyzer won't trigger when you press START. If you're using more than one probe and the probes are linked synchronously, each probe must be connected to the same clock point in your SUT.

Using the Menus and Cursor

The PM403 is controlled by selections you make in the analyzer's menus. You can always call up the Main menu by pressing MENU.

You don't have to specify the 65x when you select disassembly information from the Main menu. The analyzer looks at the probe inputs to find out that the PM403 is connected. For more information about using the menus and cursor, refer to your logic analyzer operator's manual.

Online Help

At the bottom of the disassembly screen, a one-line help message tells you which keys to press for disassembly functions. If you need more help, press NOTES while the disassembly screen is displayed. The analyzer then displays five pages of in-depth information about 65x disassembly, including the disassembler's software version number, which appears on the first page of disassembly notes. You can press MENU at any time to exit the notes and return to the previous display.

SETTING UP TO ACQUIRE DATA

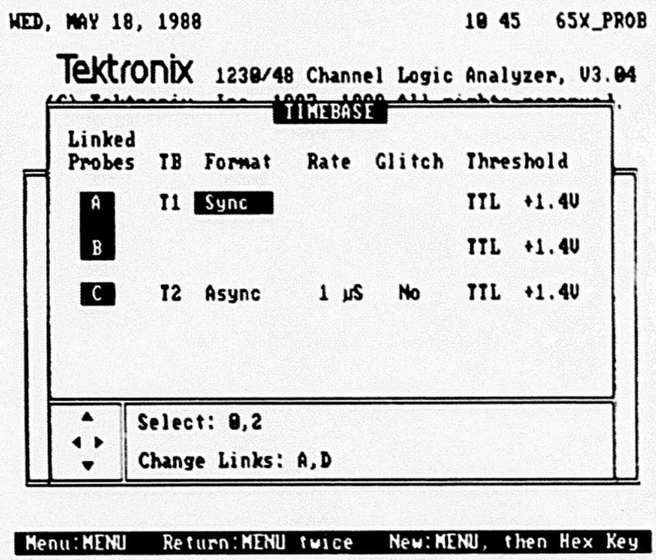
This discussion shows you how the PM403 sets up the analyzer for 65x disassembly. The setups shown here are for an analyzer with 32 channels. Example 1, later in this manual, shows a data acquisition using this 32-channel default setup.

A setup is a set of parameters that describes the current analyzer configuration for data acquisition and storage. For example, the setup includes information about probe links, acquisition rates, glitch capture, threshold voltage, and 65x trigger conditions.

You may use the setup as it is uploaded from the PM403, or you may change any part of the configuration. While the discussion in this section is about the default PM403 setup, you are free to change any part of the analyzer configuration manually.

Timebase

The acquisition timebase, probe links, glitch capture, and threshold voltage for 65x disassembly are shown in Figure 6. If you're using a 1230, the PM403 uses the synchronous clock rate of your SUT. If you're using a 1220 or 1225, the PM403 is set up for synchronous acquisition at 100 ns or slower.



6594-06

Figure 6. Timebase menu. Probes A and B must be linked synchronously for correct disassembly.

Probe Links. The PM403 is a 32-channel disassembly probe which uses probe slots A and B. For 65x disassembly, probes A and B are linked together synchronously in timebase T1 so that all disassembly is done with the same acquisition format and rate. If you're also using one or more acquisition probes in addition to the PM403, the acquisition probes are linked asynchronously in T2.

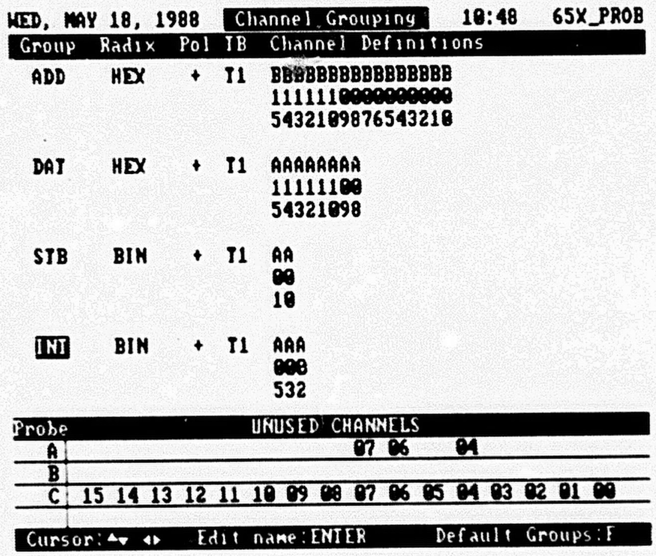
Clocking. The default disassembly clock format is synchronous so that you use the clock rate in your SUT as the data sampling rate. The PM403 automatically qualifies your SUT clock with software internal to the probe. There are no external clock qualifiers for the 65x disassembly probe.

For the 1230, the clock rate is set by your SUT. For the 1220/1225, the clock rate is set to $\leqslant$100 ns by default. For 65x disassembly, you must use a clock rate of $\geqslant$100 ns if you're using a 1220/1225.

Glitch Capture. The PM403 does not acquire glitches. When you turn glitch capture on, the upper eight channels are deleted from each channel group. Because the PM403 is a 32-channel probe, if you turned glitch capture on for disassembly, the analyzer would not be able to complete a legal acquisition.

Channel Grouping

The PM403 sets up the analyzer's channel groups as shown in Figure 7. The Channel Grouping menu shows how the channel groups are named; for example, ADD for the address bus. The control lines are separated into two channel groups: strobe lines and interrupt lines. Channels that are assigned to the asynchronous timebase (T2) are in the unused list. If you want to use those channels, you must manually add them to a group. The screen is large enough to see only four groups. To see more groups, scroll up or down the screen.



6594-07

Figure 7. Channel Grouping menu. The screen size allows for viewing of only four channel groups. To see more channel groups, scroll up or down the screen.

Trigger Conditions

The Conditions menu lets you define data conditions which the analyzer can recognize and trigger on. When you upload the 65x setup, the 65x input signals are already grouped for you to correspond to the analyzer channels as listed earlier in Table 1. The conditions listed in Table 2 show the logic states corresponding to 65x operations.

Table 2
65x Cycle Types and Analyzer Conditions

Signal Line	ADD hex	DAT hex	STB bin	INT bin
OPC FET	XXXX	XX	11	XXX
MEM READ	XXXX	XX	01	XXX
MEM WRIT	XXXX	XX	00	XXX
RESET	XXXX	XX	XX	0XX
NMI	XXXX	XX	XX	X0X
IRQ	XXXX	XX	XX	XX0

All signals are sampled synchronously with a 65x machine cycle, except for $\overline{\text{NMI}}$ (nonmaskable interrupt). $\overline{\text{NMI}}$ is displayed only at the negative edge for one cycle.

Figure 8 shows the Conditions and Trigger Spec menus. The trigger statement shown in the figure is for a 1230. If you're using a 1220/1225, the default trigger action is START instead of TRIG.

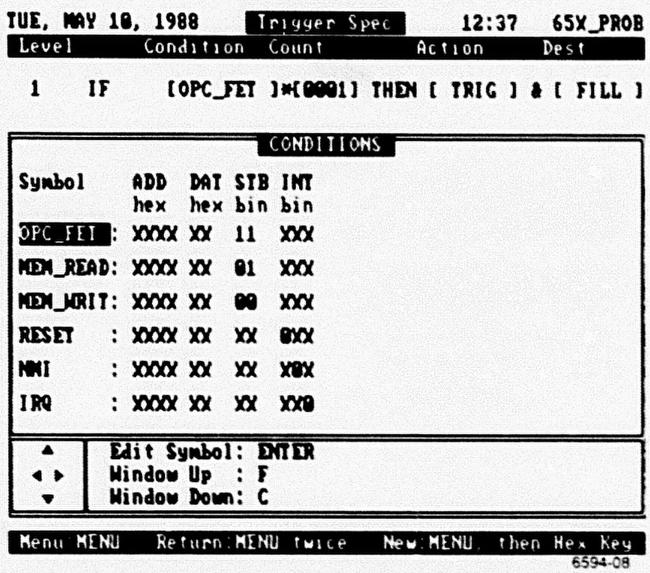


Figure 8. Conditions and Trigger Spec menus. The default condition window is large enough to show the six defined conditions. Table 2 lists all signals/conditions defined for the PM403. The default trigger statement is an "if then" statement with the first condition, OPC FET, as the trigger condition. For the 1230, the trigger action is TRIG. For the 1220/1225, the trigger action is START.

Trigger Specification

The default trigger statement is an "if then" statement. At initialization, the analyzer is set to trigger and fill memory when the condition OPC FET occurs. Figure 8 shows the Trigger Spec menu along with the Conditions menu.

Run Control

When you load the 65x setup, the Run Control menu is set up as shown in Figure 9. The default display for acquired data is a disassembly display. The trigger position is set at memory location 1024, and the analyzer looks for the trigger after the pretrigger memory is full.

The Run Control menu also sets the memory-compare mode to Manual and tells you that the default channel mask for comparing memories is OPC FET, which is also the default trigger condition. A window (or viewport) at the bottom of the screen lists the value for OPC FET. Remember that channels set to X (don't care) are masked, or not compared, during a memory comparison.

```
TUE, MAY 10, 1988      Run Control      12:37   65X_PROB

 Update Memory    : [1]       Display: [Disassembly]
 Trigger Position: [1024]     0 [         ]  2K
 Look for Trigger: [After Pre-Trigger Memory Full]
 ===================================================
 Compare          : [Manual]
 Compare Memory 1 to Memory: [2]


 Compare Mem Locations: [0000] to [1792]
 Use Channel Mask     : [OPC_FET ]
 Display Data at least: [9] seconds
 ---------------------------------------------------
 |          ADD  DAT STB INT                        |
 |Symbol    hex  hex bin bin                        |
 |OPC_FET : XXXX XX  11  XXX                        |
 ---------------------------------------------------
 Cursor: ▲▼◄►      Select: 0,2
```

6594-09

Figure 9. Run Control menu. The defaults in this menu include the display format set to disassembly and the trigger position set to 1024.

SETTING UP TO DISASSEMBLE CODE

Once you've set up the analyzer for disassembly, you can start to acquire and display data from your SUT. Your logic analyzer operator's manual tells how to display data in state and timing formats. This discussion shows you how to display disassembled 65x data, which you can do only when the PM403 is connected to the analyzer.

As long as the acquisition memory is valid and the channel groups are set to the default 65x setup definitions, the disassembly display is also valid. Channel grouping is only used for the timing and state displays.

Disassembly Mnemonics. The PM403 lets you display acquired data in disassembly mnemonics. Disassembly mnemonics are assembly-language instructions that have been disassembled from a machine language program. For example, 65x disassembly mnemonics include JMP, CMP, NOP, and DEC instructions. An actual disassembly line might read STA A1, which means "store the accumulator in memory location A1." Figure 10 shows an example of disassembly mnemonics.

TUE, MAY 10, 1988 Disasm Memory 1 12:41 65X_PROB

Loc	Addr	Data	65C02 Disassembly		Operation	Status
0038	D9AD	AD			MEM READ	
0039	D9A6	AD	LDA	3F14	OPC FETCH	
0040	D9A7	14			MEM READ	
0041	D9A8	3F			MEM READ	
0042	3F14	B1			MEM READ	
0043	D9A9	29	AND	#40	OPC FETCH	
0044	D9AA	40			MEM READ	
0045	D9AB	F0	BEQ	D9A6	OPC FETCH	
0046	D9AC	F9			MEM READ	
0047	D9AD	AD			MEM READ	
0048	D9A6	AD	LDA	3F14	OPC FETCH	
0049	D9A7	14			MEM READ	
0050	D9A8	3F			MEM READ	
0051	3F14	B1			MEM READ	
0052	D9A9	29	AND	#40	OPC FETCH	
0053	D9AA	40			MEM READ	
0054	D9AB	F0	BEQ	D9A6	OPC FETCH	
0055	D9AC	F9			MEM READ	
0056	D9AD	AD			MEM READ	
0057	D9A6	AD	LDA	3F14	OPC FETCH	

Func:F Scroll Rate: 7,8 [20] Mode: X [Hardware]

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Figure 10. Disassembly mnemonics in hardware mode. All bus operations and acquired cycles are displayed. A software display that corresponds to this figure is shown later in Figure 12, later in this manual.

Displaying in Hardware or Software Mode. With the PM403 attached, you can display disassembled data in hardware or software mode. In hardware display mode, the analyzer shows all bus operations and displays every acquired cycle. In software display mode, the analyzer shows only instructions; reads and writes are suppressed so that the display looks like an assembly listing. You can toggle between display modes by pressing DON'T CARE.

Error Conditions. The analyzer will display ?SYNC WR? when both the SYNC and the WRITE lines are high. Figure 11 shows this microprocessor error condition in disassembly information. Since software mode only displays valid opcodes, error conditions are not displayed in software mode.

```
WED, MAY 11, 1988  Disasm  Memory 1   10 43   65X_PROB
 Loc   Addr Data 65C02 Disassembly  Operation  Status
-1176--0002-00---------------------MEM READ---RST-----
 1177  0009 00   BRK               OPC FETCH  RST
 1178  000B 00   BRK               OPC FETCH  RST
 1179  000D 00   BRK               OPC FETCH  RST
 1180  0003 00   BRK               OPC FETCH  RST
 1181  0009 00   BRK               OPC FETCH  RST
 1182  000B 00                     MEM WRITE  RST
 1183  000D 00   BRK               OPC FETCH  RST
 1184  0004 00                     MEM READ   RST
 1185  0009 00   BRK               OPC FETCH  RST
 1186  000B 00                     ?SYNC WR?  RST
 1187  000D 00                     MEM WRITE  RST
 1188  0005 00   BRK               OPC FETCH  RST
 1189  0009 00   BRK               OPC FETCH  RST
 1190  000B 00                     MEM WRITE  RST
 1191  000D 00   BRK               OPC FETCH  RST
 1192  0006 00                     MEM READ   RST
 1193  0009 00   BRK               OPC FETCH  RST
 1194  000B 00   BRK               OPC FETCH  RST
 1195  000D 00                     MEM WRITE  RST
 Func:F      Scroll Rate: 7,8 [18]     Mode: X [Hardware]
```

6594-11

Figure 11. Microprocessor error condition displayed in hardware mode. A microprocessor error is shown as ?SYNC WR? in location 1186. Since software mode only displays opcodes, error conditions are not displayed in software mode.

Searching for Events. Searching for events in the Disassembly menu works the same as searching for events in the State Table. Press 0 or 2 to cycle through the available conditions (including the beginning and end of acquisition and the trigger event). Press 1 to perform the search.

When the analyzer finds the search event, it redisplays the disassembly screen so that the cursor is positioned in the middle of the screen indicating the search event. If you searched for an event that did not occur, the analyzer displays the message Not Found. One of the menu bars at the bottom of the screen lists the current search event. For more information about searching, refer to your logic analyzer operator's manual.

The analyzer can display and search for opcode fetches in software mode. However, since reads and writes (which are not opcode fetches) are suppressed in software mode, the analyzer cannot display those instructions if you try to search for them. If you're using software mode and search for an event that is not an opcode fetch, the analyzer sets the cursor to the previous opcode fetch and displays the instruction where the previous valid search event occurred.

Change Processor. Because some opcodes work differently on a 65C802 than on a 65C02, press C to toggle between the two processors. The 6502 will be correctly disassembled using either choices. Refer to your processor data sheets for more information about the specific processor you're using.

Using the Hardware Display Mode

For disassembly displays in hardware mode, the analyzer displays each sample location with address and data from the 65x bus cycle. Disassembled instructions are displayed at the beginning of each valid machine cycle. Figure 10, earlier in this discussion, shows a hardware disassembly display.

In the displays, the Loc column shows memory locations. The Addr column shows the address, while the Data column displays acquired data. When the PM403 recognizes the beginning of an instruction, the analyzer disassembles that instruction and displays it in the middle column.

The Operation column displays the decoded cycle types OPC FETCH, MEM READ, and MEM WRITE. Applicable bus operations are displayed in the order they occur; for example, an OPC READ and then a MEM WRITE.

The last column displays the status of interrupt lines. In the Status and Operation columns, the interrupt with the highest priority is listed. For example, if an $\overline{\text{NMI}}$ and $\overline{\text{IRQ}}$ occur at the same time, the $\overline{\text{NMI}}$ signal is listed in the display. Table 3 lists interrupt priorities.

Table 3
Active Interrupt Priorities

Active Line	Description
$\overline{\text{RES}}$	Reset
$\overline{\text{NMI}}$	Nonmaskable interrupt
$\overline{\text{IRQ}}$	Interrupt request

Pressing DON'T CARE while in the hardware display mode toggles the disassembly screen to the software display mode, and vice versa.

Using the Software Display Mode

The software display mode is useful because it displays only instructions – memory reads and writes are suppressed. The display resembles an assembly or program listing because it shows only one opcode fetch per line and each line must be the start of an instruction sequence. Because of this, the locations displayed are not contiguous. Figure 12 shows a software disassembly display.

```
TUE, MAY 10, 1988  Disasm:  Memory 1   12 41   65X_PROB
Loc   Addr Data           65C02/  Disassembly  Operation

0018  D9AB F0F9           BEQ     D9A6
0021  D9A6 AD143F         LDA     3F14         3F14=B1
0025  D9A9 2940           AND     #40
0027  D9AB F0F9           BEQ     D9A6
0030  D9A6 AD143F         LDA     3F14         3F14=B1
0034  D9A9 2940           AND     #40
0036  D9AB F0F9           BEQ     D9A6
0039  D9A6 AD143F         LDA     3F14         3F14=B1
0043  D9A9 2940           AND     #40
0045  D9AB F0F9           BEQ     D9A6
0048  D9A6 AD143F         LDA     3F14         3F14=B1
0052  D9A9 2940           AND     #40
0054  D9AB F0F9           BEQ     D9A6
0057  D9A6 AD143F         LDA     3F14         3F14=B1
0061  D9A9 2940           AND     #40
0063  D9AB F0F9           BEQ     D9A6
0066  D9A6 AD143F         LDA     3F14         3F14=B1
0070  D9A9 2940           AND     #40
0072  D9AB F0F9           BEQ     D9A6
0075  D9A6 AD143F         LDA     3F14         3F14=B1
Func:F     Scroll Rate: 7,8 [20]     Mode: X [Software]
```

6594-12

Figure 12. Software disassembly display. Reads and writes are suppressed so this display looks like an assembly listing. This display corresponds to the hardware disassembly shown in Figure 10. Press DON'T CARE to toggle between software and hardware display modes.

The Data column displays bytes that make up the opcode and also displays any data fetches for the instruction. The Operation column lists the bus operations for the instruction sequence. For each instruction cycle, the analyzer uses the Operation column to tell you the memory address and data activity for that cycle. In this column, the address is displayed on the left of the equals sign; data is displayed on the right. Figure 14 under *Examples* shows address and data information.

Searching for Events. You can search for events in the software disassembly display the same as you search for events in the State Table. However, because memory reads and writes are suppressed, if you search for an event that occurs on a memory read or write cycle, the analyzer will display the instruction that caused the memory read or memory write. To search for a memory read or write cycle, press DON'T CARE to toggle to hardware mode, select the search event, and then press 1 to search.

When you press DON'T CARE to switch display modes, the analyzer goes through memory to find the opcode fetch closest to the cursor position. When it finds the opcode fetch, the analyzer displays the disassembly in software mode with the cursor in the middle of the screen. If it can't find an opcode fetch, the analyzer returns to hardware mode.

EXAMPLES

These three examples show you how to acquire data for disassembly, display the data in hardware and software modes, and cross-trigger the disassembly probe from a different timebase (using an acquisition probe).

The first example uses the default setup for a simple acquisition. In the second example, you define specific conditions on which you want to trigger. The third example uses 36 channels to cross-trigger the PM403 from the acquistion probe using a different timebase than the disassembly probe.

Example 1. A Simple Acquisition

This example uses the default 65x setup uploaded when you connected the analyzer to a SUT and initialized the analyzer. This example shows you how to:

- acquire and disassemble data
- jump to a specific location
- search for a particular event
- toggle between display modes.

Follow these steps to make a simple acquisition and begin manipulating data.

1. Make sure the PM403 is connected to your SUT and the analyzer is initialized with the default disassembly setup.
2. Press START to acquire data. In the default setup, the analyzer will trigger on the first opcode fetch that occurs after the pre-trigger memory is full. The Acquisition Process screen is displayed, telling you the status of the acquisition. When the acquisition is complete, the analyzer stops and displays the data in disassembly since that is the default data format.

3. The information will automatically be displayed in disassembly format. Figure 13 shows the hardware display mode for the disassembly data. In hardware display mode, all bus operations and acquired cycles are displayed.

4. Press DON'T CARE to toggle to software display mode. In software display mode, only instructions are displayed.

   When you switch disassembly modes, the analyzer goes through memory to find the opcode fetch closest to the cursor. If it can't find an opcode fetch, it will return to hardware mode. Figure 14 shows the corresponding software display mode.

5. Press ENTER to tell the analyzer you want to enter a new location to be displayed, then enter 0000 to jump to the beginning of memory. As you finish entering the digits, the analyzer jumps to the selected memory address and displays the new information.

6. Press 0 or 2 to cycle through available search functions until you choose the trigger as the search event.

7. Press 1 to search for the trigger. Figures 13 and 14 show the trigger event in hardware and software modes.

The scroll rate, jump, and search features for disassembly displays work the same as they do in the State Table. For more information about these features, refer to your logic analyzer operator's manual.

```
TUE, MAY 10, 1988   Disasm:  Memory 1    12 47   65X_PROB
 Loc   Addr Data 65C02  Disassembly   Operation  Status
 1014  3F14 B1                        MEM READ
 1015  D9A9 29   AND    #40           OPC FETCH
 1016  D9AA 40                        MEM READ
 1017  D9AB F0   BEQ    D9A6          OPC FETCH
 1018  D9AC F9                        MEM READ
 1019  D9AD AD                        MEM READ
 1020  D9A6 AD   LDA    3F14          OPC FETCH
 1021  D9A7 14                        MEM READ
 1022  D9A8 3F                        MEM READ
 1023  3F14 B1                        MEM READ
-TRIG--D9A9-29---AND----#40-----------OPC FETCH---------
 1025  D9AA 40                        MEM READ
 1026  D9AB F0   BEQ    D9A6          OPC FETCH
 1027  D9AC F9                        MEM READ
 1028  D9AD AD                        MEM READ
 1029  D9A6 AD   LDA    3F14          OPC FETCH
 1030  D9A7 14                        MEM READ
 1031  D9A8 3F                        MEM READ
 1032  3F14 B1                        MEM READ
 1033  D9A9 29   AND    #40           OPC FETCH
 Func F    Search For: 0.2 [Trigger ]     Do Search: 1
```

6594-13

Figure 13. Hardware disassembly display. The search event in this example is the trigger event, which occurred at memory location 1024 as specified in the Run Control menu.

```
TUE, MAY 10, 1988   Disasm   Memory 1    12 48   65X_PROB
 Loc   Addr Data          65C02   Disassembly   Operation
 0993  D9A6 AD143F        LDA     3F14          3F14=B1
 0997  D9A9 2940          AND     #40
 0999  D9AB F0F9          BEQ     D9A6
 1002  D9A6 AD143F        LDA     3F14          3F14=B1
 1006  D9A9 2940          AND     #40
 1008  D9AB F0F9          BEQ     D9A6
 1011  D9A6 AD143F        LDA     3F14          3F14=B1
 1015  D9A9 2940          AND     #40
 1017  D9AB F0F9          BEQ     D9A6
 1020  D9A6 AD143F        LDA     3F14          3F14=B1
-TRIG--D9A9-2940----------AND-----#40---------------------
 1026  D9AB F0F9          BEQ     D9A6
 1029  D9A6 AD143F        LDA     3F14          3F14=B1
 1033  D9A9 2940          AND     #40
 1035  D9AB F0F9          BEQ     D9A6
 1038  D9A6 AD143F        LDA     3F14          3F14=B1
 1042  D9A9 2940          AND     #40
 1044  D9AB F0F9          BEQ     D9A6
 1047  D9A6 AD143F        LDA     3F14          3F14=B1
 1051  D9A9 2940          AND     #40
 Func F    Scroll Rate  7,8 [20]    Mode: X [Software]
```

6594-14

Figure 14. Corresponding Software disassembly. Because the search event was not a memory read or write, the software disassembly display (corresponding to the hardware display shown in Figure 14) shows the trigger event at the cursor. The Operation column shows the address (left side of equals sign) and data information for the instructions that occurred.

Example 2: Trigger on a Specific Event

This example shows you how to acquire specific data. In this example, a particular subroutine occurs a number of times in the program. You want to acquire only the subroutine. You need to define two conditions: the beginning of the subroutine and the end of the subroutine. The beginning of the subroutine is defined as JSR (jump to new location saving return address) and has a data value of 20_{hex}. The end of the subroutine is defined as RTS (return from subroutine) and has a data value of 60_{hex}.

In order to show an example of a multi-level acquisition, we'll have the analyzer acquire the subroutine, then loop back and acquire it again until we stop the acquisition manually.

This example uses the default setup except for defined conditions and trigger statements. You don't need to change the timebase, channel grouping, or run-control information from the default 32-channel setup for this example. Follow these steps to trace a subroutine and trigger on the subroutine.

1. In the Conditions menu, rename the G condition word to JSR and define it as DAT 20. Figure 15 shows the new JSR condition word definition: XXXX 20 XX XXX.

2. Rename the H condition word to RTS and define it as DAT 60. Figure 15 shows the new RTS condition word definition: XXXX 60 XX XXX.

3. In the Trigger Spec menu, define two levels of "if then" trigger statements as shown in Figure 15. When the analyzer finds 20_{hex} on the data line (the beginning of the subroutine) it starts to store data, then moves on to level 2. When the analyzer finds 60_{hex} on the data line (the end of the subroutine) it stops storing data, then loops back up to level 1 again to look for 20_{hex} again.

4. In the Run Control menu, the data display should default to Disassembly. Because you will halt the acquisition manually, the stop point will be in the trigger position. Change the Trigger Position to 1920 so that the stop point is near the end of memory allowing for more storage of data. Figure 16 shows the Run Control menu for this example.

5. Press START. At the first occurence of the subroutine, the analyzer starts storing the information, when the return is encountered, the storage stops and the analyzer loops back up to condition 1 to search for the next occurence of the JSR.

6. After a few seconds press STOP. The analyzer stops acquiring data and displays the acquisition in disassembly format. Figures 17 and 18 show the hardware and software disassembly for this example.

```
TUE, MAY 10, 1988     Trigger Spec        15 13   65X_PROB
 Level        Condition  Count          Action      Dest

  1    IF     [JSR       ]*[0001] THEN [STR ON] & [GOTO 2]

  2    IF     [RTS       ]*[0001] THEN [STROFF] & [GOTO 1]

  3

                        CONDITIONS
Symbol      ADD  DAT STB INT
            hex  hex bin bin
JSR      : XXXX 20   XX  XXX
RTS      : XXXX 60   XX  XXX

   ▲   Edit Symbol: ENTER
  ◄ ►  Window Up  : F
   ▼   Window Down: C

Menu:MENU    Return:MENU twice    New:MENU, then Hex Key
```

6594-15

Figure 15. Subroutine setup. The two new conditions define the beginning and end of the subroutine you're tracing. The two levels of trigger statements tell the analyzer to store everything between the beginning and end of the subroutine, and then loop back up to level 1 and search for the beginning of the next occurence of the same subroutine and store it again.

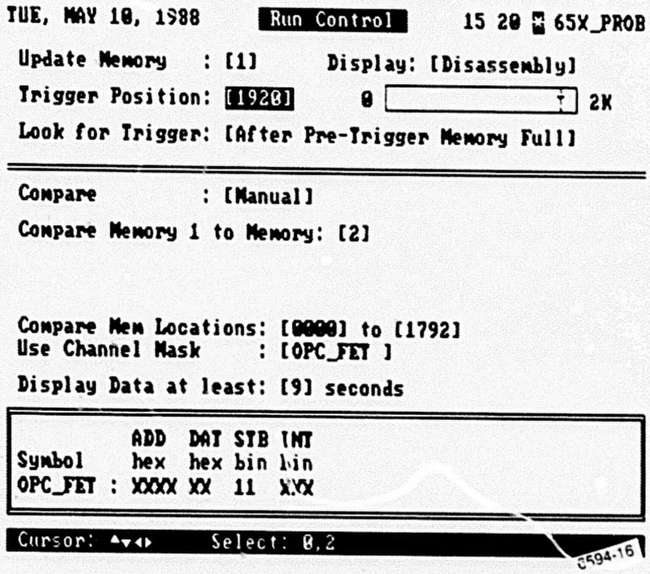
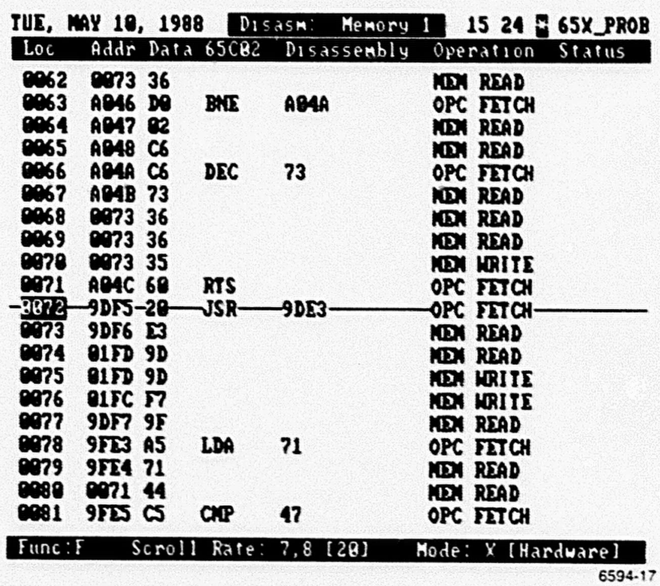


Figure 16. Run Control menu. The default display is set to Disassembly and the trigger position is changed to 1920.



Loc	Addr	Data	65C02	Disassembly	Operation	Status
0062	0073	36			MEM READ	
0063	A046	D0	BNE	A04A	OPC FETCH	
0064	A047	02			MEM READ	
0065	A048	C6			MEM READ	
0066	A04A	C6	DEC	73	OPC FETCH	
0067	A04B	73			MEM READ	
0068	0073	36			MEM READ	
0069	0073	36			MEM READ	
0070	0073	35			MEM WRITE	
0071	A04C	60	RTS		OPC FETCH	
0072	9DF5	20	JSR	9DE3	OPC FETCH	
0073	9DF6	E3			MEM READ	
0074	01FD	9D			MEM READ	
0075	01FD	9D			MEM WRITE	
0076	01FC	F7			MEM WRITE	
0077	9DF7	9F			MEM READ	
0078	9FE3	A5	LDA	71	OPC FETCH	
0079	9FE4	71			MEM READ	
0080	0071	44			MEM READ	
0081	9FE5	C5	CMP	47	OPC FETCH	

Figure 17. Hardware display with JSR condition. The cursor marks the search event, the beginning of the subroutine, which occurred at address 9DF5 (at analyzer location 0072). The hardware display mode shows each memory read and write that occurred during the subroutine.

```
TUE, MAY 10, 1988   Disasm:  Memory 1    15 24   65X_PROB
Loc   Addr Data          65C02   Disassembly   Operation
0034  A034 B002          BCS     A038
0037  A038 9270          STA     (70)          44CA=00
0042  A03A C66E          DEC     6E            006E=04
0047  A03C C66E          DEC     6E            006E=03
0052  A03E E670          INC     70            0070=CB
0057  A040 D002          BNE     A044
0060  A044 A573          LDA     73            0073=36
0063  A046 D002          BNE     A04A
0066  A04A C673          DEC     73            0073=35
0071  A04C 60            RTS
0072  9DF5 20E39D        JSR     9DE3          9DF7=9F
0078  9FE3 A571          LDA     71            0071=44
0081  9FE5 C547          CMP     47            0047=40
0084  9FE7 9008          BCC     9FF1
0086  9FE9 D00E          BNE     9FF9
0089  9FF9 A549          LDA     49            0049=47
0092  9FFB C571          CMP     71            0071=44
0095  9FFD 9008          BCC     A007
0097  9FFF D00C          BNE     A00D
0100  A00D A56E          LDA     6E            006E=03
Func:F    Scroll: ▼▲    Cursor: ◄►    Jump: ENTER
```

6594-18

Figure 18. Software display with JSR condition. You can show the search event, in software mode by pressing DON'T CARE. You can see the subroutine sequence in a more compact form in software mode since only one instruction is displayed for each bus operation.

Example 3: Cross-Triggering

If you're using a 1225 or 1230 Logic Analzyer, you can acquire data on 16-channel acquisition probe at the same time you use the PM403. You can also set the PM403to trigger off the timebase of the acquisition probe, or vice versa. This example shows you how to set up the PM403 to trigger off the acquisition probe.

Configuration. This example uses a 1225/1230 with 48 channels. The PM403 is still plugged into probe slots A and B. The 16-channel acquisition probe (P6443 or P6444) is plugged into probe slot C.

What This Example Shows. This example shows how to set up an acquisition probe to trigger on a condition, then set up the disassembly probe to automatically cross-trigger and show the acquired information in disassembly display. In this example, you want to know what will happen to your code when you trigger the acquisition probe on a particular event.

The analyzer then automatically cross-triggers the disassembly probe so that you can display the disassembly data for that acquisition.

Figures 19 through 23 show the setup menus for this example. The menus show how to set up the 1225/1230 with these parameters:

- Probes A and B are in T1; probe C is in T2.
- Channel group GPE is renamed to TST and contains 8 channels from probe C.
- The trigger condition GET is defined for the specific event upon which you wish to trigger.
- The trigger timebase is T2 (the acquisition probe) so that the 1225/1230 recognizes the trigger condition GET and automatically cross-triggers the disassembly probe when GET occurs.

The Steps for Cross-Triggering. Follow these steps to cross-trigger the PM403 off the acquisition probe and search for the trigger event in the resulting disassembly display.

1. In the Timebase menu, link probes A and B in timebase T1 (separately from probe C, which should be in T2). Refer to Figure 19.
2. In the Channel Grouping menu, scroll to channel group GPE and change the channel group name to TST. Add channels C07-C00 to this new group. Refer to Figure 20.
3. In the Conditions menu, define a condition GET to the value A6hex in group TST. Figure 21 shows the Trigger Spec menu and the value of the trigger condition GET.
4. In the Trigger Spec menu, set the trigger condition to GET Figure 21 shows the Trigger Spec menu.
5. Look at the menu bar at the bottom of the Trigger Spec menu, and press D to toggle the trigger timebase to T2. Refer to Figure 21.
6. In the Run Control menu, make sure the 1225/1230 looks for the trigger GET after the pretrigger memory is full. The default data display format should still be set to Disassembly. Refer to Figure 22.

7. Press START. The 1225/1230 acquires data until the trigger condition is encountred. Then the analyzer triggers all modules, fills memory, and stops. The disassembly screen is displayed. Figure 23 shows a sample disassembly display.

8. Press 0 or 2 to cycle through available search events until you select Trigger, then press 1 to locate the trigger. Figure 23 shows the trigger event in a hardware disassembly display.

9. In order to view the data from the acquisition probe, you must change the timebase. Go to the State display and you'll see the disassembly information in state format. Press F until you see the Timebase: field. Press 9 to change to Timebase T2. The State display will now show the data that was acquired on the acquisition probe.

Once you've made the acquisition, you can call up state, disassembly, and timing displays for the acquired data. Since you used two timebases to make the acquisition, you must change pages to display what happened in T2 on the acquisition probe, and then what happened in T1 on the disassembly probe.

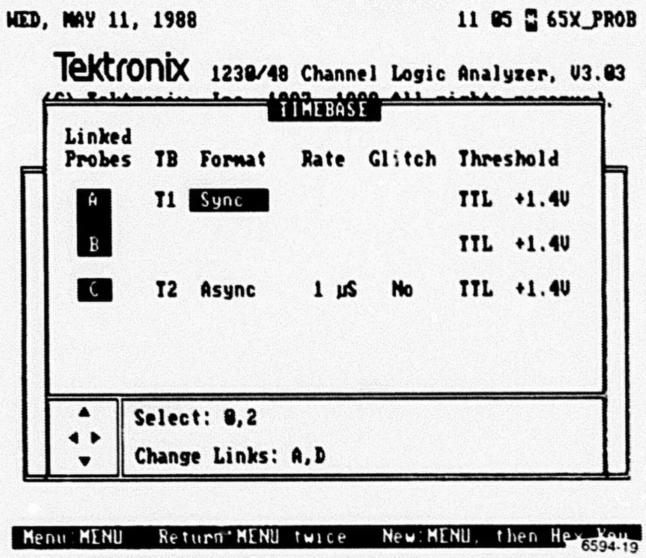


Figure 19. Timebase for cross-trigger. Probes A and B (the PM403) are linked in T1, and probe C (the acquisition probe) is in T2. This lets you acquire data with different timebases.

```
WED, MAY 11, 1988   Channel Grouping   11:02   65X_PROB
Group  Radix  Pol  TB  Channel Definitions
ADD    HEX    +    T1  BBBBBBBBBBBBBBBB
                       1111110000000000
                       5432109876543210

DAT    HEX    +    T1  AAAAAAAA
                       11111100
                       54321098

STB    BIN    +    T1  AA
                       00
                       10

INT    BIN    +    T1  AAA
                       000
                       532

TST    HEX    +    T2  CCCCCCCC
                       00000000
                       76543210

OPT    HEX
```

6594-20

Figure 20. Channel Grouping for cross-trigger. The analyzer screen shows only four channel groups at a time. This figure is a modification of two combined screens so you can see all six channel group definitions. The channel group shows that the fifth channel group is renamed to TST and contains 8 channels for the acquisition probe (timebase T2).

```
THU, MAY 19, 1988    Trigger Spec       09:43 ▪ 65X_PROB
Level        Condition  Count         Action      Dest

1    IF      [GET      ]*[0001] THEN [ TRIG ] & [ FILL ]

2

3

4

5

CONDITION:
          ADD   DAT  STB  INT  TST
Symbol    hex   hex  bin  bin  hex
GET      :X0XX  XX   XX   XXX  A6

Cur:▲▼◄► Sel:0,2 Instr:ENTER TrigTB:D[T2] Advanced:1
```

6594-21

Figure 21. Conditions and Trigger Spec for cross-trigger. The trigger condition GET is defined as A6hex. The menu bar at the bottom of the Trigger Spec screen shows that the trigger timebase is T2.

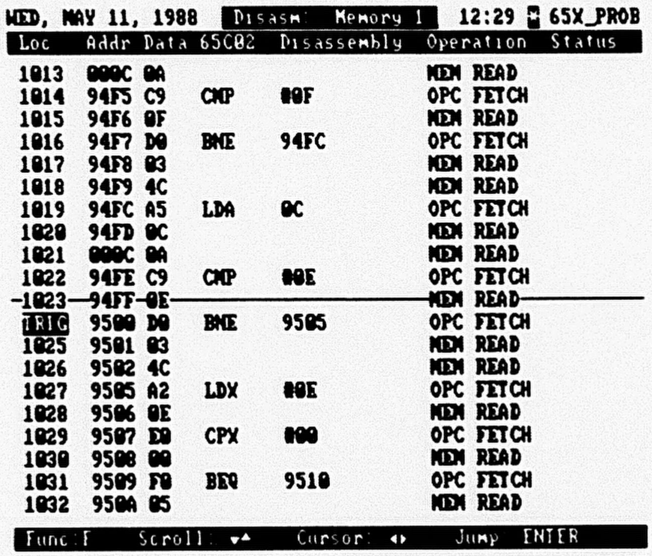
```
THU, MAY 12, 1988        Run Control        00:01 ▣ 65X_PROB

 Update Memory   : [1]      Display: [Disassembly]
 Trigger Position: [0128]     0 [T              ] 2K
 Look for Trigger: [After Pre-Trigger Memory Full]
=======================================================
 Compare         : [Manual]
 Compare Memory 1 to Memory: [2]


 Compare Mem Locations: [0000] to [1792]
 Use Channel Mask     : [OPC_FET ]
 Display Data at least: [9] seconds
+-------------------------------------------------------+
|            ADD  DAT STB INT TST                       |
| Symbol     hex  hex bin bin hex                       |
| OPC_FET :  XXXX XX  11  XXX XX                        |
+-------------------------------------------------------+
 Cursor: ▲▼◀▶        Select: 0,2
```

6594-22

Figure 22. Run Control for cross-trigger. The 1225/1230 looks for the trigger after the pre-trigger memory is full. When the trigger condition GET is found, the probe C cross-triggers the disassembly probe (A and B) and fills the memory. The analyzer stops and displays the acquired data in disassembly format.



WED, MAY 11, 1988 Disasm: Memory 1 12:29 65X_PROB

Loc	Addr	Data	65C02	Disassembly	Operation	Status
1013	000C	0A			MEM READ	
1014	94F5	C9	CMP	#0F	OPC FETCH	
1015	94F6	0F			MEM READ	
1016	94F7	D0	BNE	94FC	OPC FETCH	
1017	94F8	03			MEM READ	
1018	94F9	4C			MEM READ	
1019	94FC	A5	LDA	0C	OPC FETCH	
1020	94FD	0C			MEM READ	
1021	000C	0A			MEM READ	
1022	94FE	C9	CMP	#0E	OPC FETCH	
1023	94FF	0E			MEM READ	
TRIG	9500	D0	BNE	9505	OPC FETCH	
1025	9501	03			MEM READ	
1026	9502	4C			MEM READ	
1027	9505	A2	LDX	#0E	OPC FETCH	
1028	9506	0E			MEM READ	
1029	9507	E0	CPX	#00	OPC FETCH	
1030	9508	00			MEM READ	
1031	9509	F0	BEQ	9510	OPC FETCH	
1032	950A	05			MEM READ	

Func: F Scroll: ▼▲ Cursor: ◄► Jump ENTER

6594-23

Figure 23. Hardware disassembly display. TRIG marks the event that occurred in timebase T1 when trigger event GET occurred in timebase T2.