

Return to [unclear]

TYPE 11B2

NOTES

Written and Produced in Field Training

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SLIDE LIST -- TYPE 11B2

B-11B2-0004	C-11B2-0031
B-11B2-0010	B-11B2-0035
B-11B2-0011	B-11B2-0036
B-11B2-0012	B-11B2-0037
B-11B2-0013	B-11B2-0050
B-11B2-0014	B-11B2-0052
B-11B2-0015	B-11B2-0038
B-11B2-0016	B-11B2-0051
B-11B2-0010	B-11B2-0039
B-11B2-0017	B-11B2-0028
B-11B2-0018	B-11B2-0029
B-11B2-0019	B-11B2-0030
B-11B2-0020	B-11B2-0031
B-11B2-0021	C-11B2-0032
C-11B2-0030	B-11B2-0053
B-11B2-0040	B-11B2-0054
C-11B2-0030	B-11B2-0048
B-11B2-0040	B-11B2-0049
B-11B2-0022	B-11B2-0047
B-11B2-0041	B-11B2-0046
B-11B2-0023	
B-11B2-0042	
B-11B2-0024	
B-11B2-0043	
B-11B2-0025	
C-11B2-0030.1	
B-11B2-0026	
B-11B2-0032	
B-11B2-0027	
B-11B2-0044	
B-11B2-0045	
B-11B2-0033	
B-11B2-0034	

TYPE 11B2 PLUG-IN

I. INTRODUCTION

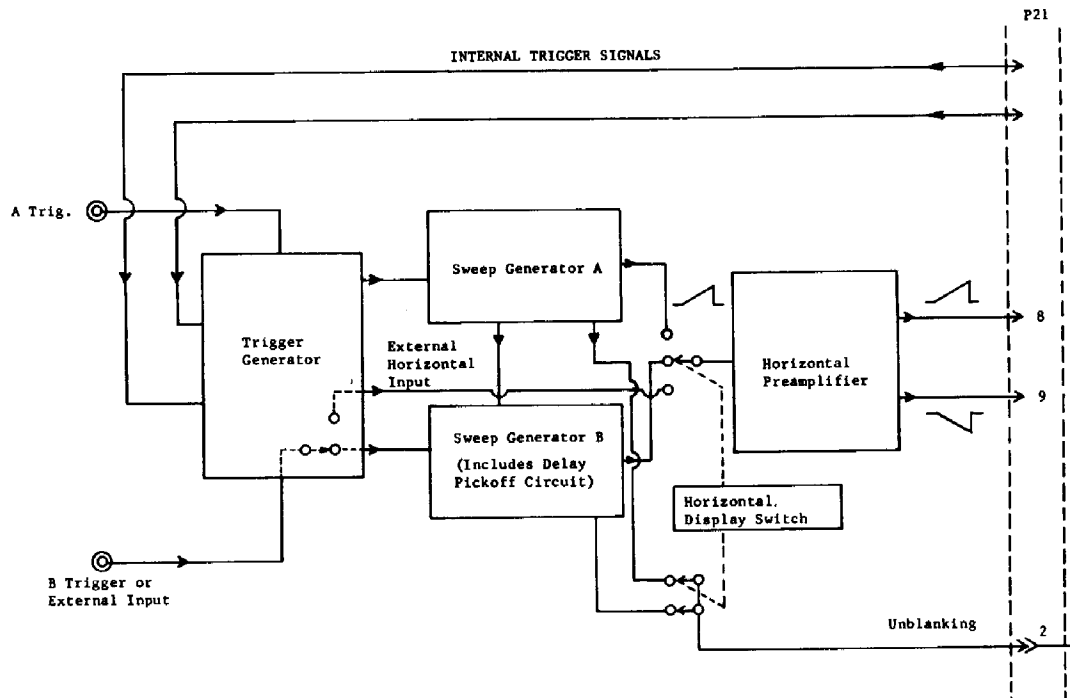
A. The Type 11B2 is a delaying sweep plug-in for the Type 647.

1. Time base A and time base B each have 24 calibrated sweep rates.
 - a. 5 sec/cm to .1 μ sec/cm.
 - b. Independently variable over range of 2.5 to 1 -- neon indicates uncal'd.
 - c. Time base A is the main time base.
2. Both sweeps trigger from DC to over 50 mc in all modes.
3. Time Base A Trigger:
 - a. COUPLING
 - (1) AC
 - (2) AC LF REJ
 - (3) DC
 - b. SLOPE
 - (1) + or -
 - c. TRIG MODE
 - (1) FREE RUN
 - (2) AUTO
 - (3) NORM
 - (4) SINGLE SWP
 - d. SOURCE
 - (1) INT
 - (2) LINE
 - (3) EXT, $\pm 5v$
 - (4) EXT X10, $\pm 50v$

4. Time Base B Trigger:
 - a. Coupling
 - (1) AC
 - (2) DC
 - b. Slope
 - (1) + or -
 - c. Source
 - (1) INT
 - (2) EXT
5. The HORIZ DISPLAY switch has six operating modes:
 - a. B DELY'D BY A (not triggered)
 - b. A INTEN BY B (not triggered)
 - c. A
 - d. A INTEN BY B (triggered)
 - e. B DELY'D BY A (triggered)
 - f. EXT INPUT
6. A X10 MAG is provided.
 - a. A neon indicates MAG ON.
7. Time base A is considered the main time base .
8. Time base B is a delayed time base .
 - a. It is always controlled by time base A .
 - b. An electrical interlock prevents time base B from running unless time base A is operating .
 - (1) The "wrap around" problem in the 535/545 series is thereby prevented .

- c. B sweep rates are controlled by pulling out on the SWEEP RATE control, thereby engaging the B sweep timing switch.
 - d. Time base B usually is set to run faster than time base A.
9. In A INTENS BY B mode (non-triggered), time base A operates in the normal manner but time base B will not start until a time determined by the DELAY TIME MULTIPLIER and the A SWEEP RATE.
- a. The trace is brightened during the B time base interval.
10. In the A INTEN BY B mode (triggered), time base B will become armed at the end of the DELAY TIME interval but will omit a trigger before beginning sweep.
11. In the B DELY'D BY A mode, the B time base will begin at a time after the start of A sweep, determined by the setting of the DELAY TIME MULTIPLIER and the A SWEEP RATE.
- a. Only the B sweep will be displayed.
 - b. In the triggered mode, the B time base will be armed by the DELAY TIME INTERVAL but will await a trigger before beginning sweep.
12. Single sweep feature is available.
- a. The ready light is housed inside the RESET button.
13. EXT HORIZ amplification is available through the TRIG IN or EXT INPUT jack.
14. Front panel outputs (miniature male BNC connectors):
- a. A SWEEP OUT, 15v, 1.6K.
 - b. B SWEEP OUT, 15v, 1.6K.
 - c. A GATE OUT, 10v, 750Ω.
 - d. B GATE OUT, 10v, 750Ω.

B. Block Diagram



Type 11B2 Plug-In

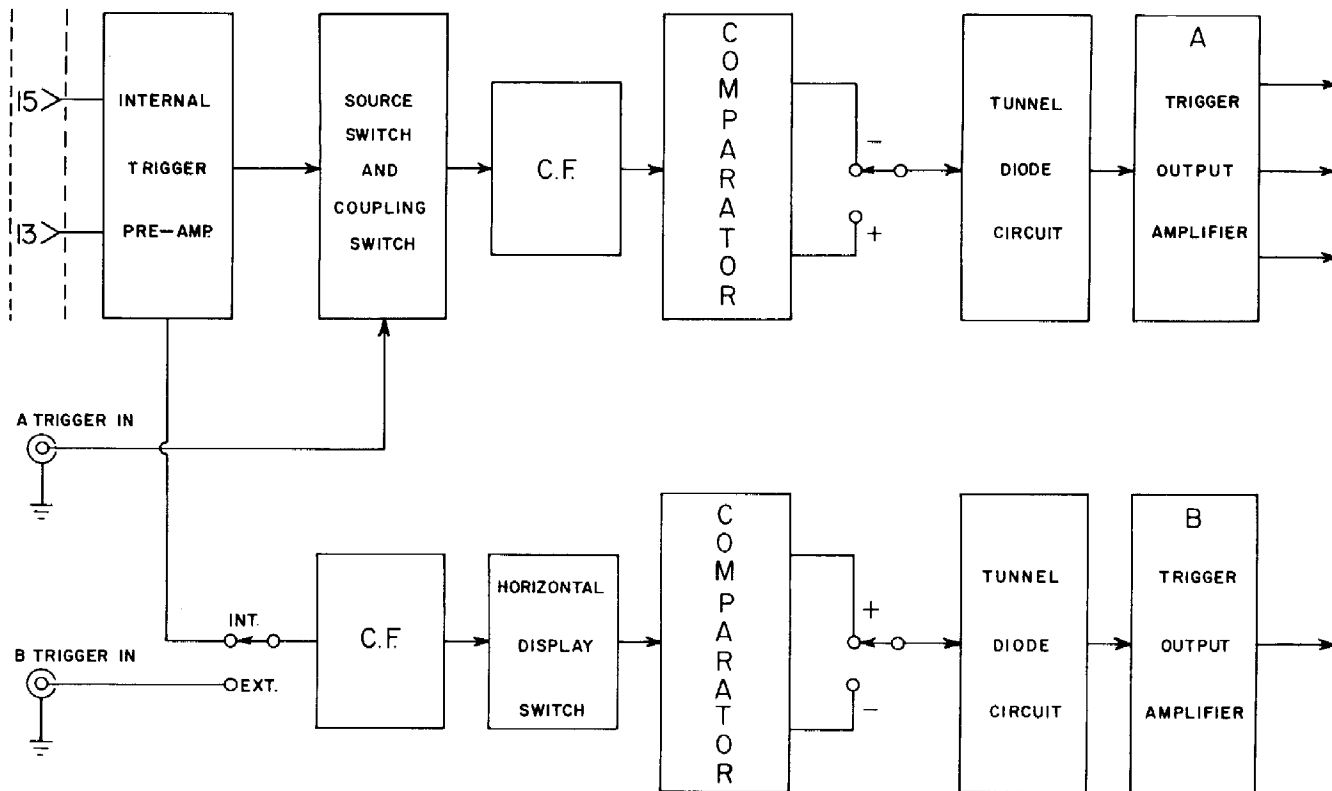
II. TRIGGER GENERATOR

A. The trigger generator provides a trigger of uniform shape and polarity for both A and B sweeps.

B. Basic Circuits

1. Internal trigger preamplifier.
2. Two nuvistor cathode followers (one for each sweep).
3. Two comparator circuits.
4. Two tunnel diode trigger shaper circuits.
5. Time trigger output amplifier.

C. Block Diagram



TYPE 11B2 TRIGGER GENERATOR
BLOCK DIAGRAM

B-11B2-0010
10-24-63 jg

Type 11B2 Plug-In

D. Switches and Controls

1. Two (trigger) SOURCE switches (one for each sweep).
2. Two (trigger) COUPLING switches.
3. Two SLOPE switches.
4. Two TRIGGER LEVEL controls.

E. Inputs

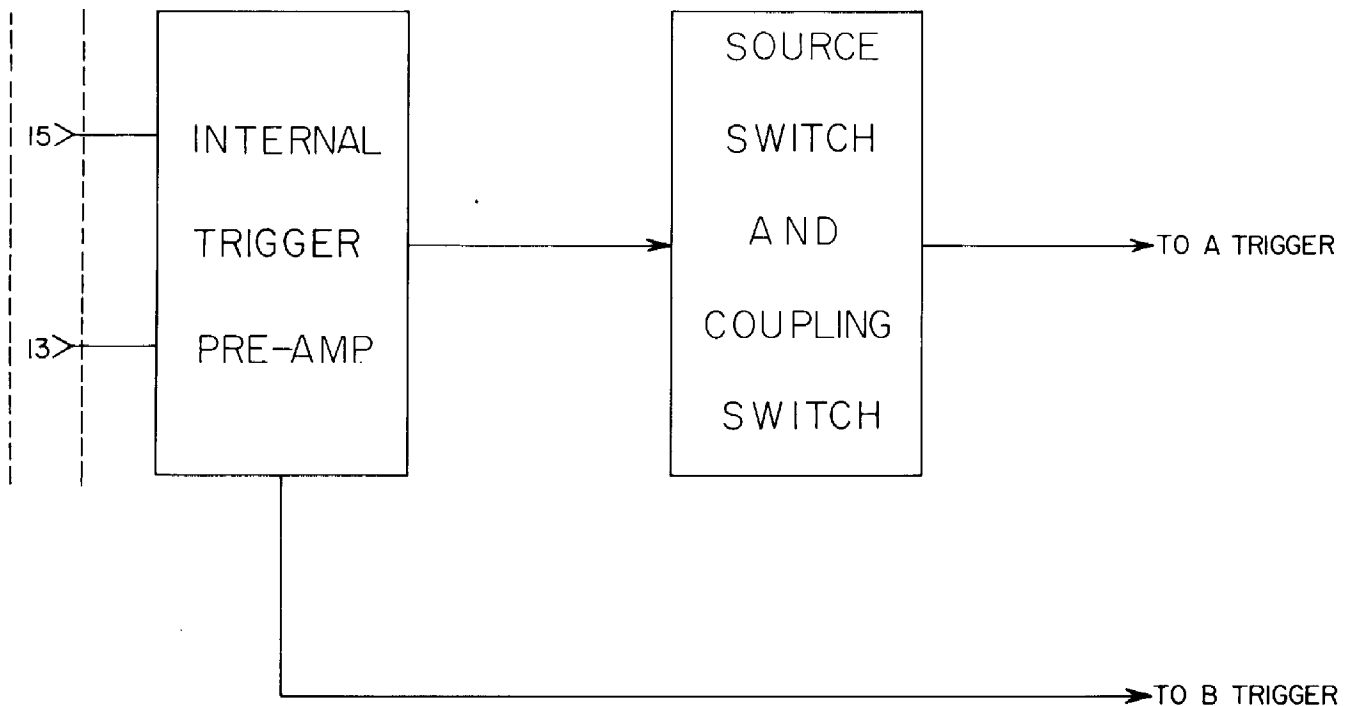
1. Internal trigger (at pins 13 and 15) from the 10A2 Trigger Amplifier.
2. (A) TRIG IN. (Front Panel Jack)
3. (B) TRIG IN or EXT (HORIZ) INPUT. (Front Panel Jack)

F. Outputs

1. A Sweep Auto circuit (anode D105).
2. A Sweep Auto circuit (to D105 through C102, D102).
3. A Sweep Gating TD (to D125 through D120, D121).
4. B Sweep Gating TD (to D225 through D220, D221).

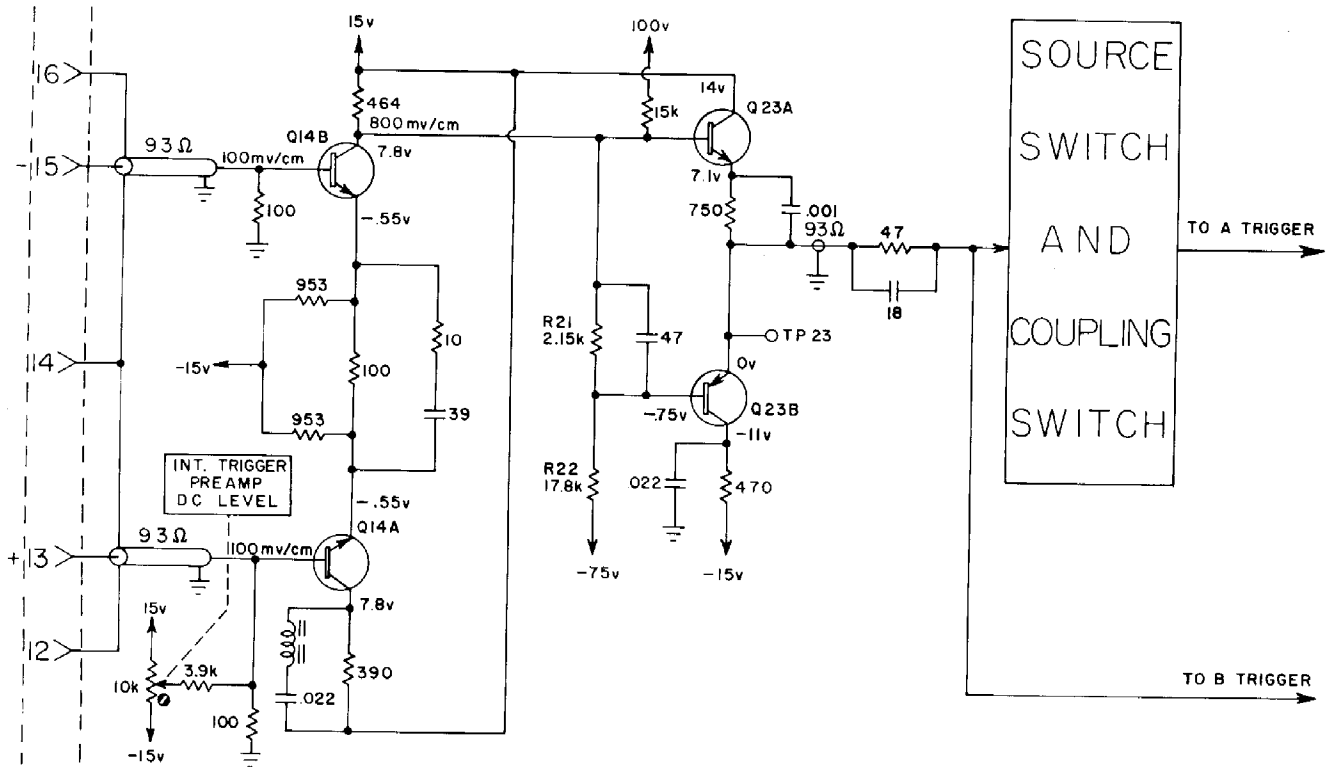
G. Internal Trigger Preamp

1. Block Diagram



Type 11B2 Plug-In

2. The circuit consists of a push-pull transistor amplifier (151-108 transistors) driving a complementary pair of emitter followers.
 - a. The NPN is a 151-108 and the PNP is a 151-122.
3. It converts the push pull Internal Trigger to a single ended trigger signal.



TYPE 11B2 TRIGGER GENERATOR
INTERNAL TRIGGER PREAMPLIFIER

B-11B2-0012x

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Type 11B2 Plug-In

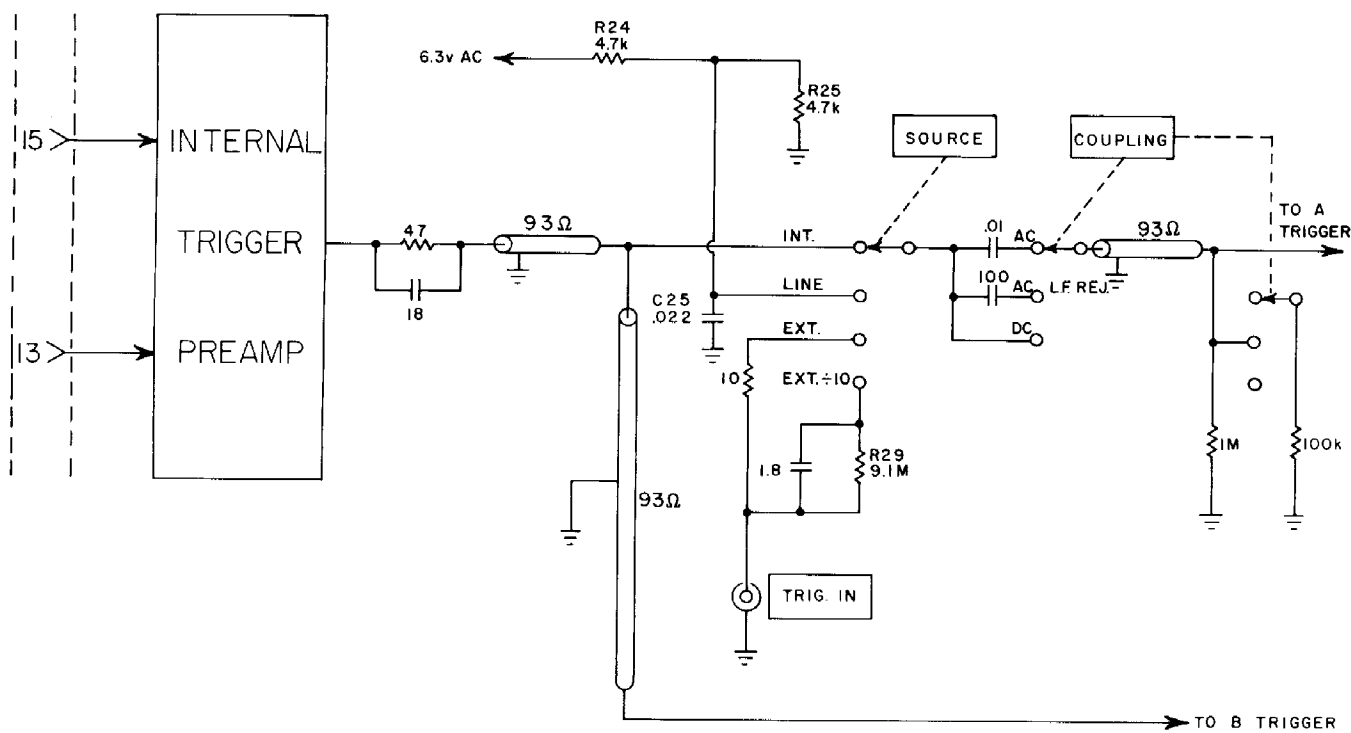
4. The input signal from the 10A2 Trigger Amplifier.
 - a. The signal passes from the 10A2 blue ribbon connector through the 647 and appears on pins 13 and 15 on the 11B2 connector.
 - b. Adjacent blue ribbon connector pins 12, 14 and 16 are grounded, providing uniform shielding and effectively extending the 93 Ω transmission line into the connector.
 - c. The 93 Ω transmission lines are terminated at Q14A and Q14B bases in 100 Ω .
 - d. Signal level is 100 mv/cm each side.
 - e. + signal appears on pin 13, - signal on pin 15.
5. Single ended output is taken across Q14B collector load.
 - a. Q14A collector load resistor provides temperature stabilization by balancing power dissipation.
 - b. The signal level at Q14B collector is 800 mv/cm.
6. Quiescent levels, Q14A, Q14B.
 - a. Q14A, Q14B Bases, 0v.
 - b. Q14A, Q14B Emitters, -.55v.
 - c. Q14A, Q14B Collectors, 7.8v.
7. Q23A and Q23B are a NPN-PNP complementary pair.
8. R21, R22 set Q23B base at -.75v.
 - a. Q23B base potential assures compatibility with other trigger inputs by setting the emitter at 0v.
 - b. DC zero at Q23B emitter is assured by INT TRIG PREAMP DC BAL adj. at the base of Q14A.

Type 11B2 Plug-In

9. Quiescent levels, Q23A, Q23B.

- a. Q23A base, 7.8v.
- b. Q23A collector, 14v.
- c. Q23A emitter, 7.1v.
- d. Q23B base, -.75v.
- e. Q23B collector, -11v.
- f. Q23B emitter, 0v.

H. SOURCE Switch (A Sweep Trigger)



TYPE 11B2 TRIGGER GENERATOR
SOURCE AND COUPLING SWITCH

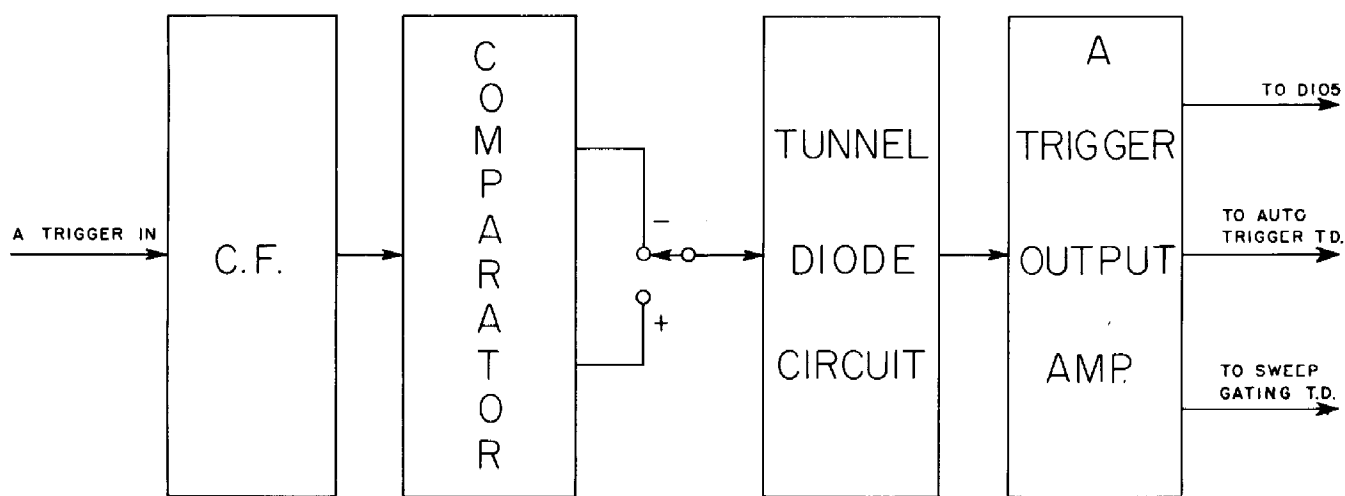
B-11B2-0013x
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Type 11B2 Plug-In

1. A lever wafer switch provides selection of INT, LINE, EXT and EXT X10.
 2. 6.3v AC is tied to pin 30 (blue ribbon connector).
 - a. The 6.3v is attenuated to 3.15 by R24, R25.
 - b. C25 helps reduce the aberrations found on the sine wave at the power transformer secondary.
 3. EXT input Z is 1 M at 25 pf.
 4. EXT X10 uses the 9.1 M (R29) and the 1 M R30A for X10 attenuation.
 - a. Note that in the AC LF REJ position of the coupling switch, the attenuation is X100.
 - b. Can accept 500v without damages.
 - c. Input Z is 10 M at 5 pf.
- I. COUPLING Switch (A Sweep Trigger)
1. A lever wafer switch provides selection of DC, AC, and AC LF REJ coupling.
 - a. AC coupled is 3 db down at 16 cps (TC = .01 sec).
 - b. AC LF REJ is 3 db down at 16 kc (TC = 10 μ sec).
 2. The 93 Ω coax used between the COUPLING switch and the CF is just a shielded wire, not a transmission line.

Type 11B2 Plug-In

J. "A" Trigger Generator Block



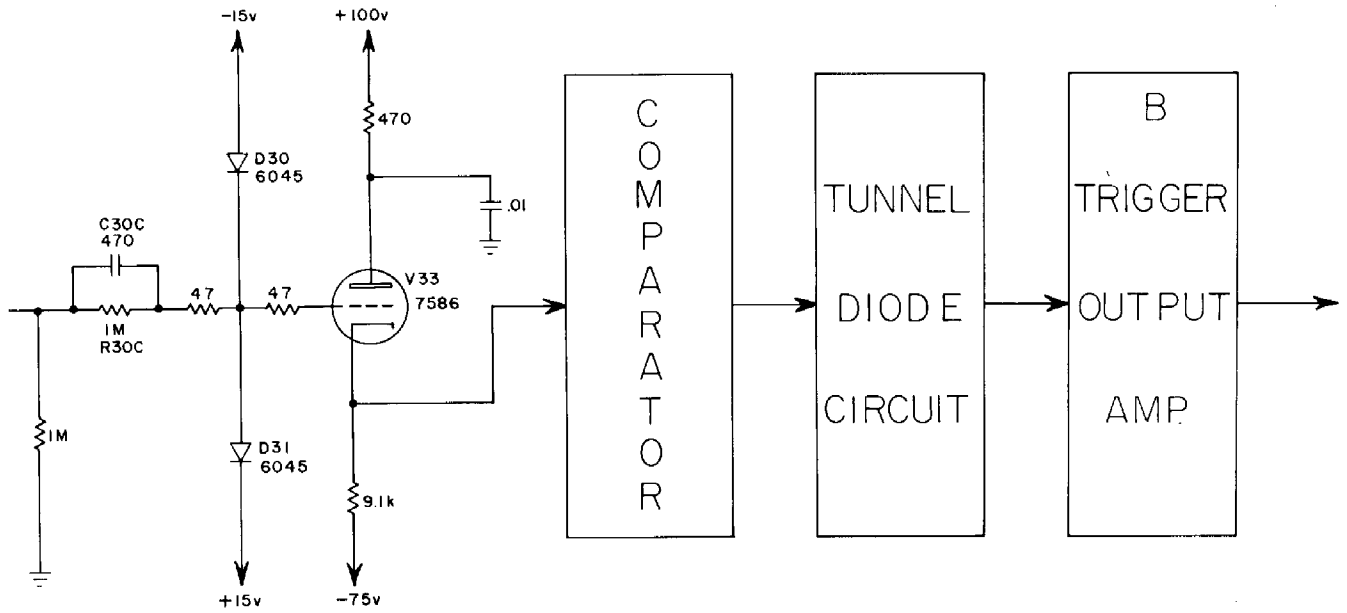
TYPE 11B2 TRIGGER GENERATOR
A TRIGGER BLOCK DIAGRAM

B-11B2-0014

10-29-'63 DL

Type 11B2 Plug-In

K. "A" Trigger Input CF (V33)



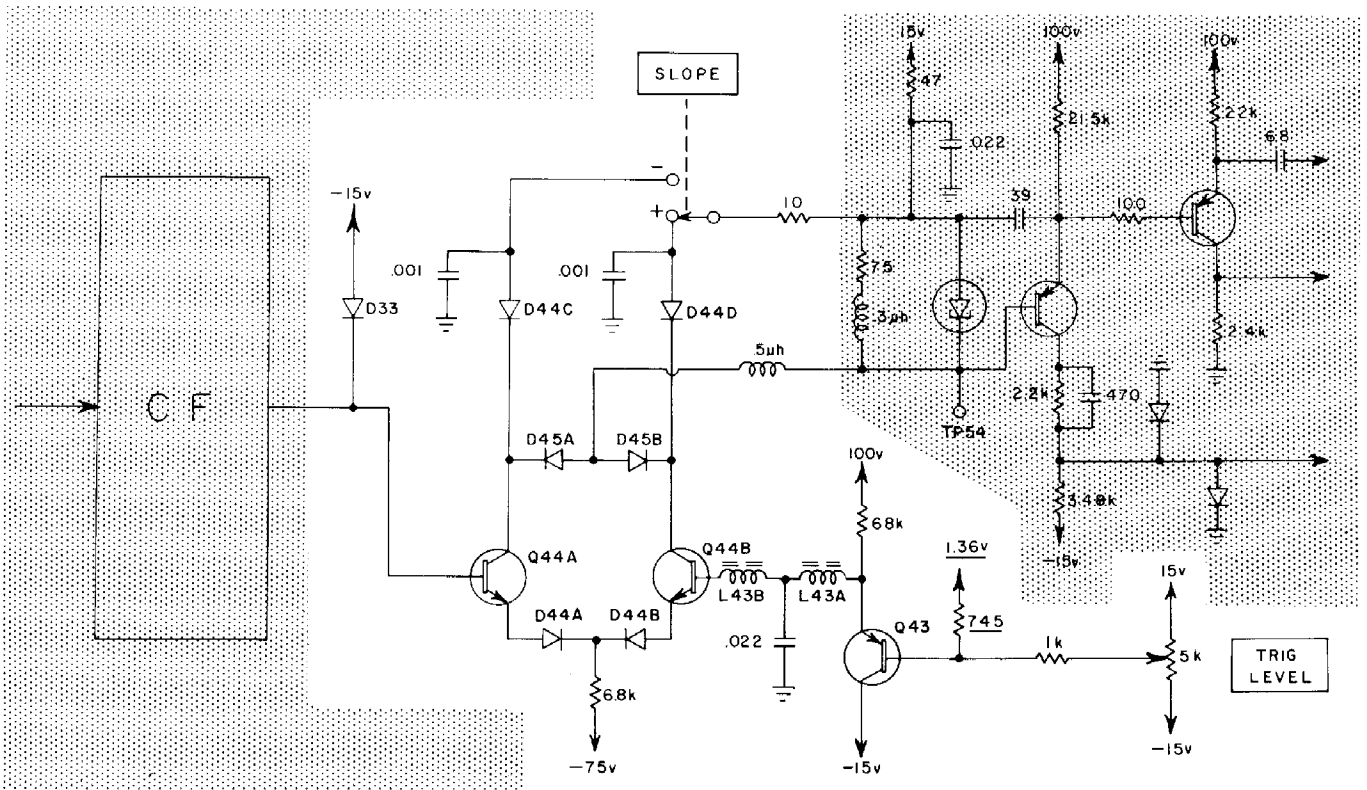
TYPE IIB2 TRIGGER GENERATOR
A TRIGGER INPUT C.F.

B-IIB2-0015x
10-28-63 jg

Type 11B2 Plug-In

1. A 7586 nuvistor is used as a trigger input cathode follower.
2. Nuvistor protection is provided by the conventional 1M protective resistor R30C (bypassed by C30C) and diodes D30 and D31.
 - a. The diodes and R30C theoretically provide protection to 40,000v -- practical limitation of about 400v is imposed by capacitor breakdown voltage.
 - b. The diodes allow the grid to move $\pm 15v$.
3. The cathode is long-tailed to -75v.
 - a. The CF draws about 8 ma.

L. "A" Trigger Comparator



TYPE IIB2 TRIGGER GENERATOR
A TRIGGER TUNNEL DIODE AND OUTPUT AMPLIFIER

B-IIB2-0016.3

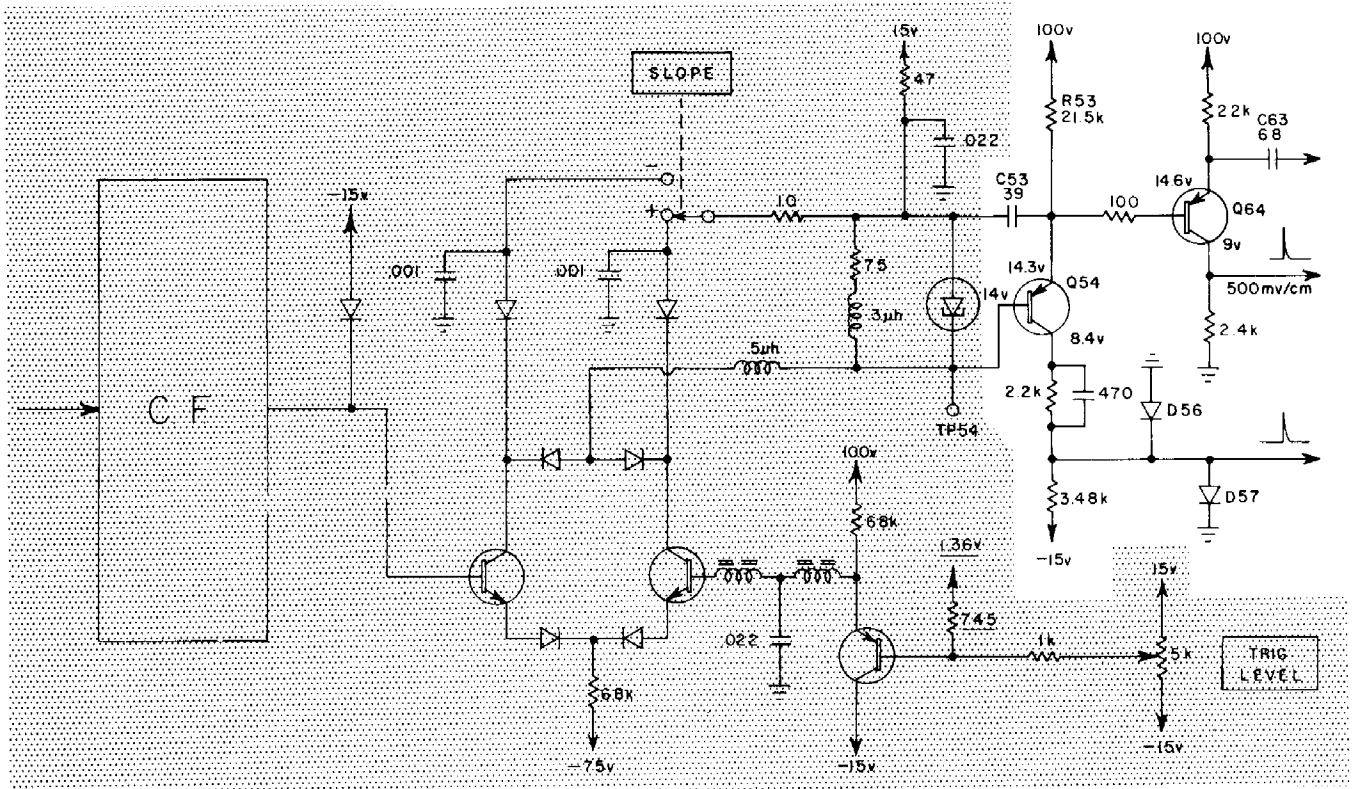
10-28-'63 jg

Type 11B2 Plug-In

1. The comparator provides a current trigger for the TD.
2. Trigger waveforms on Q44A base are compared with the TRIG LEVEL voltage on Q44B base.
3. The SLOPE switch provides selection of either + or - slope.
4. Each collector has two current paths selected by the SLOPE switch.
 - a. In the + SLOPE position, Q44A collector current passes through D45A and the TD.
 - b. In the - SLOPE position, D44C anode is tied to +15v bringing it into conduction.
 - c. D45A cathode is pulled up cutting it off.
 - d. Q44A collector current flows through D44C to +15v.
 - e. In the - SLOPE position, Q44B collector current flows through D45B to the tunnel diode.
5. D33 protects Q44A during nupistor warm-up.
6. The TRIG LEVEL control has a swing of 30v ($\pm 15v$).
 - a. The swing is limited by R42A and 42B to 14.5v on Q43 base.
 - b. R42A and R42B equivalent circuit is 745Ω to 1.36v.
7. Q43 provides a low impedance source for TRIGGER LEVEL voltage.
 - a. Q43 is long-tailed to +100v.
8. Although the comparator bases normally operate close together, it is possible for the bases to be 22v apart.
 - a. Q44A base can swing $\pm 15v$ and Q44B base can swing $\pm 7v$.
 - b. D44A and D44B protect Q44A and Q44B from emitter-base breakdown.
 - c. V_{EBO} for a 151-103 is 5v.

Type 11B2 Plug-In

N. "A" Trigger Output Amplifier



TYPE IIB2 TRIGGER GENERATOR
A TRIGGER TUNNEL DIODE AND OUTPUT AMPLIFIER

B-11B2-0016.1

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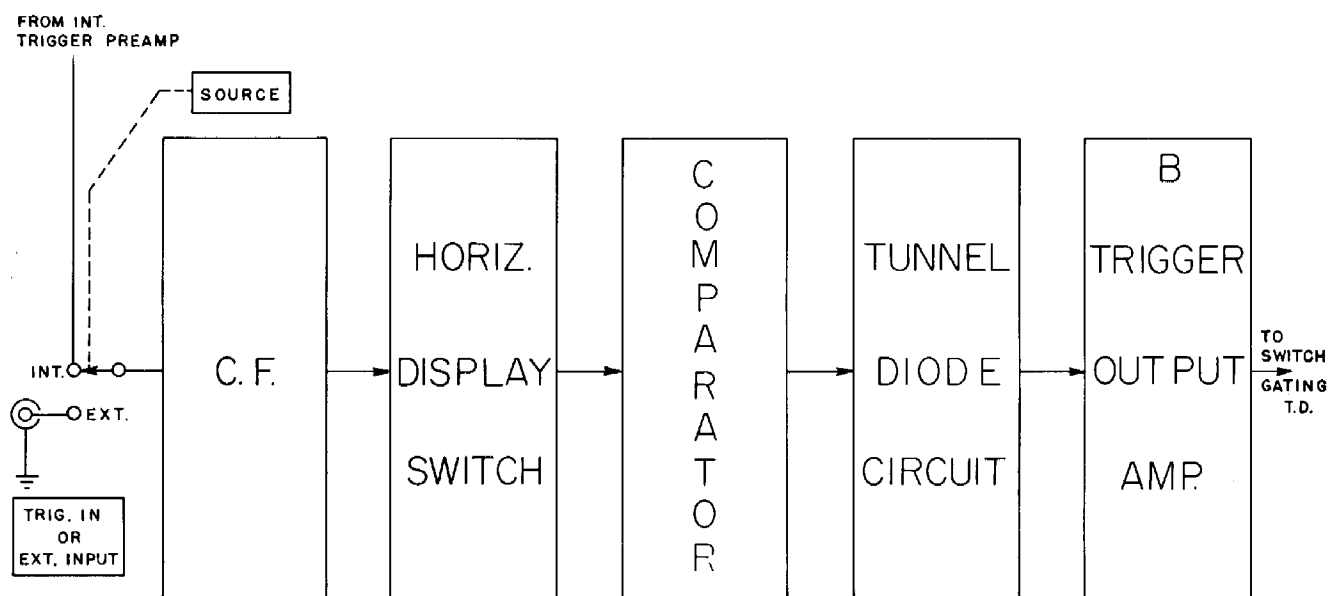
1. Q54 is a 2N964 Motorola Germanium transistor.
2. The 500 mv TD swing is applied to Q54 base.
3. Practically the full 500 mv appears across the 21.5k emitter resistor (R53) to drive Q64 base.
4. With a large proportion of the base signal appearing on the emitter, there is practically no change in collector current.
 - a. The (6 nsec) leading edge of the TD waveform does appear at the collector, however.

Type 11B2 Plug-In

- b. C53 bypasses the emitter for 6 nsec negative going pulse.
 - c. Pulse risetime on the collector is about 1.5 nsec.
5. D56 and D57 limit the pulse amplitude to prevent crosstalk to the Sweep Generator.
6. Q64 is a Motorola 2N967 Germanium transistor.
7. Q64 can be considered a phase inverter.
 - a. Collector output is about 50 mv.
8. C63 is a bypass capacitor that grounds into the AUTO circuit instead of chassis ground.
9. Quiescent levels Q54.
 - a. Q54 base, 14v.
 - b. Q54 emitter, 14.3v.
 - c. Q54 collector, 8.4v.
10. Quiescent levels Q64.
 - a. Q64 base, 14.3v.
 - b. Q64 emitter, 14.6v.
 - c. Q64 collector, 9v.
11. Outputs.
 - a. The 50 mv output from Q64 collector goes to D105 in the AUTO circuit through C102 and D102.
 - b. The current drive from Q54 collector goes to the A Sweep Gating TD through D120 and D121.

Type 11B2 Plug-In

O. B Trigger Block Diagram



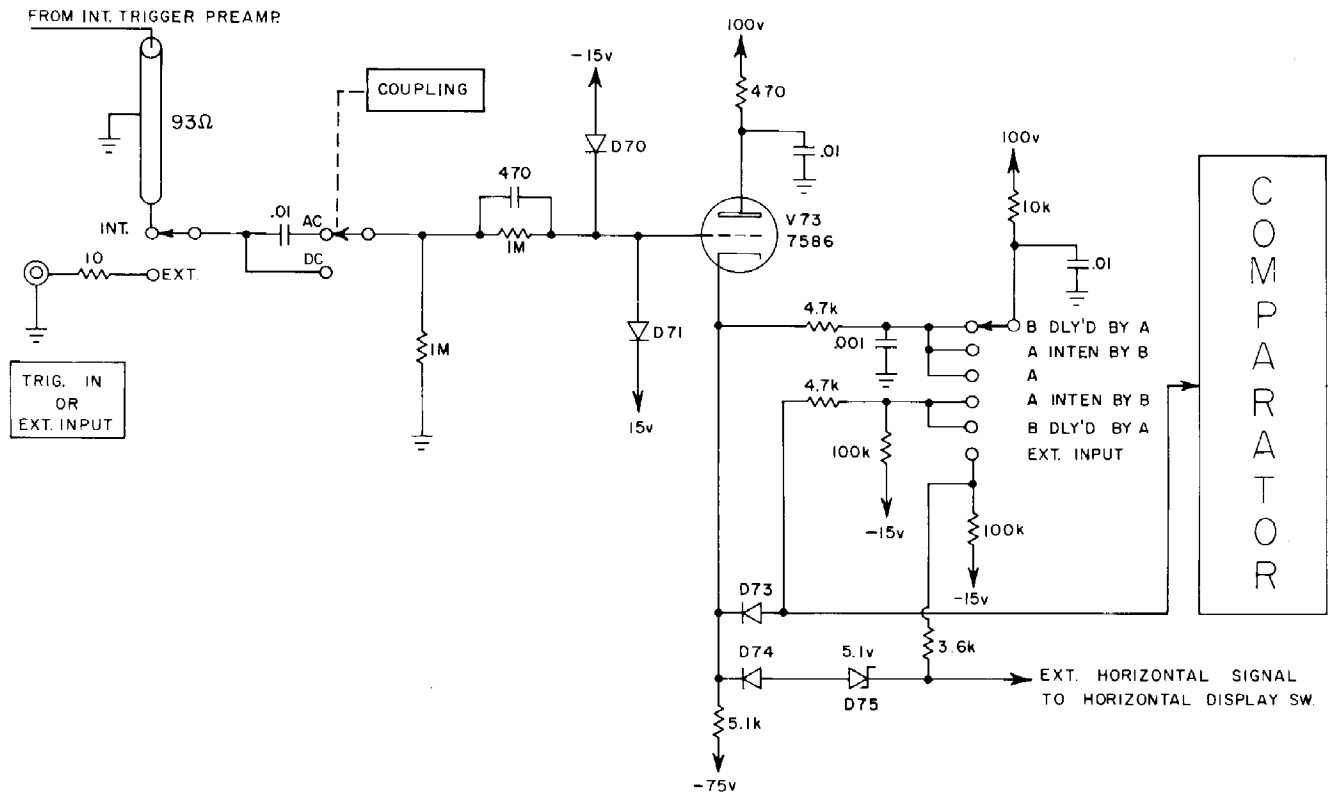
TYPE 11B2 TRIGGER GENERATOR
B TRIGGER BLOCK DIAGRAM

B-11B2-0017

10-28-63 DL

Type 11B2 Plug-In

P. "B" Trigger Input CF (V73)



TYPE 11B2 TRIGGER GENERATOR
B TRIGGER CATHODE FOLLOWER

B-11B2-0018x
11-8-63 jg

1. The circuit is basically the same as the A Trigger CF.
2. In the EXT INPUT mode of the HORIZ DISPLAY switch, the CF becomes the EXT HORIZ input CF.

Type 11B2 Plug-In

3. INPUTS selected by the SOURCE switch.
 - a. EXT position connects to TRIG IN or EXT INPUT jack.
 - (1) BNC front panel jack.
 - (2) 1M at 25 pf input impedance.
 - b. INT position connects to the INT TRIGGER PREAMPLIFIER through a 93 Ω coax.
 - (1) INT TRIG PREAMP can drive both A and B trigger circuits simultaneously.
 - (2) About 30 nsec signal delay is encountered between the 10A2 input and the CF cathode.
4. Coupling has AC and DC positions.
 - a. No AC LF REJ.

Q. HORIZ DISPLAY Switch (1R Section)

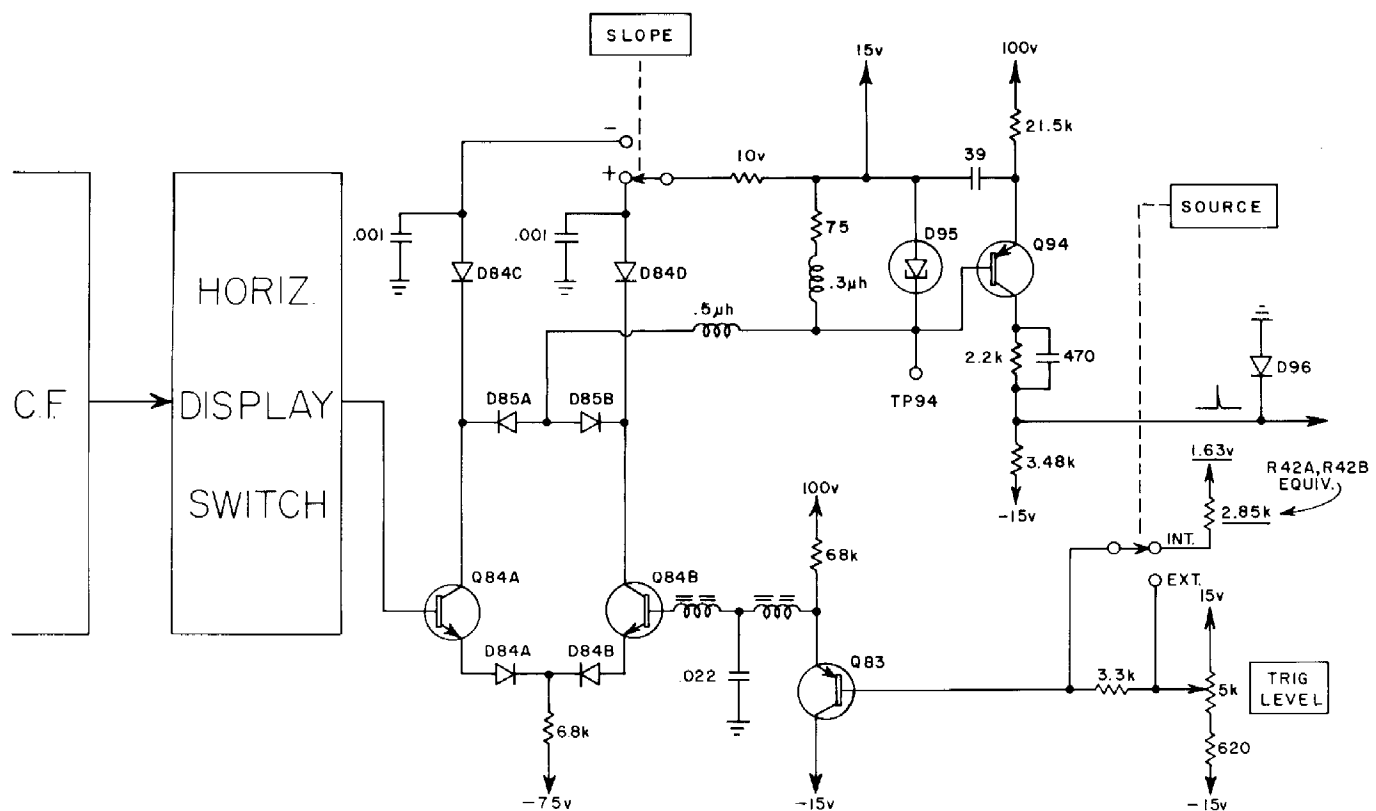
1. Selects three basic modes:
 - a. Non-Triggered B Sweep.
 - b. Triggered B Sweep.
 - c. EXT HORIZ INPUT.
2. Non-Triggered B Sweep Modes
 - a. V73 cathode is tied to 100v through a 10k and 4.7k resistor by the HORIZ DISPLAY switch.
 - (1) The equivalent circuit is 3.78k to -30v.
 - (2) About 8 ma flows through V73.

Type 11B2 Plug-In

- b. D73 anode is connected through 100k to -15v.
 - (1) D73 cuts off.
 - (2) The signal path to the comparator is open.
 - c. D74 anode is connected to -14v through 100k and D75.
 - (1) D74 cuts off.
 - (2) The signal path to the HORIZ PREAMP is open.
3. Triggered B Sweep Modes
- a. D73 anode is tied to +100v through 4.7k and 10k.
 - (1) D73 conducts, allowing triggers to be applied to the comparator.
 - b. D74 is cut off.
 - (1) The signal path to the HORIZ PREAMP is open.
4. EXT INPUT Mode
- a. D73 anode is tied to -15v (through 100k) and is cut off.
 - (1) The signal path to the comparator is open.
 - b. D74 anode is tied to +100v through 10k.
 - (1) D74 conducts.
 - (2) EXT HORIZ INPUT signal can pass to the HORIZ PREAMP.
 - c. The DC level is raised (from 1.7v on the V73 cathode) to 7v by D75, a 5v zener.
 - (1) The 7v at the HORIZ PREAMP input places the trace in the center of the screen in the EXT INPUT mode.

Type 11B2 Plug-In

R. "B" Trigger Comparator



TYPE IIB2 TRIGGER GENERATOR
B TRIGGER COMP, T.D. AND TRIGGER OUTPUT AMPLIFIER

B-11B2-0019x
11-7-63 jg

1. The trigger comparator composed of Q84A and Q84B and associated circuitry is the same as the A trigger comparator.

Type 11B2 Plug-In

2. A section of the SOURCE switch changes the range of the TRIG LEVEL control.
 - a. Q83, the TRIG LEVEL EF, has a swing of $\pm 5\text{v}$ in the INT position.
 - b. In the EXT position R82C is shorted, increasing the range of TRIGGER LEVEL to $\pm 13\text{v}$ at Q83 base.

- S. "B" Trigger Tunnel Diode Trigger Shaper
 1. The TD circuit composed of D95 and associated components is the same as the A Trigger Shaper.

- T. "B" Trigger Output Amplifier
 1. The B trigger output amplifier has only one output -- to the B sweep SWP GATING TD, D225 through D220 and D221.
 2. A negative going current pulse about 6 nsec wide.
 3. Clamping diode D96 limits the negative voltage excursion.

Type 11B2 Plug-In

III. SWEEP GENERATOR A

A. Sweep Generator A supplies linear sweep ramp to the Horizontal Preamp.

B. Triggering Modes

1. SINGLE SWEEP
2. NORM
3. AUTO
4. FREE RUN

C. Outputs

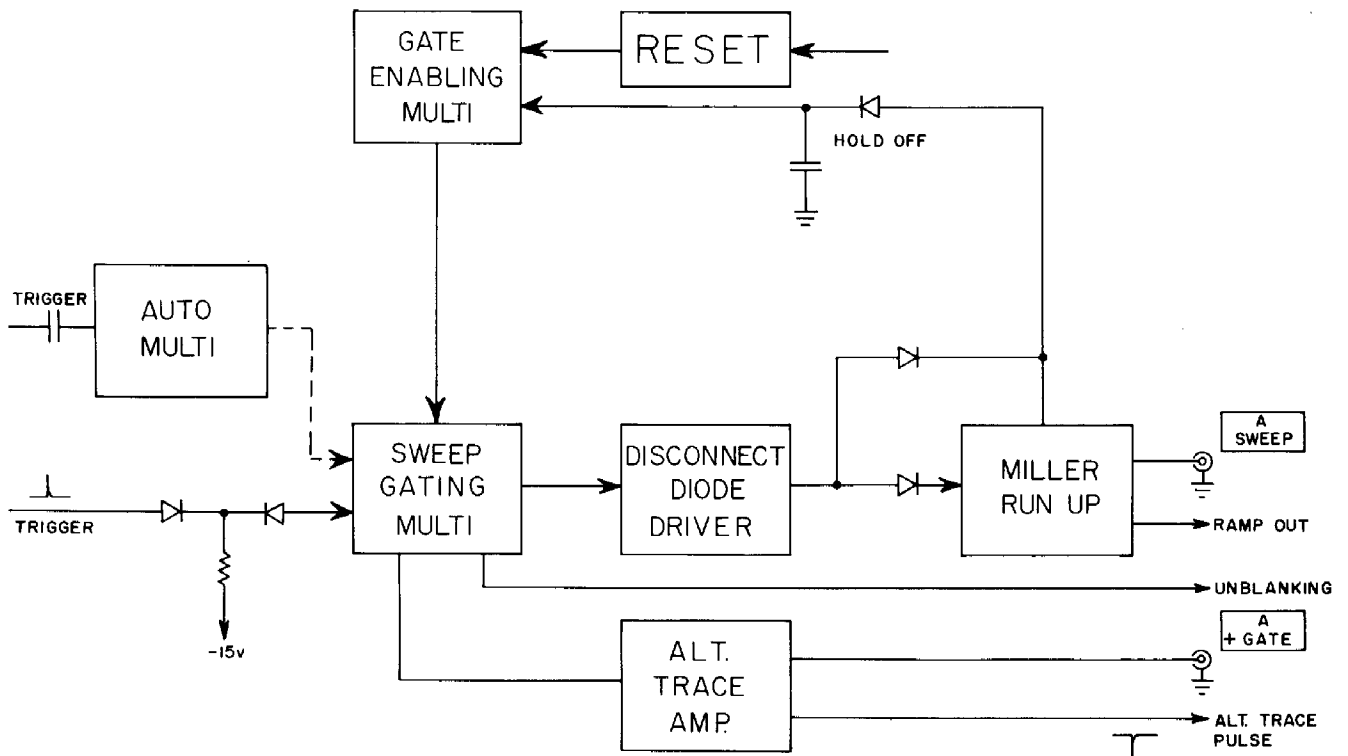
1. "A" SWEEP out (front panel jack) 10v.
2. "A" + GATE out (front panel jack) 15v.
3. A 10v positive going ramp to the Horizontal Preamp.
4. 10v positive going ramp to the Delay Pickoff circuit, B Sweep.
5. A 5v negative going alternate trace pulse.
6. A 6.5v negative going unblanking pulse.

D. Basic Circuits

1. Sweep Gating Multi (TD circuit and Q124).
2. Disconnect Diode Drive Amp (Q154).
3. Miller Run-Up.
4. Gate Enabling Multi.
5. Auto Multi.
6. Alt Trace Amplifier.
7. Single Sweep Circuit.

Type 11B2 Plug-In

E. Block Diagram



TYPE 11B2 'A' SWEEP GENERATOR
BLOCK DIAGRAM

B-11B2-0020
11-19-'63 jg

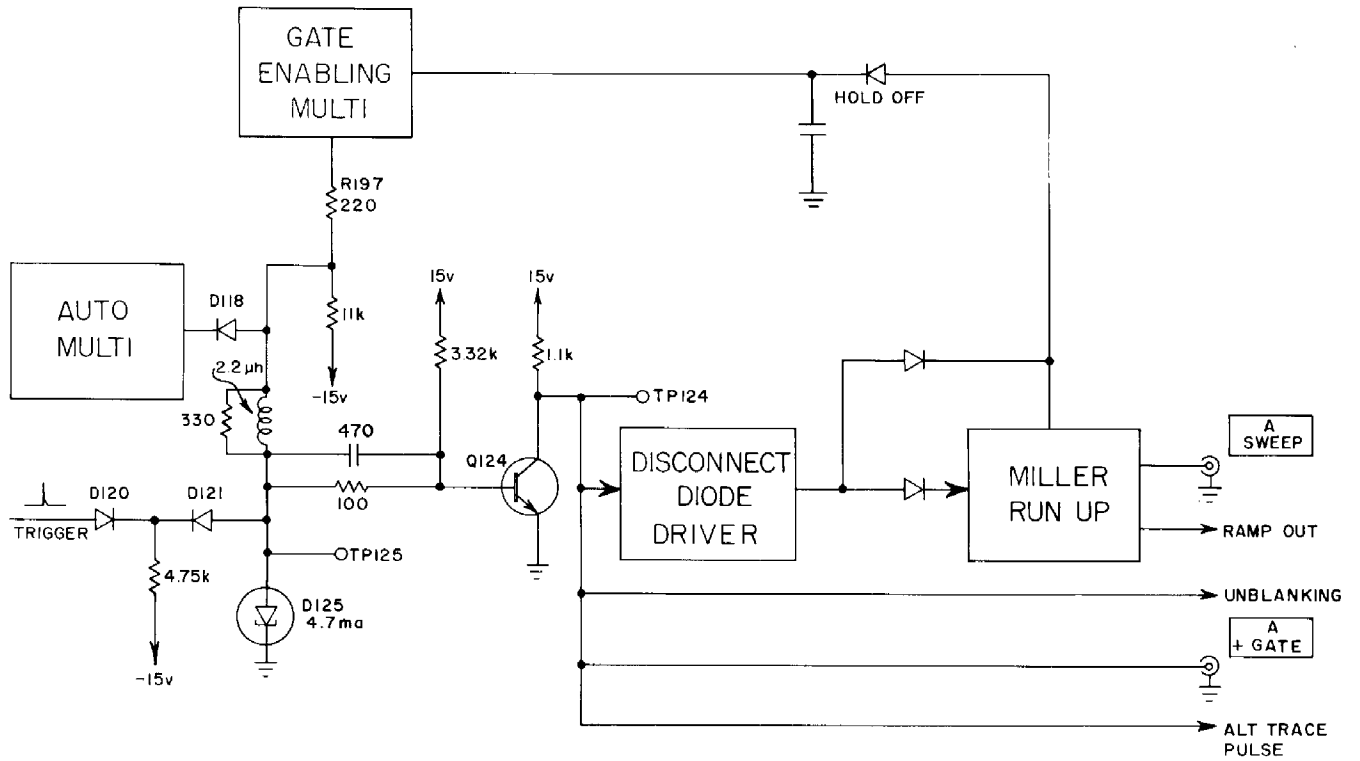
Type 11B2 Plug-In

1. Block Logic

- a. A positive going trigger flips the Sweep Gating TD (D125) into its high state.
- b. The output from the Sweep Gating circuit (Q124 collector) is a negative going step.
- c. The negative step appears amplified at the Disconnect Diode Driver output (Q154 collector).
- d. The negative step cuts off the Disconnect Diodes (D158, D159) starting sweep.
- e. The Miller Run-Up output is a positive going ramp 10v peak to peak.
- f. The sweep ramp is fed through the hold-off diode (D180) and through Q183 to the Gate Enabling Multi.
- g. As the end of the sweep is reached, the Gate Enabling Multi flips, opening the Sweep Gating TD current path.
- h. Reverse current through the Sweep Gating TD flips it to the locked out (non-triggerable) low state.
- i. The resultant positive step brings the disconnect diodes into conduction.
- j. The sweep ramp is terminated and retrace begins.
- k. The hold-off diode opens allowing the hold-off cap to discharge slowly.
- l. At the end of hold-off, the Gate Enabling Multi flips to its quiescent state.
- m. The Sweep Gating TD is returned to its triggerable state.

Type 11B2 Plug-In

F. Sweep Gating Multi

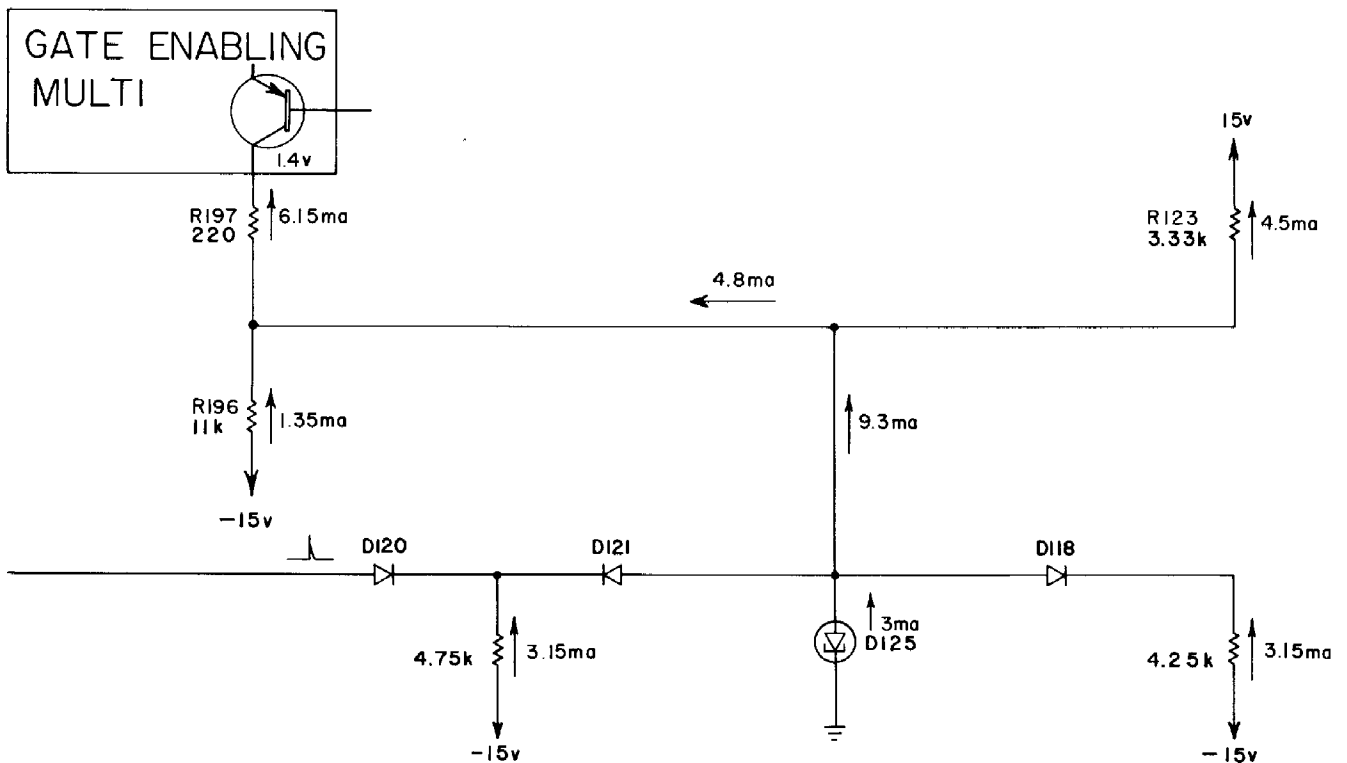


TYPE 11B2 'A' SWEEP GENERATOR
SWEEP GATING MULTI

B-11B2-0021x
11-19-63 jg

Type 11B2 Plug-In

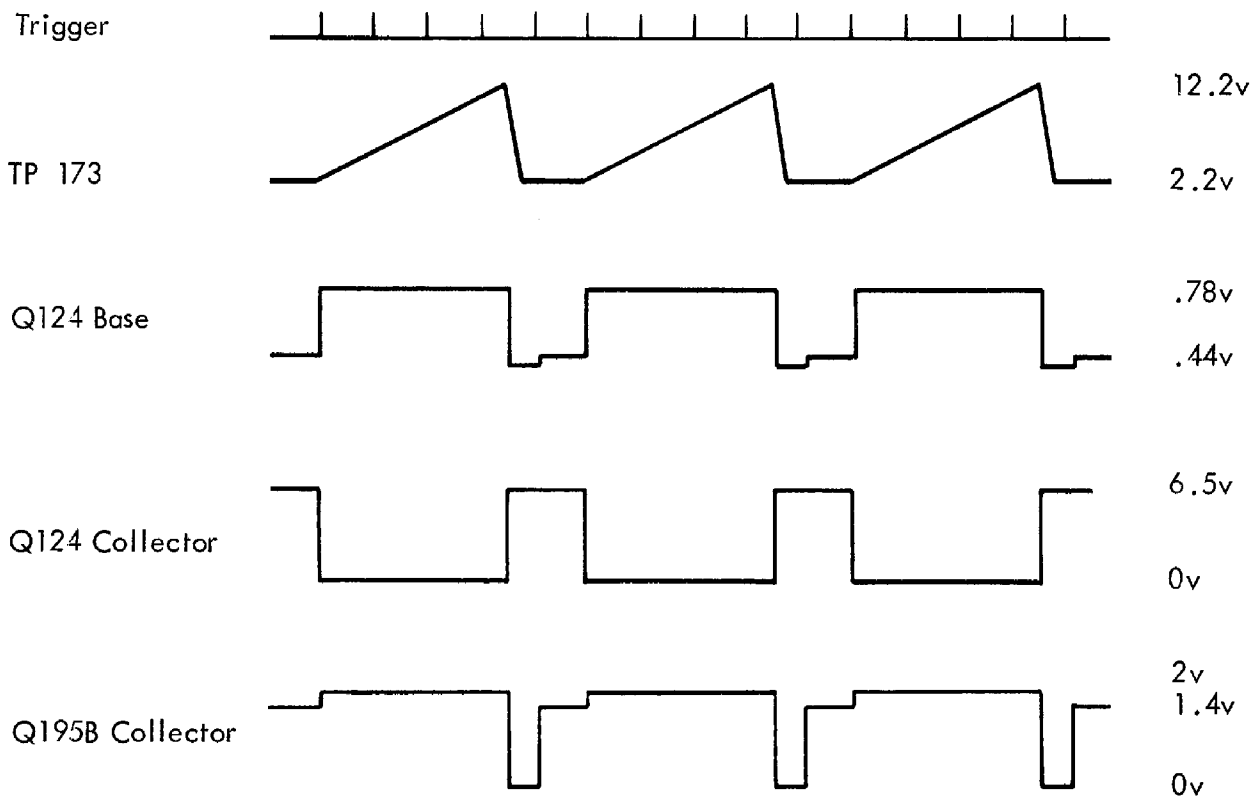
1. The Sweep Gating Multi provides a negative going (6.5v) step to start sweep.
2. D125 is a 4.7 ma GE tunnel diode*.
3. Q124 is a 151-108 Motorola silicon NPN transistor.
4. In the quiescent condition, the TD is in its low state with 3 ma forward current.
 - a. D120 (HD 5000) is cut off, D121 (HD5000) is conducting.
 - b. Q124 is cut off.
 - c. D118 is conducting.
 - d. The Gate Enabling Multi holds the top of R197 at 1.4v.
5. Current distribution in the quiescent state.



* See curve in appendix.

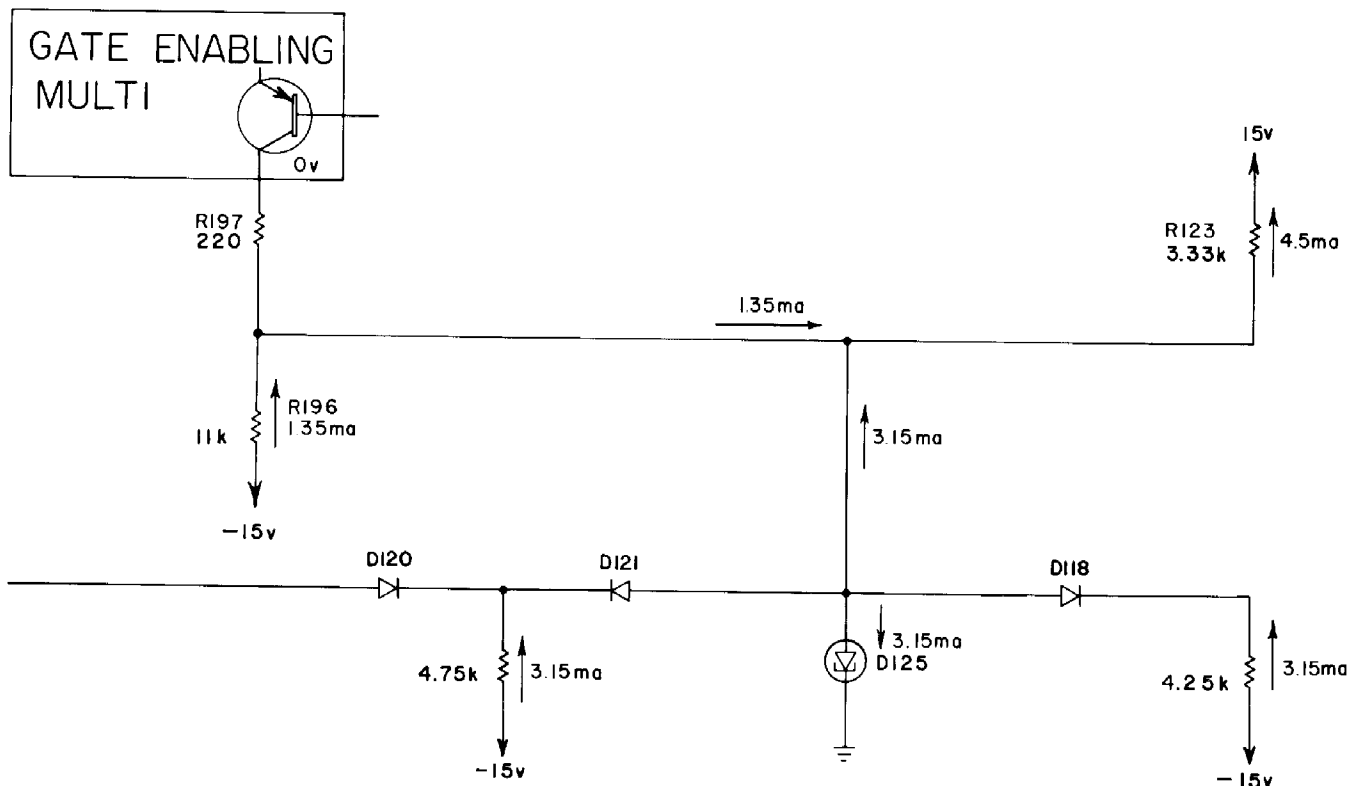
Type 11B2 Plug-In

- a. 6.15 ma flows through R197.
 - (1) 1.35 ma of this flows through R196 leaving 4.8 ma from the TD circuit.
 - b. 4.8 ma and 4.5 ma through R123 totals 9.3 ma from the TD circuit.
 - c. The 9.3 ma is composed of:
 - (1) 3.16 ma through D121.
 - (2) 3.16 ma through D118.
 - (3) 3 ma through D125.
 - d. D125 requires an additional 1.7 ma to flip it into its high state.
6. Sequence of operation at start of sweep.



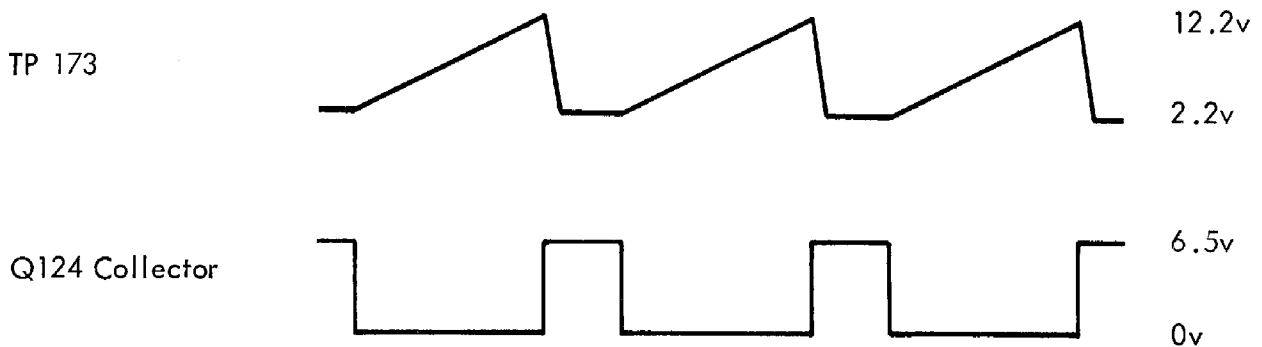
Type 11B2 Plug-In

- a. A positive going trigger (6 nsec wide) lifts D120 into conduction, disconnecting D121.
 - b. The current (3.16 ma) through D121 is diverted to the TD.
 - (1) The 3.16 ma is added to the 3 ma of quiescent TD current.
 - (2) This is enough to flip the TD into its high state.
 - c. As the TD flips, its anode lifts to about 500 mv.
 - d. Q124 base is raised to 780 mv.
 - (1) Q124 is turned on.
 - (2) Q124 collector drops from 6.5v to 0v.
 - e. After the trigger has passed (6 nsec), D121 conducts again robbing the TD of the 3.16 ma.
 - (1) The TD hysteresis will not allow the TD to slip to its low state, however, until its current is reduced to about .4 ma.
7. As the sweep ramp reaches its maximum, the Gate Enabling Multi drops the top of R197 to 0v.
- a. 3.15 ma of reverse current flows through D125 flipping to its low state.
8. Current distribution during hold-off.



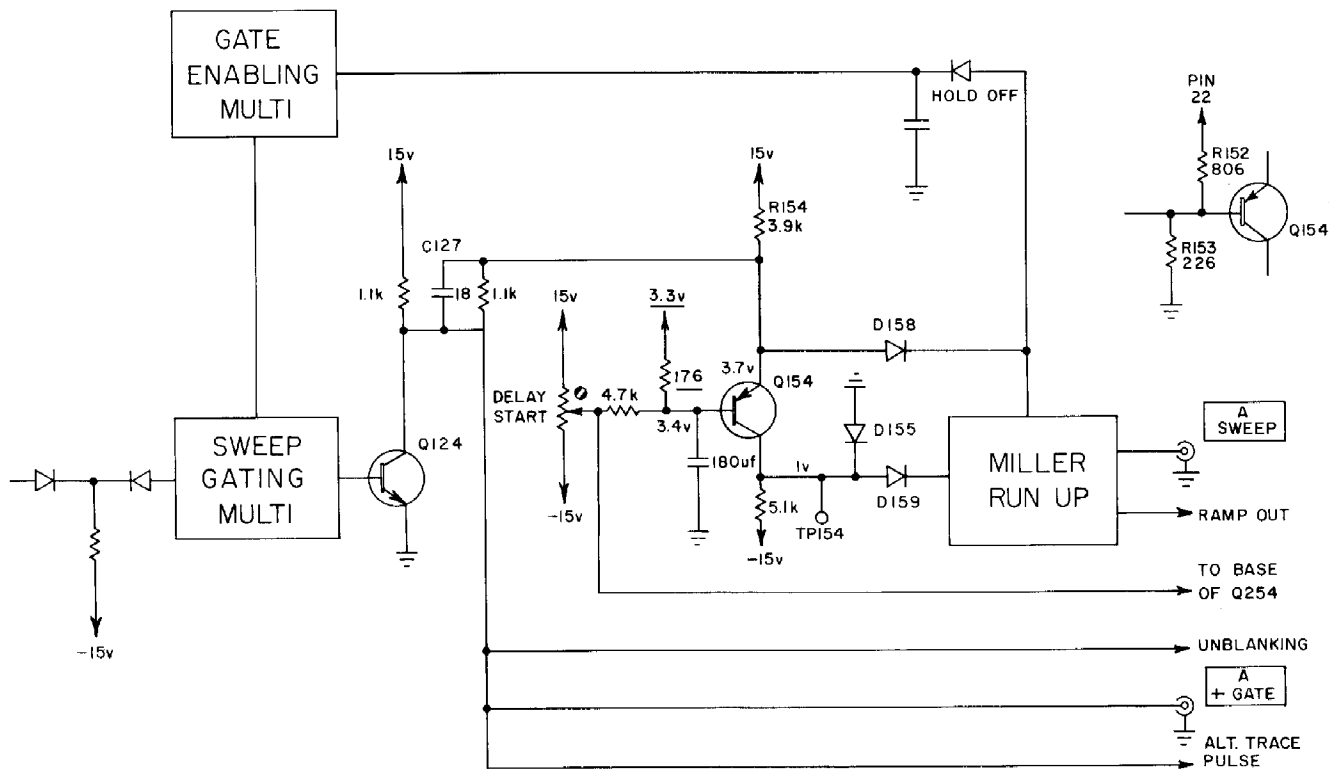
Type 11B2 Plug-In

- a. With no current flowing through R197, the 1.35 ma through R196 flows through R123 to +15v.
 - b. As 4.5 ma flows through R123, 3.15 ma must flow from the TD circuit.
 - c. 3.15 ma flowing through D121 and 3.15 ma through D118 total 6.32 ma flowing into the TD circuit.
 - d. With only 3.15 ma flowing away from the TD, the TD has 3.15 ma of reverse current.
9. As D125 flips to the reverse bias state, Q124 base is dropped to .44v.
- a. Q124 cuts off.
 - b. A124 collector rises to 6.5v.
10. In this state, incoming triggers cannot flip the TD.
11. At the end of hold-off, the Gate Enabling Multi lifts the top of R197 to 1.4v.
12. The Sweep Multi has returned to the quiescent state.
13. The circuit output waveform (Q124 collector) is a negative going (6.5v to 0v) rectangular waveform of the same duration as the sweep.
- a. It drives the Diode Driver Amplifier.
 - b. Serves as unblanking pulse.
 - c. It drives the Alternate Trace Amplifier.



Type 11B2 Plug-In

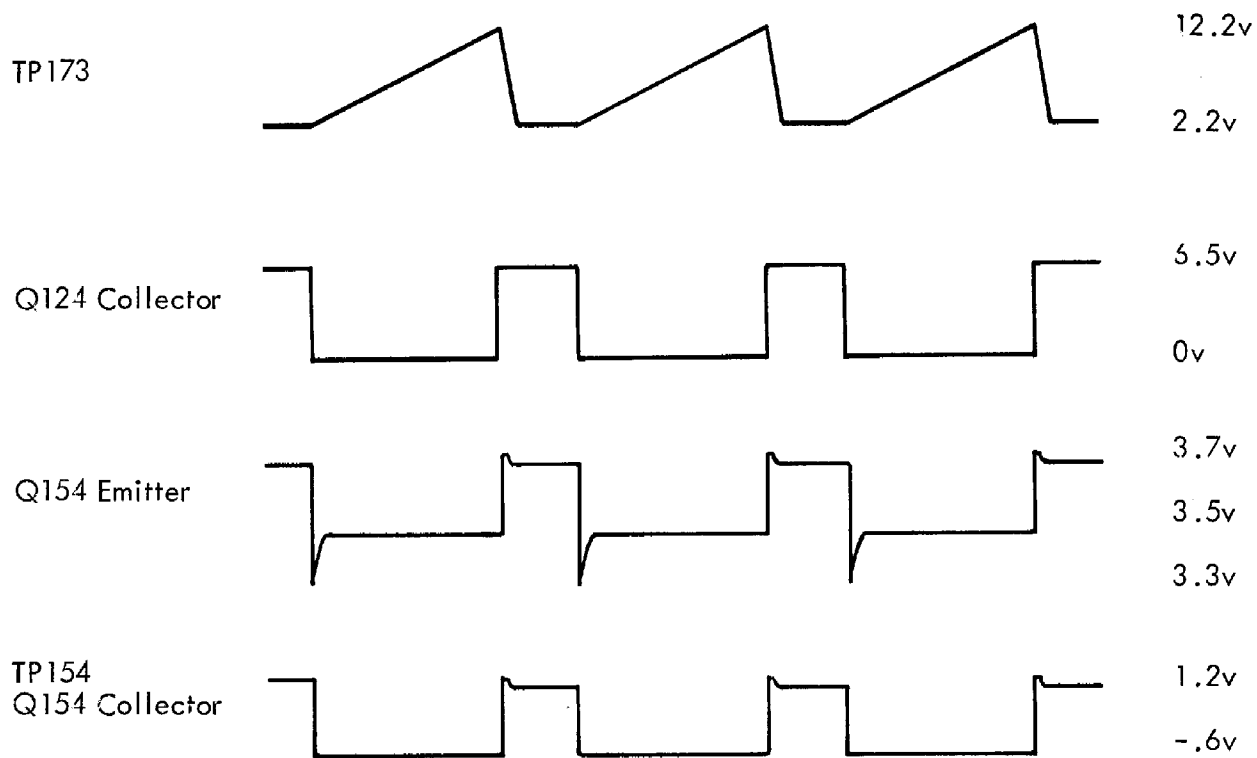
G. Disconnect Diode Driver (Q154)



1. Provides the negative going step that turns off the disconnect diodes (D158 and D159).
2. Q154 is a 2N967 PNP Germanium transistor; D155 is a 1N3605 GE silicon diode.
3. Q154 quiescent levels (these are typical values -- the Delay Start Adj sets the base potential).
 - a. Q154 base, 3.4v.
 - b. Q154 emitter, 3.7v.
 - c. Q154 collector, 1v (TP154).

Type 11B2 Plug-In

4. As an incoming trigger flips the Sweep Gating TD, the negative step at Q124 collector passes through C127 to Q154 emitter.
5. Sequence of operation at start of sweep.

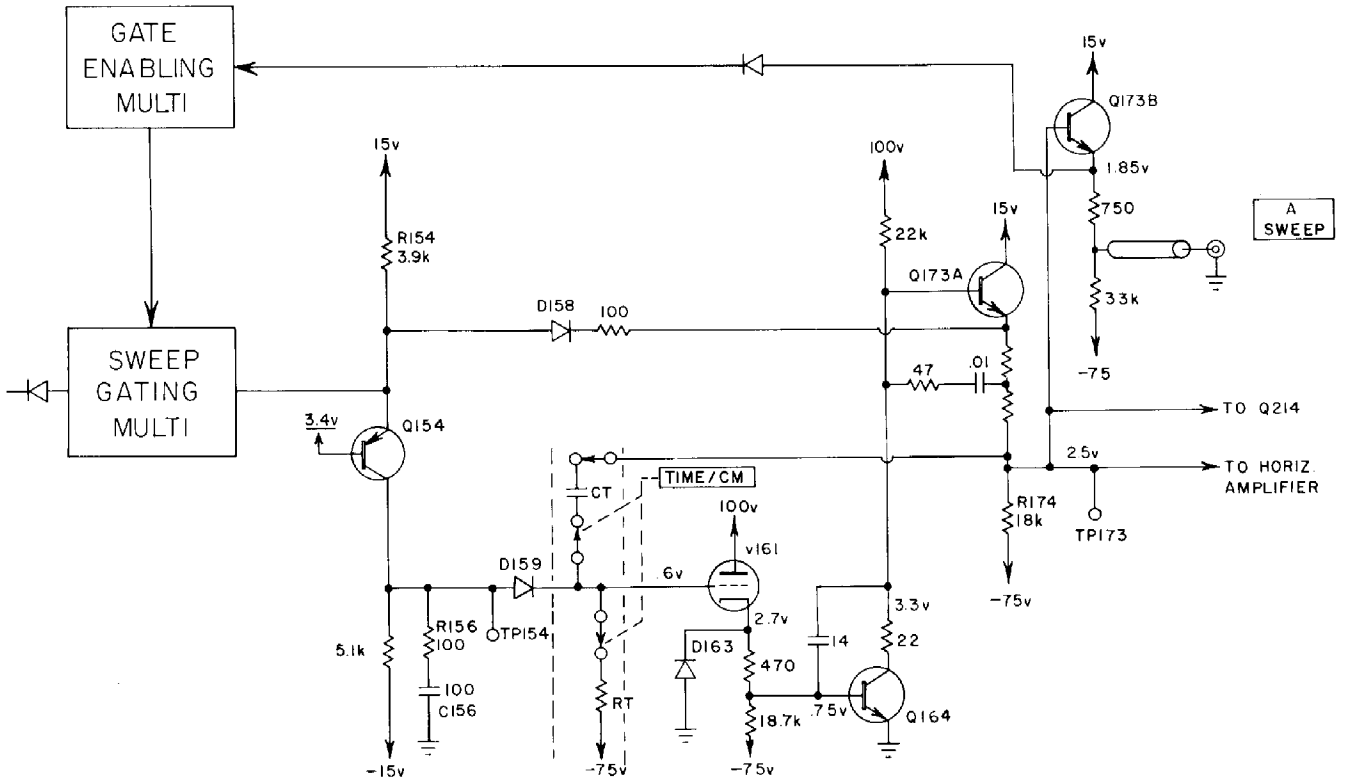


- a. Q154 emitter drops from 3.7v to 3.3v.
 - (1) The negative step disconnects D158.
 - (2) The emitter returns on a rather fast RC curve to 3.5v.
- b. The collector drops from 1.2v to -.6v.
 - (1) D155 conducts, limiting the collector swing to -.6v.
 - (2) D155 protects D159 from reverse bias breakdown.
- c. The negative step pulls down on D159 cutting it off.
 - (1) Sweep starts.

Type 11B2 Plug-In

6. Sequence of operation at the end of sweep.
 - a. The TD flips to its non-triggerable low state.
 - b. The positive step from Q124 collector lifts Q154 emitter to 3.75v.
 - c. Q154 collector raises to 1.6v.
 - d. D159 conducts.
 - e. Sweep stops and retrace begins.
 - f. At the end of retrace, D158 conducts.
 - (1) The added current through R154 drops Q154 emitter to 3.7v.
 - (2) Q154 collector drops to 1.2v.
7. The circuit has returned to its quiescent state.
8. The DELAY START ADJ sets the start of both A and B sweeps.
 - a. The purpose of the control is discussed under DELAY PICKOFF CIRCUIT.
 - b. A divider forms the equivalent circuit 176Ω to 3.3v.
 - c. The divider ties to pin 22 which is tied directly to the power supply.
 - (1) Pin 22 supplies this point and the top of the DELAY TIME MULTIPLIER only.
 - (2) Prevents jitter.
 - d. A uniform sweep starting point assumes greater importance with only a 10v sweep ramp out of the Miller circuit.

H. Miller Run-Up Circuit



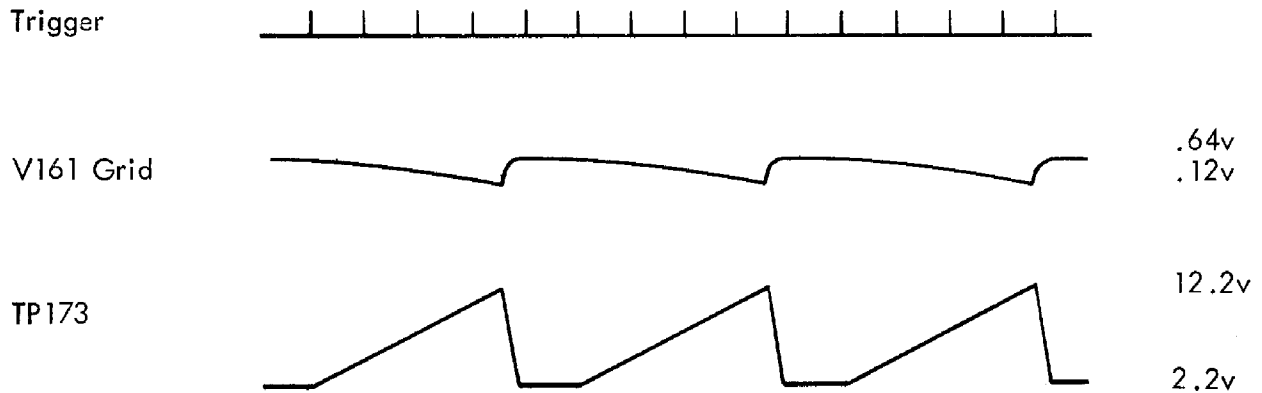
TYPE IIB2 'A' SWEEP GENERATOR
MILLER RUN UP

B-IIB2-0023x
II-27-'63 jg

1. The Miller Run-Up circuit supplies a linear sweep ramp to the HORIZ PREAMPLIFIER.
 - a. 10v peak-to-peak.
 - b. 2.5 to 12.5v at TP173.

2. Basically this is the familiar Miller Integrator circuit.
3. The circuit is composed of a nuvistor, three transistors and two diodes.
 - a. V161 is a 7586 RCA nuvistor.
 - b. Q164 is a 2N2369 Fairchild NPN silicon transistor.
 - c. Q173A is a 151-108 selected Motorola 2N2501 NPN silicon transistor.
 - d. Q173B is a 151-103 selected Motorola 2N2219 NPN silicon transistor.
 - e. D158 is a 3605 GE silicon diode.
 - f. D159 is a Tek GaAs diode.
4. Sweep linearity design spec is 1%.
 - a. Leakage currents in timing circuits must not exceed 20 na from all sources at high ambient temperatures.
 - b. Nuvistor input to the Miller amplifier, a low leakage Tek GaAs disconnect diode and low leakage Tek-made timing capacitors all help keep leakage currents low.
5. A gain of 1000 is desirable in order to achieve linearity.
 - a. 1000 gain is not available in a triode.
 - b. Pentode nuvistor not available.
 - c. Highest regulated supply is 100v -- inadequate for conventional Miller run-up tube circuit.
6. V161 is used as an input CF.
7. Q164 is a high gain amplifier.
8. Q173A and Q173B are emitter followers.

- 9. Quiescent levels, V161, Q104, Q173A, Q173B.
 - a. V161 grid .6v (set by DELAY START ADJ).
 - b. V161 cathode, 2.7v.
 - c. Q164 base, .75v.
 - d. Q164 collector, Q173A base, 3.3v.
 - e. Q173A emitter, Q173B base, 2.5v.
 - f. Q173B emitter, 1.85v.
- 10. Quiescent current paths establishing stable starting point for the sweep ramp:
 - a. Current is flowing through the timing resistor, D159 and Q154, to +15v.
 - b. Current flows through R174, D158 and R154 to +15v.
- 11. Sequence of operation:



- a. Q154 emitter and collector voltages drop.
 - b. D158 and D159 cut off.
 - c. The timing resistor current previously flowing through D159 is diverted to the timing capacitor.
 - d. The timing capacitor begins to charge.
 - e. V161 grid and cathode begin to fall toward -75v.
 - f. The change applied to Q164 base is inverted and greatly amplified in Q164.
 - g. Q173A emitter (driving the Horizontal Preamp, the delay pickoff, and the timing capacitor begin to run up).
 - h. Q173B emitter (driving the A SWEEP out and the hold-off circuit begins to run up).
 - i. The amplified change (positive going ramp) is fed back to the top of the timing cap, opposing the change on V161 grid.
 - (1) V161 grid change is opposed.
 - (2) The grid will change less than 70 mv.
 - (3) The grid change depends on system gain.
 - j. As the voltage drop across the timing resistor remains virtually constant, the current into the timing capacitor will be virtually constant.
 - k. A constant current into a capacitor will result in a linear ramp across it.
 - l. A linear output sweep ramp is assured.
12. RC network R156, C156 prevents the negative step from Q154 collector from becoming capacitively coupled across D159.

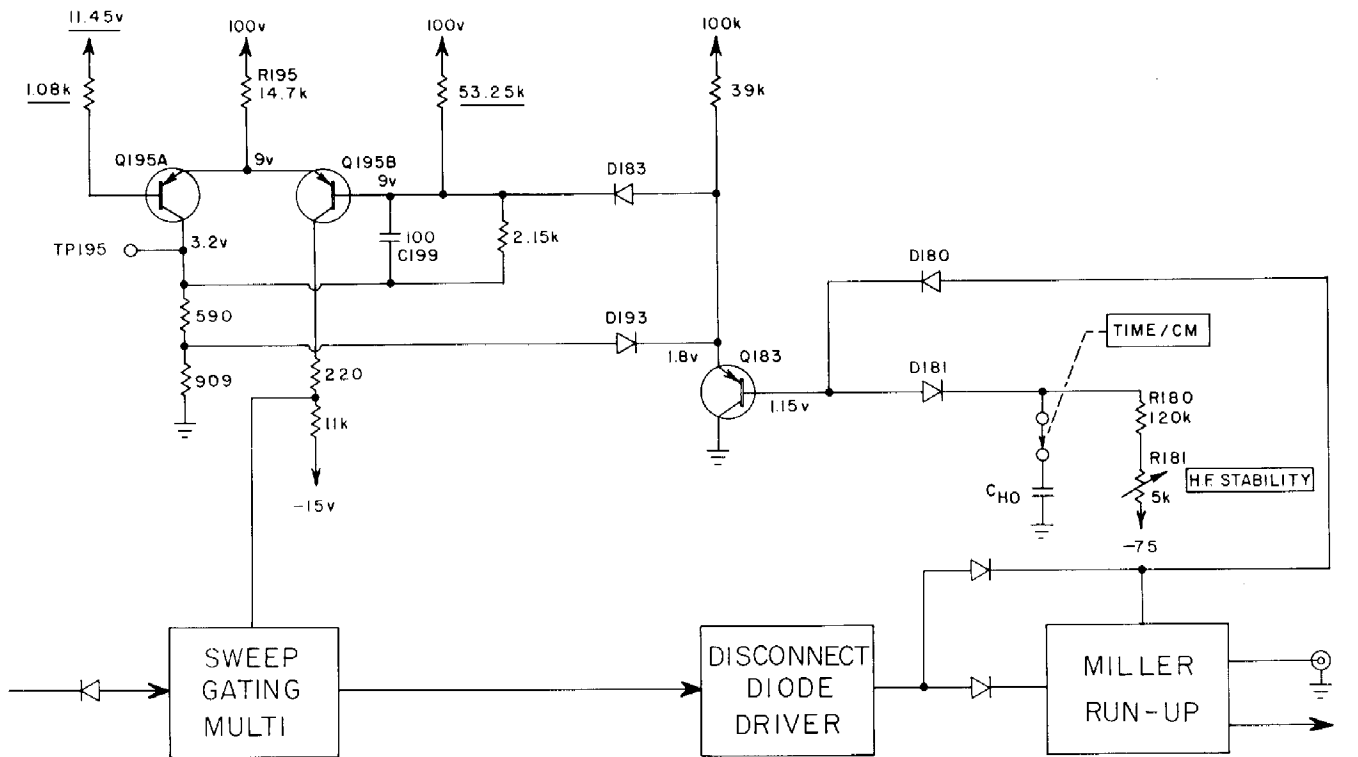
13. D163 protects Q164 from reverse emitter base breakdown damage if V161 opens.
 - a. BV_{EBO} is 4.5v.
14. Sequence of operation at the end of sweep.
 - a. As sweep reaches the required amplitude (10v), the sweep ramp flips Sweep Gating TD and Q154 collector raises to 1.6v.
 - b. D159 conducts.
 - c. Charging current into the timing capacitor is diverted through D159.
 - d. V161 grid pulls up to its quiescent level.
 - e. Retrace begins.
 - f. Timing capacitor discharge current flows through D159, Q154 and R154 to +15v.
15. As retrace ends, D158 conducts.
 - a. Added current through R154 pulls Q154 emitter down to 3.7v (from 3.75v).
 - b. Q154 collector drops to 1.2v (from 1.6v).
16. D158 clamps the output circuit (TP173) to 2.2v.
 - a. D158 also clamps (through Q173B) the A SWEEP out at 0v.
17. Various resistors and RC networks in the Miller circuit and timing switch prevent oscillations at some sweep speeds.
 - a. R177, R176, R172, R173, C165, R171, C171 help suppress oscillations.

Type 11B2 Plug-In

1. Gate Enabling Multi and Hold-Off

1. The Gate Enabling Multi is a bistable multi.

- a. In the quiescent state, Q195B draws 6.15 ma from the sweep Gating TD circuit (and from R196).
- b. At the end of sweep, it draws zero current from the TD circuit causing the TD to flip to its low state.
- c. At the end of hold-off it returns to its quiescent state -- it allows (enables) the Sweep Gate to accept a trigger.



TYPE 11B2 'A' SWEEP GENERATOR
GATE ENABLING MULTI AND HOLD OFF

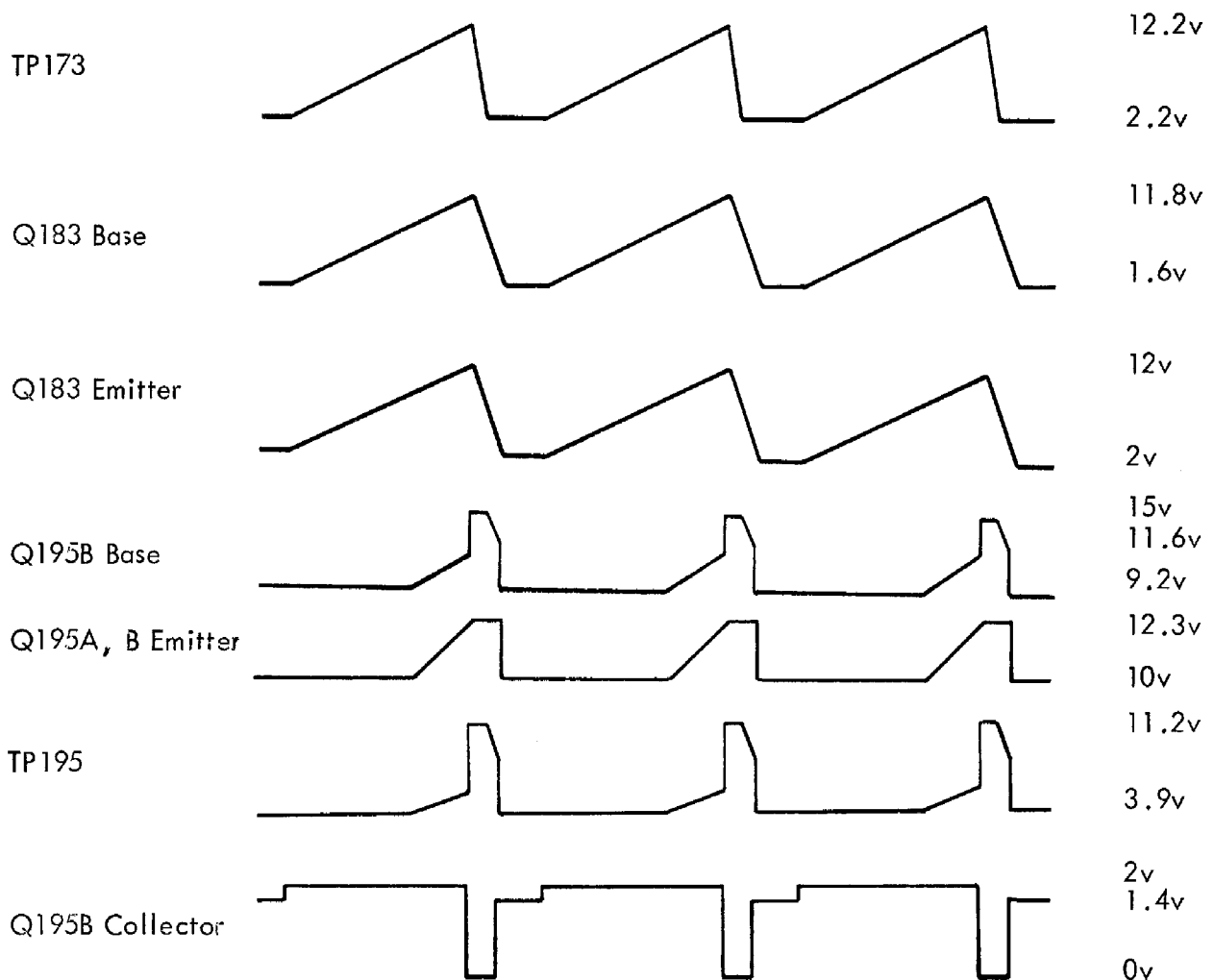
B-11B2-0024x
12-2-'63

2. The circuit is composed of two multi transistors, a hold-off EF transistor, and four diodes.

- a. Q195A and Q195B are 151-122, selected Fairchild S5909 silicon PNP transistors.

Type 11B2 Plug-In

- b. Q183, the hold-off EF, is a 151-087, a selected TI J3138 silicon PNP transistor.
- c. D180, D181, D183, D193 are GE IN 3605 diodes.
- 3. In the quiescent state, Q195B is conducting and Q195A is cut off.
- 4. Q183 is conducting, D180 is conducting.
- 5. Quiescent levels Q183, Q195A, Q195B.
 - a. Q183 base, 1.15v.
 - b. Q183 emitter, 1.8v.
 - c. Q195B base, 9v.
 - d. Q195A, Q195B emitters, 9v.
 - e. Q195A collector, 3.2v.
- 6. Sequence of operation during sweep.



Type 11B2 Plug-In

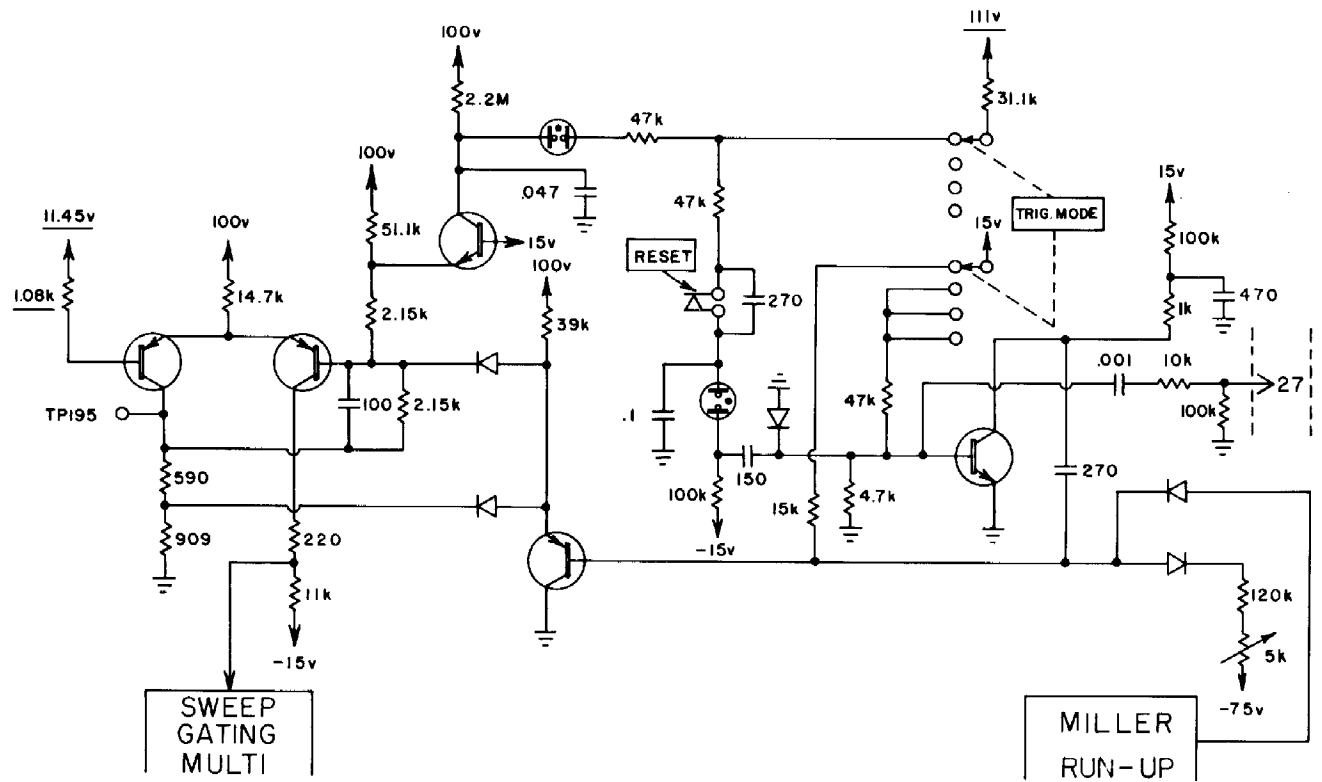
- a. The positive going sweep ramp passes through D180 and Q183 and appears at Q183 emitter.
 - (1) The hold-off cap charges to 11v (ramp maximum).
- b. Quiescently Q195B base sets at 9v.
 - (1) D183 comes into conduction as the sweep ramp reaches 9v.
- c. As the ramp continues to rise, Q195B base and Q195B emitter follow the ramp.
- d. Q195A base sets at 11.45v.
- e. As Q195A emitter (and Q195B emitter) reaches this level, Q195A begins to conduct.
- f. Q195A collector pulls up, lifting Q195B base (through C199) out of conduction.
 - (1) Emitter current through R195 is diverted to Q195A.
- g. The Bistable Multi flips.
 - (1) Q195A conducts, Q195B is cut off.
 - (2) As Q195A goes into full conduction, its collector rises to 11v allowing Q195B base to rise to 14.5v.
 - (3) D183 cuts off.
7. The Sweep Gating Multi TD current path through Q195B is open.
 - a. The TD flips to its low state, stopping sweep.
 - b. Retrace begins.
8. Sequence of operation at end of trace.
 - a. As retrace starts, the charge on the hold-off cap holds D180 cathode while the falling retrace waveform on the anode cuts off the diode.

Type 11B2 Plug-In

- b. The hold-off cap begins to discharge through R180 and R181.
 - c. As Q183 emitter drops to 6.8v, D193 conducts.
 - d. The hold-off waveform continues down; Q195A collector and Q195B base follows.
 - e. As Q195B base reaches the emitter potential of 11.4v, Q195B begins to conduct.
 - f. Q195A emitter is pulled below its base cutting it off.
 - g. The multi flips.
- 9. The multi has returned to its quiescent state.
 - 10. With Q195B conducting, it draws current from the Sweep Gating TD circuit, returning it to its 3 ma triggerable state.
 - 11. D181 has a function only in the Single Sweep Mode.
 - 12. The HF STABILITY control permits the operator to vary hold-off time.
 - a. As Q195B turns on after hold-off, a short but significant amount of time is required for the current through D125 to reach the triggerable level.
 - b. At triggering signals above 10 ma, triggering may become erratic (jitter horizontally).
 - c. The operator can advance or delay the end of hold-off (Q195B turn on time).
 - d. The coincidence of the TD becoming triggerable and the arrival of a trigger can be adjusted to reduce or eliminate jitter.

Type 11B2 Plug-In

J. SINGLE SWEEP and RESET Light Circuits



TYPE 11B2 'A' SWEEP GENERATOR
SINGLE SWEEP AND READY LIGHT CIRCUIT

B-11B2-0025
12-4-'63 jg

Type 11B2 Plug-In

1. In the SINGLE SWEEP mode of the TRIGGER MODE switch, sweep cannot occur until the RESET button is pushed.
 - a. The RESET light will light.
 - b. The next trigger will initiate sweep.
 - c. When sweep is started the light will extinguish.
 - d. At the end of one sweep the system returns to its quiescent condition.
2. The circuit consists of transistors Q204 and Q184, a diode and two neons.
 - a. Q184 is a 151-196 selected RCA (or Fairchild) 2N1938 silicon NPN switching transistor.
 - b. Q204 is a 151-103 selected Motorola 2N2219 silicon NPN transistor.
 - c. B186 is a NE-2V indicator neon (RESET light) housed in the RESET switch push-button.
 - (1) A blunt nose neon for visual indication.
 - (2) Exciting voltage 90v.
 - (3) Maintaining voltage 46v - 78v.
 - d. B200 is a NE-2V neon.
3. In the SINGLE SWEEP mode the top of R182 is connected to 15v.
 - a. Q183 base sets at 5.8v.
4. Q195B is cut off, Q195A is conducting, Q204 is cut off, Q183 is conducting.
 - a. Note that the SINGLE SWEEP quiescent condition differs from the NORM quiescent condition.
5. Q195B is drawing no current from the Sweep Gating TD.
 - a. The TD is in its reverse bias state.
 - b. Triggers cannot flip the Sweep Gating TD.

Type 11B2 Plug-In

6. Quiescent DC voltages Q184, Q204, Q195B, Q183.
 - a. Q204 base, 0v.
 - b. Q204 collector, 15v.
 - c. Q183 base, 5.8v.
 - d. Q183 emitter, 6.7v.
 - e. Q195B base, 15v.
 - f. D193 anode, 6.9v.
 - g. Q184 emitter, 18v.
 - h. Q184 collector, 36v.
 - i. Q195B collector, 0v.
7. Quiescent DC voltages in the RESET switch circuit.
 - a. The bottom of B200 is 15v.
 - b. The top of B200 is at 0v.
 - c. The top of the RESET switch is 109v.
 - d. The junction of R188, R189A and R189B is 109v.
8. Sequence of operation as the RESET switch is pressed.

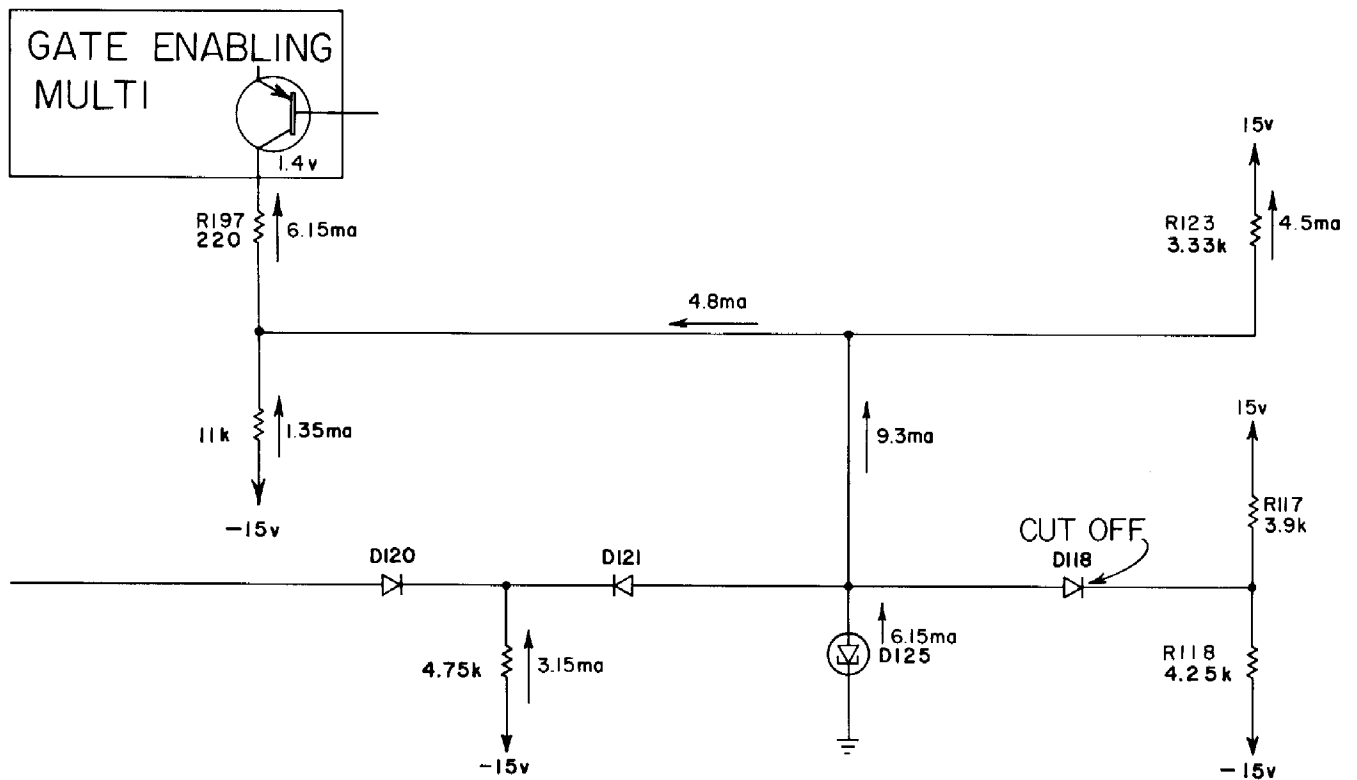
Type 11B2 Plug-In

- a. A voltage divider is formed consisting of R200, B200, R188 and R189A and R189B in parallel.
 - b. The top of R188 drops to 90v.
 - c. The top of the B200 raises to 76v.
 - d. The neon ignites.
 - e. The bottom of the neon raises to 22v.
 - f. A positive pulse turns on Q204 and drives it to saturation.
 - g. Q204 collector drops from 15v to zero for the duration of the pulse.
 - h. D181 disconnects momentarily preventing the pulse from returning to ground through the hold-off cap.
 - i. The negative going pulse drives Q183 into conduction.
 - j. As Q183 emitter drops, the negative pulse passes through D193, R193, C199 to Q195B base.
 - k. Q195B base is pulled down into conduction.
 - l. The multi flips.
 - m. Q184 turns on as the emitter is pulled down to 14.5v.
 - n. Q184 collector drops to 14.5v.
 - o. B186, the RESET light ignites.
9. As Q195B goes into conduction, it draws current (6.15 ma, 1.35 ma through R196 and 4.8 ma from the TD circuit).
- a. The TD returns to its triggerable state.
 - b. A trigger will flip the multi and start the sweep.
10. At the end of sweep the Gate Enabling Multi will flip as in the NORMAL mode.
- a. The Sweep Gating TD will return to its reverse bias (locked out) condition.
 - b. B186 turns off.

Type 11B2 Plug-In

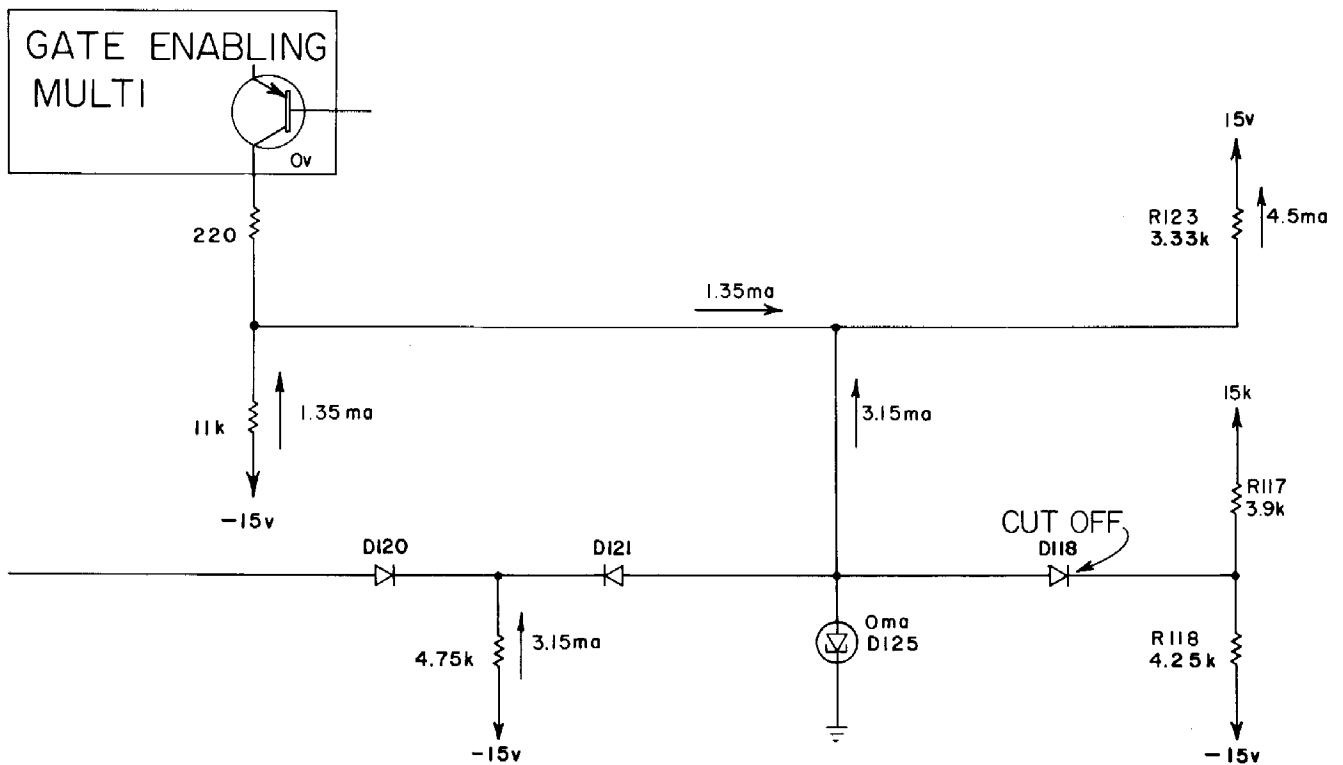
11. As hold-off begins and Q183 base begins to drop, the base cannot drop below 5.8v.
 - a. The divider, composed of R182, D181, R180 and R181 sets this level.
12. Because hold-off cannot be completed, the Gate Enabling Multi cannot return the Sweep Gating Multi TD to its triggerable condition.
13. The circuit has returned to its SINGLE SWEEP quiescent condition.

K. Free Run Mode



Type 11B2 Plug-In

1. In the Free Run mode of the TRIG MODE switch, the top of R117 is connected to 15v.
 - a. D118 cathode is lifted to cut off.
 - b. The 3.15 ma through R118 is diverted through R117.
 - c. 3.15 ma has been removed from the TD circuit.
2. When (at the end of hold-off) the Gate Enabling Multi draws 6.5 ma from the TD circuit, 6.15 ma must flow through the TD (D125).
3. 6.15 ma will flip the TD into its high state, starting sweep.
 - a. A trigger is not required.
4. At the end of sweep when the Gate Enabling Multi flips and draws no current from the TD circuit, no current flows through the TD.



Type 11B2 Plug-In

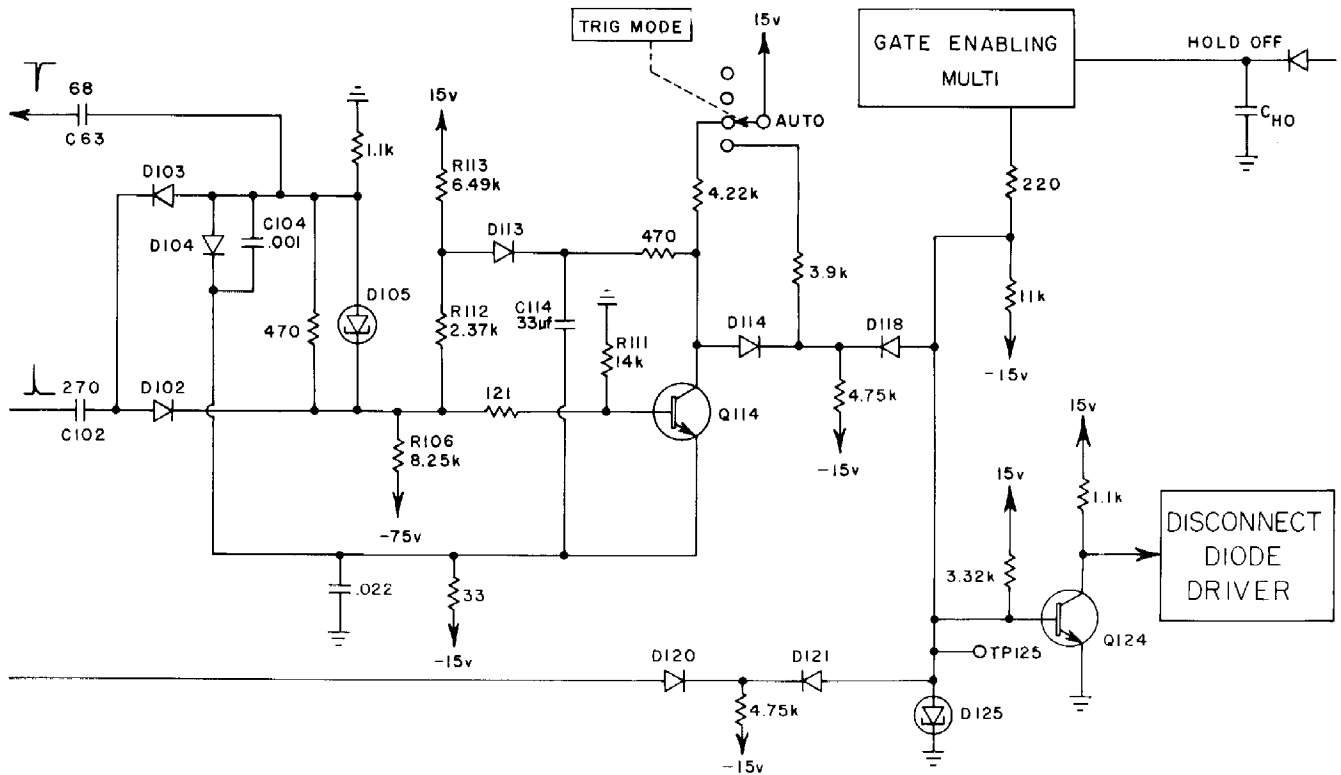
- a. The TD flips to its low state.
 - b. Sweep is stopped and retrace begins.
5. The circuit will free run at a rate set by the TIME/CM switch.

L. AUTO Circuit

1. When in the AUTO mode, the AUTO circuit causes the Sweep circuit to free run in the absence of triggers.
2. When triggers are present (at least one trigger every 80 msec), the Sweep circuit responds to triggers in the same manner as in the NORMAL mode.
3. Conduction or non-conduction of D118 determines the free run or triggered operation.
 - a. When D118 conducts, the Sweep Gating Multi requires a trigger to start sweep.
 - b. When D118 is cut off, the Sweep will free run (see section on FREE RUN operation).

Type 11B2 Plug-In

4. The circuit is composed of a transistor, a tunnel diode and six signal diodes.



TYPE 11B2 'A' SWEEP GENERATOR
AUTO MULTI

B-11B2-0026x
12-5-'63 jg

- a. Q114 is a 151-103 selected Motorola 2N2219 silicon NPN transistor.
- b. D105 is a GE STD 704 4.7 ma tunnel diode.
- c. D102 and D103 are Hughes HD5000 silicon diodes.
- d. D104, D113, D114 and D118 are GE 1N3605 silicon diodes.

Type 11B2 Plug-In

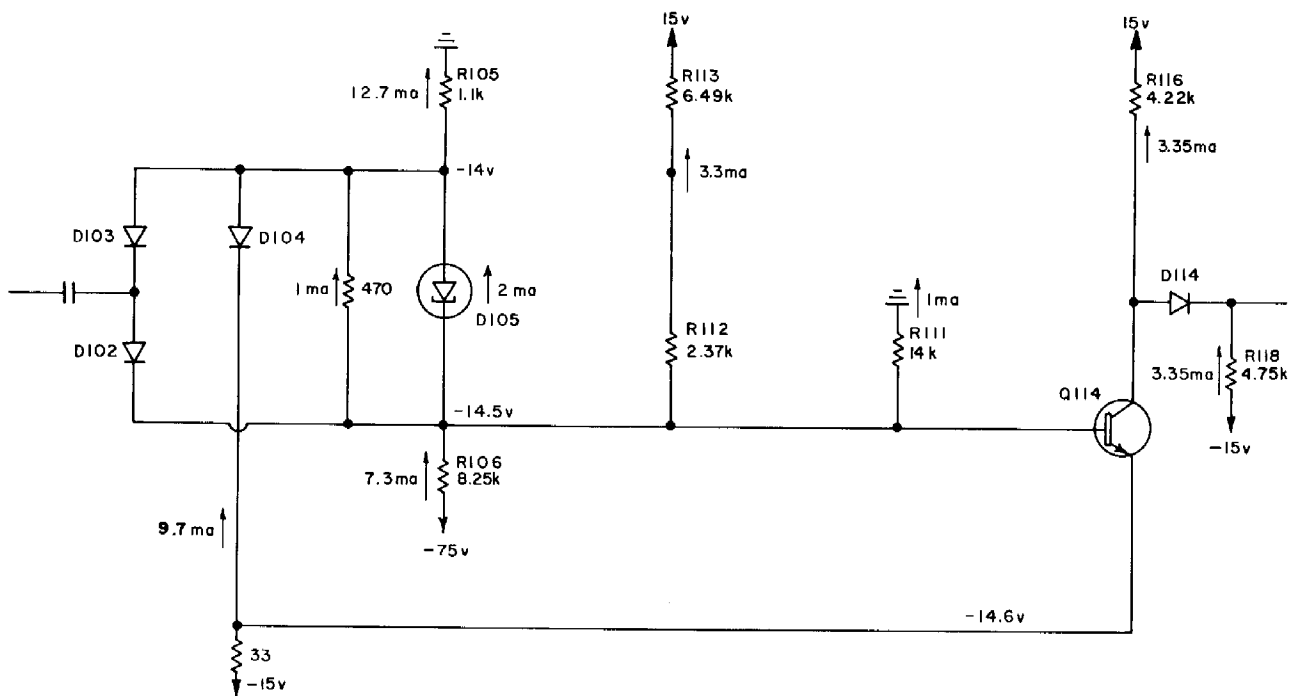
5. Quiescent conditions (AUTO MODE and no triggers).

- a. Q114 is cut off.
- b. D105 is in its high state.
(1) About 2 ma flowing*.
- c. D104 is conducting.
- d. D113 is cut off.
- e. D114 is conducting.
- f. D118 is cut off.
- g. D102 and D103 are barely conducting.

6. Quiescent voltages, Q114, D105.

- a. Q114 Base, -14.5v.
- b. Q114 emitter, -14.6v.
- c. Q114 collector, 1.1v.
- d. Q105 anode, 14v.

7. Current distribution in the quiescent state.



* See Curve in Appendix.

Type 11B2 Plug-In

- a. 7.3 ma through R106 supplies the TD circuit.
 - b. 3.3 ma flows through R112 and R113 to 15v.
 - c. 1 ma flows through R111 to ground.
 - d. 2 ma flows through the TD.
8. With D118 open, the Sweep Circuit will free run.
9. Sequence of operation as a trigger arrives.
- a. Positive going current trigger pulse pulls D102 into heavy conduction and cuts off D103.
 - b. TD current is diverted through D102.
 - c. The TD flips to its low state.
 - (1) Current below .5 ma will flip the TD.
 - d. The TD anode drops about 50 mv.
 - e. The TD cathode raises about 500 mv.
 - f. The 500 mv positive step biases Q114 to conduction.
 - g. Q114 collector drops to -14v.
 - h. D114 cuts off.
 - i. D118 conducts.
10. With D118 conducting, the Sweep circuit returns to its triggerable state.
- a. 3.16 ma through D118 decreases the Sweep Gating TD current to 3 ma.
 - b. A trigger will flip the TD and start sweep.
11. As Q114 collector reaches -6.4v (on the way to -14v), D113 conducts.
- a. D113 anode (and the top of R112) is pulled down to -13.4.

Type 11B2 Plug-In

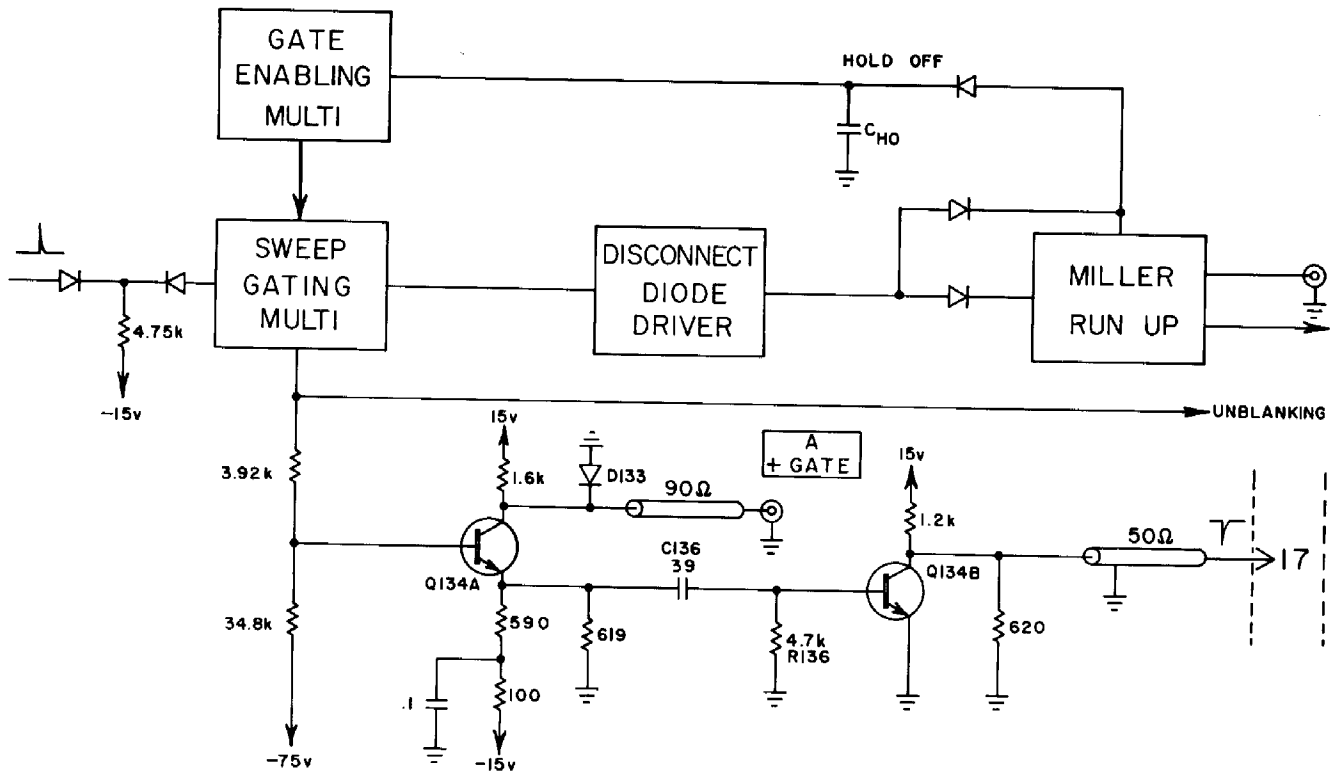
- b. With no voltage drop across R112, 5.3 ma flows through the TD.
- c. The TD flips to its high state.
 - (1) 4.7 ma will flip the TD to its high state.
- 12. As Q114 collector drops to -14v, C114 changes to this value.
- 13. If triggers continue to arrive at less than 80 msec apart, C114 will maintain enough charge to keep D114 cut off and D118 conducting.
 - a. The Sweep Circuit will operate in its triggerable condition.
- 14. D103 functions as a DC restorer allowing C102 to charge between triggers.
- 15. D104 provides temperature compensation for Q114 and maintains a low impedance point for D105 anode.
 - a. D104 conducts under all conditions.
 - b. C104 prevents the fast TD switching spike from cutting off D104.
- 16. The connection from C63 Trigger Generator provides a close loop ground for Q64 emitter bypass capacitor, C63.

M. ALTERNATE TRACE AMP

- 1. The Alternate Trace Amplifier supplies a negative going 5v trigger to the 10A2 dual trace switching circuit.
 - a. Pulse is fed to pin 17 blue ribbon connector.
 - b. Pulse must be coincident with end of sweep.

Type 11B2 Plug-In

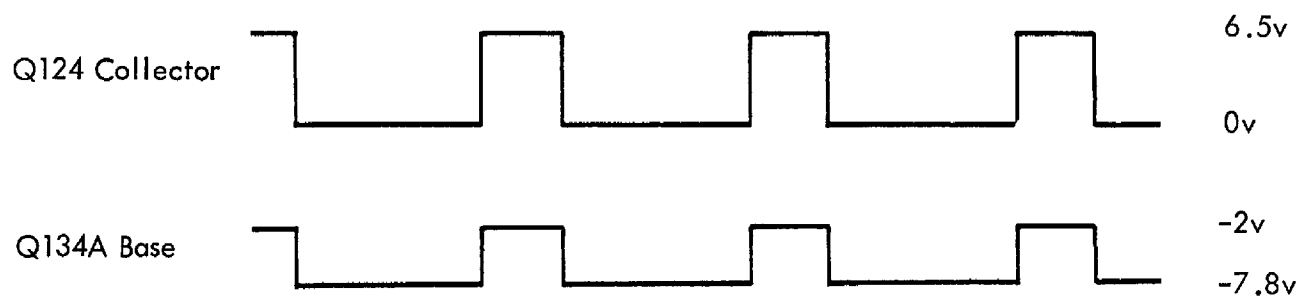
2. The circuit also provides a 15v A + GATE waveform and a 6.5v unblanking pulse.



3. The circuit consists of two transistors and a clamping diode.
- a. Q134A and Q134B are 151-108 selected Motorola silicon NPN transistors (2N2501).
 - b. D133 is a GE 1N3605 silicon diode.

Type 11B2 Plug-In

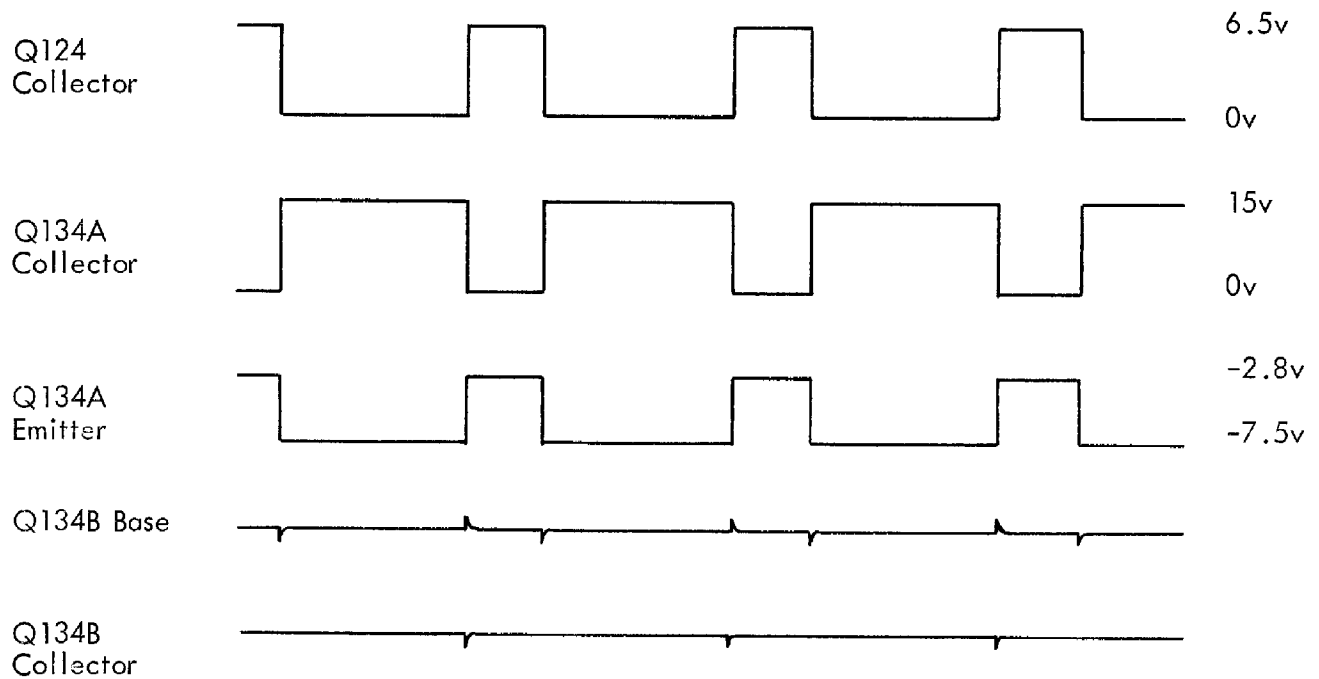
4. The waveform at Q124 collector supplies the Alternate Trace Amp.



- a. The 6.5v waveform supplies the unblanking circuit.
 - b. The waveform is 0v during sweep and +6.5v when no sweep occurs.
 - c. The waveform is attenuated to 5.8v peak-to-peak at Q134A base.
 - (1) -7.8v during sweep.
 - (2) -2v between sweeps.
5. Quiescent voltages Q134A, Q134B (no sweep).
- a. Q134A base, -2v.
 - b. Q134A emitter, -2.8v.
 - c. Q134A collector, 0v.
 - d. Q134B base, 0v.
 - e. Q134B collector, 5v.

Type 11B2 Plug-In

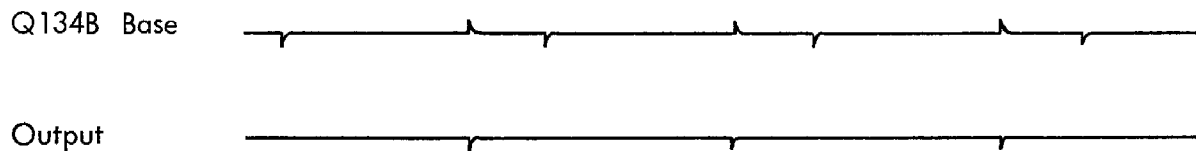
6. In the quiescent condition, Q134A is conducting and Q134B is cut off.
 - a. Q134A collector is clamped at ground by D133.
 - b. Q134B collector 5v level is set by divider R138, R139.



7. At the beginning of sweep, Q134A base drops to -7.8v.
 - a. Q134A cuts off.
 - b. The emitter drops to -7.5v.
 - c. The collector raises to 15v.
 - d. The collector waveform is fed to the front panel A + GATE.

Type 11B2 Plug-In

- 8. The Q134A emitter waveform is differentiated in C136, R136.
 - a. $T_c = 183$ nsec.
- 9. The negative going pulse does not effect cut off Q134B.
- 10. The positive going pulse drives Q134B into saturation.
 - a. The collector drops to 0v for the duration of the pulse.
 - b. The output waveform is a negative going 5v pulse with a T_c of 183 nsec.



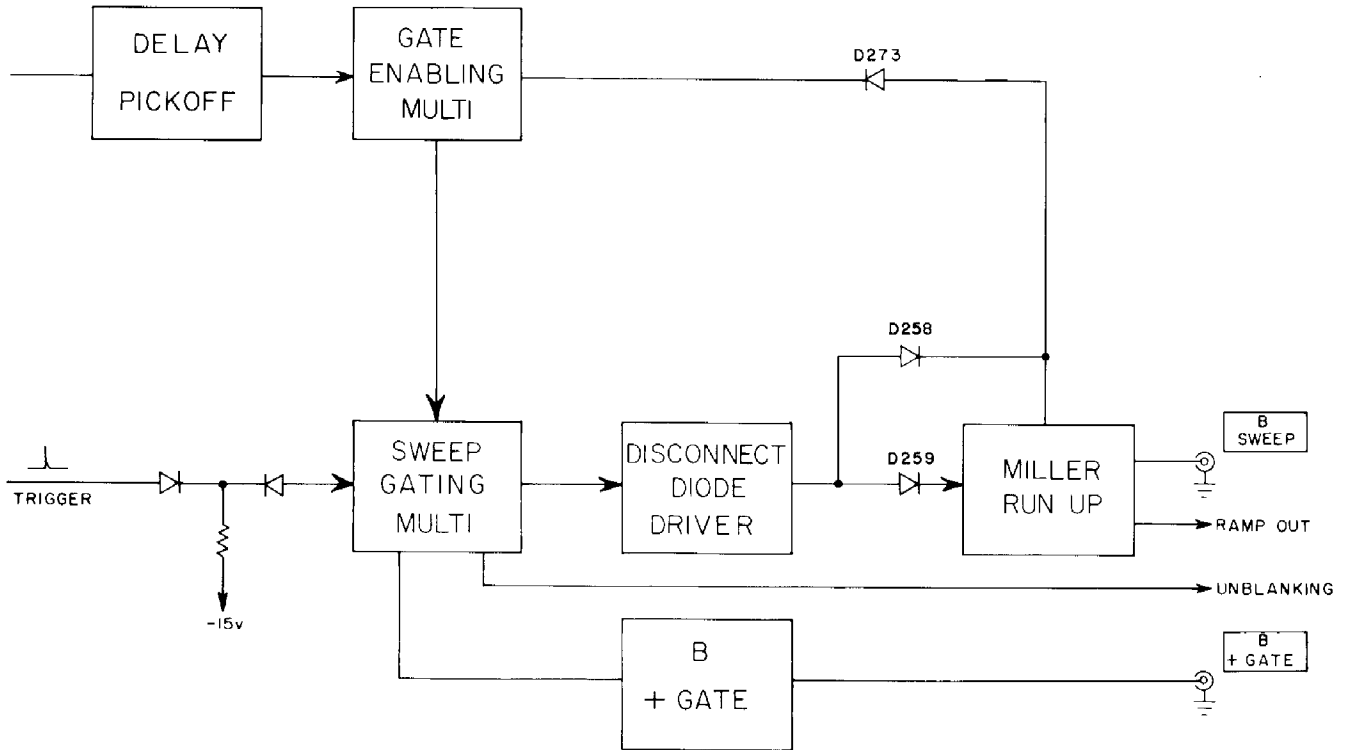
Type 11B2 Plug-In

IV. SWEEP GENERATOR B

- A. The Sweep Generator B is considered the Delaying Sweep.
- B. It supplies a linear sweep ramp to the Horizontal Preamp in the following HORIZ DISPLAY switch modes:
 - 1. B DELY'D BY A
 - 2. B DELY'D BY A (Triggered)
- C. Sweep Generator B provides an unblanking pulse to the CRT in these modes:
 - 1. B DELY'D BY A
 - 2. A INTENS BY B
 - 3. B DELY'D BY A (Triggered)
 - 4. B DELY'D BY B (Triggered)
- D. Outputs -- present in all by A mode of the HORIZ DISPLAY SW:
 - 1. "B" Sweep out (Front Panel Jack) - 10v.
 - 2. "B" + GATE out (Front Panel Jack) - 15v.
- E. Basic Circuits
 - 1. Sweep Gating Multi (TD circuit and Q224).
 - 2. Disconnect Diodes Driver Amp (Q254).
 - 3. Miller Run-Up.
 - 4. Gate Enabling Multi.
 - 5. Delay Pickoff.

Type 11B2 Plug-In

F. Block Diagram



TYPE 11B2 'B' SWEEP GENERATOR
BLOCK DIAGRAM

B-11B2-0033x
12-26-63 jg

Type 11B2 Plug-In

1. Block Logic, B DELY'D BY A (Non-Triggered):
 - a. After the start of A Sweep, at a time delay determined by the setting of the Delay Time Multiplier, a negative step appears at the Delay Pickoff output.
 - b. The step turns on Q295B in the Enabling Multi.
 - c. Enabling Multi current flips the Sweep Gating TD to its high state (no trigger required).
 - d. A negative step from the Sweep Gating circuit is amplified in the Disconnect Diode Driver Amp and appears at its output (Q254 collector).
 - e. The step turns off the disconnect diodes starting sweep.
 - f. The B Sweep ramp is fed to the Horizontal Preamp and through D273 to the Enabling Multi.
 - g. When the B Sweep ramp reaches proper amplitude, the Enabling Multi flips.
 - (1) Should the A and B TIME/CM switches be set to allow the B Sweep to run beyond the end of A Sweep, the Delay Pickoff will flip the Enabling Multi at the end of A Sweep.
 - (2) In this case, D273 may not come into conduction and the sweep ramp does not reach the Enabling Multi.
 - h. As the Enabling Multi flips, its current requirement from the TD drops to zero.
 - i. The TD flips to its low state.
 - j. The positive step from the Sweep Gating output (Q224 collector) is amplified in the Disconnect Diode Driver Amp.

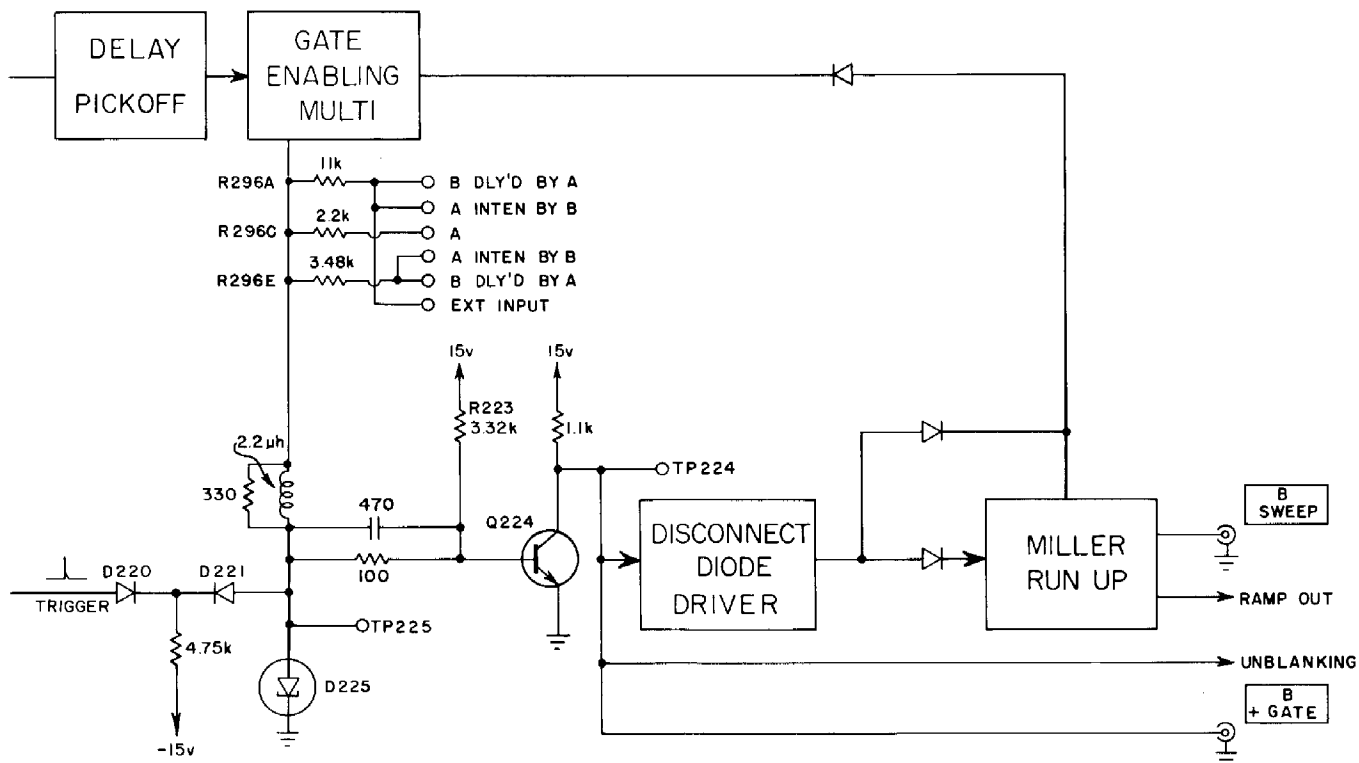
Type 11B2 Plug-In

- k. The positive going step at the Disconnect Driver output brings the Disconnect Diode (D259) into conduction.
 - l. Sweep stops and retrace starts.
 - (1) Hold-off is not necessary as B Sweep cannot start again until A Sweep has delayed the start.
 - m. When retrace is completed, D258 conducts clamping the start of sweep.
 - n. Although retrace is completed, the Sweep Enabling Multi cannot turn on until the next signal from the Delay Pickoff arrives.
2. Block Logic, A INTENS BY B (Non-Triggered):
- a. Circuit operation is the same as B DELY'D BY A except the Sweep ramp is not fed to the Horizontal Preamp.
 - b. Unblanking waveform is fed to the CRT.
 - c. B + GATE and B SWEEP out are present.
3. Block Logic, A Mode:
- a. The Delay Pickoff will switch the Enabling Multi as in B DEL'D BY A mode.
 - b. Currents in the TD circuit set by HORIZ DISPLAY switch are not adequate to flip the TD into its high state.
 - c. B Sweep cannot start.
4. Block Logic, A INTEN BY B (Triggered):
- a. Operation is the same as the A INTEN BY B non-triggered except that as the Enabling Multi turns on the Sweep Gating TD will not flip until a trigger arrives.

Type 11B2 Plug-In

- 5. Block Logic, B DELY'D BY A (Triggered):
 - a. Operation is the same as the B DELY'D BY A non-triggered except that the Enabling merely enables the Sweep Gating TD.
 - b. A trigger is required to flip the TD to its high state and start sweep.
- 6. Block Logic, EXT INPUT:
 - a. The circuit operates like in the B DELY'D BY A non-triggered mode.
 - b. The circuit free runs and cannot be triggered.
 - c. The unblanking waveform is not fed to the CRT.
 - (1) EXT HORIZ unblanking is explained as part of the 11B2 Interconnecting Plug discussion.
 - d. B + GATE and B Sweep are present.

B. Sweep Gating Multi (TD)

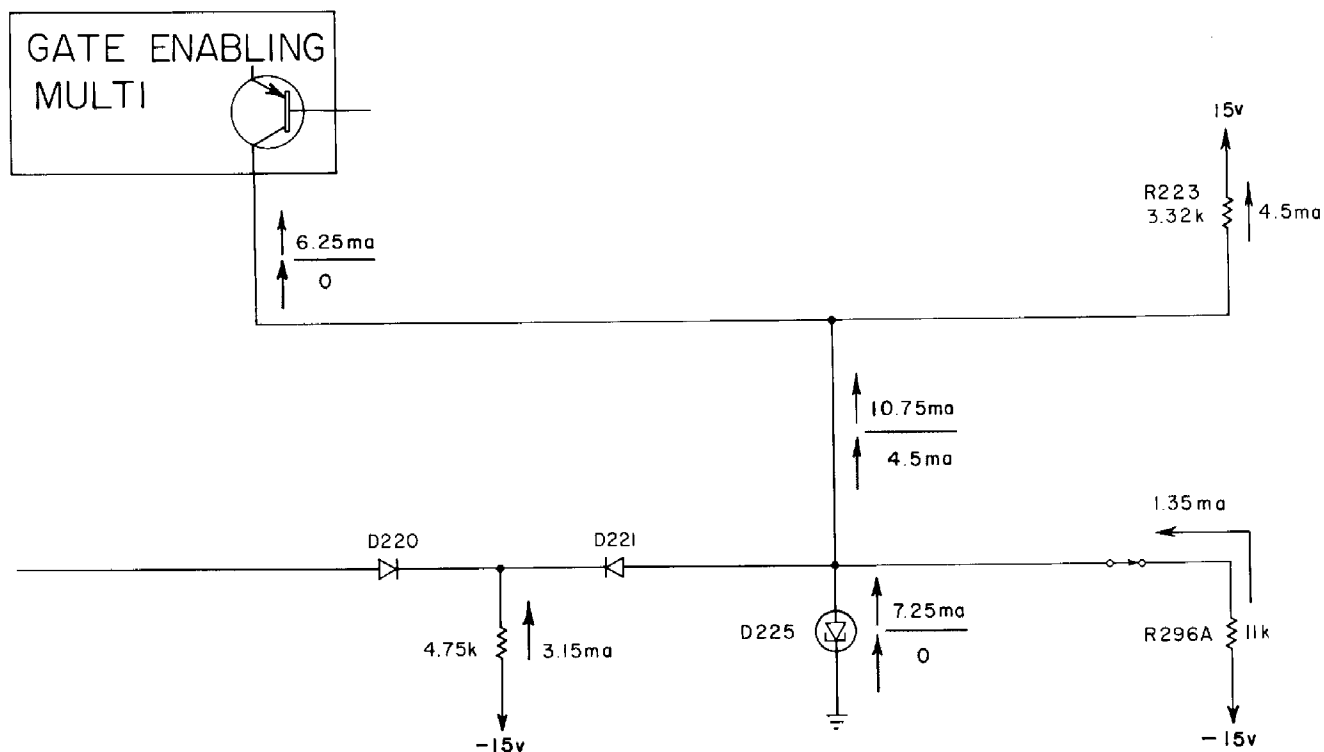


TYPE 11B2 'B' SWEEP GENERATOR
SWEEP GATING MULTI

B-11B2-0034x
12-26-63 jg

Type 11B2 Plug-In

1. Circuit operation is essentially the same as the A Sweep Gating Multi.
2. Current distribution, B DELY'D BY A (non-triggered), A INTEN BY B (non-triggered) and EXT INPUT modes.

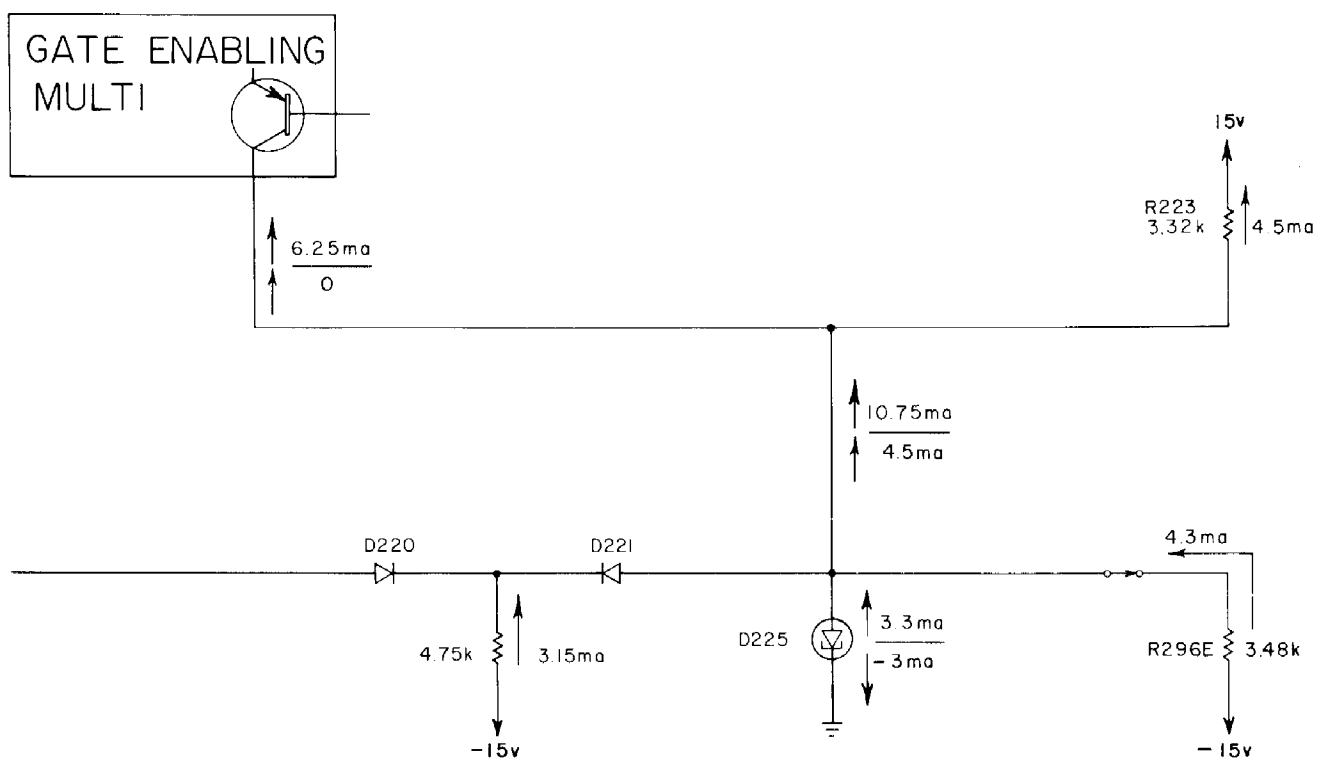


- a. Quiescently the Enabling Multi is turned off.
 - (1) No current flows from the TD circuit.
- b. 4.5 ma flows through R223.
- c. 3.15 ma flows through D221.
- d. 1.35 ma through R296A.
- e. No current flows through the TD.
 - (1) The TD is in its low state.

Type 11B2 Plug-In

- f. Should a trigger arrive and cut off D221, the TD will draw only 3.15 ma.
 - (1) 4.7 ma is required to flip the TD.
 - (2) It will remain in its low state.
- g. When the Enabling Multi turns on it draws 6.25 ma from the TD circuit.
- h. 7.25 ma through the TD will flip it to its high state.
- i. A trigger is not required.

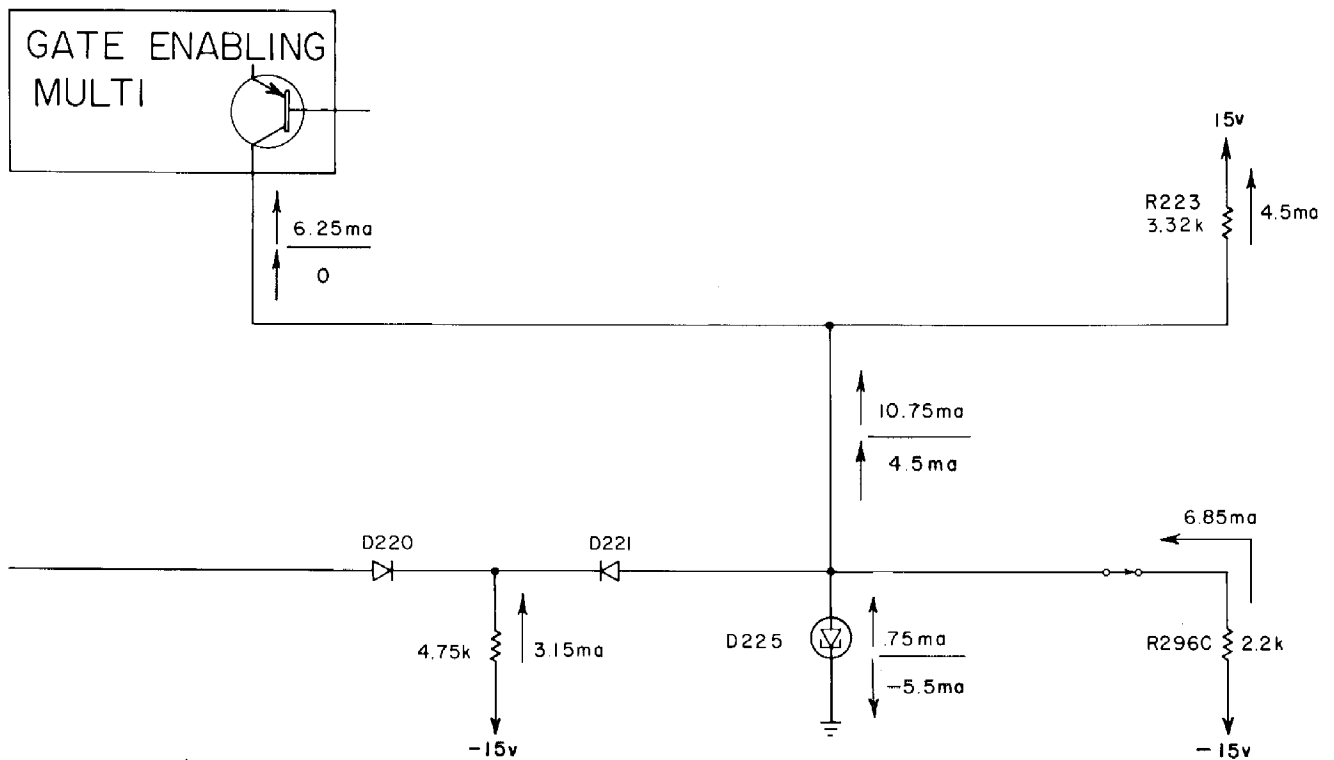
3. Current distribution, B DELY'D BY A (Triggered) and A INTENS BY B (Triggered):



- a. Quiescently the Enabling Multi is turned off.
 - (1) No current flows from the TD circuit.
- b. 4.5 ma flows through R223.

Type 11B2 Plug-In

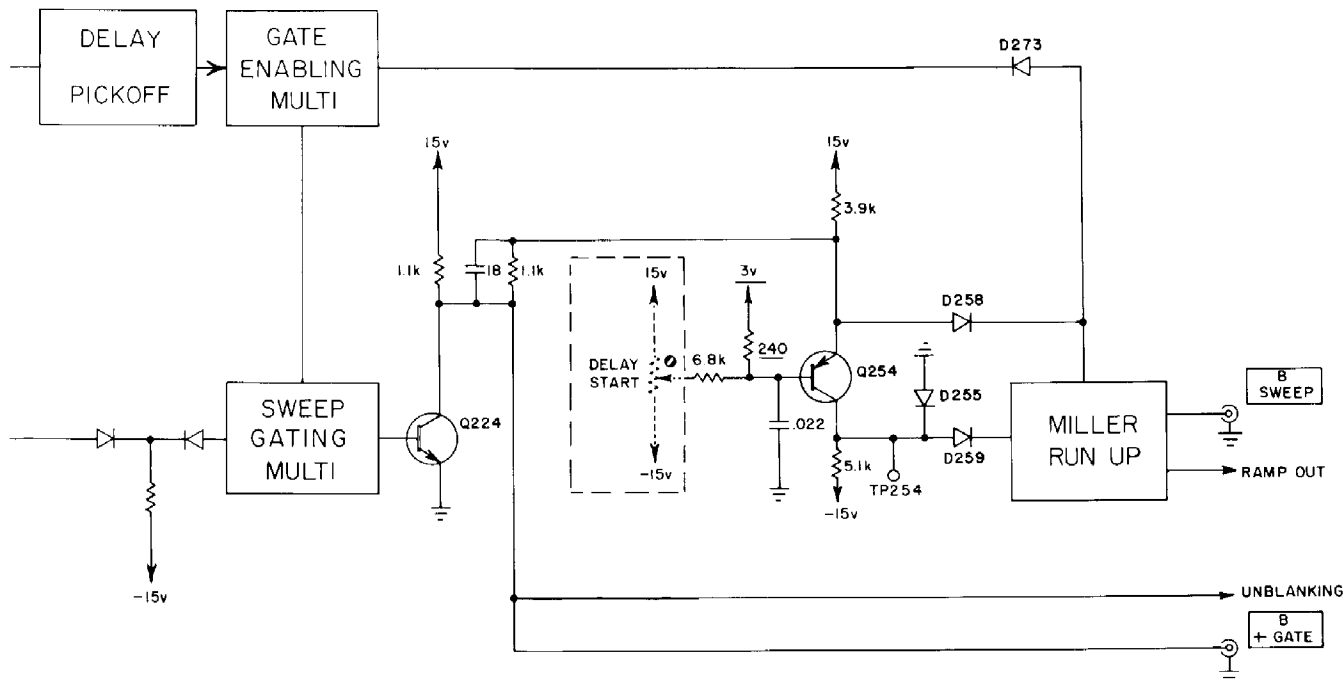
- c. 3.15 ma flows through D221.
 - d. 4.3 ma flows through R296E.
 - e. 4 ma of reverse current flows through the TD.
 - (1) The TD is in its low state.
 - (2) A trigger cannot flip the TD to its high state.
 - f. When the Enabling Multi is turned on it draws 6.25 ma from the TD circuit.
 - g. 3.3 ma forward current now flowing through the TD places it in the triggerable state.
 - h. As a trigger arrives, D221 disconnects.
 - (1) There is now 6.45 ma flowing through the TD.
 - (2) It will flip to its high state.
4. Current distribution in A mode.



Type 11B2 Plug-In

- a. 6.85 ma flows through R296C.
 - b. With the Enabling Multi off, the TD has 5.5 ma of reverse current .
 - (1) It is in a reverse bias low state.
 - c. When the Enabling Multi turns on, .75 ma flows through the TD.
 - d. In neither position of the Enabling Multi can a trigger flip the TD to its high state.
 - (1) A trigger will increase the forward TD current to 3.9 ma.
 - (2) 4.7 ma is required to flip the TD to its high state.
5. The output at Q224 collector is the same as in Sweep Generator A.

H. Disconnect Diode Driver Amp (Q254)



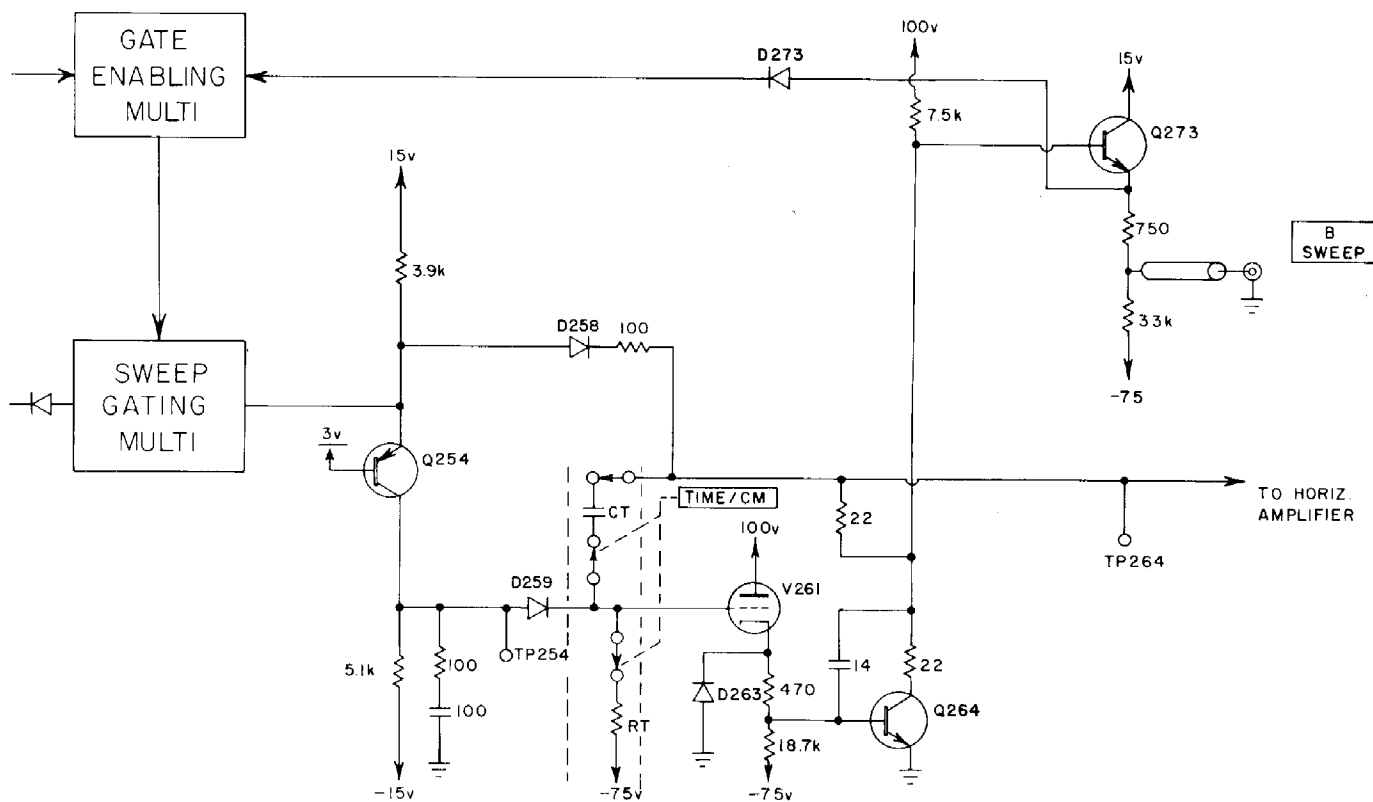
TYPE 11B2 'B' SWEEP GENERATOR
DIODE DRIVER

B-11B2-0035x
12-26-63 jg

Type 11B2 Plug-In

1. All components, circuit configurations, DC voltages and signal values are the same as Sweep Generator A.
2. The DELAY START control (SWEEP GENERATOR A) is common to both A and B Sweeps.

I. Miller Run-Up



TYPE 11B2 'B' SWEEP GENERATOR
MILLER RUN UP

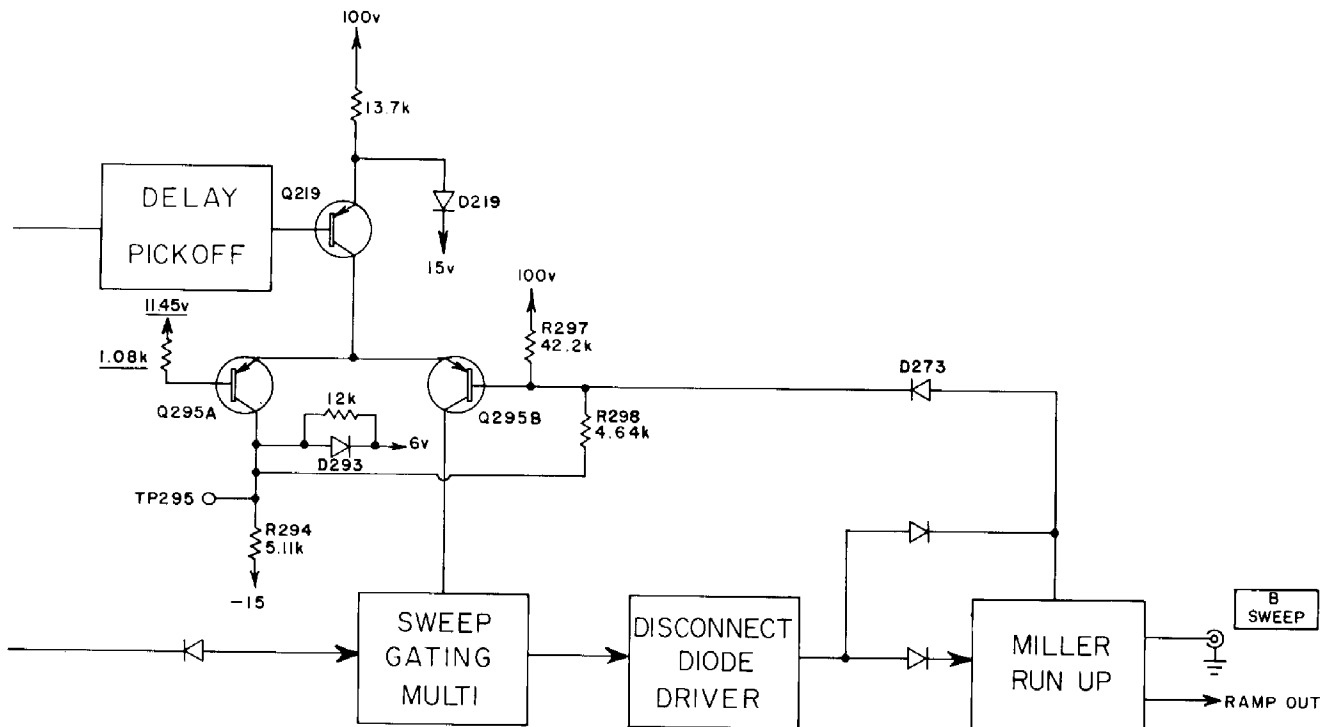
B-11B2-0036 x
12-26-'63 jg

Type 11B2 Plug-In

1. The disconnect diode, input nuvistor and Miller amplifier transistor circuits are the same as Sweep Generator A.
2. Only one output EF is used.
 - a. An EF is not required for drive to the Horizontal Preamp.
 - b. An EF is required in Sweep Generator A to drive the Delay Pickoff circuit.

J. Gate Enabling Multi

1. The Gate Enabling Multi supplies a current load for the Sweep Gating Multi TD.
2. The Enabling Multi circuit is composed of a transistorized bistable multivibrator, Q295A, Q295B, a driver amplifier, Q219, and two diodes.
 - a. Q295A and Q295B are 151-087 General J7138 silicon PNP transistors.
 - b. Q219 is a 151-122, a selected Fairchild 55909 silicon PNP transistor.



TYPE 11B2 'B' SWEEP GENERATOR
GATE ENABLING MULTI

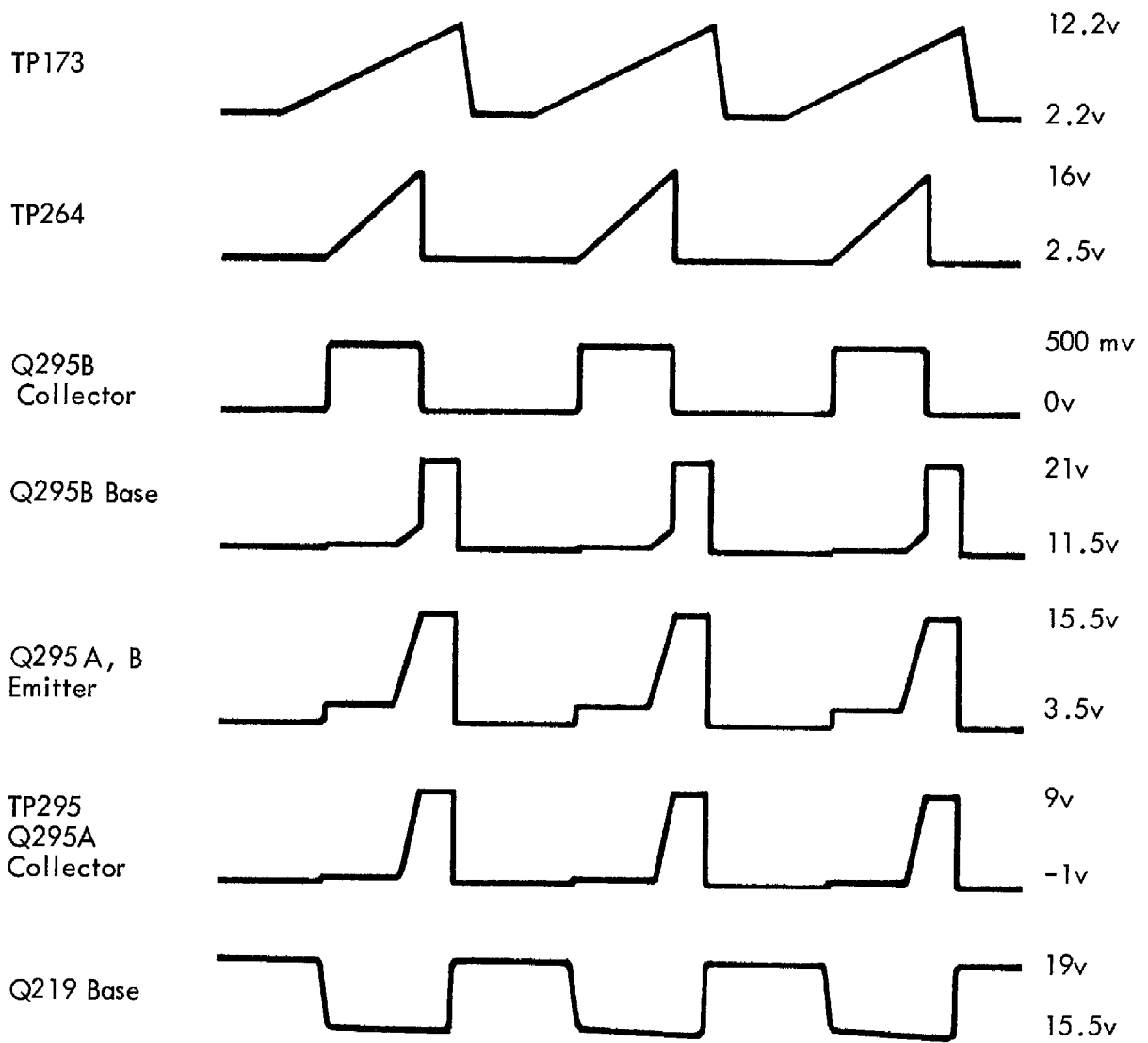
B-11B2-0037x
12-27-'63 jg

Type 11B2 Plug-In

3. When the multi is "turned on", Q295B is conducting.
 - a. It draws 6.25 ma from the TD circuit.
4. When it is "turned off", Q295B is not conducting.
 - a. It presents no load to the TD circuit.
5. The multi can be turned on by a negative step from the Delay Pickoff.
6. It can be turned off by the B Sweep ramp or a positive step from the Delay Pickoff, whichever comes first.
7. The multi will continue to flip with each A sweep in all modes; even in the A mode or EXT INPUT mode.
8. Static DC voltages, Q295A, Q295B and Q219.
 - a. Q295A base, 9v.
 - b. Q295A, Q295B emitters, Q219 collector, 2.2v.
 - c. Q295B collector, 0v.
 - d. Q295A collector, -1v.
 - e. Q295A base, 11.45v.
 - f. Q219 base, 16.1v.
 - g. Q219 emitter, 15.4v.
9. Sequence of operation:
 - a. In the quiescent condition, Q219 is cut off.
 - (1) Q295A and Q295B emitters are open.
 - (2) Scope reading using X1 probe (1 meg Z) is 2.2v on the emitters from the leakage current.
 - (3) Q219 emitter is held at 15.4 by D219.

Type 11B2 Plug-In

- b. Q295B collector is at 0v.
- c. A divider is composed of R294, R298, R297, setting Q295A collector and Q295B base levels.
- d. At a time set by the Delay Time Multiplier after the start of A Sweep, a negative step brings Q219 into conduction.
 - (1) Q219 emitter pulls down to 14v.

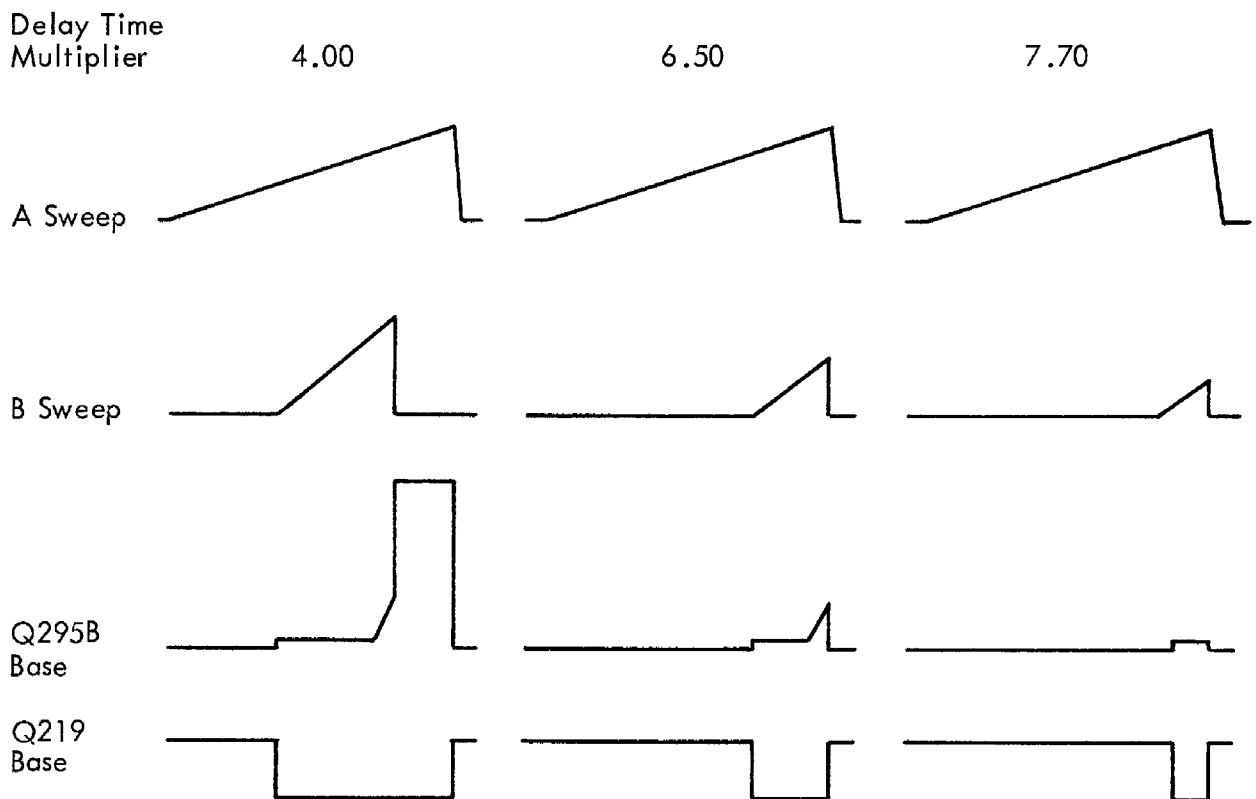


Type 11B2 Plug-In

- e. Q295B turns on.
 - (1) Q259 emitters raise to 9v.
- f. As Q295B turns on, 6.25 ma flows from the TD circuit.
 - (1) If the HORIZ DISPLAY switch is in the B DELY'D BY A or the A INTENS BY B (non-triggered) of the EXT INPUT mode, the Sweep Gating TD will flip to its high state and sweep will start.
 - (2) If in the B DELY'D BY A or A INTENS BY B (triggered) modes, the Sweep Gating Multi will be in its triggerable state, awaiting trigger.
 - (3) If in the A mode, there is no additional reaction in the Sweep Generator B.
- g. As the sweep ramp reaches 9v it lifts D273 into conduction.
 - (1) Q295B base follows.
 - (2) Q295 emitters follow Q295B base.
- h. When Q295A emitter reaches 11.4v, Q295A begins to conduct.
 - (1) Emitter current is transferred from Q295B to Q295A.
 - (2) The Multi flips.
 - (3) Q295B cuts off.
 - (4) Q295B collector current stops.
- i. The Sweep Gating TD returns to its low state and A Sweep stops.
- j. At the end of A Sweep, a positive step from the Delay Pickoff cuts off Q295A.

Type 11B2 Plug-In

- k. The Gate Enabling circuit has returned to its quiescent state.
 - l. As Q219 and Q295A cut off, Q295 emitters return to 2.2v only if a test scope with a 1M input Z is connected to this point.
10. Anti-wrap-around feature.
- a. If the Delay Time Multiplier is set to allow the B Sweep to run beyond the end of A Sweep, the anti-wrap-around feature begins to function.



Type 11B2 Plug-In

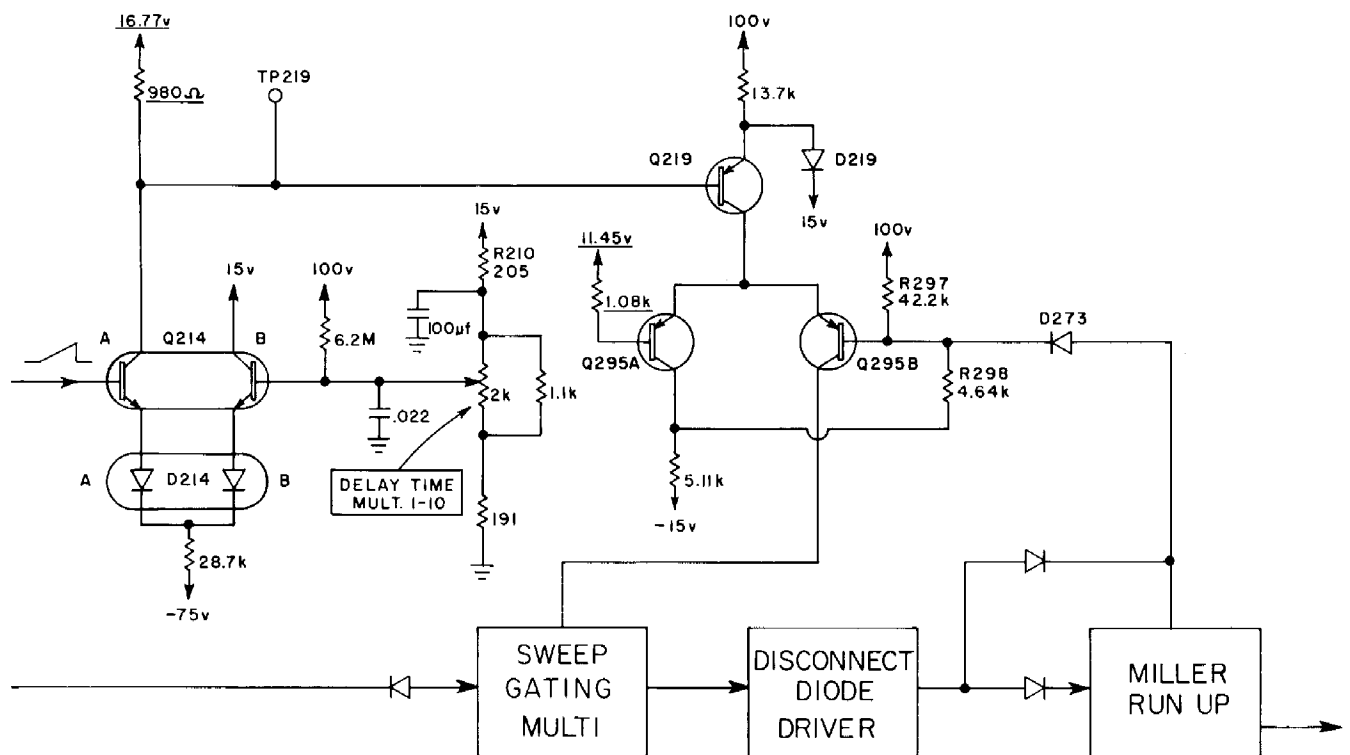
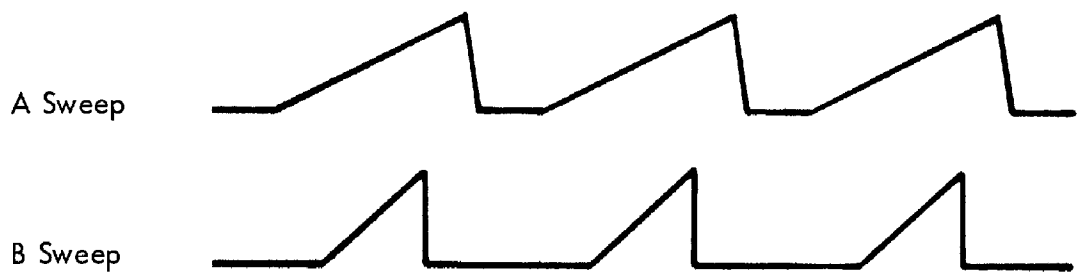
- b. The waveforms above illustrate conditions as the Delay Time Multiplier is advanced (delay increased).
- c. If the B Sweep ends before the end of A Sweep (4.00 on the Delay Time Multiplier in the illustration above), the Enabling Multi will flip when the Sweep ramp on Q295B base reaches 11.2v.
 - (1) Q295A conducts, its collector rises to 7v.
 - (2) Q295B base (divider R297, R298) rises to 16v.
 - (3) At the end of A Sweep when Q219 cuts off, Q295A collector drops to -1v.
 - (4) Q295B base drops to 9v.
- d. With the Delay Time Multiplier set at 6.50 (in the illustration above), the Sweep ramp at Q295B base does not quite reach the 11.2v necessary to flip the multi before the end of A Sweep.
 - (1) At the end of A Sweep, Q219 cuts off.
 - (2) Q295B is robbed of current.
 - (3) The Sweep Gating TD flips to its low state stopping sweep.
 - (4) Q295A does not conduct during the cycle.
- e. With the Delay Time Multiplier set to 7.70, the B Sweep ramp does not bring D273 into conduction (ramp does not reach 9v).
 - (1) The B Sweep ramp does not reach Q295B base before Q219 cuts off, ending sweep.

K. Delay Pickoff

- 1. The Delay Pickoff supplies a negative going waveform to the Enabling Multi.

Type 11B2 Plug-In

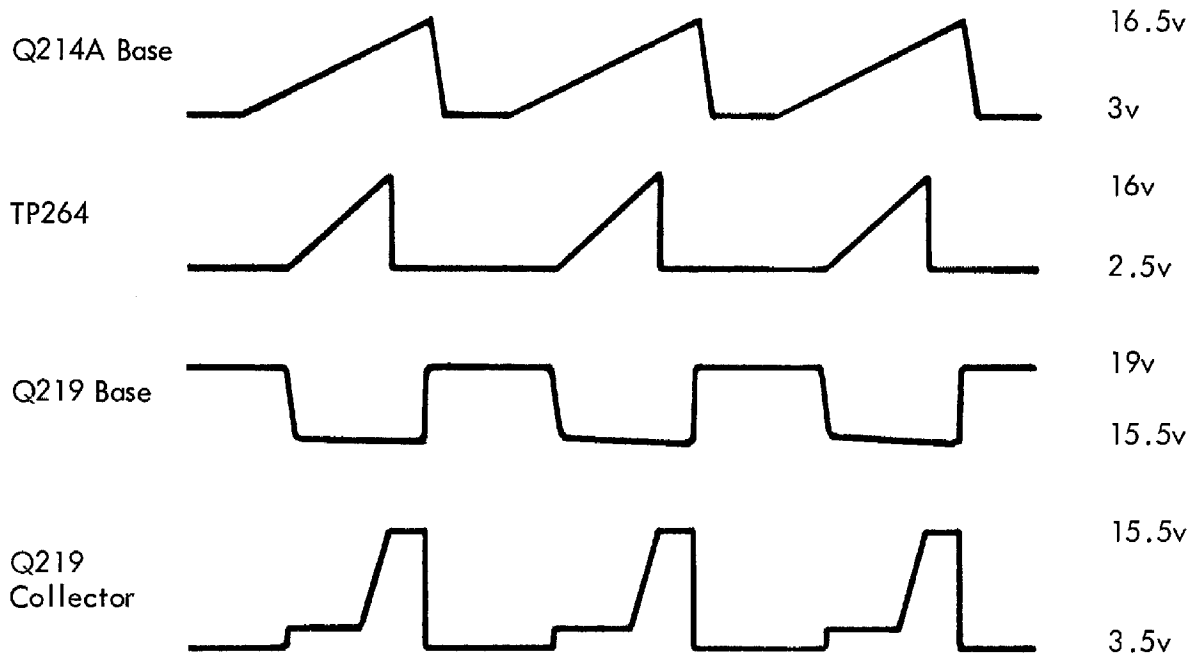
- a. The delay, after the start of A Sweep, is set by the DELAY TIME MULTIPLIER.
- b. The setting of the TIME/CM control is multiplied by the reading on the DELAY TIME MULTIPLIER dial to obtain delay time.
- c. As an example, the waveforms below were taken with A SWEEP TIME/CM at .5 msec/cm and the DTM at 3.80.
- d. $.5 \text{ msec/cm} \times 3.8 = 1.9 \text{ msec delay.}$



TYPE 11B2 'B' SWEEP GENERATOR
DELAY PICK OFF

Type 11B2 Plug-In

2. The circuit is composed of a dual transistor and a dual diode.
 - a. Q214 is 151-104, a selected Fairchild SP8481 dual silicon NPN transistor pair.
 - b. D214 is a pair of 1N3605 silicon diodes, encapsulated by Tek for uniform temperature compensation (Tek No. 152-151).
3. Static conditions, Q214, D214 (with DTM at 3.80).
 - a. Q214A base, 2v.
 - b. Q214B base, 6v (DTM at 3.80).
 - (1) A range from 2.5v to 12v with DTM settings.
 - c. Q214A collector, TP219, 16.1v.
 - d. D214 cathodes, 4v.
4. Sequence of operation (DTM at 3.8).



Type 11B2 Plug-In

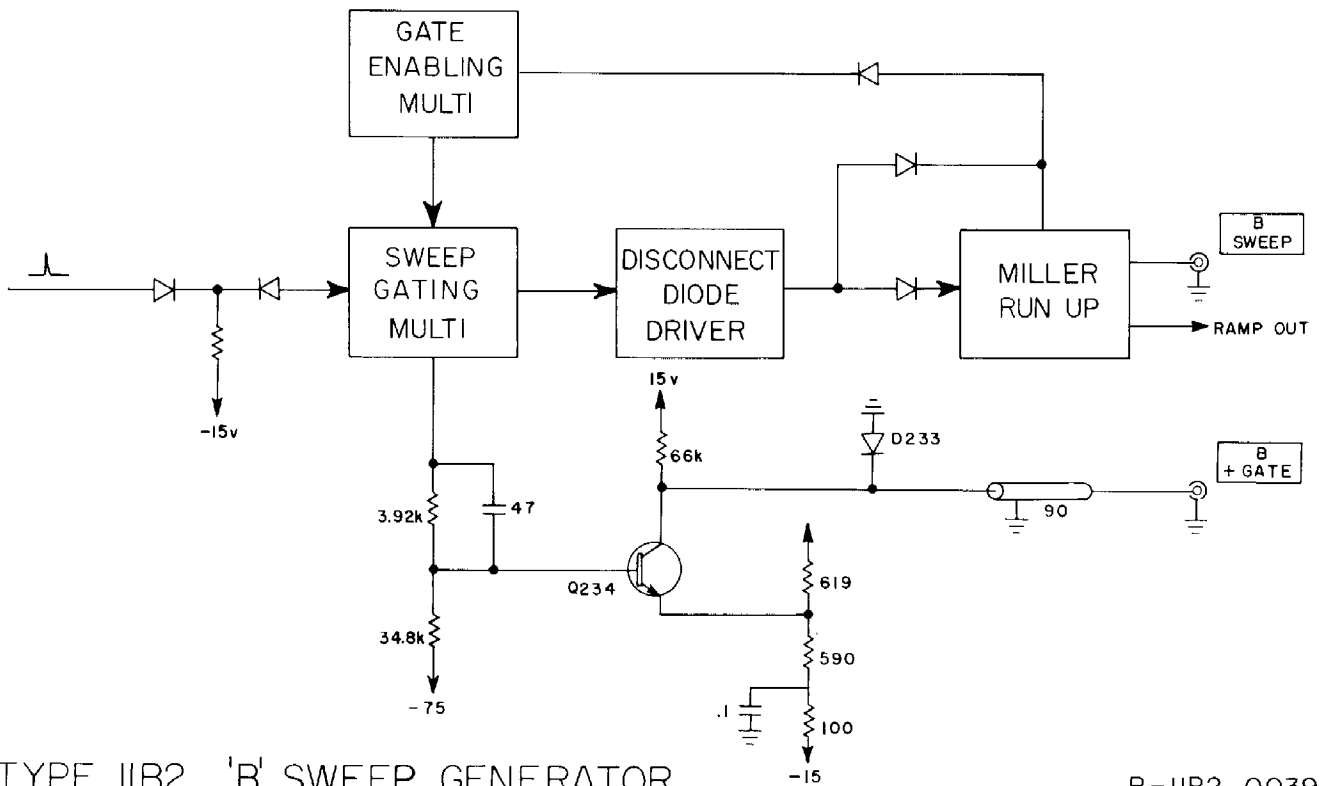
- a. Quiescently Q214A is cut off, Q214B is conducting.
 - b. 1.9 msec after A Sweep starts Q214A begins to conduct.
 - c. As Q214 conducts, it lifts D214 cutting off D214B.
 - d. Current through R215 previously flowing through D214B and Q214B is diverted to D214A and Q214A.
 - e. Current through Q214A collector load drops Q214A collector to 13v.
 - (1) Constant current is achieved by long tailing Q214 emitters through 28.7k to -75v.
 - (2) Collector voltage changes .24v while the A Sweep ramp on Q214A base rises from 2v to 12.5v.
 - f. At the end of A Sweep, retrace drops Q214A base to 2v.
 - g. Q214A cuts off and its collector rises to 16.1v.
 - h. The positive step cuts off Q219.
 - i. The Delay Pickoff circuit has returned to its quiescent state.
5. The DELAY TIME MULTIPLIER is a 10 turn 2k miniature Helipot ($\pm 3\%$ resistance tolerance).
 6. The top of the Helipot ties (through R210) to pin 22 of the blue ribbon connector.
 - a. Pin 22 ties to the +15v regulated supply.
 - b. The only other load from pin 22 is to Q154 (Sweep Generator A Disconnect Diode Driver) base.
 - c. Prevents crosstalk from other 15v loads thereby reduces time jitter in the Delay circuit.

Type 11B2 Plug-In

- 7. The DELAY START adjustment (Sweep Generator A) adjusts the start of A and B sweeps.
 - a. Since, for any DTM setting, the delay time is fixed, an adjustment of the start of A Sweep will adjust delay time relative to the start of A Sweep.

L. B + GATE Amplifier

- 1. The B + Gate Amplifier delivers a 15v positive going waveform to the B + Gate jack on the front panel.
 - a. Same duration as B Sweep.
- 2. The circuit, components, DC voltages and signal voltages are the same as Q134 circuit in the A Sweep Alternate Trace Amplifier.



TYPE 11B2 'B' SWEEP GENERATOR
B + GATE

B-11B2-0039
1-13-'64 dl

Type 11B2 Plug-In

V. HORIZONTAL PREAMP

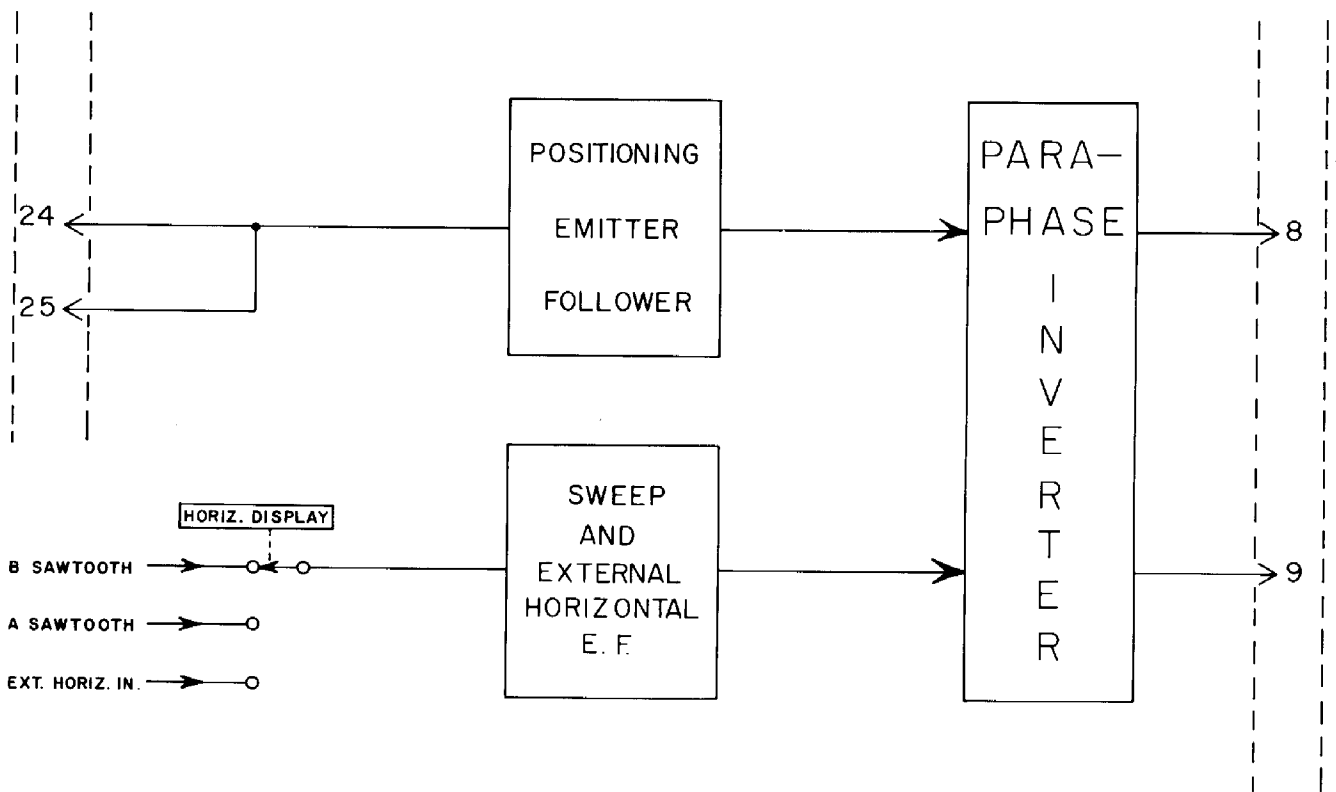
A. The Horizontal Preamp provides a push-pull sweep ramp and positioning information to the Type 647 Horizontal Amplifier.

1. The output appears at pins 8 and 9, blue ribbon connectors.
2. The output is a current drive ($347 \mu\text{a}/\text{cm}$ each side) to the Type 647 Horizontal Amplifier.
3. The $347 \mu\text{a}/\text{cm}$ is standardized for plug-in main frame compatibility.
4. A X10 magnifier is available.

B. Basic Circuits

1. Positioning EF.
2. Sweep and EXT Horizontal EF.
3. Paraphase inverter.

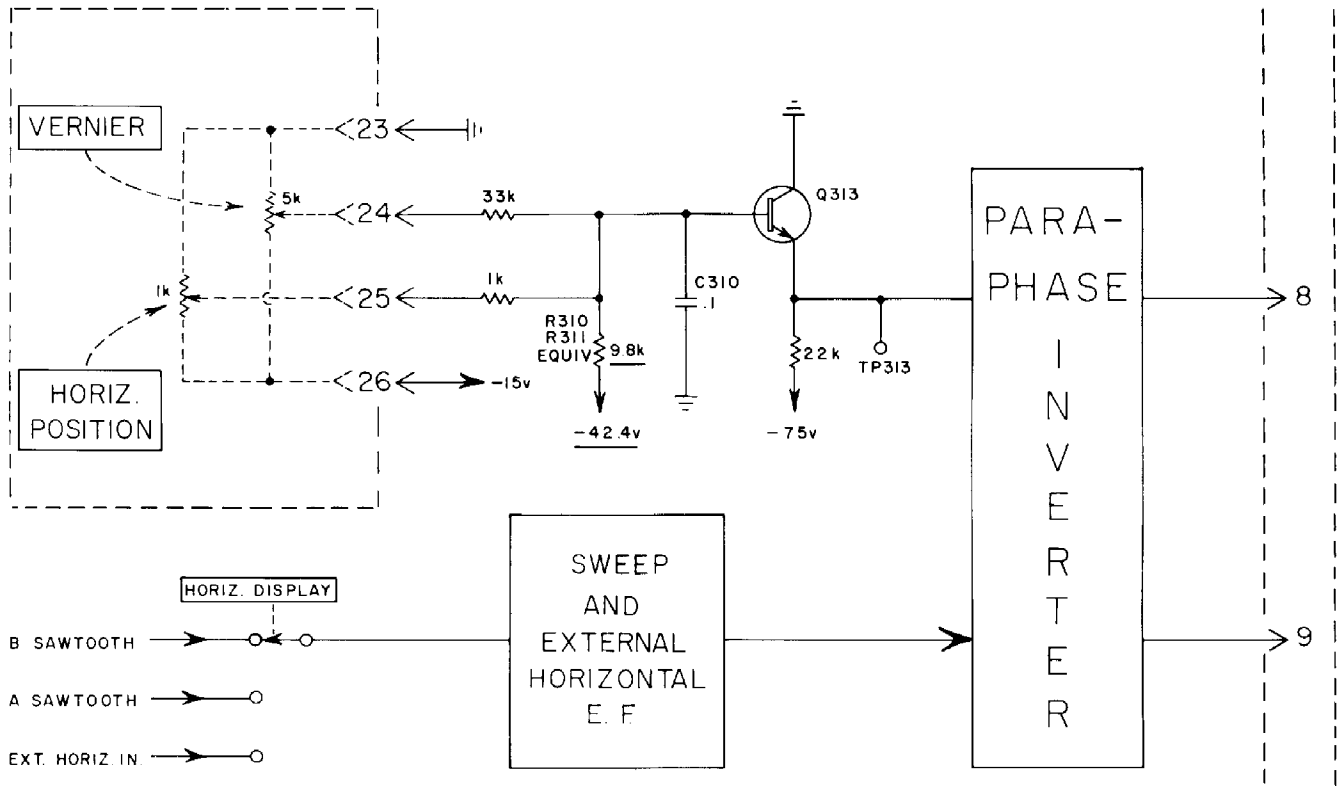
C. Block Diagram



TYPE 11B2 HORIZONTAL PREAMPLIFIER
BLOCK DIAGRAM

Type 11B2 Plug-In

D. Positioning EF



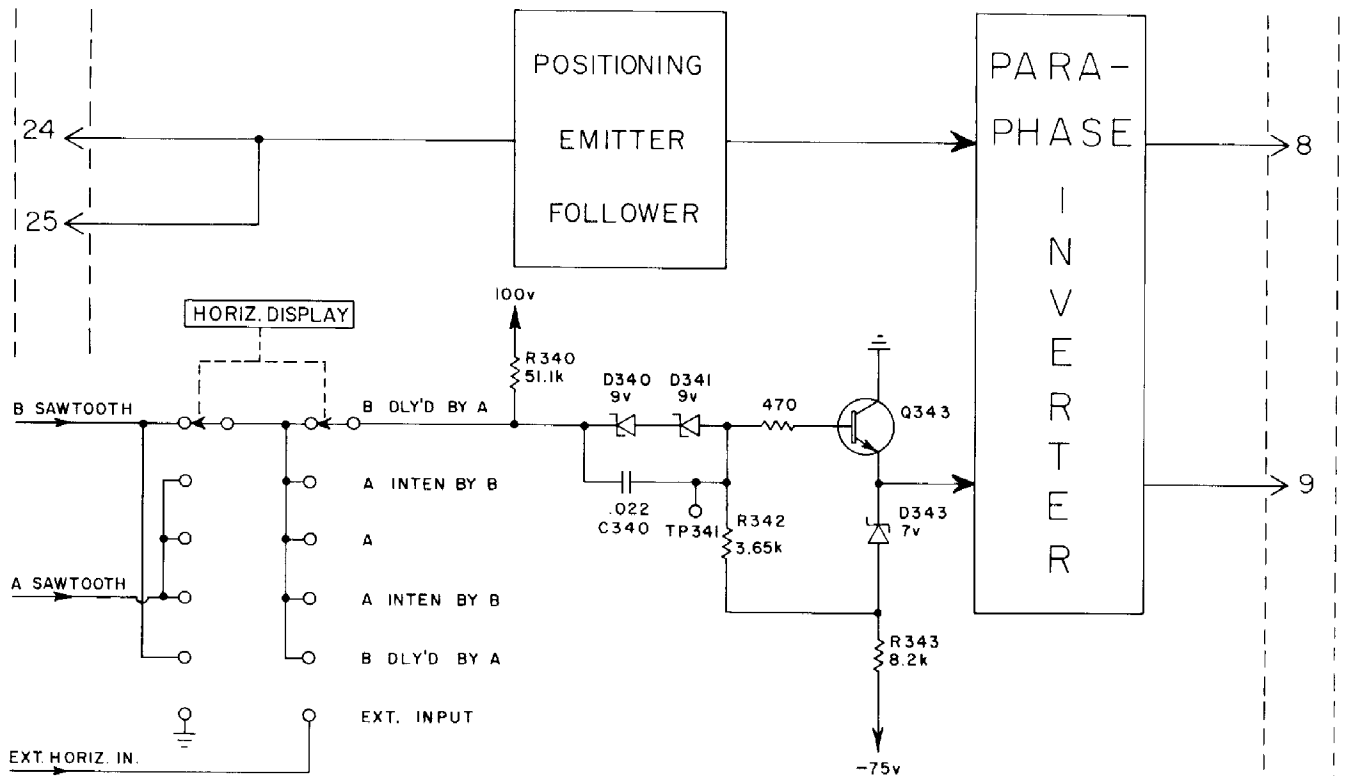
TYPE 11B2 HORIZONTAL PREAMPLIFIER
POSITIONING EMITTER FOLLOWER

B-11B2-0029
12-11-'63 jg

2. Q313 is a 151-103 selected Motorola 2N2219 silicon NPN transistor.
3. Positioning information from the Type 647 main frame appears at pins 24 and 25 of the blue ribbon connector.
 - a. Each positioning control has a swing at pins 24 and 25 of 0v to -15v.
 - b. The HORIZ POSITION control will swing the beam (EXT HORIZ INPUT MODE) 13 cm.
 - c. The VERNIER control swings the beam 2.5 cm.

Type 11B2 Plug-In

- 4. HORIZ POSITION and VERNIER control rotational sensitivity is set by the 3.3k and 1k resistors and R310 and R311.
 - a. R310 and R311 form an equivalent circuit of 9.8k to -42.4v.
 - 5. Q313 voltages with the beam at 0 cm and 10 cm.
 - a. Q313 base, -5.6v to -15v.
 - b. Q313 emitter (TP313), -6.2v to -15.5v.
 - 6. Q313 voltages with the beam at 5 cm.
 - a. Q313 base, -10.4v.
 - b. Q313 emitter (TP313), -11.1v.
 - 7. C310 bypasses pot noise from the positioning controls.
- E. Sweep and EXT INPUT EF
- 1. Delivers Sweep and EXT HORIZ information to the Paraphase Inverter.



TYPE 11B2 HORIZONTAL PREAMPLIFIER SWEEP AND EXT. INPUT E.F.

B-11B2-0030
12-13-63 jg

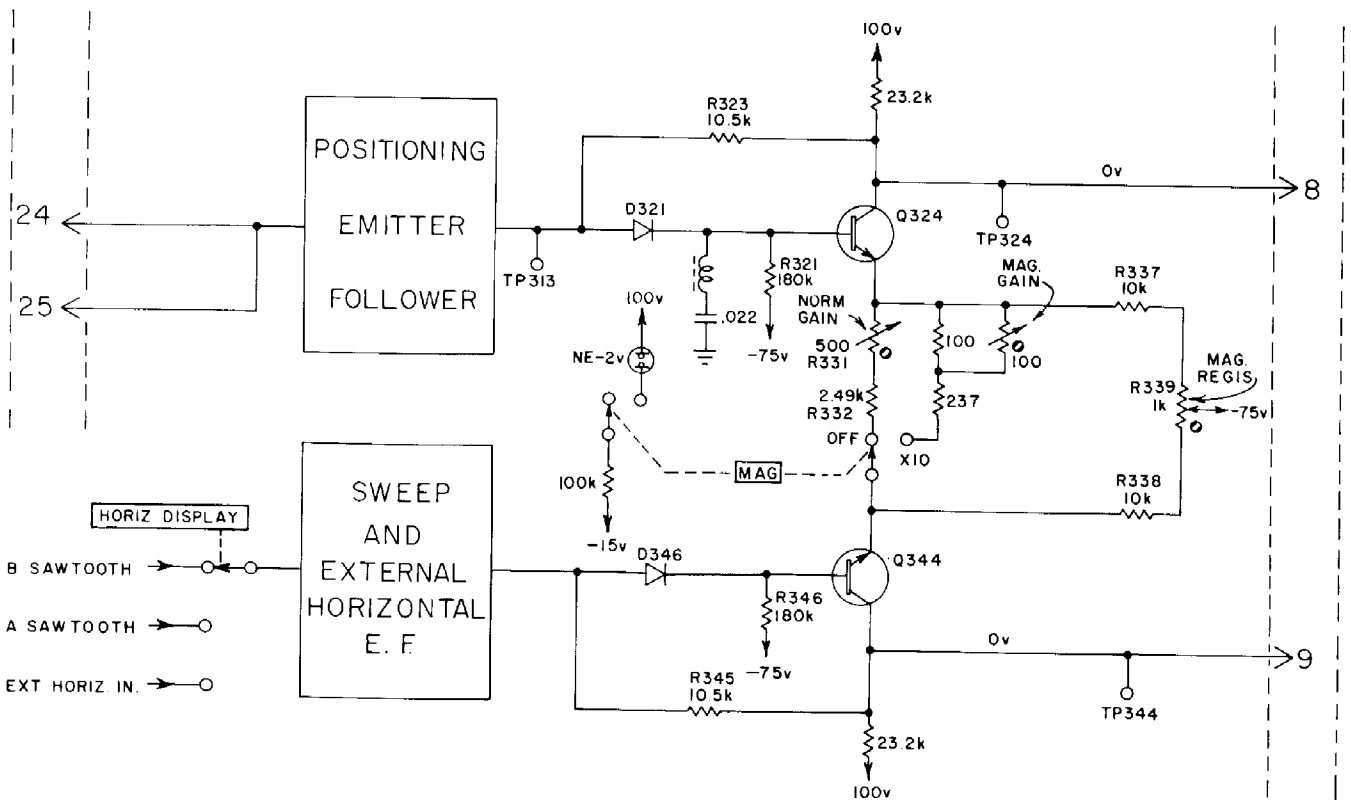
Type 11B2 Plug-In

2. Q343 is a 151-103 silicon transistor.
3. Three inputs selectable by the HORIZ DISPLAY switch.
 - a. The sweep ramp from Sweep Generator A.
 - b. The sweep ramp from Sweep Generator B.
 - c. EXT HORIZ INPUT information from Trigger Generator B Input CF.
4. EXT HORIZ INPUT has a sensitivity of 1v/cm.
5. The DC level in the EXT HORIZ INPUT mode is 7.5v.
6. The Sweep ramps (at wafer 2R of the HORIZ DISPLAY SW) are 10v positive going sawtooth waveforms (2.5v to 12.5v.).
 - a. The mid point on the waveform (sweep halfway across the screen) is 7.5v and compatible with EXT HORIZ INPUT DC level of 7.5v.
7. These input DC levels must be lowered to be compatible with positioning information on Q313.
 - a. D340 and D341 (1N935A Motorola 9v, 5% zeners) drop the DC level 18v.
 - b. Mid-screen DC level on Q343 base is -10.5v.
 - c. Sweep ramp at Q343 base rises from -15v to -5v.
8. 6.8v across R342 (.6v Q343 base emitter junction plus 6.2v across D343) provides about 2 ma of holding current for D340 and D341.
 - a. The current returns through R340 to +100v.
 - b. D343 sets a convenient potential for the bottom of R342.
 - c. D343 is a 10% TI 6.2v zener.
 - d. About 5 ma flows through D343 and Q343.
9. C340 reduces zener noise.

Type 11B2 Plug-In

F. Paraphase Inverter

1. The Paraphase Inverter converts the single ended positioning, A or B Sweep, or EXT HORIZ INPUT signal voltages to push-pull signal current to drive the Type 647 Horizontal Amplifier.



TYPE 11B2 HORIZONTAL PREAMPLIFIER
PARAPHASE INVERTER

B-11B2-0031
12-13-63 jg

Type 11B2 Plug-In

2. The input signal at Q313 or Q443 emitter is 960 mv/cm.
3. The output signal current is 347 μ a/cm.
 - a. The voltage change at pins 8 and 9 is about .4v for full sweep.
4. The circuit uses two transistors and four diodes.
 - a. Q324 and Q344 are 151-108, selected Motorola 2N2501 silicon NPN transistors.
 - b. D321 and D346 are GE 1N3605 silicon diodes.
5. Normal sweep swings Q343 base from -7.5v to -16.7v.
6. Quiescent DC voltages (beam is the center of the screen).
 - a. Q324, Q344 bases, -11.5v.
 - b. Q324, Q344 emitters, -12v.
 - c. Q324, Q344 collectors about 0v.
 - (1) Collector voltages will be set by the Type 647 Horizontal Amplifier.
 - (2) Q324 collector typically 1.3v.
 - (3) Q344 collector typically -.5v.
7. Since the Paraphase Inverter converts from voltage drive to a current output the stage can be said to have a trans-admittance gain*.

a. Trans-admittance gain = $\frac{\Delta \text{Output current}}{\Delta \text{Input Voltage}}$

b. $A_y = \frac{\Delta i_o}{\Delta e_i}$

Where A_y is transconductance gain

Δi_o is the output signal current

Δe_i is the input signal voltage.

* See June 1963 Service Scope

Type 11B2 Plug-In

8. Since there is a signal loss in cathode follower V73 (Trigger Generator diagram), the overall transimpedance gain of the EXT HORIZ INPUT is 347 $\mu\text{a}/\text{volt}$.

$$a. \quad A_y = \frac{3.47 \text{ ma}}{10\text{v}}$$

$$A_y = 347 \mu\text{a}/\text{volt}$$

9. Output current (collector current) can be calculated by the expression

$$\Delta i_o = \frac{\Delta e_i}{R_e}$$

Where Δi_o is the output signal current

Δe_i is the base signal voltage

R_e is the emitter to emitter resistance.

a. e_i is 960 mv/cm.

b. R_e is 2.425k.

(1) R_e is R332 plus one-half of R331, paralleled by series network R338, R339 and R337.

c. $\Delta i_o = \frac{960 \text{ mv/cm}}{2.425\text{k}}$

$$\Delta i_o = 395 \mu\text{a}/\text{cm}$$

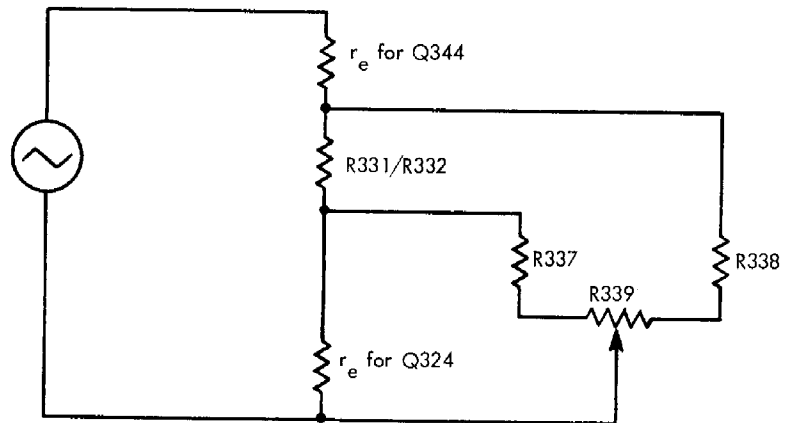
- d. 48 $\mu\text{a}/\text{cm}$ flows through the collector resistors and feedback resistors, and 347 $\mu\text{a}/\text{cm}$ flows to the output load.

10. Like vacuum tube paraphase inverters, the transistor paraphase inverter has some unbalance.

- a. The emitter current return resistors shunt the undriven side of the Paraphase Inverter.

Type 11B2 Plug-In

- b. The equivalent circuit shows the uneven loading with Q344 being driven.



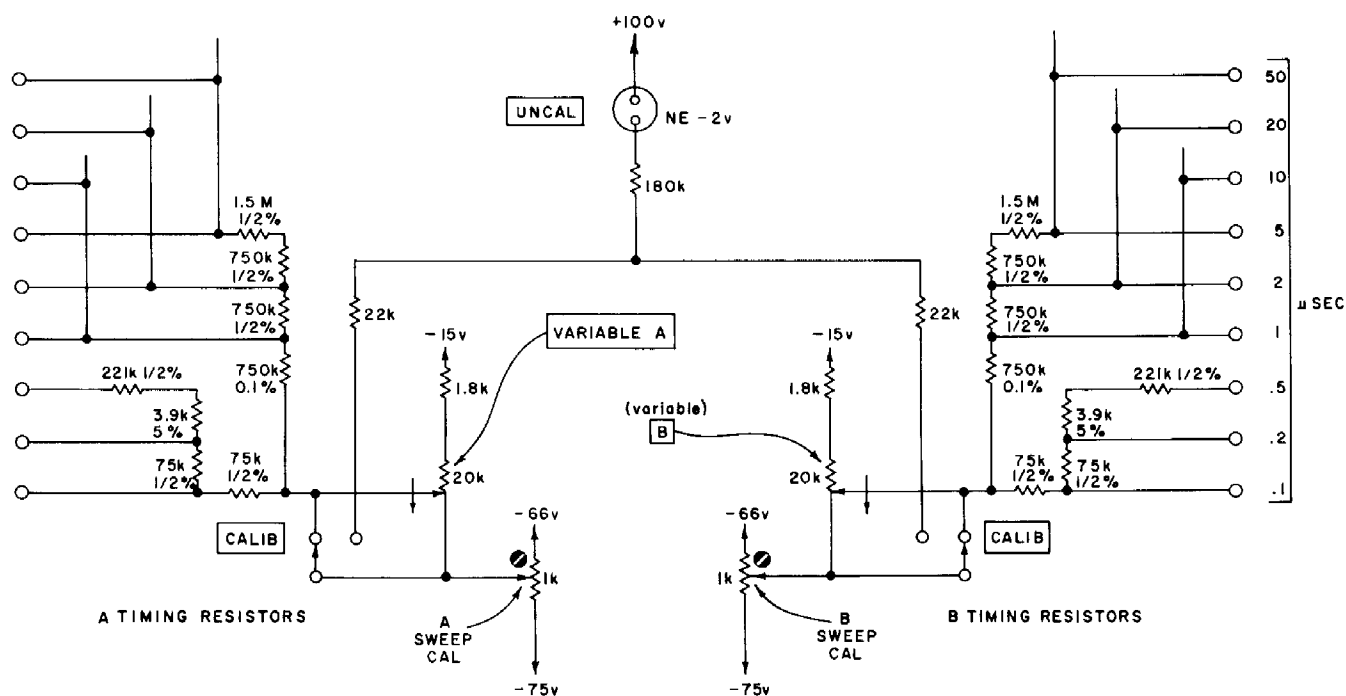
- c. Since (in the illustration) Q344 emitter will have signal voltage about equal to the signal voltage on the base, signal current will flow through R337 and R339.
- d. Signal current in Q344 will exceed the signal current in Q324 by this amount.
- e. Feedback resistors R323 and R345 help minimize the unbalance.
 - (1) Note that R323 is equal to R337 and half R339.
 - (2) R345 is equal to R338 and half R339.

Type 11B2 Plug-In

- f. Since Q344 base will have signal voltage nearly equal to that on the emitter, signal current through R345 will equal that through R338 and R339.
 - g. The output currents will be balanced.
11. The MAG switches in emitter tying resistors about one-tenth the resistance value of R331 and R332.
- a. Only 94 mv/cm base drive is required to produce 347 μ a/cm of output current providing X10 gain.
 - b. This gives the stage a trans-admittance gain of 3.62 ma/volt.
 - c. This approaches the maximum theoretical gain of the stage.
 - d. A neon (NE -2v) indicates MAG ON.
12. MAG REGIS control balances currents to both sides of the amplifier.
- a. To adjust MAG REGIS, turn MAG on, center the beam with the POSITION control, then turn MAG off and recenter the beam using MAG REGIS.
13. D321 and D346 allow the paraphase amplifier transistor bases to follow their emitters if an emitter is raised.
- a. Base-emitter breakdown is prevented.
 - b. V_{EBO} for a 151-108 is 6v.
14. R321 and R346 bias diodes D321 and D346 to heavier conduction.
- a. The diodes have more linear characteristics when biased to heavier forward current.
 - b. The transistor drive current is a smaller portion of the current through the diodes.

Type 11B2 Plug-In

- B. Sweep Generator B Timing Switch switches timing resistors and timing capacitors.
 - 1. Sweep Generator B has no hold-off circuit.
- C. A VARIABLE control is provided for both Sweep A and Sweep B (variable time/cm).



- 1. The controls provide a variable increase of up to 2.5:1 over the calibrated sweep ranges.
- 2. An UNCAL lamp lights when either knob is turned away from its calibrated position.

D. A Sweep Timing Switch

- 1. Timing Caps
 - a. Timing Switch positions .1 sec to 5 sec use 10 μ f TEK made mylar caps.
 - b. Switch positions 10 msec to 50 msec use 1 μ f TEK made mylar caps.

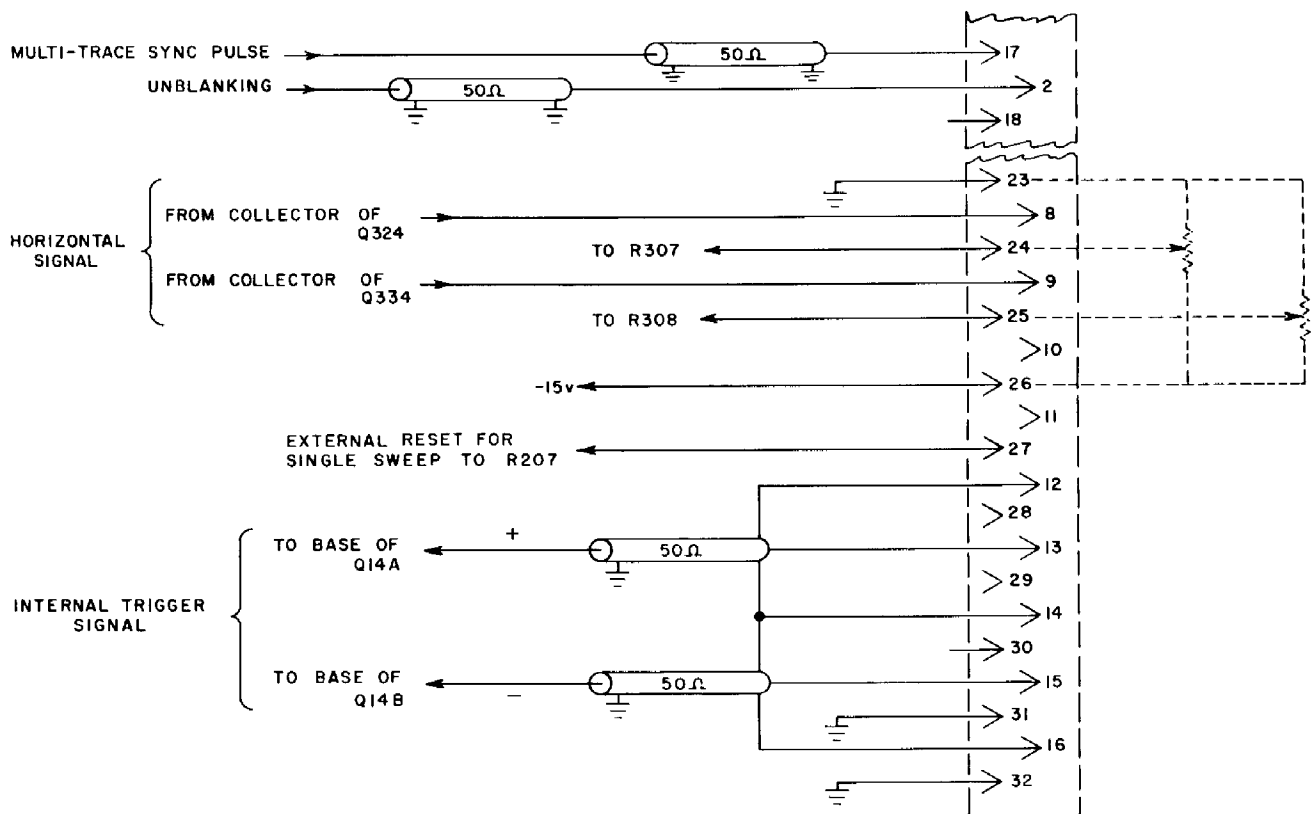
Type 11B2 Plug-In

- c. Positions 1 msec to 5 msec use .1 μ f TEK mylar caps.
 - d. Positions .1 msec to .5 msec use .01 μ f TEK made mylar caps.
 - e. Positions 10 μ sec to 50 μ sec use .001 μ f TEK made mylar caps.
 - f. Positions .- μ sec to 5 μ sec use a combination of 84 pf Sprague 2% ceramic and variable caps.
2. Timing Resistors
 - a. The resistors used in the .5 sec to 5 sec positions are 1% pyrofilm deposited carbon resistors.
 - b. All other timing resistors are 1/2% IRC metal film resistors.
 3. Hold-Off Caps
 - a. The hold-off caps are mounted on the back of the timing switch.
 - b. They are miniature types; the three used from 1 msec to 5 sec are miniature tantalum capacitors.
 4. The A Sweep Timing Switch circuit includes the A SWP CAL adjustment in series with the Timing Resistor returns to -75v.
 5. An RC network (R160R and C160R) help prevent oscillation at some sweep speeds.
- E. B Sweep Timing Switch
1. All components and circuits are the same as the A Sweep except for the absence of a hold-off circuit.

Type 11B2 Plug-In

VII. INTERCONNECTING PLUG

- A. The Interconnecting Plug diagram includes the blue ribbon connector, the unblanking portion of the HORIZ DISPLAY switch, voltage sources and signal paths.
- B. Signal Paths

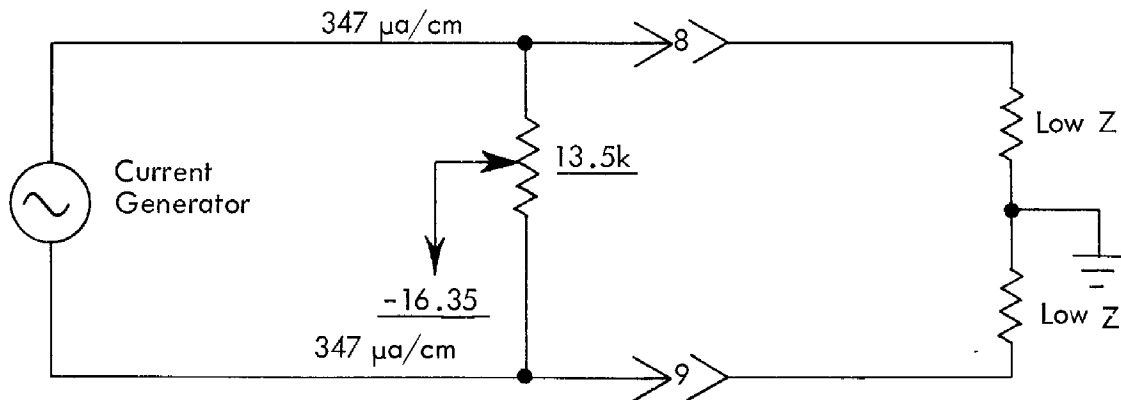


TYPE IIB2 INTERCONNECTING PLUG
SIGNAL CONNECTIONS

B-IIB2-0048
1-20-64 dl

Type 11B2 Plug-In

1. Pins 8 and 9 feed from the Horizontal Preamp to the Type 647 Horizontal Amplifier.

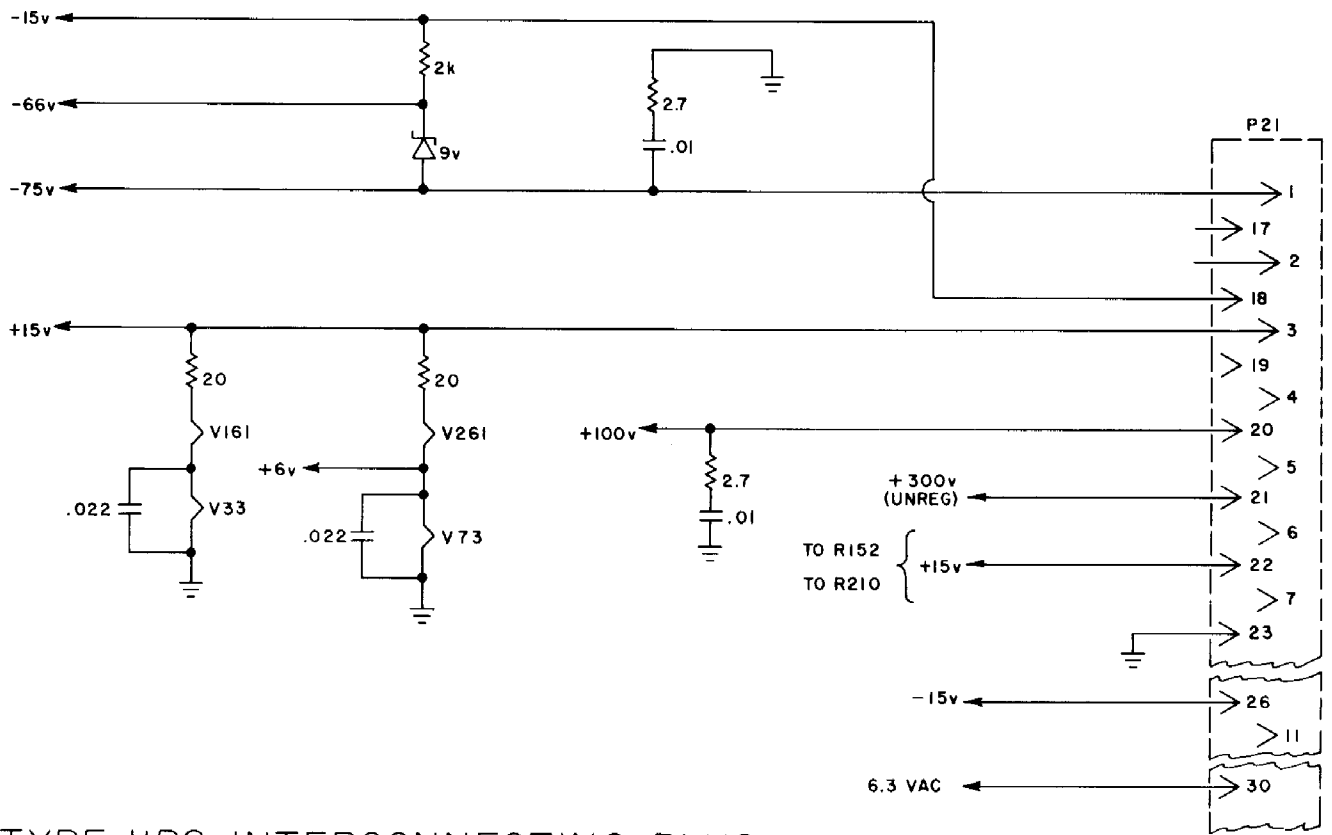


- a. The equivalent circuit consists of a current generator driving the low impedance input of a push-pull operational amplifier in the Type 647.
 - b. DC level at pins 8 and 9 is within 1.5v of ground.
 - c. Signal voltage is not more than .5v.
 - d. Signal current is 347 μA/cm each side.
2. The alternate sync pulse from Sweep Generator A feed through pin 17, through pin 17 of the 10A2 blue ribbon connector to the Alternate Trigger Amplifier.
 - a. A 5v negative going pulse about 70 nsec wide.
 - b. Output impedance is about 400Ω.
 3. Positioning information is present on pins 24 and 25.
 - a. HORIZ POSITION information on pin 25 (0v to -15v).
 - b. VERNIER information on pin 24 (0v to -15v).

Type 11B2 Plug-In

- 4. Internal Trigger Signal on pins 13 and 15.
 - a. Push-pull trigger from 10A2 trigger amplifier.
 - b. DC levels on pins 13 and 15 about 0v.
 - c. Signal level between 90 mv/cm and 140 mv/cm each side.
 - d. Output impedance (from 10A2 Trigger Amp) about 750Ω.
 - e. Input impedance (11B2 Internal Trigger Preamp) 100Ω.
- 5. Unblanking information on pin 2.
 - a. Unblanking voltage will be less than a volt.
 - b. Unblanking current will be about ±2.3 ma.
 - c. Input impedance (647 CRT unblanking circuit) is about 100Ω.

C. Supply Voltages



TYPE 11B2 INTERCONNECTING PLUG
VOLTAGE CONNECTIONS

B-11B2-0049
1-20-'64 dl

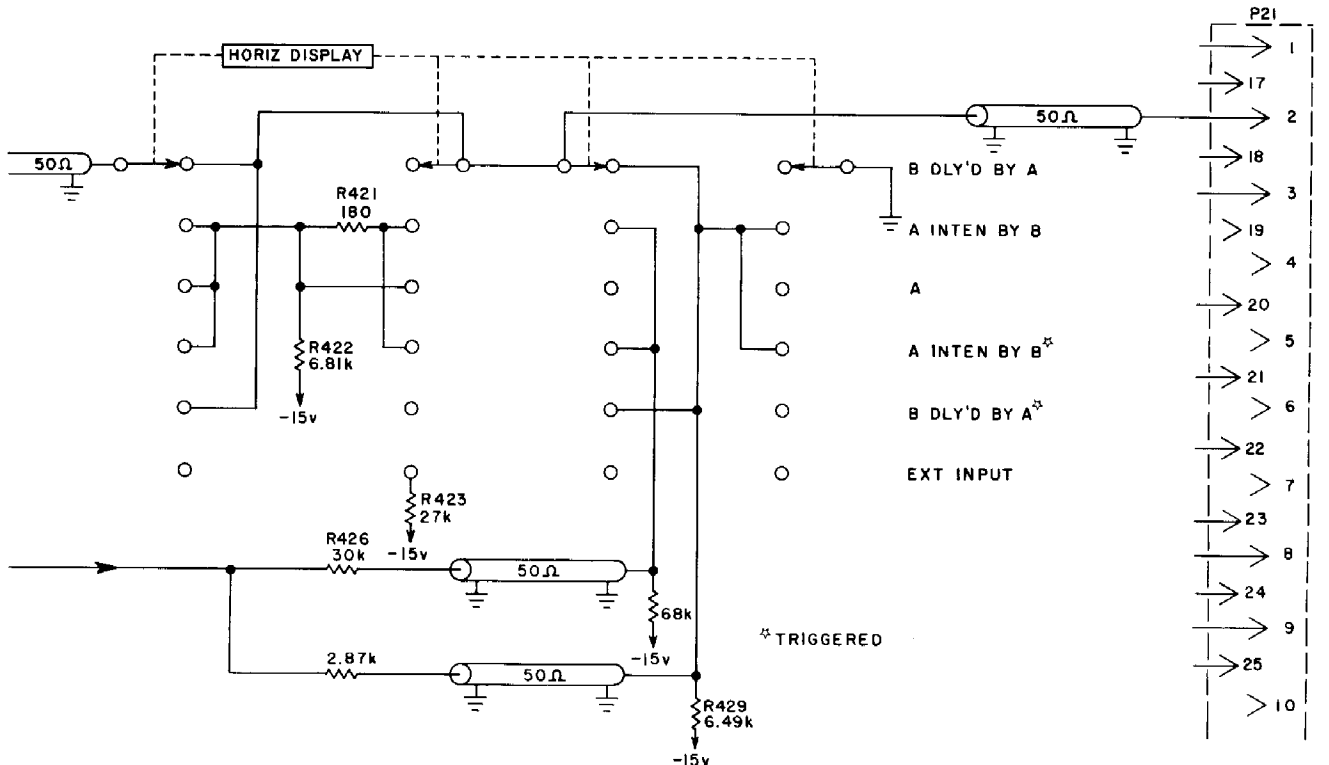
Type 11B2 Plug-In

1. +15, -15, +100, -75v DC voltages are available from the regulated power supply.
2. +15v on pin 22 is a clean supply that supplies Q154 (Disconnect Diode Driver Amp) base and the top of the Delay Time Multiplier divider.
3. 6.3v AC on pin 13 supplies LINE trigger.
4. The 4 nuvistors obtain their heater current from +15v at pin 3.
 - a. V161 and V33 heaters are in series.
 - b. V261 and V73 heaters are in series.
 - c. A tap between V261 and V73 provides +6v for clamping diode D293 in the B Sweep Enabling Multi.
5. A divider between pin 1 (-75v) and pin 18 (-15v) provides -66v for use on the A and B Sweep Cal adj. pots.
 - a. A 9v zener (D407) assures a constant -66v.
 - b. D407 is a Motorola 1N735A 5% 9v zener.
6. Unregulated 300v on pin 22 supplies the RESET ready light in the A Sweep.

Type 11B2 Plug-In

D. Unblanking Mixer

1. Sections 3F, 4F, 4R and 1F of the HORIZ DISPLAY switch provide for various combinations of unblanking currents from Sweep Generator A and Sweep Generator B.



TYPE IIB2 INTERCONNECTING PLUG
UNBLANKING MIXER

B-IIB2-0047x
1-16-'64 dl

2. Unblanking waveforms generated in the Type 11B2 Sweep Generator circuits are fed through pin 2 to the Type 647 Unblanking Amplifier.

Type 11B2 Plug-In

- a. Input impedance (Type 647 Unblanking Amplifier) is about 65Ω .
- b. The equivalent circuit below shows Unblanking Mixer connections in B DLY'D BY A, A INTENS BY B, and A positions of the HORIZ DISPLAY switch.

