2630
FOURIER ANALYZER SERVICE

WARNING

The following servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing other than that contained in the User's Guide unless you are qualified to do so. Refer to the Service Precautions in Section 1 before performing any service.

DECEMBER 1988

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Overview

Introduction

This manual contains service information for the Tektronix 2630 Fourier Analyzer for use by Tektronix service personnel who are familiar with 2630 operation.

Maintenance Philosophy

This product is maintained using field-replaceable units. The Field Replaceable Unit (FRU) is the lowest unit or assembly that is replaceable in the product, either at the installed site or in the repair center.

In troubleshooting a problem, isolate and replace the FRU only. The 2630 can then return to use while the faulty card or assembly is returned to the factory for repair. The FRUs in the 2630 are:

Description	Part Number
FXP (Fixed Point Processor) Board	671-0625-00
DFE (Digital Front End) Board	671-0624-00
DBE (Digital Back End) Board	671-0626-00
MBD (Mother) Board	671-0623-00
DIO (Digital I/O) Board	671-0969-00
PI (Parallel Interface) Board	671-0970-00
LED Board	671-0971-00
Power supply	118-7767-00
Fan	119-3194-00
Line Filter	119-3195-00
AC Module	118-7766-00

Do not replace:

Components that are soldered in place
Cable connectors (replace the cable)
Chip sockets (replace the board)

Handling Printed Circuit Boards

Be careful when handling printed circuit boards to prevent static electricity from destroying the components. Observe the following precautions:

1. Before removing or installing a board, always turn off the power to both the 2630 and the host computer.
2. Leave the board in its anti-static bag until it is needed.
3. Whenever the board must contact another object, such as a table or bench, reference yourself to the object first.
4. When removing a board from its anti-static bag, reference yourself to the bag by holding the bag at the opening. Remove the board from the bag by holding the board along its outer edge.
5. When installing a board into the unit, reference yourself to the unit by placing your free hand on the chassis.
6. When passing the board to another person, hold the board in one hand and make contact with the other person with your free hand. Continue contact with the other person until the other person is holding the card.

Service Precautions

The following service precautions are for qualified service personnel only.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing with Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections or components while power is on.

Disconnect power before removing protective panels or replacing components or assemblies.

Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor is essential for safe operation.

2

Corrective Maintenance

Introduction

This section contains:

- A problem determination guide. The problem determination guide is a list of symptoms and probable causes of the more common 2630 problems.
- Test procedures for the system and the individual boards within the system.
- Power supply adjustment procedure.

Problem Determination Guide

The following guide lists some of the more common 2630 problems with possible causes and suggestions of things to check.

Symptom	Action
Power indicator does not come on; fan does not turn.	1. Check the line fuse (see Section 3). 2. Check the power supply (see *Adjusting the Power Supply* in this section).
Power indicator does not come on; fan turns.	1. Check the Power indicator. 2. Check the power supply (see *Power Supply Check* in this section)
Input channels will not calibrate (none of the four)	1. Check the output channel for dc offset. Perform the *DBE Board Test Procedure* in this section. 2. Replace the DBE Board.
ACTIVE indicator does not flash (about once per second).	1. Check serial interface cable connection. 2. Check that host computer is powered up.

2630 System Test Procedure

The following test procedure verifies proper operation of the entire 2630. To perform this procedure, you must be familiar with 2630 operation as described in the *2630 Fourier Analyzer User's Guide.*

Equipment Requirements

This test procedure requires the following equipment:

- Host computer (IBM PC or equivalent)
- Digital multimeter (DC volts and AC volts, 1 percent accuracy)
- Special test cable (part number 100-109704-00)
- Small screwdriver (preferably non-metallic)
- 2630 test setup diskette (part number 100-109704-00)
- A DBE (Digital Back End) Board (if the 2630 doesn't already have one)
- Option 2H (two channel zoom) for a two- channel system or Option 3H (four channel zoom) for a four-channel system

If the 2630 system test setup files are not on the host computer hard disk, copy the files from the test setup diskette into the Instrument Program directory using the DOS command:

```
copy *.*
```

Test Setup

1. Turn off the 2630 and disconnect the ac power cord.
2. Remove the 2630 cover. See Section 3.
3. Connect ac power to the 2630. Do not turn on power yet.
4. Connect the interface cable between the 2630 Primary Port and the host computer serial port.
5. Turn on the host computer and the 2630. The 2630 Power indicator should be on and the Active indicator should begin blinking. If not, troubleshoot the problem with the *Problem Determination Guide* at the front of this section.

Power Supply Check

6 Measure the +5-volt power supply. Connect the DVM to U48 pin 20 (+) and TP-16 (-) on the DFE Board (see Figure 2-1). The voltage must be between 4.9 and 5.1 volts (Table 2-1). If the voltage is outside of this range, see *Adjusting the Power Supply* in this section.

7 Measure the +15-volt power supply. Connect the DVM between U23 pin 4 (+) and TP-16 (-) on the DFE Board. The voltage must be between 14.85 and 15.15 volts (Table 2-1). If the voltage is outside of this range, see *Adjusting the Power Supply* in this section.

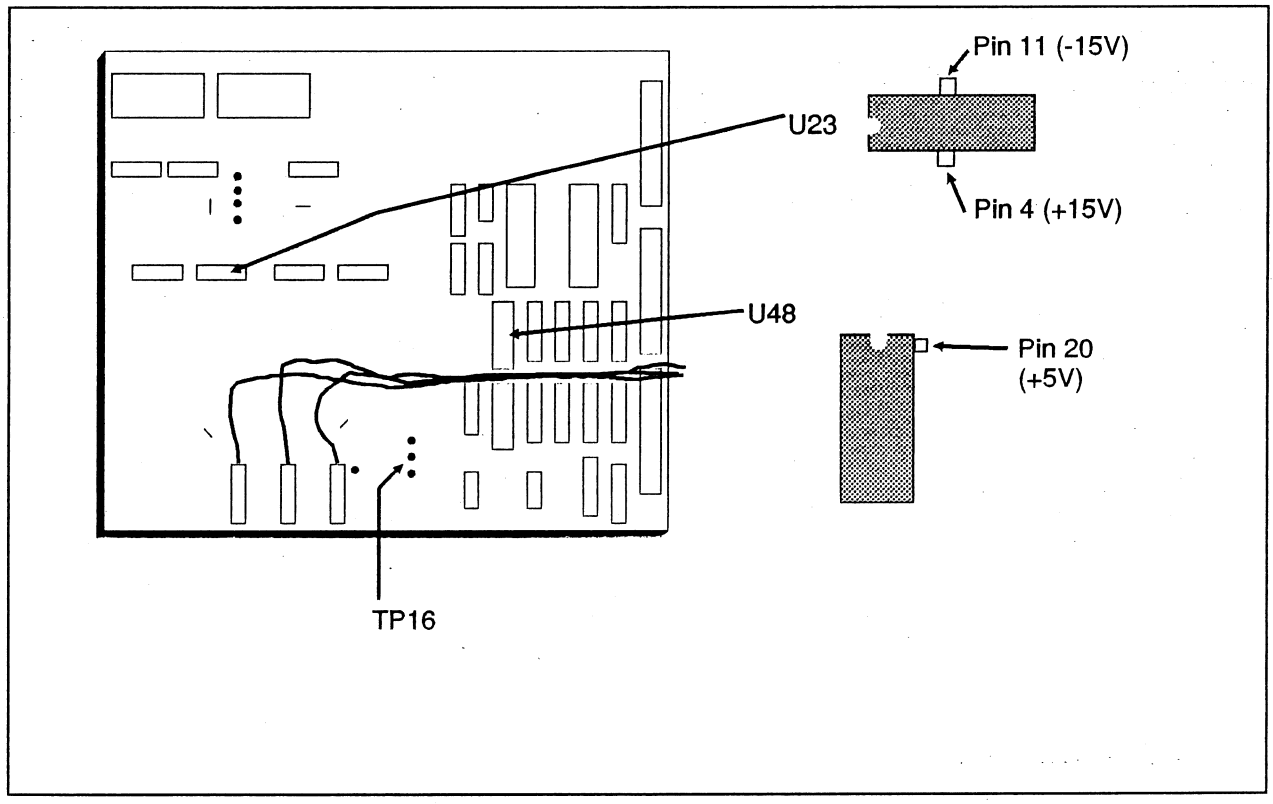


Figure 2-1. Power Supply Test Points

8 Measure the -15-volt power supply. Connect the DVM between U23 pin 11 (-) and TP-16 (+) on the DFE Board. The voltage must be between -14.85 and -15.15 volts (Table 2-1). If the voltage is outside of this range, see *Adjusting the Power Supply* in this section.

Table 2-1. Power Supply Voltages

Supply	Test Points	Acceptable Range
+5V	+ U48 Pin 20 - TP-16	4.90 to 5.10
+15V	+ U23 Pin 4 - TP-16	14.85 to 15.15
-15V	- U23 Pin 11 + TP-16	14.85 to 15.15

System Initialization

This procedure assumes that the host computer is initialized and that the directory containing the Instrument Program is the active directory.

9 Start the Instrument Program (enter "IP"). The host computer downloads code to the 2630 and the Transfer indicator blinks. After initialization, the Instrument Program appears on the host screen.

10 Use the Instrument Program STORAGE function to call up the STUP file. When the stored file loads, the upper display shows a 500 Hz sine wave in the time domain. The lower display shows an ASPEC of the sine wave.

Verify Output Channel Calibration

Before making any measurements, you must verify the output channel calibration.

11 Set the output frequency for 500 Hz and the output voltage for 10 volts.

12 Set the DVM to the 20-volt ac range and check the voltage at the 2630 Output connector. The output voltage must be between 7.00 and 7.14 volts. If the voltage is outside of this range, discontinue system verification and perform the *DBE Test Procedure* in this section.

Common Mode Rejection

The following tests verify the common mode rejection for Input channels 1 through 4. If any of these tests fail, discontinue the system test procedure and perform the *DFE Test Procedure* in this section.

13 Use the Instrument Program STORAGE function to call up the CMRTST file.

14 Connect the special test cable (100-100034-00) between the 2630 Output connector and Channel 1 Input connector. This cable has a phono jack and BNC connector on one end. This end plugs into the Input connector.

15 Check the 500 Hz spectral line on the lower display. The line must be less than -75 dB.

16 Disconnect the special test cable from Channel 1 and connect it to Channel 2.

17 Change the lower display to Ch=2.

18 Check the 500 Hz spectral line on the lower display. The line must be less than -75 dB.

19 If the 2630 has four channels, repeat steps **16** through **18** for Channels 3 and 4.

20 Disconnect the special test cable from the 2630.

Gain and Offset

21 Press "Q" on the host computer keyboard. The Instrument Program will be replaced by a menu.

22 Press "W". The 2630 gain and offset measurements for all the channels will display in about 10 to 20 seconds.

The gain factors should be between 0.95 and 1.05. Offset measurements should be between -100 and +100.

23 Press "C" to continue.

Filter Phase Matching

24 Use the Instrument Program STORAGE function to call up the PHTST file.

25 Press "R" on the host keyboard to run an averaged transfer function.

NOTE: After you press R, wait for the Run indicator to turn off indicating that averaging is completed.

The lower display shows phase matching between Channels 2 and 1 and should vary less than plus or minus 1 degree.

The upper display shows filter ripple matching between Channels 2 and 1 and should vary less than plus or minus 0.1 dB.

26 If the 2630 has four channels, proceed to step **27**. If the 2630 has two channels, proceed to step **29**.

NOTE: In the following steps, every time you change the channel selection for the upper and lower display, you must enter Y to reset the proper Y-axis calibration for the lower display and Alt-Y for the upper display.

27 Change the upper and lower displays to Ch=3/1 and repeat Step **25** to measure Channel 3.

28 Change the upper and lower displays to Ch=4/1 and repeat Step **25** to measure Channel 4.

Triggering

29 Use the Instrument Program STORAGE function to call up the TRGTST file. The upper display is set for channel 1 and displays a sine wave. The trigger mode is set for channel 1 and Auto.

30 Adjust the Instrument Program trigger mode + and - slope selector and level controls and observe that the sine wave triggers at the appropriate level and slope as you change the settings.

31 Change the upper display and trigger source to channel 2 and repeat Step **30**.

32 If the 2630 has four channels, repeat Step **30** for channels 3 and 4.

AC/DC Coupling

33 Use the Instrument Program STORAGE function to call up the CPLGTST file.

34 Connect Channel 1 input to the Output connector with a coax cable. The lower display shows an ASPEC of a 1 Hz sine wave.

35 Using the cursor, measure and record the 1 Hz sine wave level.

36 Change the coupling of the lower display from DC to AC. The level of the sine wave at 1 Hz should reduce by at least 1 dB.

37 Change the lower display to Ch=2 and connect the Output to Channel 2.

38 Repeat Steps **35** and **36**.

39 If the 2630 has four channels, repeat Steps **35** and **36** for channels 3 and 4.

Harmonic Distortion

This test requires the Zoom Option.

40 Use the Instrument Program STORAGE function to call up the HDTST file.

41 Connect the Output to Channel 1 input.

42 Press "R" on the keyboard to run an ASPEC average.

43 Observe the spectral line at 10 kHz in the Zoom ASPEC on the lower display. There should be no harmonics greater than -76 dB.

44 Connect the Output to Channel 2 input.

45 Change the lower display to Ch=2 and repeat steps **42** and **43**.

46 If the 2630 has four channels, repeat steps **42** and **43** for channels 3 and 4.

Zoom

This test requires the Zoom Option.

47 Using the 2630 Storage mode, call up the ZMTST file.

48 Observe the lower display for a zoom ASPEC of a noise spectra with 50 Hz bandwidth on either side of 6000 Hz.

49 Use the OUTPUT controls to change the bandwidth of the shaped random noise from 500 Hz to 50 Hz.

50 Observe that the width of the spectral shape on the lower display gets narrower.

51 Use the FREQUENCY controls to change the bandwidth from 1 kHz to 500 Hz.

52 Observe that the width of the spectral shape on the lower display gets wider.

53 Change the lower display to Ch=2, use the OUTPUT controls to change the bandwidth of the shaped random noise to 50 Hz, and use the FREQUENCY controls to change the bandwidth to 1 kHz.

54 Repeat Steps **48** through **52** for Channel 2.

55 If the 2630 has four channels, repeat Steps **48** through **52** for Channels 3 and 4.

Digital Filters

56 Use the Instrument Program STORAGE function to call up the DIGFLT file.

57 Change the upper display to Ch=1. If this is a four channel system, change the lower display to Ch=3.

58 Observe both displays and decrease the bandwidth from 20 kHz in steps to 20 Hz, ensuring that the ASPEC is flat across the band. (The input is random noise.) Allow enough time between steps for the 2630 to complete the ASPEC for each frequency range.

Mother Board Test Procedure

The following test procedure verifies proper operation of the 2630 Mother Board. To perform this procedure, you must be familiar with 2630 operation as described in the *2630 Fourier Analyzer User's Guide*.

Note: Perform this test only if the *2630 System Test Procedure* fails and you suspect a problem with the Mother Board.

Equipment Requirements

This test procedure requires no special equipment.

Test Setup

1. With the 2630 power off and the power cord unplugged, remove the 2630 cover (see Section 3).
2. Disconnect the flat ribbon connectors between the Mother Board and the FXP, DFE, and DBE Boards.
3. Make sure that the Mother Board jumpers at locations J8, J9, and J10 are installed.

Test Procedure

4. Plug in the 2630 and turn on both the 2630 and the host computer. The 2630 Power indicator should be on and the Active indicator should be blinking.
5. Press and hold the Reset switch on the Mother Board. The Active indicator should not blink (it should either stay on or off).
6. Release the Reset switch. The Active indicator should begin to blink.

   If the Active indicator does not blink:

   - Check the serial interface cable between the 2630 and the host computer.
   - Check that the host computer is powered up.

7. On the host computer, select the directory where the Instrument Program is located, but do not start the Instrument Program.

8 Enter the following commands:

```
tomon -k
@
XQ
```

You should see the following message on the monitor:

```
mem ends at 80000
FXP  ERR1
DFEM ERR5
DFE1 ERR0
No DFE2
No DBE   OR  DBE ERR1
```

9 Start the memory diagnostic with the following command:

```
xm
```

The memory diagnostic takes 10 to 12 seconds per pass. The messages are self explanatory.

10 After five successful passes, press Ctrl-C to terminate the diagnostic.

If the Mother Board successfully passes all of the tests, the board is probably okay. If the Mother Board fails any of the tests, replace the Mother Board.

FXP Board Test Procedure

The following test procedure verifies proper operation of the FXP (Fixed Point Processor) Board. To perform this procedure, you must be familiar with 2630 operation as described in the *2630 Fourier Analyzer User's Guide*.

Note: Perform this test only if the *2630 System Test Procedure* fails and you suspect a problem with the FXP Board.

Equipment Requirements

This test procedure requires the following equipment:

- The host computer
- 2630 Setup Diskette 100-109704-00
- Safety glasses

NOTE: To successfully test the FXP Board, all of the other boards in the 2630 must be okay. If you suspect any of the other boards, either replace the questionable board or do not run this test.

If the 2630 system test setup files are not on the host computer hard disk, copy the files from the test setup diskette into the Instrument Program directory using the DOS command:

```
copy *.*
```

Test Setup

1 Turn on both the 2630 and the host computer.

2 Call up the Instrument Program on the host computer.

FXP Test

3 Use the Instrument Program STORAGE function to call up the STUP file. The upper display should show the ASPEC of the sine wave.

4 Check that the sine wave has no anomalies.

If the FXP Board successfully passes the above test, it is probably okay. If the FXP Board fails the test, replace the board.

DFE Board Test Procedure

The following test procedure verifies proper operation of the DFE (Digital Front End) Board. To perform this procedure, you must be familiar with 2630 operation as described in the *2630 Fourier Analyzer User's Guide*.

NOTE: Perform this test only if the *2630 System Test Procedure* fails and you suspect a problem with the DFE Board.

This procedure tests only one DFE Board, on channels 1 and 2. If you have a four-channel 2630, you should perform this test on both DFE Boards. To test the second DFE Board, substitute channels 3 and 4 for channels 1 and 2 in the following procedure.

Equipment Requirements

This test procedure requires the following equipment:

- The host computer
- The optional Output Channel (the DBE Board)
- Option 2H (two channel zoom) for a two- channel system or Option 3H (four channel zoom) for a four-channel system
- Small screwdriver
- Special test cable (part number 100-100034-00)
- 2630 Test Setup Diskette (part number 100-109704-00)
- Safety glasses

If the 2630 system test setup files are not on the host computer hard disk, copy the files from the test setup diskette into the Instrument Program directory using the DOS command:

```
copy *.*
```

Test Setup

1. With the power off, remove the 2630 cover (see Section 3).
2. Make sure that the DFE Board jumpers at locations J7, J8, and J9 are installed.
3. Turn on the 2630 and the host computer.
4. Start the Instrument Program.

Common Mode Rejection Adjustment

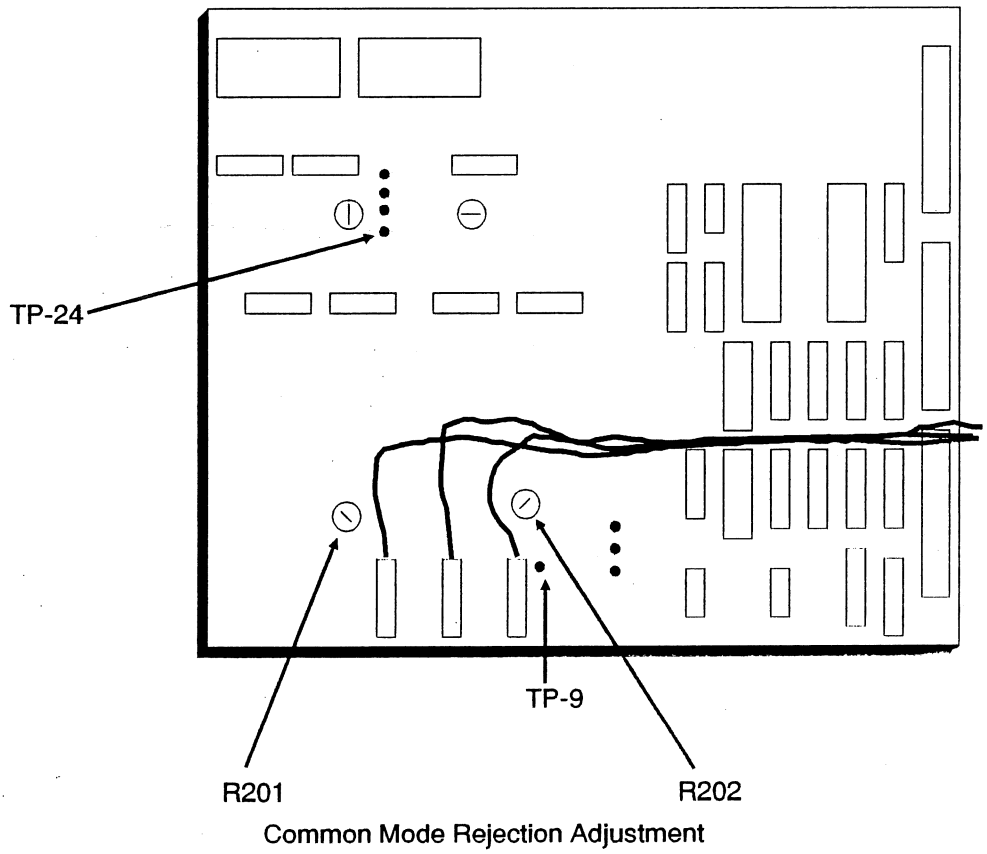
5 Use the Instrument Program Storage feature to call up the CMRTST file.

6 Connect the special test cable (100-100034-00) between the 2630 Output connector and Channel 1 Input connector. This cable has a phono jack and BNC connector on one end. This end plugs into the Input connector.

7 Use the Cursor mode on the lower display to show the ASPEC of Channel 1 and adjust R201 on the DFE Board until the 500 Hz line is as small as the adjustment will allow (below -80 dB). See Figure 2-2.

8 Remove the special test cable from Channel 1 and connect it to Channel 2.

9 Set the lower display to Ch=2 ASPEC i.



Common Mode Rejection Adjustment

Figure 2-2. DFE Board Common Mode Rejection Adjustments

10 Adjust R202 on the DFE Board until the 500 Hz line on the display is less than -80 dB.

11 Disconnect the special test cable from the 2630.

Gain and Offset

12 Press "Q" to exit the Instrument Program, then press "W". The program will calibrate the 2630 and create or update the calibration file.

When through, the program displays the gain and offset values for all of the attenuator settings.

13 Check that the attenuator measurements are between 0.95 and 1.05.

14 Check that the offset measurements are between -100 and +100.

Filter Ripple

15 Press "C" to return to the Instrument Program.

16 Use the Instrument Program STORAGE function to call up the FLTTST file.

17 Connect a jumper between TP-24 and TP-9 on the DFE Board. See Figure 2-2.

18 Press "R" to run the test. The lower display (Y-axis -11 dB to -13 dB) displays the Channel 2 filter ripple. The ripple should not vary more than 0.3 dB.

19 Remove the jumper from TP-24 and TP-9.

Filter Phase Matching

20 Use the Instrument Program STORAGE function to call up the PHTST file.

21 Press "Y" to set the lower display to plus or minus 1 degree, then press Alt-Y to set the upper display to plus or minus 1 degree.

22 Observe the lower display and adjust R203 and R204 until the phase delta from dc to 20 kHz is less than plus or minus 1 degree (you will have to run an average after each adjustment). See Figure 2-3.

23 Using the cursor in the upper display, find the highest and the lowest reading between 50 Hz and 20 kHz. The delta should be less than 0.2 dB.

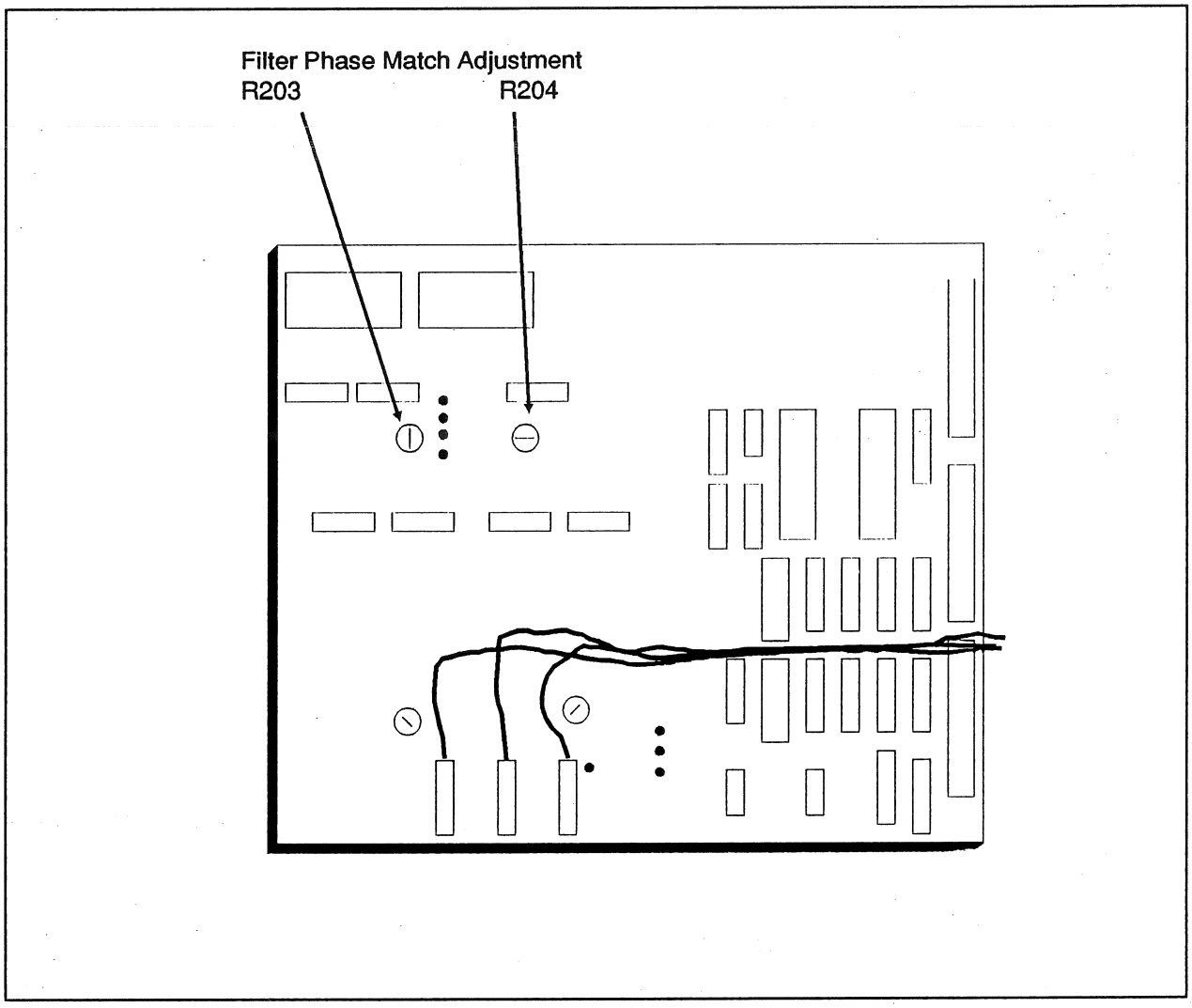


Figure 2-3. DFE Board Filter Phase Match Adjustments

Harmonic Distortion

This test requires the Zoom Option.

24 Use the Instrument Program STORAGE function to call up the HDTST file.

25 Connect Input Channel 1 to the Output channel with a coax cable.

26 Press R to run. The ASPEC a of the sine wave at 5 kHz on the lower display should show no harmonics greater than -76 dB at 10 kHz and 15 kHz.

27 Remove the coax cable from Input Channel 1 and connect it to Input Channel 2.

28 Change the lower display to Ch=2 and observe the same results as in Step 26.

AC/DC Coupling

29 Use the Instrument Program STORAGE function to call up the CPLGTST file.

30 Remove the coax cable from Input Channel 2 and connect it to Input Channel 1.

31 Using the cursor, measure and record the amplitude of the 1 Hz spectral line on the lower display.

32 Change the coupling from DC to AC and check that the amplitude of the spectral line is down at least 1.0 dB.

33 Change the lower display to Ch=2.

34 Remove the coax cable from Input Channel 1 and connect it to Input Channel 2.

35 Change the coupling from AC to DC and measure and record the spectral line at 1 Hz.

36 Change the coupling from DC to AC and check that the amplitude of the spectral line is down at least 1.5 dB.

Trigger

37 Use the Instrument Program STORAGE function to call up the TRGTST file.

38 Set the trigger mode to Auto and check that the sine wave on the upper display triggers on both slopes and at all levels.

39 Change the upper display to Ch=2 and the trigger source to Ch2.

40 Change the trigger slope and observe that the sine wave triggers on the new slope setting.

Zoom

This test requires the Zoom Option.

41 Use the Instrument Program STORAGE function to call up the ZMTST file.

42 Observe the lower display for a zoom ASPEC of a noise spectra with 50 Hz bandwidth on either side of 6000 Hz.

43 Use the OUTPUT controls to change the bandwidth of the shaped random noise from 500 Hz to 50 Hz.

44 Observe that the width of the spectral shape on the lower display gets narrower.

45 Use the FREQUENCY controls to change the bandwidth from 1 kHz to 500 Hz.

46 Observe that the width of the spectral shape on the lower display gets wider.

47 Change the lower display to Ch=2, use the OUTPUT controls to change the bandwidth of the shaped random noise to 50 Hz, and use the FREQUENCY controls to change the bandwidth to 1 kHz.

48 Repeat Steps **42** through **46** for Channel 2.

49 If the 2630 has four channels, repeat Steps **42** through **46** for Channels 3 and 4.

If the board successfully passes all of the above tests, it is probably okay. If it fails any of the tests, replace it.

DBE Board Test Procedure

The following test procedure verifies proper operation of the optional DBE Board. Before performing this procedure, you must be familiar with 2630 operation as described in the *2630 Fourier Analyzer User's Guide*.

NOTE: Perform this test only if the *2630 System Test Procedure* fails and you suspect a problem with the DBE Board.

Equipment Requirements

This test procedure requires the following equipment:

- Host computer (IBM PC or equivalent)
- Option 2H (two channel zoom) for a two- channel system or Option 3H (four channel zoom) for a four-channel system
- Small screwdriver
- Digital multimeter (DC volts and AC volts, 1% accuracy)
- 2630 test setup diskette (part number 100-109704-00)
- Safety glasses

If the 2630 system test setup files are not on the host computer hard disk, copy the files from the test setup diskette into the Instrument Program directory using the DOS command:

```
copy *.*
```

Test Setup

1 With the 2630 power off, remove the 2630 cover (see Section 3).

2 Make sure that DBE Board jumper J1 is installed.

3 Power up the 2630 and the host computer and start the Instrument Program.

DBE Calibration

4 Use the Instrument Program STORAGE function to call up the STUP file.

5 Observe the 500 Hz sine wave in the upper display.

6 Set the output of the sine wave for 10 volts.

7 Measure the 2630 output jack with the DVM set for AC on the 20-volt range.

8 Adjust R101 on the DBE Board until the voltmeter reads between 7.00 and 7.14 volts. See Figure 2-4.

If you are unable to adjust the voltage to within the specifications, continue with Step **9**. If you are successful, go to Step **14**.

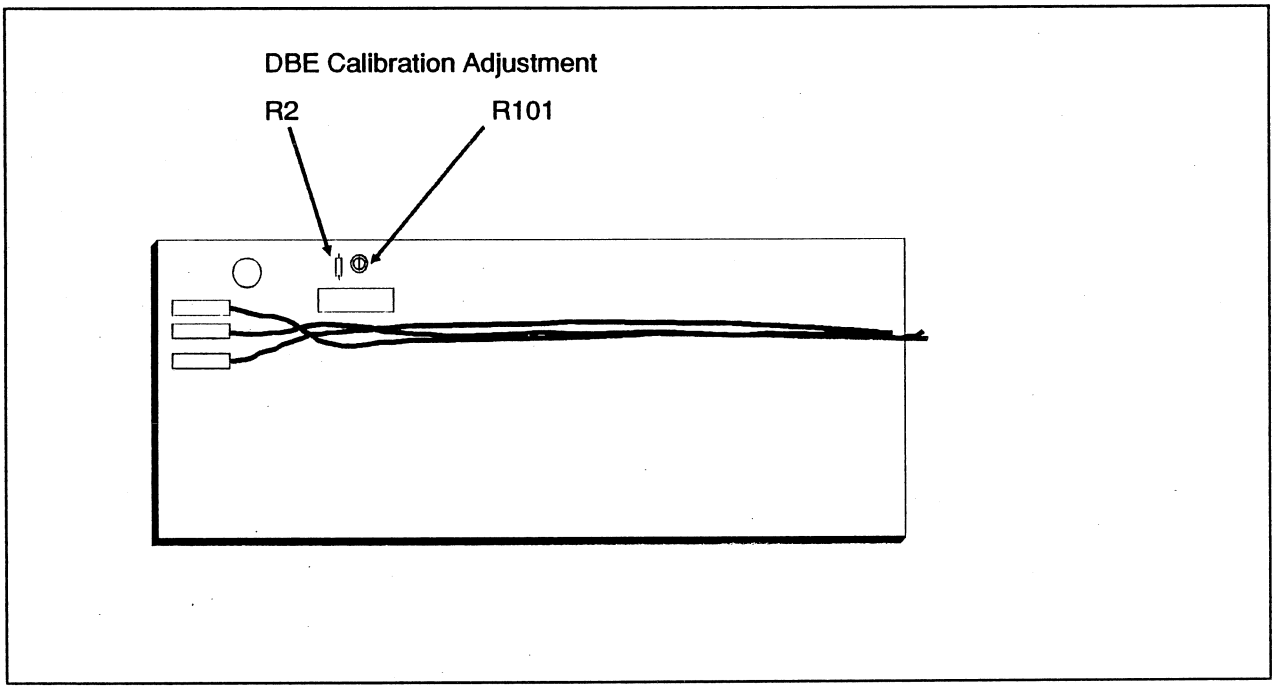


Figure 2-4. DBE Board Calibration Adjustment

9 Center R101.

10 Measure and record the output voltage from Step 7.

11 Press "Q" to quit the Instrument Program and run DBECAL. Follow the program's instructions and the program will specify a resistor value to place in parallel with R2 on the DBE Board.

12 Select a standard size resistor (5%, 1/4 watt) closest in value to the resistance the DBECAL program recommended.

13 Power down the 2630 and solder the resistor in parallel with R2 (see Figure 2-3). Return to Step 1 and repeat the DBE calibration test.

Check Output Loopback

14 Set the output sine wave to 5 volts.

15 Set the upper display to Ch=2 and the input coupling mode to > < (loopback). You should see a sine wave.

16 Set the upper display to Ch=1 and the input coupling to > <. You should see a sine wave.

17 If the 2630 has four channels, repeat Steps **15** and **16** for channels 3 and 4.

Harmonic Distortion

This test requires the Zoom Option.

18 Use the instrument Program STORAGE function to call up the HDTST file.

19 Press "R" to run. Harmonics at 10 kHz should be -76 dB or lower.

Function Generator

20 Select OUTPUT and, by observing the Channel 1 input on the upper display and ASPEC i on the lower display, check that all of the output functions work:

Sine
Square
Sawtooth
Triangle
Random
Adj-Rand
Impulse

Filter Ripple

21 Use the Instrument Program STORAGE function to call up the DBEFRTST file.

22 Connect a coax cable (with jumper clips on one end) between Input Channel 1 and TP21 on the DBE Board. Connect the ground clip (from the coax shield) to the J3 connector shell.

23 Connect a coax cable (with jumper clips on one end) between Input Channel 2 and U50 pin 1 (center conductor) on the DBE Board. Connect the ground clip (from the coax shield) to J3 connector shell.

24 Press "R" to run. The lower display (Y-axis 5 dB to 4 dB) should show the DBE filter ripple. The filter ripple should not vary more than 0.3 dB.

If the board successfully passes all of the above tests, it is probably okay. If it fails any one of the tests, replace it.

Adjusting the Power Supply

To adjust the 2630 power supply, you have to remove several 2630 assemblies. Due to the complexity of this procedure, do not attempt it unless absolutely necessary.

Equipment Requirements

This adjustment procedure requires the following equipment:

- Digital multimeter (DC volts and AC volts, 1% accuracy)
- Small screwdriver (preferably non-metallic)
- Safety glasses

Getting to the Power Supply

1. Turn off the 2630 power and disconnect the ac power cord.
2. Remove the 2630 cover (see Section 3 if necessary).
3. Remove the four screws that hold the front panel. See Figure 2-5.
4. Remove the three stiffener screws from the bottom. See Figure 2-6.
5. Remove six screws from the rear panel. See Figure 2-7.

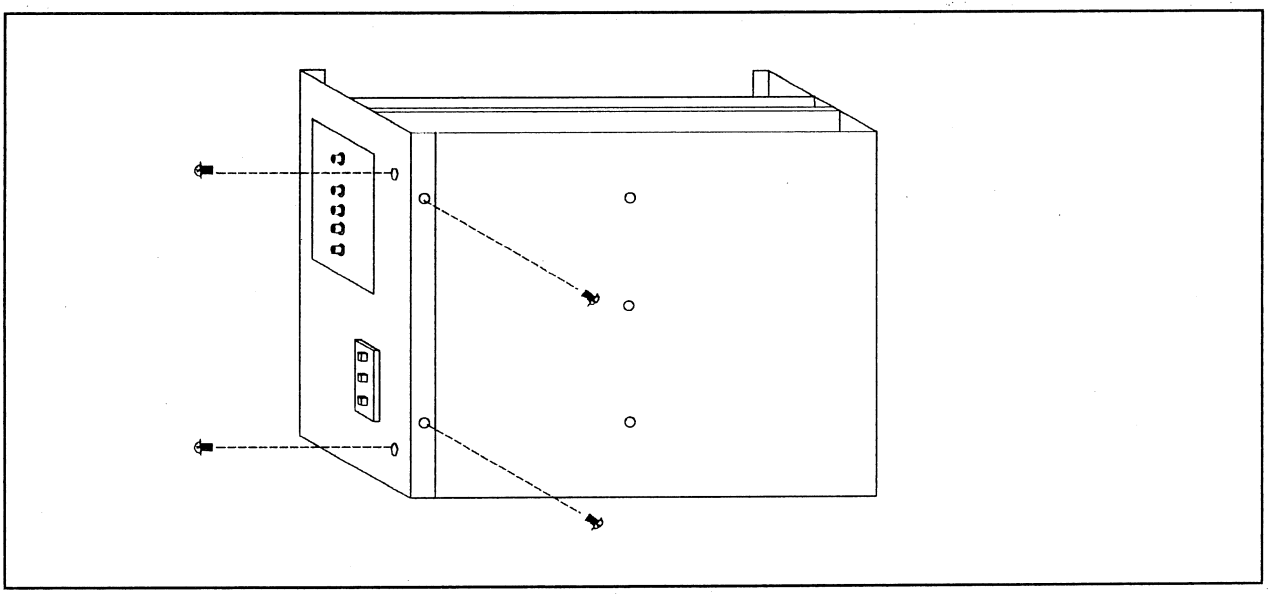


Figure 2-5. Removing the Front Panel Screws

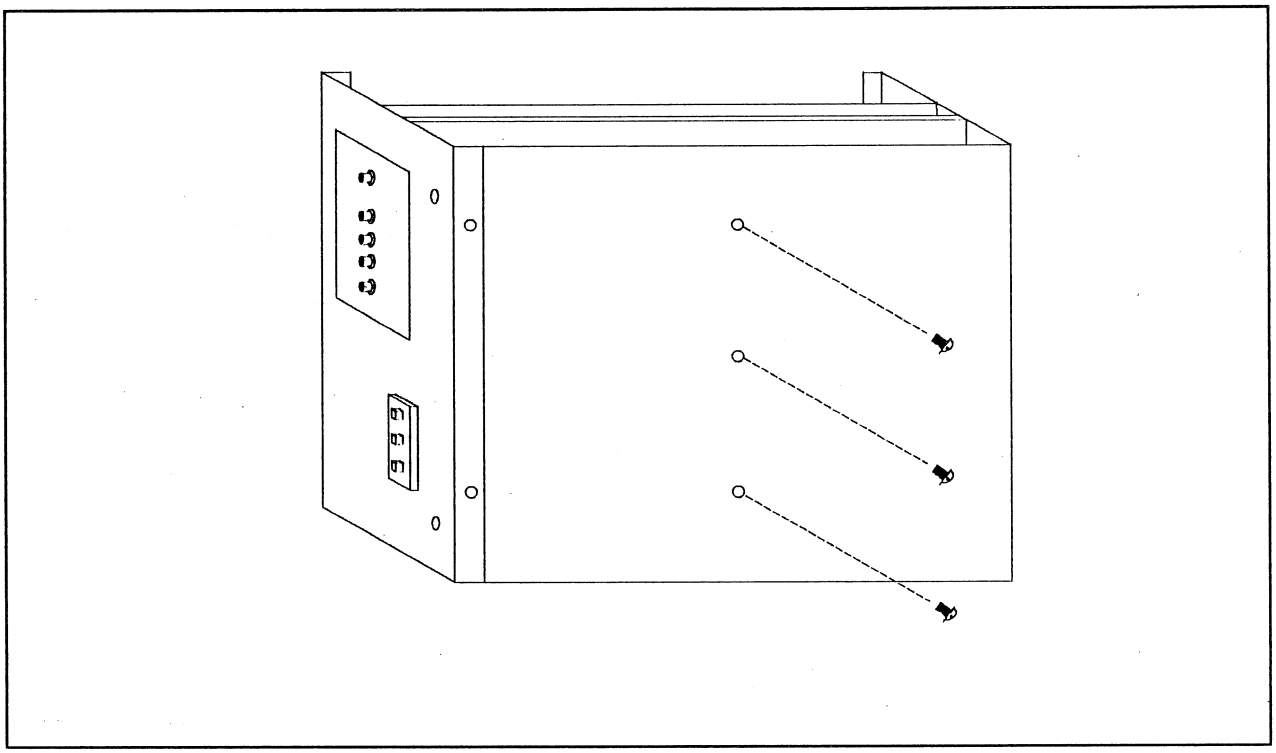


Figure 2-6. Removing Three Screws from the Bottom

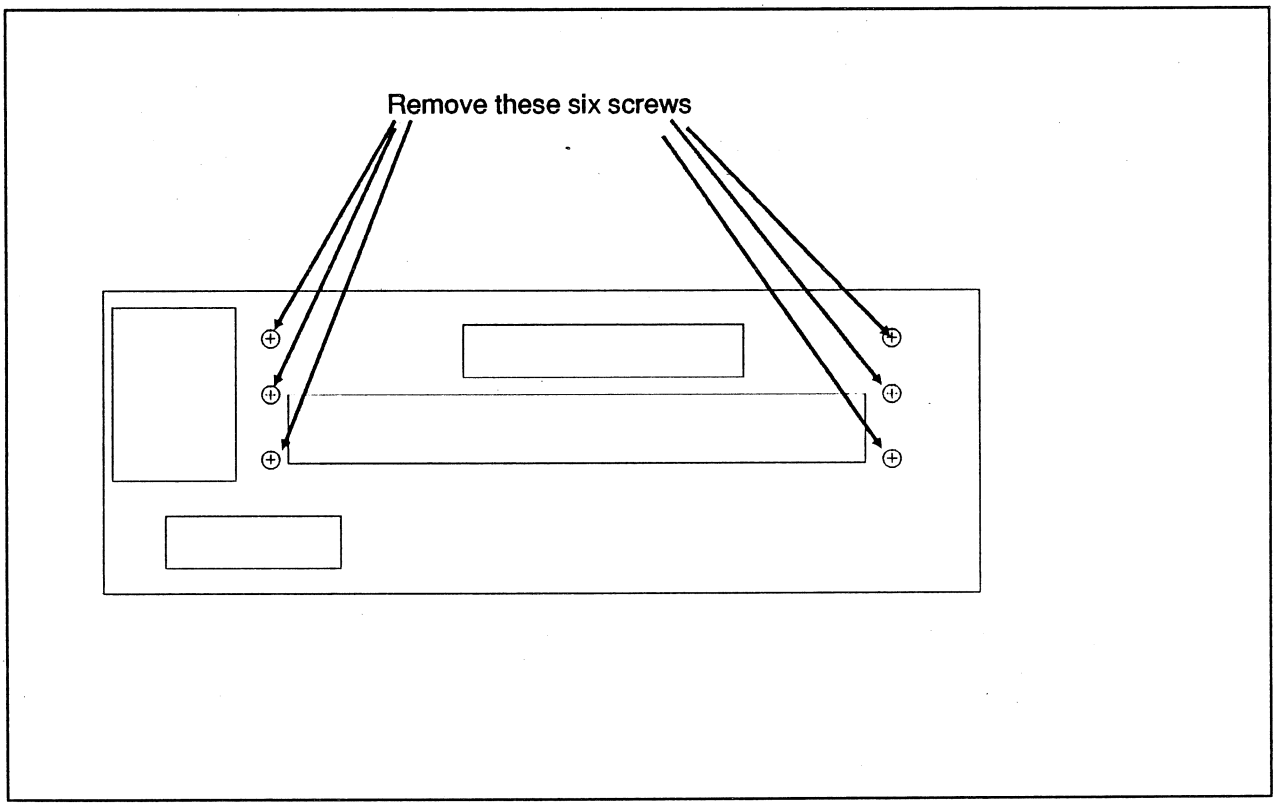


Figure 2-7. Removing the Six Screws from the Rear Panel

6 Carefully lift up the platform containing all of the printed circuit boards, rotate it 180 degrees, and set the entire assembly off to the left side of the chassis (looking at it from the front) onto an insulated surface.

7 Plug in the 2630 and power it on.

8 Check the power supply voltages at the test points listed below. Adjust the power supply if necessary. See Figures 2-8 and 2-9.

Voltage	Test Point
Ground	DFE Board TP-16
+5V	DFE Board U48 pin 20
+15V	DFE Board U23 pin 4
-15V	DFE Board U23 pin 11

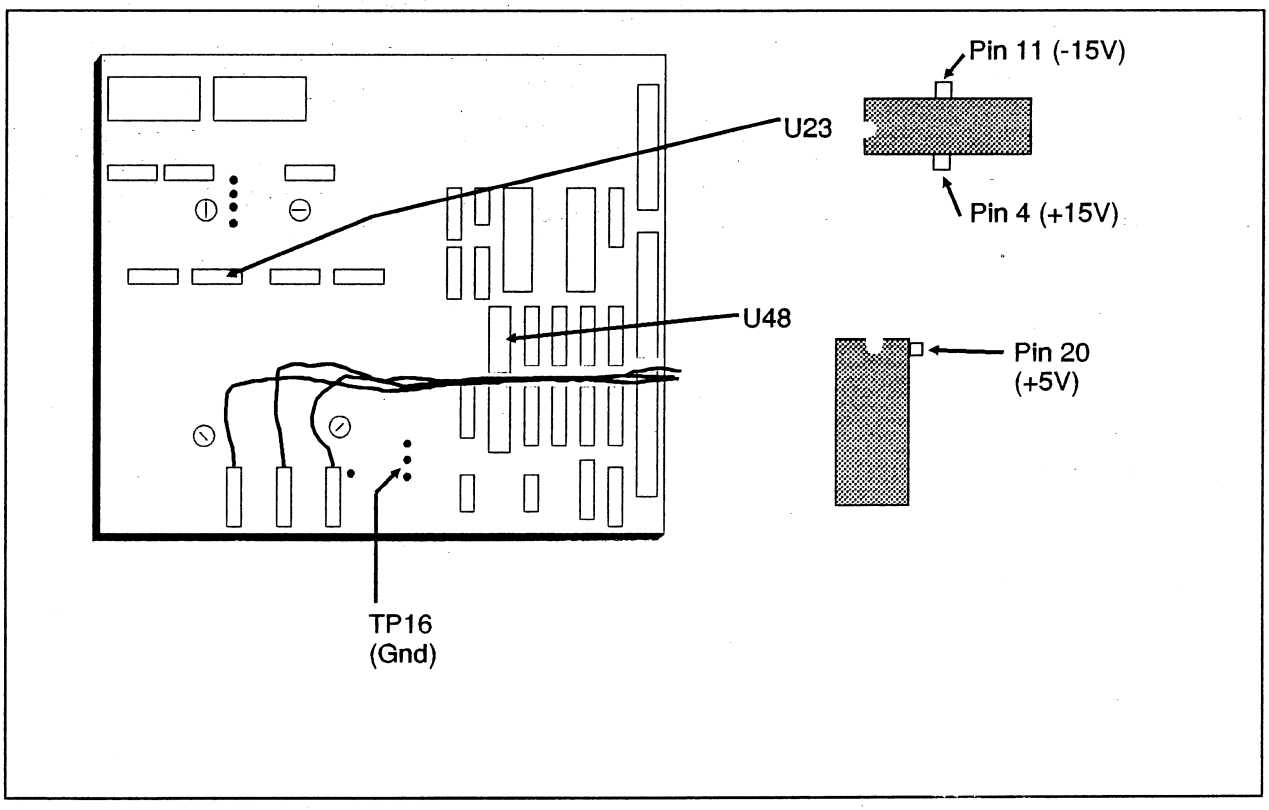


Figure 2-8. DFE Board Test Points

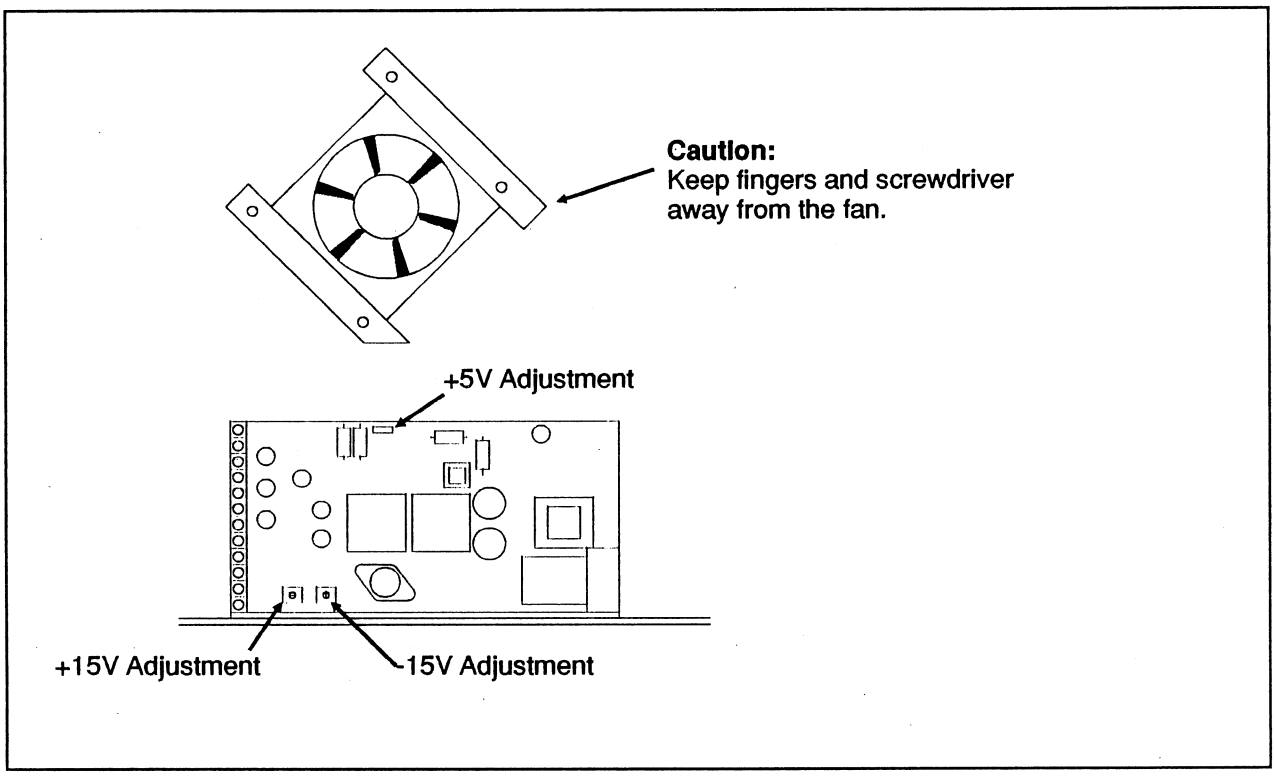


Figure 2-9. Power Supply Adjustments

Changing the 2630 Operating Voltage

The 2630 operating voltage is defined by a voltage selector card on the power module on the 2630 rear panel. To change the 2630 operating voltage:

1 Turn off the 2630 power and unplug the power cord.

2 Use a small screwdriver to pry out the fuse holder from the power module. See Figure 2-10.

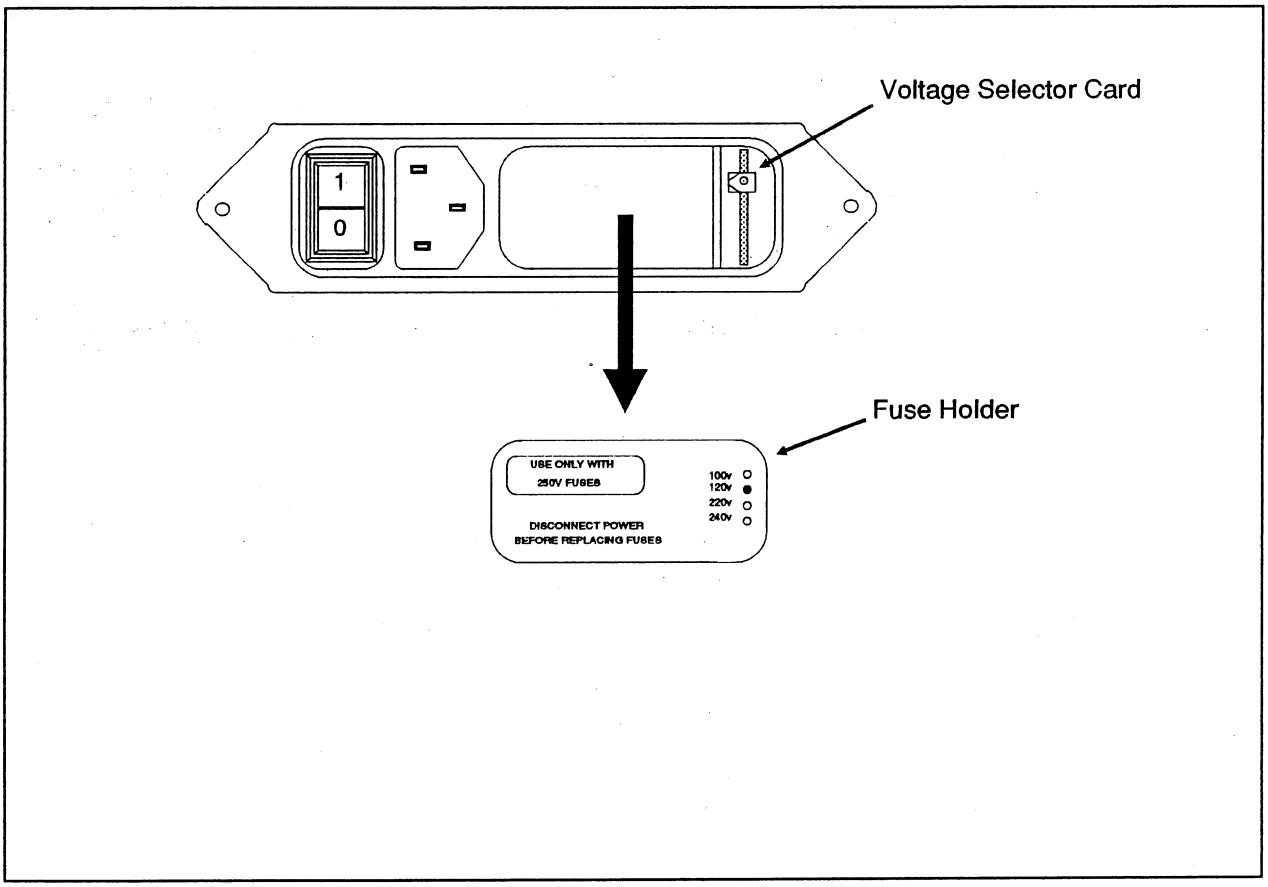


Figure 2-10. Removing the Fuseholder

3 Remove the voltage selector card from the power module and rotate the voltage selector pin 180 degrees, as shown in Figure 2-11.

4 Replace the voltage selector card.

5 The voltage indicator pin shows through the 240-volt window.

When changing the operating voltage, normally you must also change the fusing arrangement. North American operation on 120-volts uses only one fuse. European operation on 220-volts uses two fuses. See *Changing the Fusing Arrangement*, on the next page.

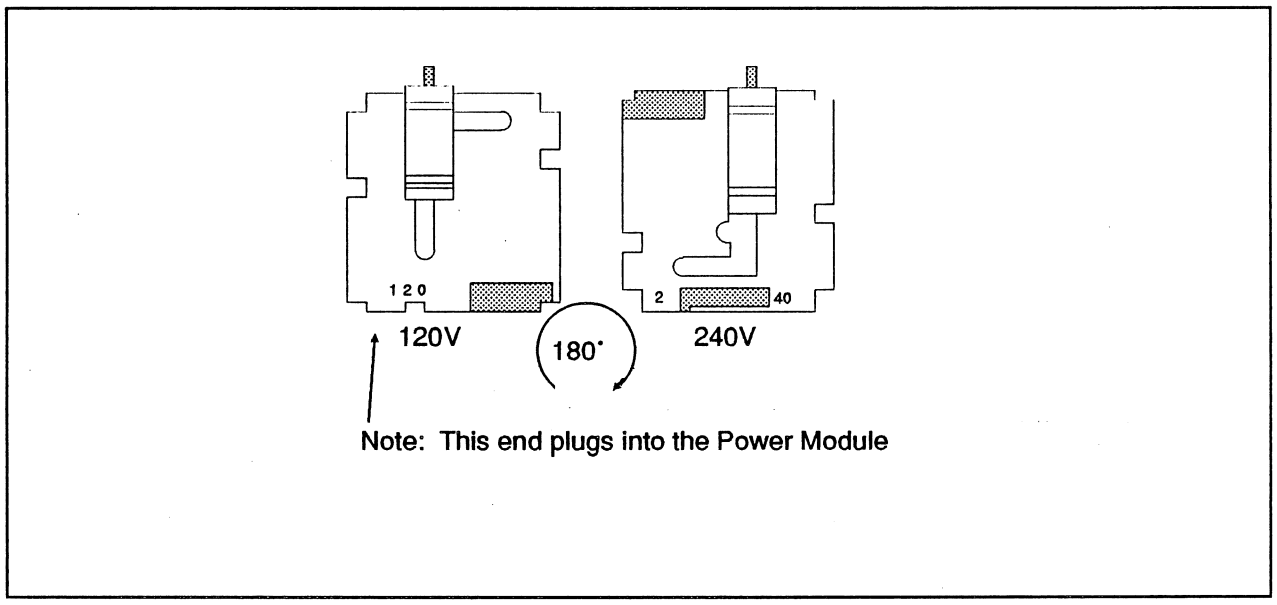


Figure 2-11. Voltage Selector Card

Changing the Fusing Arrangement

The 2630 can accommodate either the North American fusing arrangement (one fuse) or the European fusing arrangement (two fuses). To change from one fusing arrangement to the other:

1 Remove the fuse holder from the power module as described in Steps 1 and 2 under *Changing the 2630 Operating Voltage*.

2 Loosen the screw that holds the fuse block to the fuse holder cover and remove the fuse block. See Figure 2-12.

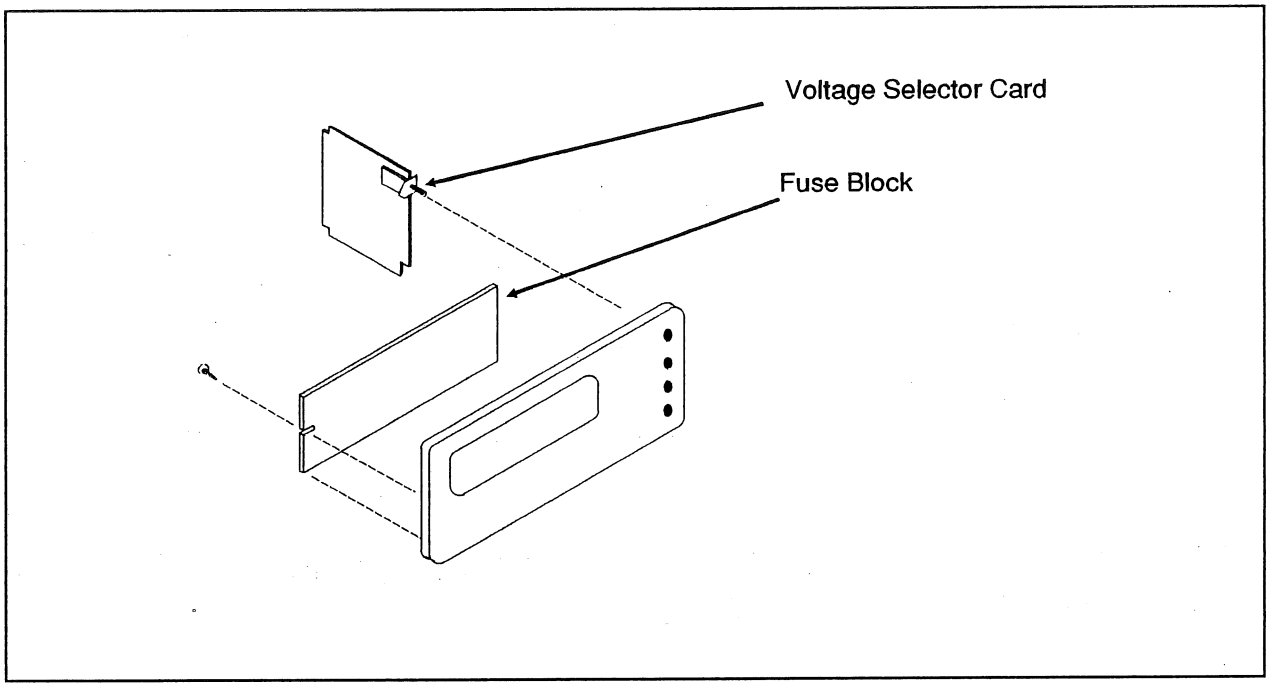
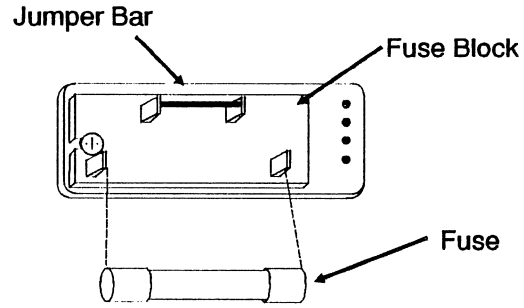


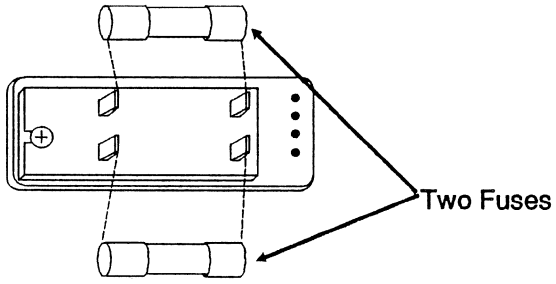
Figure 2-12. Removing the Fuse Block from the Fuse Holder

3 Flip the fuse block over and reinstall it to the cover. See Figure 2-13.

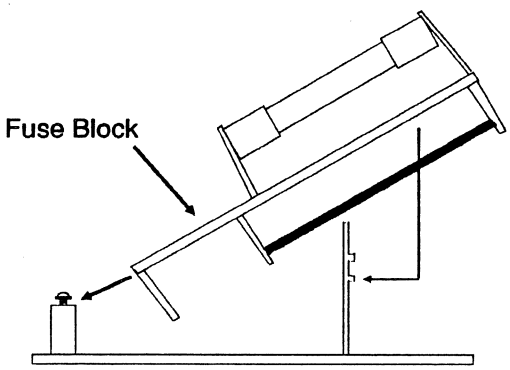
4 Replace the fuse block and cover assembly in the power module.



North American Fusing Arrangement
105 to 125 Vac
Fuse: 2 Amp 250 Volt, Slow Blow
Buss BK/MDX-2 or Equivalent.



European Fusing Arrangement
207 to 253 Vac
Fuse: 1 Amp 250 Volt, Slow Blow
Buss BK/GDC-1A or Equivalent.



Fuse Block/Cover Assembly

Figure 2-13. Changing the Fusing Arrangement

2630 Calibration Procedures

The following procedure explains how to:

- Verify that the 2630 is properly calibrated.
- Calibrate the 2630 using the optional Output Channel.
- Calibrate the 2630 using an external signal source in place of the optional Output Channel.

Equipment Requirements

This test procedure requires the following equipment:

- A signal generator (preferably a synthesizer) capable of generating a 500 (±2.5) Hz sine wave from 0.5V to 10V peak, with less than -65 dB harmonic distortion.
- An ac voltmeter capable of measuring 0.4 to 7.5 VRMS with an accuracy of 0.5% or better.
- Host computer (IBM PC or equivalent).
- Coax cable and coax "T" connectors to connect the signal generator to the input BNC connectors on the 2630.

System Setup and Software Installation

1. Connect the 2630 to the host computer as described in the *2630 User's Guide.*
2. Turn on the host computer and the 2630.
3. Start the Instrument Program (enter "IP"). The host computer downloads code to the 2630 and the Transfer indicator blinks. After initialization, the Instrument Program appears on the host screen.
4. Proceed to one of the following paragraphs:

   Verifying 2630 Calibration
   Calibrating the 2630 Using the Output Option
   Calibrating the 2630 Using an External Signal Source

Verifying 2630 Calibration

To verify the 2630 calibration:

1. Set the external signal source for a 500 (±5) Hz sine wave at 10 (±0.05) volts peak (7.07 ±0.035 volts RMS) and connect to 2630 Input Channel 1.

2. Use the Instrument Program STORAGE function to call up the 2630CAL program. This retrieves a setup file to set the parameters of the Instrument Program for measuring the calibration signal.

3. Press the F6 key. This positions the cursor on a 500 Hz spectral line on the lower display.

4. Verify that the frequency is 500 Hz and that the value is 10.0 (±0.2) volts. If the value is within specifications, proceed to Step 5. If the value is not within specifications, proceed to *Calibrating the 2630 Using an External Signal Source.*

5. Set the external signal source for a 500 (±5) Hz sine wave at 5 (±0.025) volts peak (3.53 ±0.017V RMS). Connect the signal source to 2630 channel 1.

6. Press the L key on the keyboard to move the cursor to the lower display.

7. Use the left or right arrow keys to position the cursor on the voltage range, presently set for 10V.

8. Use the down arrow key to reduce the voltage range to 7.1V.

9. Verify that the voltage read at 500 Hz is 5 (±0.1) volts.

10. Change the input voltage to one of the settings below and verify the resulting reading. Repeat the test for each of the settings given.

Frequency	Source Voltage Peak	Source Voltage RMS	2630 Range	2630 Meas. Volts
500	5 ±0.25	3.53 ±0.017	5	5 ±0.1
500	2 ±0.01	1.414 ±0.007	2.4	2 ±0.04
500	0.6 ±0.003	0.424 ±0.002	0.63	0.6 ±0.012

11. Repeat Steps 1 through 10 for all 2630 channels.

Calibrating the 2630 Using the Optional Output Channel

To calibrate the 2630 with the internal Output Channel option:

1. Use the Instrument Program STORAGE function to call up the 2630DBE program.
2. Connect the ac voltmeter to the Output BNC connector.
3. Verify that the voltage is 7.07 ±0.07 volts RMS. If the voltage is within the specification, go to Step 4. If the voltage is not within the specification, return the 2630 to Tektronix for repair.
4. Press the Q key (for Quit), then press the W key. The 2630 starts the auto-calibrate mode.

After about 15 to 30 seconds, the auto-calibrate mode displays a table of factors for each gain range on all channels. The 2630 uses these factors to compensate input data, providing excellent accuracy. The gain factors (16 factors per channel) are normally between 0.95000 and 1.05000. The offset factors are normally between -100 and +100.

Calibrating the 2630 Using an External Signal Source

If the 2630 does not have the Output Channel Option, you can calibrate the 2630 using an external signal source, as described below. The external signal source must be able to generate the following sine wave test signals.

- 0.5 volts peak (0.353 RMS) ±10%, 500 Hz ±2.5 Hz.
- 10.0 volts peak (7.07 RMS) ±0.5%, 500 Hz ±2.5 Hz.
- Harmonic distortion and noise 65 dB down.

The amplitude accuracy of the 10.0 volt signal determines the calibration accuracy of the 2630.

The 2630 input impedance is 100K ohms per channel. For a four channel system, the input impedance is 25K ohms. If your external signal source output impedance is 600 ohms, you will have an error of 2.4%. You must set or measure your source voltage after connecting it to all the 2630 Input channels to accommodate for this loading.

If the source frequency is unknown, use the Instrument Program to set the frequency to 500.00 Hz. Select the BoxCar window and the 1 kHz range. Adjust the source until the leakage is minimum when observing the instantaneous power spectrum. This is not too critical, since the calibration program uses the Flattop window.

To calibrate the 2630 with an external signal source:

1 Use coaxial cable and appropriate BNC connectors to connect the external signal source to all 2630 Input channels, simultaneously.

2 Quit the Instrument Program.

3 While in the Instrument Program subdirectory, enter the following command and press Return (note that if the DOCAL program is not in your Instrument Program subdirectory, you will have to copy it from your distribution disk):

```
DOCAL
```

4 Follow the instructions on the screen as the calibration program prompts you through the procedure.

CAUTION

When prompted, the calibration program will change the calibration factors in the 2630 EEROM (Electrically Erasable ROM). To use the new calibration in the 2630, you must respond "Yes" to this prompt.

The calibration program writes the calibration factors into a file called SP.CAL in the Instrument Program subdirectory. This file is used by older analyzers that are not equipped with the EEROM.

The calibration file is standard ASCII. The second column in the file has the gain factors. These factors should be between 0.94 and 1.06. If the factors are outside of these values, you may either have an inaccurate source or a defective 2630.

3

Disassembly and Assembly

Overview

This section illustrates and describes how to disassemble and assemble the 2630.

Contents **Page**

Removing the 2630 Cover

The 2630 cover is attached with six screws to the bottom chassis. To remove the top cover:

1. Turn off the 2630 and disconnect the power cord.
2. Lay down padding or packing material on a clean place on the work surface to protect the 2630.
3. Turn the 2630 upside down onto the padding.
4. Remove the six screws from the bottom of the chassis as shown in Figure 3-1.
5. Turn the 2630 back to the right-side up position.
6. Slowly slide the cover forward to remove it.

CAUTION:

Make sure that the cover does not catch on any internal cables or assemblies.

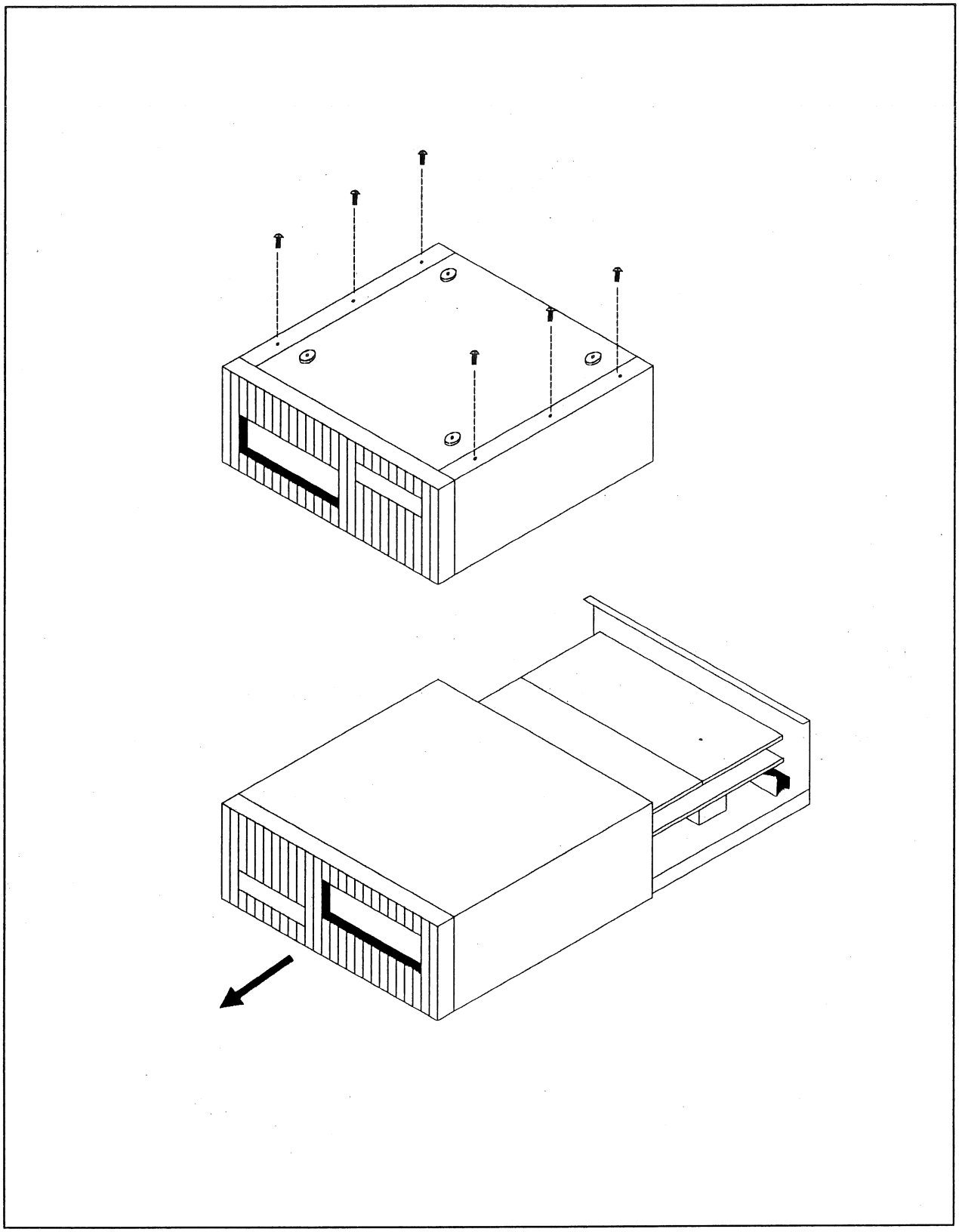


Figure 3-1. Removing the 2630 Cover

Removing the DFE Board(s)

To remove the DFE Boards:

1. Remove the 2630 cover as described under *Removing the 2630 Cover*.
2. Remove the three coax cables from the DFE Board. See Figure 3-2.
3. Remove the five screws that hold the DFE Board to the Mother Board or the lower DFE Board. See Figure 3-2.
4. Disconnect the three flat ribbon cables. See Figure 3-2.

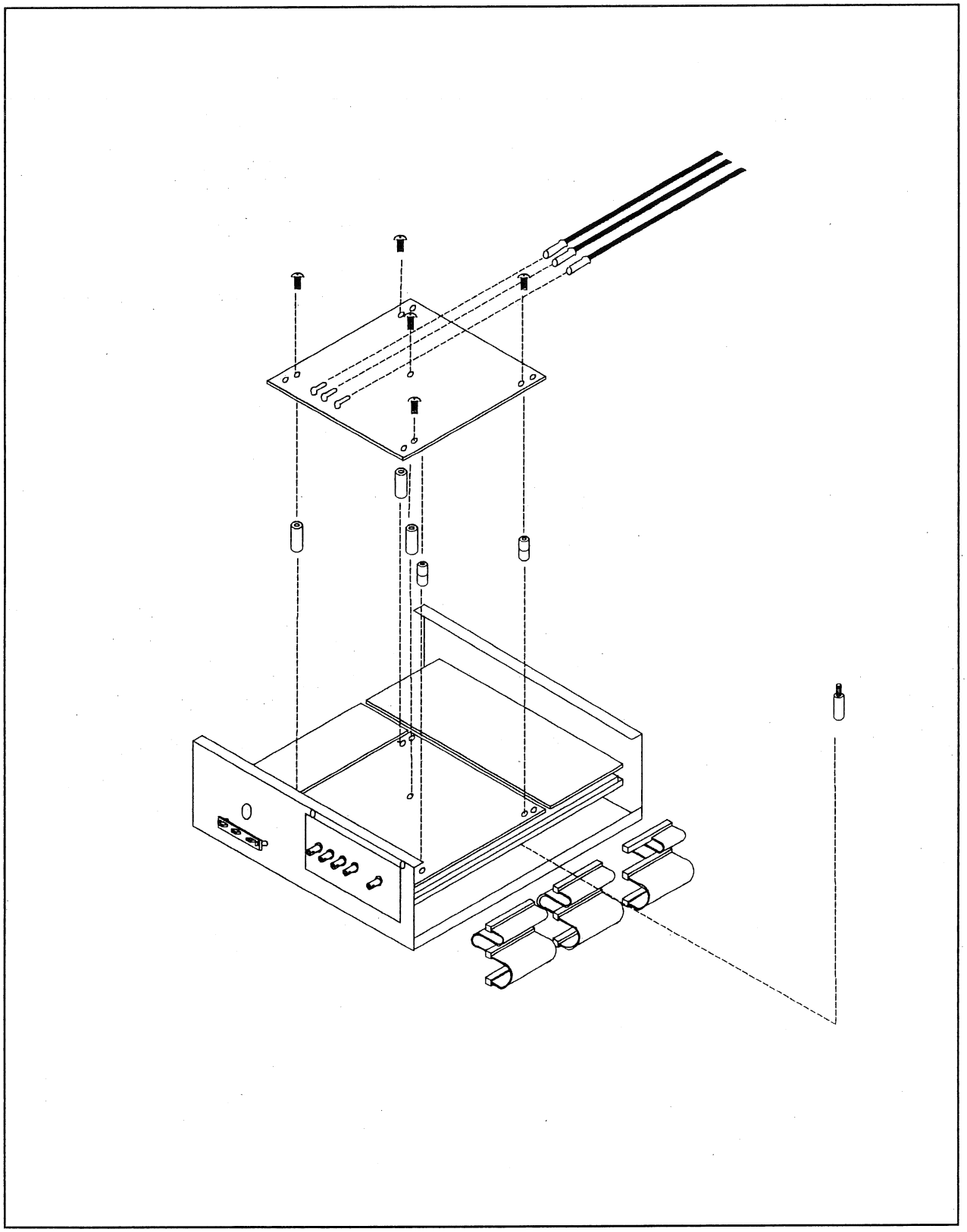


Figure 3-2. Removing the DFE Boards

Removing the DBE Board

To remove the DBE Board:

1. Remove the 2630 cover as described under *Removing the 2630 Cover*.
2. Remove the two or three coax cables from the DBE Board. See Figure 3-3.
3. Remove the five screws that hold the DBE Board to the Mother Board. See Figure 3-3.
4. Disconnect the flat ribbon cable. See Figure 3-3.

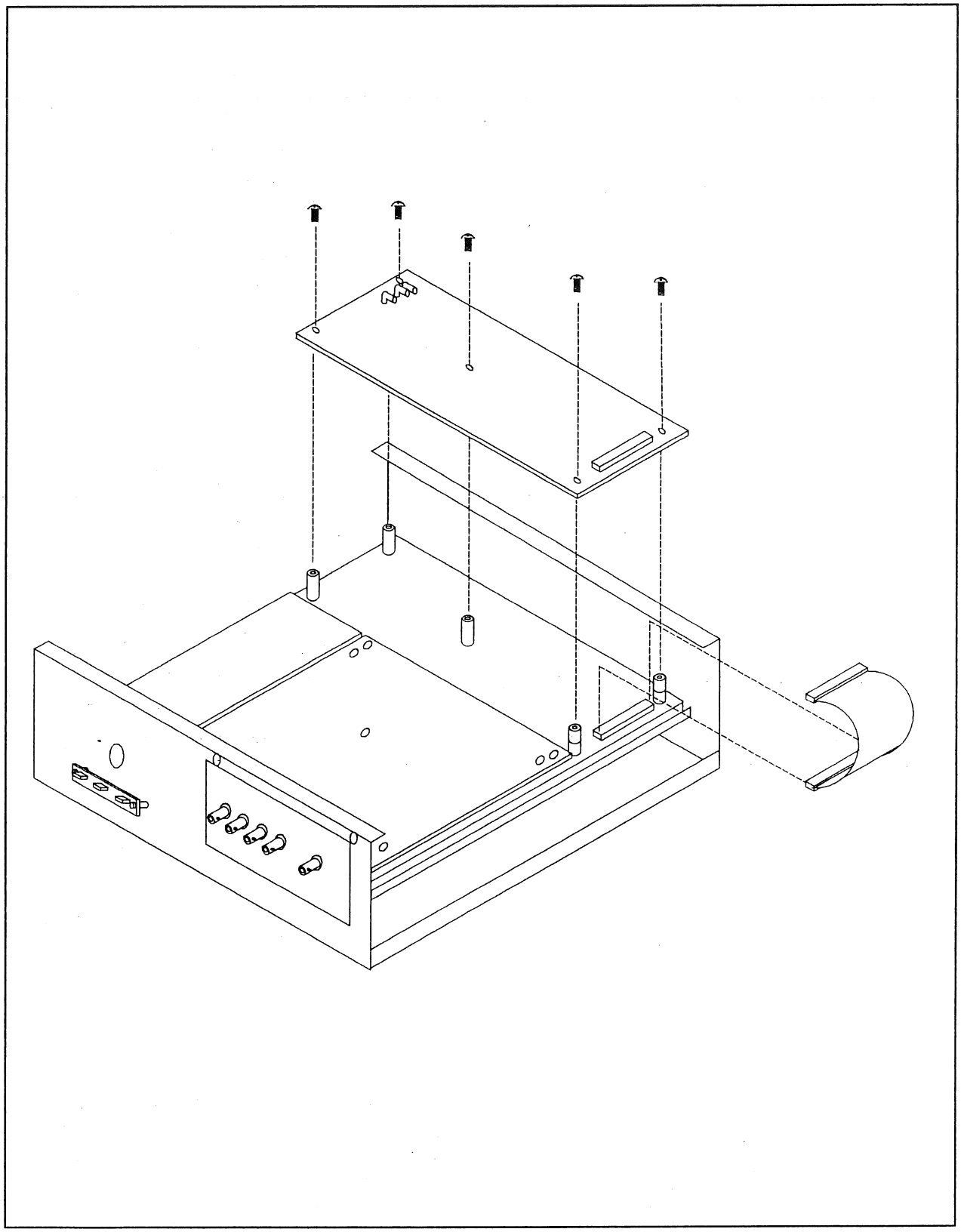


Figure 3-3. Removing the DBE Board

Removing the DIO Board

To remove the optional DIO Board:

1. Remove the 2630 cover as described under *Removing the 2630 Cover*.

2. Remove the four screws that hold the DIO Board to the FXP Board. See Figure 3-4.

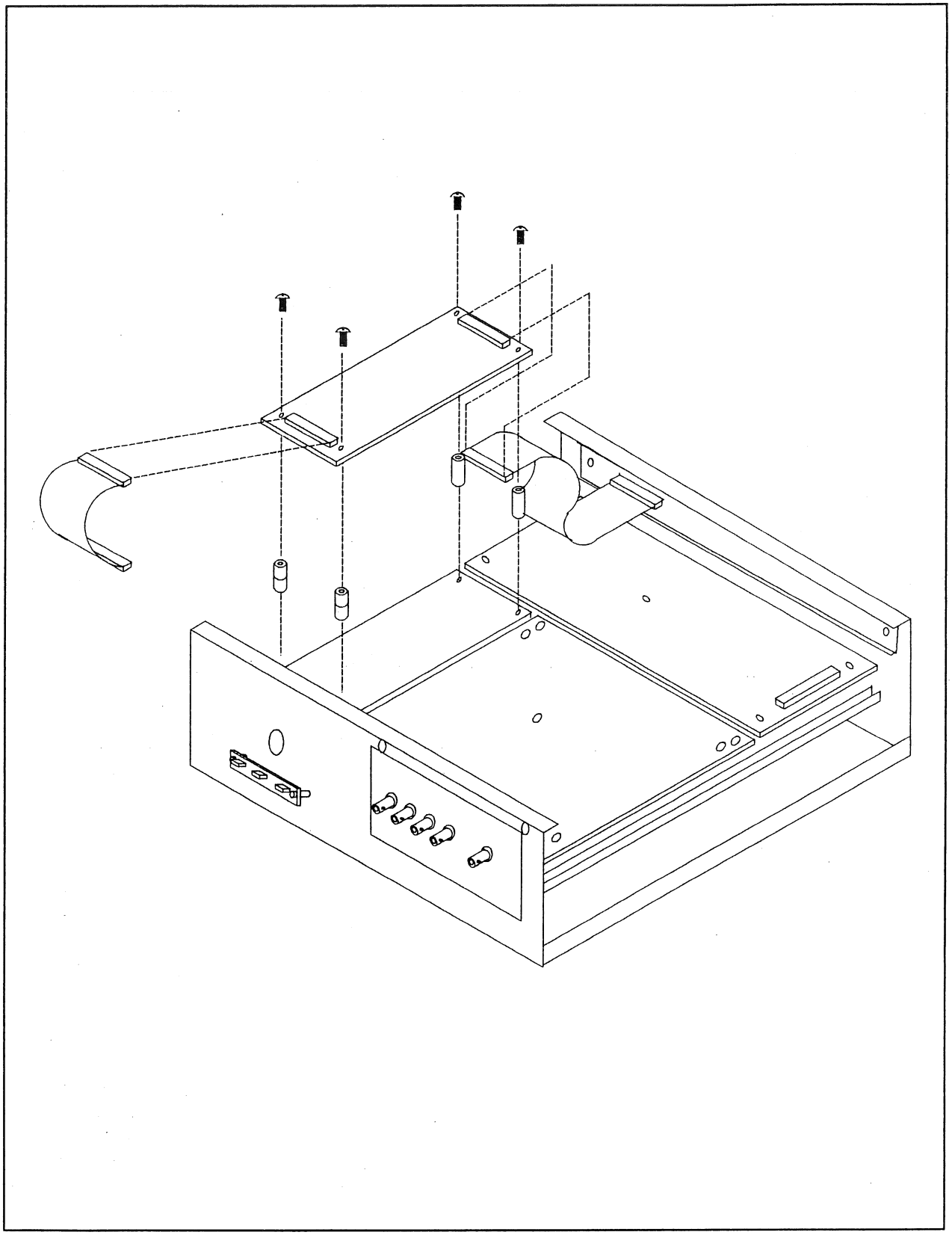


Figure 3-4. Removing the DIO Board

Removing the FXP Board

To remove the FXP Board:

1. Remove the 2630 cover as described under *Removing the 2630 Cover*.
2. If the optional DIO Board is installed, remove it as described above.
3. Remove the four screws that hold the FXP Board to the Mother Board. See Figure 3-5.
4. Disconnect the flat ribbon cable. See Figure 3-5.

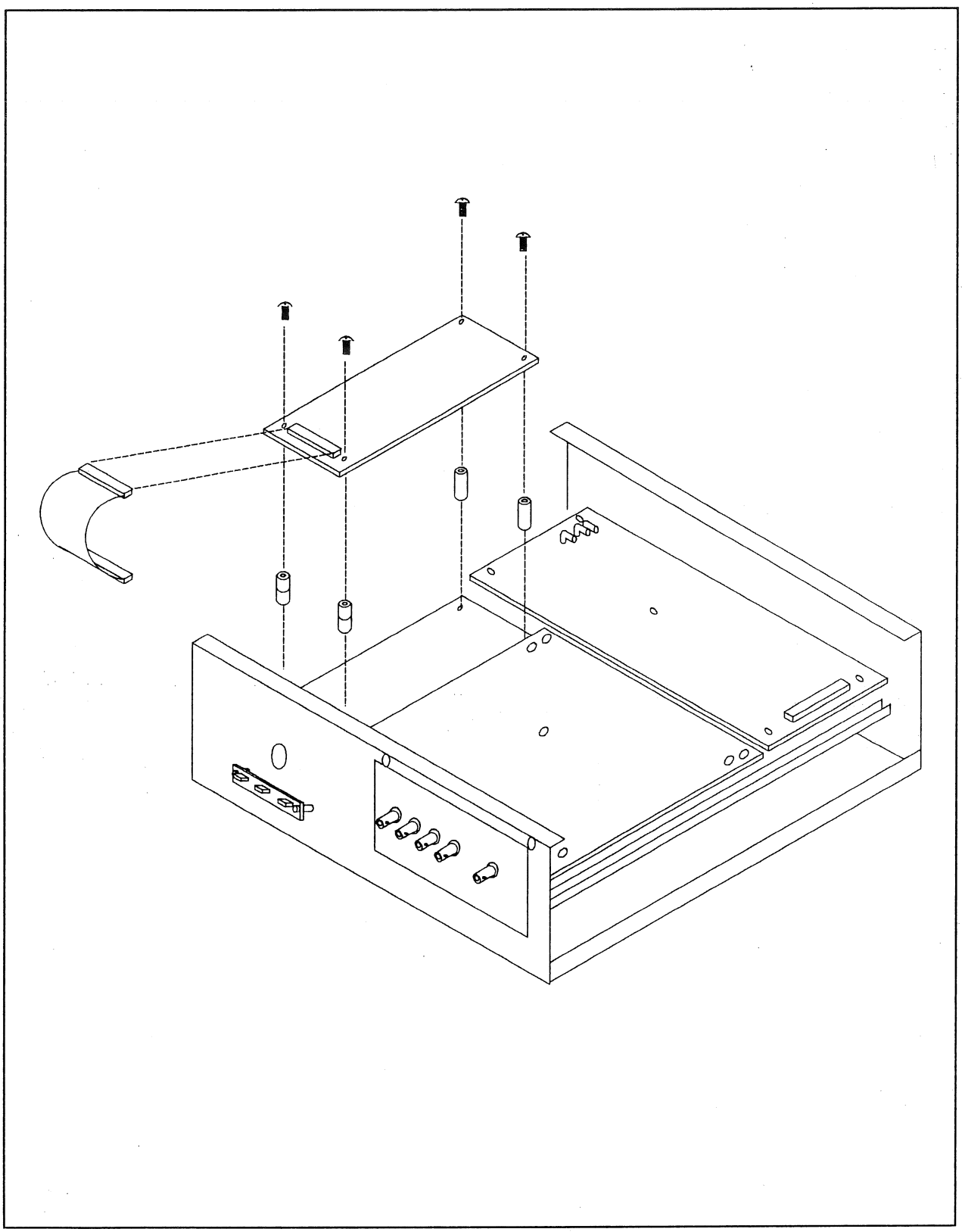


Figure 3-5. Removing the FXP Board

Removing the Mother Board

To remove the Mother Board:

1. Remove the 2630 cover as described under *Removing the 2630 Cover*.
2. Remove the DFE Board(s) as described earlier.
3. Remove the DBE Board as described earlier.
4. If installed, remove the DIO Board as described earlier.
5. Remove the FXP Board as described earlier.
6. Remove the four screws that hold the front panel. See Figure 3-6.
7. Remove the three screws from the bottom. See Figure 3-7.

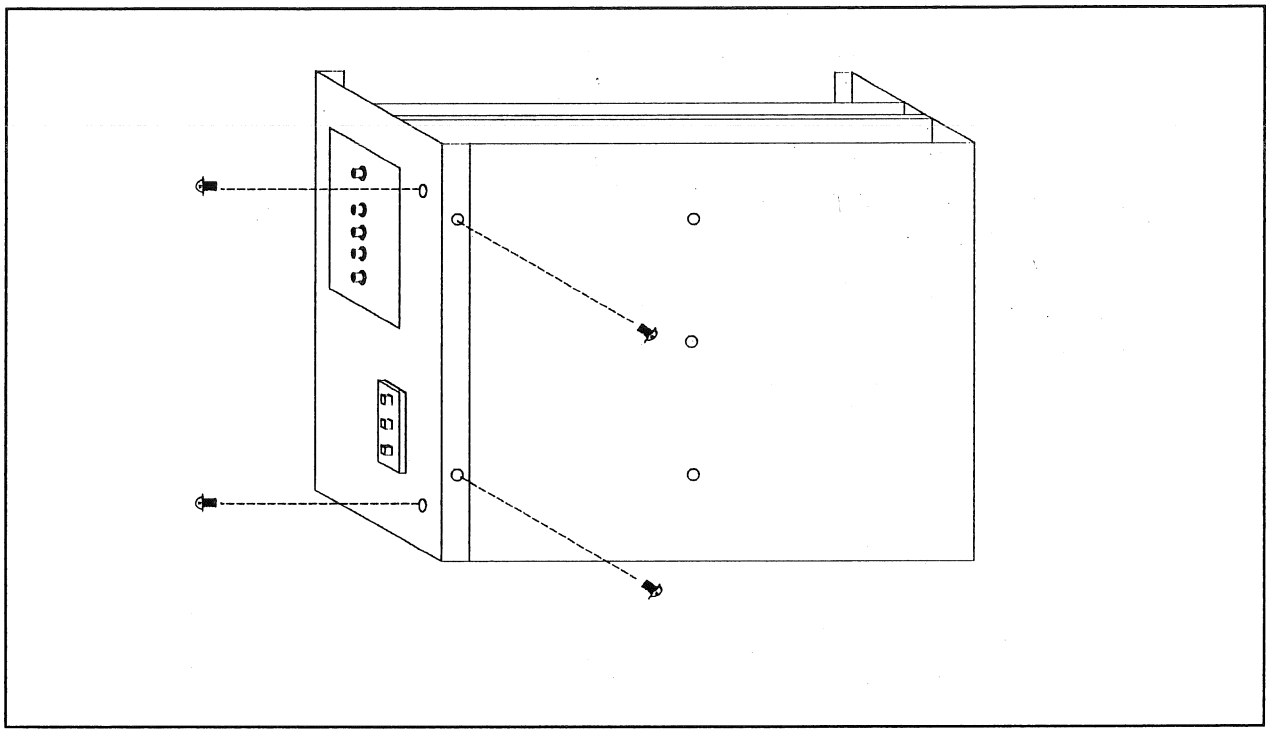


Figure 3-6. Removing the Front Panel Screws

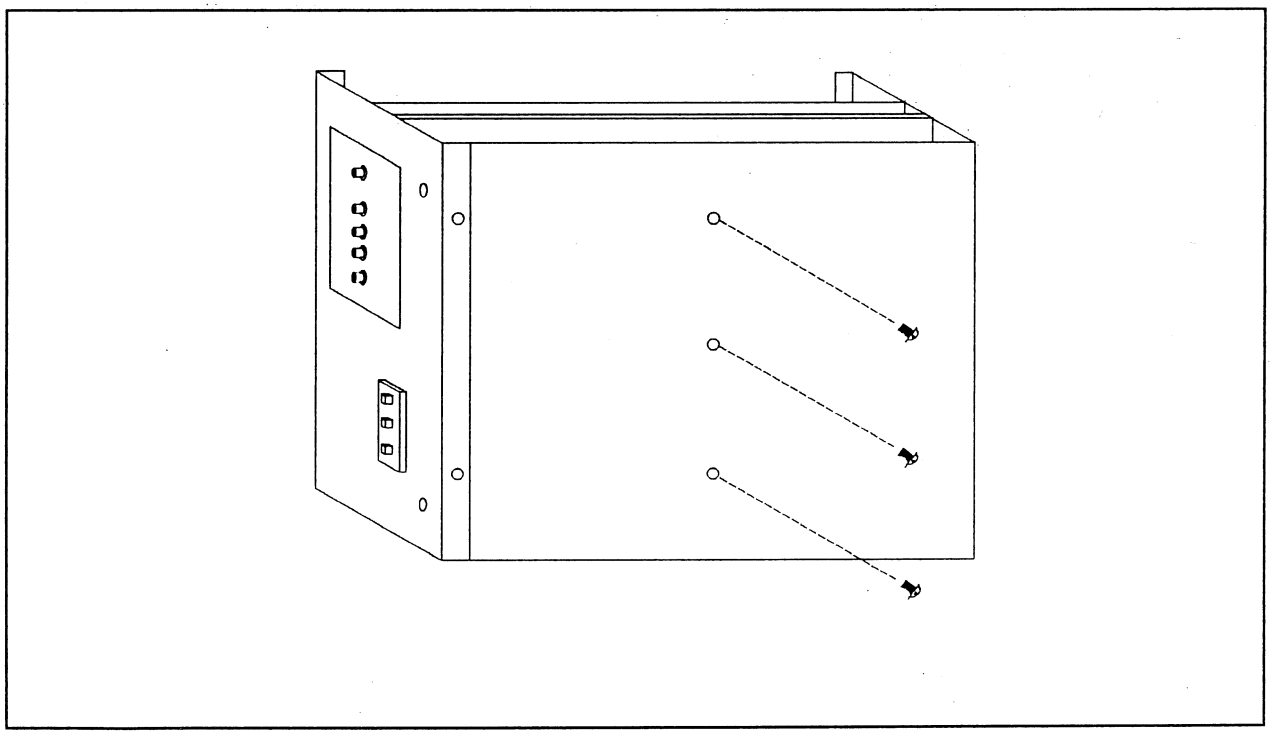


Figure 3-7. Removing the Bottom Screws

8 Remove the six screws from the rear panel. See Figure 3-8.

9 Disconnect the power supply cable from the underside of the Mother Board.

10 Carefully lift up the platform containing the Mother Board and remove it from the chassis.

11 Remove the nine screws that hold the Mother Board to the platform. See Figure 3-9.

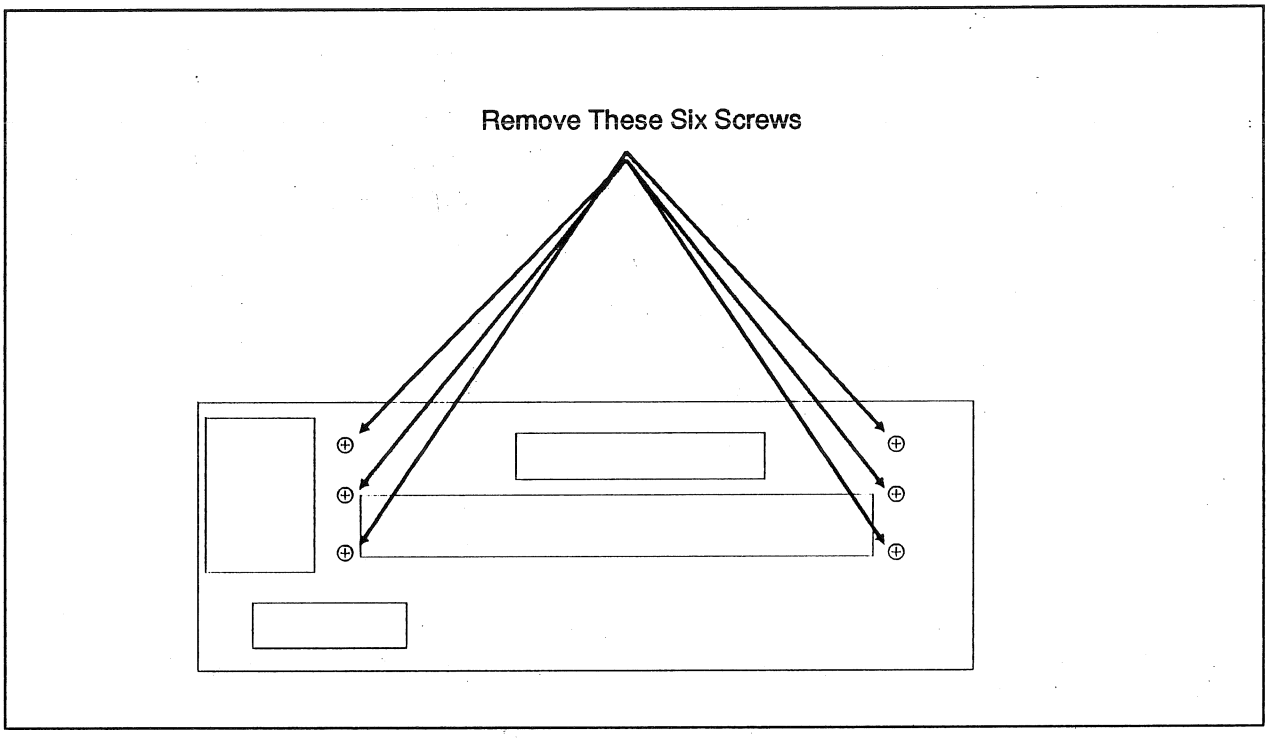


Figure 3-8. Removing the Rear Panel Screws

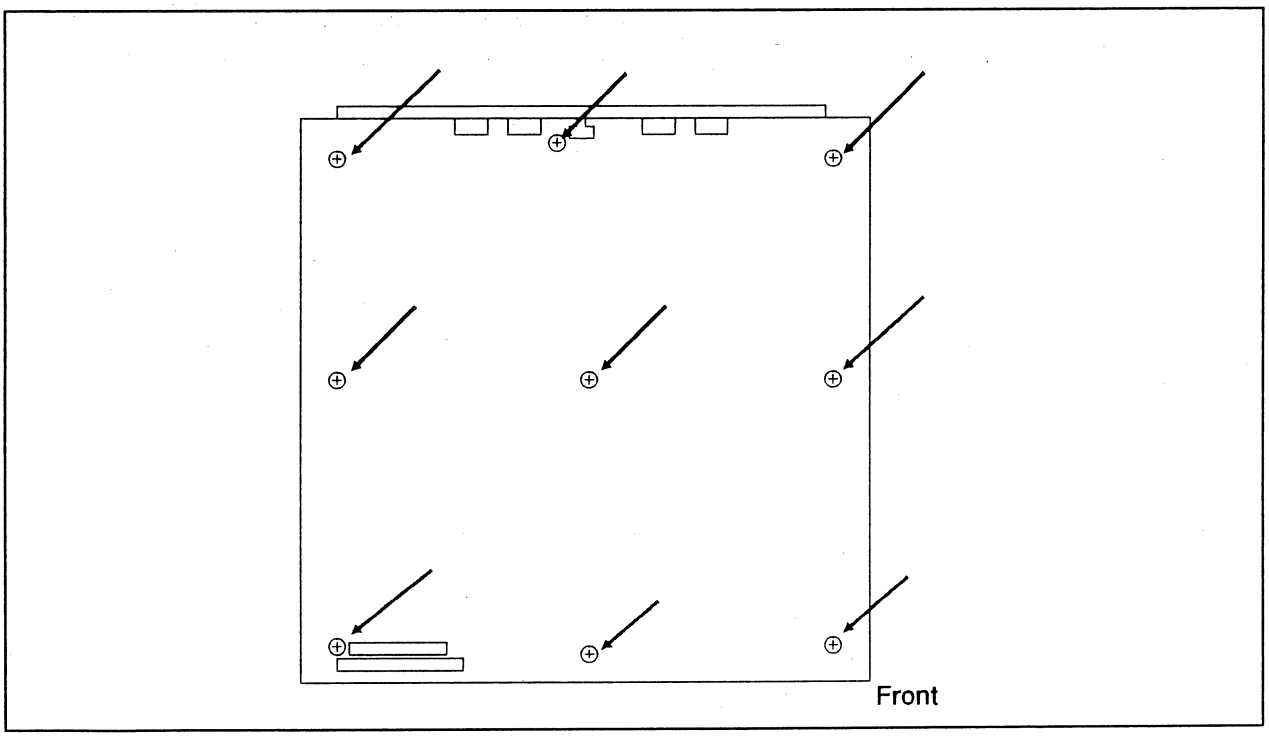


Figure 3-9. Removing the Mother Board Screws

Removing the Power Supply

To remove the power supply:

1. Remove the 2630 cover as described under *Removing the 2630 Cover*.
2. Remove the DFE Board(s) as described earlier.
3. Remove the DBE Board as described earlier.
4. If installed, remove the DIO Board as described earlier.
5. Remove the FXP Board as described earlier.
6. Remove the Mother Board as described earlier (Steps 1 through 10 only - do not remove the Mother Board from the platform).
7. Disconnect the three ac wires from the power supply. See Figure 3-10
8. Locate the two small wires that run from the power supply to the power module on the rear panel and disconnect the two wires from the power module.
9. Cut the cable ties that hold the ac wires.
10. Turn the chassis on its side and remove the two screws that hold the power supply to the chassis.

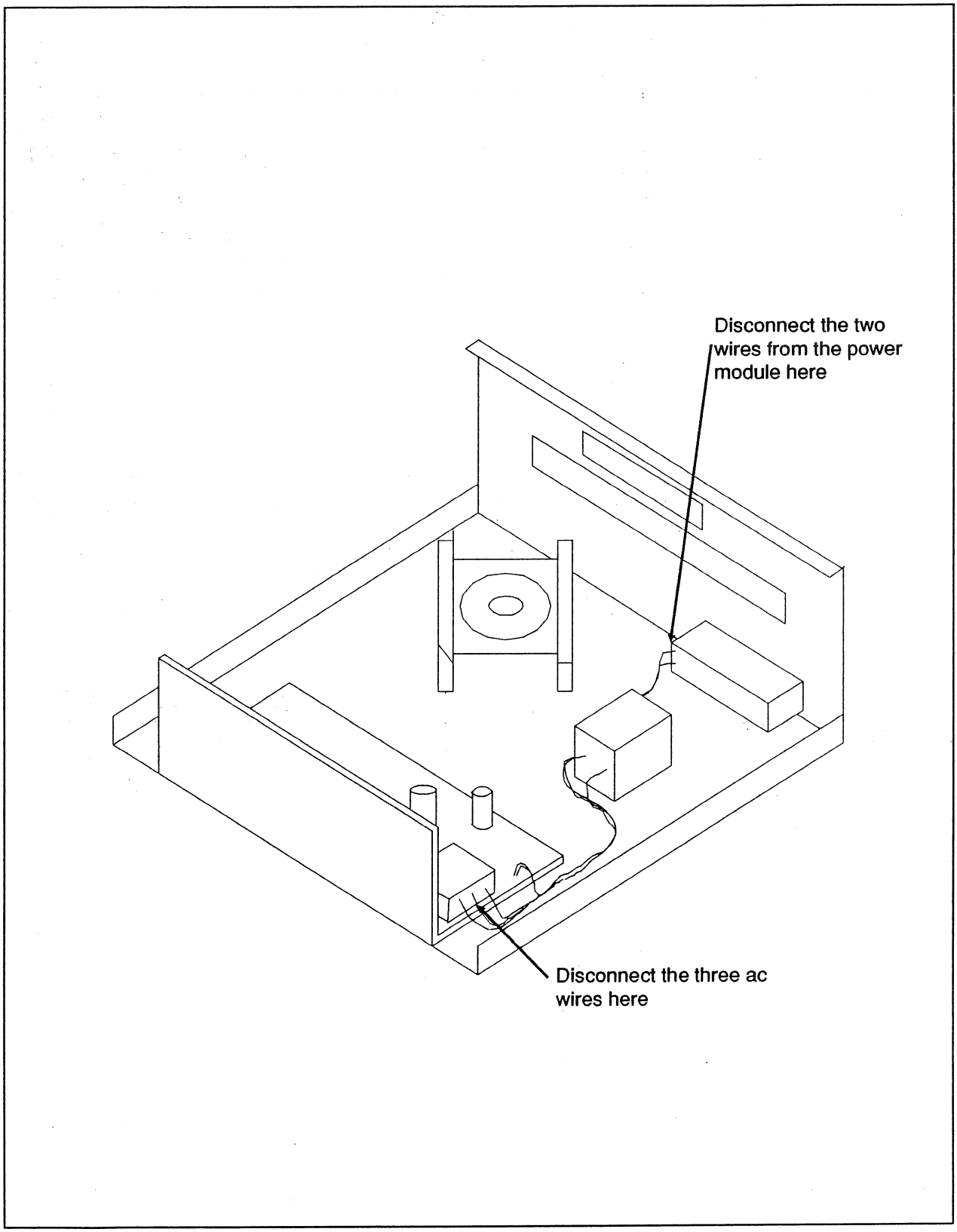


Figure 3-10. Power Supply

4

Technical Description

Introduction

This section provides an overview of the 2630 hardware to assist the test technician in understanding the system. Since the 2630 is to be serviced to the printed circuit board level, the following description does not go into very much detail.

The 2630 contains five main assemblies:

- A Mother (MBD) Board
- A Fixed Point Processor (FXP) Board
- One or two Digital Front End (DFE) Boards
- An optional Digital Back End (DBE) Board
- An optional Parallel Interface

The block diagram in Figure 4-1 shows these assemblies and their interrelationships.

The 2630 is roughly divided into five major parts: input subsystem, central processor, array processor, optional output subsystem, and optional parallel interface. These five parts correspond to the five main assemblies above.

DFE Board

The DFE Board interfaces the signals from up to two analog input channels to the central processor. The 2630 can support two DFE Boards. Each board processes the analog signals from two input channels and converts them to digital. Figure 4-2 shows the DFE Board block diagram.

The input signal ports are differential, with the low side (shield) returned to ground through a 10 ohm resistor and back-to-back diodes. Input switches on the input of the DFE Board select, under program control, input from the input channels or from the optional output channel (DBE). By being able to connect an input channel directly to the DBE, the operator does not have to attach extra coax cables to route this signal. This feature is also used to calibrate the 2630 using the output channel.

Following the input selectors, the input signal passes through programmable ac/dc coupling circuits. DC coupling allows the signal to pass through to the preamplifiers with any accompanying dc offset level. AC coupling passes the signal through a capacitor to isolate the signal from dc offset.

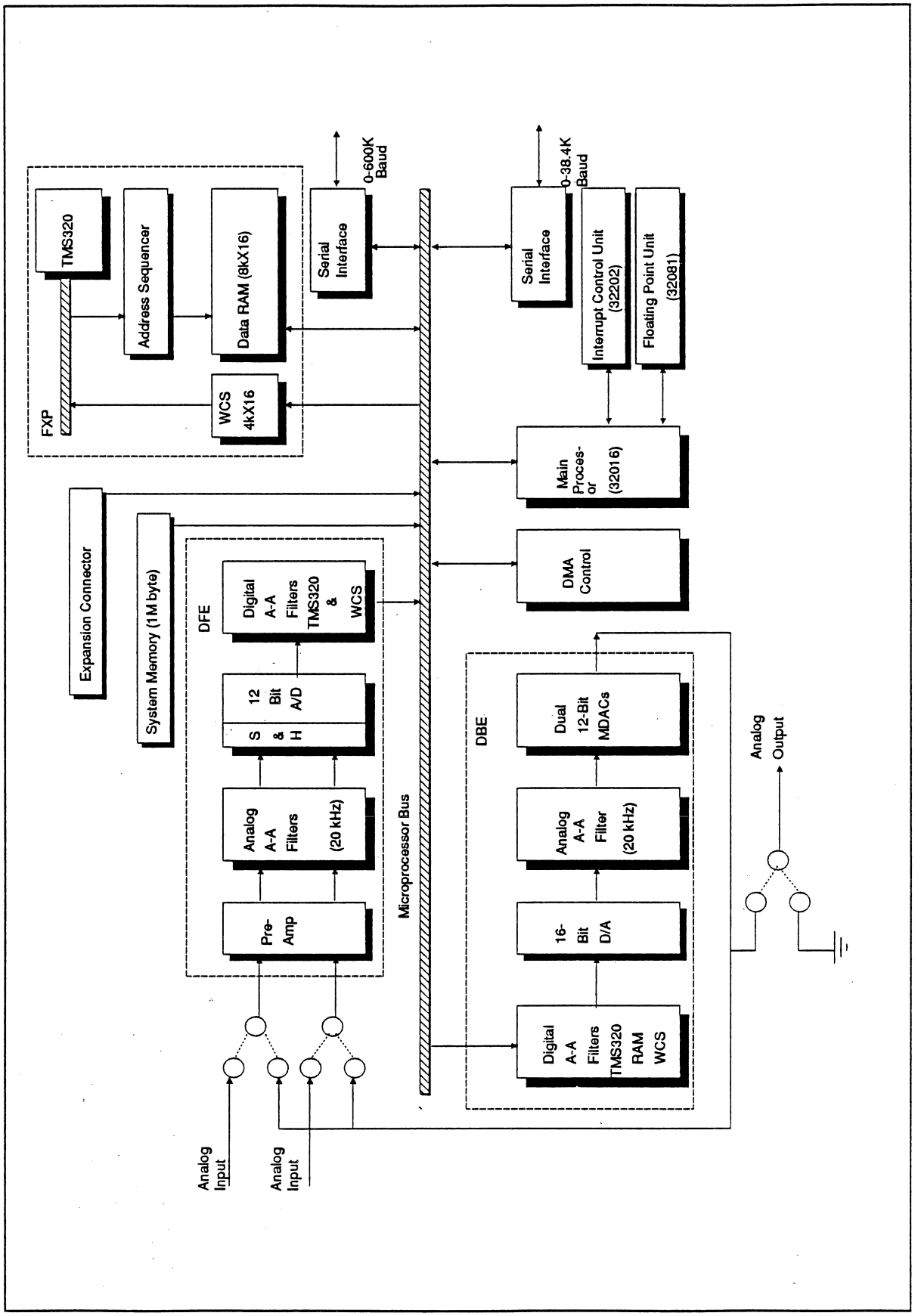


Figure 4-1. 2630 Block Diagram

After the ac/dc coupling circuits, the signal passes through a differential amplifier to the offset circuit. The offset circuit adds a dc level to the incoming signal to effectively zero-out any offset inherent in the analog devices on the DFE Board.

Following the offset circuit, the gain selection circuit provides program control of the input signal level. The input gain is controllable in 16 voltage range selections in factors of 1.414 (3 dB) steps from 55 mV to 10V.

Next, the signal passes on to the analog (elliptic) low pass filter. An overload detector in front of the elliptic filters monitors the analog signal for an overvoltage condition. In addition, an overload detector monitors the output of the analog-to-digital converter. If the detector senses an overload, it sets a bit that can be read by the 32016 microprocessor on the Mother Board.

Following the elliptic filters, the analog signal passes to a sample-and-hold circuit, then to a 12-bit analog-to-digital (A-D) converter. The sample-and-hold circuit holds the analog value long enough for the A-D converter to make the analog-to-digital conversion, then resumes "tracking" the analog signal until the next sample period.

The digitized signal then passes to a digital filter based on the TMS32010 microprocessor. A single TMS32010 handles the digital filtering for both channels on the DFE Board. The TMS32010 is controlled by code stored in 4K by 16-bit writable control store (WCS). The digital filter WCS is actually on the Mother Board, since the same WCS is used for both DFE Boards.

The digital filter takes digital data from the A-D converter at the system sample rate of 51.2 kHz. The 51.2 kHz sample rate is 2.56 times the maximum 2630 bandwidth of 20 kHz.

The digital filters always maintain a sample rate that is 2.56 times the baseband frequency. In these filters, 78 percent of the frequency values are included in the pass band ripple specification and are free from aliased high frequency components to a level of at least -75 dB below full scale.

A second, optional, TMS32010 on the DFE Board provides the zoom option. Zoom results in two sequences of numbers; the real and imaginary parts of the signal. When using zoom, the 2630 performs a complex-to-complex FFT rather than a real-to-complex FFT.

Following the digital filters, the digitized signal is sent via the DMA channel to the 2630 main memory (on the Mother Board).

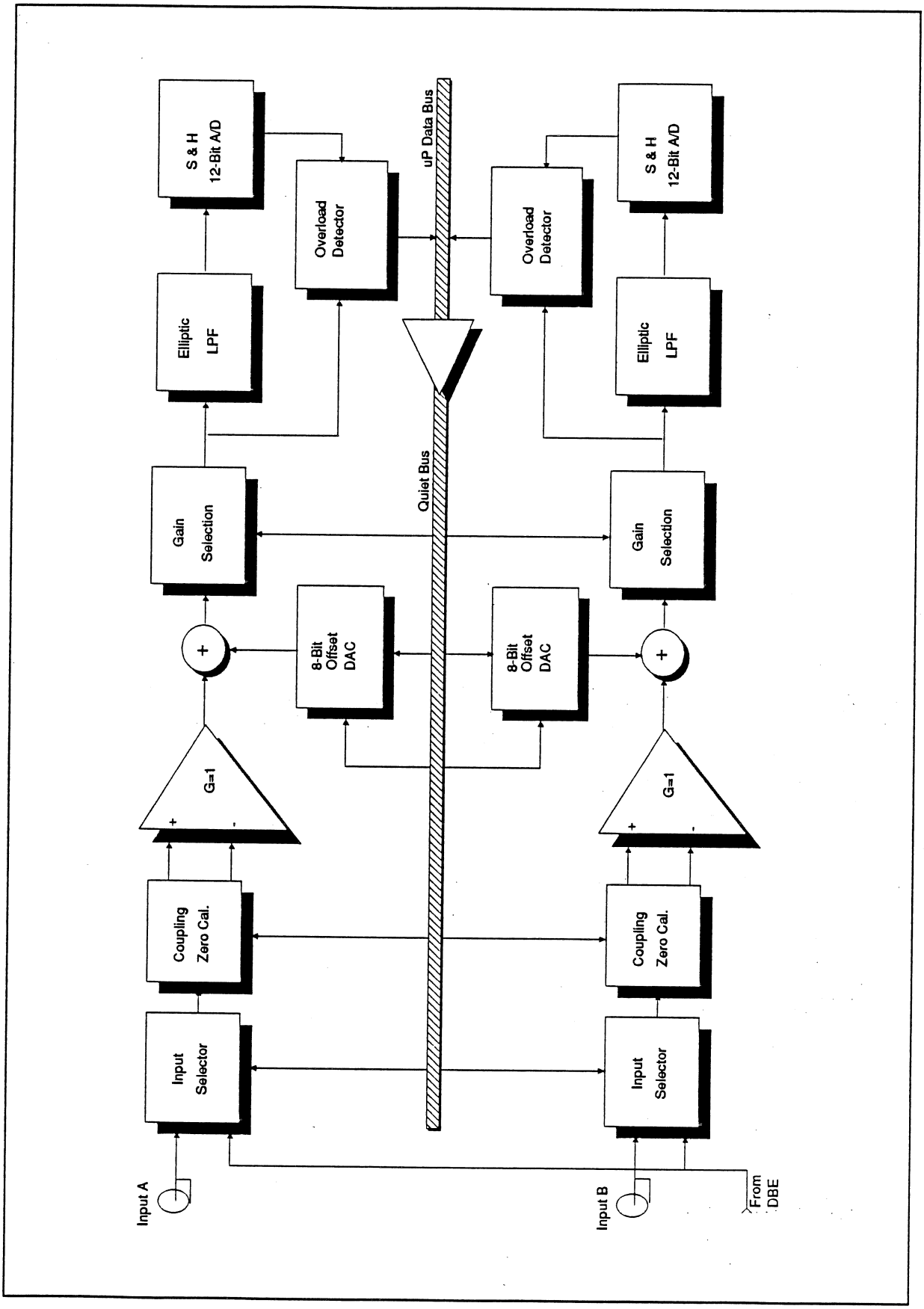


Figure 4-2. DFE Board Block Diagram (Page 1 of 2)

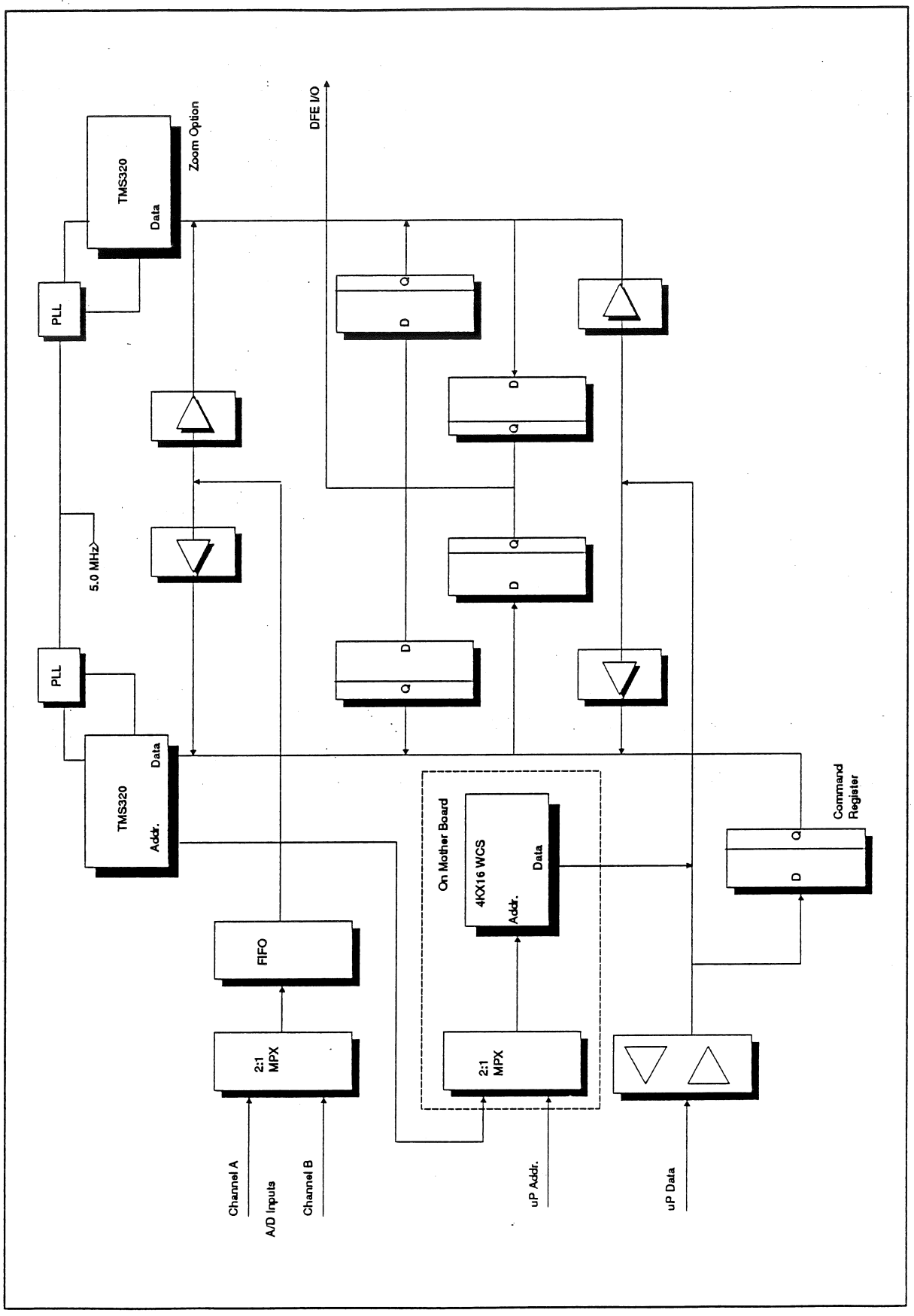


Figure 4-2. DFE Board Block Diagram (Page 2 of 2)

Mother Board

The Mother Board, shown in Figure 4-3, contains the central processor, which is a National 32016 microprocessor with a 32202 interrupt control unit, and 32081 floating point coprocessor, In addition, the Mother Board contains 1M byte main memory, system clocks, DMA controller, interrupt control unit, serial ports, boot PROMs, EEROMs, and various other circuits.

Main Processor

The main processor is a National Semiconductor 32016 microprocessor. This microprocessor (known as the CPU) has 32-bit internal data paths, a 16-bit data bus, and a 24-bit address bus. The 32016 is supported by a 32081 32-bit floating point processor (known as the FPU).

Main Memory

The main memory contains 32 256K-bit by 1-bit DRAM chips. The DRAM chips are organized into four banks of 256K bytes per bank. Two banks at a time are enabled to the main 16-bit data bus.

DMA Controller

The DMA controller consists of two AMD Am9516 Universal DMA Controllers (UDC). Each UDC contains two DMA channels, providing a total of four DMA channels. Each channel is dedicated as follows:

Dynamic RAM refresh
Digital front end (DFE)
Digital back end (DBE) - arbitrary output
Selectable port (software-selectable)

The selectable port allows transfers between memory and either of the serial ports or the expansion connector. The expansion connector is usually used for communications with the Parallel Interface Option. The selectable port can also perform block memory moves, such as memory-to-memory DMA transfers.

The four channels are completely independent, so that four DMA operations may be active at once. The single memory bus is shared with each DMA channel and the 32016 microprocessor in a round-robin type priority scheme (DMA1, microprocessor, DMA2, microprocessor, etc.). Data transfers are in the flowthrough mode. In this mode, data from main memory or a device is loaded into a UDC register on one cycle, then sent to the destination on the next cycle. Each transfer requires two cycles (1.33 microseconds).

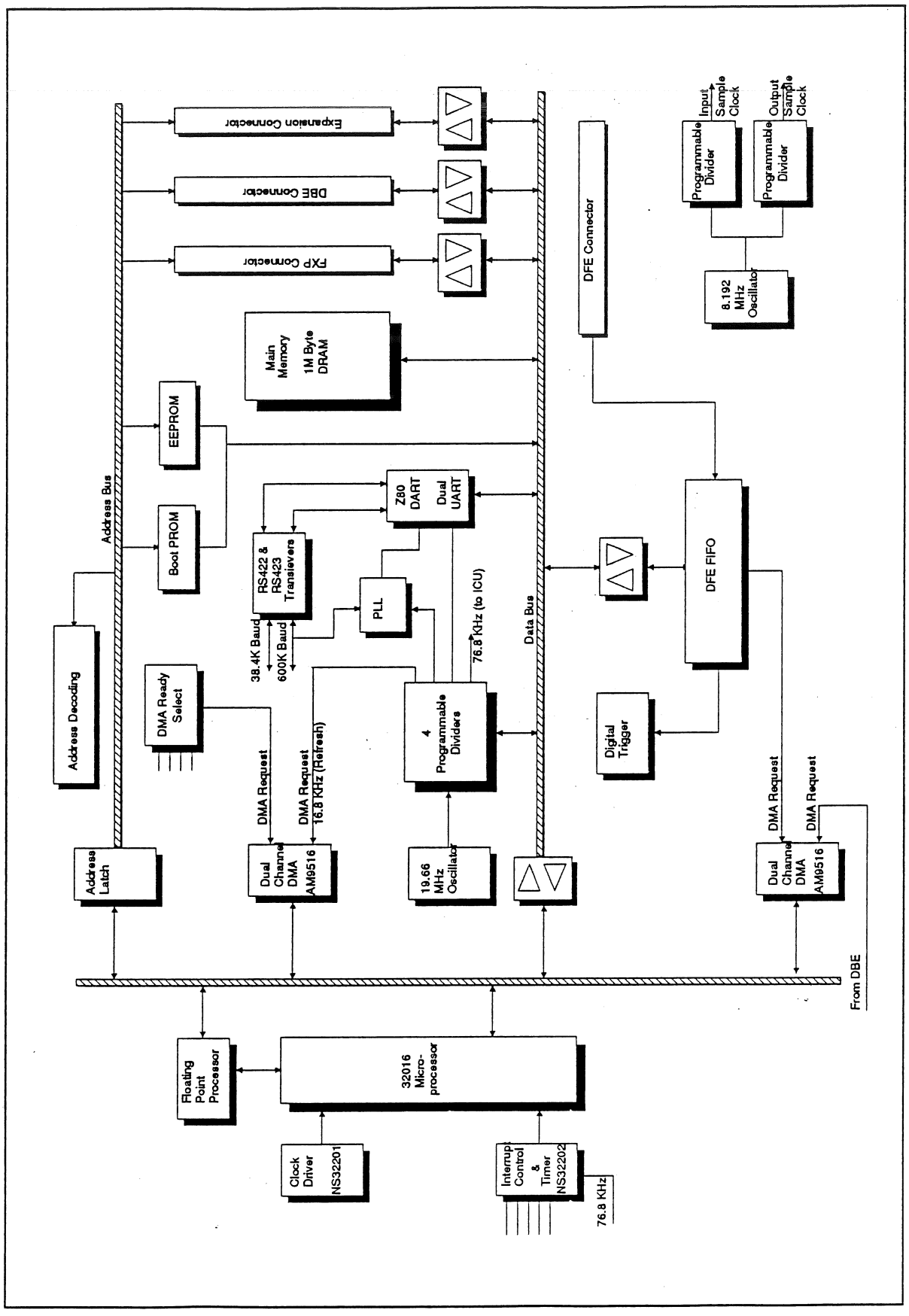


Figure 4-3. Mother Board Block Diagram

Data transfers can take place in an interleaved basis, where every other cycle is "stolen" from the CPU. For example, a DMA transfer from one location can be initiated, then, at the completion of this DMA operation, a second can be initiated which transfers data to or from a different location.

The maximum transfer rate of a DMA channel depends on what the microprocessor and other DMA channels are doing. Since a DMA transfer takes 1.33 microseconds, the maximum DMA transfer rate is 1.5M words per second if only one DMA channel is active and the microprocessor is in a wait state. If all three data channels are operating simultaneously (the fourth channel is memory refresh), the rate per channel is reduced to somewhat less than 500k words per second. The memory refresh channel need only occur every few milliseconds so it is not a significant factor in the estimates.

Interrupt Control Unit

The interrupt control unit minimizes the software and overhead associated with multi-level prioritized interrupts. The interrupt controller manages up to 16 interrupt sources, resolves priorities, and supplies a single byte interrupt vector to the CPU. The interrupt priorities, from highest to lowest, are:

DMA controller 1
DMA controller 2
Serial ports (DART)
Fixed point processor (FXP)
Expansion connector

Serial Ports

The 2630 has two serial ports, referred to as ports 1 and 2. These ports provide the communications path between the 2630 and the host computer. Currently, only one port, port 1, is supported. Both ports support RS-232, RS-422, and RS-423 standards.

Both ports are controlled by a Z8470 Z80 Dual Asynchronous Receiver Transmitter (DUART). These two channels (only port 1 is normally used) interface the 2630 to the host computer.

The 2630 can drive port 1 at up to 614.4k baud and port 2 at up to 72k baud. The DART is driven by a clock frequency of 1.2288 MHz (from the 12 MHz oscillator that provides the CPU and RAM clocks). The DART has internal divide factors of 1, 16, 32, and 64. These factors do not allow all of the normal baud rates. A baud rate register allows programmable factors that provide further dividing of the clock frequency. A six-bit number in the register provides the numerator of the ratio. The denominator is always 64, giving ratios of 1/64 to 62/64 (63/64 is not allowed).

Port 1 uses special synchronization logic that allows use of the full clock frequency or division by programmable factors of 1/64 to 62/64, providing all the normal baud rates.

The port 2 baud rate control uses a divide-by-16 circuit to reduce the 1.2288 MHz clock to 76.8 kHz. The 76.8 kHz clock is divided by the factors in the baud rate register to provide rates of 1200 (1/64) to 72k baud (60/64).

Table 4-1 lists the serial port pin layouts.

Table 4-1. Serial Pin Layouts

Pin	Signal
RS-232 and RS-423	
1	Ground
2	Clear to send (input to 2630)
3	Ground
4	Ground
5	Received data (input to 2630)
6	Transmitted data (output from 2630)
7	Request to send (output from 2630)
8	Not used
9	Not used
RS-422	
1	-Clear to send (input to 2630)
2	+Clear to send (input to 2630)
3	Ground
4	-Received data (input to 2630)
5	+Received data (input to 2630)
6	Not used
7	Request to send (output from 2630)
8	-Transmitted data (output from 2630)
9	+Transmitted data (output from 2630)
The board is configured for RS-232 at the factory. The RS-422 configuration requires alternate jumpers on the board.	

Boot PROMS

The boot PROMS contain the boot and monitor program, MON16. The MON16 program is described in Appendix E of the *2630 Fourier Analyzer User's Guide*. The MON16 program is contained in two PROMS on the mother board.

When the 2630 is powered on, the program in the boot PROMs initialize the 2630 and prepare it to receive downloaded instructions from the host computer.

FXP Board

The FXP (Fixed Point Processor) Board, shown in Figure 4-4, contains an array processor that performs the FFT, windowing, and autospectrum functions. The board performs the complex discrete Fourier transform algorithm functions on data passed to it from the central processor. The computations are performed in a TMS320 microprocessor.

The TMS320 performs the computations in 16-bit fixed point arithmetic, employing a block floating scaling strategy. The resulting data is in complex fixed point format with a block scale factor that indicates the final scaling of the FFT results.

The TMS320 is controlled by microprogram contained in a 4k by 16-bit writable control store (WCS). The WCS microprogram is loaded when the 2630 is initialized (with TOMON).

The 8k by 16-bit data RAM holds 4096 complex points. Half of the 8k data RAM (4k) is used to store sine and cosine values needed by the FFT. These values are loaded when the 2630 is initialized (with TOMON). The remaining 4k of the RAM holds FFT data. Thus the largest FFT possible is a 4096 real-to-complex FFT or a 2048 complex-to-complex FFT. Two address counters are used to help the TMS320 access the data RAM quickly.

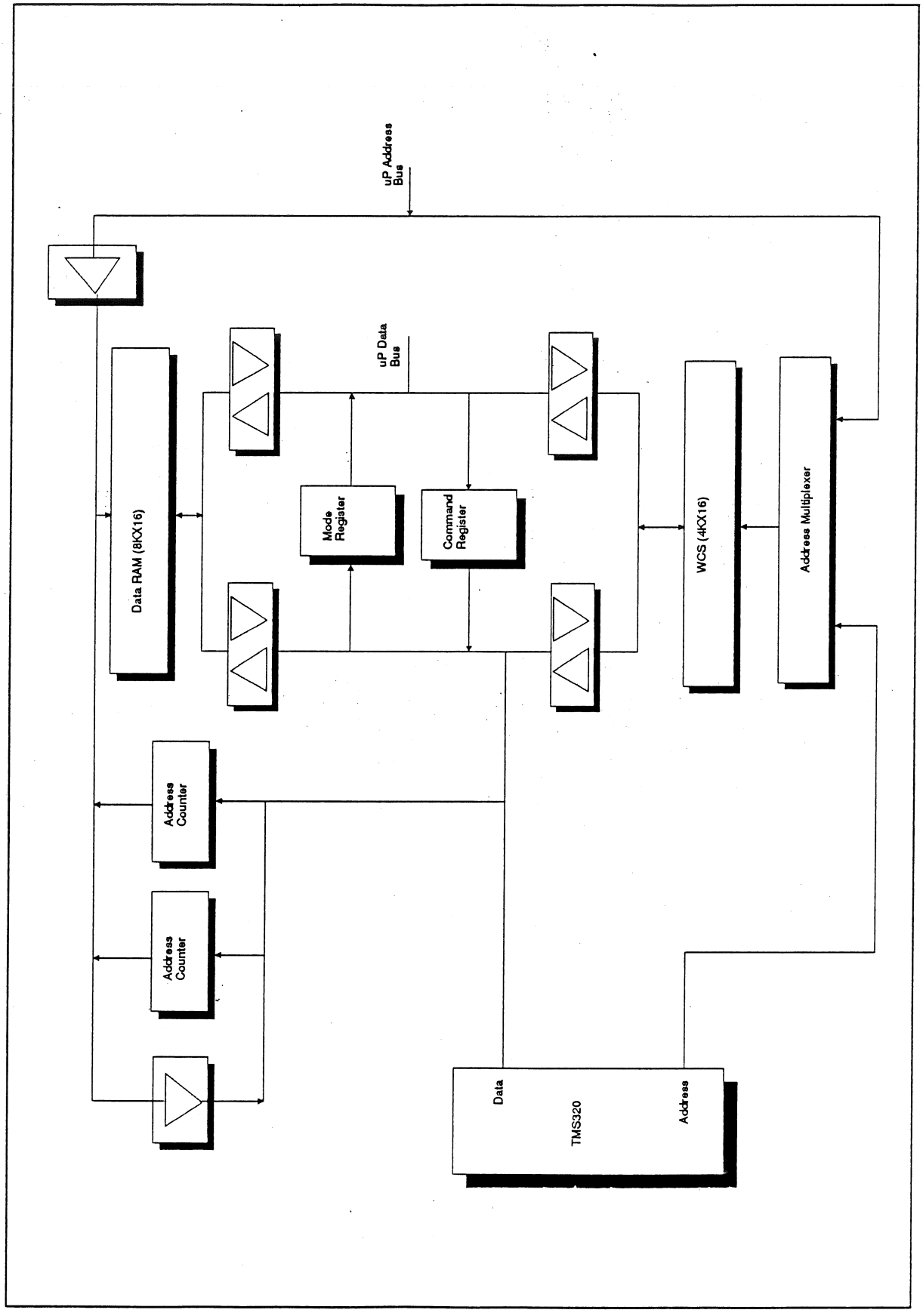


Figure 4-4. FXP Board Block Diagram

DBE Board

The DBE Board, shown in Figure 4-5, is a 2630 option that provides an analog output channel. The output channel generates preprogrammed functions or user-defined functions. A preprogrammed function can be any one of the following waveforms:

sine
square
sawtooth
triangle
random
adjustable-random
impulse

User-defined functions may be sent from the host computer to the DBE Board, where the function is stored in RAM for subsequent output through the output channel. The user-defined function normally comes from a file on the host computer that contains either a computed function or data previously sampled from an input channel.

The output of stored functions is nearly the exact opposite of the A-D conversion performed on the DFE Board. To output a stored function, stored data passes through a digital-to-analog (D-A) converter at a 51.2 kHz fixed sample rate. The input data may be at some lower sample rate, so the TMS320 "fills in" the missing samples.

The 51.2 kHz data functions go to the D-A converter, which creates the analog output signal. The analog signal at this point is still discrete steps, so the signal passes to an elliptic filter that smoothes the output signal.

The signal then passes to a dual MDAC (multiplying digital-to-analog converter) that attenuates the output signal by a factor x:

$$x = AF/4096$$

where AF is a 12-bit word. Both MDACs receive the factor and multiply the output data so the final multiplication performed on the data is x-squared. AF ranges from 0 to 4095, so that the maximum factor is slightly less than unity (4095/4096).

The attenuated signal then passes through a summer that removes any dc offset from the signal before passing the signal to the output connector. The offset value is set when the 2630 auto-calibration procedure is performed.

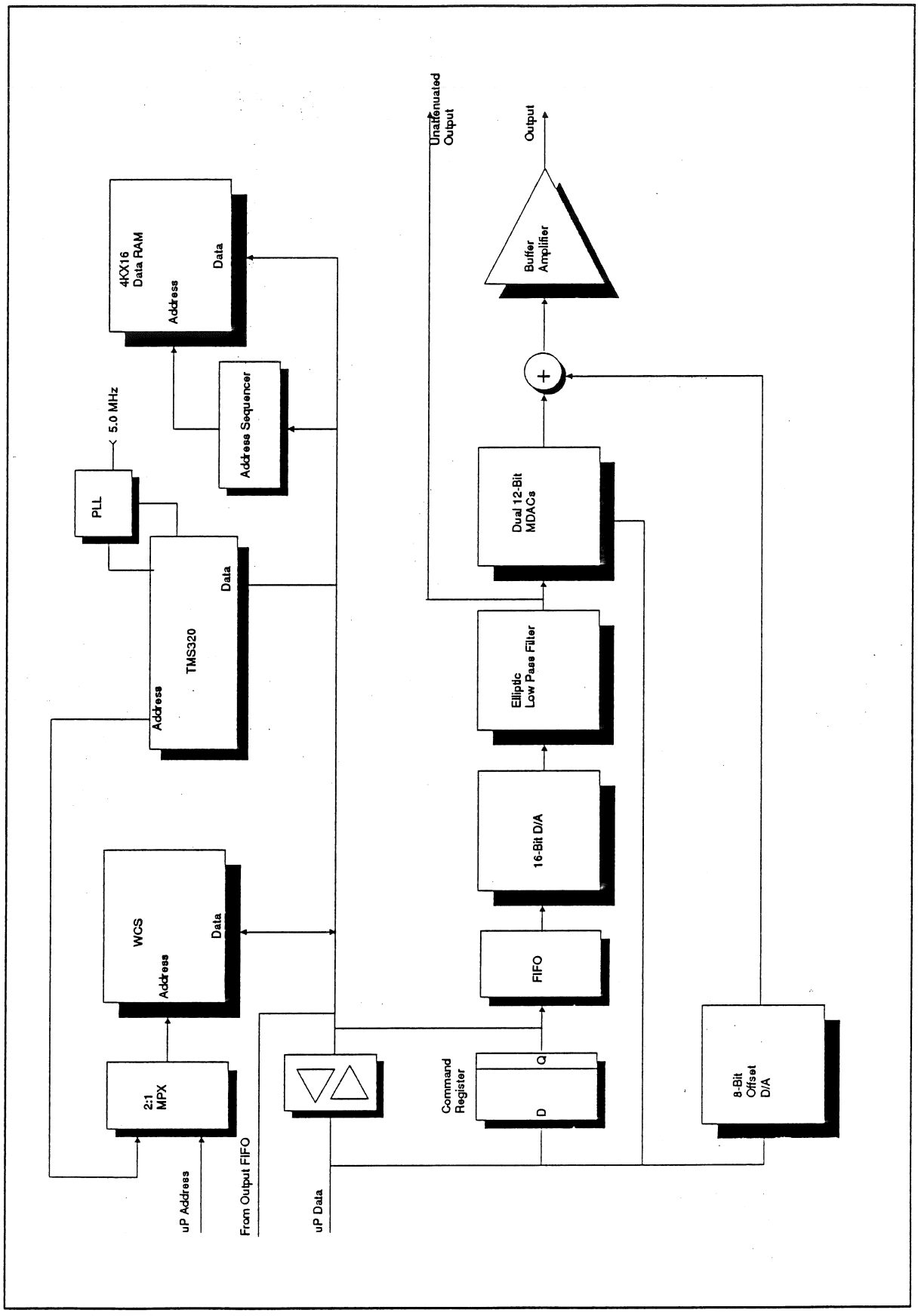


Figure 4-5. DBE Board Block Diagram

Parallel Interface

The Parallel Interface Option, shown in Figure 4-6, consists of a Digital I/O Board, a Parallel Interface Board, and an interface cable. The Digital I/O Board installs in the 2630 and connects with the 2630 Mother Board Expansion connector by way of a ribbon cable. The Parallel Interface Board installs in any empty option slot in the host computer.

The Parallel Interface Option allows bidirectional transfers of digitized data between the 2630 and the host computer hard disk or RAM (using a RAM disk). The maximum transfer rate that can be accommodated in real time is about 25,600 samples per second (sps) when writing to an AT disk drive, or about 51,200 sps when writing directly to a RAM disk or to a very high performance disk drive.

Data transfers are in parallel, 16-bits at a time. On 2630-to-host transfers, the Digital I/O Board receives the 16-bit data words from the mother board data bus, stores the data words in an input first-in-first-out (FIFO) buffer, then transfers the data to the Parallel Interface Board. On host-to-2630 transfers, the Digital I/O Board again uses FIFO buffers to receive data from the host and transfer the data to the 2630 data bus.

The input FIFO buffers permit the Digital I/O Board to send and receive the data at the maximum data rate of the 2630 DMA controller or the Parallel Interface Board.

Data transfers between the Parallel Interface Board and the Digital I/O Board are in 16-bit words. Data transfers between the Parallel Interface Board and the host backplane are in 8-bit bytes. The Parallel Interface Board communication register is divided into two parts; an upper eight-bit register and a lower eight-bit register. The Parallel Interface Board alternates between these two registers when reading from or writing to the host.

Jumpers on the Parallel Interface Board permit selection of the host I/O address and the host interrupt request line.

Address Selection. The I/O address is specified by two jumpers, as follows:

S04	S05	Address Range
Out	Out	270 to 273 (Normal)
In	Out	2B0 to 2B3
Out	In	2D0 to 2D3
In	In	370 to 373

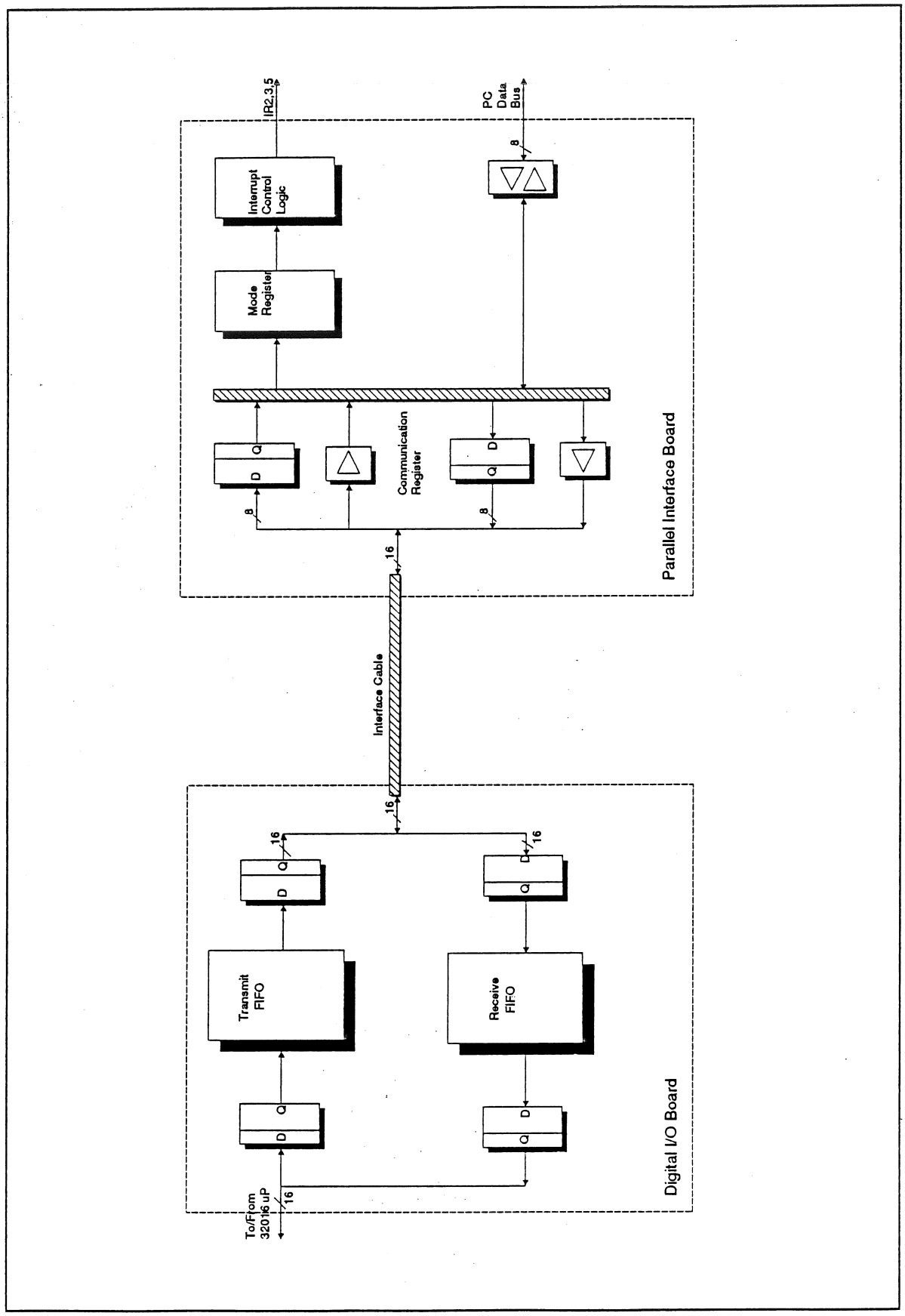


Figure 4-6. Parallel Interface Block Diagram

Interrupt Selection. The interrupt request is specified by a single jumper in one of three positions, as follows:

Position	Interrupt Line
S01	IRQ2(Normal position for PC- and XT-class computers)
S02	IRQ3
S03	IRQ5 (Normal position for AT-class computers)

5

Option Installation

Overview

This section describes how to install the various 2630 options, such as:

- Two additional input channels (Option 1H)
- Output channel (Option 4H)
- Parallel interface (Option 5H)
- Zoom (Options 2H and 3H)
- TurboPac (Option 2S)

Contents **Page**

Two Additional Input Channels Option

The two additional input channels option (Option 1H) consists of the following parts:

- DFE Board
- Coax cables (three)
- Flat ribbon cables (three)
- BNC connectors (two)
- Hinge pins (two)
- Nylon standoffs (three)

1 Turn off the 2630 power and remove the cover (see Section 3).

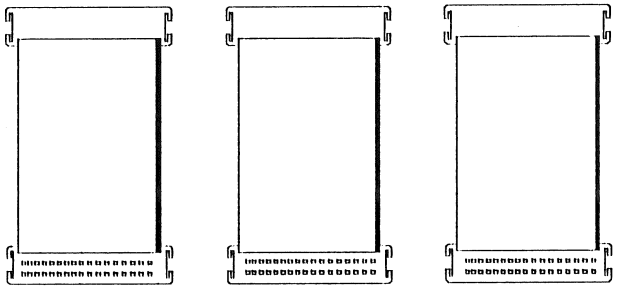
2 Remove the six screws from the front panel that attach the panel to the main chassis. (Three screws attach the panel to the underside of the chassis.)

3 On the front panel, replace the two blank panels with the two coax connectors.

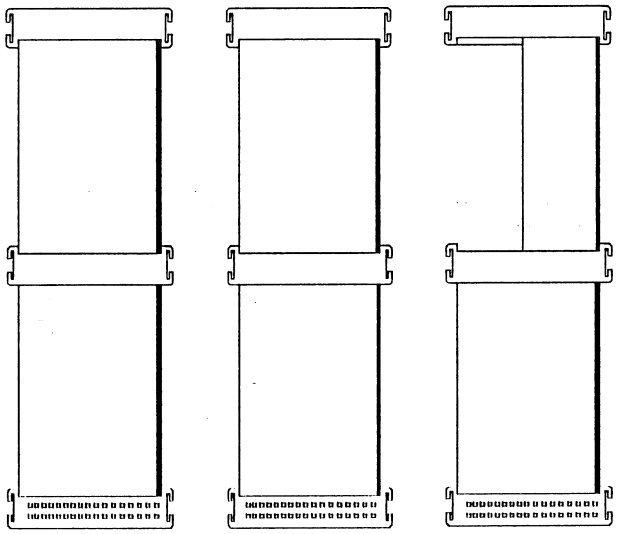
4 Remove the existing DFE Board (five screws).

5 Add the two hinge pins to the existing DFE Board.

6 Remove the three flat ribbon cables from between the existing DFE Board and the Mother Board and replace with the new longer flat ribbon cables. See Figure 5-1.



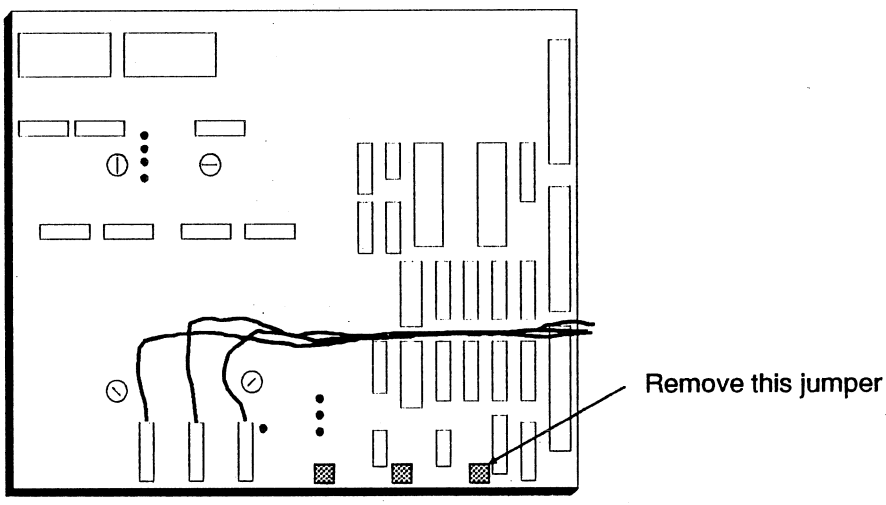
The three flat-ribbon cables used for one DFE Board.



The three flat ribbon cables used for two DFE Boards.

Figure 5-1. DFE Option Flat Ribbon Cables

7 Make sure that J4 is removed from the Channel 3 & 4 DFE Board, as shown below.



8 Reinstall the existing DFE Board with the three nylon standoffs.

9 Install the new DFE Board on top of the existing DFE Board; attach with five screws. See Figure 5-2.

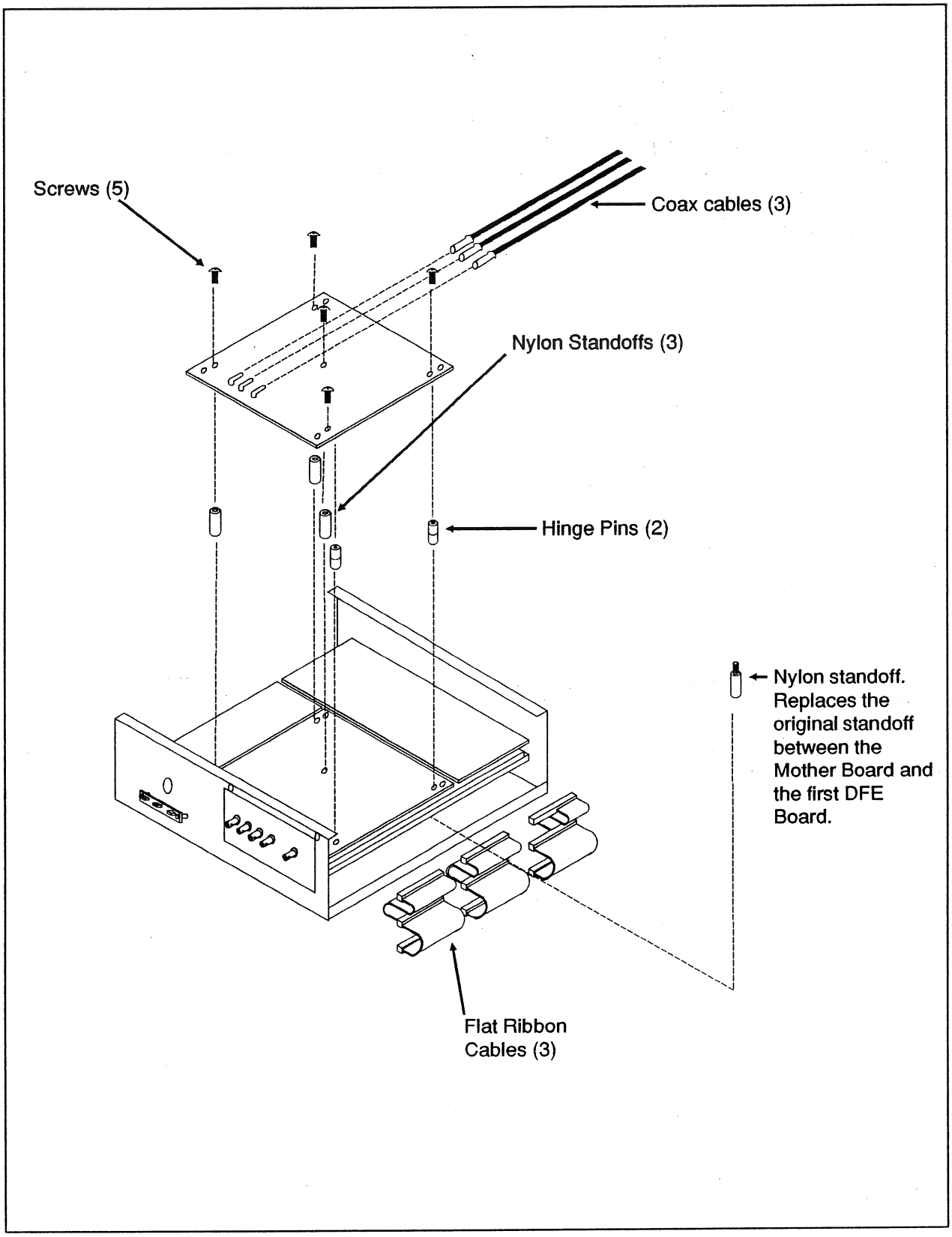


Figure 5-2. DFE Assembly

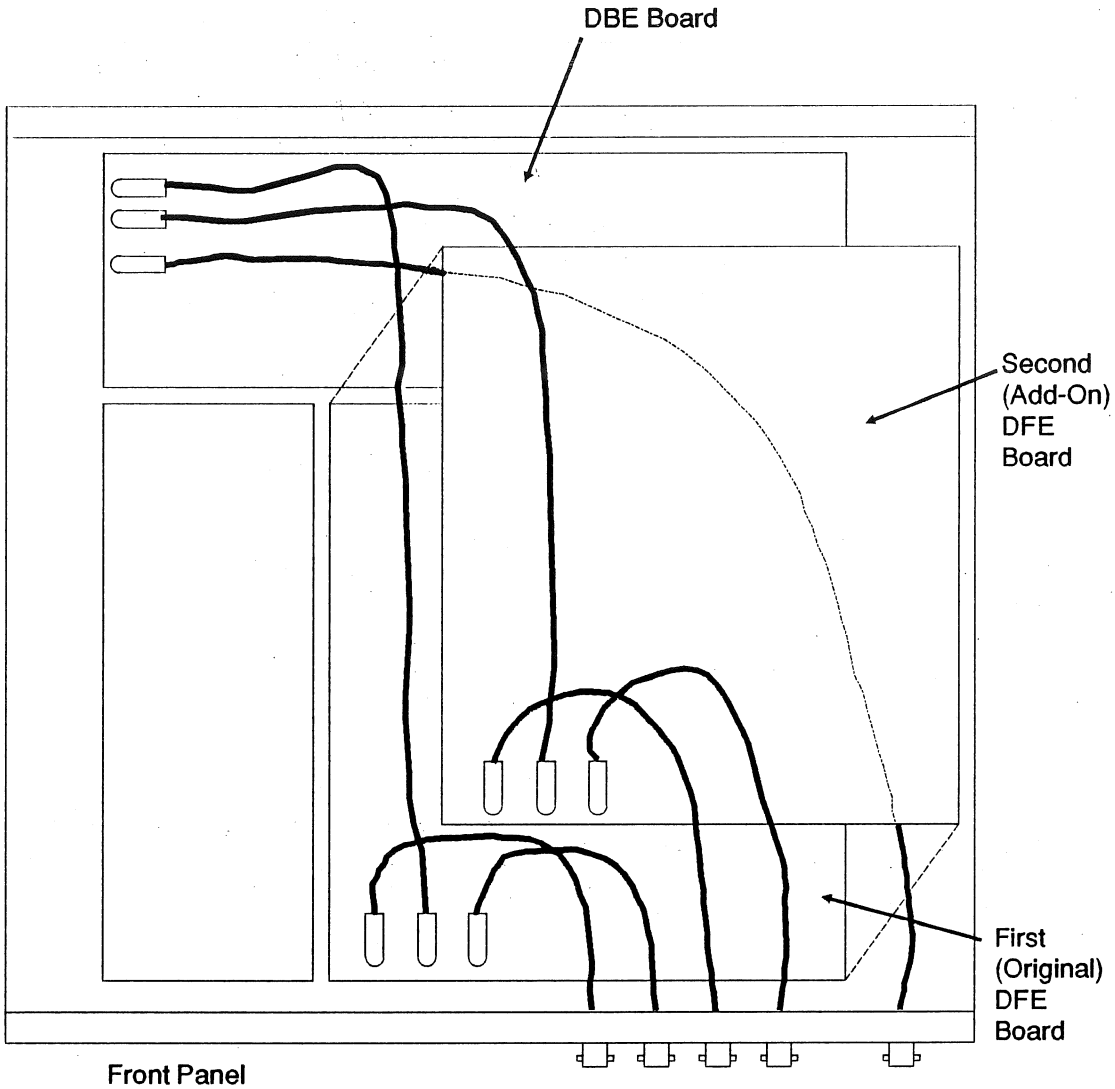
10 Install two coax cables from the new DFE Board to the coax connectors on the front panel. See Figure 5-3.

11 If the 2630 has the Output Channel Option, connect the third coax cable between the new DFE Board and the DBE Board.

12 Reattach the front panel.

13 Power on the 2630 and check the power supply voltages. Adjust if necessary (see Section 2, *Adjusting the Power Supply*).

14 Run the 2630 auto-calibration procedure (see Section 6 in the *2630 Fourier Analyzer User's Guide*).



NOTE:
This diagram shows the cable connections, not the cable routing. The cables must be neatly bundled and routed along the right side of the chassis.

Figure 5-3. DFE Board Coax Cables

Output Channel Option

The Output Channel Option consists of the following parts:

- DBE Board
- Hinge pins (two)
- Flat ribbon cable
- Coax cables (three)
- Nylon standoffs (four)

1 Turn off the 2630 power and remove the cover (see Section 3).

2 Remove two screws from the Mother Board and install the two hinge pins in place of the screws. See Figure 5-4.

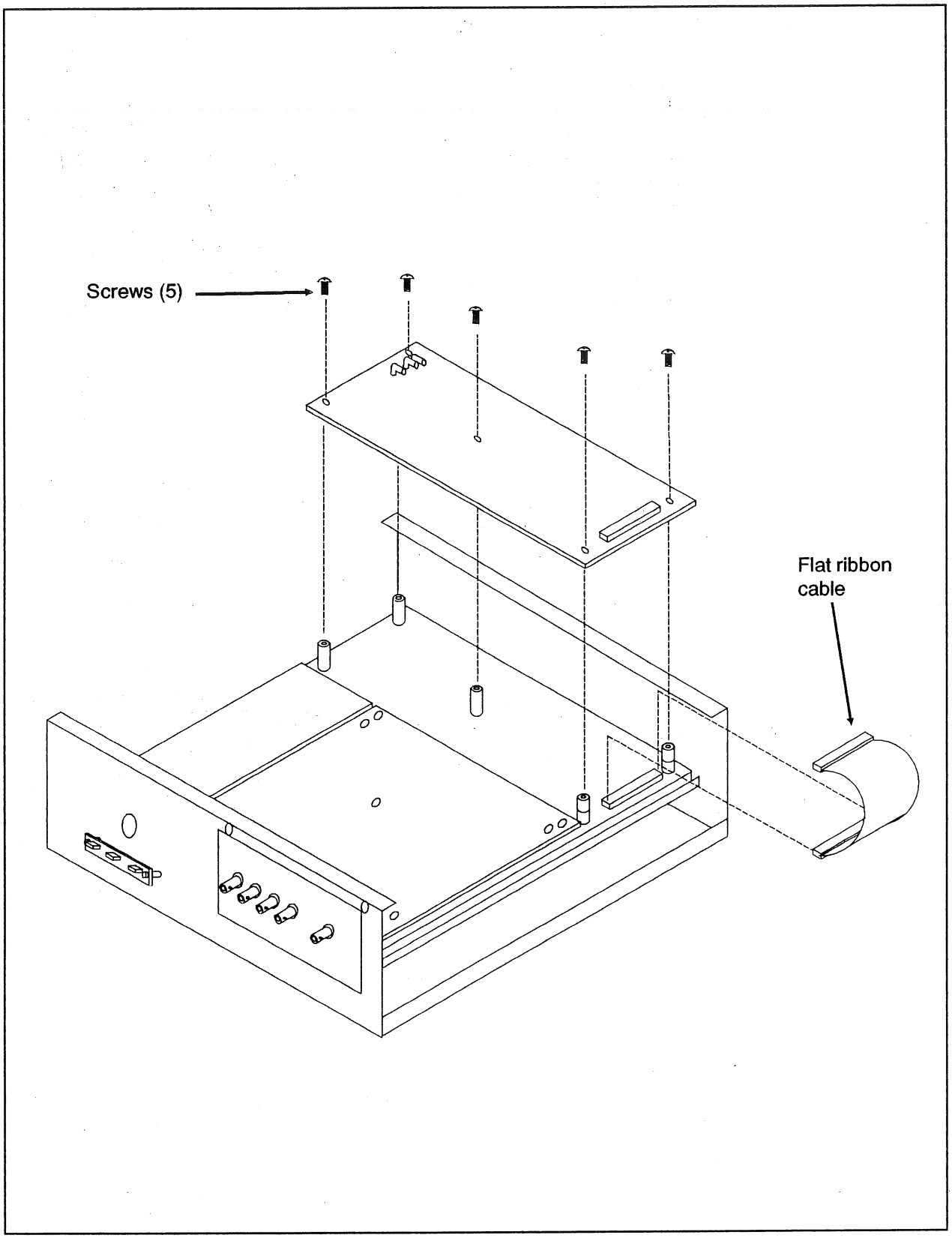


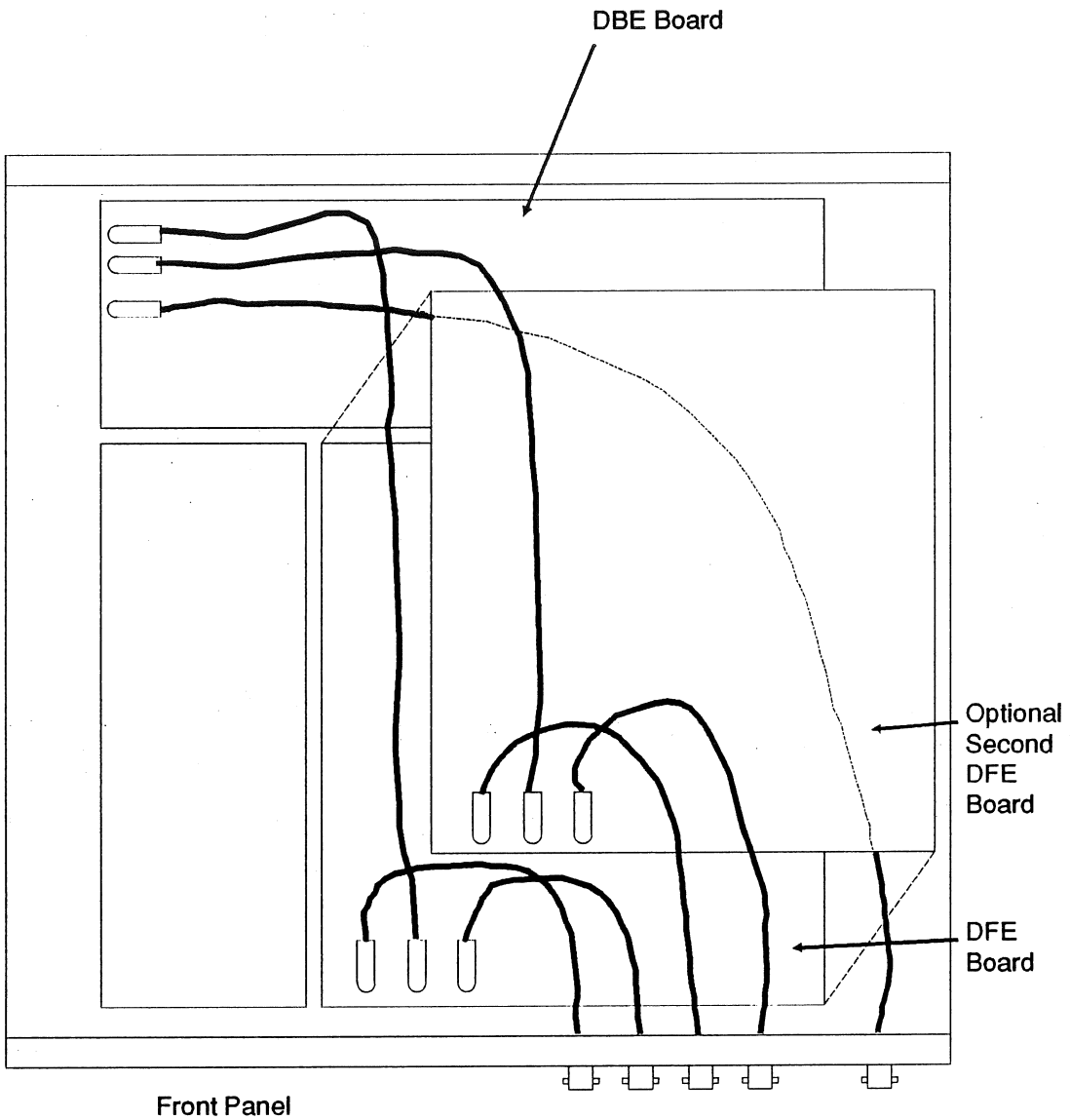
Figure 5-4. DBE Assembly

3 Install the DBE Board on top of the Mother Board.

4 Install the coax cables as shown in Figure 5-5. If the 2630 does not have the two additional input channel option, you will need only two of the three coax cables.

5 Power on the 2630 and check the power supply voltages. Adjust if necessary (see Section 2, *Adjusting the Power Supply*).

6 Run the 2630 auto-calibration procedure (see Section 6 in the *2630 Fourier Analyzer User's Guide*).



NOTE:
This diagram shows the cable connections, not the cable routing. The cables must be neatly bundled and routed along the right side of the chassis.

Figure 5-5. DBE Coax Cables

Parallel Interface Option

The Parallel Interface Option consists of the following parts:

- Digital I/O Board
- Parallel Interface Board
- Flat ribbon cable, short
- Flat ribbon cable, medium
- Flat ribbon cable, long
- Rear panel connector assembly
- Nylon standoffs (four)

1 Turn off the host computer power and remove the cover.

2 Set the Parallel Interface Board interrupt level jumpers as follows (see Figure 5-6):

Jumper	Interrupt Level	
S01	IRQ2	Normal position for PC- and XT-class computers.
S02	IRQ3	Not normally used.
S03	IRQ5	Normal position for AT-class computers.

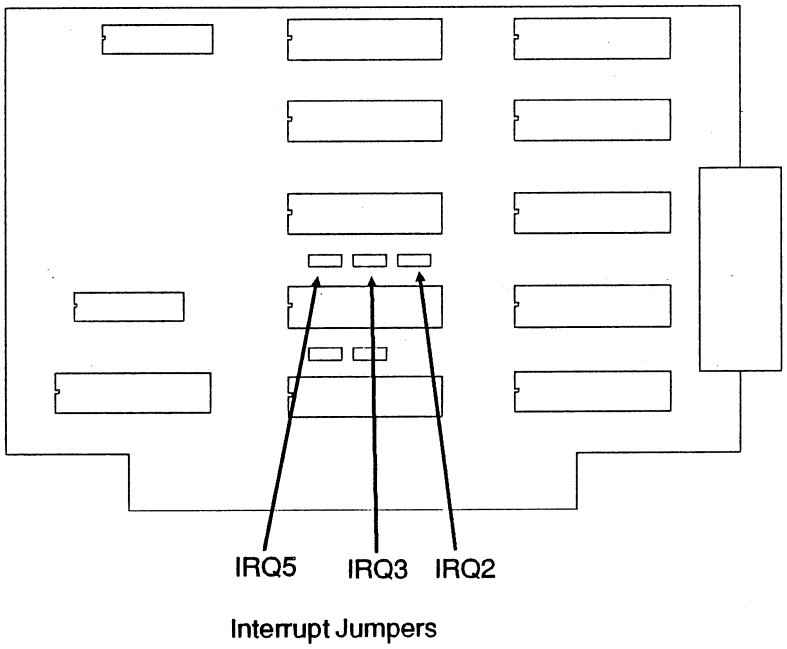


Figure 5-6. Parallel Interface Board Interrupt Jumpers

3 Install the Parallel Interface Board in a spare slot in the host computer.

4 Turn off the 2630 power and remove the cover (see Section 3).

5 Remove the FXP Board (four screws).

6 Install one end of the short-length flat ribbon cable to the Mother Board.

7 Add the four nylon standoffs to the FXP Board.

8 Re-install the FXP Board.

9 Install the Digital I/O Board. See Figure 5-7.

10 Connect the flat ribbon cable from the Mother Board to the Digital I/O Board.

11 Remove the blank panel from the rear panel and install the new rear panel connector assembly in its place.

12 Connect the medium-length flat-ribbon cable between the Digital I/O Board and the rear panel assembly.

13 Connect the long flat ribbon cable between the 2630 rear panel connector and the host computer Parallel Interface Board.

14 Power up both the host computer and the 2630.

15 If the parallel interface diagnostics are not already on the host computer hard disk, install them as described below. If the diagnostics are installed, proceed with Step **16**.

15a Place the Parallel Interface Distribution disk in drive A.

15b Enter the following:

```
> A:
> copydma
```

The installation batch file creates two subdirectories on drive C: \tpac\dio (for the TurboPac demonstration programs) and \diag (for the parallel interface diagnostics).

16 Set the current directory to \diag:

```
> cd \diag
```

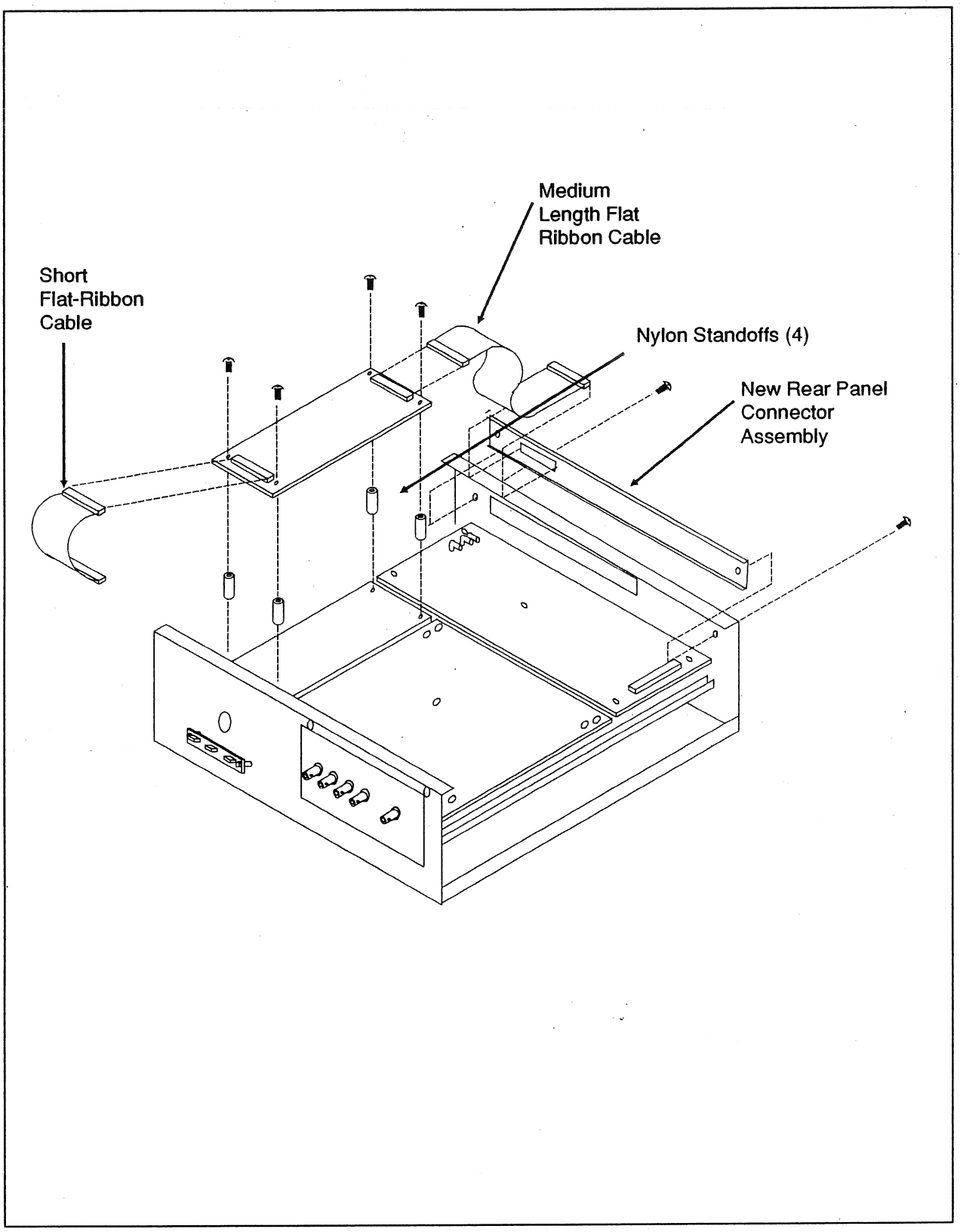


Figure 5-7. Digital I/O Board Assembly

Note: The diagnostic program expects the program TOMON.EXE to be on the DOS path. If TOMON.EXE is not on the path, put it on or edit the diagnostic batch file (DIAGPEE.BAT or DIAGPEE2.BAT) accordingly.

17 Run the Parallel Interface diagnostics:

```
diagpee (for serial port 1)
```

or

```
diagpee2 (for serial port 2)
```

If the diagnostic proceeds normally, here is what you will see:

a. First the digital I/O registers are tested:

```
DIO:  Test Registers for R/W
DIO_MODE:
DIO_CNFG:
DONE:SP TEST 0 STATUS 0
OK - SP ready for programmed xfer from PC
```

b. The diagnostic passes five blocks of data to the 2630 and checks that the blocks are received correctly:

```
PC   :send blocks to 2630 in programmed mode
PASS 1
PASS 2
PASS 3
PASS 4
PASS 5
DONE:SP TEST 1 STATUS 0
PC : done with send test, now get blocks from 2630
```

c. The diagnostic sends data blocks from the 2630:

```
RECEIVED PASS 1
RECEIVED PASS 2
RECEIVED PASS 3
RECEIVED PASS 4
RECEIVED PASS 5
DONE:SP TEST 2 STATUS -1
```

d. The diagnostic initializes the hardware for interrupt driven operation on both ends of the link. Short messages are exchanged using programmed transfer and interrupts:

```
OK:  Com board registers initialized
Sent Handshake message to 2630
Waiting for response
```

e. The diagnostic transfers five blocks of 1024 random words to the 2630. The Active indicator (only) should come on and the blocks will count off rather slowly.

f. The diagnostic transfers five blocks of 1024 random words are transferred to the host PC and checked for validity. Any discrepancies are noted.

g. The diagnostic transfers random blocks back and forth continuously. If an error occurs, it is noted. A count of the blocks transferred and the total block errors encountered is continuously updated.

18 Press the space bar to terminate the diagnostic.

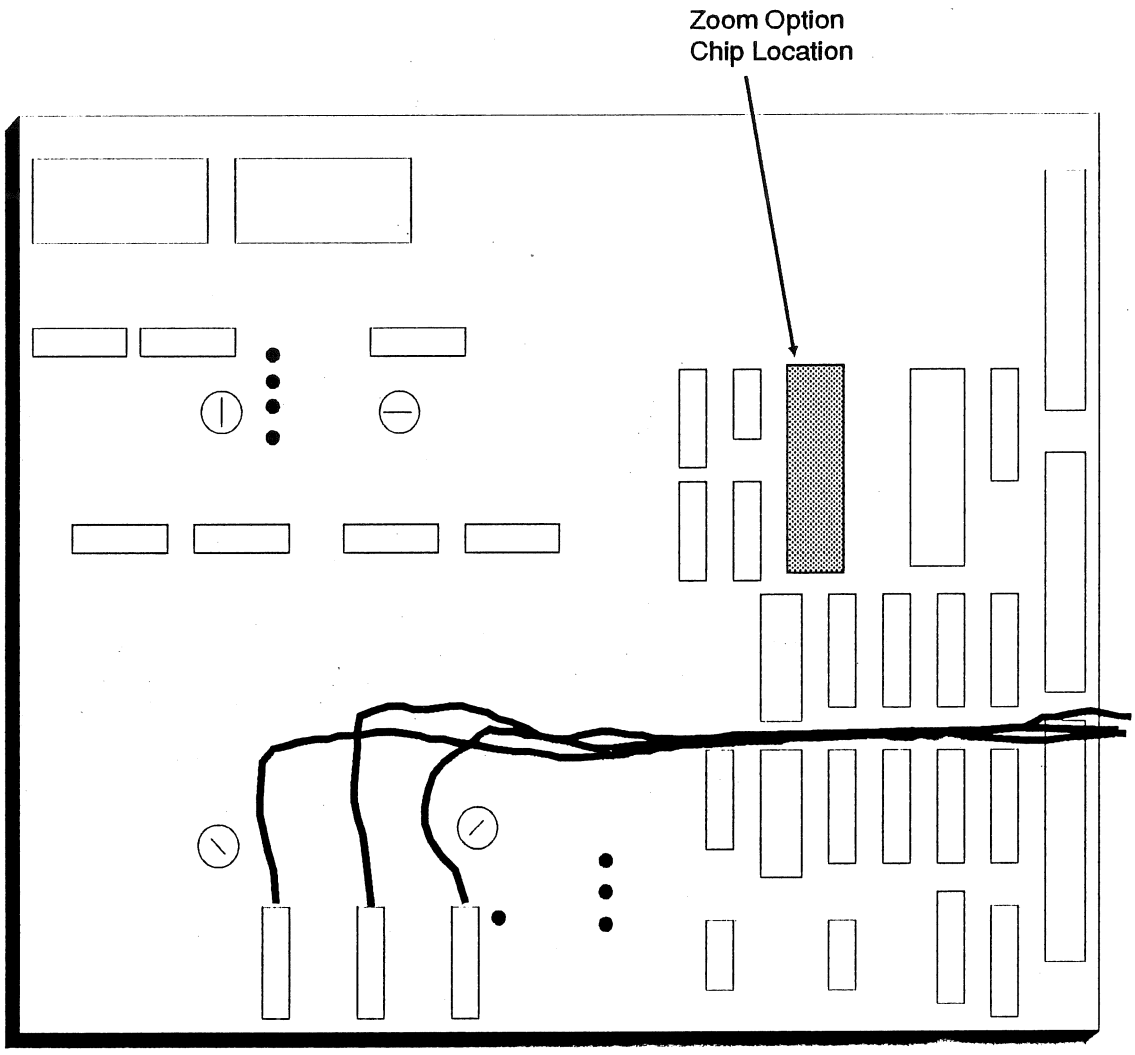
19 Re-install the host computer and 2630 covers.

Zoom Option

There are two Zoom Options: Two-channel zoom and four-channel zoom. The two-channel zoom option adds zoom to one DFE Board. The four-channel zoom option adds zoom to two DFE Boards. The following instructions apply to either option.

The Zoom Option consists of a TMS320 microprocessor chip.

1. Turn off the 2630 power and remove the cover (see Section 3).
2. Install the TMS320 chip into the socket on the DFE Board. See Figure 5-8.
3. Power up the 2630 and the host computer.
4. Reprogram the 2630 EEPROM with the EEPROM program on the diagnostic diskette. The program walks you through the procedure.



NOTE:
This diagram shows the cable connections, not the cable routing. The cables must be neatly bundled and routed along the right side of the chassis

Figure 5-8. Zoom Option Chip Location

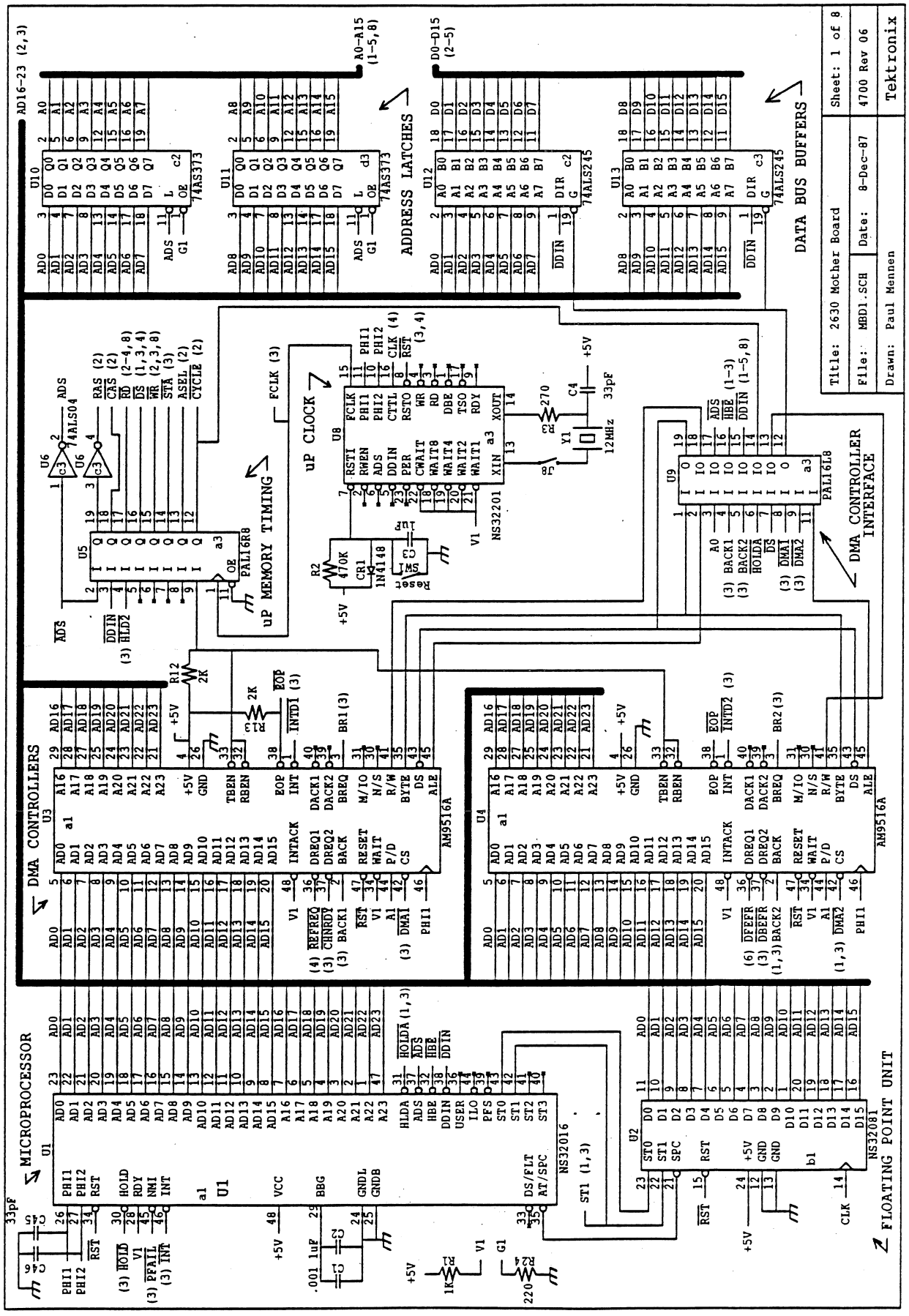
TurboPac Option

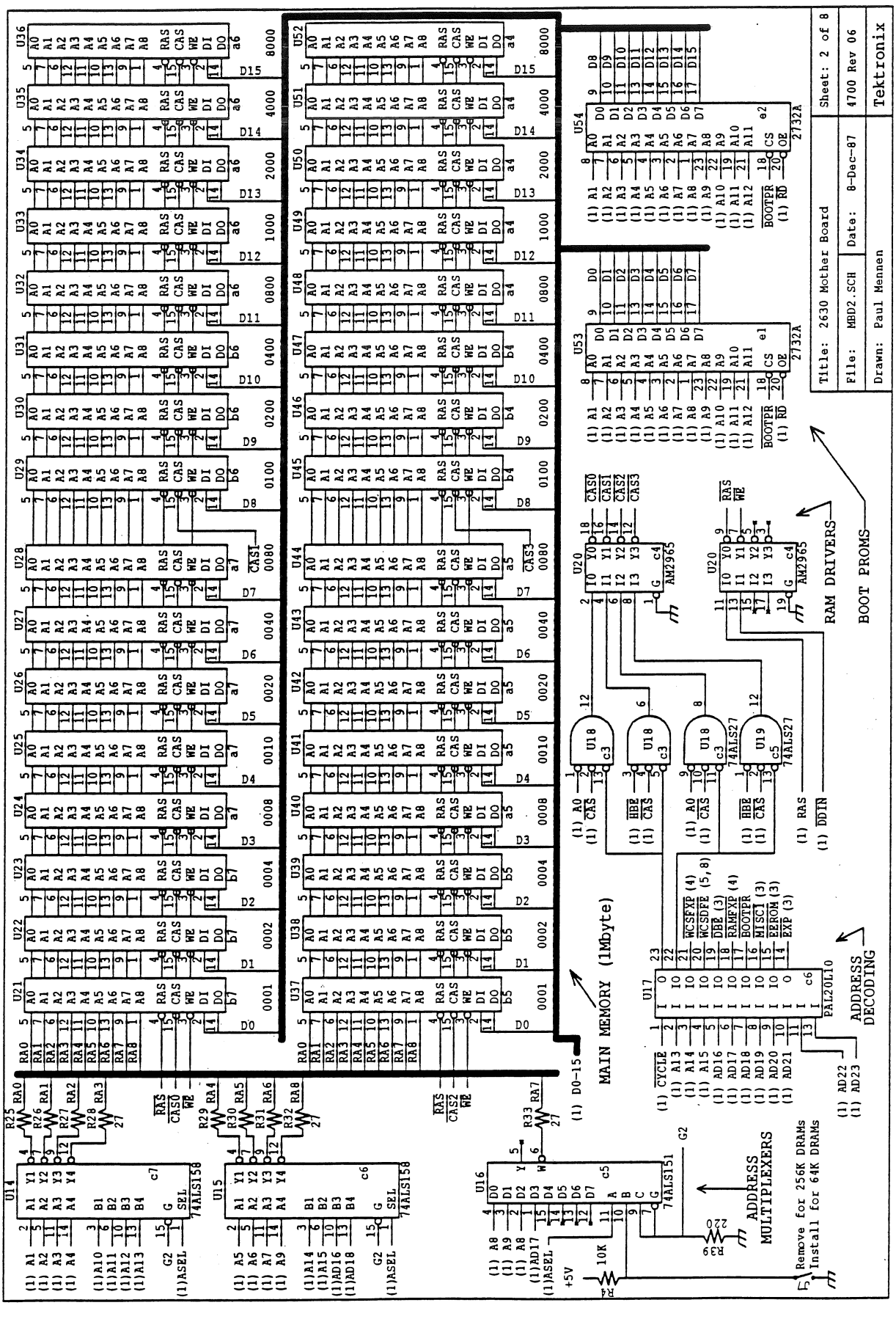
The TurboPac option does not require the installation of any parts within the 2630. Reprogram the 2630 EEPROM with the EEPROM program on the diagnostic diskette. The program walks you through the procedure.

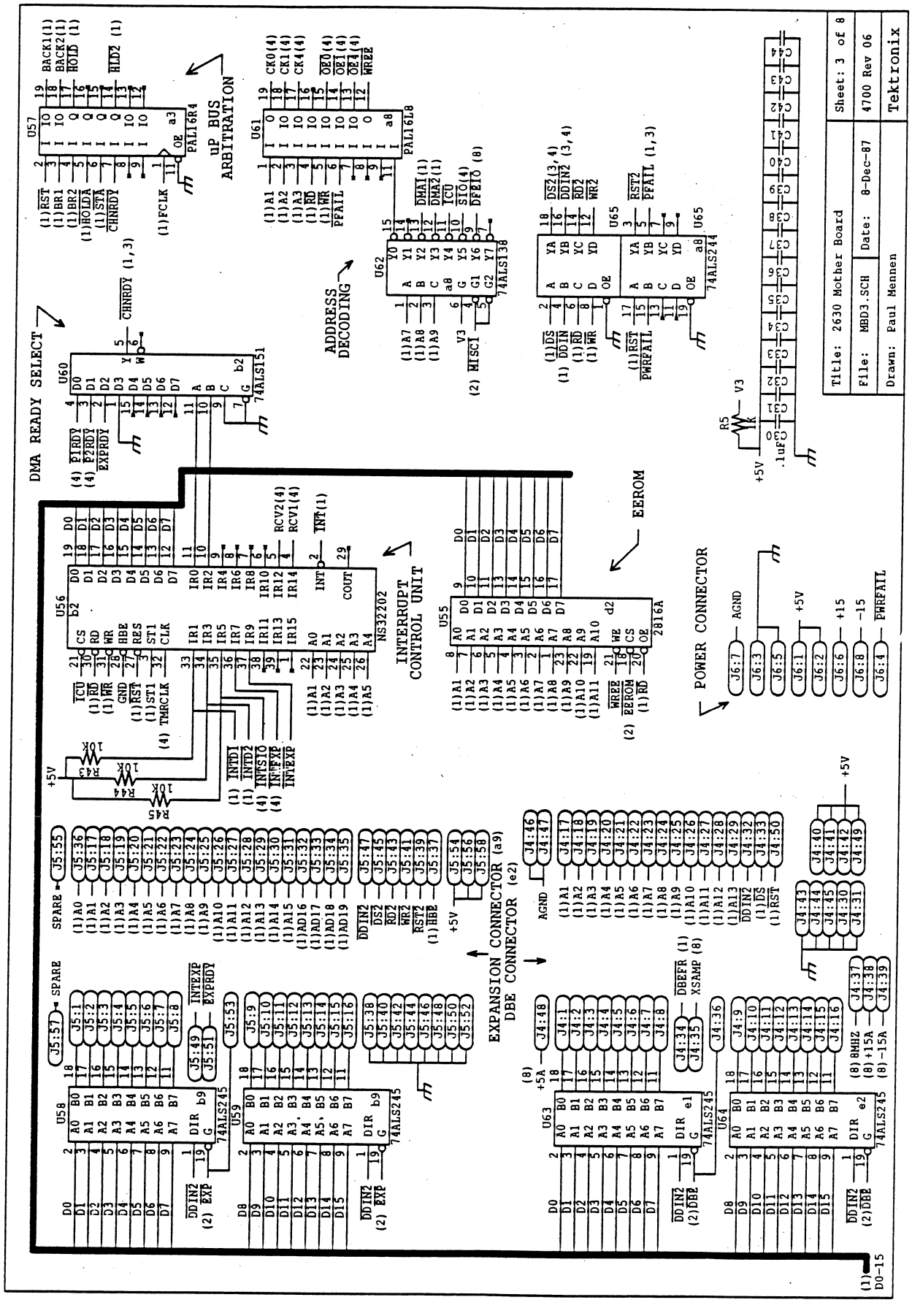
6

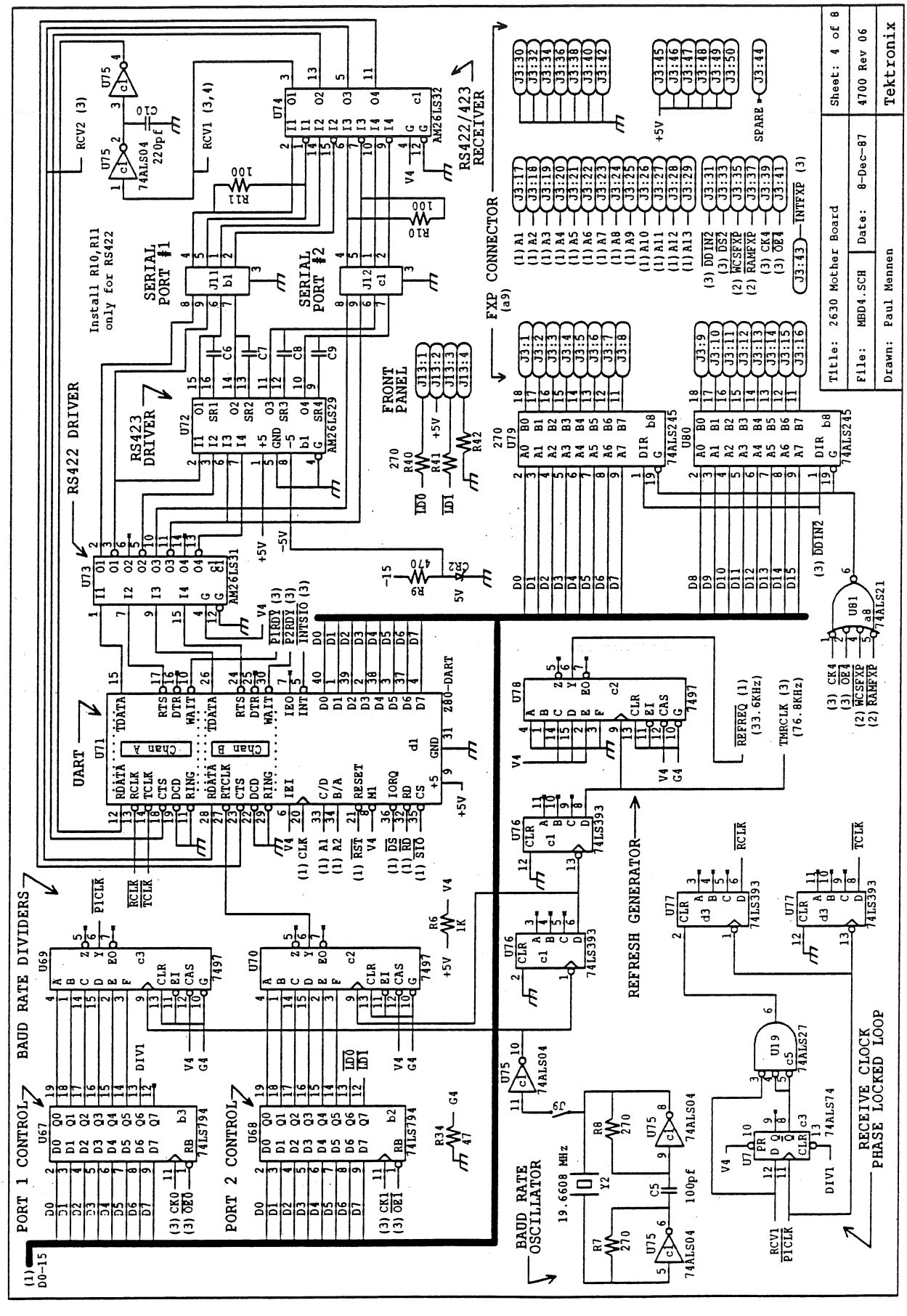
Schematics

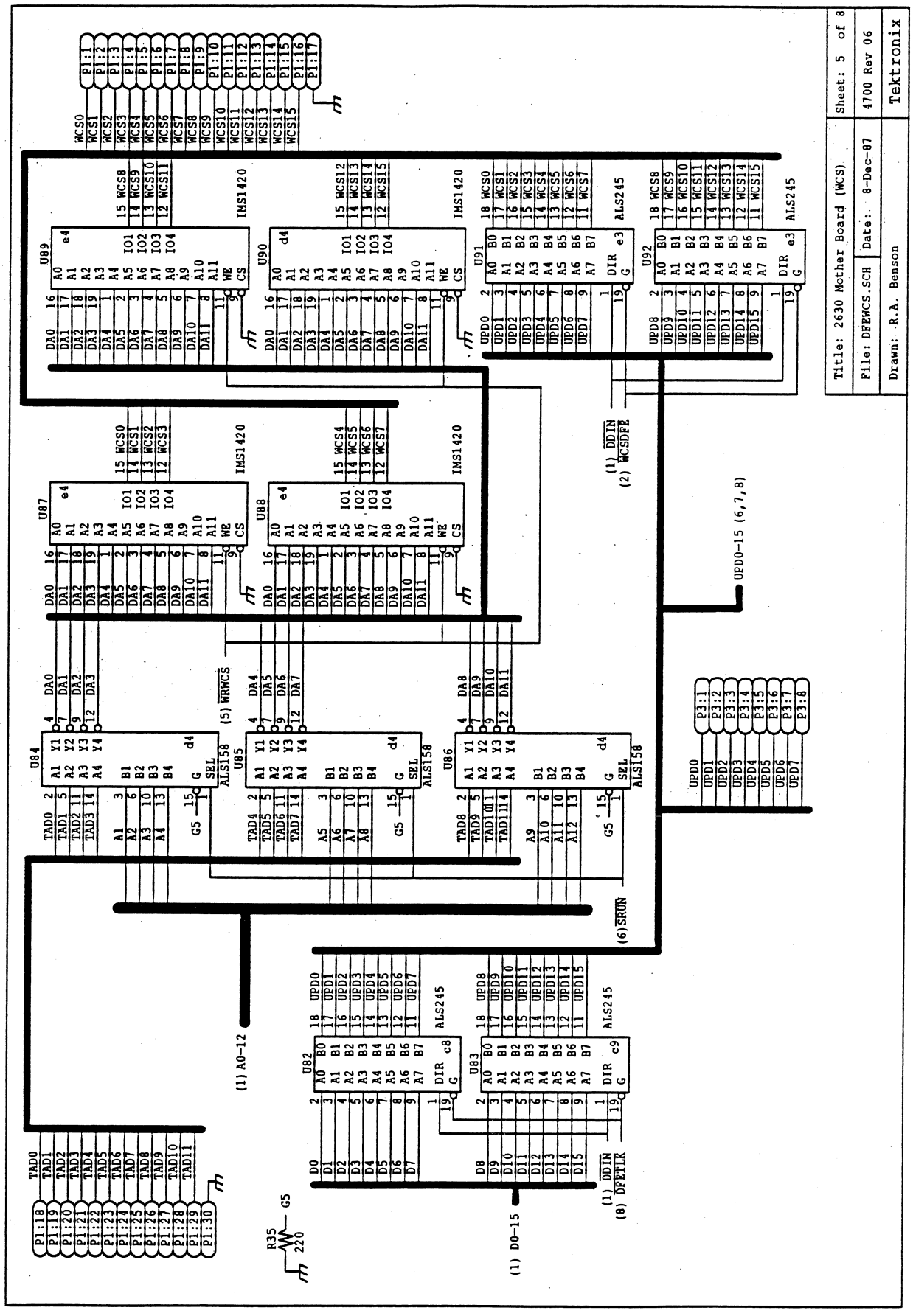
This section contains the 2630 schematics:

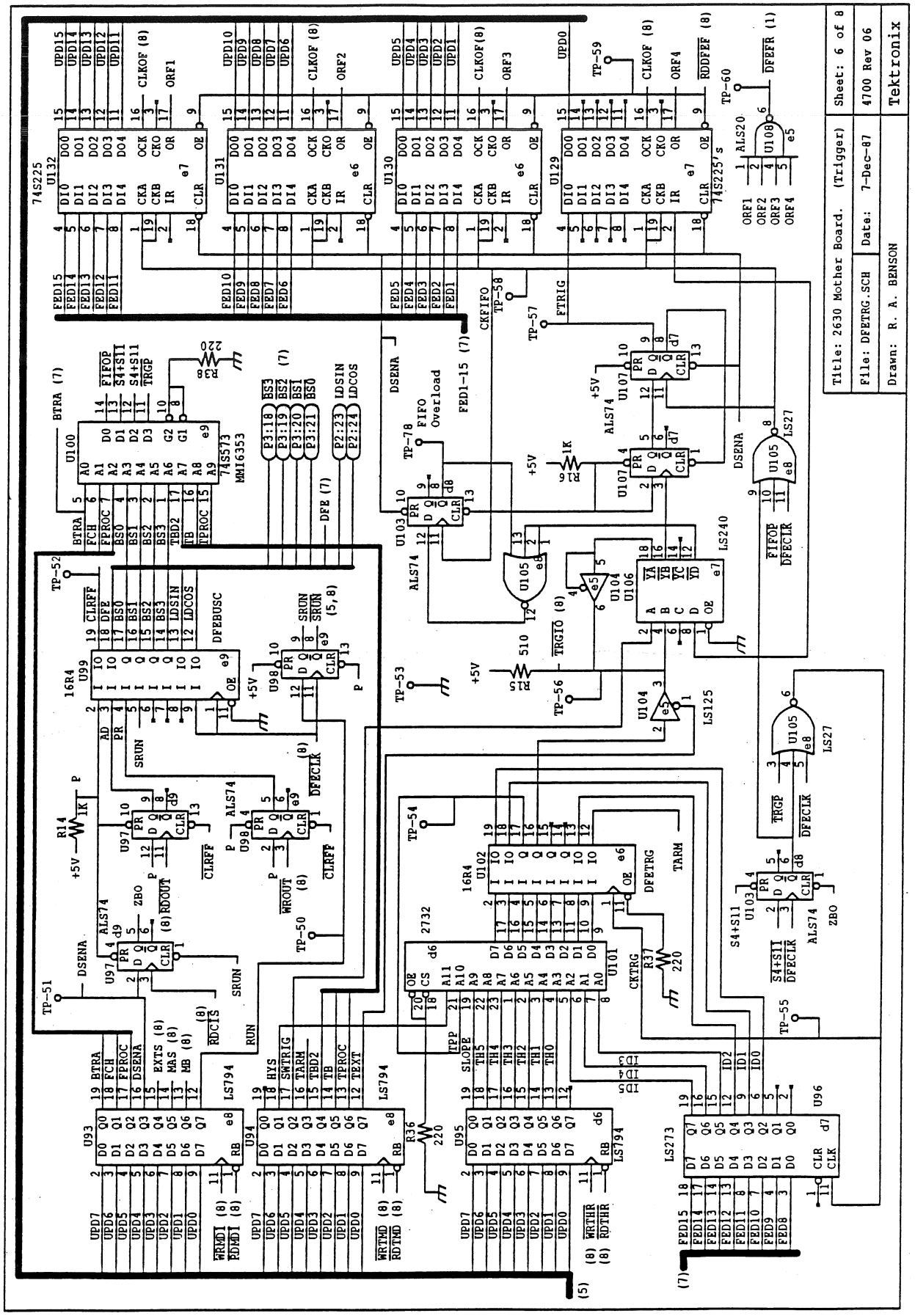

MICROPROCESSOR
FLOATING POINT UNIT
DMA CONTROLLERS
DMA CONTROLLER INTERFACE
uP MEMORY TIMING
uP CLOCK
ADDRESS LATCHES
DATA BUS BUFFERS
Title: 2630 Mother Board
File: MBD1.SCH
Date: 8-Dec-87
Drawn: Paul Mennen
Sheet: 1 of 8
4700 Rev 06
Tektronix

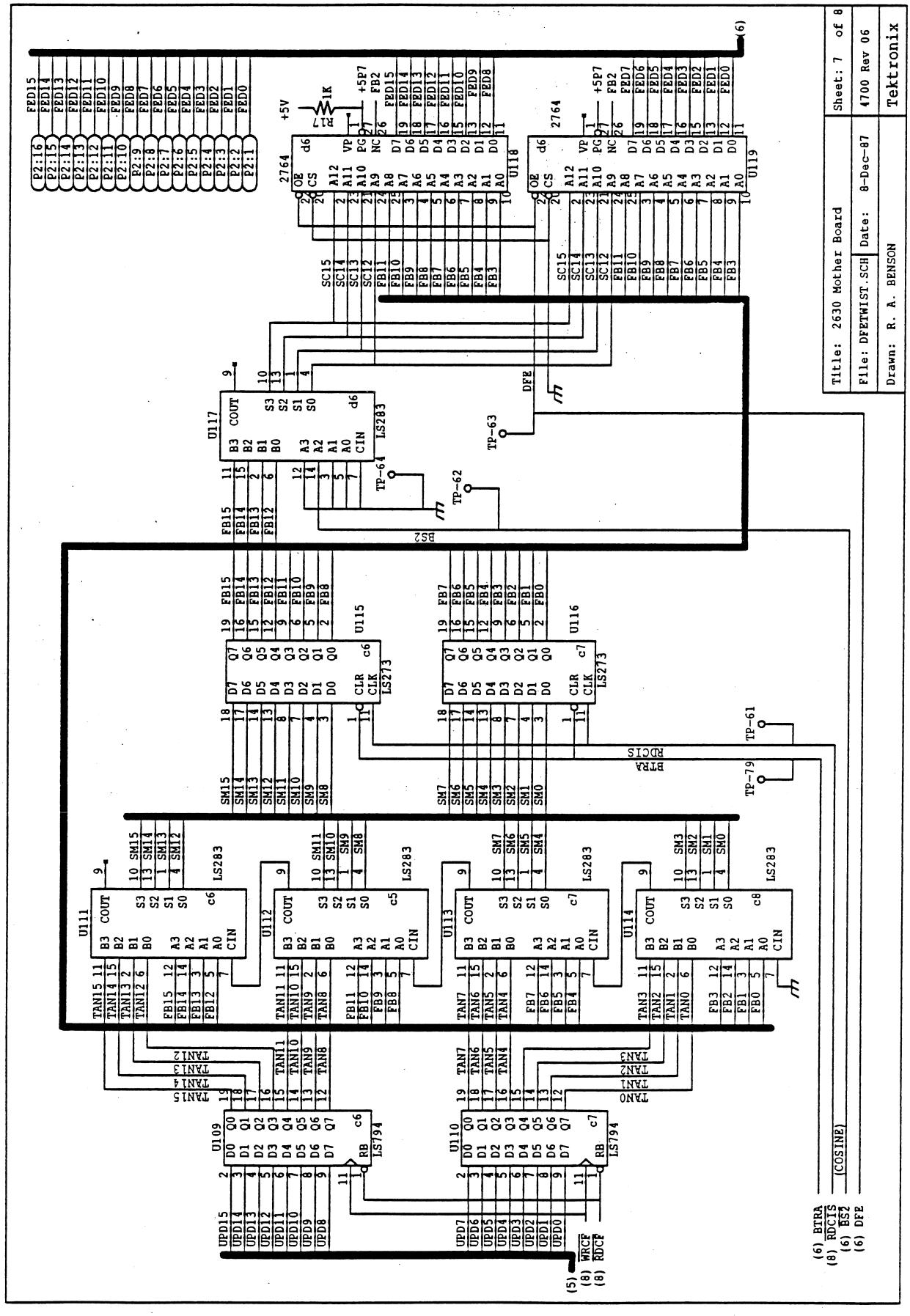

Title: 2630 Mother Board
Sheet: 2 of 8
File: MBD2.SCH
Date: 8-Dec-87
4700 Rev 06
Drawn: Paul Mennen
Tektronix
MAIN MEMORY (1Mbyte)
RAM DRIVERS
BOOT PROMS
ADDRESS DECODING
ADDRESS MULTIPLEXERS
Remove for 256K DRAMs
Install for 64K DRAMs
74ALS158
74ALS151
74ALS27
AM2965
2732A
PAL20L10

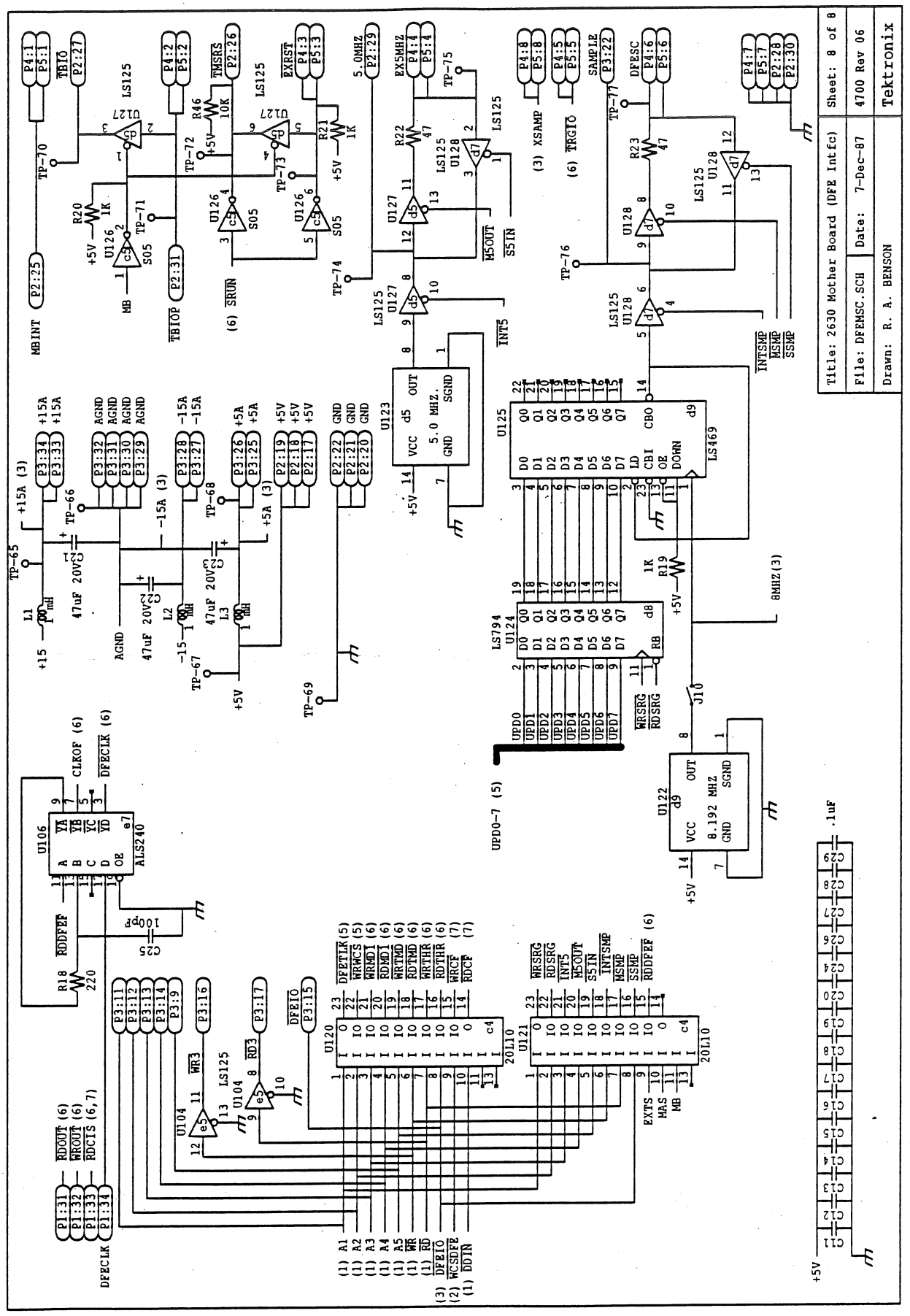

DMA READY SELECT
uP BUS ARBITRATION
ADDRESS DECODING
INTERRUPT CONTROL UNIT
EEROM
POWER CONNECTOR
EXPANSION CONNECTOR (a9)
DBE CONNECTOR (e2)
Title: 2630 Mother Board
Sheet: 3 of 8
File: MBD3.SCH
Date: 8-Dec-87
4700 Rev 06
Drawn: Paul Mennen
Tektronix

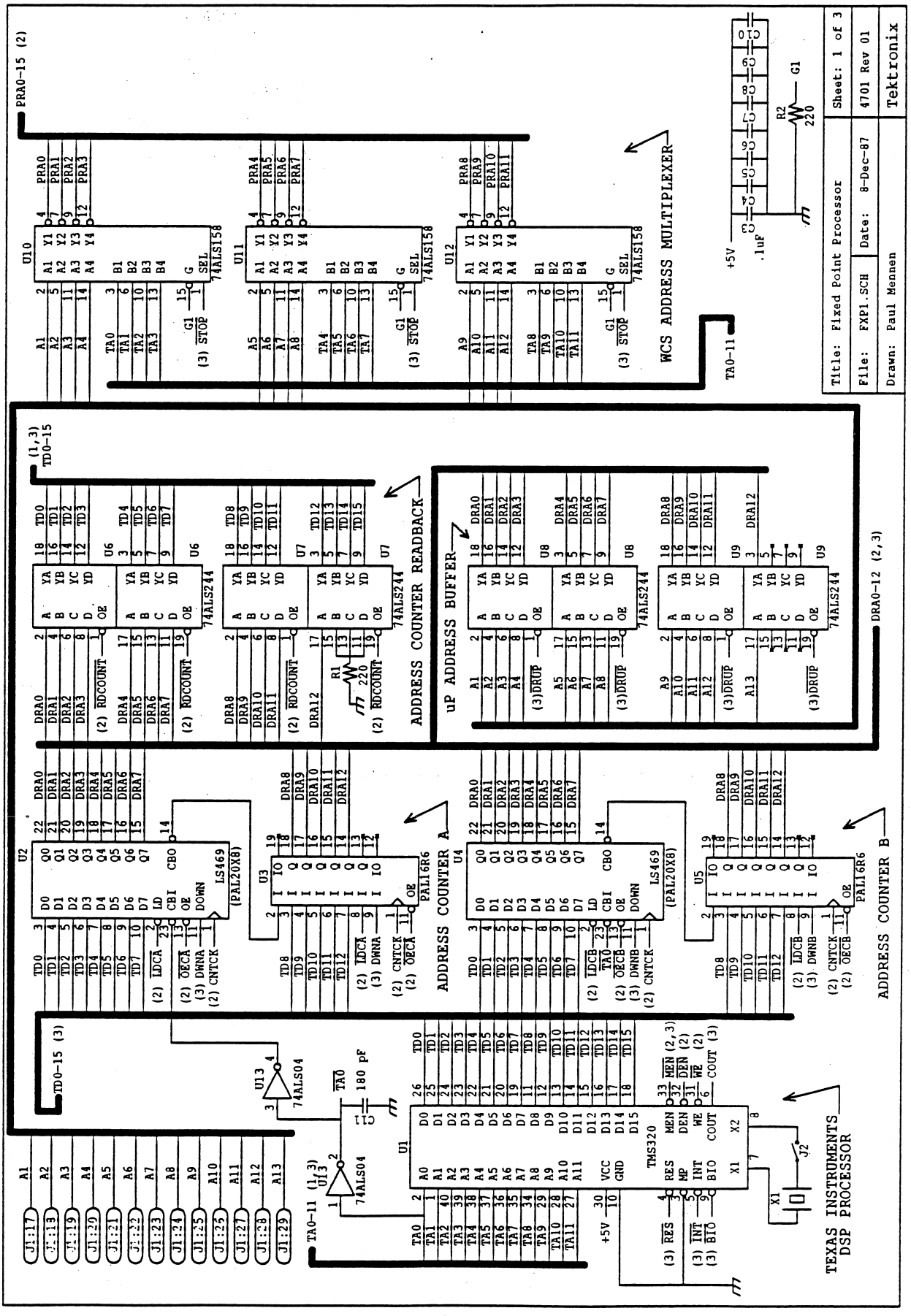

PORT 1 CONTROL
BAUD RATE DIVIDERS
PORT 2 CONTROL
BAUD RATE OSCILLATOR
19.6608 MHz
RECEIVE CLOCK
PHASE LOCKED LOOP
REFRESH GENERATOR
UART
RS422 DRIVER
RS423 DRIVER
SERIAL PORT #1
SERIAL PORT #2
FRONT PANEL
FXP CONNECTOR
RS422/423 RECEIVER
Install R10,R11 only for RS422
Title: 2630 Mother Board
File: MBD4.SCH
Date: 8-Dec-87
Drawn: Paul Mennen
Sheet: 4 of 8
4700 Rev 06
Tektronix

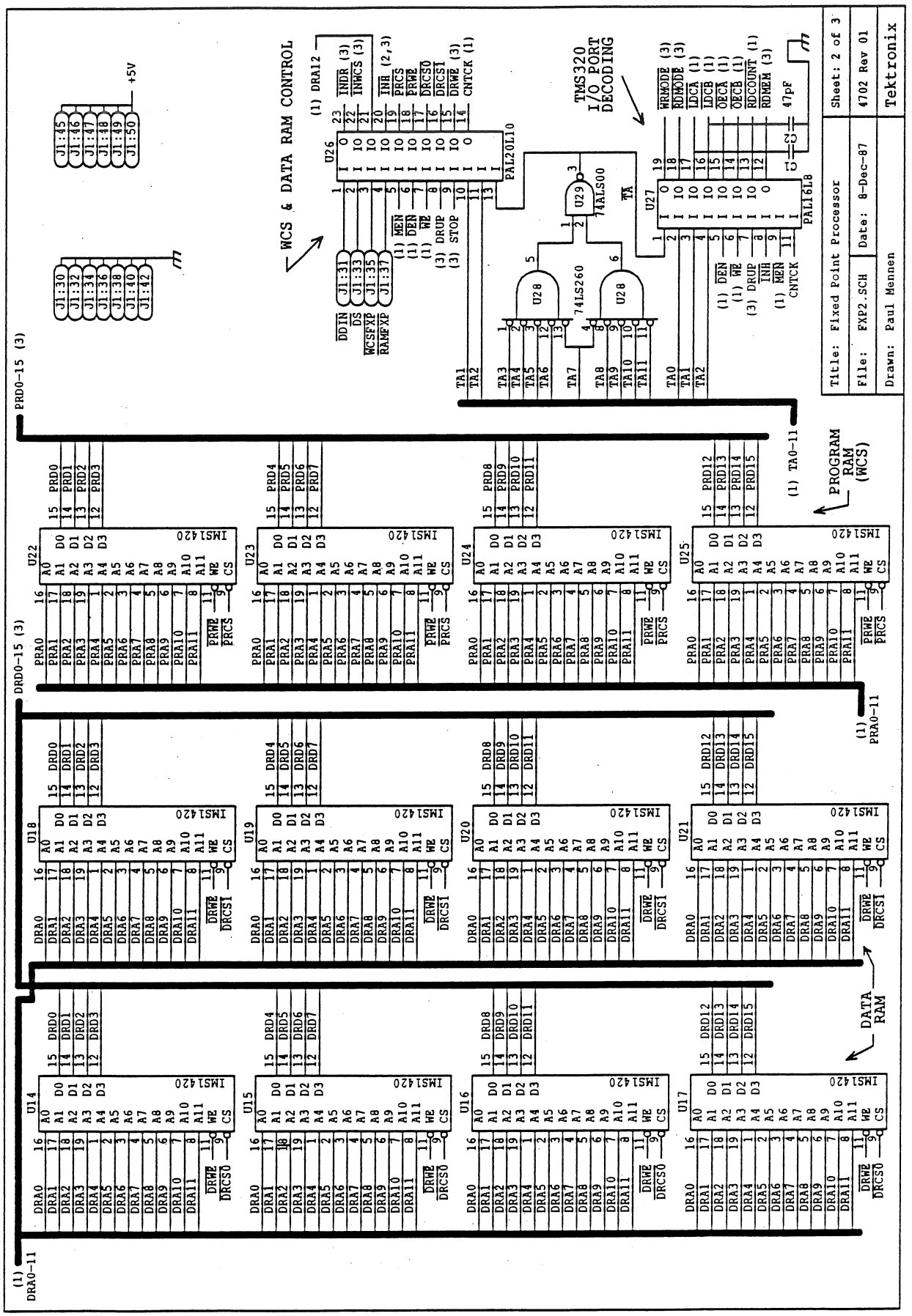

Title: 2630 Mother Board (WCS)
Sheet: 5 of 8
File: DFBWCS.SCH
Date: 8-Dec-87
4700 Rev 06
Drawn: R.A. Benson
Tektronix
U84
U85
U86
U87
U88
U89
U90
U91
U92
U82
U83
ALS158
IMS1420
ALS245
(1) A0-12
(1) D0-15
(5) WRWCS
(6)SRUN
(1) DDIN
(8) DFETIR
(2) WCSDFB
UPD0-15 (6,7,8)
R35
220
G5

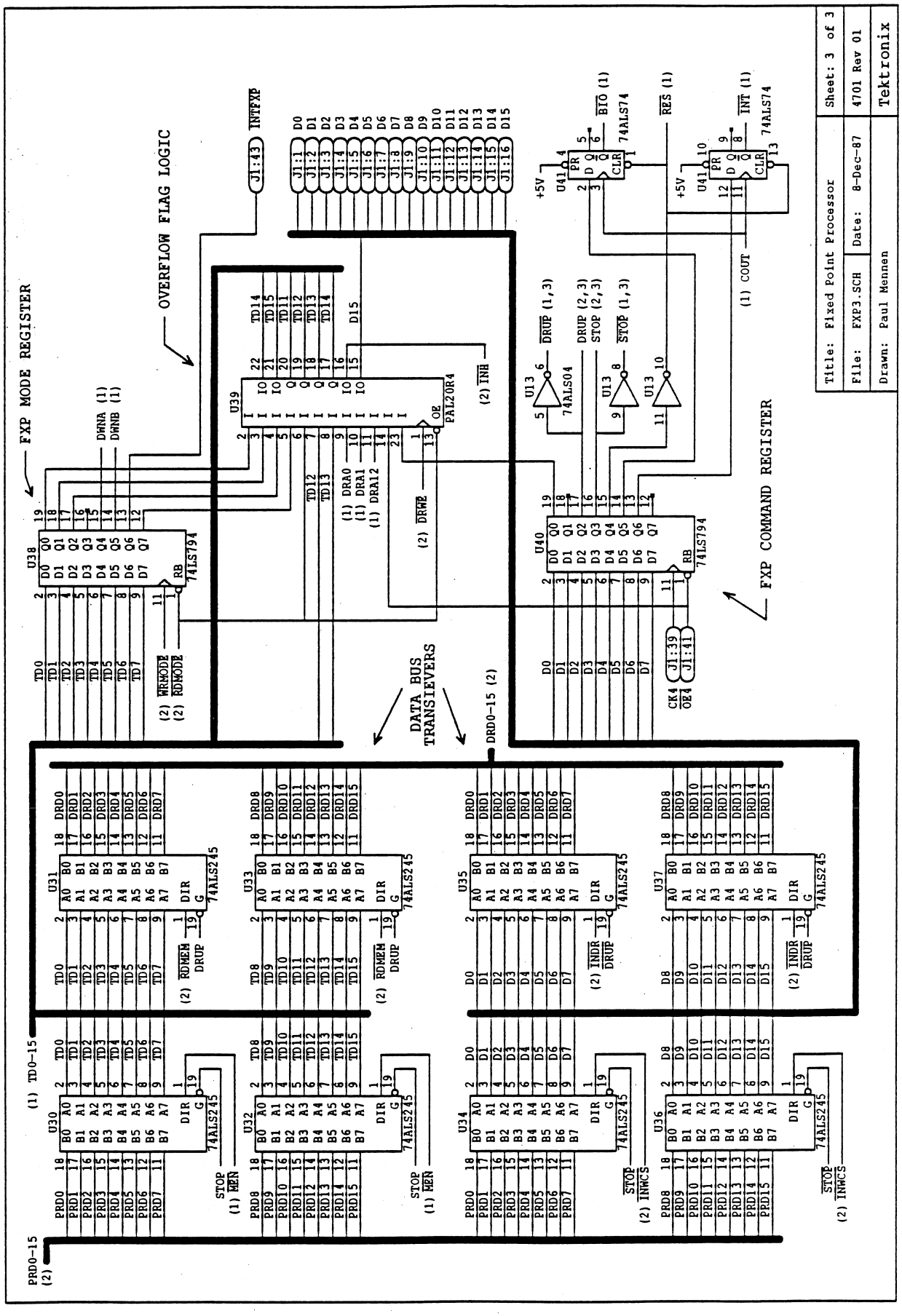

Title: 2630 Mother Board. (Trigger)
Sheet: 6 of 8
File: DFETRG.SCH
Date: 7-Dec-87
4700 Rev 06
Drawn: R. A. BENSON
Tektronix

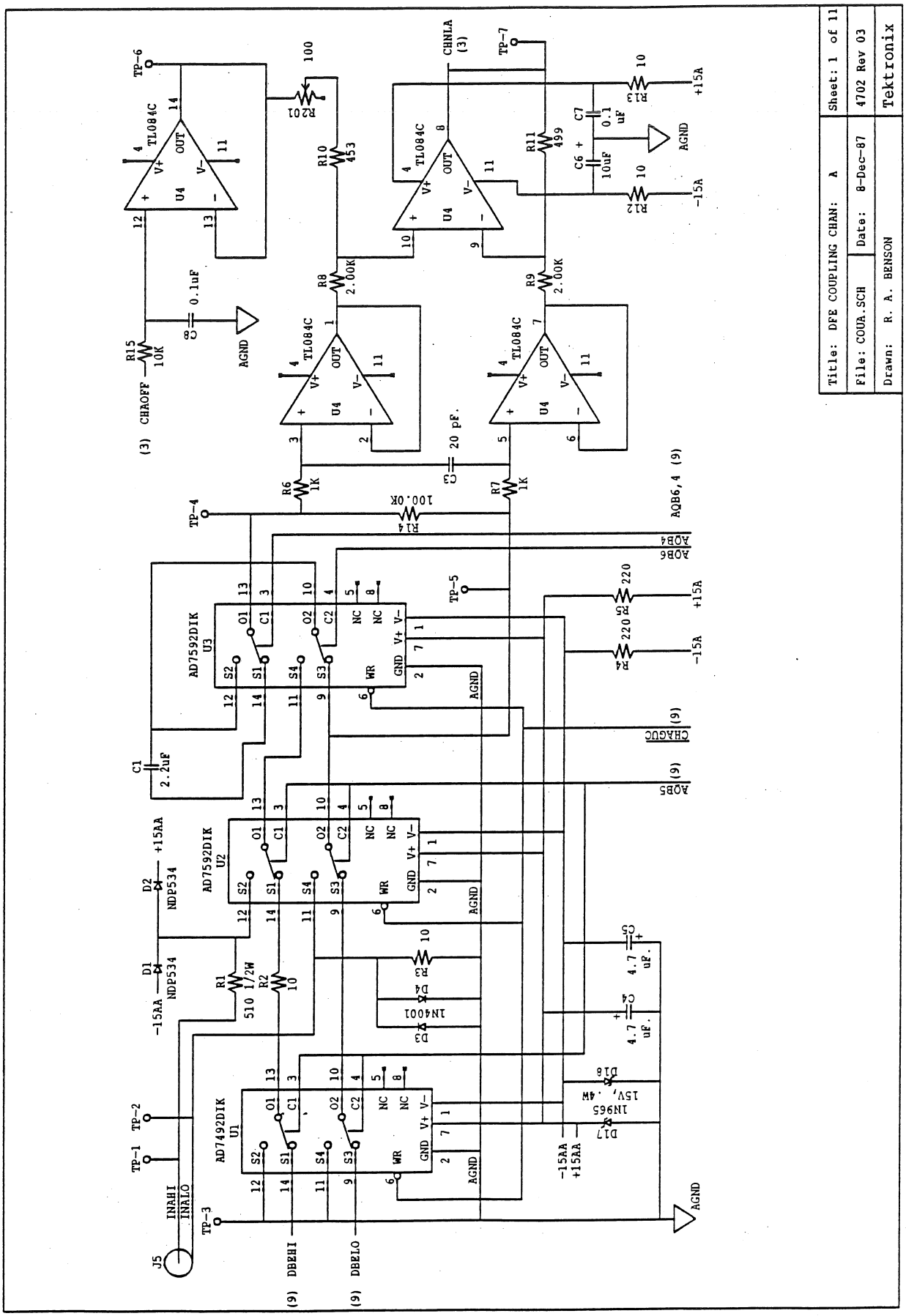

Title: 2630 Mother Board
Sheet: 7 of 8
File: DFETWIST.SCH
Date: 8-Dec-87
4700 Rev 06
Drawn: R. A. BENSON
Tektronix
U111
U112
U113
U114
U115
U116
U117
U118
U119
U109
U110
LS283
LS273
LS794
2764
TP-61
TP-62
TP-63
TP-64
TP-79
BS2
DFE
BTRA
RDCTS
(COSINE)
WRCF
RDCF

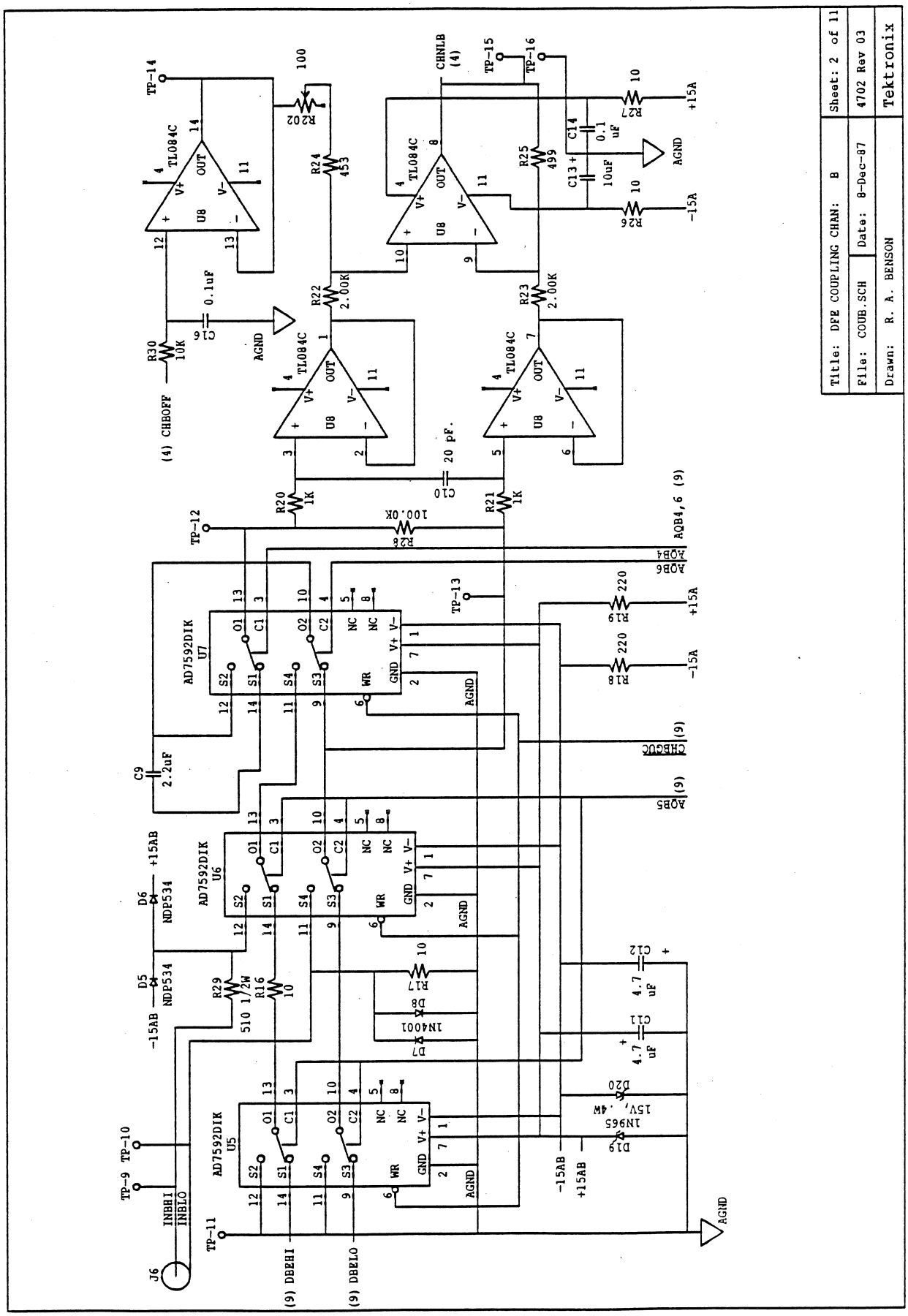

Title: 2630 Mother Board (DFE Intfc)
Sheet: 8 of 8
File: DFEMSC.SCH
Date: 7-Dec-87
4700 Rev 06
Drawn: R. A. BENSON
Tektronix

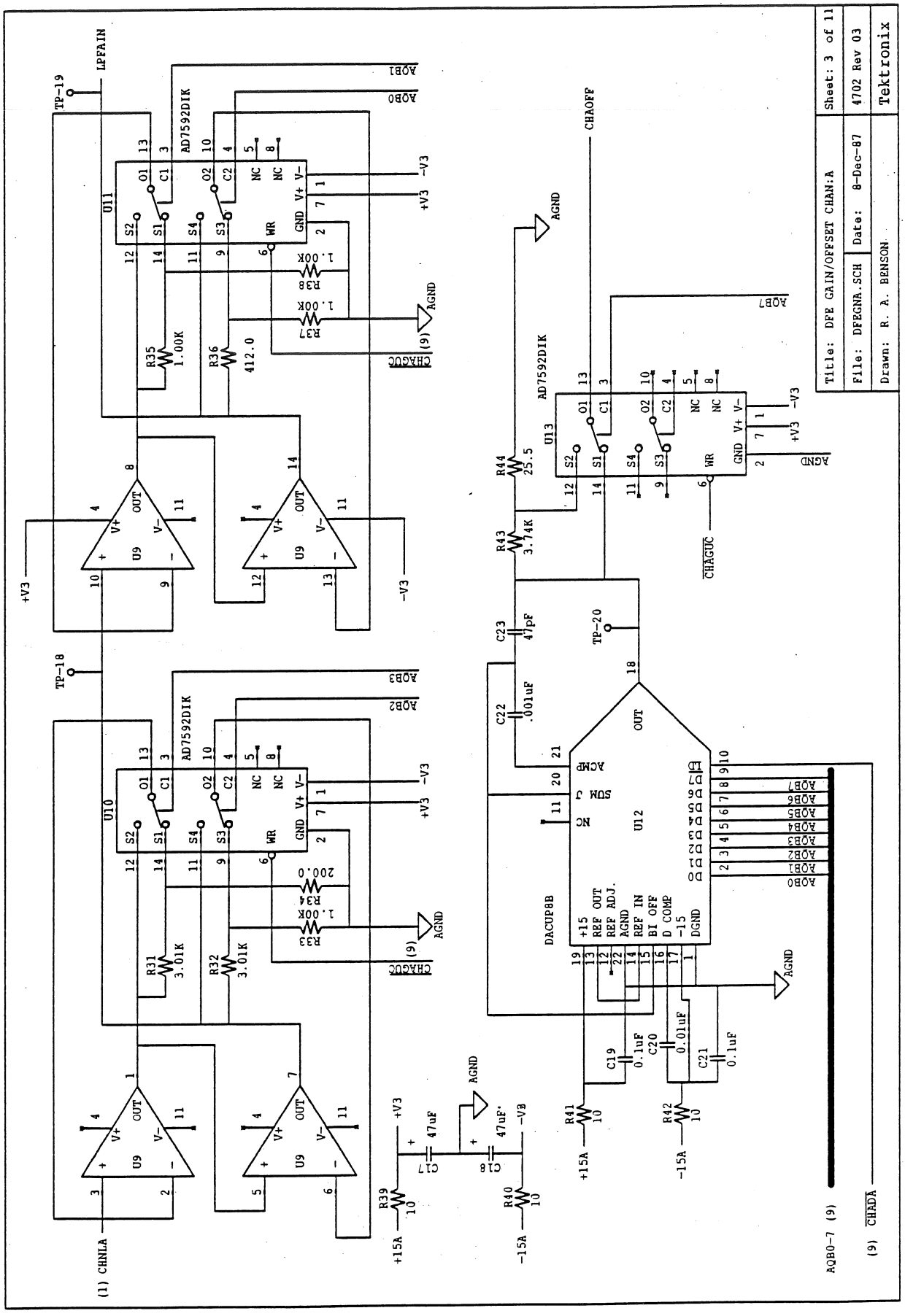

PRA0-15 (2)
WCS ADDRESS MULTIPLEXER
TA0-11
+5V
.1uF
R2
220
G1
Title: Fixed Point Processor
Sheet: 1 of 3
File: FXP1.SCH
Date: 8-Dec-87
4701 Rev 01
Drawn: Paul Mennen
Tektronix
(1,3) TD0-15
ADDRESS COUNTER READBACK
uP ADDRESS BUFFER
DRA0-12 (2,3)
ADDRESS COUNTER A
ADDRESS COUNTER B
TD0-15 (3)
TA0
180 pF
TEXAS INSTRUMENTS
DSP PROCESSOR
TMS320
74ALS244
74ALS158
74ALS04
PAL16R6
PAL20X8
LS469

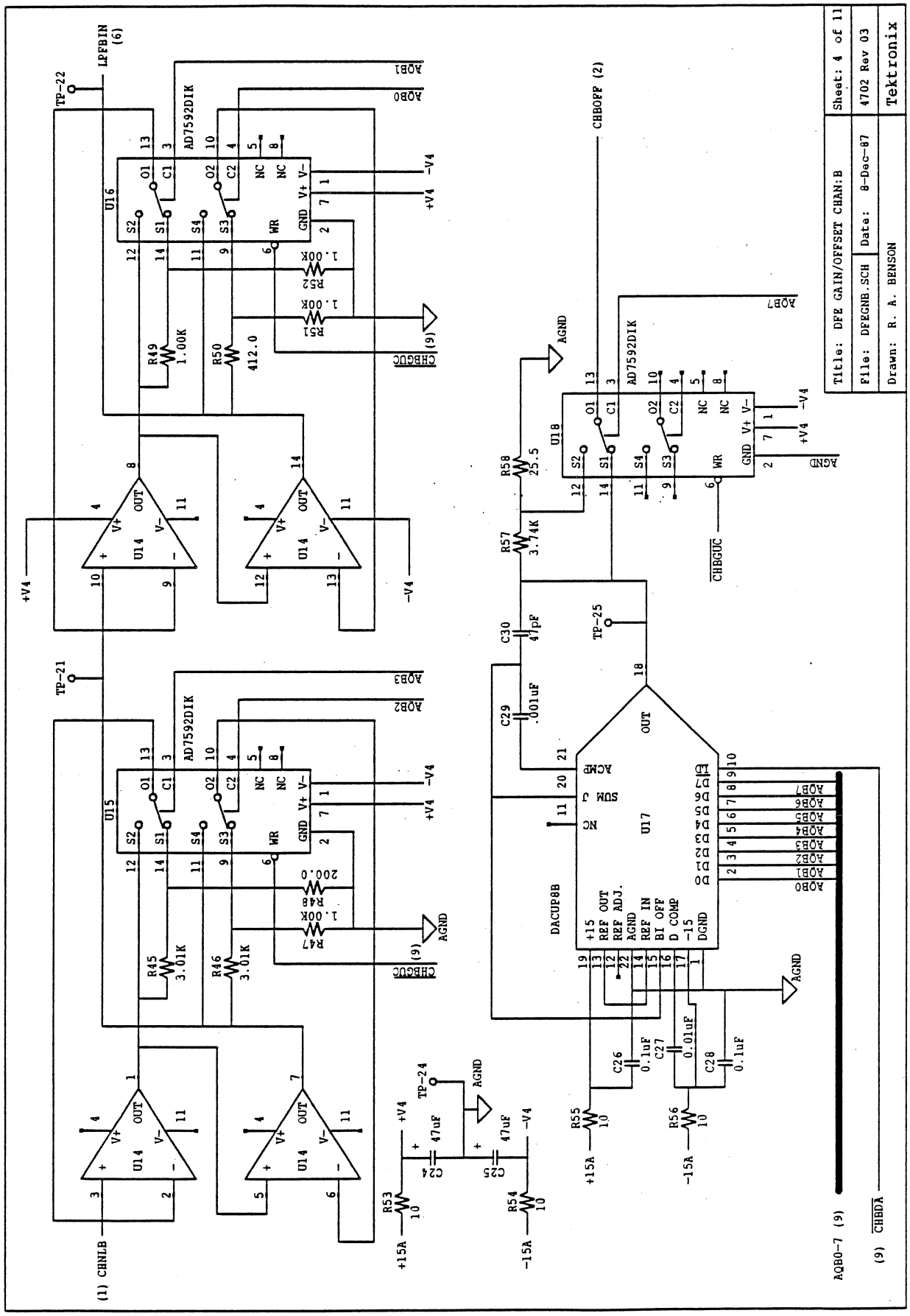

WCS & DATA RAM CONTROL
TMS320 I/O PORT DECODING
PROGRAM RAM (WCS)
DATA RAM
PRD0-15 (3)
DRD0-15 (3)
(1) DRA0-11
(1) PRA0-11
(1) TA0-11
+5V
47pF
PAL20L10
PALI6L8
74ALS00
74LS260
IMS1420
Title: Fixed Point Processor
Sheet: 2 of 3
File: FXP2.SCH
Data: 8-Dec-87
4702 Rev 01
Drawn: Paul Mennen
Tektronix

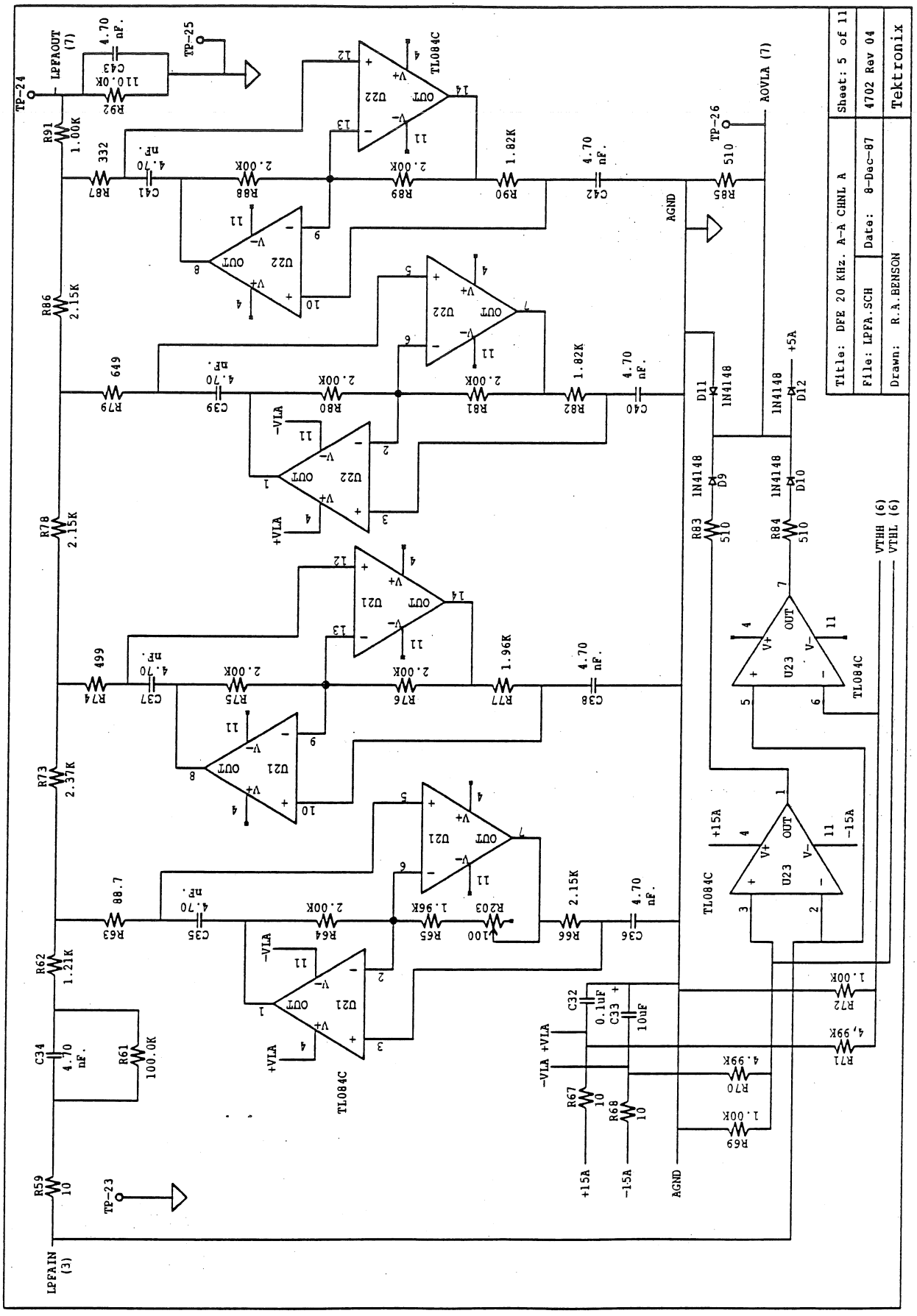

FXP MODE REGISTER
OVERFLOW FLAG LOGIC
FXP COMMAND REGISTER
DATA BUS TRANSCEIVERS
INTFXP
DWNA (1)
DWNB (1)
(2) WRMODE
(2) RDMODE
(2) INH
(2) DRWE
(1) DRA0
(1) DRA1
(1) DRA12
DRUP (1,3)
DRUP (2,3)
STOP (2,3)
STOP (1,3)
(1) COUT
BIO (1)
RES (1)
INT (1)
(1) TD0-15
PRD0-15 (2)
DRD0-15 (2)
(1) MEN
(2) INWCS
(2) RDMEM
(2) INDR
Title: Fixed Point Processor
File: FXP3.SCH
Drawn: Paul Mennen
Date: 8-Dec-87
Sheet: 3 of 3
4701 Rev 01
Tektronix

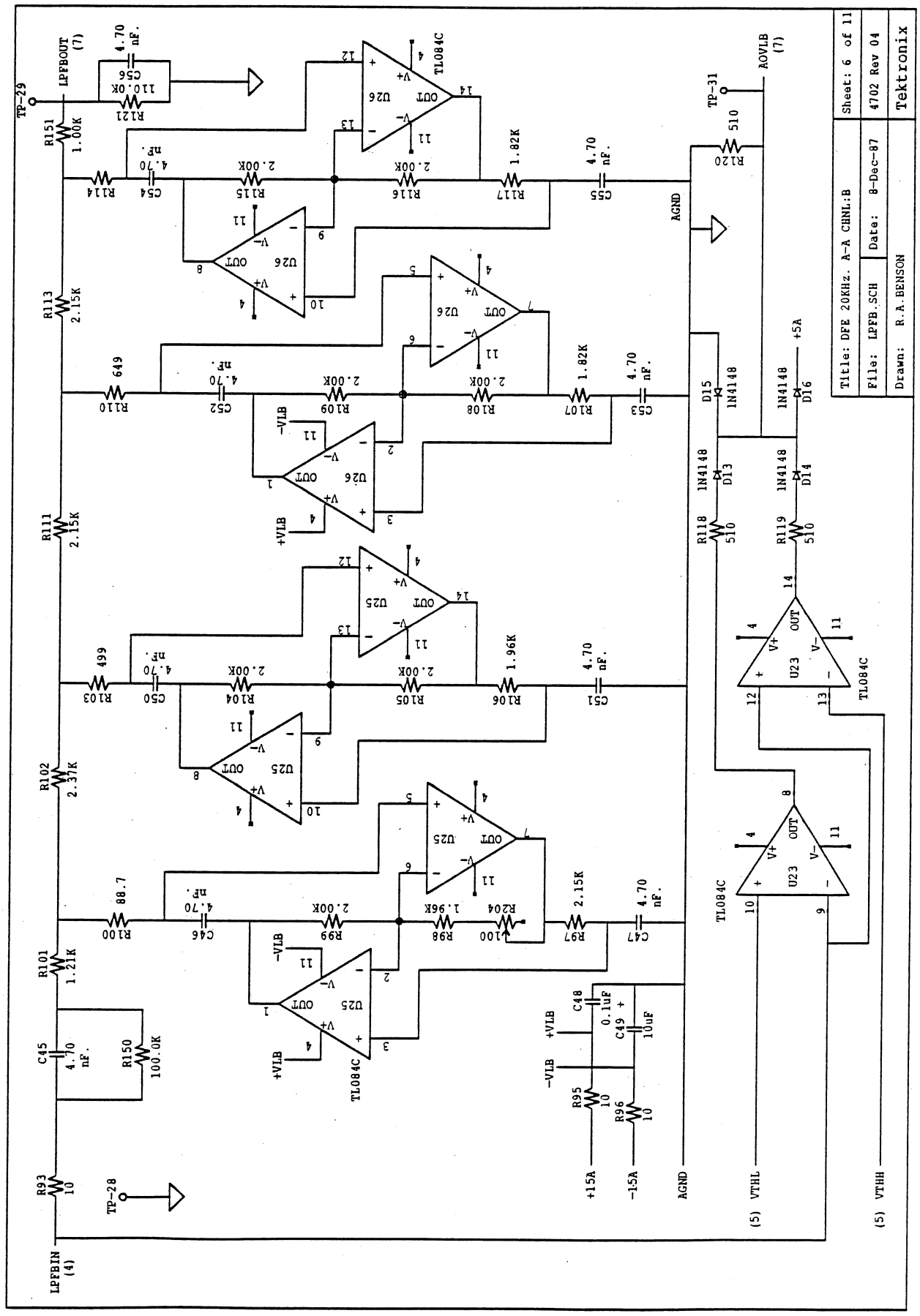

Title: DFE COUPLING CHAN: A
Sheet: 1 of 11
File: COUA.SCH
Date: 8-Dec-87
4702 Rev 03
Drawn: R. A. BENSON
Tektronix
TL084C
AD7592DIK
AD7492DIK
NDP534
IN4001
IN965
2.00K
1K
100.0K
453
499
510 1/2W
2.2uF
0.1uF
20 pF.
4.7 uF.
15V, .4W
+15A
-15A
-15AA
+15AA
AGND
CHNLA (3)
(3) CHAOFF
INAHI
INALO
DBEHI
DBELO
CHAGUC (9)
AQB6,4 (9)
AQB5 (9)
AQB4
AQB6

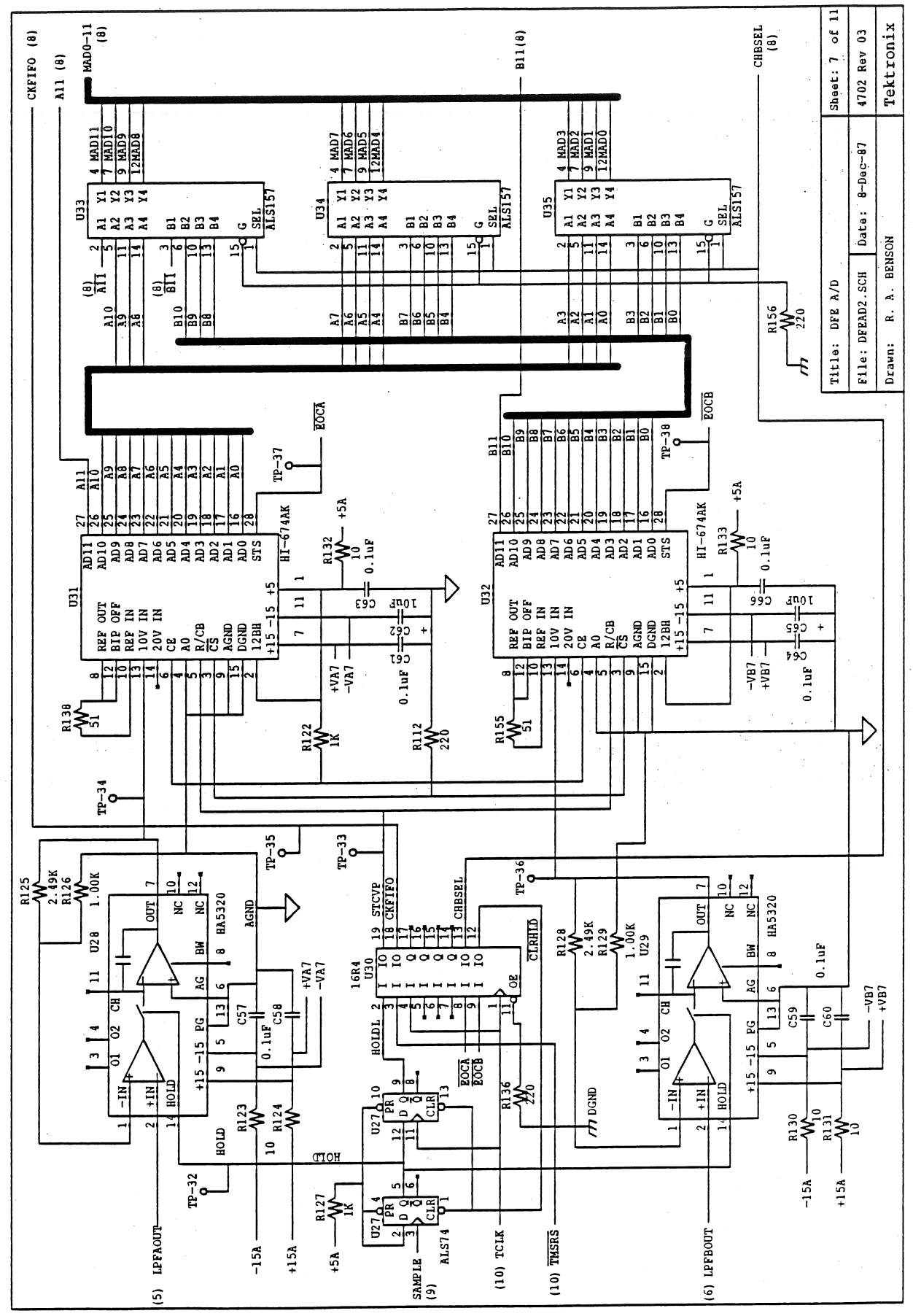

Title: DFE COUPLING CHAN: B
Sheet: 2 of 11
File: COUB.SCH
Date: 8-Dec-87
4702 Rev 03
Drawn: R. A. BENSON
Tektronix
TP-14
TP-15
TP-16
TP-12
TP-13
TP-9
TP-10
TP-11
CHNLB (4)
(4) CHBOFF
TL084C
AD7592DIK
U5
U6
U7
U8
R202
R24
R25
R27
R26
R22
R23
R30
R20
R21
R28
R29
R16
R17
R18
R19
C5
C6
C9
C10
C11
C12
C13
C14
D5
D6
D7
D8
D19
D20
NDP534
IN4001
IN965
AGND
+15A
-15A
+15AB
-15AB
INBHI
INBLO
J6
(9) DBEHI
(9) DBELO
AQB4,6 (9)
AQB4
AQB6
AQB5
CHBGUC (9)
100
453
499
2.00K
1K
100.0K
0.1uF
20 pF.
2.2uF
4.7 uF
10uF
0.1 uF
220
10
510 1/2W

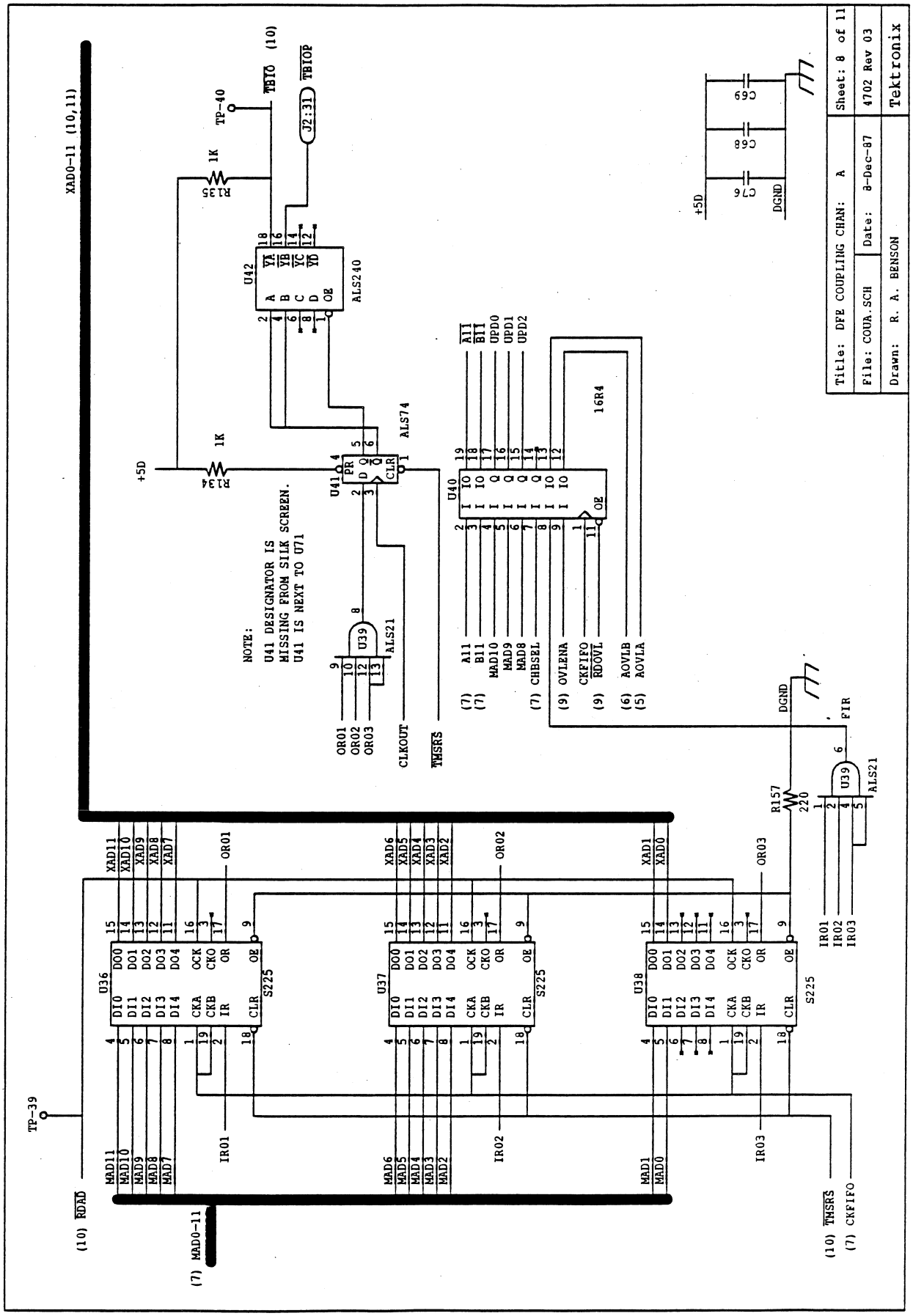

Title: DFE GAIN/OFFSET CHAN:A
Sheet: 3 of 11
File: DFEGNA.SCH
Date: 8-Dec-87
4702 Rev 03
Drawn: R. A. BENSON
Tektronix
LPFAIN
TP-19
TP-18
TP-20
AD7592DIK
U11
U10
U13
U12
DACUP8B
R35 1.00K
R36 412.0
R37 1.00K
R38 1.00K
R31 3.01K
R32 3.01K
R33 1.00K
R34 200.0
R43 3.74K
R44 25.5
R39 10
R40 10
R41 10
R42 10
C19 0.1uF
C20 0.01uF
C21 0.1uF
C22 .001uF
C23 47pF
C17 47uF
C18 47uF
CHAOFF
CHAGUC
CHADA
AGND
+V3
-V3
+15A
-15A
AQB0
AQB1
AQB2
AQB3
AQB4
AQB5
AQB6
AQB7
AQB0-7 (9)
(1) CHNLA
(9) CHAGUC
(9) CHADA

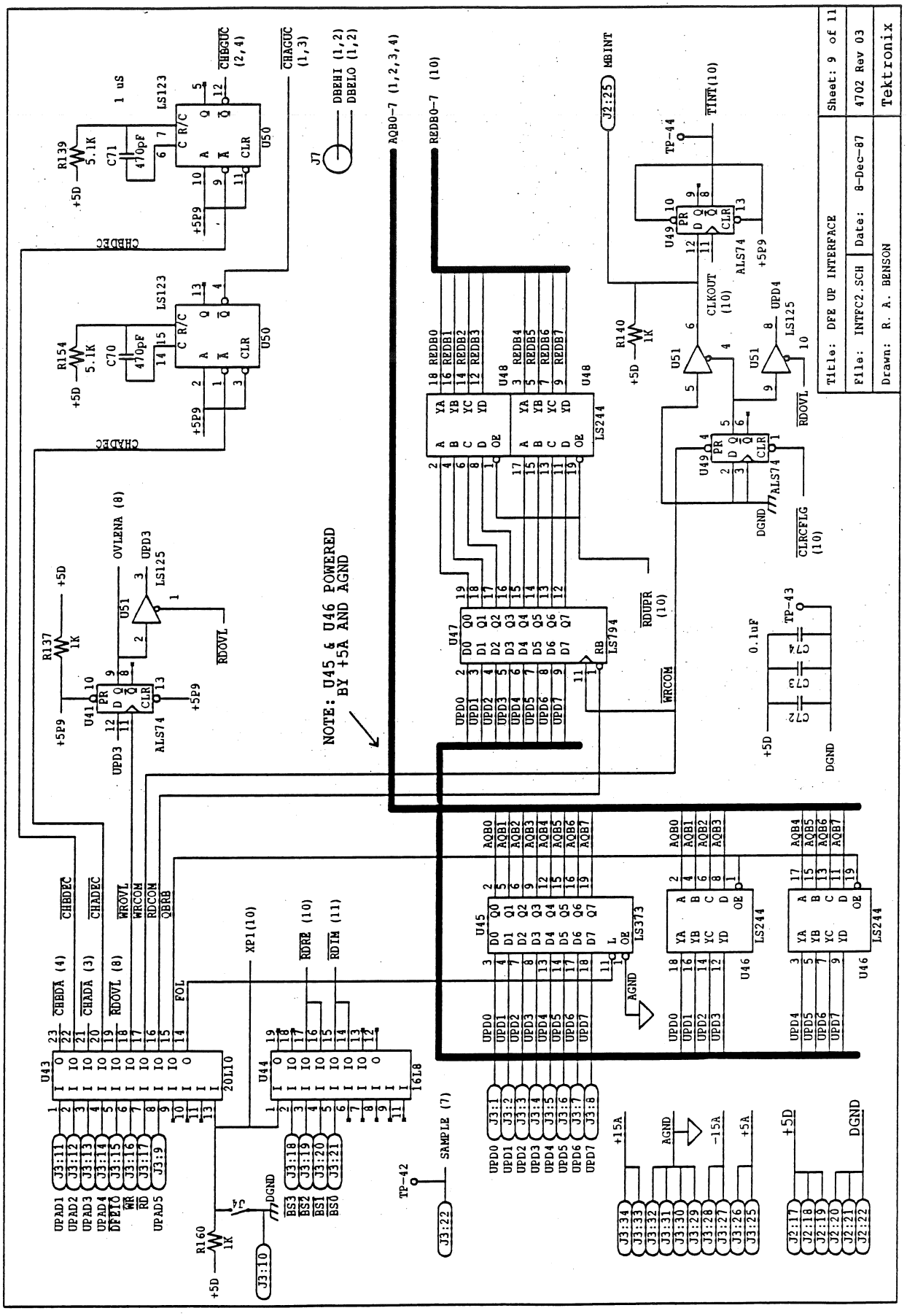

Title: DFE GAIN/OFFSET CHAN:B
Sheet: 4 of 11
File: DFEGNB.SCH
Date: 8-Dec-87
4702 Rev 03
Drawn: R. A. BENSON
Tektronix
LFFBIN (6)
CHBOFF (2)
AD7592DIK
U16
U15
U18
U17
DACUP8B
R49 1.00K
R50 412.0
R51 1.00K
R52 1.00K
R45 3.01K
R46 3.01K
R47 1.00K
R48 200.0
R57 3.74K
R58 25.5
C30 47pF
C29 .001uF
C26 0.1uF
C27 0.01uF
C28 0.1uF
C24 47uF
C25 47uF
R53 10
R54 10
R55 10
R56 10
TP-21
TP-22
TP-24
TP-25
+V4
-V4
AGND
+15A
-15A
CHBGUC
(9)
(1) CHNLB
AQB0-7 (9)
(9) CHBDA

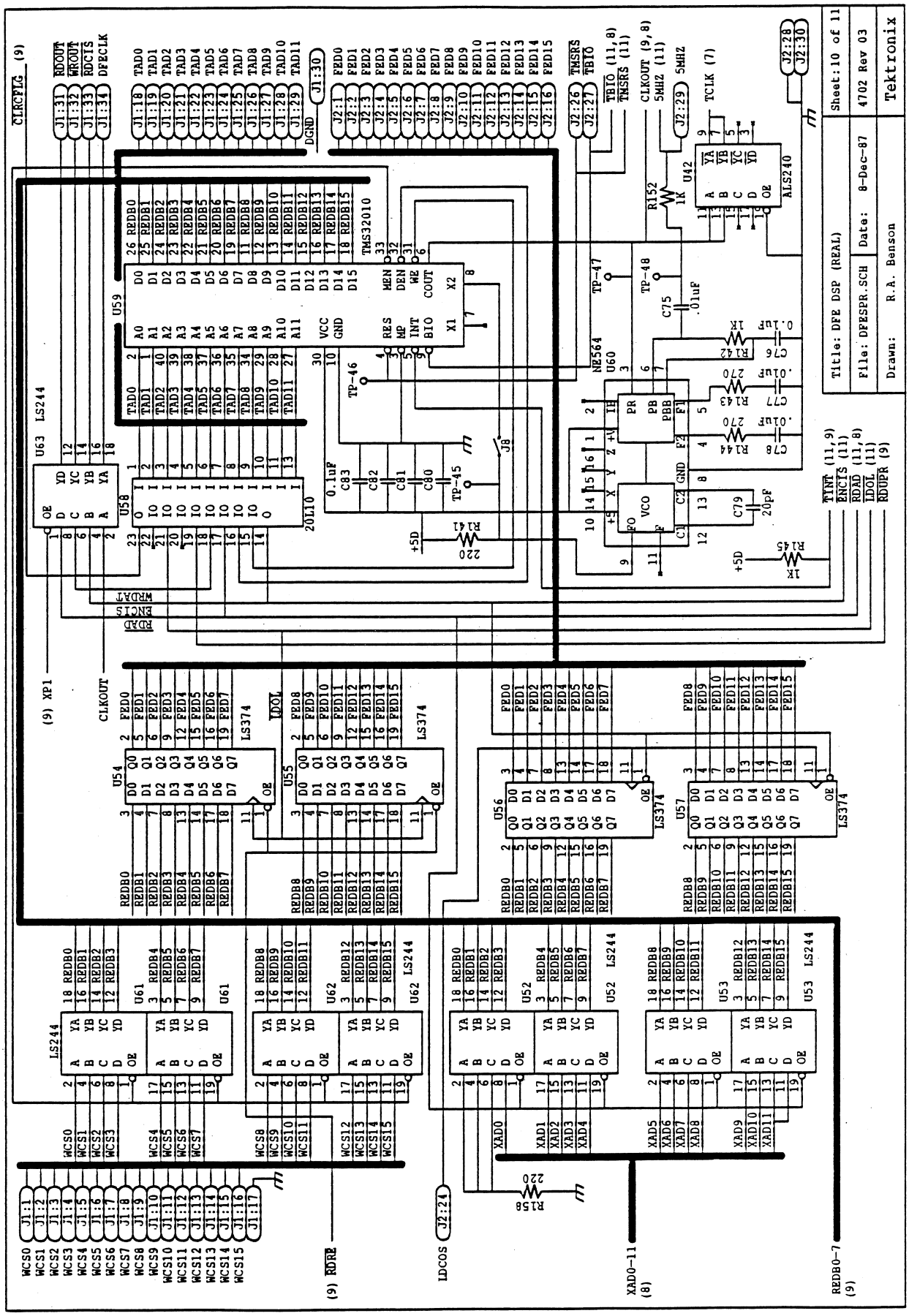

Title: DFE 20 KHz. A-A CHNL A
File: LPFA.SCH
Drawn: R.A.BENSON
Date: 8-Dec-87
Sheet: 5 of 11
4702 Rev 04
Tektronix
TP-24
TP-25
TP-26
TP-23
LPFAOUT (7)
LPFAIN (3)
AOVLA (7)
AGND
+5A
+15A
-15A
+VLA
-VLA
VTHH (6)
VTHL (6)
TL084C
1N4148
R91 1.00K
R92 110.0K
C43 4.70 nF.
R87 332
C41 4.70 nF.
R88 2.00K
R89 2.00K
R90 1.82K
C42 4.70 nF.
R85 510
R86 2.15K
R79 649
C39 4.70 nF.
R80 2.00K
R81 2.00K
R82 1.82K
C40 4.70 nF.
R78 2.15K
R74 499
C37 4.70 nF.
R75 2.00K
R76 2.00K
R77 1.96K
C38 4.70 nF.
R73 2.37K
R63 88.7
C35 4.70 nF.
R64 2.00K
R65 1.96K
R203 100
R66 2.15K
C36 4.70 nF.
R62 1.21K
C34 4.70 nF.
R61 100.0K
R59 10
C32 0.1uF
C33 10uF
R67 10
R68 10
R69 1.00K
R70 4.99K
R71 4.99K
R72 1.00K
D11 1N4148
D12 1N4148
D9 1N4148
D10 1N4148
R83 510
R84 510
U22
U21
U23

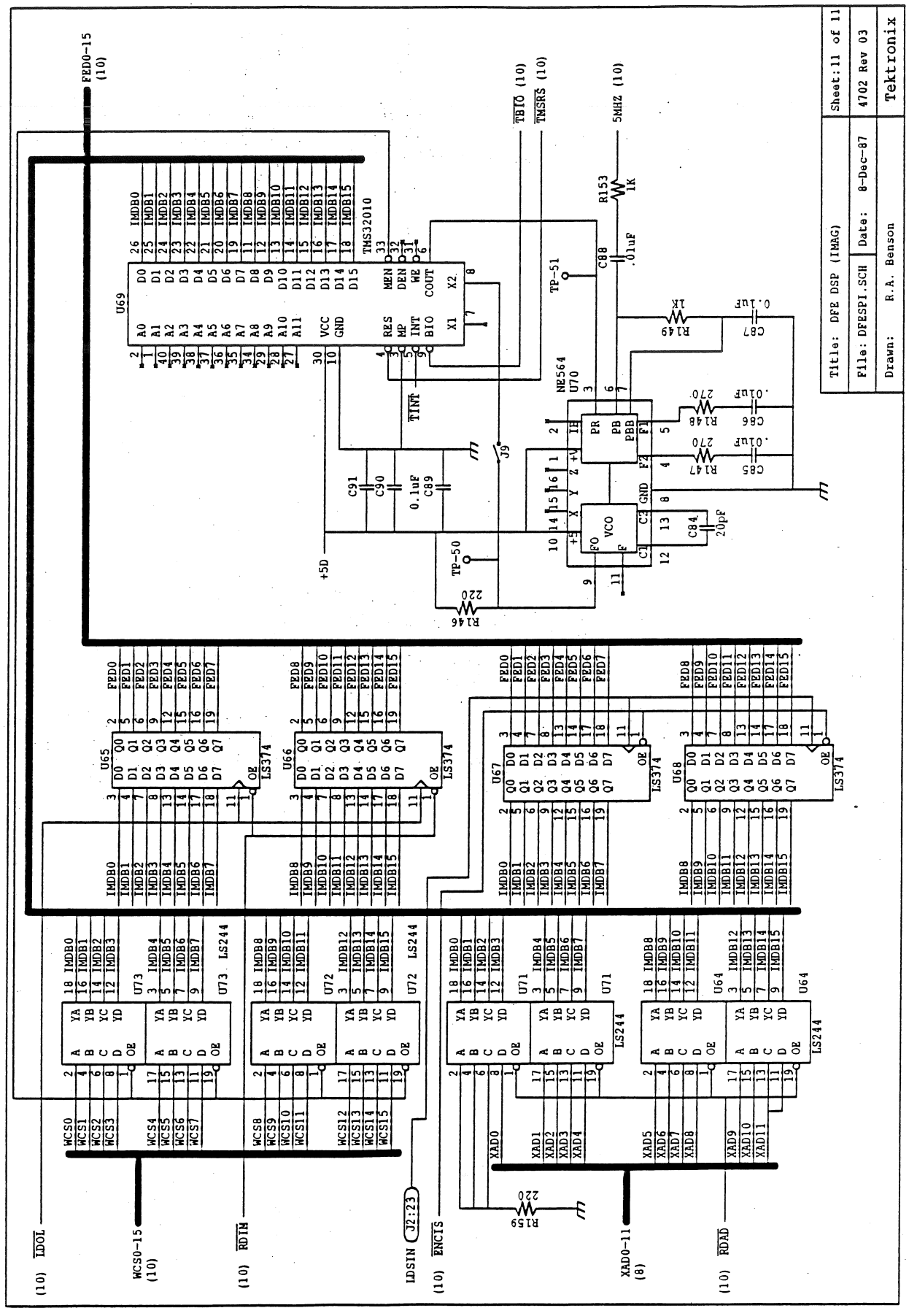

Title: DFE 20KHz. A-A CHNL:B
File: LPFB.SCH
Drawn: R.A.BENSON
Date: 8-Dec-87
Sheet: 6 of 11
4702 Rev 04
Tektronix
TP-29
LPFBOUT (7)
TP-31
AOVLB (7)
TP-28
LPFBIN (4)
AGND
+15A
-15A
+VLB
-VLB
+5A
(5) VTHL
(5) VTHH
TL084C
U23
U25
U26
D13
D14
D15
D16
1N4148

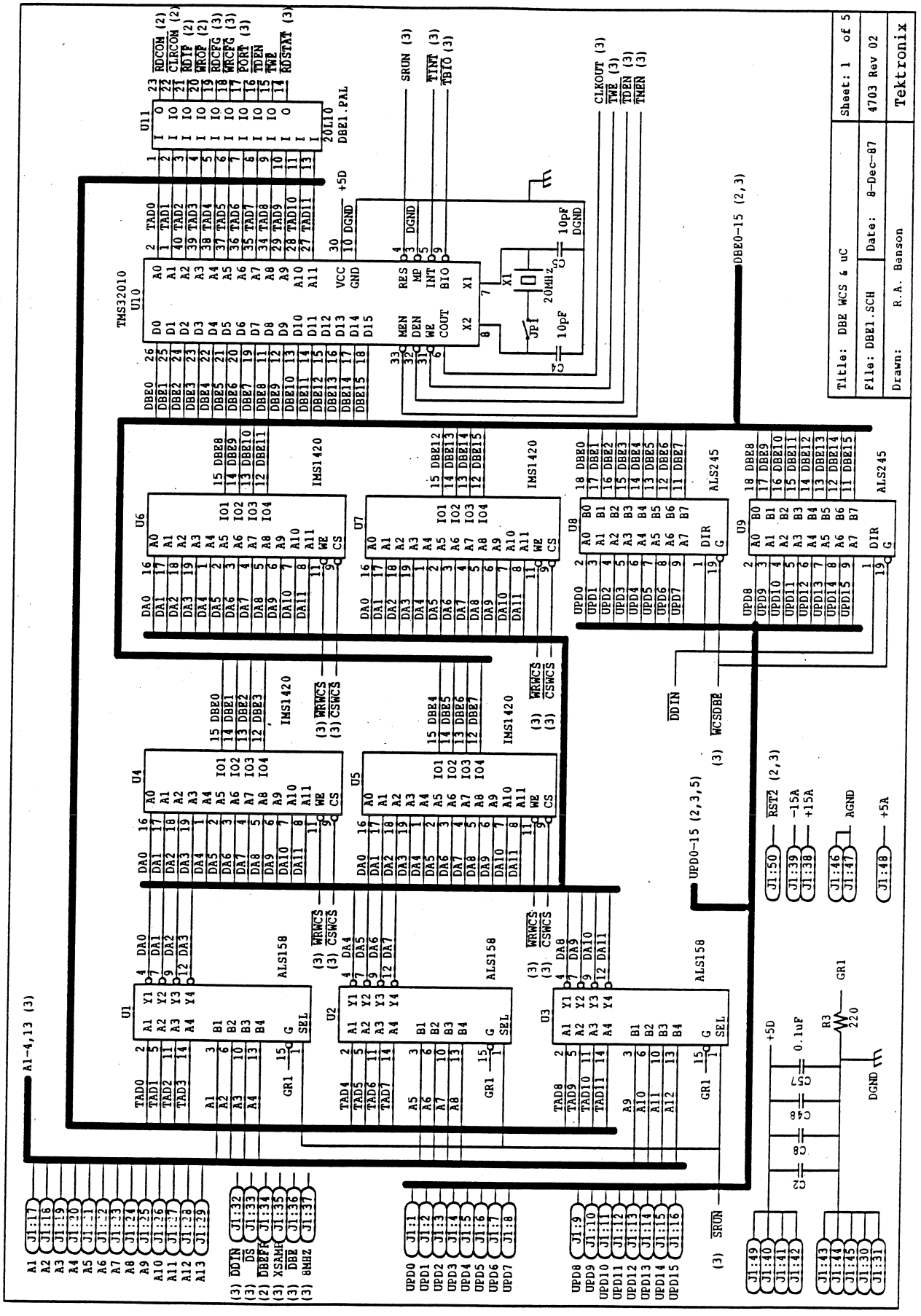

Title: DFE A/D
File: DFEAD2.SCH
Date: 8-Dec-87
Drawn: R. A. BENSON
Sheet: 7 of 11
4702 Rev 03
Tektronix
CKFIFO (8)
A11 (8)
MAD0-11 (8)
B11(8)
CHBSEL (8)
U31
U32
U33
U34
U35
HI-674AK
ALS157
HA5320
ALS74
16R4
U30
U27
U28
U29
R125
R126
R127
R128
R129
R130
R131
R132
R133
R136
R138
R155
R156
R112
R122
R123
R124
C57
C58
C59
C60
C61
C62
C63
C64
C65
C66
TP-32
TP-33
TP-34
TP-35
TP-36
TP-37
TP-38
EOCA
EOCB
HOLD
HOLDL
CLRHLD
STCVP
CKFIFO
CHBSEL
SAMPLE (9)
(10) TCLK
(10) TMSRS
(5) LPFAOUT
(6) LPFBOUT
+5A
-15A
+15A
+VA7
-VA7
+VB7
-VB7
DGND
AGND

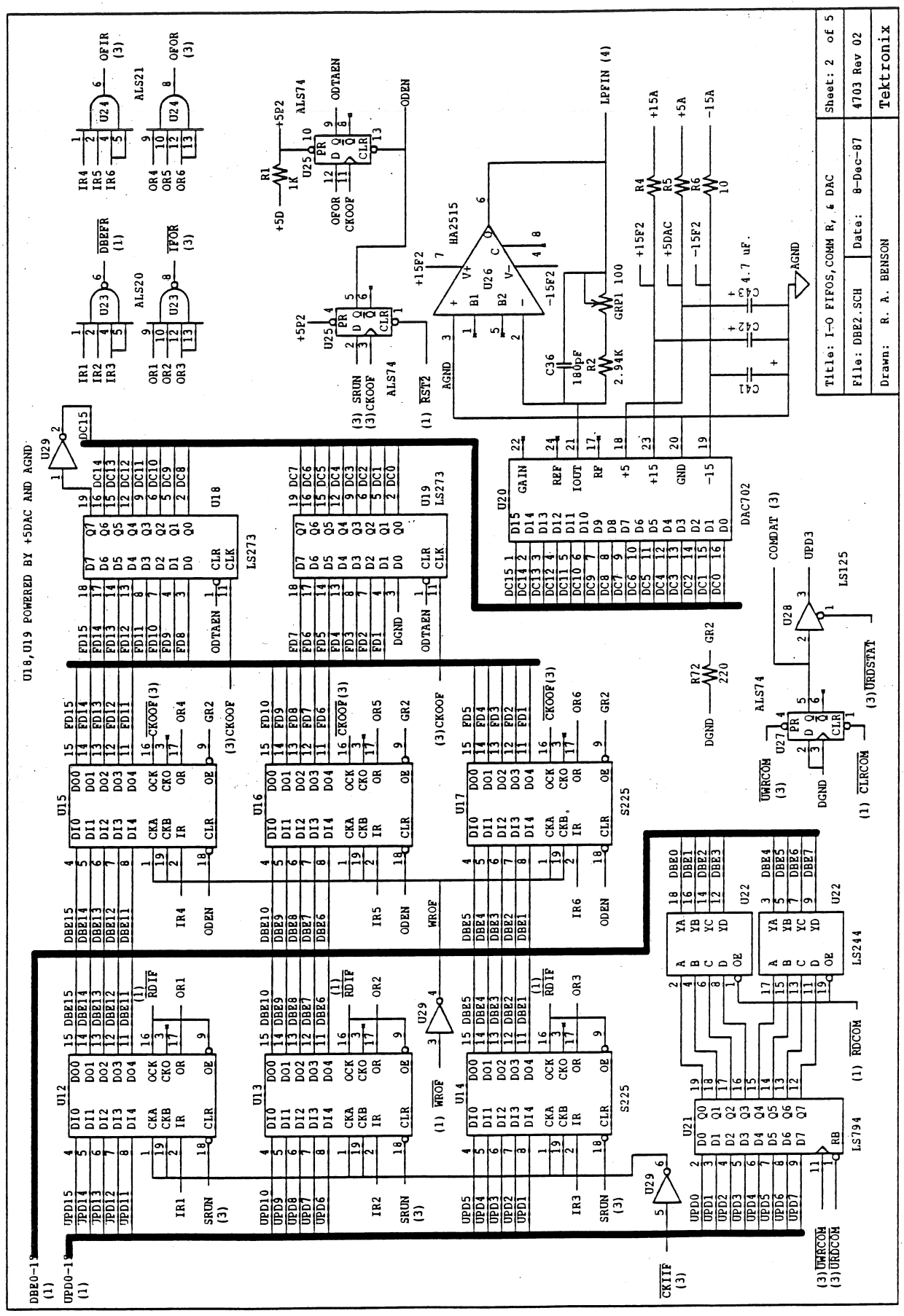

XAD0-11 (10,11)
TBIO (10)
TBIOP
TP-40
J2:31
R135
1K
U42
ALS240
R134
1K
+5D
U41
ALS74
U39
ALS21
NOTE:
U41 DESIGNATOR IS
MISSING FROM SILK SCREEN.
U41 IS NEXT TO U71
OR01
OR02
OR03
CLKOUT
TMSRS
U40
16R4
A11
B11
UPD0
UPD1
UPD2
MAD10
MAD9
MAD8
CHBSEL
OVLENA
CKFIFO
RDOVL
AOVLB
AOVLA
+5D
C76
C68
C69
DGND
Title: DFE COUPLING CHAN: A
Sheet: 8 of 11
File: COUA.SCH
Date: 8-Dec-87
4702 Rev 03
Drawn: R. A. BENSON
Tektronix
TP-39
RDAD
MAD0-11
XAD11
XAD10
XAD9
XAD8
XAD7
XAD6
XAD5
XAD4
XAD3
XAD2
XAD1
XAD0
MAD11
MAD10
MAD9
MAD8
MAD7
MAD6
MAD5
MAD4
MAD3
MAD2
MAD1
MAD0
U36
U37
U38
S225
IR01
IR02
IR03
R157
220
FIR
TMSRS
CKFIFO

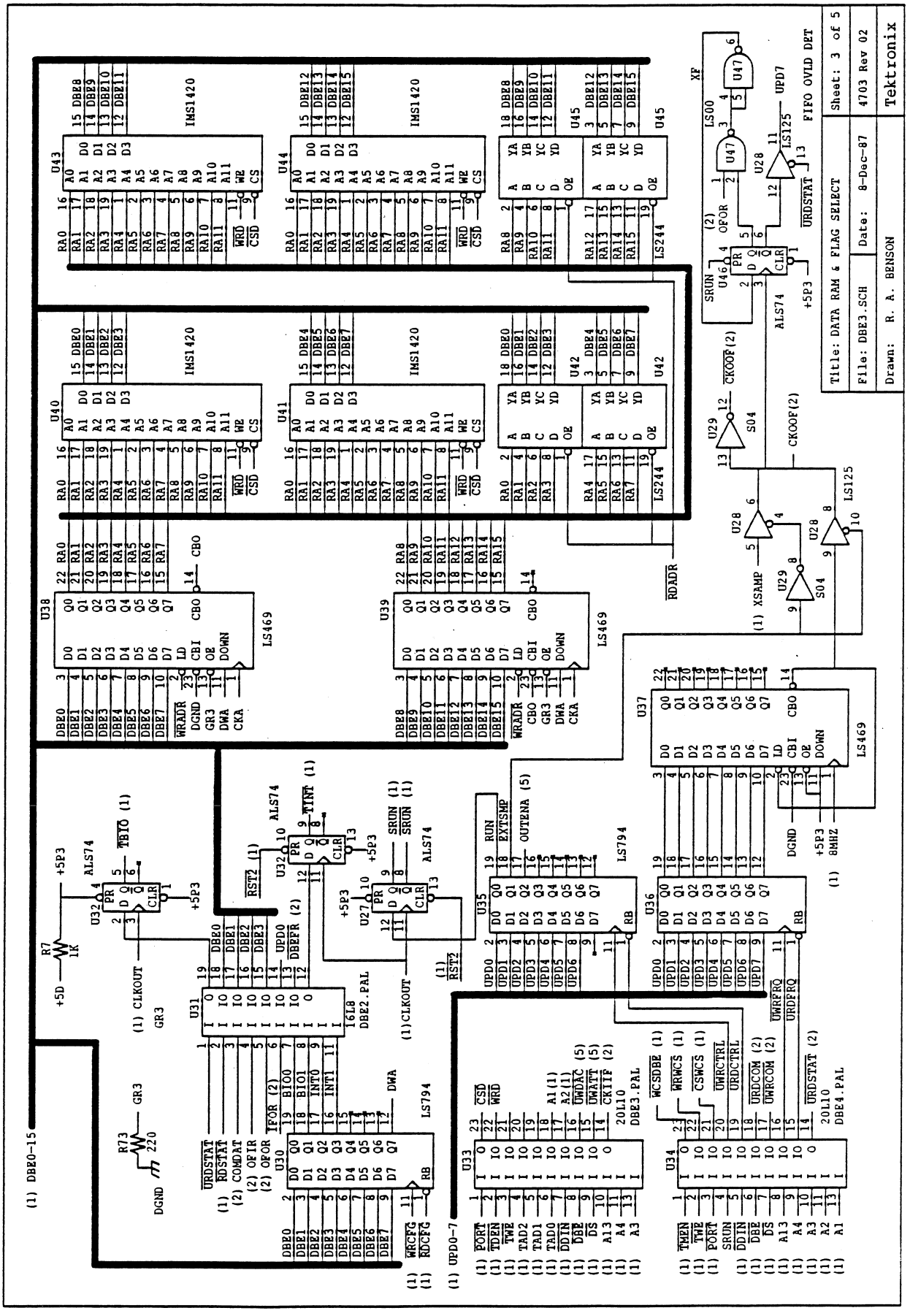

NOTE: U45 & U46 POWERED BY +5A AND AGND
Title: DFE UP INTERFACE
File: INTFC2.SCH
Drawn: R. A. BENSON
Date: 8-Dec-87
Sheet: 9 of 11
4702 Rev 03
Tektronix

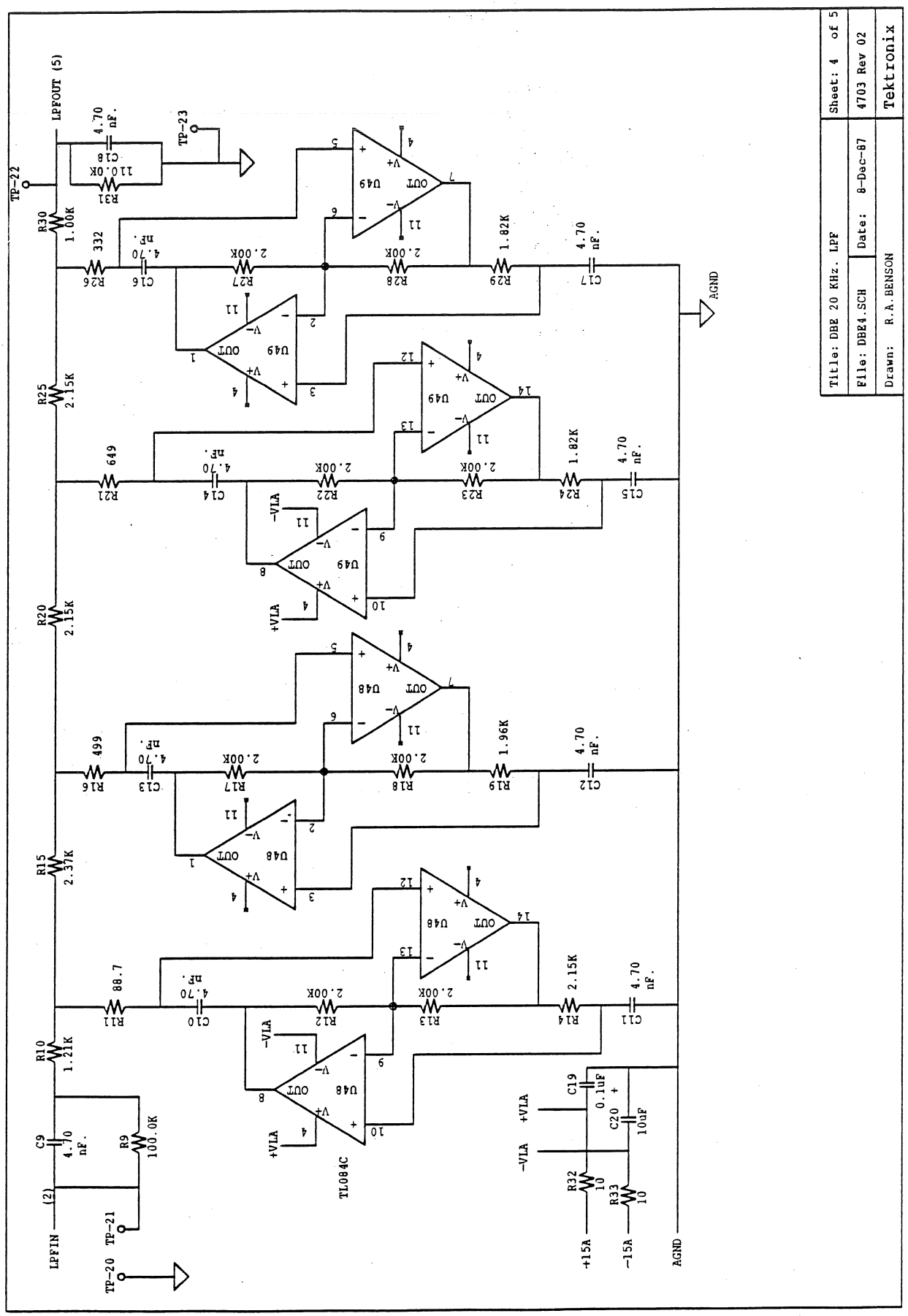

Title: DFE DSP (REAL)
File: DFESPR.SCH
Drawn: R.A. Benson
Data: 8-Dec-87
Sheet: 10 of 11
4702 Rev 03
Tektronix
CLKCFIG (9)
RDOUT
WROUT
RDCTS
DFECLK
TAD0
TAD1
TAD2
TAD3
TAD4
TAD5
TAD6
TAD7
TAD8
TAD9
TAD10
TAD11
DGND
FED0
FED1
FED2
FED3
FED4
FED5
FED6
FED7
FED8
FED9
FED10
FED11
FED12
FED13
FED14
FED15
TMSRS
TBIO (11,8)
TMSRS (11)
CLKOUT (9,8)
5MHZ (11)
5MHZ
TCLK (7)
U63 LS244
U58 20L10
U59 TMS32010
U60 NE564
U42 ALS240
U54 LS374
U55 LS374
U56 LS374
U57 LS374
U61 LS244
U62 LS244
U52 LS244
U53 LS244
(9) XP1
CLKOUT
IDOL
RDAD
ENCTS
WRDAT
TINT (11,9)
ENCTS (11)
RDAD (11,8)
IDOL (11)
RDUPR (9)
WCS0
WCS1
WCS2
WCS3
WCS4
WCS5
WCS6
WCS7
WCS8
WCS9
WCS10
WCS11
WCS12
WCS13
WCS14
WCS15
(9) RDRE
LDCOS
XAD0-11 (8)
REDB0-7 (9)

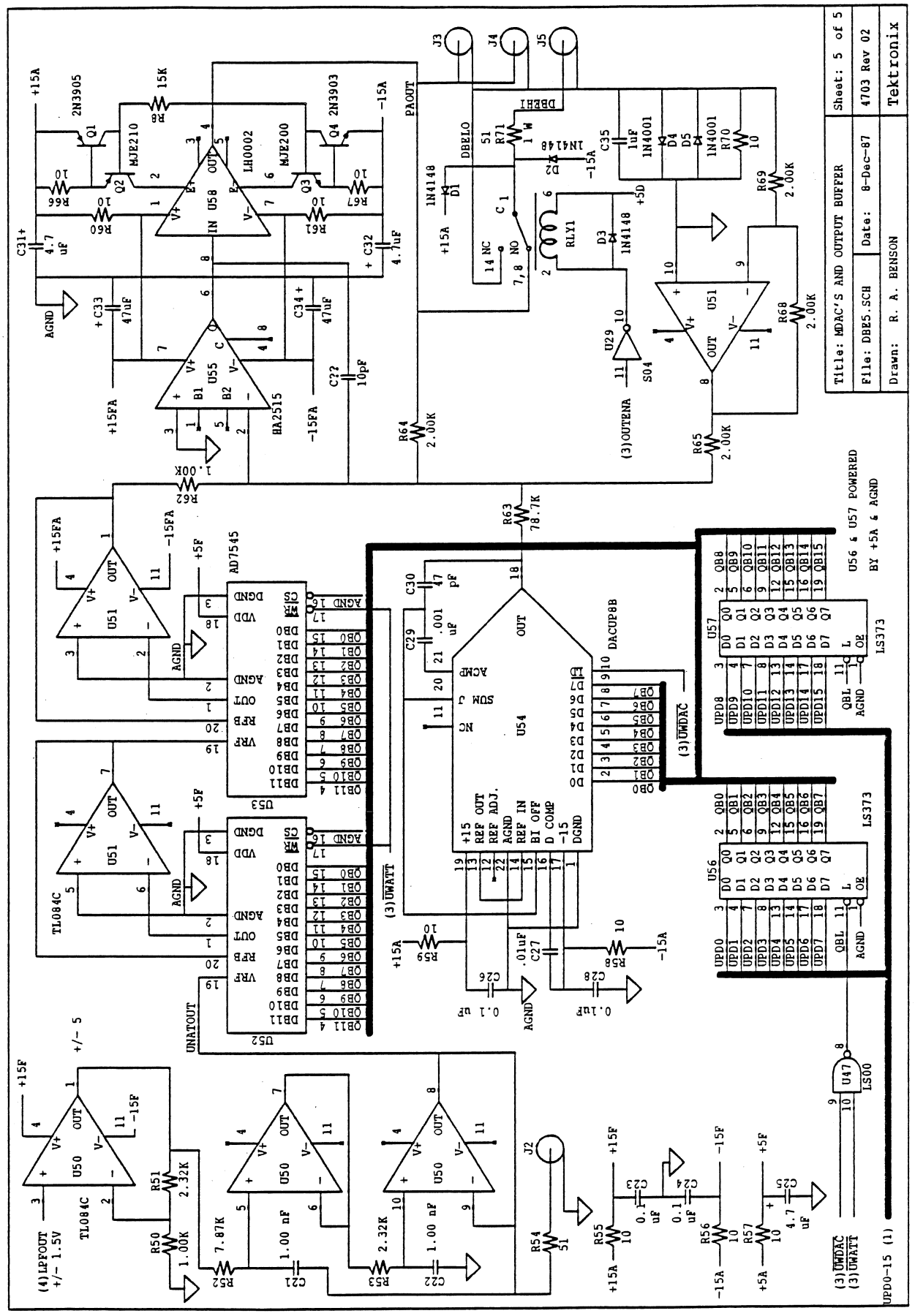

Title: DFE DSP (IMAG)
Sheet:11 of 11
File: DFESPI.SCH
Date: 8-Dec-87
4702 Rev 03
Drawn: R.A. Benson
Tektronix
FED0-15 (10)
TBIO (10)
TMSRS (10)
5MHZ (10)
TMS32010
NE564
VCO
LS374
LS244
TP-50
TP-51
+5D
J9
R146 220
R147 270
R148 270
R149 1K
R153 1K
C84 20pF
C85 .01uF
C86 .01uF
C87 0.1uF
C88 .01uF
C89 0.1uF
C90
C91
(10) LDOL
WCS0-15 (10)
(10) RDIM
LDSIN J2:23
(10) ENCIS
XAD0-11 (8)
(10) RDAD
R159 220

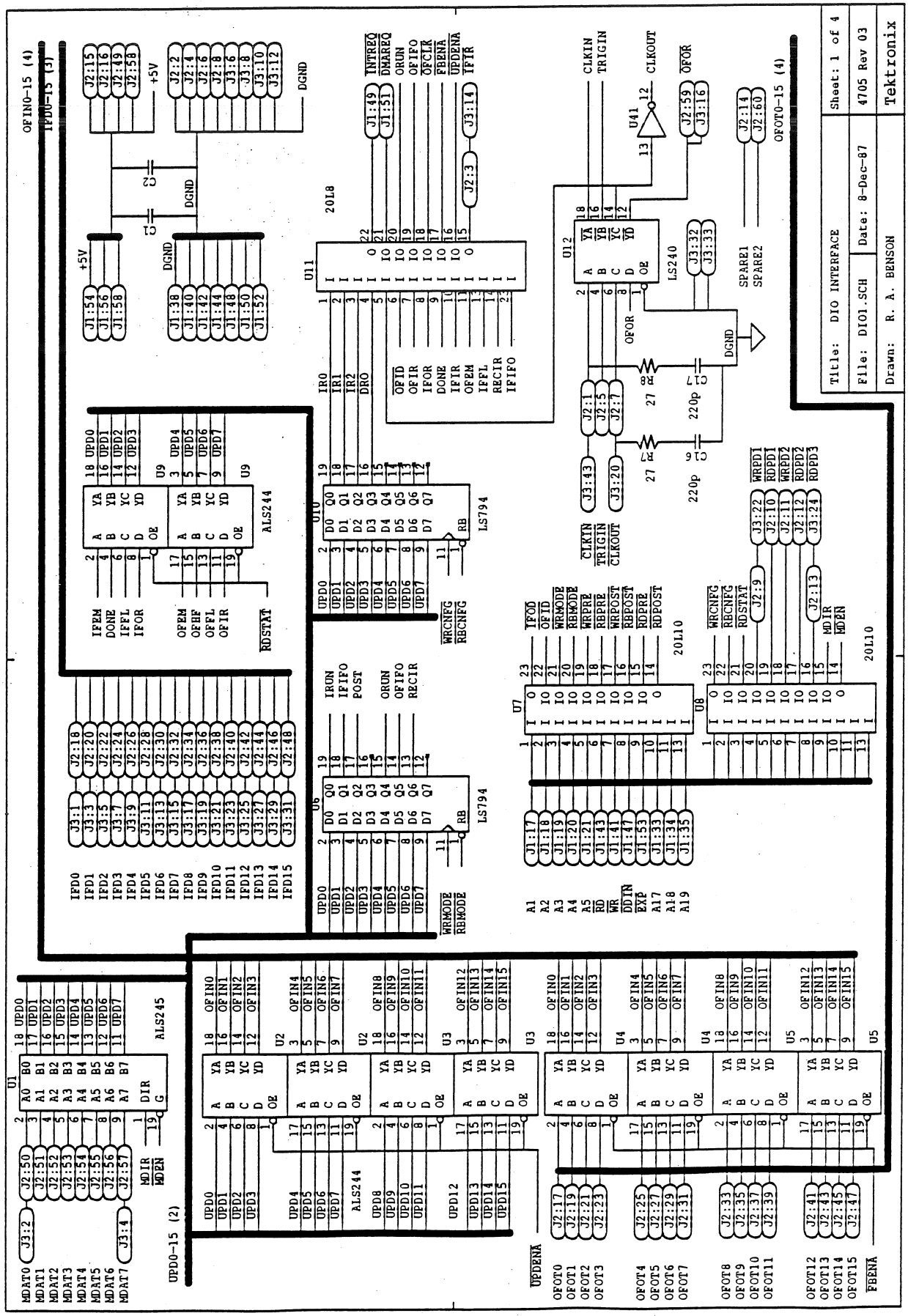

Title: DBE WCS & uC
File: DBE1.SCH
Drawn: R.A. Benson
Date: 8-Dec-87
Sheet: 1 of 5
4703 Rev 02
Tektronix
TMS32010
U10
U11
20L10
DBE1.PAL
IMS1420
U1
U2
U3
U4
U5
U6
U7
U8
U9
ALS158
ALS245
A1-4,13 (3)
DBE0-15 (2,3)
UPD0-15 (2,3,5)
SRUN (3)
RDCON (2)
CLRCON (2)
RDTP (2)
WROF (2)
RDCFG (3)
WRCFG (3)
PORT (3)
TDEN
TWE
KOSTAT (3)
CLKOUT (3)
TWE (3)
TDEN (3)
TMEN (3)
TINT (3)
TBIO (3)
DDIN
WCSDBE
WRWCS
CSWCS
RST2 (2,3)
-15A
+15A
+5A
+5D
AGND
DGND
0.1uF
20MHz
10pF
220
GR1

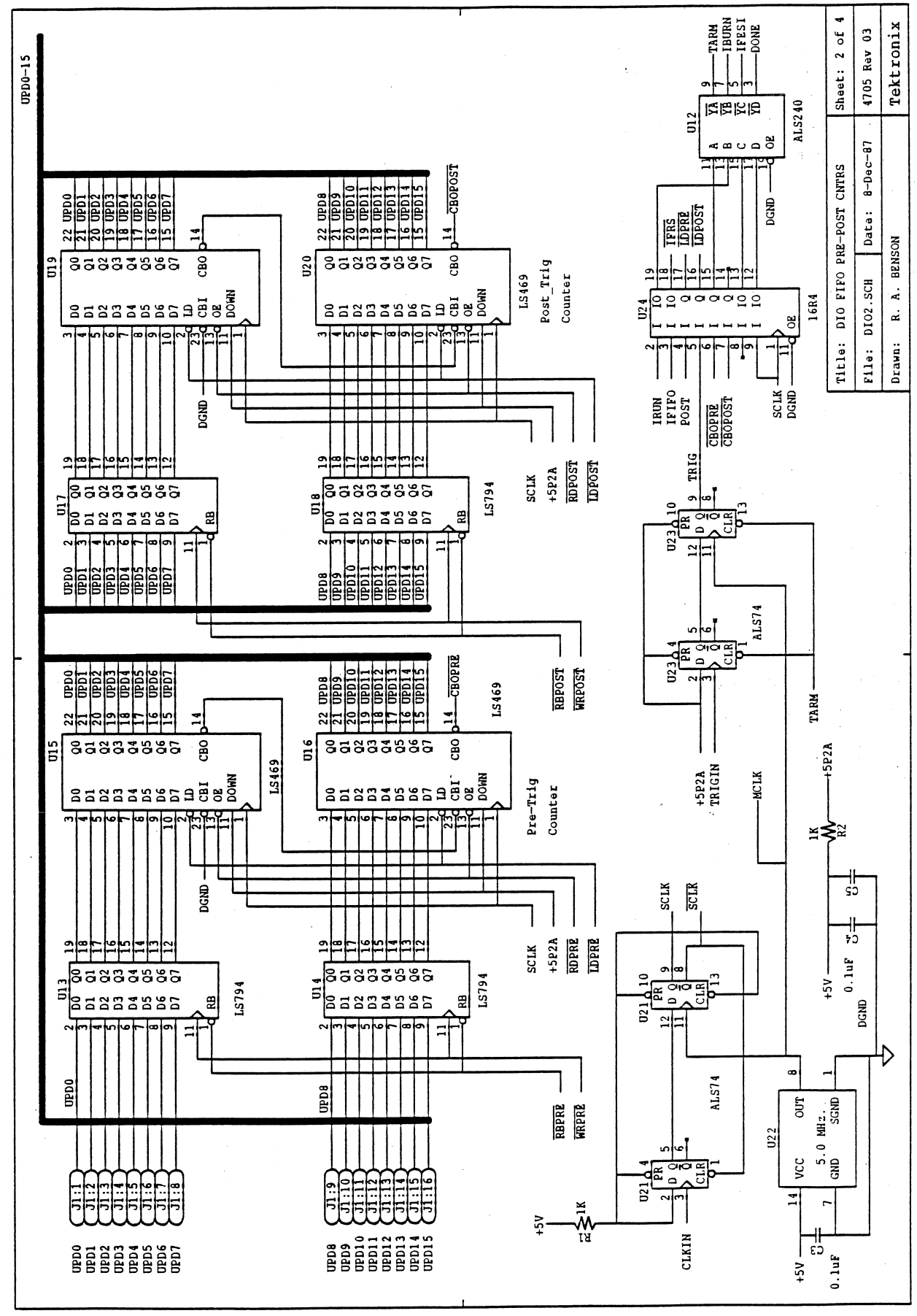

U18,U19 POWERED BY +5DAC AND AGND
Title: I-O FIFOS,COMM R, & DAC
File: DBE2.SCH
Date: 8-Dec-87
Drawn: R. A. BENSON
Sheet: 2 of 5
4703 Rev 02
Tektronix
DBE0-15 (1)
UPD0-15 (1)
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
U29
LS273
LS244
LS794
S225
DAC702
HA2515
ALS74
ALS20
ALS21
LS125
R1 1K
R2 2.94K
R4
R5
R6
R72 220
GRP1 100
C36 180pF
C41
C42
C43 4.7 uF
+5D
+5P2
+15P2
-15P2
+5DAC
+15A
+5A
-15A
AGND
DGND
LPFIN (4)
COMDAT (3)
IR1
IR2
IR3
IR4
IR5
IR6
OR1
OR2
OR3
OR4
OR5
OR6
OFIR (3)
OFOR (3)
DBEFR (1)
TFOR (3)
ODTAEN
ODEN
SRUN (3)
(3)CKOOF
(1) RST2
(3) SRUN
(3)CKOOF
(1) WROF
(1) RDCOM
(3) UWRCOM
(3) URDCOM
(1) CLRCOM
(3) UWRCOM
(3) UPD3
(3) URDSTAT
CKIIF (3)

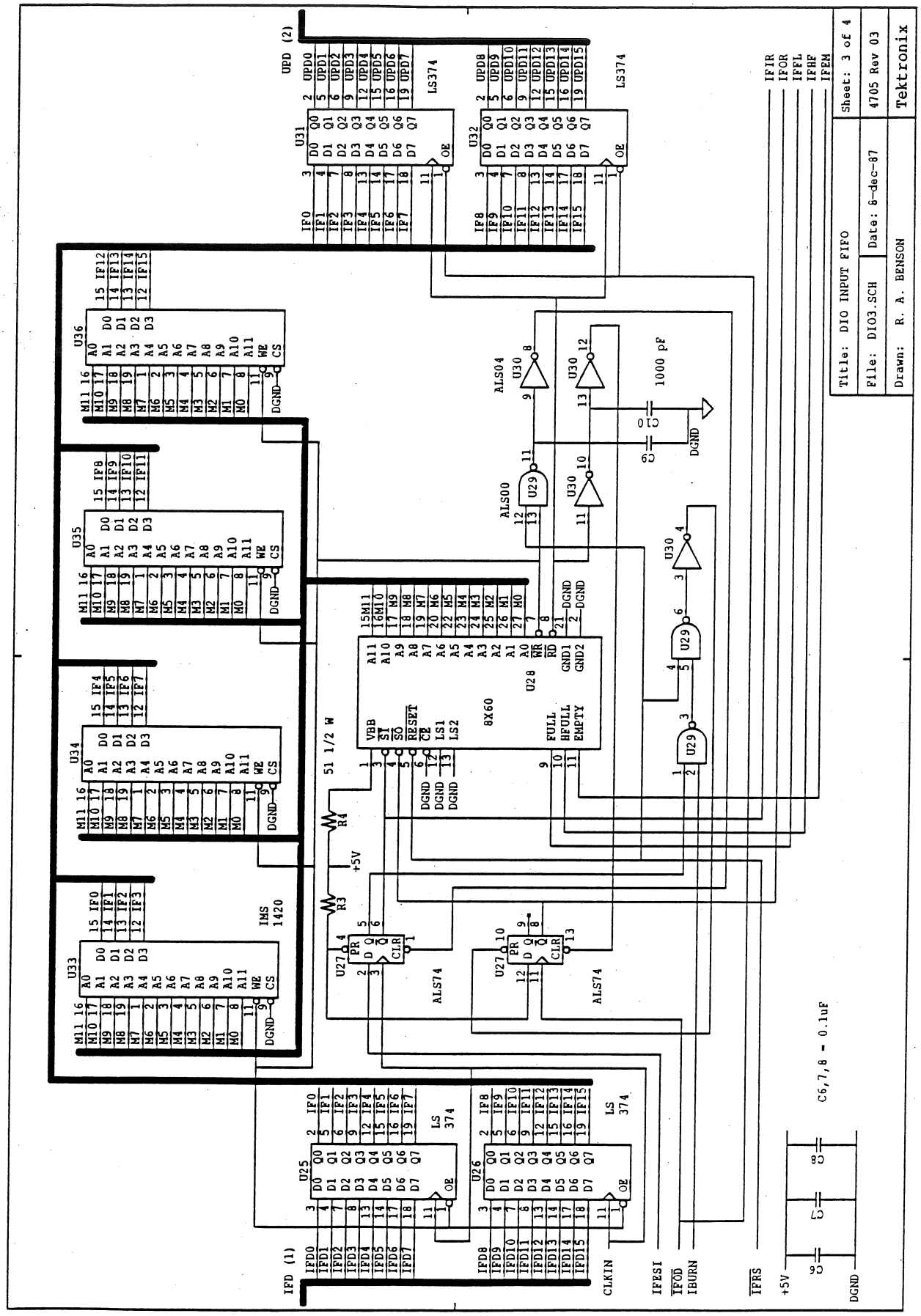

Title: DATA RAM & FLAG SELECT
Sheet: 3 of 5
File: DBE3.SCH
Date: 8-Dec-87
4703 Rev 02
Drawn: R. A. BENSON
Tektronix
FIFO OVLD DET
IMS1420
LS469
LS244
LS794
ALS74
LS125
LS00
S04
16L8
20L10
DBE2.PAL
DBE3.PAL
DBE4.PAL
+5P3
+5D
DGND
8MHZ
RDADR
CKOOF(2)
XSAMP
SRUN
OFOR
TBIO
TINT
RST2
CLKOUT
RUN
EXTSMP
OUTENA (5)
UPD0-7
DBE0-15

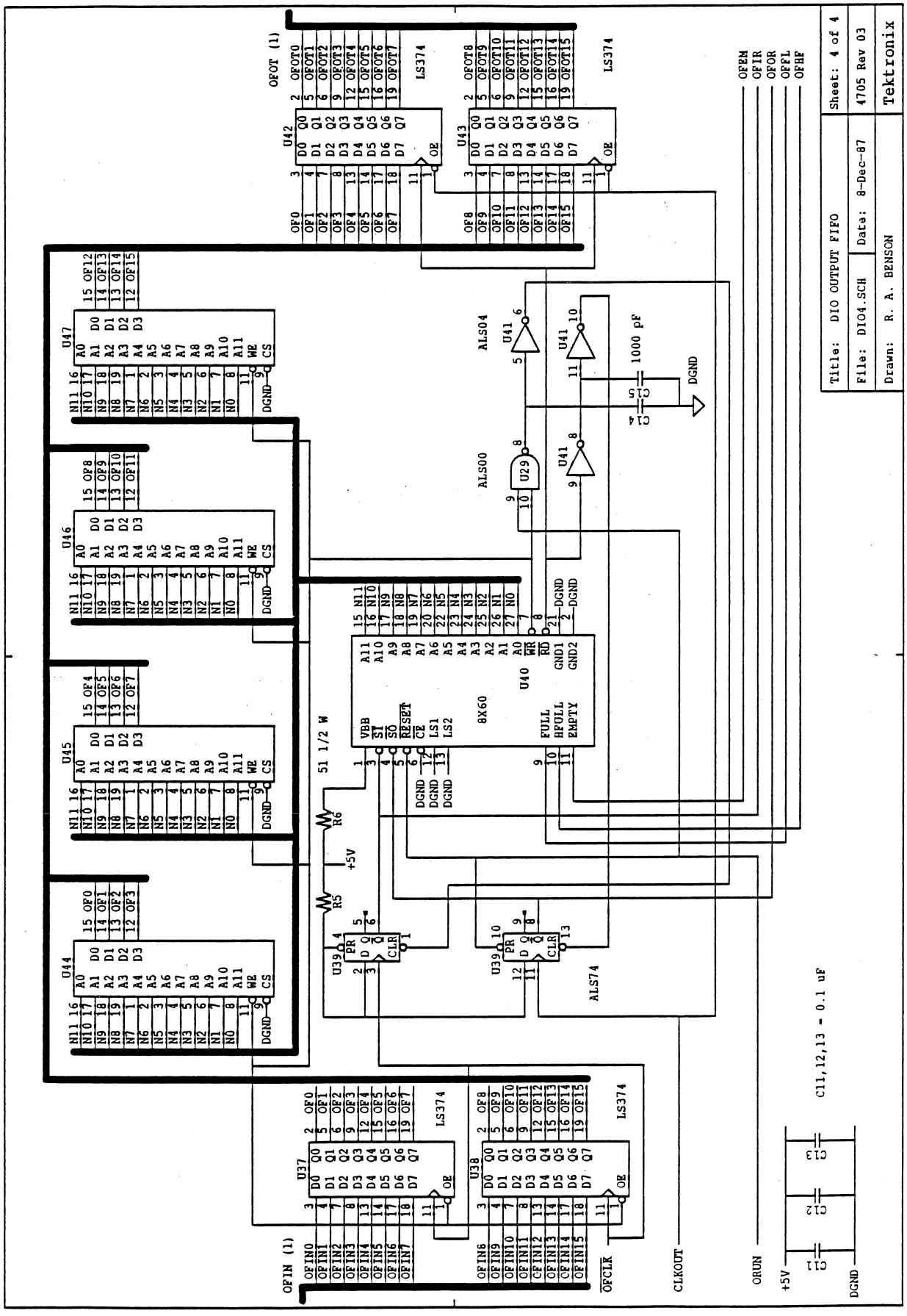

Title: DBE 20 KHz. LPF
Sheet: 4 of 5
File: DBE4.SCH
Date: 8-Dec-87
4703 Rev 02
Drawn: R.A.BENSON
Tektronix
LPFOUT (5)
LPFIN (2)
TP-20
TP-21
TP-22
TP-23
AGND
+15A
-15A
+VLA
-VLA
TL084C
R9 100.0K
R10 1.21K
R11 88.7
R12 2.00K
R13 2.00K
R14 2.15K
R15 2.37K
R16 499
R17 2.00K
R18 2.00K
R19 1.96K
R20 2.15K
R21 649
R22 2.00K
R23 2.00K
R24 1.82K
R25 2.15K
R26 332
R27 2.00K
R28 2.00K
R29 1.82K
R30 1.00K
R31 110.0K
R32 10
R33 10
C9 4.70 nF.
C10 4.70 nF.
C11 4.70 nF.
C12 4.70 nF.
C13 4.70 nF.
C14 4.70 nF.
C15 4.70 nF.
C16 4.70 nF.
C17 4.70 nF.
C18 4.70 nF.
C19 0.1uF
C20 10uF
U48
U49

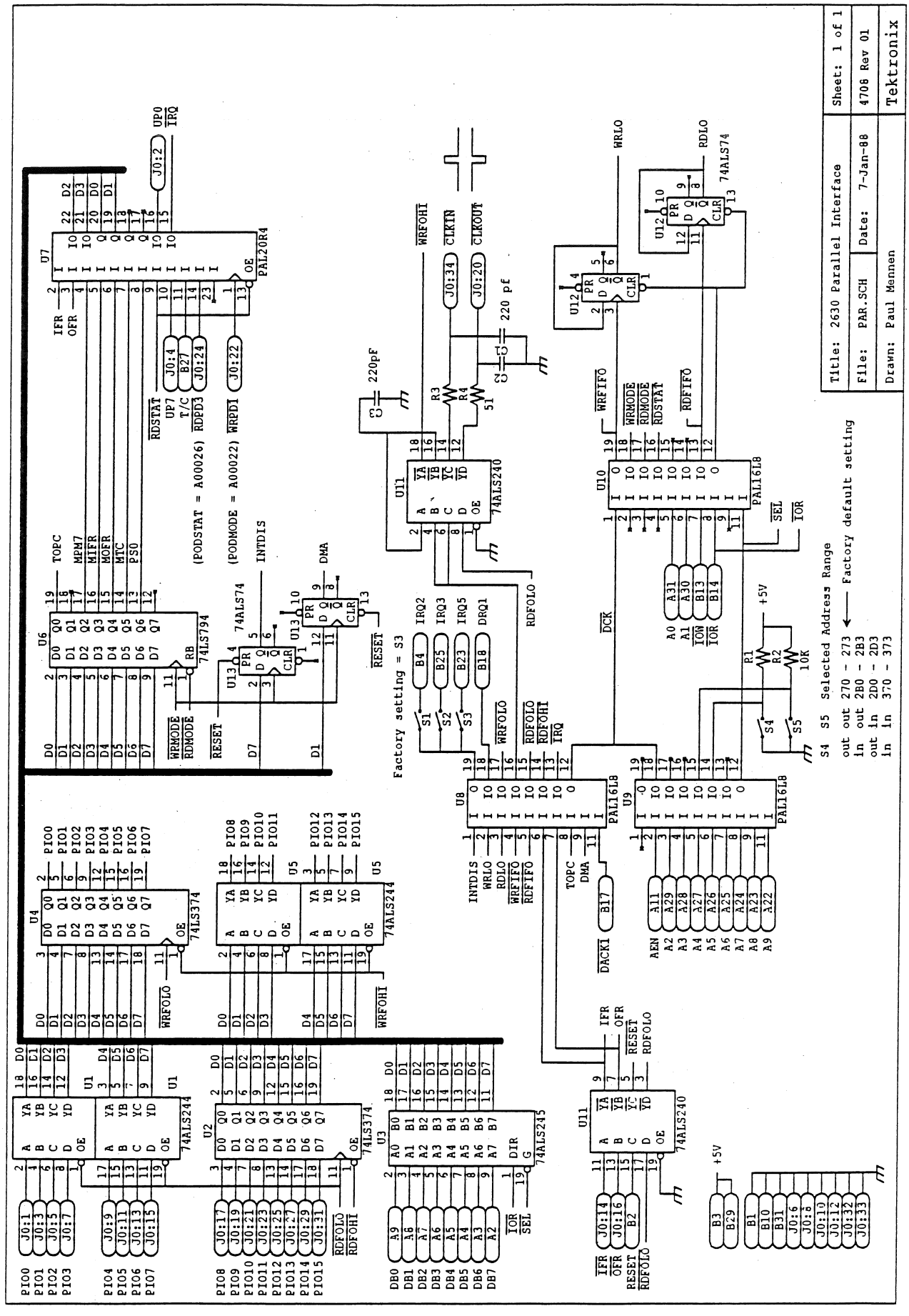

Title: MDAC'S AND OUTPUT BUFFER
Sheet: 5 of 5
File: DBE5.SCH
Date: 8-Dec-87
4703 Rev 02
Drawn: R. A. BENSON
Tektronix
U56 & U57 POWERED BY +5A & AGND
UPD0-15 (1)
(3)UWDAC
(3)UWATT
(3)UOUTENA
(4)LPFOUT +/- 1.5V
+/- 5
UNATOUT
PAOUT
DBEHI
DBELO
AD7545
DACUP8B
LH0002
MJE200
MJE210
HA2515
TL084C
LS373
LS00
S04
1N4148
1N4001
2N3905
2N3903

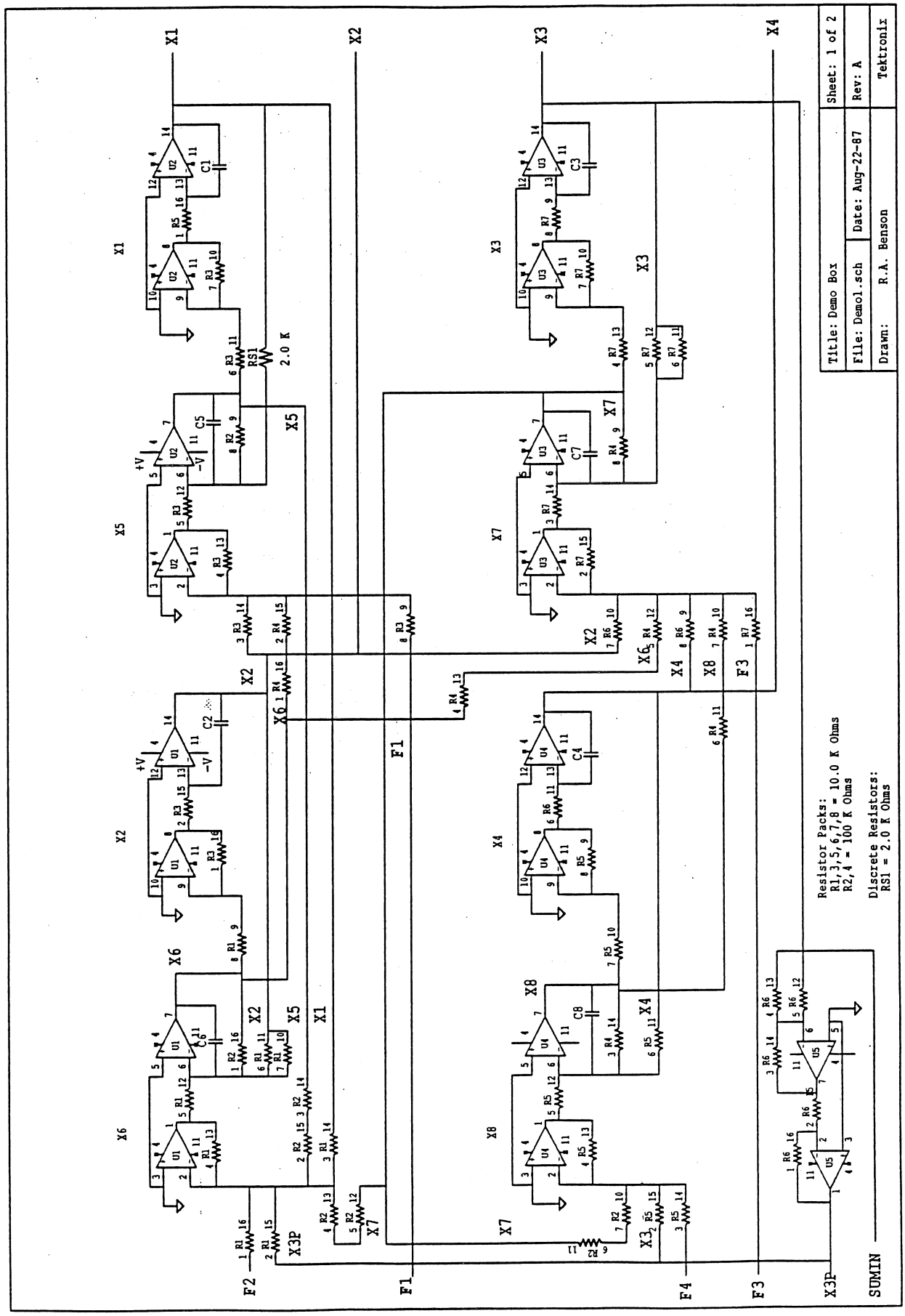

Title: DIO INTERFACE
Sheet: 1 of 4
File: DIO1.SCH
Date: 8-Dec-87
4705 Rev 03
Drawn: R. A. BENSON
Tektronix
ALS245
ALS244
LS794
LS240
20L10
2018
+5V
DGND
MDAT0
MDAT1
MDAT2
MDAT3
MDAT4
MDAT5
MDAT6
MDAT7
MDIR
MDEN
UPD0-15 (2)
IFD0
IFD1
IFD2
IFD3
IFD4
IFD5
IFD6
IFD7
IFD8
IFD9
IFD10
IFD11
IFD12
IFD13
IFD14
IFD15
OFIN0-15 (4)
IFD0-15 (3)
OFOT0-15 (4)
UPDENA
FBENA
WRMODE
RBMODE
WRCNFG
RBCNFG
RDSTAT
IRUN
IFIFO
POST
ORUN
OFIFO
RECIR
INTREQ
DMARQ
CLKIN
TRIGIN
CLKOUT
OFOR
SPARE1
SPARE2
WRPD1
RDPD1
WRPD2
RDPD2
RDPD3
MDIR
MDEN

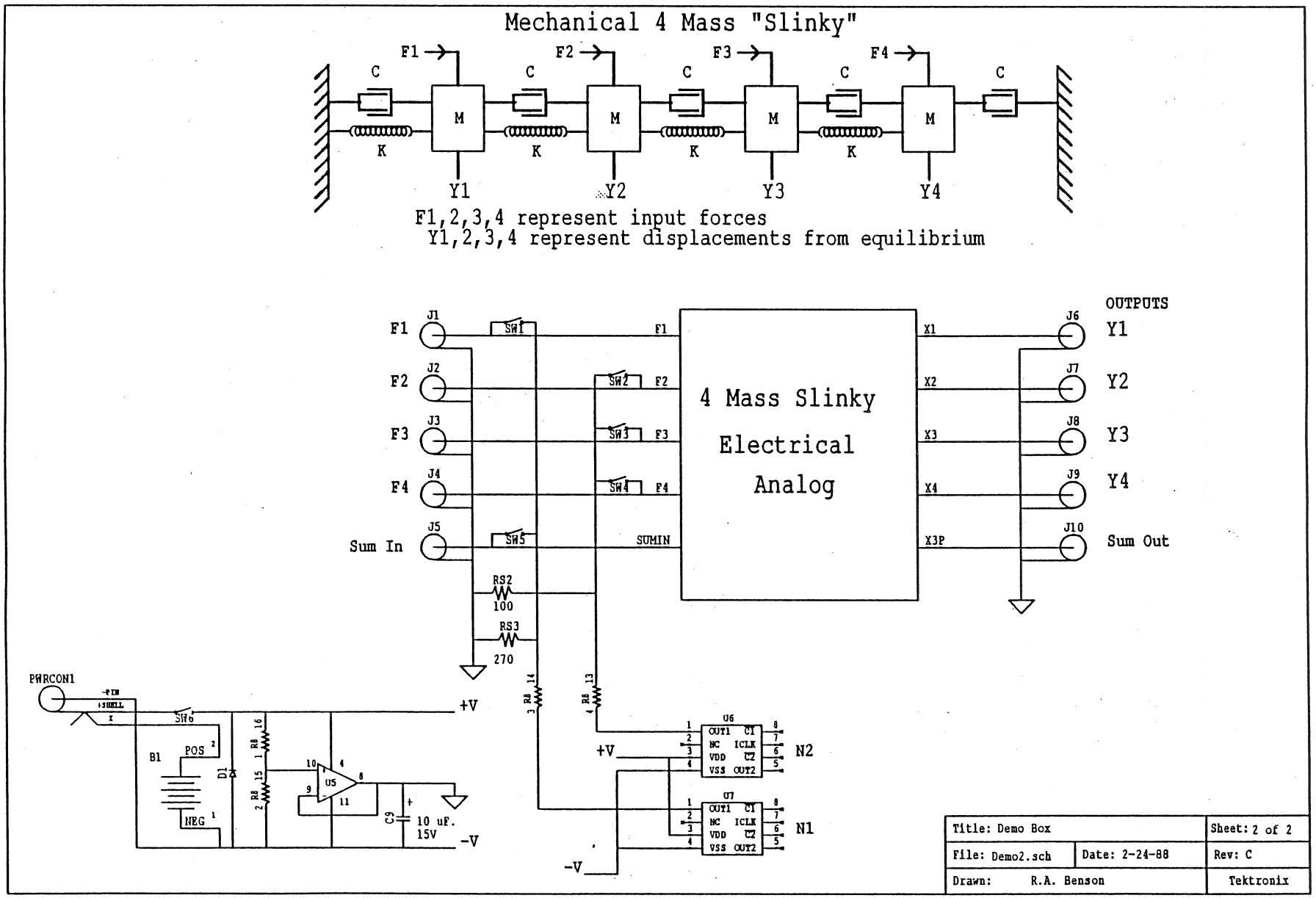

Title: DIO FIFO PRE-POST CNTRS
Sheet: 2 of 4
File: DIO2.SCH
Data: 8-Dec-87
4705 Rev 03
Drawn: R. A. BENSON
Tektronix
LS469
Post_Trig Counter
Pre-Trig Counter
LS794
ALS74
ALS240
16R4
5.0 MHz.
0.1uF
1K
DGND
SCLK
MCLK
TARM
IBURN
IFESI
DONE
IRUN
IFIFO
POST
TRIG
CLKIN
UPD0-15

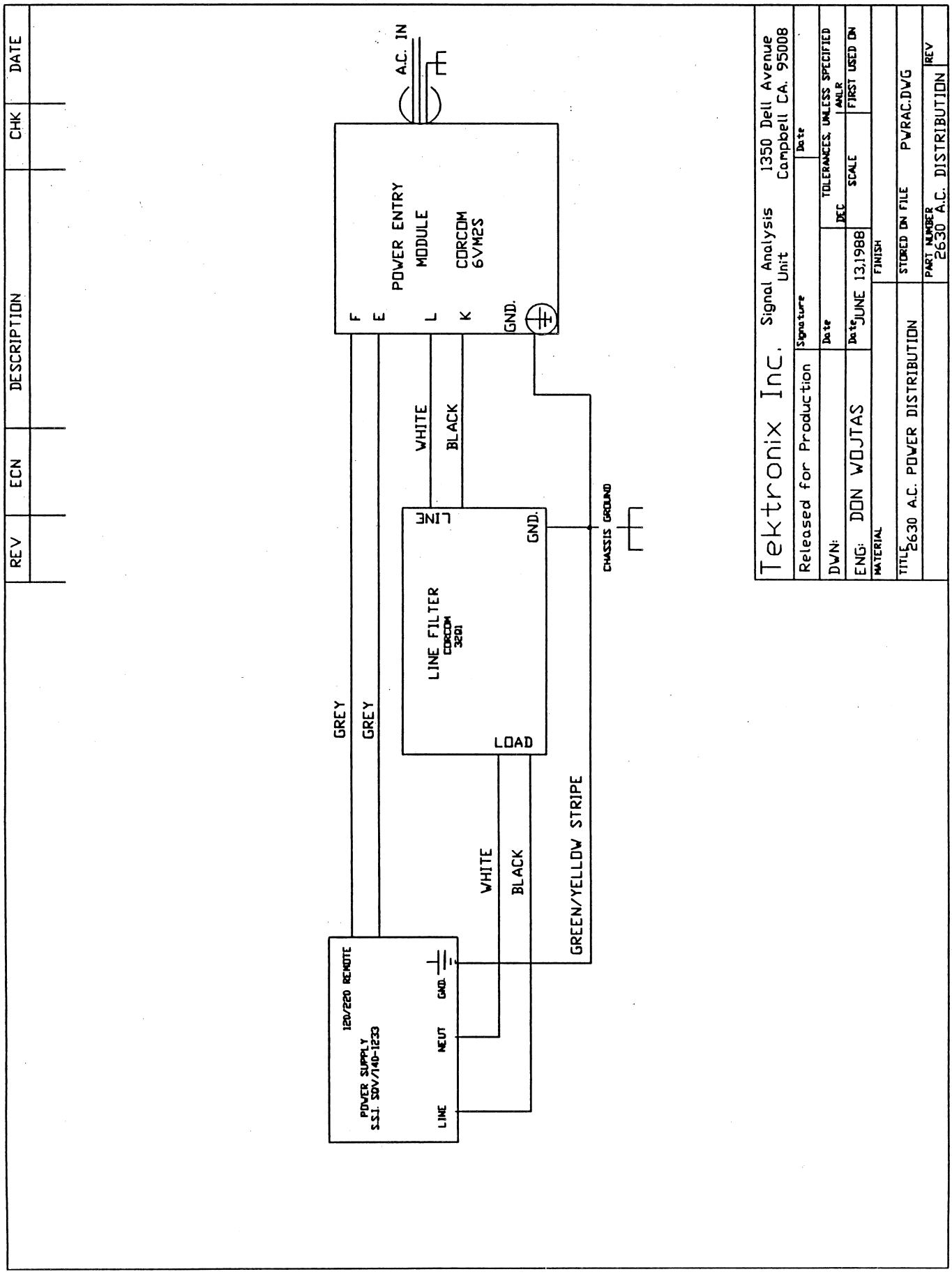

Title: DIO INPUT FIFO
Sheet: 3 of 4
File: DIO3.SCH
Date: 6-dec-87
4705 Rev 03
Drawn: R. A. BENSON
Tektronix
UPD (2)
IFD (1)
U31
U32
U33
U34
U35
U36
U25
U26
U27
U28
U29
U30
LS374
ALS74
ALS00
ALS04
IMS 1420
8X60
51 1/2 W
1000 pF
C6,7,8 - 0.1uF
+5V
DGND
CLKIN
IFESI
IFOD
IBURN
IFRS
IFIR
IFOR
IFFL
IFHF
IFEM

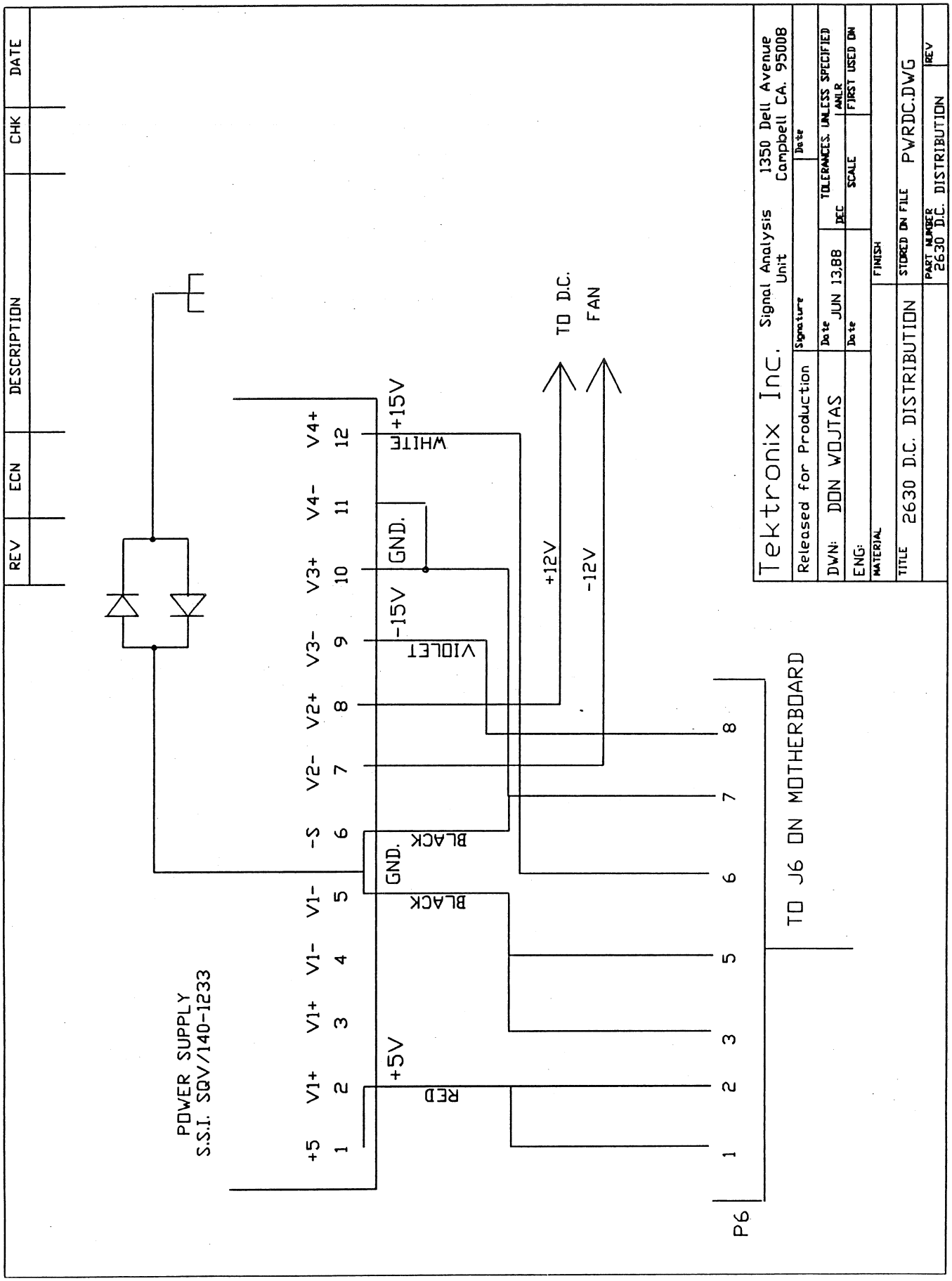

Title: DIO OUTPUT FIFO
Sheet: 4 of 4
File: DIO4.SCH
Date: 8-Dec-87
4705 Rev 03
Drawn: R. A. BENSON
Tektronix
OFOT (1)
OFIN (1)
LS374
ALS04
ALS00
ALS74
8X60
1000 pF
51 1/2 W
+5V
DGND
C11,12,13 - 0.1 uF
CLKOUT
ORUN
OFEM
OFIR
OFOR
OFFL
OFHF


Title: 2630 Parallel Interface
Sheet: 1 of 1
File: PAR.SCH
Date: 7-Jan-88
4708 Rev 01
Drawn: Paul Mennen
Tektronix
Factory setting = S3
S4 S5 Selected Address Range
out out 270 - 273 ← Factory default setting
In out 2B0 - 2B3
out In 2D0 - 2D3
In In 370 - 373
74ALS244
74LS374
74ALS245
74LS794
74ALS240
PAL16L8
PAL20R4
74LS74
74ALS374
220pF
220 pf
10K
+5V


Title: Demo Box
File: Demol.sch
Drawn: R.A. Benson
Date: Aug-22-87
Sheet: 1 of 2
Rev: A
Tektronix
Resistor Packs:
R1,3,5,6,7,8 = 10.0 K Ohms
R2,4 = 100 K Ohms
Discrete Resistors:
RS1 = 2.0 K Ohms
2.0 K
+V
-V
F1
F2
F3
F4
SUMIN
X3P


Mechanical 4 Mass "Slinky"
F1
F2
F3
F4
C
M
K
Y1
Y2
Y3
Y4
F1,2,3,4 represent input forces
Y1,2,3,4 represent displacements from equilibrium
OUTPUTS
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
SW1
SW2
SW3
SW4
SW5
SW6
Sum In
Sum Out
SUMIN
4 Mass Slinky
Electrical
Analog
X1
X2
X3
X4
X3P
Y1
Y2
Y3
Y4
RS2
100
RS3
270
PWRCON1
B1
POS
NEG
D1
U5
U6
U7
OUT1
NC
VDD
VSS
C1
ICLK
C2
OUT2
N1
N2
C9
10 uF.
15V
+V
-V
Title: Demo Box
Sheet: 2 of 2
File: Demo2.sch
Date: 2-24-88
Rev: C
Drawn: R.A. Benson
Tektronix


REV
ECN
DESCRIPTION
CHK
DATE
A.C. IN
POWER ENTRY MODULE
CORCOM 6VM2S
F
E
L
K
GND.
WHITE
BLACK
LINE FILTER
CORCOM 3201
LINE
GND.
LOAD
CHASSIS GROUND
GREY
GREY
WHITE
BLACK
GREEN/YELLOW STRIPE
POWER SUPPLY
S.S.I. SDV/140-1223
120/220 REMOTE
GND.
NEUT
LINE
Tektronix Inc.
Signal Analysis Unit
1350 Dell Avenue
Campbell CA. 95008
Released for Production
Signature
Date
DWN:
Date
TOLERANCES, UNLESS SPECIFIED
DEC
ANLR
ENG: DON WOJTAS
Date JUNE 13,1988
SCALE
FIRST USED ON
MATERIAL
FINISH
TITLE 2630 A.C. POWER DISTRIBUTION
STORED ON FILE
PWRAC.DVG
PART NUMBER
2630 A.C. DISTRIBUTION
REV


REV
ECN
DESCRIPTION
CHK
DATE
Tektronix Inc. Signal Analysis Unit 1350 Dell Avenue Campbell CA. 95008
Released for Production
DWN: DON WOJTAS
ENG:
MATERIAL
FINISH
TOLERANCES UNLESS SPECIFIED
SCALE
FIRST USED ON
STORED ON FILE PWRDC.DWG
TITLE 2630 D.C. DISTRIBUTION
PART NUMBER 2630 D.C. DISTRIBUTION
REV
POWER SUPPLY
S.S.I. SQV/140-1233
+5 V1+ V1+ V1- V1- V2- V2+ V3- V3+ V4- V4+
1 2 3 4 5 6 7 8 9 10 11 12
+5V
RED
GND.
BLACK
-S
-15V
VIOLET
GND.
+15V
WHITE
+12V
-12V
TO D.C.
FAN
P6
TO J6 ON MOTHERBOARD