## Service Manual

## Tektronix

## 2440 <br> Oscilloscope <br> Serial Number B014064 \& below <br> 070-6603-00

[^0]Please check for change information at the rear of this manual.

## Instrument Serial Numbers

Each instrument manufactured by Tektronix has a serial number on a panel insert or tag, or stamped on the chassis. The first letter in the serial number designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B010000 Tektronix, Inc., Beaverton, Oregon, USA<br>E200000 Tektronix United Kingdom, Ltd., London<br>J300000 Sony/Tektronix, Japan<br>H700000 Tektronix Holland, NV, Heerenveen, The Netherlands

Instruments manufactured for Tektronix by external vendors outside the United States are assigned a two digit alpha code to identify the country of manufacture (e.g., JP for Japan, HK for Hong Kong, IL for Israel, etc.).

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Tektronix warrants that this product will be free from defects in materials and workmanship for a period of three (3) years from the date of shipment. If any such product proves defective during this warranty period, Tektronix, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronixshall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronixservice center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

This warranty shall not apply to any defect, failure or damage caused by improper use or improper or inadequate maintenance and care. Tektronix shall not be obligated to furnish service under this warranty a) to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair or service the product; b) to repair damage resulting from improper use or connection to incompatible equipment; or c) to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

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## TABLE OF CONTENTS

Page
iii
LIST OF ILLUSTRATIONS
$v$
LIST OF TABLES
vi
OPERATORS SAFETY SUMMARY
vii
SERVICING SAFETY SUMMARY
Section 1 SPECIFICATION
INTRODUCTION ..... 1-1
PERFORMANCE CONDITIONS ..... 1-4
Section 2 PREPARATION FOR USE
SAFETY ..... 2-1
LINE VOLTAGE SELECTION ..... 2-1
LINE FUSE ..... 2-1
POWER CORD ..... 2-3
INSTRUMENT COOLING ..... 2-3
START-UP ..... 2-3
POWER-DOWN ..... 2-4
REPACKAGING FOR SHIPMENT ..... 2-4
Section 3 THEORY OF OPERATION
SECTION ORGANIZATION. ..... 3-1
INTEGRATED CIRCUIT DESCRIPTIONS ..... 3-1
SIMPLIFIED BLOCK DIAGRAM DESCRIPTION ..... 3-2
DETAILED BLOCK DIAGRAM DESCRIPTION ..... 3-8
INTRODUCTION ..... 3-8
INPUT SIGNAL CONDITIONING
AND ANALOG SAMPLING ..... 3-8
ACQUISITION PROCESS
AND CONTROL ..... 3-10
DATA CLOCKING TO
ACQUISITION MEMORY ..... 3-10
ANALOG DATA CONDITIONING
AND A/D CONVERSION ..... 3-11
ACQUISITION PROCESSING
AND DISPLAY. ..... 3-12
DETAILED CIRCUIT
DESCRIPTION ..... 3-15
SYSTEM PROCESSOR ..... 3-15
WAVEFORM PROCESSOR
SYSTEM ..... 3-22
Page
FRONT PANEL PROCESSOR. ..... 3-28
FRONT PANEL CONTROLS. ..... 3-30
SYSTEM DAC AND ACQUISITION CONTROL REGISTERS. ..... 3-31
SYSTEM DAC (cont) AND
AUXILIARY FRONT PANEL ..... 3-33
SYSTEM CLOCKS ..... 3-35
TIME BASE CONTROLLER AND ACQUISITION MEMORY ..... 3-39
ATTENUATORS AND PREAMPLIFIERS ..... 3-43
PEAK DETECTORS AND ..... 3-45
TRIGGERS AND PHASE CLOCKS ..... 3-51
JITTER CORRECTION RAMPS ..... 3-56
TRIGGER HOLDOFF, JITTER COUNTERS, AND CALIBRATOR ..... 3-58
CCD OUTPUT ..... 3-61
A/D CONVERTER AND
ACQUISITION LATCHES ..... 3-62
DISPLAY AND ATTRIBUTES MEMORY ..... 3-63
DISPLAY CONTROL ..... 3-66
DISPLAY OUTPUT ..... 3-73
HIGH VOLTAGE POWER
SUPPLY AND CRT ..... 3-75
SYSTEM I/O ..... 3-80
VIDEO OPTION ..... 3-84
LOW VOLTAGE POWER SUPPLY ..... 3-92
LOW VOLTAGE REGULATORS ..... 3-98
Section 4 PERFORMANCE CHECK AND FUNCTIONAL VERIFICATION PROCEDURE
INTRODUCTION ..... 4-1
PREPARATION ..... 4-1
INITIAL SETUP ..... 4-4
VERTICAL SYSTEM ..... 4-6
TRIGGERING SYSTEMS ..... 4-18
HORIZONTAL SYSTEM ..... 4-26
ADDITIONAL VERIFICATIONS AND CHECKS ..... 4-29

## TABLE OF CONTENTS (cont)

Page
Section 5 ADJUSTMENT PROCEDURE INTRODUCTION ..... 5-1
CALIBRATION SEQUENCE AND PARTIAL PROCEDURES ..... 5-1
WARM-UP TIME REQUIREMENT ..... 5-1
PRESERVATION OF
INSTRUMENT
CALIBRATION ..... 5-2
INTERNAL ADJUSTMENTS ..... 5-3
SELF CALIBRATION ..... 5-19
EXTERNAL CALIBRATION ..... 5-20
Section 6 MAINTENANCE
INSTRUMENT CALIBRATION ..... 6-1
NATIONAL BUREAU OF
STANDARDS TRACEABILITY ..... 6-2
VOIDING CALIBRATION ..... $6-2$
STATIC-SENSITIVE COMPONENTS ..... 6-3
PREVENTIVE MAINTENANCE ..... 6-4
introduction ..... 6-4
general care ..... 6-4
INSPECTION AND CLEANING ..... 6-4
LUBRICATION ..... 6-6
SEMICONDUCTOR CHECKS ..... 6-6
PERIODIC READJUSTMENT ..... 6-6
TROUBLESHOOTING ..... 6-7
INTRODUCTION ..... 6-7
TROUBLESHOOTING AIDS ..... 6-7
TROUBLESHOOTING EQUIPMENT ..... 6-9
TROUBLESHOOTING TECHNIQUES ..... 6-9
CORRECTIVE MAINTENANCE ..... 6-11
INTRODUCTION ..... 6-11
MAINTENANCE PRECAUTIONS ..... 6-11
OBTAINING REPLACEMENT PARTS ..... 6-11
MAINTENANCE AIDS ..... 6-12
INTERCONNECTIONS ..... 6-12
TRANSISTORS AND
INTEGRATED CIRCUITS ..... 6-12
SOLDERING TECHNIQUES ..... 6-14
REMOVAL AND REPLACEMENT procedure ..... 6-15
Page
DIAGNOSTICS AND INTERNAL CALIBRATION ROUTINES ..... 6-25
INTRODUCTION ..... 6-25
OVERVIEW ..... 6-25
CALIBRATION ROUTINES ..... 6-25
DIAGNOSTIC ROUTINES ..... 6-27
diagnostics operation VIA THE GPIB INTERFACE. ..... 6-34
DIAGNOSTIC PROCEDURES ..... 6-35
Section 7 OPTIONS AND ACCESSORIES
OPTIONS DESCRIPTION ..... 7-1
OPTIONS AT-A5-INTERNATIONAL POWER CORDS ..... $7-1$
OPTION 1R-RACKMOUNTED 2440 ..... $7-1$
OPTION 03-WORD
RECOGNIZER PROBE ..... 7-2
OPTION 05-VIDEO OPTION ..... 7-2
OPTION 11-PROBE POWER ..... 7-2
STANDARD ACCESSORIES ..... 7-2
RÁCKMOUNTING ACCESSORIES ..... 7-2
OPTIONAL ACCESSORIES ..... 7-2
Section 8 REPLACEABLE ELECTRICAL PARTS
Section 9 DIAGRAMS
Section 10 REPLACEABLE MECHANICAL PARTS
CHANGE INFORMATION
Diagnostic and Troubleshooting Information:
Diagnostics ..... 6-25
Diagnostic Operation ..... 6-30
Diagnostic Procedures. ..... 6-32
2440 Troubleshooting Procedures Table. ..... 6-35
Video Option Troubleshooting Table ..... 6-99
Troubleshooting Charts ..... Section 9

## LIST OF ILLUSTRATIONS

Figure Page
The 2440 Digital Oscilloscope ..... viii
1-1 Dimensional drawing ..... 1-24
2-1 LINE VOLTAGE SELECTOR, line fuse, and power cord receptacle ..... 2-1
3-1 2440 simplified block diagram ..... 3-3
3-2 Simplified Memory Map of the 2440 ..... 3-18
3-3 System Clock waveforms ..... 3-37
3-4 Simplified Peak Detector block diagram. ..... 3-47
3-5 Simplified CCD architecture ..... 3-49
3-6 Trigger Logic Array Control Data Byte ..... 3-53
3-7 Jitter correction waveforms. ..... 3-57
3-8 Readout State Machine flow chart ..... 3-71
3-9 Vertical Vector Generator ..... 3-73
3-10 DC Restorer ..... 3-78
3-11 GPIB data flow diagram. ..... 3-81
3-12 GPIB three-wire handshake state diagram ..... 3-82
3-13 Video Option waveforms ..... 3-87
3-14 Video Option field-sync identification ..... 3-88
3-15 PWM Regulator and Inverter ..... 3-94
3-16 PWM switching waveforms. ..... 3-96
5-1 Adjustment locations for Displays 4 through 6 ..... 5-4
5-2 Display 5-Vertical and Horizontal Gain, Offset, and Vector Compensation adjustment pattern ..... 5-5
5-3 Display 6-Integrator Time adjustment pattern ..... 5-6
5-4 (SN B010250 \& Above) CH 1 and CH 2 CCD Clock Adjustments (shown centered, as after doing part b) ..... 5-7
5-4 (SN B010249 \& Below) CH 1 and CH 2 CCD Clock Adjustments (shown centered, as after doing part b) ..... 5-8
5-5 CCD counts display and CM adjustment menu ..... 5-8
5-6 CCD sides 1-4 for CH 1 before L-clock adjustment ..... 5-12
5-7 Sides 1 and 3 before adjustment of L1S and after ..... 5-13
5-8 CH 1 with L-clocks correctly adjusted, but with stray samples ..... 5-14
5-9 Display for adjusting CCD A and T clocks ..... 5-15
5-10 Typical CH 1 and CH 2 displays after clock adjustment ..... 5-16
5-11 Checking sample dispersion ..... 5-17
5-12 Input and output (after adjustment) waveforms ..... 5-20
6-1 Multipin connector ..... 6-8
6-2 Circuit board Location ..... 6-16
6-3 Installation sequence for installing the crt frame screws ..... 6-23
6-4 Trigger LED binary coding for diagnostic tests ..... 6-29
6-5 Main EXT DIAG Menu. ..... 6-30
6-6 Initial troubleshooting chart ..... 6-36
6-7 Mux Test waveforms ..... 6-41

## LIST OF ILLUSTRATIONS (cont)

Page
6-8 Typical Register test waveforms ..... 6-55
6-9 Front Panel $\mu \mathrm{P}$ diagnostics test. ..... 6-79
6-10 System $\mu \mathrm{P}$ data bit D 7 in the Bus Isolate mode. ..... 6-102
9-1 Color codes for resistors and capacitors.
9-2 Semiconductor lead configurations.
9-3 Locating components on schematic diagrams and circuit board illustrations.
9-4a Detailed 2440 Block Diagram.
9-4b Detailed 2440 Block Diagram (cont).
9-5 A12_Processor Board.
9-6 A13—Side Board.
9-7 A14_Front Panel Board.
9-8 A10—Main Board.
9-9 A30, A31, A32 and A33-Gain Cell Boards.
9-10 A11—Timebase/Display Board.
9-11 A17-High Voltage Board.
9-12 A16-Low Voltage Power Supply Board.

## LIST OF TABLES

Table Page
1-1 Electrical Characteristics ..... 1-5
1-2 Environmental Characteristics ..... 1-19
1-3 Mechanical Characteristics ..... 1-21
1-4 Option 05 (TV Trigger) Electrical Characteristics ..... 1-22
2-1 Voltage, Fuse, and Power-Cord Data ..... 2-2
3-1 Host Memory-Mapped I/O ..... 3-20
3-2 Processor Control Register Functions ..... 3-21
3-3 Processor Miscellaneous Register (PMREG) Output Functions ..... 3-22
3-4 Waveform $\mu \mathrm{P}$ Address Decoding. ..... 3-27
3-5 Trigger Logic Array Addresses (6080h-6087h) ..... 3-52
3-6 Phase Clock Array Control Lines (CC3 through CC0). ..... 3-55
3-7 Holdoff Delay Range for Current Source vs Charging Capacitor Combinations ..... 3-59
3-8 Side Board Address Decoding ..... 3-60
4-1 Test Equipment Required ..... 4-2
4-2 Accuracy Limits CH 1 and CH 2 CURSOR VOLTS Readout and A and B TRIGGER LEVEL Readouts ..... 4-10
4-3 Minimum Display Level for CH 1 or CH 2 Triggering ..... 4-19
4-4 Minimum Signal Level for EXT1 or EXT2 Triggering ..... 4-21
6-1 Relative Susceptibility to Static-Discharge Damage ..... 6-3
6-2 External Inspection Check List. ..... 6-5
6-3 Internal Inspection Check List ..... 6-6
6-4 Power Supply Voltage and Ripple Limits ..... 6-10
6-5 Maintenance Aids ..... 6-13
6-6 $\quad 2440$ Troubleshooting Procedures ..... 6-37
6-7 Video Option Troubleshooting ..... 6-104
6-8 INIT PANEL States. ..... 6-108

## OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply and do not appear in this summary.

## Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

## Terms as Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the markings, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

## Symbols in This Manual

This symbol indicates where applicable cautionary or other information is to be found. For maximum input voltage see Table 1-1.

## Symbols as Marked on Equipment

4 DANGER - High voltage.

Protective gound (earth) terminal.

ATTENTION - Refer to manual.

## Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

## Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before making any connections to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

## Danger Arising from Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulated) can render an electric shock.

## Use the Proper Power Cord

Use only the power cord and connector specified for the instrument.

## Use the Proper Fuse

To avoid fire hazard, use only the fuse specified in the instrument parts list. A replacement fuse must meet the type, voltage rating, and current rating specifications for the fuse that it replaces.

## Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this instrument in an atmosphere of explosive gasses.

## Do Not Remove Covers or Panels

To avoid personal injury, the instrument covers or panels should only be removed by qualified service personnel. Do not operate the instrument without covers and panels properly installed.

# SERVICING SAFETY SUMMARY <br> FOR QUALIFIED SERVICE PERSONNEL ONLY 

## Refer also to the preceding Operators Safety Summary.

## Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

## Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections or components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

## Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms bwetween the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding connector in the power cord is essential for safe operation.

## SPECIFICATION

## INTRODUCTION

## VERTICAL SYSTEM

The TEKTRONIX 2440 Digital Oscilloscope is a portable, dual-channel instrument with a maximum digitizing rate of 500 Megasamples per second. The scope is capable of simultaneous acquisition of Channel 1 and Channel 2 input signals. It has a real-time useful storage bandwidth of 200 MHz for single-event acquisitions, with an equivalent-time bandwidth of 300 MHz when repetitive acquisitions are acquired. Since both channels are acquired simultaneously, the XY display is available to full bandwidth. Options include a Word Recognition Probe, Video signal triggering, Probe Power, and Rackmounting.

The instrument is microprocessor controlled and menu driven, displaying at the top of the screen alphanumeric CRT readouts of the vertical and horizontal scale factors, trigger levels, trigger source, and cursor measurements. Menus, displayed at the bottom of the CRT display, are used by the operator to select the operating mode.

A user makes decisions as to what operation and mode setup the instrument must have to make the measurement wanted and then selects the proper functions using a combination of front-panel buttons and the displayed menu.

Five menu buttons mounted on the CRT bezel are used to make selections from the entry choices displayed. The top line of the menu display usually contains the menu title, and the bottom line labels the buttons with the control functions they select. The selection is made (indicated by an underscoring of the menu label in the display) when the bezel button below the selected function is pressed. The menus, system operating modes, and auxiliary functions are described in Section 5, "Controls, Connectors, and Indicators" of the Operators manual included with this instrument, and the "Getting Acquainted" procedure in Section 1 of that manual familiarizes the user with menu operation.

The two vertical channels have calibrated deflection factors from 2 mV to 5 V per division in a 1-2-5 sequence of 14 steps. Use of coded probes having attenuation factors of $1 \mathrm{X}, 10 \mathrm{X}, 100 \mathrm{X}$, and 1000X extends the minimum sensitivity to $5,000 \mathrm{~V}$ per division (with the 1000 X probe) and the maximum sensitivity to $200 \mu \mathrm{~V}$ per division (using a 1 X probe in SAVE or AVERAGE expanded mode).

VOLTS/DIV readouts are automatically switched to display a correct scale factor when properly coded probes are attached. Each channel can be separately inverted. ADD and MULT are display functions provided by the processor system.

In SAVE mode, the waveforms may be both horizontally and vertically repositioned, expanded horizontally and vertically, added to each other, or multiplied together for either XY or YT displays.

## HORIZONTAL SYSTEM

Horizontal display modes of A, A INTEN, and B Delayed are available. The time base has 29 calibrated SEC/DIV settings in a 1-2-5 sequence from 2 ns per division to 5 s per division. An External Clock mode is provided that accepts clocking signals from 1 MHz to 100 MHz .

The B Trace and the intensified zone on the A INTEN Trace may be delayed by time with respect to the $A$ trigger, and a DELAY by EVENTS function permits the A display to be delayed by a selected number of B Trigger events. In the case of DELAY by EVENTS, the B Trigger SOURCE, COUPLING, SLOPE, and LEVEL controls define the nature of the signal needed to produce events triggering. The number of events required to satisfy the
delay may be set from 1 to 65,536 , with a resolution of one event. The DELTA DELAY feature produces two independently settable delayed $B$ Traces in DELAY by TIME.

## TRIGGER SYSTEM

The trigger system of the scope provides many features for selecting and processing a signal used in triggering the acquisition system. The conventional features of SOURCE selection, Trigger LEVEL control, Trigger SLOPE, Trigger MODE, and CPLG (coupling) include enhancements not normally found in a conventional oscilloscope.

The choices of VERT, CH1 or CH2, EXT1 or EXT2, LINE, and $A^{*} B$ or WORD (16-bit data word recognition) are available as SOURCE selections for triggering A Horizontal Mode acquisitions. These sources for trigger signals provide a wide range of applications involving specialized triggering requirements. Except for $A^{*} B$ (A AND B) and LINE (power-source frequency), the same Trigger SOURCE selections are available for triggering B acquisitions. The selected trigger signal is conditioned by the choice of input CPLG (coupling). These coupling selections are AC, DC, HF REF, LF REJ, and NOISE REJ. LEVEL control provides a settable amplitude (with CRT readout) at which triggering will occur, and SLOPE control determines on which slope of the triggering signal (plus or minus) the acquisition is triggered.

Trigger MODE choices are AUTO LEVEL, AUTO, NORM, and SINGLE SEQ (single sequence), for the A and A INTENSIFIED Modes, and Triggerable After Delay and Runs After Delay, for the B Mode. AUTO LEVEL provides for automatic leveling on the applied trigger signal. AUTO MODE produces an auto trigger in the event a trigger signal is either not received or not within the limits needed to produce a triggering event. When triggering conditions are met, a normal triggered display results. At SEC/DIV settings of 100 ms per division and longer, the AUTO MODE switches to ROLL. In ROLL MODE, the display is continually updated and trigger signals are disregarded.

NORM (normal) trigger MODE requires that all triggering requirements are met before an acquisition will take place. SINGLE SEQ (single sequence) MODE is a variation of the conventional single-shot displays found on many previous oscilloscopes. In SINGLE SEQ, a single complete acquisition is done on all called-up VERTICAL MODES. Since an acquisition depends on the acquisition mode in effect, many of the scope operating features are altered in SINGLE SEQ. A complete description of this
mode is discussed in "Controls, Connectors, and Indicators" in Section 5 of the Operators manual.

The user has a choice of trigger points within the acquired waveform record by selecting the amount of pretrigger data displayed. The trigger location in the record is selectable from a choice of five pretrigger lengths beginning at one-eighth of the record length and increasing to seven-eighths of the record length. A record trigger position is independently selectable for both A and B acquisitions. Additional trigger positions in the record are selectable via the GPIB interface commands.

## CURSOR MEASUREMENTS

Time and Voltage cursors are provided for making parametric measurements on the displayed waveforms. Time may be measured either between the cursor positions (DELTA TIME) or between a selected cursor and the trigger point of an acquired waveform (ABSOLUTE). Time cursor readouts are scaled in seconds, degrees, or percentage values. The 1/TIME cursors may be scaled in hertz (Hz), degrees, or percentage.

Voltage cursor measurements on a waveform display can be selected to read either the voltage difference between the cursor positions or the absolute voltage position of a selected cursor with respect to ground. The volts measurement readouts may be scaled in units of volts, decibels (dB), or percent. The Voltage cursors and Time cursors may also be coupled to track together (V@T and SLOPE) and assigned to a particular waveform for ease in making peak-to-peak and slope waveform measurements. The units for V@T may be volts, percent, or dB; SLOPE may have units of slope (VOLTS/SEC), percent (VOLTS/VOLT), or dB.

## WAVEFORM ACQUISITION

Waveforms may be acquired in NORMAL, ENVELOPE, or AVG (Average) acquisition modes; the mode chosen depends on the measurement requirements. NORMAL mode continuously acquires and displays successive acquisitions producing a "live" waveform display similar to that seen with an analog oscilloscope. AVG (averaging) mode averages successive acquisitions of a waveform resulting in an improved signal-to-noise ratio of the displayed waveform. Low-amplitude signals masked by noise become easily visible for making measurements and analysis by averaging from 2 to 256 acquisitions for removing uncorrelated noise. ENVELOPE mode saves the
maximum and minimum data-point values over a selected number of acquisitions from 1 to 256 plus CONT (continuous). The display presents a visual image of the amount of change (envelope) that occurs to a waveshape during the accumulated acquisitions. Frequency, phase, amplitude, and position changes are easily identified when acquiring in ENVELOPE mode. The glitch-catching capability of ENVELOPE mode can capture single-event pulses as narrow as 2 ns at the slowest SEC/DIV setting of 5 seconds per division.

For all three acquisition modes, equivalent-time sampling extends the Useful Storage Bandwidth to 300 MHz if the signal is repetitive and REPET mode is turned on. At $50 \mathrm{~ns} /$ DIV and faster, randomly-acquired data points (or samples) taken from successive acquisitions of a periodic signal are used to fill the complete record (1024 data points) of the signal waveform display. Depending on the SEC/DIV setting, as few as 10 data points (at $2 \mathrm{~ns} /$ DIV) or as many as 512 data points (at $50 \mathrm{~ns} / \mathrm{DIV}$ ) may be obtained on each triggered acquisition. Sampling of successive acquisitions continues until a predetermined number of data points are acquired and any remaining points in the record are determined by interpolating between the acquired points. (The predetermined number includes at least enough data point to meet the Useful Storage Bandwidth of 300 MHz specified for REPET mode.) These interpolated points are replaced by randomly-acquired data points as they become available from successive acquisitions.

Horizontally, the record length of acquired waveforms is 1024 data points ( $512 \mathrm{max} / \mathrm{min}$ pairs in ENVELOPE mode), of which 500 make up a one-screen display ( 50 data points per division for 10 divisions). The entire record may be viewed by using the Horizontal POSITION control to position any portion of the record within the viewing area.

## STORAGE AND I/O

Acquired waveforms may be saved in any of four REF waveform nonvolatile memories. Any or all of the saved reference waveforms may be displayed for comparison with the waveforms being currently acquired. The source and destination of waveforms to be saved may be user designated. Assignment can be made to save either chan-
nel 1 or channel 2 (or the results of an addition or multiplication of the two channels) to any REF memory or to move a stored reference from one REF memory to another. Reference waveforms may also be written into a REF memory location via the GPIB interface.

The scope is fully controllable and capable of sending and receiving waveforms via the standard equipped GPIB interface. This feature makes the instrument ideal for making automated measurements in a production or research and development environment that calls for repetitive data taking. Self- calibration and self-diagnostic features built into the scope to aid in fault detection and servicing are also accessible via commands sent from the GPIB controller.

Another standard feature is the "DEVICES" setting for GPIB Interface control. This feature allows the user to output waveforms (and other on-screen information) from the front panel to many printers and plotters that use HP® Graphics Language. In this way, hard copies of acquired waveforms can be obtained without putting the scope into a system controller environment

## EXTENDED FEATURES

There are several other features incorporated into this instrument designed to make it more usable, namely, the HELP, Auto Setup, MEASURE, and AutoStep Sequencer features.

HELP: The HELP function can be used to display operational information about any front-panel control. When HELP mode is in effect, manipulating almost any front-panel control causes the scope to display information about that control. When HELP is first invoked, an introduction to HELP is displayed on screen.

Auto Setup: The Auto Setup function is used to automatically setup the scope for a viewable display based on the input signal. The user can specify the waveform characteristic the display is optimized for (front-edge, period, etc.) from a menu displayed upon executing Auto Setup.

MEASURE: MEASURE automatically extracts parameters from signal input to the scope. In the "SNAPSHOT" mode, 20 different waveform parameters are extracted and displayed for a single acquisition. In the continuous extraction mode, up to four parameters are extracted continuously as the instrument continues to acquire.

AutoStep Sequencer (PRGM): With AutoStep, the user can save single front-panel setups or sequences of setups and associated flow control and Input/Output actions for later recall. If MEASURE and/or OUTPUT are saved as part of these setups they can be used for automatic parameter extraction and data printout. 100 to 800 frontpanel setups (depending on complexity) can be stored in one or more sequences.

The complete descriptions of these four features are found in Section 5 of the Operators manual included with this instrument.

The following items are standard accessories shipped with the scope instrument:

2 Probe packages
1 Snap-lock accessories pouch
1 Zip-lock accessories pouch
1 Operators manual
1 Programmer's Reference Guide
2 Users Reference Guide
1 Fuse
1 Power cord (installed)
1 Blue plastic CRT filter (installed)
1 Clear plastic CRT filter
1 Front-panel cover
For part numbers and further information about standard accessories and a list of the optional accessories, refer to "Options and Accessories" (Section 7) in this manual. For additional information on accessories and ordering assistance, contact your Tektronix representative or local Tektronix Field Office.

## PERFORMANCE CONDITIONS

The following electrical characteristics (Table 1-1) apply when the scope has been calibrated at an ambient temperature between $+20^{\circ} \mathrm{C}$ and $+30^{\circ} \mathrm{C}$, has had a warmup
period of at least 20 minutes and is operating at an ambient temperature between $-15^{\circ} \mathrm{C}$ and $+55^{\circ} \mathrm{C}$ (unless otherwise noted).

Items listed in the "Performance Requirements" column are verifiable qualitative or quantitative limits that define the measurement capabilities of the instrument.

Environmental characteristics are given in Table 1-2. The scope meets the environmental requirements of MIL-T-28800C for Type III, Class 3, Style D equipment, with the humidity and temperature requirements defined in paragraphs 3.9.2.2, 3.9.2.3, and 3.9.2.4. The rackmounted scope meets the vibration and shock requirements of MIL-T-28800C for Type III, Class 5, Style D equipment when mounted using the rackmount rear-support kit supplied with both the 1R Option and the Rackmount Conversion kit.

Mechanical characteristics of the scope are listed in Table 1-3.

Video Option characteristics are given in Table 1-4.

## RECOMMENDED ADJUSTMENTS SCHEDULE

For optimum performance to specification, the internal SELF CAL should be done:

1. If the operating temperature is changed by more that $5^{\circ} \mathrm{C}$ since the last SELF CAL was performed.
2. Immediately before making measurements requiring the highest degree of accuracy.

Table 1-1 Electrical Characteristics

| Characteristics | Performance Requirements |
| :---: | :---: |
| ACQUISITION SYSTEM-CHANNEL 1 AND CHANNEL 2 |  |
| Resolution | 8 bits. ${ }^{\text {a }}$ <br> Displayed vertically with 25 digitization levels (DL) ${ }^{\mathbf{b}}$ per division. |
| Dynamic Range ${ }^{\text {a }}$ <br> SEC/DIV <br> 100 or slower | -128 to +127 DL's. |
| 50 to 500 ns | -124 to +123 DL's. |
| 200 ns | -121 to +120 DL's. |
| 100 ns | -113 to +112 DL's. |
| 50 ns to 2 ns Repet OFF | -113 to +112 DL's. |
| Repet ON | 121 to 120 DL's. |
| Record Length | 1024 samples. ${ }^{\text {a }}$ <br> Displayed horizontally with 50 samples per division, 20.48-division trace length. ${ }^{\text {a }}$ |
| Sample Rate | 10 samples per second to 500 megasamples per second ( 5 s per division to 100 ns per division). |
| Sensitivity <br> Range | $80 \mu \mathrm{~V}$ per DL to 0.2 V per DL in a 1-2-5 sequence of 11 steps ( 2 mV per division to 5 V per division). |
| Accuracy <br> Normal and Average Modes | Within $\pm(2 \%+1$ DL $)$ at any VOLTS/DIV setting for a signal 1 kHz or less contained within $\pm 75 \mathrm{DL}$ ( $\pm 3$ divisions) of center when a SELF CAL has been performed within $\pm 15^{\circ} \mathrm{C}$ of the operating temperature. Measured on a four- or five-division signal with VOLTS or V@T cursors; UNITS set to delta volts. |
| Envelope Mode | Add 1\% to Normal Mode specifications. |
| Variable Range | Continuously variable between VOLTS/DIV settings. Extends sensitivity to 0.5 V per DL or greater, 12.5 V per division or greater. |

aperformance Requirement not checked in the manual.
b"DL" is the abbreviation for "digitization level." A DL is the smallest voltage level change that can be resolved by the internal 8 -bit A-D converter, with the input scaled to the VOLTS/DIV setting of the channel used. Expressed as a voltage, a DL is equal to $\mathbf{1 / 2 5}$ of a division times the VOLTS/DIV setting.

Table 1-1 (cont)

| Characteristics | Performance Requirements |
| :---: | :---: |
| ACQUISITION SYSTEM-CHANNEL 1 AND CHANNEL 2 (cont) |  |
| Bandwidth | Bandwidth is measured with a leveled, low distortion, $50-\Omega$ source, sine-wave generator, terminated in $50 \Omega$. The reference signal is set to 6 divisions or to the maximum leveled amplitude obtainable if the Volt/Div setting is too high to yield 6 div's on screen. <br> Bandwidth with probe is checked using a probe-tip-to-GR termination adaptor (017-0520-00). <br> Bandwidth with external termination is checked using a BNC $50-\Omega$ feed-through terminator (011-0049-01). |
| -3 dB Bandwidth <br> Normal or Average Modes. Envelope Mode at SEC/DIV settings of $0.2 \mu \mathrm{~s}$ or faster. $\begin{aligned} & -15^{\circ} \mathrm{C} \text { to }+30^{\circ} \mathrm{C} \\ & +30^{\circ} \mathrm{C} \text { to }+55^{\circ} \mathrm{C} \end{aligned}$ | Using standard accessory probe or internal termination (not checked with probe in manual). <br> Dc to 300 MHz . <br> Upper Bandwidth Limit reduced by 2.5 MHz for each ${ }^{\circ} \mathrm{C}$ above $30^{\circ} \mathrm{C}$ |
| Envelope Mode at SEC/DIV settings of $0.5 \mu \mathrm{~s}$ or slower. | Dc to 150 MHz using standard accessory probe, internal 50- $\Omega$ termination, or external $50-\Omega$ termination on $1-\mathrm{M} \Omega$ input. ${ }^{a}$ |
| -4.7 dB Bandwidth <br> Normal or Average Mode. Envelope Mode at SEC/DIV settings of $0.2 \mu \mathrm{~s}$ or faster. $+30^{\circ} \mathrm{C} \text { to }+55^{\circ} \mathrm{C}$ | Using 50- $\Omega$ external termination on $1-\mathrm{M} \Omega$ input. <br> Upper Bandwidth Limit reduced by 2.5 MHz for each ${ }^{\circ} \mathrm{C}$ above $30^{\circ} \mathrm{C}$. ${ }^{\text {a }}$ |
| Single Event Useful Storage Bandwidth <br> Normal or Average Mode, SEC/DIV at $0.1 \mu \mathrm{~s}$ or Faster; Repet OFF | DC to 200 MHz (calculated). $\text { USB }=\frac{F_{\text {(sample freg max) }}{ }^{c}}{2.5}$ |
| AC Coupled Lower -3 dB Point 1X Probe | 10 Hz or less. ${ }^{\text {a }}$ |
| 10X Probe | 1 Hz or less. ${ }^{\text {a }}$ |
| Step Response, Repet and Average On; Average Set to 16 Rise Time | 1.17 ns or less (calculated). ${ }^{\text {a }}$ $T_{r} \text { (in ns) }=\frac{350}{B W(\text { in } \mathrm{MHz})}$ |

## aperformance Requirement not checked in the manual.

csample freq. max. is 500 MHz .

Table 1-1 (cont)

| Characteristics | Performance Requirements |
| :---: | :---: |
| ACQUISITION SYSTEM-CHANNEL 1 AND CHANNEL 2 (cont) |  |
| Envelope Mode Pulse Response |  |
| Minimum Single Pulse Width for 50\% or Greater Amplitude Capture at 85\% or Greater Confidence | $2 \mathrm{~ns}{ }^{\text {a }}$ |
| Minimum Single Pulse Width for Guaranteed 50\% or Greater Amplitude Capture | $8 \mathrm{~ns} .^{\text {a }}$ |
| Channel Isolation | Measured with a 10 -division, sine-wave input and equal VOLT/DIV settings on both channels. 100:1 or greater at 100 MHz for VOLT/DIV settings from $2 \mathrm{mV} /$ DIV and $500 \mathrm{mV} /$ DIV; $50: 1$ or greater at 300 MHz for VOLT/DIV settings from $20 \mathrm{mV} / \mathrm{DIV}$ to $500 \mathrm{mV} /$ DIV. $25: 1$ or greater at 300 MHz for VOLT/DIV settings of $5 \mathrm{mV} / \mathrm{DIV}$ and $10 \mathrm{mV} /$ DIV. |
| Acquired Channel 2 Signal Delay with Respect to Channel 1 Signal at Full Bandwidth | $\pm 250$ ps. ${ }^{\text {a }}$ |
| Input $R$ and C (1 M $\Omega$ ) |  |
| Resistance | $1 \mathrm{M} \Omega \pm 0.5 \% .^{\mathrm{a}}$ <br> In each attenuator, the input resistance of all VOLTS/DIV positions is matched to within $0.5 \%$. ${ }^{\text {a }}$ |
| Capacitance | $15 \mathrm{pF} \pm 2 \mathrm{pF} \mathrm{~F}^{\mathrm{a}}$ <br> In each attenuator, the input capacitance of all VOLTS/DIV positions is matched to within 0.5 pF . ${ }^{\text {a }}$ |
| Input R (50 $\mathrm{S}_{\text {) }}$ |  |
| Resistance | $50 \Omega \pm 1 \%$. ${ }^{\text {a }}$ |
| VSWR (DC to 300 MHz ) | 1.3:1 or better. ${ }^{\text {a }}$ |
| Maximum Input Voltage $\dagger$ | 5 V rms; $0.5 \mathrm{~W} \cdot \mathrm{sec}$ for any one-second interval for instantaneous voltages from 5 V to 50 V . |

${ }^{\text {a Performance Requirement not checked in the manual. }}$

Table 1-1 (cont)

| Characteristics | Performance Requirements |
| :---: | :---: |
| ACQUISITION SYSTEM-CHANNEL 1 AND CHANNEL 2 (cont) |  |
| Maximum Input Voltages <br> Input Coupling Set to DC, AC, or GND | 400 V (dc + peak ac); 800 V p-p ac at 10 kHz or less. ${ }^{\text {a }}$ |
| Common-Mode Rejection Ratio (CMRR); ADD Mode with Either Channel Inverted | At least 10:1 at 50 MHz for common-mode signals of 10 divisions or less with VARIABLE VOLTS/DIV adjusted for best CMRR at 50 kHz . |
| POSITION <br> Range | $\pm$ (9.3 to 10.4) div., at 50 mV per division with INVERT off, when Self Cal has been done within $\pm 5^{\circ} \mathrm{C}$ of the operating temperature. |
| Gain Match between NORMAL and SAVE | $\pm 3$ DLs for positions within $\pm 5$ divisions from center. |
| Low-Frequency Linearity <br> Normal or Average Mode | 3 DLs or less compression or expansion of a two-division, center-screen signal when positioned anywhere within the acquisition window. |
| 20-MHz Bandwidth Limiter -3 dB Bandwidth | 13 MHz to 24 MHz . |
| $100-\mathrm{MHz}$ Bandwidth Limiter -3 dB Bandwidth | 80 MHz to 120 MHz . |
| Rise Time | 2.9 ns to $4.4 \mathrm{~ns}^{\text {a }}$ <br> With a five-division, fast-rise step (rise time of 300 ps or less) using $50-\Omega$ dc input coupling and VOLTS/DIV setting of 10 mV . ${ }^{\text {a }}$ |

aPerformance Requirement not checked in the manual.

Table 1-1 (cont)

| Characteristics | Performance Requirements |
| :---: | :---: |
| TRIGGERING-A and B |  |
| Minimum P-P Signal Amplitude for Stable ${ }^{\text {a }}$ Triggering from Channel 1, Channel 2, or ADD Source |  |
| A Trigger |  |
| DC Coupled | 0.35 division from $D C$ to 50 MHz , increasing to 1.0 division at 300 MHz ; 1.5 divisions at 300 MHz in ADD mode. |
| NOISE REJ Coupled | 1.2 divisions or less from $D C$ to 50 MHz ; increasing to 3 divisions at $300 \mathrm{MHz} ; 4.5$ divisions at 300 MHz in ADD mode. |
| AC Coupled | 0.35 division from 60 Hz to 50 MHz ; increasing to 1.0 division at $300 \mathrm{MHz} ; 1.5$ divisions at 300 MHz in ADD mode. Attenuates signals below 60 Hz . |
| HF REJ Coupled | 0.50 division from DC to 30 kHz . Attenuates signals above 30 kHz . |
| LF REJ Coupled | 0.50 division from 80 kHz to 50 MHz ; increasing to 1.0 division at $300 \mathrm{MHz} ; 1.5$ divisions at 300 MHz in ADD mode. Attenuates signal below 80 kHz . |
| B Trigger | Multiply all A Trigger specifications by two. |
| A.B Selected | Multiply all A Trigger specifications by two. |
| Minimum P-P Signal Amplitude for Stable Triggering ${ }^{\text {a }}$ from EXT TRIG 1 or EXT TRIG 2 Source |  |
| A Trigger |  |
| EXT Gain $=1$ |  |
| DC Coupled | 17.5 mV from DC to 50 MHz , increasing to 50 mV at 300 MHz . |
| NOISE REJ Coupled | 60 mV or less from DC to 50 MHz ; increasing to 150 mV at 300 MHz . |
| AC Coupled | 17.5 mV from 60 Hz to 50 MHz ; increasing to 50 mV at 300 MHz . Attenuates signals below 60 Hz . |
| HF REJ Coupled | 25 mV from DC to 30 kHz . |
| LF REJ Coupled | 25 mV from 80 kHz to 50 MHz ; increasing to 50 mV at 300 MHz . |
| EXT Gain $=\div 5$ | Amplitudes are five times those specified for Ext Gain = 1. |
| B Trigger | Multiply all A Trigger amplitude specifications by two. |
| A.B Selected | Multiply all A Trigger amplitude specifications by two. |

[^1]Table 1-1 (cont)

| Characteristics | Performance Requirements |
| :---: | :---: |
| TRIGGERING-A and B (cont) |  |
| Maximum P-P Signal Rejected by NOISE REJ Coupling Signals within the Vertical Bandwidth Channel 1 or Channel 2 Source | 0.4 division or greater for VOLTS/DIV settings of 10 mV and higher. <br> Maximum noise rejected is reduced at $\mathbf{2} \mathbf{~ m V}$ per division and 5 mV per division. |
| EXT TRIG 1 or EXT TRIG 2 Source | 20 mV or greater when Ext Trig Gain $=1.100 \mathrm{mV}$ or greater when Ext Trig Gain $=\div 5$. |
| EXT TRIG 1 and EXT TRIG 2 Inputs Resistance | $1 \mathrm{M} \Omega \pm 1 \%^{\text {. }}{ }^{\text {a }}$ |
| Capacitance | $15 \mathrm{pF} \pm 3 \mathrm{pF} .^{\text {a }}$ |
| Maximum Input Voltage | 400 V (dc + peak ac); 800 V p-p ac at 10 kHz or less. ${ }^{\text {a }}$ |
| LEVEL Control Range <br> Channel 1 or Channel 2 Source | $\pm 18$ divisions $\times$ VOLTS/DIV setting. ${ }^{\text {a }}$ |
| EXT TRIG 1 or EXT TRIG 2 Source EXT GAIN $=1$ | $\pm 0.9$ volt. ${ }^{\text {a }}$ |
| EXT GAIN $=\div 5$ | $\pm 4.5$ volts. ${ }^{\text {a }}$ |
| LEVEL Readout Accuracy (for triggering signals with transition times greater than 20 ns ) <br> Channel 1 or Channel 2 Source <br> DC Coupled $+15^{\circ} \mathrm{C} \text { to }+35^{\circ} \mathrm{C}$ | Within $\pm[3 \%$ of setting $+3 \%$ of p-p signal $+(0.2$ division $\times$ VOLTS/DIV setting) $+0.5 \mathrm{mV}+(0.5 \mathrm{mV} \times$ probe attenuation factor)]. |
| $\begin{aligned} & -15^{\circ} \mathrm{C} \text { to }+55^{\circ} \mathrm{C} \text { (excluding }+15^{\circ} \mathrm{C} \text { to } \\ & +35^{\circ} \mathrm{C} \text { ) } \end{aligned}$ | Add ( $1.5 \mathrm{mV} \times$ probe attenuation) to $+15^{\circ} \mathrm{C}$ to $+35^{\circ} \mathrm{C}$ specification. ${ }^{\text {a }}$ |
| NOISE REJ Coupled | Add $\pm$ ( 0.6 division $\times$ VOLTS/DIV setting) to DC Coupled specifications. <br> Checked at 50 mV per division. |

[^2]Table 1-1 (cont)

aPerformance Requirement not checked in the manual.

Table 1-1 (cont)

| Characteristics | Performance Requirements |  |  |
| :---: | :---: | :---: | :---: |
|  | TRIGGERING-A and B (cont) |  |  |
| Variable A Trigger Holdoff | A SEC/DIVa | MIN HOa | MAX HOa |
|  | 500 ns | 5-10 $\mu \mathrm{s}$ |  |
|  | $\begin{aligned} & 1 \mu \mathrm{~s} \\ & 2 \mu \mathrm{~s} \\ & 5 \mu \mathrm{~s} \end{aligned}$ | $\begin{gathered} 10-20 \mu \mathrm{~s} \\ 20-40 \mu \mathrm{~s} \\ 50-100 \mu \mathrm{~s} \end{gathered}$ | 100-150 $\mu \mathrm{S}$ |
|  | $\begin{aligned} & 10 \mu \mathrm{~S} \\ & 20 \mu \mathrm{~S} \\ & 50 \mu \mathrm{~S} \end{aligned}$ | $\begin{aligned} & 0.1-0.2 \mathrm{~ms} \\ & 0.2-0.4 \mathrm{~ms} \\ & 0.5-1.0 \mathrm{~ms} \end{aligned}$ | 1-1.5 ms |
|  | $\begin{aligned} & 100 \mu \mathrm{~S} \\ & 200 \mu \mathrm{~S} \\ & 500 \mu \mathrm{~S} \\ & \hline \end{aligned}$ | $1-2 \mathrm{~ms}$ 2-4 ms $5-10 \mathrm{~ms}$ | $10-15 \mathrm{~ms}$ |
|  | 1 ms <br> 2 ms <br> 5 ms | $\begin{gathered} 10-20 \mathrm{~ms} \\ 20-40 \mathrm{~ms} \\ 50-100 \mathrm{~ms} \end{gathered}$ | 90-150 ms |
|  | 10 ms 20 ms 50 ms | $\begin{aligned} & 0.1-0.2 \mathrm{~s} \\ & 0.2-0.4 \mathrm{~s} \\ & 0.5-1.0 \mathrm{~s} \\ & \hline \end{aligned}$ | 0.9-1.5 s |
|  | 100 ms <br> 200 ms | $\begin{aligned} & 1-2 \mathrm{~s} \\ & 2-4 \mathrm{~s} \end{aligned}$ |  |
|  | $\begin{gathered} 500 \mathrm{~ms} \\ 1 \mathrm{~s} \\ 2 \mathrm{~s} \\ 5 \mathrm{~s} \\ \hline \end{gathered}$ | 5-10 s | 9-15 s |
| SLOPE Selection | Conforms to trigger-source and ac-power-source waveforms. |  |  |
| Trigger Position Jitter (P-P) | Checked in NORMAL ACQUIRE mode with a 5-division step having less than or equal to 1 ns rise time. |  |  |
| A Mode, B Mode (TRIG AFTER) SEC/DIV 100 ns and slower | $0.04 \times$ SEC/DIV |  |  |
| SEC/DIV 50 ns and faster | $\left(0.04 \times\right.$ SEC/DIV setting) $+200 \mathrm{ps}^{\text {a,b }}$ |  |  |
| B Mode (RUNS AFTER) |  |  |  |
| SEC/DIV $50 \mu$ s to 100 ns | $0.04 \times$ B SEC/DIV ${ }^{\text {a }}$ |  |  |
| SEC/DIV $100 \mu \mathrm{~s}$ and slower | $0.08 \times$ B SEC/DIV ${ }^{\text {a }}$ |  |  |

## aperformance Requirements not checked in the manual.

buse B SEC/DIV setting it mode is B; otherwise, use A SEC/DIV setting.

Table 1-1 (cont)

| Characteristics | Performance Requirements |
| :---: | :---: |
| TIME BASE |  |
| Sample Rate Accuracy <br> Average Over 100 or More Samples | $\pm 0.0015 \%$. ${ }^{\text {a }}$ |
| External Clock Repetition Rate Minimum | $1 \mathrm{MHz}{ }^{\text {a }}$ |
| Maximum | $100 \mathrm{MHz}{ }^{\text {a }}$ |
| Events Count | 1 to $65,536^{\text {a }}$ |
| Events Maximum Repetition Rate | $100 \mathrm{MHz}{ }^{\text {a }}$ |
| Signal Levels Required for EXT Clock or EVENTS Channel 1 or Channel 2 SOURCE DC Coupled | 0.7 division from DC to 50 MHz ; increasing to 2.0 divisions at $100 \mathrm{MHz} ; 3.0$ divisions at 100 MHz in ADD mode. ${ }^{\text {a }}$ |
| NOISE REJ Coupled | 2.4 divisions or less from $D C$ to 50 MHz ; increasing to 6.0 divisions at $100 \mathrm{MHz} ; 9.0$ divisions at 100 MHz in ADD mode. ${ }^{\text {a }}$ |
| AC Coupled | 0.7 division from 60 Hz to 50 MHz ; increasing to 2.0 divisions at $100 \mathrm{MHz} ; 3.0$ divisions at 100 MHz in ADD mode. Attenuates signals below 60 Hz . ${ }^{\text {a }}$ |
| HF REJ Coupled | 1.0 division from $D C$ to 30 kHz . Attenuates signals above $30 \mathrm{kHz} .^{\mathrm{a}}$ |
| LF REJ Coupled | 1.0 division from 80 kHz to 50 MHz ; increasing to 2.0 divisions at 100 MHz ; 3.0 divisions at 100 MHz in ADD mode. Attenuates signals below $80 \mathrm{kHz}{ }^{\text {a }}$ |
| EXT TRIG 1 or EXT TRIG 2 Source <br> Ext Gain $=1$ <br> DC Coupled | 35 mV from DC to 50 MHz ; increasing to 100 mV at 100 MHz . ${ }^{\text {a }}$ |
| NOISE REJ Coupled | 120 mV or less from DC to 50 MHz ; increasing to 300 mV at $100 \mathrm{MHz}{ }^{\text {a }}$ |
| AC Coupled | 35 mV from 60 Hz to 50 MHz ; increasing to 100 mV at 100 MHz . Attenuates signals below 60 Hz . ${ }^{\text {a }}$ |
| HF REJ Coupled | 50 mV from DC to $30 \mathrm{kHz} .^{\text {a }}$ |
| LF REJ Coupled | 50 mV from 80 kHz to 50 MHz ; increasing to 100 mV at 100 MHz . ${ }^{\text {a }}$ |
| Ext Gain $=\div 5$ | Amplitudes are five times those specified for Ext Gain $=1 .{ }^{\text {a }}$ |

[^3]Table 1-1 (cont)

| Characteristics | Performance Requirements |
| :---: | :---: |
| TIME BASE (cont) |  |
| Delay Time Range <br> B RUNS AFTER DELAY <br> SEC/DIV 50 ns and faster REPET ON | ( $0.08 \times \mathrm{B} \mathrm{SEC/DIV}$ ) to $1.05 \mathrm{~ms}{ }^{\text {a }}$ |
| REPET OFF | (0.08 $\times$ B SEC/DIV) to $524 \mu \mathrm{~s}$. ${ }^{\text {a }}$ |
| SEC/DIV $50 \mu \mathrm{~s}$ to 100 ns | ( $0.08 \times$ B SEC/DIV) to $\left(65,536 \times 0.08 \times\right.$ B SEC/DIV) ${ }^{\text {a }}$ |
| SEC/DIV $100 \mu$ s and slower | ( $0.04 \times$ B SEC/DIV) to ( $65,536 \times 0.04 \times$ B SEC/DIV) ${ }^{\text {a }}$ |
| B TRIGGERABLE AFTER DELAY SEC/DIV 50 ns and faster REPET ON | 16 ns to $1.05 \mathrm{~ms} .^{\text {a }}$ |
| REPET OFF | 8 ns to $524 \mu \mathrm{~s}$. ${ }^{\text {a }}$ |
| SEC/DIV $50 \mu \mathrm{~s}$ to 100 ns | ( $0.08 \times$ B SEC/DIV) to ( $65,536 \times 0.08 \times$ B SEC/DIV) ${ }^{\text {a }}$ |
| SEC/DIV $100 \mu$ s and slower | ( $0.04 \times$ B SEC/dIV) to ( $65,536 \times 0.04 \times$ B SEC/DIV) ${ }^{\text {a }}$ |
| Delay Time Resolution <br> B RUNS AFTER DELAY <br> SEC/DIV $50 \mu$ s and faster | (0.08 $\times$ B SEC/DIV). ${ }^{\text {a }}$ |
| SEC/DIV $100 \mu$ s and slower | (0.04 $\times$ B SEC/DIV). ${ }^{\text {a }}$ |
| B TRIGGERABLE AFTER DELAY SEC/DIV 50 ns and faster REPET ON | $16 \mathrm{~ns} .^{\text {a }}$ |
| REPET OFF | $8 \mathrm{~ns} .^{\text {a }}$ |
| SEC/DIV $50 \mu \mathrm{~s}$ to 100 ns | ( $0.08 \times$ B SEC/DIV) $^{\text {a }}$ |
| SEC/DIV $100 \mu \mathrm{~s}$ and slower | (0.04 $\times$ B SEC/DIV) ${ }^{\text {a }}$ |
| Delay Time Accuracy | $\pm 0.0015^{\text {a }}$. |

aPerformance Requirement not checked in the manual.

Table 1-1
Electrical Characteristics (Cont.)

| Characteristic | Nerformance Requirement |
| :--- | :--- |
| NONVOLATILE MEMORY |  |
| Front-Panel Setting, Waveform Data, Sequencer, and <br> Calibration Data Retention Time | Greater than 3 years. <br> Proprietary Data Removal from Memory |
| Executing a TEKSECURE Erase Memory irretrievably deletes <br> all saved waveforms (on screen or in Reference memories), <br> all front-panel settings, and all sequences stored in <br> Sequencer memory. To further assure that no proprietary data <br> remains stored, Erase Memory also clears all remaining NV <br> RAM, except those locations storing calibration constants, <br> calibration status/results, and data for the real-time clock. <br> The instrument is left with a default front-panel setup (the <br> same one invoked by doing an INIT front panel). |  |

Table 1-1
Electrical Characteristics (Cont.)

| Characteristic | Performance Requirement |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| SIGNAL OUTPUTS |  |  |  |  |
| CALIBRATOR <br> Voltage (with A SEC/DIV switch set to 1 ms ) $1 \mathrm{M} \Omega$ Load | CALIBRATOR output amplitu $0.4 \mathrm{~V} \pm 1 \% .^{\text {a }}$ | utput amplitu es at 1 ms SE | at 5 MHz are IV setting. ${ }^{\text {a }}$ | least $50 \%$ of |
| $50 \Omega$ Load | $0.2 \mathrm{~V} \pm 1.5 \%$ |  |  |  |
| Current (short circuit load with A SEC/DIV switch set to 1 ms ) | $8 \mathrm{~mA} \pm 1.5 \%$. |  |  |  |
| Repetition Period | A SEC/DIV Setting ${ }^{\text {a }}$ | Calibrator Frequencya | Calibrator Perioda | Div/Cycle ${ }^{\text {a }}$ |
|  | $\begin{array}{r} 2 \mathrm{~ns} \\ 5 \mathrm{~ns} \\ 10 \mathrm{~ns} \\ 20 \mathrm{~ns} \\ 50 \mathrm{~ns} \\ 100 \mathrm{~ns} \\ 200 \mathrm{~ns} \end{array}$ | 5 MHz | 200 ns | $\begin{array}{r} 100 \\ 40 \\ 20 \\ 10 \\ 4 \\ 2 \\ 1 \end{array}$ |
|  | $\begin{array}{r} 500 \mathrm{~ns} \\ 1 \mu \mathrm{~s} \\ 2 \mu \mathrm{~s} \end{array}$ | 1 MHz | $1 \mu \mathrm{~s}$ | $\begin{array}{r} 2 \\ 1 \\ 0.5 \end{array}$ |
|  | $\begin{array}{r} 5 \mu \mathrm{~s} \\ 10 \mu \mathrm{~s} \\ 20 \mu \mathrm{~s} \end{array}$ | 50 kHz | $20 \mu \mathrm{~s}$ | 4 2 1 |
|  | $\begin{array}{r} 50 \mu \mathrm{~s} \\ 100 \mu \mathrm{~s} \\ 200 \mu \mathrm{~s} \end{array}$ | 5 kHz | $200 \mu s$ | 4 2 1 |
|  | $500 \mu \mathrm{~s}$ 1 ms 2 ms | 500 Hz | 2 ms | 4 2 1 |
|  | 5 ms 10 ms 20 ms 50 ms 100 ms 200 ms 500 ms 1 s 2 s 5 s | 50 Hz | 20 ms | 4 2 1 0.4 0.2 0.1 0.04 0.02 0.01 0.004 |

aPerformance Requirements not checked In the manual.

Table 1-1 (cont)

| Characteristics | Performance Requirements |
| :---: | :---: |
| SIGNAL OUTPUTS (cont) |  |
| CH 2 SIGNAL OUTPUT |  |
| Output Voltage | 20 mV per division $\pm 10 \%$ into $1 \mathrm{M} \Omega$. <br> 10 mV per divison $\pm 10 \%$ into $50 \Omega$. |
| Offset | $\pm 10 \mathrm{mV}$ into $50 \Omega$, when dc balance has been performed within $\pm 5^{\circ} \mathrm{C}$ of the operating temperature. |
| -3 dB Bandwidth | DC to greater than 50 MHz . |
| A TRIGGER, RECORD TRIGGER, and WORD RECOGNIZER Output |  |
| Logic Polarity | Negative true. Trigger occurrence indicated by a HI to LO transition. ${ }^{\text {a }}$ |
| Output Voltage HI |  |
| Load of $400 \mu \mathrm{~A}$ or Less | 2.5V to $3.5 \mathrm{~V} .{ }^{\text {a }}$ |
| $50 \Omega$ Load to Ground | 0.45 V or greater. ${ }^{\text {a }}$ |
| Output Voltage LO |  |
| Load of 4 mA or Less | 0.5 V or less. ${ }^{\text {a }}$ |
| $50 \Omega$ Load to Ground | 0.15 V or less. ${ }^{\text {a }}$ |
| SEQUENCE OUT, STEP COMPLETE Outputs |  |
| Logic Polarity | Negative true. HI to LO transition indicates the event occurred. |
| Output Voltage HI |  |
| 50- $\Omega$ Load to Ground | 0.45 V or greater. ${ }^{\text {a }}$ |
| Output Voltage LO |  |
| 50- $\Omega$ Load to Ground | 0.15 V or less. ${ }^{\text {a }}$ |
| SEQUENCE IN Input |  |
| High-Level Input Current | $20 \mu \mathrm{~A}$ maximum at Vin $=2.7 \mathrm{~V}$. ${ }^{\text {a }}$ |
| Low-Level Input Current | -0.4 mA maximum at Vin $=0.4 \mathrm{~V}$. ${ }^{\text {a }}$ |
| High-Level Input Voltage | 2.0 V minimum. ${ }^{\text {a }}$ |
| Low-level Input Voltage | 0.8 V maximum. ${ }^{\text {a }}$ |
| Absolute Maximum Ratings |  |
| Vin max | +7.0 V. ${ }^{\text {a }}$ |
| Vin min | -0.5 V. ${ }^{\text {a }}$ |

[^4]Table 1-1 (cont)

| Characteristics | Performance Requirements |
| :---: | :---: |
| DISPLAY |  |
| Graticule | $80 \mathrm{~mm} \times 100 \mathrm{~mm}(8 \times 10 \text { divisions })^{\text {a }}$ |
| Phosphor | P31. ${ }^{\text {a }}$ |
| Nominal Accelerating Potential | $16 \mathrm{kV} .^{\text {a }}$ |
| Waveform and Cursor Display, Vertical Resolution, Electrical | One part in 1024 (10 bit). Calibrated for 100 points per division. ${ }^{\text {a }}$ |
| Gain Accuracy | Graticule indication of voltage cursor difference is within $1 \%$ of CRT cursor readout value, measured over center 6 divisions. |
| Centering; Vectors OFF Offset with Vectors ON | Within $\pm 0.1$ division. Less than 0.05 division. |
| Linearity | Less than 0.1 division difference between graticule indication and crt cursor readout when active volts cursor is positioned anywhere on screen and inactive cursor is at center screen. ${ }^{\text {a }}$ |
| Vector Response NORMAL Mode Step Aberration | +4\%, -4\%, 4\% p-p. |
| Fill | Edges of filled regions match reference lines within $\pm 0.1$ division. |
| ENVELOPE Mode Fill | Less than $1 \%$ change in $\mathrm{p}-\mathrm{p}$ amplitude of a 6 -division, filled ENVELOPE waveform when switching vectors ON and OFF. |
| Waveform and Cursor Display, Horizontal Resolution, Electrical | One part in 1024 (10 bit). Calibrated for 100 points per division. ${ }^{\text {a }}$ |
| Gain Accuracy | Graticule indication at time cursor difference is within $1 \%$ of cr cursor readout value, measured over center 6 divisions. |
| Centering; Vectors OFF Offset with Vectors ON | Within $\pm 0.1$ division. Less than 0.05 division. |
| Linearity | Less than 0.1 division difference between graticule indication and crt cursor readout when active time cursor is positioned anywhere along center horizontal graticule line and inactive cursor is at center screen. ${ }^{\text {a }}$ |

[^5]Table 1-1 (cont)

| Characteristics | Performance Requirements |
| :---: | :---: |
| AC POWER SOURCE |  |
| Source Voltage Nominal Ranges $115 \text { V }$ | 90 V to $132 \mathrm{~V} .{ }^{\text {a }}$ |
| 230 V | 180 V to $250 \mathrm{~V} .^{\text {a }}$ |
| Source Frequency | 48 Hz to 440 Hz . ${ }^{\text {a }}$ |
| Fuse Rating | $5 \mathrm{~A}, 250 \mathrm{~V}$, AGC/3AG, Fast Blow; or $4 \mathrm{~A}, 250 \mathrm{~V}, 5 \times 20 \mathrm{~mm}$ Time-Lag (T). ${ }^{\text {a }}$ <br> Each fuse type requires a different fuse cap. ${ }^{\text {a }}$ |
| Power Consumption <br> Typical (standard instrument) | 160 watts (250 VA). ${ }^{\text {a }}$ |
| Maximum (fully optioned instrument) | 200 watts ( 300 VA ). ${ }^{\text {a }}$ |
| Primary Grounding ${ }^{\text {c }}$ | Type test $0.1 \Omega$ maximum. Routine test to check grounding continuity between chassis ground and protective earth ground. ${ }^{a}$ |

${ }^{\text {a Performance Requirement not checked in the manual. }}$
${ }^{\text {c Routine test is with ROD-L/EPA Electronic Model 100AV Hi-Pot Tester. This tests both the Primary Circuit Dielectric Withstand and }}$ Primary Grounding in one operation. Contact Tektronix Product Safety prior to using any other piece of equipment to perform these tests.

Table 1-2
Environmental Characteristics

| Characteristics | Performance Requirements |
| :---: | :---: |
| STANDARD INSTRUMENT |  |
| Environmental Requirements | This Oscilloscope meets the environmental requirements of MIL-T28800C for Type III, Class 3, Style D equipment, with the humidity and temperature requirements defined in paragraphs 3.9.2.2, 3.9.2.3, and 3.9.2.4 |
| Temperature |  |
| Operating | $-15^{\circ} \mathrm{C}$ to $+55^{\circ} \mathrm{C}$. |
| Nonoperating (storage) | $-62^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$. |
| Altitude |  |
| Operating | To 15,000 feet ( 4500 meters). Maximum operating temperature decreased $1^{\circ} \mathrm{C}$ for each 1000 feet ( 300 meters) above 5000 feet ( 1500 meters). |
| Nonoperating (storage) | To 50,000 feet (15,000 meters). |
| Humidity |  |
| Operating and Storage | Stored at $95 \%$ relative humidity for five cycles (120 hours) from $30^{\circ} \mathrm{C}$ to $60^{\circ} \mathrm{C}$, with operation performance checks at $30^{\circ} \mathrm{C}$ and $55^{\circ} \mathrm{C}$. |
| Vibration |  |
| Operating | 15 minutes along each of three axes at a total displacement of 0.025 inch ( 0.64 mm ) p-p ( 4 g at 55 Hz ), with frequency varied from 10 Hz to 55 Hz in one-minute sweeps. Hold 10 minutes at each major resonance, or if none exist, hold 10 minutes at 55 Hz ( 75 minutes total test time). |
| Shock |  |
| Operating and Nonoperating | 50-g, half-sine, 11 -ms duration, three shocks on each face, for a total of 18 shocks. |
| Transit Drop (not in shipping package) | 12-inch ( $300-\mathrm{mm}$ ) drop on each corner and each face (exceeds MIL-T-28800C, paragraphs 3.9.5.2 and 4.5.5.4.2). |
| Bench Handling <br> Cabinet On and Cabinet Off | MIL-STD-810C, Method 516.2, Procedure V (MIL-T-28800C, Paragraph 4.5.5.4.3). |
| Topple (cabinet installed) Operating | Set on rear feet and allow to topple over onto each of four adjacent faces (Tektronix Standard 062-2858-00). |
| Packaged Transportation Drop | Meets the limits of the National Safe Transit Assn., test procedure 1A-B-2; 10 drops of 36 inches ( 914 mm ) (Tektronix Standard 062-2858-00). |
| Vibration | Meets the limits of the National Safe Transit Assn., test procedure 1A-B-1; excursion of 1 inch ( 25.4 mm ) p-p at 4.63 Hz $(1.1 \mathrm{~g})$ for 30 minutes (Tektronix Standard 062-2858-00). |

Table 1-2 (cont)

| Characteristics | Performance Requirements |
| :---: | :---: |
| STANDARD INSTRUMENT (cont) |  |
| Environmental Requirements (cont) <br> EMI (electromagnetic interference) | Meets MIL-T-28800C; MIL-STD-461B, part 4 (CE-03 and CS-02), part 5 (CS-06 and RS-02), and part 7 (CS-01, RE-02, and RS-03-limited to 1 GHz ); VDE 0871, Category B; Part 15 of FCC Rules and Regulations, Subpart J, Class A; and Tektronix Standard 062-2866-00. |
| Electrostatic Discharge Susceptibility | Meets Tektronix Standard 062-2862-00. The instrument will not change control states with discharges of less than 10 kV . |
| X-Ray Radiation | Meets requirements of Tektronix Standard 062-1860-00. |
| RACKMOUNTED INSTRUMENT |  |
| Environmental Requirements <br> Temperature (operating) | Listed characteristics for vibration and shock indicate those environments in which the rackmounted instrument meets or exceeds the requirements of MIL-T-28800C with respect to Type III, Class 5, Style D equipment with the rackmounting rearsupport kit installed. Refer to the Standard Instrument Environmental Specification for the remaining performance requirements. Instruments will be capable of meeting or exceeding the requirements of Tektronix Standard 062-2853-00, class 5. <br> $-15^{\circ} \mathrm{C}$ to $+55^{\circ} \mathrm{C}$, ambient temperature measured at the instrument's air inlet. Fan exhaust temperature should not exceed $+65^{\circ} \mathrm{C}$. |
| Vibration | 15 minutes along each of three major axes at a total displacement of 0.015 inch $(0.38 \mathrm{~mm}) \mathrm{p}-\mathrm{p}(2.3 \mathrm{~g}$ at 55 Hz$)$, with frequency varied from 10 Hz to 55 Hz to 10 Hz in one-minute sweeps. Hold 10 minutes at each major resonance, or if no major resonance is present, hold 10 minutes at 55 Hz ( 75 minutes total test time). |
| Shock (operating and nonoperating) | $30-g_{\text {, }}$ half-sine, 11 -ms duration, three shocks per axis in each direction, for a total of 18 shocks. |

Table 1-3
Mechanical Characteristics

| Characteristics | Description |
| :---: | :---: |
| STANDARD INSTRUMENT |  |
| Weight |  |
| With Front Cover, Accessories, and Accessories Pouch | $\simeq 12.8 \mathrm{~kg}$ ( 28.1 lbs ) . |
| Without Front Cover, Accessories, and Accessories Pouch | $\simeq 10.9 \mathrm{~kg}$ (23.9 lbs). |
| Domestic Shipping Weight | $\simeq 16.4 \mathrm{~kg}$ ( 36 lbs ). |
| Overall Dimensions | See Figure 1-1 for a dimensional drawing. |
| Height |  |
| With Feet and Accessories Pouch | 190 mm (7.48 in). |
| Without Accessories Pouch | 160 mm ( 6.3 in ). |
| Width (with handle) | 330 mm (13.0 in). |
| Depth |  |
| With Front Cover | 479 mm (18.86 in). |
| With Handle Extended | 550 mm (21.65 in). |
| Cooling | Forced air circulation; no air filter. |
| Finish | Tektronix Blue vinyl-clad material on aluminum cabinet. |
| Construction | Aluminum-alloy/plastic-composite chassis (spot-molded). Plasticlaminate front panel. Glass-laminate circuit boards. |
| RACKMOUNTING |  |
| Rackmounting Conversion Kit |  |
| Domestic Shipping Weight | 6.3 kg ( 13.8 lbs ). |
| Height | 178 mm ( 7 in ). |
| Width | 483 mm (19 in). |
| Depth | 419 mm (16.5 in). |
| Rear Support Kit |  |
| OPTION 1R |  |
| Rackmounted Instrument (Option 1R) Weight | $\simeq 15.8 \mathrm{~kg}$ ( 34.9 lbs ). |
| Domestic Shipping Weight | $\simeq 18.1 \mathrm{~kg}$ ( 39.9 lbs ). |
| Height | 178 mm ( 7 in ). |
| Width | 483 mm (19 in). |
| Depth | 419 mm (16.5 in). |

Table 1-4
Option 05 (TV Trigger) Electrical Characteristics

| Characteristics | Performance Requirements |
| :---: | :---: |
| VERTICAL-CHANNEL 1 AND CHANNEL 2 |  |
| Frequency Response Full Bandwidth 50 kHz to 5 MHz | Within $\pm 1 \%$. |
| Greater than 5 MHz to 10 MHz | Within $+1 \%,-2 \%$. |
| Greater than 10 MHz to 30 MHz | Within $+2 \%,-3 \%$. <br> For VOLTS/DIV switch settings between 5 mV and 0.2 V per division with VARIABLE VOLTS/DIV set to CAL. Five-division, 50 kHz reference signals from a $50 \Omega$ system. With external $50 \Omega$ termination on a $1 \mathrm{M} \Omega$ input. |
| 20 MHz Bandwidth Limit 50 kHz to 5 MHz | Within $+1 \%,-4 \%$. |
| Square Wave Flatness <br> Field Rate $5 \mathrm{mV} /$ div to $20 \mathrm{mV} / \mathrm{div}$ | $\pm 1 \%, 1 \% \mathrm{p}-\mathrm{p}$ at 60 Hz with input signal of 0.1 V . |
| $50 \mathrm{mV} / \mathrm{div}$ | $\pm 1 \%, 1 \%$ p-p at 60 Hz with input signal of 1.0 V . <br> With fast-rise step (rise time 1 ns or less), $1 \mathrm{M} \Omega$ dc input coupling, an external $50 \Omega$ termination, and VARIABLE VOLTS/DIV set to CAL. Exclude the first 20 ns following the step transition and exclude the first 30 ns when 20 MHz BW LIMIT is set. |
| Line Rate $5 \mathrm{mV} / \mathrm{div}$ to $20 \mathrm{mV} / \mathrm{div}$ | $\pm 1 \%, 1 \% \mathrm{p}-\mathrm{p}$ at 15 kHz with input signal of 0.1 V . |
| $50 \mathrm{mV} / \mathrm{div}$ | $\pm 1 \%, 1 \% \mathrm{p}-\mathrm{p}$ at 15 kHz with input signal of 1.0 V . |
| TV (Back-Porch) Clamp (CH 2 Only) 60 Hz Attenuation | 18 dB or greater. <br> For VOLTS/DIV switch settings between 5 mV and 0.2 V with VARIABLE VOLTS/DIV set to CAL. Six-division reference signal. |
| Back-Porch Reference | Within $\pm 1.0$ division of ground reference. |


| Characteristics | Performance Requirements |
| :---: | :---: |
| TRIGGERING |  |
| Sync Separation | Stable video rejection and sync separation from sync-positive or sync-negative composite video, 525 to 1280 lines, 50 Hz or 60 Hz , interlaced or noninterlaced systems. |
| Trigger Modes <br> A Horizontal Mode | Ail lines: <br> Field 1, selected line ( 1 to $n$ ), <br> Field 2, selected line ( 1 to n ), <br> Alt fields, selected line ( 1 to $n$ ). <br> n is equal to or less than the number of lines in the frame and less than or equal to 1280. |
| B Horizontal Mode | Delayed by time. |
| Minimum Input Signal Amplitude for Stable Triggering ${ }^{a, b}$ <br> Channel 1 and Channel 2 <br> Composite Video | 2 divisions. |
| Composite Sync | 0.6 divisions. <br> Peak signal amplitude within 18 divisions of input ground reference. |
| EXT TRIG 1 or EXT TRIG 2 EXT GAIN $=1$ <br> Composite Video | 60 mV . |
| Composite Sync | $30 \mathrm{mV} .$ <br> Peak signal amplitude within $\pm 0.9 \mathrm{~V}$ from input ground reference. |
| EXT GAIN $=\div 5$ <br> Composite Video | 300 mV . |
| Composite Sync | $150 \mathrm{mV}$ <br> Peak signal amplitude within $\pm 4.9 \mathrm{~V}$ from input ground reference. |

## ${ }^{\text {a }}$ Performance Requirement not checked in manual.

${ }^{b}$ A stable trigger is one that results in a unitorm, regular display triggered on the selected slope ( $\pm$ ). A stably-triggered display should NOT have the trigger point switch between opposite slopes on the waveform, nor should it "roll" across the screen, as successive acquisitions occur. At TIME/DIV settings of $2 \mathrm{~ms} / \mathrm{DIV}$ and faster, the TRIG'D LED is constantly lit if the display is stably triggered (the LED can flash for SEC/DIV settings of $10 \mathrm{~ms} / \mathrm{DIV}$ and slower).


Dimensions are in inches [mm]

Figure 1-1. Dimensional drawing.

## PREPARATION FOR USE

## SAFETY

This section tells how to prepare for and to proceed with the initial start-up of the TEKTRONIX 2440 Digital Oscilloscope.

Refer to the Operators and Servicing Safety Summaries at the front of this manual for power source, grounding, and other safety considerations pertaining to the use of the instrument. Before connecting the oscilloscope to a power source, read both this section and the Safety Summaries.


This instrument may be damaged if operated with the LINE VOLTAGE SELECTOR switch set for the wrong applied ac input-source voltage or if the wrong line fuse is installed.

## LINE VOLTAGE SELECTION

The scope operates from either a 115 V or 230 V nominal ac power-input source having a line frequency ranging from 48 Hz to 440 Hz . Before connecting the power cord to a power-input source, verify that the LINE VOLTAGE SELECTOR switch, located on the rear panel (see Figure 2-1), is set for the correct nominal ac inputsource voltage. To convert the instrument for operation from one line-voltage range to the other, move the LINE VOLTAGE SELECTOR switch to the correct nominal ac source-voltage setting (see Table 2-1). The detachable power cord may have to be changed to match the particular power-source outlet.

## LINE FUSE

To verify the proper value of the instrument's powerinput fuse, perform the following procedure:

1. Press in the fuse-holder cap and release it with a slight counterclockwise rotation.
2. Pull the cap (with the attached fuse inside) out of the fuse holder.
3. Verify proper fuse value (see Table 2-1).
4. Install the proper fuse and reinstall the fuse-holder cap.

## NOTE

A $4 \mathrm{~A}, 250 \mathrm{~V}, 5 \times 20 \mathrm{~mm}$ Time-lag (T) fuse may be substituted for the factory-installed fuse. However, the two types of fuses are NOT directly interchangeable; each requires a different type of fuse cap.


Figure 2-1. LINE VOLTAGE SELECTOR, line fuse, and power cord receptacle.

Table 2-1
Voltage, Fuse, and Power-Cord Data

| Plug Configuration | Category | Power Cord And Plug Type | Line Voltage Selector Setting | Voltage Range (AC) | Factory Installed Instrumen Fuse | Fuse Holder Cap | Reference Standards ${ }^{\text {b }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | U.S. <br> Domestic <br> Standard | $\begin{aligned} & \text { U.S. } \\ & 120 \mathrm{~V} \\ & 15 \mathrm{~A} \end{aligned}$ | 115 V | $\begin{aligned} & 90 \mathrm{~V} \text { to } \\ & 132 \mathrm{~V} \end{aligned}$ | 5A, 250V AGC/3AG Fast-blow (UL 198.6) | AGC/3AG | ANSI C73.11 NEMA 5-15-P UL 198.6 |
|  | Option A1 | $\begin{gathered} \text { EURO } \\ 240 \mathrm{~V} \\ 10-16 \mathrm{~A} \end{gathered}$ | 230 V | $\begin{aligned} & 180 \mathrm{~V} \text { to } \\ & 250 \mathrm{~V} \end{aligned}$ | 5A, 250V AGC/3AG Fast-blow (UL 198.6) | AGC/3AG | $\begin{aligned} & \text { CEE(7). II. IV. VII } \\ & \text { IEC } 83 \\ & \text { IEC } 127 \end{aligned}$ |
|  | Option A2 | $\begin{gathered} U K^{\mathrm{a}} \\ 240 \mathrm{~V} \\ 6 \mathrm{~A} \end{gathered}$ | 230 V | $\begin{aligned} & 180 \mathrm{~V} \text { to } \\ & 250 \mathrm{~V} \end{aligned}$ | 5A, 250V <br> AGC/3AG <br> Fast-blow <br> (UL 198.6) | AGC/3AG | BS 1363 IEC 83 IEC 127 |
|  | Option A3 | $\begin{aligned} & \text { Australian } \\ & 240 \mathrm{~V} \\ & 10 \mathrm{~A} \end{aligned}$ | 230 V | $\begin{aligned} & 180 \mathrm{~V} \text { to } \\ & 250 \mathrm{~V} \end{aligned}$ | 5A, 250V AGC/3AG Fast-blow (UL 198.6) | AGC/3AG | $\begin{aligned} & \text { AS C112 } \\ & \text { IEC } 127 \end{aligned}$ |
|  | Option A4 | North American 240V 15A | 230 V | $\begin{aligned} & 180 \mathrm{~V} \text { to } \\ & 250 \mathrm{~V} \end{aligned}$ | 5A, 250V AGC/3AG Fast-blow (UL 198.6) | AGC/3AG | ANSI C73.20 <br> NEMA 6-15-P <br> IEC 83 <br> UL 198.6 |
|  | Option A5 | $\begin{aligned} & \text { Switzerland } \\ & 220 \mathrm{~V} \\ & 6 \mathrm{~A} \end{aligned}$ | 230 V | $\begin{aligned} & 180 \mathrm{~V} \text { to } \\ & 250 \mathrm{~V} \end{aligned}$ | 5A, 250V AGC/3AG Fast-blow (UL 198.6) | AGC/3AG | SEV <br> IEC 127 |

${ }^{\text {a }}$ A 6A, Type C fuse is also installed inside the plug of the Option A2 power cord.
${ }^{\mathrm{b}}$ Reference Standards Abbreviations:

ANSI-American National Standards Institute AS-Standards Association of Australia BS—British Standards Institution
CEE-International Commission on Rules for the Approval of Electrical Equipment

IEC-International Electrotechnical Commission NEMA-National Electrical Manufacturer's Association SEV-Schweizevischer Elektrotechischer Verein UL-Underwriters Laboratories Inc.

## POWER CORD

This instrument has a detachable three-wire power cord with a three-contact plug for connection to both the power source and protective ground. The power cord is secured to the rear panel by a cord-set securing clamp. The protective ground contact on the plug connects (through the power cord protective grounding conductor) to the accessible metal parts of the instrument. For protection against electrical shock, insert this plug into a powersource outlet that has a properly grounded protectiveground contact.

Instruments are shipped with the required power cord as ordered by the customer. Information on the available power cords is presented in Table 2-1, and part numbers are listed in "Options and Accessories" (Section 7). Contact your Tektronix representative or local Tektronix Field Office for additional power-cord information.

## INSTRUMENT COOLING

To prevent instrument damage from overheated components, adequate internal airflow must be maintained. Before turning on the power, first verify that air-intake holes on the bottom and side of the cabinet and the fan exhaust holes are free of any obstruction to airflow. The scope has a thermal cutout that will activate if overheating occurs. The scope shuts down immediately with no attempt to save waveforms or front-panel conditions if a cutout happens. Power will be disabled to the scope until the thermal cutout cools down, at which time the power-on sequence is redone. The resulting loss of the last frontpanel and waveform data will cause the power-on self test to fail and is indicated to the user by a failed CKSUMNVRAM test (number 6000 in the main EXTENDED DIAGNOSTICS menu). The cause of the overheating must be corrected before attempting prolonged operation of the scope. Pressing the MENU OFF/EXTENDED FUNCTIONS button restores the scope to the normal operating mode.

## START-UP

This instrument automatically performs power-up tests each time the instrument is turned on. These tests provide the highest possible confidence level that the instrument is fully functional. If no faults are encountered, the instrument
will enter the Scope mode in the either ACQUIRE or SAVE Storage mode, depending on the mode in effect when it was powered off.

If tests are failed, the scope displays the Extended Diagnostics menu. If the failure is in the range of 1000 5300 and the message "HARDWARE PROBLEM-SEE SERVICE MANUAL." is displayed with the menu, see "Diagnostics" in Section 6 for more information. If the failure is in 1000-5300 range, but "RUN SELF CAL WHEN WARMED UP" is displayed, the SELF CAL procedure should be executed from the EXTENDED FUNCTIONS menu (wait for the NOT WARMED UP message to disappear from the SELF CAL menu). If failures persist after the SELF CAL is run (the "HARDWARE PROBLEM-SEE SERVICE MANUAL" message will be displayed), see "Diagnostics" in Section 6 for more information.

Failure of a test in the range of 7000 to 9300 may not indicate a fatal scope fault. Several conditions can occur that will cause a non-fatal failure of the tests. The scope will display "RUN SELF CAL WHEN WARMED UP" to indicate a SELF CAL should be performed. If SELF CAL does not clear the failure ("HARDWARE PROBLEM-SEE SERVICE MANUAL" is displayed), the scope may still be usable for your immediate measurement purposes. For example, if the problem area is in $\mathrm{CH} 2, \mathrm{CH} 1$ may still be used with full confidence of making accurate measurements. Press the MENU OFF/EXTENDED FUNCTIONS button to exit EXTENDED DIAGNOSTICS and enter Scope mode.

## NOTE

The SELF CAL procedure is detailed in Section 5 of this manual. Refer to Section 6 of this manual for information on the power-up tests and the procedures to follow in the event of a failed powerup test.

A fatal fault in the operating system will cause the scope to abort. No displays are possible, and the user is notified of an abort situation only by the flashing of the Trigger LED indicators (if that is possible). Cycling the power off then back on may clear the problem, but a failure of this magnitude usually requires the scope to be referred to a qualified service person for checkout and repairs. Persistent or reoccurring failures of the power-on or self-diagnostic tests should be brought to the attention of a qualified service person at the first opportunity. Consult your service department, your local Tektronix Service Center, or nearest Tektronix representative if further assistance is needed.

## POWER-DOWN

## NOTE

POWER INTERRUPTION TO THE INSTRUMENT WHEN THE SELF-CALIBRATION ROUTINE IS EXECUTING INVALIDATES THE INSTRUMENT CALIBRATION CONSTANTS. Upon such an interruption, the instrument sets an internal flag denoting that SELF CAL was running at shutdown. When power is reestablished, the scope will display "RUN SELF CAL WHEN WARMED UP". When the "NOT WARMED UP" message disappears from the SELF CAL menu, the user MUST perform a SELF CAL to escape the EXT DIAG menu (the $t$ menu button MUST be used to access the SELF CAL menu-see Section 6 for more information). If failures persist after the SELF CAL is performed, refer the instrument to qualified service personnel.

For a normal power-off from the scope mode, an orderly power-down sequence retains the SAVE and SAVEREF waveforms, the current front-panel control settings, and any stored front-panel settings. If a power-off or transient power fluctuation occurs during SELF CAL, or EXTENDED CALIBRATION, or the instrument shuts-down at any time due to overheating, the normal power-down sequence is not executed. The result is loss of stored calibration constants or last front-panel control settings (or both) and a failure of the next power-on self-test (60006400 range). If front panel, sequencer, or stored waveform information was lost, the error will clear itself on the next power-down/power-up cycle. If calibration constants were lost the instrument will display information indicating if calibration is needed.

If power is momentarily interrupted, starting the poweroff sequence, but is reestablished before the sequence completes, the scope will redo the power-on procedure. If the scope is in the middle of a waveform acquisition when power interruption occurs, the waveform data will not be saved, and the invalid waveform data display will be seen when power-on has completed. Press ACQUIRE to restart the acquisition and obtain valid waveform data.

## REPACKAGING FOR SHIPMENT

It is recommended that the original carton and packing material be saved in the event it is necessary for the instrument to be reshipped using a commercial transport carrier. If the original materials are unfit or not available, then repackage the instrument using the following procedure.

1. Use a corrugated cardboard shipping carton having a test strength of at least 275 pounds and with an inside dimension at least six inches greater than the instrument dimensions.
2. If the instrument is being shipped to a Tektronix Service Center, enclose the following information: the owner's address, name and phone number of a contact person, type and serial number of the instrument, reason for returning, and a complete description of the service required.
3. Completely wrap the instrument with polyethylene sheeting or equivalent to protect the outside finish and prevent entry of harmful substances into the instrument.
4. Cushion instrument on all sides using three inches of padding material or urethane foam, tightly packed between the carton and the instrument.
5. Seal the shipping carton with an industrial stapler or strapping tape.
6. Mark the address of the Tektronix Service Center and also your own return address on the shipping carton in two prominent locations.

## THEORY OF OPERATION

## SECTION ORGANIZATION

This section of the manual is divided into three subsections, with each subsection increasing in detail. The first subsection is the "Simplified Block Diagram Description" which contains a general summary of instrument operation by diagram. A simplified block diagram accompanies the text. Subsection two is the "Detailed Block Diagram Description" which discusses the circuit functions in greater detail and provides a more in-depth look at the acquisition system. A detailed block diagram is located in the foldout pages at the rear of this manual. Generally, both block diagram descriptions follow the signal-flow path as much as possible and not the schematic diagram number order as is done in the "Detailed Circuit Description".

Subsection three is the "Detailed Circuit Description" which discusses the circuitry shown in the schematic diagram foldouts, also located at the rear of this manual. The schematic diagram number associated with each description is identified in the text and is shown on the block diagrams. For best understanding of the circuit being described, refer to the appropriate schematic diagram and the block diagrams. The order of discussion in the circuit descriptions follows the schematic diagram number order.

## INTEGRATED CIRCUIT DESCRIPTIONS

Digital logic circuits perform most of the functions within the instrument. Functions and operation of the logic circuits are shown using logic symbols and terms. Most logic functions are described using the positive-logic convention. Positive logic is a notation system in which the more positive of the two logic levels is the HI (or 1) state; the more negative level is the LO (or 0 ) state. Voltages that constitute a HI or a LO state vary between specific devices. Refer to the device manufacturer's data book for specific electrical characteristics or logical operation of common parts.

The functioning of linear integrated circuit devices in this section is discussed using waveforms or other techniques such as voltage measurements and simplified diagrams, where required, to illustrate their operation.

## SIMPLIFIED BLOCK DIAGRAM DESCRIPTION

This discussion is of the block diagram shown in Figure 3-1.

## Attenuators and Preamplifiers (diagram 9)

ATTENUATORS. The Attenuators are settable to 1X, 10X, or 100X attenuation, to reduce the input signal level to within the dynamic range of the Preamplifiers. Input coupling for the signal to the Attenuators may be either AC or DC with $1 \mathrm{M} \Omega$ termination or DC with $50 \Omega$ termination. Attenuator and coupling switching are controlled by the System $\mu \mathrm{P}$ using register-activated magnetic-latch switches.

PREAMPLIFIERS. The Preamplifiers provide switchable gain setting and buffering of the attenuated input signal. Single-ended input signals are converted to double-ended (differential) output signals. Variable Vertical Mode gain, vertical position, and DC Balance are controlled by input signals to the Preamplifiers. The System $\mu \mathrm{P}$-controlled gain in combination with the switchable attenuator settings allow the complete range of available VOLTS/DIV switch settings from 2 mV to 5 V to be obtained. Trigger pickoffs provide a sample of the input signal to the trigger system for use as a triggering signal source. With the Video Option installed, a Channel 2 pickoff signal is supplied from the Preamplifiers as a trigger signal source. Also, a Channel 2 Offset signal used to control the back-porch clamping is provided from the Video Option to the Channel 2 Preamplifier.

## Peak Detectors and CCD/Clock Drivers (diagram 10)

PEAK DETECTORS. Additional buffering of the signal to the CCDs is provided by the Peak Detectors for all acquisition modes. The bandwidth of the input amplifiers of the Peak Detectors is switchable for FULL, 100 MHz , and 20 MHz bandwidths. In Envelope acquisition mode, dual min-max Peak Detectors detect and hold the minimum and maximum peak signal amplitudes that occur between sampling clocks. Those min and max signal values are then applied to the CCDs for sampling. Control data from the System $\mu \mathrm{P}$ controls the bandwidth selection, and peak detector clock signals multiplex the signal samples from the Peak Detectors to the CCDs. A calibration signal input is provided to the Peak Detectors for use in automatic calibration and diagnostic testing of the acquisition system.

Common-mode adjust circuitry on the output of the Peak Detectors is used to control the overall gain of the Peak Detector/CCD acquisition subsystem. Using digital signals to the DAC system, analog voltages are generated that set the gain of the Common-mode adjust amplifiers. These amplifiers monitor the dc common-mode level of the Peak Detector outputs and match it to the control gain level set by the System $\mu \mathrm{P}$. That dc level sets the CCD signal gain.

CCD/CLOCK DRIVERS. The CCDs are fast analog shift registers that can hold more that enough samples to fill the complete waveform record of 1024 samples per channel. The extra samples are used to account for the uncertainty of the trigger point location in the 32 samples stored in the input register. Once a trigger occurs, the samples not needed to fill the waveform records are basically discarded. For fast signals, waveform samples are stored very rapidly and then shifted out at a rate that can be handled by the A/D Converter. When the sample rate is slow enough to allow direct conversion of the input samples, a Short Pipeline mode is used to shift samples directly through the CCD registers. The Clock Driver portion of the devices produces the phase clocks that shift the analog data through the CCD registers. Other clocks used to sample the signal and transfer the samples into and out of the CCD arrays are generated in the CCD Clock and System Clock circuits (diagrams 11 and 7 respectively).

## CCD Output (diagram 14)

The differential signals from the four sides of both channels of the CCD arrays are combined and multiplexed onto a single data line to the A/D Converter. The output clocking is referenced to the sample and phase clocks to maintain the correct data timing relationships of the samples. Waveform data samples are therefore stored in the correct Acquisition Memory locations after being digitized.

## A/D Converter and Acquisition Latches (diagram 15)

A/D CONVERTER. The combined samples of analog signals are converted to eight-bit data bytes by the $A / D$ Converter. In Envelope Mode, the data bytes are applied to two magnitude comparators, along with the previous maximum and minimum data bytes to determine if it is greater in magnitude than the last maximum or minimum. If a new data byte is greater, the new data byte is latched into the Acquisition Latches; otherwise, latching does not occur. Clocking to direct the signals into the Acquisition


Figure 3-1. Simplified block diagram.

## Theory of Operation-2440 Service

Latches comes from the System Clock circuit and is referenced to the Output Clocks to maintain the correct data input to the magnitude comparators for making the Envelope min-max comparisons.

ACQUISITION LATCHES. For Normal and Average acquisitions, the data bytes are passed directly through the Acquisition Latches to the Acquisition Memory where they are stored temporarily before transfer to Waveform Processor Data Bus and the Waveform Processor Save Memory. The Envelope acquisition waveform bytes in the Acquisition Latches are the maximum and minimum data point values that occurred in the sampling interval. When the SEC/DIV setting reaches the maximum sampling rate, only one min-max pair is present during a sampling interval; and, in that case, the Envelope data byte comparisons are done by a firmware routine as the data is transferred from the Save Memory to the Display Memory.

## Time Base Controller and Acquisition Memory (diagram 8)

ACQUISITION MEMORY. Digitized waveform data bytes are transferred from the Acquisition Latches to the Acquisition Memory under control of the Time Base Controller. The data is temporarily stored here before moving to the Waveform Processor Save Memory under control of the Waveform Processor.

TIME BASE CONTROLLER. The Time Base Controller, under direction of the System $\mu \mathrm{P}$, monitors and controls the acquisition functions. When the pretrigger samples are obtained, the digitization process is started. Samples are counted to store the correct number in the Acquisition Memory, and the trigger point is properly located in the waveform record. Among the various tasks done by the Time Base Controller, Clock signals generated by the Time Base Controller provide the acquisition rate, the calibrator frequency, and enable the Trigger circuitry to accept a trigger after the pretrigger data is acquired.

## Waveform Processor (diagram 2)

The Waveform Processor performs the high-speed data-handling operations required to produce and update the CRT displays. Waveform data is transferred from the Acquisition Memory to a "Save" Memory in the Waveform $\mu \mathrm{P}$ work space. Waveforms may be digitally added, multiplied, or averaged, as part of the display processing that the Waveform Processor does before transferring the data to the Display Memory. The Save Memory is kept alive during periods of power-off by the battery-backup system. This back-up system holds the Save waveforms, the reference waveforms and/or front-panel setups for up to three years. The waveform $\mu \mathrm{P}$ memory space and all devices on the Waveform $\mu \mathrm{P}$ address bus are addressable by the System $\mu \mathrm{P}$ via the Bus Connect circuitry for I/O operations.

The Bus Connect circuitry includes logic gating that arbitrates when the Waveform $\mu \mathrm{P}$ memory space (RAM) and addressable devices are under control of the System $\mu \mathrm{P}$. The System $\mu \mathrm{P}$ may gain control by a BUS REQUEST to which the Waveform $\mu \mathrm{P}$ issues a BUS GRANT signal; or if the Waveform $\mu \mathrm{P}$ is held reset, the System $\mu \mathrm{P}$ issues a BUSTAKE signal. The BUSTAKE is used when the System $\mu \mathrm{P}$ writes a waveform display task list into the Waveform $\mu \mathrm{P}$ Command RAM space. When the reset is then removed from the Waveform $\mu \mathrm{P}$, it does all the waveform data processing tasks given to it to do by the System $\mu \mathrm{P}$ without further need of System $\mu \mathrm{P}$ action.

## Display and Attributes Memory (diagram 16)

The 512 data points to be displayed out of the 1024 data-point record are transferred to the Display Memory from the Waveform $\mu \mathrm{P}$ Save Memory after any required processing such as adding, subtracting, multiplying, or interpolating is done. Subsequent refreshes of the display are then continually made from data stored in the Display Memory, and that memory is only updated as necessary to display different waveforms or portions of the waveform record (a new horizontal position or new waveform called up for display). The Attributes Memory holds all the VOLTS/DIV and SEC/DIV scale factors for each of the waveforms displayed. Readouts of that data are also displayed on the crt.

## Display Controller (diagram 17)

The Display Control System controls the display of the waveforms and readouts. Data bytes stored in the Display Memory are read out and D-to-A converted into vertical and horizontal current signals used to generate the waveform dots and readout characters. State-machine circuitry under control of the System $\mu \mathrm{P}$ performs all the display tasks assigned including control of the Z-Axis. The System $\mu \mathrm{P}$ and the Waveform $\mu \mathrm{P}$ are therefore free to carry on with other functions until it becomes necessary to make a display change (such as a menu or display mode change or a waveform data update). Display state-machine clocks are generated from the Time Base Controller 5 MHz clock signal.

## Display Output (diagram 18)

Horizontal and vertical signal current from the Display Controller are converted into the deflection voltage signals used to drive the crt deflection plates by the Display Output circuitry. Vector generation circuitry provides a choice of either connected waveform dots (vectors on) or a dotsonly waveform display. Display switching circuitry connects the correct deflection signals to the vertical and horizontal output amplifier for YT (vertical signal versus time), XY (horizontal signal versus versus vertical signal), or readout data. Dynamic offset correction of the vertical and horizontal output amplifiers is provided that minimizes trace shift due to intensity changes.

## System Processor (diagram 1)

The System $\mu \mathrm{P}$, under program direction, controls all the functions of the scope and coordinates the functions of the two other microprocessors (the Front-Panel $\mu \mathrm{P}$ and the Waveform $\mu \mathrm{P}$ ). The System $\mu \mathrm{P}$ has a 16 -bit address bus and a separate 8 -bit data bus. No multiplexing of the data bus is required. Addresses are decoded to access the memory-mapped devices on the data bus, and control signals generated by the System $\mu \mathrm{P}$ control communication between the $\mu \mathrm{P}$ and the bus devices. An extensive interrupt circuit enables devices on the bus to request servicing when necessary to get new instructions or take other action. A power-up reset circuit permits an orderly poweron and power-off sequence of the System $\mu \mathrm{P}$.

Permanent programming used to control the Operating System resides in the System ROM. The System ROM contains one 16 K byte $\times 8$-bit memory device and four 64 K byte $\times 8$-bit memory devices for a total of 272 K bytes of memory. A page-switching scheme is used to permit the System $\mu \mathrm{P}$ to access all the available memory addresses of ROM.

System RAM consists of a single 32 K byte $\times 8$-bit memory device. Data needing short-term storage (data used for performing various control functions) as well as data needing long-term storage (calibration constants, the front-panel setup at power down, etc.) are stored in this nonvolatile RAM. A battery-backup system maintains the data in this memory during power off.

## NOTE

> Although all the data in this memory device is backed up and is, therefore, nonvolatile, that part of the System RAM reserved for data that NEEDS to be backed up is referred to as NVRAM throughout this section. Parts of System RAM that do NOT NEED backing up are referred to as volatile RAM or just RAM.

## Front Panel Processor (diagram 3)

The Front Panel $\mu \mathrm{P}$ is a special-purpose device used to respond to switch and control changes. When a control changes, the Front Panel $\mu \mathrm{P}$ informs the System $\mu \mathrm{P}$ so that the operating state may be altered to match the requested change. Potentiometer controls are digitized to provide the necessary change data to the System $\mu \mathrm{P}$. The System $\mu \mathrm{P}$ notes the control that changed, the amount and direction of change (if a pot), and sends out the necessary commands to make the change. New settings are updated in the nonvolatile RAM so that they will be available in the event of a power-off. On a power-on, the Front-Panel $\mu \mathrm{P}$ receives instructions as to how the switches are to be interpreted and then begins scanning the front panel, watching for a control to change. The System $\mu \mathrm{P}$ is then free to carry on with other functions.

## Front Panel (diagram 4) and Auxiliary Front Panel (diagram 6)

All the buttons and knobs of the Front Panel and Auxiliary Front Panel are "soft" controls and do not directly activate a circuit function. This fact allows the switch functions and menu labels to be changed (especially the bezel buttons of the Auxiliary Front Panel which are used to make menu selections) as necessary. Buttons may be defined by the System $\mu \mathrm{P}$ to be push-push on-off, momentary contact, continuous, or toggle switches. Control changes are monitored by the Front Panel $\mu \mathrm{P}$. Potentiometer controls are digitized; and when a change occurs, the amount and direction of change is sent to the System $\mu \mathrm{P}$ to make the appropriate operational changes. Push buttons that are pressed are interpreted as to what type of switch action occurred (from the switch-type definition list) and that information is sent to the System $\mu \mathrm{P}$ to make the appropriate operational changes.

All the buttons and knobs located to the right of the crt (facing the scope) are monitored via circuitry of the Front Panel. The Auxiliary Front Panel contains the circuitry required to monitor the bezel buttons (menu selection buttons). the push buttons, and the INTENSITY knob (all located directly beneath the crt). Probe coding for the vertical-channel and external-trigger BNC connectors and the $50 \Omega$ overload circuits for CH 1 and CH 2 are also monitored via the Auxiliary Front Panel circuitry.

## System DAC (diagrams 5 and 6)

The System DAC is used in normal operation to set the various analog control voltages throughout the instrument. Such things as preamplifier gain, vertical position and centering, trigger levels, holdoff time, common-mode adjust, scale illumination, intensity of the various CRT displays, and CCD positions offsets are all controlled by the System $\mu \mathrm{P}$ via the System DAC. Digital values representing the analog voltage levels required for the various controls are written to the digital-to-analog converter (DAC) input registers where they are converted to analog voltage levels at the inputs to the Sample-and-Hold circuits. The Sample-and-Hold circuits maintain a fixed output voltage to the controlled circuit between updates by the System $\mu \mathrm{P}$.

For calibration and diagnostic purposes, the System DAC is used to send known voltage levels to various circuits. Those levels may then be adjusted to remove offsets and set gain levels to achieve analog calibration or to test the gains and offsets for diagnostic purposes.

## Acquisition Control Registers (diagram 5)

The Acquisition Control Registers are the digital control interface between the System $\mu \mathrm{P}$ and the switchable acquisition circuitry. Switching data is written to the

Registers to control the setup of the Peak Detectors, the A/B Trigger Generator, the Trigger Logic Array, and the Phase Clock Array. Additional decoding circuitry produces clocking signals used to load controlling data into Attenuator Register, the CH 1 and CH 2 Preamplifiers, and the $\mathrm{A} / \mathrm{B}$ Trigger Generator.

## Triggers and CCD Clocks (diagram 11)

TRIGGERS. The Trigger circuits detect when a trigger meeting the setup conditions occurs. Triggering signals are selectable by the A/B Trigger Generator from a choice of the following sources: $\mathrm{CH} 1, \mathrm{CH} 2$, EXT 1, EXT 2, and LINE. The Trigger Logic Array makes possible the further choices of TV Trigger (TVTG), WORD Trigger ( $\overline{\text { WDTTL }}$ ), or $A$ and $B$ Trigger. Upon receiving a valid trigger, the acquisition in progress is allowed to complete. Conditions for triggering, such as Level, Slope, Coupling, and Mode, are determined by the A/B Trigger Generator. Other triggering conditions such as delay by time, delay by events, and A and B Trigger are decided by the Trigger Logic Array which produces the output gates signaling a trigger event. The System $\mu \mathrm{P}$ sets up the operating modes for the A/B Trigger Generator and the Trigger Logic Array via the Acquisition Control Registers (diagram 5). Control signals to the Jitter Correction Ramps (RAMP and $\overline{\text { RAMP }}$ ) are generated by the Trigger Logic Array to start measuring the time between the sample clock and the trigger event. That time difference is used to correctly place the samples when repetitive sampling is used.

CCD CLOCKS. The CCD Clocks (used to move data into and out of the CCDs), the Peak Detector Clocks, the ramp-switching signals to the Jitter Correction Ramp circuits, and the trigger location bits (needed to place the trigger position with respect to the waveform data) are all generated by the Phase Clock Array. A master clock signal of 500 MHz is generated by the Phase-Locked Loop circuit and voltage-controlled oscillator. The master clock frequency needed is determined by the sampling rate at a particular SEC/DIV switch setting. Frequency dividers in the Phase Clock Array reduce the master clock frequency to the lower rates of the output clocks as determined by the System $\mu \mathrm{P}$ via the Acquisition Control Registers (diagram 5).

## Jitter Correction Ramps (diagram 12)

The Jitter Corrections Ramps work in conjunction with the Jitter Counters to detect and measure the time difference between a trigger event (that occurs randomly) and the sample clock. That time difference is used to correctly place sampled data points into the waveform record when those samples are acquired on different triggers (repetitive sampling). Two ramp generators are used, so two time measurements are made. The System
$\mu \mathrm{P}$ will determine which measurement is the one actually used. The RAMP and RAMP signals from the Trigger circuits control the start and stop of the ramp signals while the SLRMP1 and SLRMP2 signals control switching between the fast-charging current source and slowdischarging current source. Since the SLRMP signals are related to the sample clock, the amount of charge stored from the fast-charging current source before switching to the slow ramp occurs is a measure of the time difference between the trigger and the sample clock. The Jitter Counters start counting when the SLRMP signal switches to the slow ramp, and they are stopped when a comparator circuit determines that the ramp level has discharged to a fixed reference level.

## Trigger Holdoff and Jitter Counters (diagram 13)

TRIGGER HOLDOFF. The A Trigger Holdoff circuit prevents the $A / B$ Trigger Generator (diagram 11) from recognizing a new trigger event for a certain amount of delay time after an acquisition has been completed. The delay allows all of the data handling of the acquired samples to be completed before starting a new waveform acquisition. Minimum holdoff time is dictated by the SEC/DIV switch setting. A front-panel HOLDOFF control permits the user to increase the holdoff time as an aid in improving triggering stability on certain signals.

JITTER COUNTERS. The Jitter Counters (one for RAMP1 and one for RAMP2) start counting the 40 MHz clock when a START signal is received from the Jitter Counter Ramps switching circuit. That start occurs at the beginning of the slow ramp discharge. When the level of the slow ramp decreases to the fixed reference level, a STOP signal generated by a comparator in the Jitter Counter Ramps circuit halts the count. The 8 -bit count bytes held in the Jitter Counters are then read by the System $\mu \mathrm{P}$ via address-selected bus buffers as two measures of the time difference between the trigger point and the sample clock. Since the timing between the two ramps is not identical (but both times are referenced), one measurement may have been made with better slope characteristics than the other (over a more linear portion of the discharge curve). The count producing the least ambiguity is used by the System $\mu \mathrm{P}$ to correctly position the waveform samples in the memory when repetitive sampling is done.

## Calibrator (diagram 13)

The Calibrator circuitry shapes the CALCLK signal from the Time Base Controller to produce a signal with a faster rise and fall time and very precise amplitude. Frequency of the Calibrator signals changes (within limits) as the SEC/DIV switch changes. Signal amplitude is 400 mV (starting from zero), and the effective output impedance is $50 \Omega$.

## System Clocks (diagram 7)

The System Clocks circuitry produces the fixedfrequency clock signals used throughout the scope. A 40 MHz crystal-controlled oscillator circuit produces the master clock signal that is divided down to provide the various system clocks that are needed. Some of the special clocks generated are the CCD Data Clocks, used primarily to switch the analog signal samples from the CCDs to the input of the A/D Converter and switch the converted data bytes to the Acquisition Latches. The reference frequency ( 10 MHz ) to the Phase Clock Array in the CCD Clock circuitry (diagram 11) is also selected by the System Clocks circuitry. A Secondary Clock Generator state-machine circuit produces three clocking signals to the Waveform $\mu \mathrm{P}$ to control the activity of that device.

## High Voltage and CRT (diagram 19)

The High Voltage and CRT circuitry provides the auxiliary voltages needed by the CRT to produce a display. Focus, intensity, trace rotation, astigmatism, geometry, $Y$ Axis alignment, heater, and cathode-to-anode accelerating voltage are all provided by the various circuits included. These circuits are: the High Voltage Oscillator, the High Voltage Regulator, the +61 V Supply, the Cathode Supply, the Anode Multiplier, the DC Restorer, the Focus and Z-Axis Amplifiers, the Auto Focus Buffer, and the various crt adjustment potentiometers.

## System I/O (diagram 20)

The System I/O circuits provide the interfaces between the scope and external devices that may be connected. Included in the interfaces is a standard general-purpose interface bus (GPIB) that permits two-way communication between the System $\mu \mathrm{P}$ and a GPIB controller or other IEEE 488-1980 compatible GPIB devices. The GPIB interface permits waveforms, front-panel setups, and other commands or messages to be both sent and received by the scope.

A second interface is the Word Trigger circuitry used to control the word recognization patterns of the optional Word Recognizer probe. All firmware and hardware (including connectors) required for use of the Word Recog. nizer probe is supplied as standard equipment. A trigger produced by the probe (WDTTL) may be internally selected to trigger the scope, and it may be supplied to an external device via the WORD TRIG OUT connector on the rear panel.

Three BNC connectors comprise a third interface which is used to help control the AutoStep Sequencer. SEQUENCE IN is an input that accepts TTL-compatible signals for starting a sequence and stepping a paused sequence. SEQUENCE OUT is an output that issues a TTL-compatible signal upon the completion of a sequence. STEP COMPLETE issues a TTL-compatible signal to indicate when a step in sequence is complete.

Probe power connectors are an option for supplying the power requirement of active Tektronix probes. The option consists of two probe power connectors installed on the rear panel of the scope.

An audible alarm bell is provided to give the user warning of events that may require attention. GPIB errors are typical events that produce the warning bell so that a user may take notice of the error event. Another instance that causes the warning bell is an attempted call-up of an invalid operating condition from either the front panel or the GPIB. Typically, warning and error messages are also displayed on the crt to aid the user in determining the nature of the problem.

## Video Option (diagram 21)

The Video Option (Option 05) consists of additional installed hardware that enhances triggering on and viewing of composite video signals. Option 05 circuitry contains both Video Processing and Trigger Generation circuitry. Video Processing stabilizes the input signal and separates the video sync signals (horizontal and vertical sync pulses) from the video signal. A wide range of video signal levels are accommodated by using automatic gain control of the amplifier that sets the level into the sync separator. Separated sync pulses are counted to permit the user to select the line number that will produce a trigger event. Back-porch clamping is available for the Channel 2 display, and when used, it removes or reduces the level of powersupply hum that may be accompanying the composite video signal display.

## Low Voltage Power Supply (diagram 22)

The majority of the low voltages required to power the scope are produced by a high-efficiency, switching power supply. Input ac power of either 115 V or 230 V within the frequency range of 48 Hz to 400 Hz is rectified and used to drive a switching circuit at a frequency of about 50 kHz . A smaller power transformer is possible with the higher

## Theory of Operation-2440 Service

frequency switching, and much more efficient power transfer is possible. Regulation of the power to the switching transformer is controlled by a pulse-width modulator (PWM) using feedback from one of the rectifier transformer outputs. The PWM controls the on-time of the switching transistors that deliver energy to the transformer primary winding. If the feedback voltage is too low, more energy is supplied by turning on the switching transistors longer. Automatic overvoltage and overcurrent sensing circuits shut down the switching if either type of overload occurs. The ac input has an interference filter, primary line fusing, and a thermal cutout that shuts down the power supply in the event of overheating.

## Low Voltage Regulators (diagram 23)

The Low Voltage Regulators remove ac noise and ripple from the rectified output voltages from the power transformer. Each regulator automatically current limits the output and prevents the current from exceeding the normal power limits. This limiting prevents further possible damage to the power supply or other scope circuitry. Each of the power supply regulators controls its output voltage level by comparing the output to a known voltage reference level. To maintain stable and well-regulated output voltages, highly stable reference voltages are developed for making the comparisons.

# DETAILED BLOCK DIAGRAM DESCRIPTION 

## INTRODUCTION

This description of the Detailed Block Diagram (found in the "Diagrams" section of this manual) provides an overview of the operation of many of the circuits and their functions. The emphasis is on the acquisition system, and a "signal flow" approach is used as much as possible. No attempt is made in this discussion to specifically cover all the circuitry shown on the block diagram, though most is covered in general as it relates to those areas described in detail. The components discussed for each schematic diagram are generally outlined in functional blocks on their corresponding schematic diagram. These "function blocks" also appear on the "Detailed Block Diagram" within outlined areas that correspond to the schematic diagrams. Refer to both the Detailed Block Diagram and the Schematic Diagrams as needed while reading the following description.

## INPUT SIGNAL CONDITIONING AND ANALOG SAMPLING

Signals applied to the CH 1 and CH 2 input connectors are coupled to their respective attenuators. The CH 1 and CH 2 attenuators (diagram 9) are settable for 1X, 10X, and 100X attenuation, with input-coupling mode choices of AC, DC, and GND. Input termination resistance of either $1 \mathrm{M} \Omega$ or $50 \Omega$ is selectable with the DC input coupling choice. The attenuation factor, input coupling mode, and input termination settings for each input are controlled by the System $\mu \mathrm{P}$ (diagram 1) through the Attenuator Control Register (diagram 9), based on the Front Panel control settings chosen by the user.

The attenuated CH 1 and CH 2 signals are buffered by their respective Preamps (diagram 9) before they are passed on to the Peak Detectors. Preamplifier gain is controlled by the System $\mu \mathrm{P}$ using a serial control-data line via the Miscellaneous Register (diagram 1) and the DAC MUX (digital-to-analog converter multiplexer) Select circuit. Serial data is clocked into the internal register of the Preamps via the Control Register Clock Decoder (diagram 5). As with the attenuator settings, the gainsetting data output by the System $\mu \mathrm{P}$ depends on the user-selected Front Panel control settings. The range of attenuation settings coupled with the gain-control settings of the Preamps allows the complete range of available VOLTS/DIV switch settings (from 2 mV to 5 V ) to be obtained.

In addition to signal gain and input signal buffering, the Preamps convert the single-ended input signal to a double-ended differential output signal that improves the common-mode rejection ratio. Input ports used to control the DC Balance, the Variable VOLTS/DIV gain, and the Vertical Position are provided in the Preamp stages. Analog control voltages to these inputs are developed by the System DAC and routed to the Preamps via the DAC MUX/0 Sample-and-Hold circuit (diagram 5). Trigger pickoff circuits in each Preamp provide a sample of the vertical signal that may be selected by the Trigger circuitry as the trigger signal source.

The differential output signals from the Preamps are applied to their corresponding Peak Detector. Input amplifiers within the CH 1 and CH 2 Peak Detectors (diagram 10) buffer the applied signals and provide a constant input resistance of about $75 \Omega$ to those signals. The
buffered signals are then either amplified further or "peak detected" and amplified, depending on the acquisition mode setting.

The System $\mu \mathrm{P}$ controls the operating mode of the Peak Detectors via control data writes to the Acquisition Control Registers (diagram 5). Some of the resulting digital outputs drive control inputs on the Peak Detectors, while others control the enabling and disabling of the Peak Detector clock signals from the CCD (charge-coupled device) Phase Clock Generator (diagram 11). The effect of this combined action depends on the acquisition mode selected. For NORMAL and AVG (average) acquisition modes, the peak-detect function of the Peak Detectors is disabled and the input signals are only amplified for application to the CCDs. For ENVELOPE mode, however, the peak-detect portion of the internal circuitry is enabled, and the maximum and minimum signal amplitude levels that occur during a sampling interval are detected. Those maximum and minimum values are then amplified and passed on to the CCDs.

Other inputs to the Peak Detectors control the input amplifier Bandwidth Limit setting (FULL, 100 MHz , or 20 MHz ) and provide for the application of the calibration signal used for instrument calibration and self diagnostics. Calibration voltage levels applied to the Peak Detectors are generated by the System $\mu \mathrm{P}$ via the System DAC (diagram 5), DAC MUX 3, and the Cal Ampl circuit (diagram 6). The System $\mu \mathrm{P}$ selects between either the normal signal inputs or the calibration signal inputs using data written to the Acquisition Control Registers. The bandwidth of the input amplifiers of the Peak Detectors is also controlled via the Acquisition Control Registers, based on the user-selected Bandwidth Limit setting.

The signal-sampling process of CCDs (diagram 10) requires that four differential-signal pairs be available from each Peak Detector. Each CCD will use two or four of the output pairs as input signals, depending on the analog sampling mode, Briefly, the FISO sampling mode (fast-in, slow-out) requires 1088 samples to be shifted into each CCD. Clocking is such that each of the four sides of the CCD receives one-quarter of the required samples (272) on one of four synchronized clocks of the same frequency ( 62.5 MHz ) but different phase (each lags its predecessor by 90 degrees). The first pair of differential outputs are shifted into a pair of internal registers in one side of the CCD. Each of three remaining pairs of differential output signals is identical to the first pair, and each pair is shifted into two registers corresponding to its CCD side. Since, as mentioned, each CCD side is clocked at 62.5 MHz , but receives its samples on clocks ( 90 degrees) out-ot-phase, a maximum sampling rate of 250 megasamples per second is produced using only a 16 ns clocking rate. A second sampling method, called the "Short-Pipeline" mode, uses only two sides of each CCD and samples only
two of the output signal pairs from the Peak Detectors. FISO and Short-Pipeline analog sampling modes are both discussed later in this description and in the "Time Base Controller and Acquisition Memory" portion of the Detailed Circuit Description.

The Common-Mode Adjust circuits (U540A, B, C, and D, and associated components) vary, under control of the System $\mu \mathrm{P}$, the common-mode voltage levels at the output of the Peak Detectors. These voltages are adjusted at instrument calibration to optimize CCD operation.

The common-mode adjusted signal pairs (two per Peak Detector) are applied to their corresponding side of the CCDs. There, they are analog sampled. The process consists of converting the analog voltages into individual, charged "packets" having a charge directly related to the voltage amplitude of the signal sample.

At SEC/DIV settings of $50 \mu \mathrm{~s}$ and faster, the signals are sampled at a faster rate than the maximum conversion rate of the A/D Converter. This mode is the "fast-in, slowout'" (FISO) sampling mode. When enough samples have been stored in the parallel register array of the CCDs to fill a waveform record after a trigger event, sampling stops (fast-in). The stored analog samples are then clocked out of the CCD arrays at a rate that the A/D Converter can handle (hence, slow-out). For SEC/DIV settings slower than $50 \mu \mathrm{~s}$, the Short-Pipeline sampling mode is used. In Short-Pipeline, the acquisition rates are slower than the maximum digitizing rate of the A/D Converter. Samples are taken at a constant rate in Short-Pipeline mode, but to account for the slower acquisition rates needed for each successively slower SEC/DIV setting (from $100 \mu \mathrm{~s}$ to 5 s ), samples that are not needed are ignored. Short-Pipeline mode is so named because the samples do not fill all of the parallel registers within the CCDs, but take a "short" serial path through the CCDs (see the "Detailed Circuit Description" for more information).

Analog samples are continually clocked into the CCDs by the output clocks of the CCD Phase Clock Array until a valid trigger is recognized by the Acquisition System. The Time Base Controller (diagram 8) provides the reference frequency to the CCD Phase Clock Array via the Reference Frequency Selector and the Phase-Locked Loop circuit (diagram 11). Dividers in the CCD Phase Clock Array synthesize the clocking frequencies needed for saving the acquisition at the different SEC/DIV settings. The Time Base Controller also controls the acquisition mode (FISO, Short-Pipeline, or ROLL) and the storing of acquired samples into the Acquisition Memory.

At this point in the sampling process the Time Base Controller is waiting for a triggering gate from the Trigger System to complete the acquisition (see "Acquisition Process and Control'). Extra pretrigger samples acquired while waiting for a trigger will either be flushed out of the output wells of the CCDs (FISO mode) or converted and stored in the circular Acquisition Memory (diagram 8), but not moved to the Save Memory (Short-Pipeline mode). The exception to this is ROLL mode; a trigger event is not required for ROLL acquisitions. Digitized data is moved through the Acquisition System to continually update the display with each waveform data point acquired.

## ACQUISITION PROCESS AND CONTROL

To do a waveform acquisition, the System $\mu P$ addresses the internal instruction registers within the Time Base Controller and then writes the setup data into the registers. The setup data defines the acquisition mode (FISO, Short-Pipeline, or ROLL), the time base clocking rate (for the SEC/DIV setting), the trigger position, and other instructions for how an acquisition is to be made.

Once the setup data is in the Time Base Controller instruction registers, the System $\mu \mathrm{P}$ generates a strobe that starts the acquisition and turns control of the Acquisition System over to the Time Base Controller. The Time Base Controller then begins monitoring the CCD Phase Clocks to determine when an adequate number of analog samples are in the CCDs to fill the pretrigger requirements. When those samples have been obtained, the Time Base Controller enables the Trigger Logic Array (diagram 11) to accept a trigger and begins looking for a triggering gate from the Trigger Logic Array (via the CCD Phase Clock Array). This waiting period is the continuous analog sampling state for the CCDs referred to at the end of the "Input Signal Conditioning and Analog Sampling" discussion.

With the Trigger System enabled, the A/B Trigger Generator (diagram 11) monitors the selected source for a signal that meets the analog triggering criteria. Source selection and triggering criteria are controlled by serial data writes from the System $\mu \mathrm{P}$ (via the Data MUX Select circuit) based on the Front Panel settings selected by the user. When the analog triggering conditions are met, the A/B Trigger Generator gates the Trigger Logic Array. Once enabled, the Trigger Logic Array monitors other triggering criteria (Trigger Mode, Delay Time setting, Hold Off timing, etc.) to determine the actual "Record" trigger point in the waveform data record. The System $\mu \mathrm{P}$ writes data control bits defining the Trigger Logic Array operating mode to the internal registers of the Trigger Logic Array via the Acquisition Control Registers.

When the Trigger Logic Array determines that the additional triggering conditions are also met, the Time Base Controller is gated (via the CCD Phase Clock Array), and the post-trigger samples are taken (if required) to finish the acquisition. How the acquisition is completed after the trigger point is determined, depends on the analog sampling mode in effect.

## FISO Mode

For FISO mode, the CH 1 and CH 2 CCDs must each hold 1024 samples (plus some extra samples used in locating the correct trigger point). After the trigger event, the Time Base Controller counts a sampling clock from the CCD Phase Clock Generator to determine when enough post-trigger samples have been shifted into the CCDs to finish the acquisition. When the record is filled, the analog sampling process is stopped by disabling the sampling clocks output by the CCD Phase Clock Generator. Converting the stored analog information into digital data and saving it into the Acquisition Memory is then started. Both the "conversion" and "save" aspects of the acquisition process are discussed in "Analog Data Conditioning and A/D Conversion" and "Acquisition Processing and Display."

## Short-Pipeline Mode

For Short-Pipeline acquisitions, each CCD can contain only 37 samples before the "pipe" is full. This means that samples must be continuously shifted through the digitizing process and into Acquisition memory as the samples are being taken. Since the pretrigger and post-trigger distribution of the data in the acquisition record is not defined until a trigger occurs, converted data is continually stored in the Acquisition Memory. If the Acquisition Memory space should become filled before a trigger occurs, newly acquired data will simply displace the old in a circular manner (oldest data replaced first). After a trigger, the Time Base Controller counts another sampling clock to determine when enough samples have been moved into the Acquisition Memory to satisfy the post-trigger requirements and then turns the Acquisition Memory space over to the Waveform $\mu \mathrm{P}$. The Waveform $\mu \mathrm{P}$ transfers the samples into the Save Memory for eventual display.

## DATA CLOCKING TO ACQUISITION MEMORY

## FISO Mode

In FISO mode, the Time Base Controller signals the CCD Phase Clock Array (U470, diagram 11) to begin clocking waveform samples out of the CCDs. The Time Base Controller monitors the Trigger Location signals from the CCD Phase Clock Array to determine precisely where in the acquisition the trigger occurred. When the samples
not needed to fill the 1024-point waveform record have been clocked out so that only the samples properly positioned around the trigger point remain in the CCD, the Time Base Controller enables the save acquisition clocking to begin moving the digitized samples from the A/D Converter into the Acquisition Memory, thus saving the waveform record. (See "Detailed Circuit Description" for more trigger point location information.)

To do a waveform save, the Time Base Controller is selected to control writing into the Acquisition Memory via the Memory Mode Control circuit (diagram 8). The SAVEACQ clock circuitry is then enabled to pass a 4 MHz clock signal (SHIFTD200N) from the CCD Data Clock circuit (diagram 7) to do the memory writes at the FISO rate.

The memory write clock also increments the Acquisition Memory Address Counter to provide the address for writing the next data point into the Acquisition Memory. The address is latched into the Record-End Latch during each memory write so that the beginning of the acquisition record can be determined when the Acquisition Memory is accessed later.

As the samples are being moved into the Acquisition Memory, the Time Base Controller monitors clocks from the CCD Data Clock circuit to determine when the 1024 digitized samples (per each channel) are saved. The Time Base Controller then stops writing to the Acquisition Memory by disabling the write clock and switches control of the memory to the Waveform $\mu \mathrm{P}$ (again, via the Memory Mode Control circuit). The Time Base Controller then strobes the Waveform $\mu \mathrm{P}$ (diagram 2) to signal that the acquisition is complete and the waveform data is available for processing and display.

## Short-Pipeline Mode

For Short-Pipeline mode, the Time Base Controller generates an enabling clock that controls the 2 MHz write clock to the Acquisition Memory. The correct enabling rate of the SAVEACQ write clock for the selected SEC/DIV setting is synthesized within the Time Base Controller, using a CCD Data Clock input to obtain the base frequency. This enabling clock turns on the controlling gate circuit to pass only two SAVEACQ clocks (via the Mode Control Circuit) to write to the Acquisition Memory, saving one digitized data point per channel (two in Envelope Mode-one max and one min per channel). Then the synthesized clock from the Time Base Controller disables the SAVEACQ clock for a certain number of clock cycles. Specifically, the number of ungated clock cycles equals the SEC/DIV setting divided by $50 \mu \mathrm{~s}$, i.e., four clock cycles at a SEC/DIV setting of $200 \mu \mathrm{~s}$. Therefore, the samples saved in the Acquisition Memory in Short-Pipeline mode produce a constant 50 samples per horizontal division when displayed, regardless of the SEC/DIV setting.

The remainder of the Short-Pipeline save operation is similar to a FISO save. The Acquisition Memory Address Counter is incremented by the clock that writes data to the memory as in FISO, but at the synthesized rate rather than at the 4 MHz FISO rate. As in FISO, the Trigger Location information is used to determine the trigger point location. Enough samples are saved into memory after the trigger point is found to fill the post-trigger requirements before turning control over to the Waveform $\mu \mathrm{P}$.

## ANALOG DATA CONDITIONING AND A/D CONVERSION

All four pairs of the differential output signals from the CH 1 and CH 2 CCDs are applied to the inputs of the corresponding pairs of Gain-Cell amplifiers (diagrams 14 and 14a). Each amplifier (there are two Gain-Cell amplifiers on each of the four Gain-Cell boards) converts the differential signal clocked to its inputs to a single-ended output signal. That signal is used to drive the input of a corresponding Sample-and-Hold circuit (also shown on diagram 14).

The CCD Data Clocks and the CCD Output Sample Clocks (diagram 7) control the timing between when the signals are coupled to their corresponding Sample-andHold circuits and when the Sample-and-Hold circuit outputs are coupled to the single analog input of the A/D Converter (diagram 15). Briefly for FISO mode, the timing is as follows:

1. A CCD Output Sample clock gates the outputs of all four CH 1 Gain-Cell amplifiers to the input of their associated Sample-and-Hold circuit. There, the input levels are sampled, and the gating is then disabled to hold the sampled level on the Hold capacitors. One of the CH 1 Sample-and-Hold output circuits is then gated on to pass the sample level to the $A / D$ Converter for digitization.
2. While the output level of the first CH 1 Sample-andHold is gated to the A/D Converter, a CCD Output Sample clock gates the outputs of all four CH 2 Gain-Cell amplifiers to their corresponding CH 2 Sample-and-Hold circuits. Both the first CH 1 Sample-and-Hold outputs and the inputs to the CH 2 Sample-and-Hold circuit are then ungated, and the first CH 2 Sample-and-Hold output circuit is gated on to pass its held signal level to the A/D Converter.
3. The first CH 2 output is then ungated, and the second CH 1 Sample-and-Hold output and the second CH 2 Sample-and-Hold output are gated on in succession to couple their held levels to the A/D Converter. This multiplexing process continues until the third and fourth

Sample-and-Hold outputs of both CH 1 an CH 2 are gated in turn to the $A / D$ Converter. The cycle then repeats until 1024 samples from all four sides of both CCDs have been converted.

## nOTE

The samples are clocked through each side of the CCD at a 500 kHz rate, resulting in an output sampling rate of 2 MHz per channel. Also note that the 8-to-1 gating of the two channels and their respective outputs results in a 4 MHz timemultiplexed (8-to-1) signal to the A/D Converter.

For Short-Pipeline sampling mode, the gating for the inputs to the Sample-and-Hold circuits is the same as in FISO mode. However, since only one side of each CCD is used per channel, only one pair of differential outputs (per CCD) and the corresponding Gain-Cell amplifier and Sample-and-Hold circuits transfers valid waveform samples to the A/D Converter. The Short-Pipeline mode save-acquisition clocking ensures that only the valid converted data is saved (see "Short-Pipeline Mode" in "Acquisition Process and Control"). Observe, however, that the signal to the $A / D$ Converter is still a 4 MHz timemultiplexed signal, but with invalid data half of the time. Since the invalid data is, in effect, discarded by the ShortPipeline Mode save-acquisition clocking, the A/D Converter continues to operate at a constant 4 MHz conversion rate as in FISO mode.

The time-multiplexed signal is applied to the input of the A/D Converter circuit for digitization. The System Clocks circuit (diagram 7) provides a 4 MHz clock to the converter, for a 4 MHz data-conversion rate of the input signal. The resulting digital output byte is applied in four 8 -bit bytes to the Acquisition Latches (diagram 15).

For Normal and Average Acquisition Modes, data is clocked into the Acquisition Latches by another 4 MHz clock time-shifted from the 4 MHz clock used by the $A / D$ Converter. Enabling of the outputs of the Acquisition Latches is controlled by the CCD Data clocks in a sequence that ensures that the data clocked out from the enabled latch corresponds to the CCD side and Sample-and-Hold circuit that provided it. The 8 -bit sample bytes are then saved in Acquisition memory in the same order they were obtained. This "structured" method for saving acquisitions keeps the data in the correct time sequence for display.

For Envelope Mode, the Time Base Controller disables continuous gating of the 4 MHz clock to the Acquisition Latches. This action turns over the gating of that clock to the Envelope Min-Max Comparators (diagram 15). With the 4 MHz clock ungated, the CCD Data Clocks will
continue to control the enabling of the outputs of the acquisition latches as described, but the new data bytes are not continually clocked into the latches. The result is that only the data bytes clocked in by the Envelope MinMax Comparators are sequentially clocked to the Envelope Data bus in the following manner: CH 1 max, CH 2 max, CH $1 \mathrm{~min}, \mathrm{CH} 2 \mathrm{~min}$. This is the same order in which the analog samples are clocked into the $A / D$ Converter.

The output of the A/D Converter is fed to the Envelope Min-Max Comparators (diagram 15). The outputs of the Acquisition Latches are also fed back to those comparators. Due to the previously described timing action of the CCD Data Clocks, the newly digitized minimum or maximum value from the Peak Detectors (see "Input Signal Conditioning and Analog Sampling") is compared to the last value latched into the Acquisition Latch that corresponds to the new point. If the newly acquired point is outside the previous min or max value, the appropriate Envelope Min-Max Comparator gates the 4 MHz clock, and the new data byte is latched into the corresponding acquisition latch.

## ACQUISITION PROCESSING AND DISPLAY

## Data Transfer to SAVE Memory

Once the 1024 digitized signal bytes per channel are in Acquisition Memory, the Time Base Controller ungates the SAVEACQ clock and switches the the Memory Mode Control circuit to the Waveform $\mu \mathrm{P}$. It also signals the Waveform $\mu \mathrm{P}$, via the Display Status Buffer (diagram 2), that the acquisition is complete. The Waveform $\mu \mathrm{P}$ can then access the Acquisition Memory.

When the Waveform $\mu \mathrm{P}$ reads the acquisition done (ACQDN) signal from the Time Base Controller, it writes an address (via the Address Latch) which is decoded by the Register Address Decoding circuit (diagram 2). The decoded address signals the Record-End Latch (diagram 8) to enable its contents (the last addressed memory location for the stored acquisition) to the Waveform $\mu \mathrm{P}$ data bus to be read to determine the location of the last record byte stored. The Waveform $\mu \mathrm{P}$ then uses that location to determine the location of any byte in Acquisition Memory.

The Waveform $\mu \mathrm{P}$ outputs (via its Address Latch) addresses to the Address Counter for Acquisition Memory. The Address Counter is held in its load mode by the Waveform $\mu \mathrm{P}$ (via the Memory Mode Control circuit), passing the address through to Acquisition Memory. The Waveform $\mu \mathrm{P}$ enables the Acquisition Memory and provides the clocks (via the Memory Mode Control circuit)
to move stored data out to the Waveform Data bus via the Data Bus buffer. This data is written either into the Waveform Save Memory or into an internal register of the Waveform $\mu \mathrm{P}$ for processing, depending on the display requirements.

Most transfers from Acquisition Memory are straight out of Acquisition Memory, through the Waveform Data Buffer, and into a corresponding memory location in Waveform Save Memory. However, the Waveform $\mu \mathrm{P}$ sometimes disables the Waveform Data Buffer and reads the data directly into its own internal register via the Data Bus Buffer. The Waveform $\mu \mathrm{P}$ then processes it according to tasks assigned by the System $\mu \mathrm{P}$, using routines stored in its own ROM. For instance, in Envelope mode the Waveform $\mu \mathrm{P}$ will read (into a second internal register) the corresponding byte stored in Waveform Save Memory from the previous acquisition. If the new byte, stored in the first internal register, is determined to be a new max or min value, the Waveform $\mu \mathrm{P}$ uses it to replace the previous value in Waveform Save Memory.

It should be noted that the Waveform Save Memory is a paged RAM memory. The Waveform $\mu \mathrm{P}$ uses a paged address scheme to toad waveform data into one of six possible sections, depending on the source ( CH 1 or CH 2 ) or the destination (REF1, REF2, etc) of the waveform. Observe also that the Waveform Save Memory RAMs are supplied power by the Standby Circuit when instrument power is off, allowing for preservation of the waveform data stored in each of the six sections. See the "Detailed Circuit Description" for more information concerning the structuring of the Waveform Save Memory and operation of the Standby Power circuit.

## Data Transfer to Display Memory

Once an acquisition is stored in the Waveform Save Memory, it must be moved to the proper locations in Display Memory, from where it is converted back to an analog signal for display. The Waveform $\mu \mathrm{P}$ updates each section of Display Memory at the proper time, based on internal routines stored in Waveform Processor ROM and timing supplied by the Secondary Clocks via the Waveform Processor Clock and Bus Grant Decoding circuit. The Waveform $\mu \mathrm{P}$ also writes attribute changes (such as changes in horizontal position) to the Display Memory (when assigned the task by the System $\mu \mathrm{P}$ ).

The Waveform $\mu \mathrm{P}$ addresses (in parallel) both the Waveform Save Memory and the Display RAMs via the Address Multiplexer (diagram 17). The System $\mu \mathrm{P}$ gates the address through to the Display Memory (the Vertical, Horizontal, and Attribute RAMs on diagram 16) via the Dispiay Control Register (diagram 17). The Waveform $\mu \mathrm{P}$ then clocks the data out of its memory into the appropriate Display RAM.

## Data Transfer to Display DACs

When the System $\mu \mathrm{P}$ initiates the display of the data stored in Display Memory, it writes (via its data bus) the starting address of that data to the Display Counter (diagram 17). It also outputs an address that latches, via the Register Select Circuit, the starting address into the Display Counter. Simultaneously, data from the System $\mu \mathrm{P}$ initiates, via the Display Control Register (diagram 17), a strobe to the Display State Machine. The Display State Machine then signals the Address Multiplexer, gating the address(es) output by the Display Counter through to Display Memory (diagram 16), and begins to gate a clock from the Display Clocks circuit to the Display Counter. The Display Counter increments for each (display) clock cycle, accessing successive addresses in Display Memory as the System $\mu \mathrm{P}$ clocks the data out of Display Memory.

The System $\mu \mathrm{P}$ uses data writes to the Mode-Control Register (diagram 17) to select which portion of the Display Memory (Vertical, Horizontal, or Attribute) or which register (Volts Cursors or Time Cursors) is selected for output to the Vertical or Horizontal DACs. The System $\mu \mathrm{P}$ also uses the Mode-Control Register to select, via the Horizontal Data Buffers, whether the waveform data in the Horizontal Ram is applied to the Horizontal or Vertical DAC, allowing either YT or XY displays.

It should be noted that the incrementing addresses supplied via the address latch are also applied to the Ramp Buffer. Since each incremental address corresponds directly to the data byte it addresses, and since the output of the Ramp Buffer (diagram 16) will be converted to a staircase waveform by the Horizontal DAC, the addresses can provide the horizontal deflection (or "ramp") necessary for YT displays.

## Data Display

Data, waveform or other, is converted to two complementary output currents by each Display DAC. These currents are analog in nature, but reflect the $\pm 256$-bit resolution of the DACs. Therefore, the current outputs are a series of discrete analog levels (or steps, if the current is varying), each level corresponding to the 8-bit byte applied to the DAC.

The differential current outputs from the Horizontal and Vertical DACs are converted to single-ended voltages at the input to the Display Output circuitry. Those voltages then drive either the corresponding Horizontal and Vertical Vector Generators (diagram 18) for vector displays or the Horizontal and Vertical Output Amplifiers directly for dot displays.

The Vector Generators consist of a High-Current Difference Amplifier, a Sample-and-Hold circuit, and a Integrator to produce the vectors that connect the sample points in the display. Signals for vectored displays are continuously sampled and held, and integrated. The input voltage integrated is the difference between the voltage level of the sample presently being held and the intergrated level of the sample immediately preceding it. This action allows a smooth transition between the individual steps for a continuous display.

A Display Mode Switcher selects between the Vector Generator signals, a dots-only signal or an envelope display signal. With Envelope mode selected, the signal is
passed through an rc integrator that produces vectors between the min-max data points of the Envelope Mode display.

The System $\mu \mathrm{P}$, based on Front Panel settings, selects the display mode for the Vertical and Horizontal Vector Generators. The selected input, either Vector, Dot, Envelope, or Readout inputs, from each Vector Generator is coupled through to its corresponding Vertical or Horizontal Output circuit (diagram 18). There they are amplified and converted from single-ended to doubleended, to drive the Vertical or Horizontal plates of the crt (diagram 19). Both Vertical and Horizontal Output circuits have voltage offset and gain adjustments and are compensated for "spot wobble" (variations in beam placement on the crt screen with variations in beam intensity) by the Intensity circuit (diagram 6) via the Spot-Wobble Correction circuit.

## DETAILED CIRCUIT DESCRIPTION

## SYSTEM PROCESSOR

The System Processor (diagram 1) is the controi center of all operations in the scope. It consists of an 8-bit microprocessor ( $\mu \mathrm{P}$ ), an 8 -bit data bus, a 16 -bit address bus, a prioritizing interrupt system, hardware address decoding, nonvolatile RAM space, and 272 K bytes of bank-switched ROM.

The System Processor circuitry also coordinates the functions of the two other microprocessors in the 2430 . the Waveform Processor and the Front Panel Processor.

## System $\mu \mathbf{P}$

System $\mu \mathrm{P}$ U640 executes instructions stored in the System ROM in order to initiate and control the various functions of this scope. Internally, the microprocessor has 16-bit data paths; externally it has an 8-bit data bus for communication and a separate 16 -bit address bus. No address/data bus demultiplexing is necessary. The $\mu \mathrm{P}$ is driven by an external $8-\mathrm{MHz}$ clock that is divided by four internally for a $2-\mathrm{MHz}$ cycle rate. The number of cycles per instruction varies from a minimum of 2 to a maximum of 20, with the average being about 4 cycles per instruction. The $\mu \mathrm{P}$ executes, on the average, $1 / 2$ MIP (Million Instructions Per second).

System $\mu$ P U640 generates three signals used to control the communication activities of external circuitry. Of these signals, E and Q are for timing purposes. The rising edge of $Q$ signals that the address on the bus is valid; data to the $\mu \mathrm{P}$ is latched on the falling edge of E . The third signal generated is the R/W signal. It is valid the same time the address is valid, and its state ( LO or HI ) determines whether an addressed device is written to or read from.

The E signal (U640 pin 34) and the Q signal (U640 pin 35) are ORed together by U840D to generate the HVMA (Host Valid Memory Address) signal. When HVMA at U840D pin 11 is HI , the address on the bus is valid. Once the external circuitry receives a valid address signal, it proceeds with the specified memory access. The signals used to enable and time these accesses are $\overline{\mathrm{RD}}$ (read) and $\overline{W R}$ (write).

The $\overline{R D}$ signal is derived from U844A, which NANDs the HVMA signal with the $\mu \mathrm{PR} / \overline{\mathrm{W}}$ signal. Inverting buffer U572C provides added driving power to the R/W signal, and inverting buffer U884B reinverts it back to its original polarity before it is applied to NAND-gate U844A. The output of U844A is the $\overline{R D}$ signal, whose falling edge indicates the start of a read cycle. The rising edge of $\overline{\mathrm{RD}}$ is coincident with the latching of the data read into $\mu \mathrm{P}$ U640.

The $\overline{W R}$ signal is derived from an inverted version of the $\mu \mathrm{PR} / \overline{\mathrm{W}}$ signal (via U572C) with a buffered $\mu \mathrm{P}$ Q signal (via U880D) NANDed by U844B. The output of this NAND-gate is a signal with a falling edge that indicates the start of a write cycle to the addressed device and a rising edge that latches data from the $\mu \mathrm{P}$ into the addressed device. The Q signal is used here instead of HVMA (as was used to generate $\overline{R D}$ to produce a data hold time of more than 100 ns as needed by the oscilloscope Time Base Controller circuitry.

## Data Bus Buffer

Data Bus Buffer U650 provides buffering of the data bus lines. It is bidirectional to enable two-way communication between the System $\mu \mathrm{P}$ and the data bus. In normal operation, jumper J 126 will connect the chip-enable pin to ground, and the buffer is enabled to transfer data. The direction of the transfer is controlled by the $\mathrm{R} / \overline{\mathrm{W}}$ signal from the System $\mu \mathrm{P}$ via inverting buffer U572C.

Moving test jumper J126 to its "KERNEL" position disables buffer U 650 and forces it to its tri-state (highimpedance output) mode. The pull-up and pull-down resistors on the data bus lines, R742, R746, and R744, place an instruction byte on the $\mu \mathrm{P}$ data bus that causes the $\mu \mathrm{P}$ to repeatedly increment the addresses placed on its address bus lines through their entire range. This procedure is a troubleshooting aid that exercises a good portion of the address-decoding and chip-select circuitry.

## Address Buffers

Address Buffers U632 and U730 provide buffering of the System $\mu \mathrm{P}$ address lines to the various addressable devices. The buffer chips are permanently enabled and provide both current buffering and electrical isolation for the address lines. Test point TP840 is provided as a source of an oscilloscope trigger signal when checking the
incrementing address lines in the forced "KERNEL" troubleshooting mode described in the "Data Bus Buffer" description.

## System ROM

The System ROM (read-only memory) stores the commands and data used by System $\mu \mathrm{P}$ U640 to execute its control functions. The System ROM is made up of one 16 K byte $\times 8$-bit memory device, U670, that contains the System $\mu \mathrm{P}$ operating system, and four page-switched, 64K byte $\times 8$-bit memory devices, U680, U682, U690, and U692 used for storage of all the additional operating routines. This gives a total of 272 K bytes of ROM space. Each ROM is individually enabled by the ROM Select circuitry, and the addressed data will only appear on the system data bus when the RD (read) signal goes LO. Since $\mu \mathrm{P}$ U640 has the capability to address only 64K locations and has to address other things besides ROM, the System ROM is split into 17 pages. Address decoders U890A, U890B, and part of PC Register U860, select the page of ROM to be read from to allow the System $\mu \mathrm{P}$ to access the entire 272 K byte ROM space.

Immediately after the power-up reset ends, $\mu \mathrm{P}$ U640 automatically tries to fetch the reset vector (the location of the first program instruction) from locations FFFE(hex) and FFFF(hex) in its address space. Anytime the System $\mu \mathrm{P}$ tries to access memory, the HVMA (host valid memory address) signal from U840D will be HI during the time the address is guaranteed to be valid. Addresses FFFE and FFFF have bits AE and AF (the two MSBs of the address bus) set HI; therefore, with the HVMA signal HI, NANDgate U870D outputs a LO that enables U890A, and a ROM1 select output is obtained from U890A for both addresses. The $\overline{\mathrm{ROM} 1}$ applied to the chip-enable input of ROM U670, along with the LO $\overline{\mathrm{RD}}$ applied to its output enable, outputs the two 8-bit data bytes from location FFFE and location FFFF onto the system data bus via bus transceiver U660. The address contained in these bytes directs the $\mu \mathrm{P}$ to the start of its program, and the program is started.

When the $\mu \mathrm{P}$ needs information from one of the other System ROMs, it writes four bits of select data into register U860. Of these bits, PAGE-BITO and PAGE-BIT1, applied to 1-of-4 Decoder U890B, select which ROM chip of ROM0 is enabled. PAGE-BIT2 and PAGE-BIT3 are the most significant bits of the ROM addresses and determine which page of the enabled ROM is addressed.

## Power-Up Reset

The Power-Up Reset circuit holds the System $\mu \mathrm{P}$ U640 reset for 100 ms after instrument power up to make sure that all instrument power supplies are operating properly. This delay ensures that the System $\mu \mathrm{P}$ begins the operat-
ing program with all electrical components in valid (defined) states after the instrument is powered on.

The Power-Up Reset circuit consists of a Texas Instruments ${ }^{\circledR}$ TL7705 Reset Controller U942 and some RC timing components. When the instrument is first powered up, the Reset Controller's RESET output is LO, holding the System $\mu \mathrm{P}$ reset at pin 37. The Reset Controller then monitors the power supply voltage at its SENSE input at pin 7. When the supply voltage at this input reaches operating tolerance, the Reset controller allows an internal current source to begin charging C938 at pin 3. After at least 100 ms (time is determined by the $10 \mu \mathrm{f}$ capacitor C938 and the 200K resistor R936), the voltage on C938 triggers an internal comparator in the Reset Controller and the Reset Controller removes the reset at pin 37 of the System $\mu \mathrm{P}$ by switching RESET HI.

The Power-Up Reset continues to monitor the power supply voltage at its SENSE input. This voltage is divided by an internal voltage divider and continuously compared against an internal voltage reference. If the power supply drops below operating limits for some reason, the Reset Controller drives $\overline{\operatorname{RESET}}$ LO to reset the System $\mu \mathrm{P}$, and, at the same time, it discharges C938. The normal powerup sequence previously described can then occur when/if the power supply comes back within limits.

In a normal power-down sequence, the System $\mu \mathrm{P}$ is notified in advance that power is going down via the nonmaskable interrupt PWRUP from the Power Up circuit (diagram 23). The power supply remains up for a minimum of 10 ms after PWRUP is issued, and the System $\mu \mathrm{P}$ uses the time to calculate and save calibration constants, frontpanel settings, and other information needed when it is repowered up. Once these "housekeeping chores" are completed, the System $\mu \mathrm{P}$ sets the PWRDOWN bit HI at pin 15 of U760, which pulls the RESIN (reset in) input of the Reset Controller LO through inverter U254E. This forces the Reset Controller to reset the System $\mu \mathrm{P}$ as previously discussed.

## NOTE

If, for some reason, the System $\mu P$ does not set PWRDOWN to trigger the reset, the Reset Controller does so when the power monitored at the SENSE input falls below operating limits (see previous discussion).

## Interrupt Logic

The Interrupt Logic circuit provides a means by which other sub-systems may interrupt the normal program execution being done by the $\mu \mathrm{P}$ to request service. Three levels of interrupts are available in $\mu \mathrm{P}$ U640. The $\overline{\mathrm{NMI}}$ (nonmaskable interrupt) that occurs at power-down has priority over the other two interrupt leveis. If either of the other
interrupts is present at the same time as the $\overline{N M I}$, the $\mu \mathbf{P}$ gives preference to the $\overline{N M I}$ and immediately branches to the power-down routine. The power-down routine performs the operations necessary for an orderly shut-down of the scope. A cyclical-redundancy checksum of the data stored in Nonvolatile RAM is calculated and stored back into that RAM. On power-up, that checksum is used to verify the validity of the parameters and settings stored in the Nonvolatile RAM. To prevent a possible 50 -ohm overload of the Channel 1 or Channel 2 input circuitry during times that the instrument is off, part of the power-down routine is to make certain that input coupling is set to a high-impedance state.

The next interrupt in priority after the $\overline{\text { NMI }}$ is the $\overline{\text { FIRQ }}$ (fast-interrupt request). It is produced by flip-flop U894A in response to a 2 ms clock signal from the Time Base circuit (diagram 8). The 2 ms clock sets the FIRQ line LO every 2 ms to signal $\mu \mathrm{P} \cup 640$ that it is time to do the timecritical tasks like updating the DAC System. When the fast-interrupt request has been serviced, the $\mu$ P clears the FIRQ latched into U894A by outputting address 6012 h . This address is decoded by 1 -of- 8 Decoder U884 to generate a CLRFIRQ (clear fast-interrupt request) signal that resets flip-flop U894A. Servicing of a fast-interrupt request differs from other interrupt requests in that the contents of only two $\mu \mathrm{P}$ registers are pushed to an internal stack (instead of all the $\mu \mathrm{P}$ registers), allowing the $\mu \mathrm{P}$ to respond faster.

The lowest priority is given to the combined signal forming the $\overline{\mathbb{R Q}}$ (interrupt request). This interrupt allows various sub-systems to get attention from the System $\mu \mathrm{P}$, NOR-gate U850B outputs a LO when any of the five conditions occur. Inputs to NOR-gate U850B are from: the GPIB (General Purpose Interface Bus), the Display circuitry, the Front Panel, the Waveform $\mu \mathrm{P}$, and the Trigger System. Of these, the latter three interrupts may be masked off (disabled) by the $\mu \mathrm{P}$ by writing LO mask bits into register U760 which are then applied to AND-gates U880A, U880B, and U880C. A LO input to one input of an AND-gate holds the associated output pin LO and prevents an interrupt signal from being gated through to NOR-gate U850B. The Waveform $\mu \mathrm{P}$ may mask the Display System interrupt (DISDN) from the System $\mu \mathrm{P}$ by placing a LO on pin 5 (MDISDN) of AND-gate U580B from register U550 (diagram 2). The Waveform $\mu \mathrm{P}$ thereby can gain first access to the Display System if it needs to do display updates before the System $\mu \mathrm{P}$ sees that the Display System is finished with its last task. When the Waveform $\mu \mathrm{P}$ is done, it writes the MDISDN interrupt HI to let the System $\mu \mathrm{P}$ know that it is finished with the Display System and the Display System is ready to be restarted.

When an IRQ interrupt is detected, the $\mu \mathrm{P}$ executes a read of location 6010h which is the address of Interrupt Register U654 (an octal buffer). That address is decoded by 1-of-8 Decoder U884 to set INTREG LO and enable

U654. The enabled buffer passes the status of the various interrupt lines at its inputs to the data bus for the $\mu \mathrm{P}$ to read. From the status bits read, the $\mu \mathrm{P}$ determines which circuit caused the interrupt and branches to the called for interrupt service routine. If more than one interrupt is pending, the System $\mu \mathrm{P}$ IRQ interrupt handling routine decides which one needs to be (or can be) handled first. The order in which it handles these interrupts depends on the current activity of the System $\mu \mathrm{P}$.

Besides interrupt status, three other status bits are read from the Interrupt Register. These are the DCOK (dc ok) signal from the power supply (check during the calibration routine register checks), BUSGRANT from the Waveform $\mu \mathrm{P}$, and FPDNRD. DCOK signifies that the various power supply voltages are within proper limits; BUSGRANT indicates that the Waveform $\mu \mathrm{P}$ has relinquished bus control in its operating space and that those addresses are now mapped into the System $\mu \mathrm{P}$ address space. FPDNRD indicates that the Front. Panel $\mu \mathrm{P}$ has read the data sent to it from the System $\mu \mathrm{P}$.

## System Address Decode Circuit

The System Address Decode circuit uses several of the system address bits, along with other control signals, to connect the System Data Bus (via the Memory Buffer) to System RAM and ROM (called System Memory, collectively) for those addresses that map to those memories. It also isolates the System Data Bus from System Memory when the System $\mu \mathrm{P}$ output addresses that map to other memory devices or certain input/output registers. Some control signals are routed from this decode circuit to other circuits and are used to decode enables for those circuits.

MEMORY BUFFER. U660, a bi-directional buffer, connects or isolates the System Data Bus from System Mernory depending on whether enabled or disabled by the output of AND-gate U580A. Direction of data transfer is controlled by WR (write) line from the system processor. When devices other than System ROM or System RAM are addressed, the buffer outputs are switched to a highimpedance state to isolate the memory devices from the data bus.

MEMORY MAP. Figure 3-2 is a memory map showing the different memory areas and the address blocks they occupy on the System Processor and the Waveform Processor Data Bus. Addresses output by the System Processor and/or the Waveform Processor access the memory indicated in the address block depending on how those addresses are decoded. Refer to Figure 3-2 as the address blocks are discussed (both here and later for the Waveform RAM).

As indicated by the memory map, addresses from $0000 \mathrm{~h}-7 \mathrm{FFFh}$ are overlapping addresses; that is, if they are originated by the System Processor, they may map to (access) memory locations or registers connected to either


Figure 3-2. Simplified Memory Map

As indicated by the memory map, addresses from $0000 \mathrm{~h}-7 \mathrm{FFFh}$ are overlapping addresses; that is, if they are originated by the System Processor, they may map to (access) memory locations or registers connected to either the System Data Bus or the Waveform Processor Data bus. If they are originated by the Waveform Processor, they access the memories indicated on the Waveform Processor Bus. The following description of the address decoding is for System Processor addresses and how the System Address Circuit outputs control signals to the Memory Buffer and to the address decoding circuit for the Waveform Processor (diagram 2). For information on how the Waveform Processor's address decoding circuitry uses these signals, see "Waveform Processor Operation" in this section.

Addresses 8000h-FFFh - All addresses from 8000h-FFFFh have AF set HI. This HI is AF is inverted (via U866C) and routed to U580A. With the inverted AF bit holding the input of AND-gate U580A LO, the output of the gate holds the Memory Buffer U660 enabled (LO). As shown in the memory map, all addresses in this range are System ROM accesses and require System Data Bus connection to the System Memory Data Bus. Locations $8000 \mathrm{~h}-\mathrm{FFFFh}$ are not used to address any other memory devices outside System memory (decoding for the paged System ROM was discussed under "System ROM" in this section).

Addresses $0000 \mathrm{~h}-7 \mathrm{FFFh}$-All addresses in this range have the AF bit set LO. With AF LO, the inverted AF signal holds a HI at one input to the dual-input AND-gate U580A. The output of this AND-gate (and the enabling of U660) is then controlled by the output of OR-gate U332A.

When the System Processor wants these address ranges to map to the Waveform Processor Data Bus (i. e., wants the System Data Bus and the Waveform Data Bus connected), it either asserts BUSREQ to the Waveform $\mu \mathrm{P}$ to receive BUSGRANT, or it asserts BUSTAKE to force BUSGRANT. BUSGRANT at the input of OR-GATE U250D forces a HI to the input of AND-gate U862B. If this is not a MAIN or MAIN2 memory access, MAIN and MAIN2 from 1-of-8 Decoder U668 are both HI and U862B output is driven HI by the BUSGRANT. This HI is coupled through U332A and U580A to disable the U660 Memory Buffer and disconnect the System Data Bus from System Memory. MAIN and MAIN2 are routed to decoding circuitry and used to connect the System Data Bus to the Waveform Data Bus (see "System $\mu \mathrm{P}$ Access" under "Waveform Processor Operation" in this section).

If either of the host RAM enables $\overline{\text { MAIN }}$ or $\overline{\text { MAIN2 }}$ are LO, the 1-of-8 decoder U668 has decoded address lines AC, AD, and $A E$ to determine that the addresses range from

4000h-4FFFh or from 7000h-7FFFh. In these address ranges, the LO host RAM enable holds off the BUS-GRANT-forced HI at the output of U250D from driving the output of AND-gate U862B HI. If the System Processor is accessing these locations in Waveform Processor RAM, it asserts WFRAM HI (Waveform RAM) at the input to OR-gate U332A. This HI is coupled through U332A and AND-gate U580 to disable U660 regardless of BUSGRANT, MAIN and MAIN2. BUSGRANT and WFRAM are routed to decoding circuitry to connect the System DATA Bus to the Waveform Data Bus.

If the System Processor is NOT accessing Waveform Processor RAM for the 4000h-4FFFh or 7000h-7FFFh address space, WFRAM is disabled LO. With either MAIN or MAIN2 enabled LO, the output of U862B is driven LO. This LO lets OR-gate U332A, and then AND-gate U580A, switch LO and enables Memory Buffer U660 to connect the System Data Bus to the System Memory Bus. The MAIN and MAIIN2 memories are then accessed.

If the System Processor is NOT accessing Waveform Processor RAM or a MAIN-section of System RAM, BUSGRANT and WFRAM are NOT asserted HI and MAIN and MAIN2 are not asserted LO. In this case, the output of four-input AND-gate U862A controls the enabling/disabling of the Memory Buffer. U862A combines with AND-gate U432B to form a five-input AND-gate function, with output $Y 0-Y 3$ and Y5 connected to the five inputs. If the address is in the range of 0000h-4FFFh or 5000h-5FFFh, 1-of-8 decoder U668 decodes a LO output to one of the five ANDed inputs. U862A outputs a LO which is ORed (by U250D) with the disabled BUSGRANT (LO) to hold off AND-gate U862B. The LO at the output of U862B is passed through U332A (WPRAM is LO) and U580A to enable the Memory Buffer and connect the System Data Bus to the System Memory. The LO output of U322A, CYSYS, also enables the System RAM for this Miscellaneous RAM access.

Addresses 6000h-6FFFh - Addresses in this range either access devices on the Waveform Processor bus or directly access devices on the System Data Bus. If the address is in this range, U668 decodes Y6, HMMIO LO.

Since Y6 is LO, all other outputs, including those driving the five inputs to AND-function U862A/U432B, are HI. With the five inputs to AND-function U862A/U432B all HI, its output is HI to U862. With the remaining two decoder outputs U862B, $\overline{\text { MAIN }}$ and MAIN2, set HI, AND-gate U862B outputs a HI that holds the Memory Buffer disabled for ALL HMMIO accesses. HMMIO is inverted via U866B and is routed, along with address bits A3 and A4, to decoding circuitry (Diagram 2) to determine when the System Data Bus connects to the Waveform Data Bus for HMMIO accesses.

## Host Memory-Mapped I/O

To permit the System $\mu \mathrm{P}$ to control the hardware functions of the scope, several control registers have been assigned to unique addresses within the $\mu \mathrm{P}$ address space (memory-mapped). These registers appear as blocks of read-only, write-only, or read-write memory to the System $\mu \mathrm{P}$. The data bits handled by these registers control specific hardware functions, and the commands written will not violate any hardware restrictions.

As mentioned in "System Address Decode Circuit," the block of addresses from 6000h to 6FFFh corresponds to the host memory-mapped input/output (HMMIO) block. Addresses within this block are decoded to produce a LO HMMIO signal to 1-of-8 Decoder U884 and Octal buffer U830. The three MSBs of the I/O address block and the HVMA are decoded by 1-of-8 decoder U668 to decode the I/O addresses between 6000h and 6FFFh.

One-of-eight Decoder U884 uses the HMMIO line and address bits A3 and A4 as enabling signals. Address lines $A 0$ and A1 and the R $\bar{W}$ line from the processor (via inverter U572C), select one of the eight outputs of U884 to go LO when the Decoder is enabled. Table 3-1 shows the registers accessed by this decoding.

Inverting buffer U830, enabled by HMMIO for I/O operations, applies the inverted middle bits of the address bus to various functional modules as selects. The firmware routines will allow only one of these select bits to be set LO at a time. In the selected circuit, further address decoding is enabled.
Figure 3-2 illustrates the System $\mu \mathrm{P}$ address memory map and shows the blocks assigned for memory-mapped I/O. Each of the memory-mapped I/O blocks consists of 16 consecutive addresses from 6000 h to 7000 h with various functions assigned to specific addresses. These functions include clocks, chip enables, and circuit enables. Each is explained in the descriptions of the circuits they affect.

## System RAM

The System RAM provides temporary storage of data used in execution of the various control functions of the System $\mu$ P. In addition, long-term power-off storage of system-calibration constants and front-panel settings is provided, allowing the instrument to power on in the same state it was in when it was turned off.

The System RAM consists of a single memory device. It is nonvolatile RAM, that is, data is maintained when power is off. The $\mu$ P U640 controls the direction of data flow via the $\overline{\mathrm{WR}}$ and $\overline{\mathrm{RD}}$ control lines.

Table 3-1
Host-Memory-Mapped I/O

| W/R | A1 | A0 | Output Signal |
| :---: | :---: | :---: | :--- |
| LO | LO | LO | INTREG (read Interrupt <br> Register) |
| LO | LO | HI | PMISCIN (Processor <br> miscellaneous inputs) |
| LO | HI | LO | CLRFIRQ (clears FIRQ <br> flip-flop) |
| LO | HI | HI | NC |
| HI | LO | LO | PCREG (write Processor <br> Control Register) |
| HI | LO | HI | PMISCOUT (write Misc <br> Register) |
| HI | HI | LO | TVREG (write Video Option <br> Register) |
| HI | HI | HI | WDREG (write Word Probe and <br> GPIB LED Register) |

${ }^{3}$ To clear the Fast-Interrupt Request, the $\mu \mathrm{P}$ does a read of the assigned address even through an actual register does not exist. The decoded output performs the reset function and no data is transterred.

## NOTE

Although all the data in this memory device is backed up and is, therefore, nonvolatile, that part of the System RAM reserved for data that NEEDS to be backed up (such as the calibration constants and front-panel settings) is referred to as NVRAM throughout this section. Parts of System RAM that do NOT NEED backing up are referred to as volatile RAM or just RAM.

## NOTE

The stored contents of the RAM is internally maintained by U664.

The chip-select circuit for System RAM U664 consists of Q842, Q960, CR944, and associated components. With instrument power off, no bias current for Q960 is available, and the transistor is off.

When instrument power is applied the normal power supplies provide bias currents for the chip-select string between U332A and U664. As the power supplies are coming up, operations on the address bus are undefined, which could cause U332A to try to enable U664. To prevent this, the $\overline{\text { RESET }}$ signal from the Power-Up Reset stage is applied to the base circuit of Q960 through diode CR944. This LO keeps the transistor biased off until the power-up $\overline{\text { RESET }}$ signal returns HI ; at which time the data on the address bus is stable.

With normal power on, when OR-gate U332A decodes a System RAM access, its output goes LO to turn off Q842. R956 then pulls up on the base of Q960, turning that transistor on and pulling the chip-enable pin of U664 LO to enable the System RAM. The RAM enable is removed when the output of U332A goes HI, turning Q842 back on and robbing the base current from Q960. With Q960 off, R764 pulis the chip-enable input of U664 HI to disable the RAM.

## Miscellaneous Reglsters

The Miscellaneous Registers allow the System $\mu \mathrm{P}$ to initiate and control various processes by writing control words to two address-decoded locations. The Miscellaneous Registers also contain an address-decoded buffer used to read certain bits of instrument status.

The RESET line holds all of the outputs of Processor Control Register U860 LO until the Power-Up Reset goes HI, ensuring that the functions controlled by the PC register outputs start in known states. To load U860 the System $\mu \mathrm{P}$ writes data to location 6014h, generating an address-decoded $\overline{\text { PCREG clock. This rising edge of the PCREG clock when }}$ the clock returns HI causes the data on the data bus to be written into the register. Table 3-2 illustrates the select functions of the PC Register output bits.

Operation of U760, the Processor Miscellaneous Register (PMREG), is similar to U860 just described. Data is written into the register with the PMISCOUT (processor miscellaneous outputs) clock when address 6015 h is decoded by U884. Table 3-3 explains register functions.

Table 3-2
Processor Control Register Functions

| Bit | Output Name | Output Function |
| :---: | :---: | :--- |
| $\mathbf{0}$ | PAGE-BIT0 <br> $\mathbf{1}$ | ROM enable selection signals <br> for Bank-Switched System <br> ROM |
| $\mathbf{2}$ | PAGE-BIT2 <br> PAGE-BIT3 | Select a page in <br> Bank-Switched System ROM. |
| 4 | WPRESET | Resets Waveform $\mu$ P. |
| 5 | WPKERNEL | Places the Waveform $\mu$ P in <br> "Kernel" mode for diagnostics. |
| 6 | BUSREQ | System $\mu$ P requests to take <br> control of the Waveform $\mu$ P <br> busses. |
| 7 | BUSTAKE | System $\mu$ P takes control of the <br> Waveform $\mu$ P address and <br> data busses. |
| 8 | DIAGO | Diagnostic bit 0-verifies that <br> data can be written to the PC <br> register. |

The Processor Miscellaneous buffer (PMBUF), U854, at address 6011h, allows the System $\mu \mathrm{P}$ to monitor the activities of various other circuits. By reading the data byte from location 6011h, the System $\mu \mathrm{P}$ can check for the presence of a Word-Trigger probe and for Waveform $\mu \mathrm{P}$ and Front Panel $\mu \mathrm{P}$ interrupts. For diagnostic routines and self-check, correct operation of registers U760, U860, and U754 is verified by writing known values to the diagnostic bits (DIAG0, DIAG1, and DIAG2) then reading them back. If both HI'S and LO'S can be written to and read from these diagnostic locations, fairly high confidence may be placed in the addressing and selection of the registers and their data paths.

Table 3-3
Processor Miscellaneous Register (PMREG) Output Functions

| Bit | Output Name | Output Function |
| :---: | :---: | :--- |
| 0 | MWPDN | Masks off (disables) Waveform <br> Processor Done interrupt. |
| 1 | MSYNTRIG | Masks off Synchronous Trigger <br> interrupt. |
| 2 | MFPINT | Masks off Front-Panel interrupt. |
| 3 | STEP COMP | Indicates the AutoStep <br> Sequencer has completed a <br> sequence step. |
| 4 | SEQOUT | Indicates the AutoStep <br> Sequencer has completed a <br> sequence. |
| 6 | BELL | Indicates an event occurred <br> which normally rings <br> instrument's internal warning <br> bell. |

## WAVEFORM PROCESSOR SYSTEM

The Waveform Processor System (diagram 2) performs the high-speed data-handling operations needed to produce and update displays of acquired data points on the CRT including averaging, enveloping, adding, multiplying, and interpolation of the waveform data. It accepts task information from the System $\mu \mathrm{P}$ and then carries out the assigned tasks without further need of the System $\mu$ P. When that task list has been completed, it sends an interrupt to the System $\mu \mathrm{P}$ to inform it that another list of tasks can be accepted.

The Waveform $\mu \mathrm{P}$ memory space is accessible by the System $\mu \mathrm{P}$, allowing the System $\mu \mathrm{P}$ to send commands to the Waveform $\mu \mathrm{P}$ and to read any desired result or data location especially for the GPIB I/O functions.

## Waveform $\mu \mathbf{P}$

Waveform $\mu \mathrm{P}$ U470 is a specially designed, high-speed microprocessor with a 16-bit multiplexed data and address bus and separate 12-bit instruction-address and 16-bit
instruction-data busses. The Waveform $\mu \mathrm{P}$ is clocked at 2.5 MHz and executes one instruction each clock cycle. Internally the Waveform $\mu \mathrm{P}$ uses a 32-bit wide instruction word. Therefore, to enable it to obtain a complete instruction for execution with each $\mu \mathrm{P}$ cycle, instructions are "double-prefetched." Two 16-bit halves of the instruction are fetched from the instruction bus with each cycle at a 5 MHz rate, so that the instruction words are 32 bits wide.

Initially, with power-on, WPRESET (Waveform $\mu$ P reset) from Processor Controlled Register U860 (diagram 1) will be LO, holding the processor reset via U270C. This reset remains in effect until the System $\mu \mathrm{P}$ writes a HI bit to the WPRESET output of U860 to remove the reset and enable the Waveform $\mu \mathrm{P}$. The System $\mu \mathrm{P}$ also holds the Waveform $\mu \mathrm{P}$ reset while it is updating the command list in RAM of the next task that the Waveform $\mu \mathrm{P}$ is to perform. This reset occurs at the completion of each set of tasks given to the Waveform $\mu \mathrm{P}$ and is released when the new task list is in place in the Waveform $\mu$ P Command RAM, U440.

Upon release of WPRESET, the Waveform $\mu$ P fetches the first two 16-bit words from its instruction ROMs, U480 and U490, at a 5 MHz rate and forms them into a 32-bit instruction word. Waveform $\mu \mathrm{P}$ U470 then executes the first instruction and at the same time it "prefetches" the next 32-bit word from the instruction ROM (the next instruction). The Waveform $\mu \mathrm{P}$ continues fetching instructions to carry out its internal initialization routine until that is completed, and it then looks in Command RAM at a vectored location to find the first task in the task list.

The first instruction in the task list tells the Waveform $\mu \mathrm{P}$ what is to be done. The $\mu \mathrm{P}$ then switches to the routine in ROM to get the instructions that do that job. Part of that routine might be to get the arguments for the task. When the arguments are in place, the Waveform $\mu \mathrm{P}$ then finishes the task routine. When done with the first task, the Waveform $\mu \mathrm{P}$ looks at the task list for the next task. It keeps doing the commands and arguments for each task until the entire task list is done. The last task of every task list is the WPDN task (Waveform Processor Done). Upon receiving that task, the Waveform $\mu$ P sets the WPDN bit to the System $\mu$ P Interrupt circuit HI , informing the System $\mu \mathrm{P}$ that it is finished. It then enters a "loop forever" state to wait for its next set of instructions. When the System $\mu \mathrm{P}$ checks the interrupt register and finds WPDN HI, it resets the Waveform $\mu \mathrm{P}$ and writes a new list of tasks to the Waveform $\mu \mathrm{P}$ Command RAM.

Waveform $\mu \mathrm{P}$ Operation-When the Waveform $\mu \mathrm{P}$ gains control of the waveform bus, it sequentially moves the 1024 data points for each channel ( $512 \mathrm{~min} /$ max pairs in envelope) from the Acquisition Memory (diagram 8) to the Save Memory (U350). When the Waveform $\mu \mathrm{P}$ does a display update, it selects the required data points needed for each waveform display requested (according to the mode selected) from Save Memory and moves them to the Display Memory (diagram 16). At the end of the display update, DISDN (display done) from the Display Control (diagram 17) goes HI to interrupt the Waveform $\mu \mathrm{P}$ (and the System $\mu \mathrm{P}$ if the Waveform $\mu \mathrm{P}$ is also done and permits the signal to be gated to the System $\mu \mathrm{P}$ via AND-gate U580B, diagram 1). This tells the Waveform $\mu \mathrm{P}$ that the current display cycle has completed and the next update to Display Memory may be started.

When in ENVELOPE acquisition mode with more than a one acquisition accumulation to be displayed, the data bytes stored In Save Memory are not automatically overwritten with each acquisition. As the data bytes are being transferred from Acquisition Memory to Save Memory, they are compared by the Waveform $\mu$ P. If the new data byte does not exceed the current maximum or minimum value in Save Memory location that it is being compared with, that Save Memory location is not overwritten (until the envelope acquisition is reset to start a new accumulation).

In AVG acquisition mode, data from the Acquisition Memory is averaged with the waveform data in the Save Memory, and the Save Memory is then rewritten with the averaged waveform data. Waveform adds, multiplies, expansions, and interpolations are performed by the Waveform $\mu \mathrm{P}$ on the Save Memory data prior to transfer to the Display Memory for display.

Waveform $\mu$ P Address Enabling-The 2.5 MHz System Clock signal CLK1 from the Clock Divider U710 (diagram 7) is inverted by U866E and ORed with the skewed 2.5 MHz CLK3 signal by OR-gate U264B. The timing of this ORed signal is such that the output of U264B goes HI when the address on the input pins of Waveform Address Registers U562 and U364 is guaranteed to be valid. Inverter U270B
inverts the output from the OR-gate (WVMA - waveform valid-memory address), and when that output again goes LO, the rising edge of the inverted WVMA signal on the clock input of the Waveform Address Registers latches the 16-bit address from the Waveform $\mu \mathrm{P}$ into the registers.

Address Latch-DDU 366, a dual 4-to-1 multiplexer, and Address Latches U364 and U562 couple a modified version of the 16 -bit address output by the Waveform $\mu \mathrm{P}$ (DADO-DADF) to the Waveform Processor Address Bus (WAO-WAF). Addresses latched to the Waveform Processor Address Bus remain on that bus for the entire Waveform $\mu \mathrm{P}$ cycle.

Due to its architecture, the Waveform $\mu \mathrm{P}$ outputs different address blocks than those required to access the various memories on the Waveform Processor Data Bus (see Fig. 3-2), U366 selects either address bit DADC or DADB for output to address WAB of the Waveform Processor Data Bus, depending on the condition of its three most-significant address bits, DADC, DADE, and DADF. AND-gate U276B detects when these bits are all HI and outputs a HI to the " $A$ " select input of the multiplexer. With the " $B$ " select input held HI for all Waveform $\mu \mathrm{P}$ accesses by BUSCONNECT, U366 routes DADB to address bit WB via address latch U562.

If any of the three most-significant Waveform $\mu \mathrm{P}$ address bits are Jow, DADC is coupled to address bit WB. This action translates the addresses output by the Waveform $\mu \mathrm{P}$ to those required on the Waveform Processor Bus.

If BUSCONNECT is LO, the access is a System Processor access and BUSGRANT is HI. BUSGRANT disables the Address Latches and the decoding action of U366 does not affect the address on the Waveform Processor Bus. BUSGRANT is inverted via U254B enables the Bus Connect Address Buffers to connect the System Address Bus to the Waveform Processor Bus.

Test point TP562 on address line WAA provides a trigger source for an external test oscilloscope when examining address waveforms in the Waveform $\mu \mathrm{P}$ "KERNEL" mode. As the KERNEL mode exercises address lines WAO-WAA, WAA is used as the trigger point.

Waveform $\mu \mathrm{P}$ Read/Write Enabling-Once latched, the address is removed from the bus and, depending on whether $\mu \mathrm{P}$ U470 is supposed to be reading or writing, data will be read into the processor from data bus buffers U360 and U560 or written to the WD (waveform data) bus via U360, a bidirectional data bus buffer. To read data into the processor, the HI R/W (read-write) signal is applied to NAND-gate U870C where it is NANDed with CLK1. During the half period that CLK1 is HI (CLK1 is LO), the gated output from U870C is the WRD (waveform processor read) in its LO (asserted) state. The LO is applied to the direction-enabling input of bidirectional buffer U360 via U542B. This LO enables U360 for a read from the WD (waveform data) bus, and the addressed 8 -bit word on the WD bus is applied to the center eight lines of the processor 16-bit address/data bus.

The four least significant bits (LSB) and the four most significant bits (MSB) of the data applied to the WD bus come from buffer U560, which is enabled via U250B and U250A for processor reads. The four LSBs are always LO (guard bits), while the four MSBs will be set to the same level as the WD7 bit (sign-extended) of the center eight bits. This placement of the 8-bit data in the center of the 16-bit bus provides a reasonable tradeoff between dynamic range (12 bits) and guard bits (4 bits).

To write data out of the Waveform $\mu \mathrm{P}$ to the WD bus, the WRD level applied to the direction-enabling pin of U360 will be HI. The center eight bits of the Waveform $\mu \mathrm{P}$ data bus will then be buffered onto the WD (waveform data) bus by U360 and written to the currently addressed location. During writes to the WD bus, the HI level of WRD disables buffer U560, via U250B and U250A, to isolate it from the Waveform $\mu \mathrm{P}$ address/data bus.

System $\mu$ P Access - When the System $\mu \mathrm{P}$ needs to do an access in the Waveform $\mu \mathrm{P}$ address space, it checks its software copy of PCREG to see if the Waveform $\mu \mathrm{P}$ is reset. If it is not reset, the System $\mu$ P asserts BUSREQ (bus
request) to the Waveform $\mu \mathrm{P}$ and waits until the Waveform $\mu$ P outputs a BUSACK (bus acknowledge) to OR-gate U332D. The output of U332D is the BUSGRANT signal that, when HI , disables the Waveform $\mu \mathrm{P}$ data buffers, address registers, and memory control lines.

When Waveform $\mu \mathrm{P} \mathrm{U470}$ is being held reset (inactive) and cannot possibly respond to a BUSREQ, the System $\mu \mathrm{P}$ instead asserts BUSTAKE to OR-gate U332D when it needs to take control of the Waveform $\mu \mathrm{P}$ address space. The System $\mu \mathrm{P}$ can also assert BUSTAKE during diagnostics in the event of a Waveform $\mu \mathrm{P}$ failure to release the bus after a BUSREQ is given.

With BUSGRANT asserted HI, the inverted BUSGRANT, BUSGRANT is output by inverter U254B and enables Bus Connect Address Buffers U262, U260, and U564. The enabled buffers connect the System $\mu \mathrm{P}$ address bus and control signal lines to their counterparts from the Waveform $\mu$ P. The Bus Connect Data Buffer U552, a bidirectional device, is then enabled and directed by control signals from the System $\mu \mathrm{P}$ for data transfers to and from the Waveform $\mu \mathrm{P}$ data bus.

Decoding circuitry uses the signals WFRAM, $\overline{\text { MAIN }}, \overline{\text { MAIN2 }}$, and HMMIO; System-Address bits A3, A4, and AF; and BUSTAKE/BUSGRANT to determine when to enable U552 and connect the System Data Bus to the Waveform Data Bus. The addresses that produce accesses to the Waveform RAM (and require U552 to be enabled) are shown as are noted on the memory map, Figure 3-2. (Also, see "System Address Decode," appearing earlier in this section.)

The Bus Connect Data Buffer is enabled when the output of the dual-input AND-gate U432D steps HI and the output of U254D steps LO. With BUSGRANT asserted HI, the output state of U850A depends on the state of its other input which is controlled by the output of OR-gate U850A. Any HI on U850A's inputs drives its output LO. This LO output holds the output of U432D LO and U552 disabled HI via U254D.

One input to U850A is BUSGRANT. Since BUSGRANT is HI, BUSGRANT is LO a few nanoseconds after BUSGRANT enables. While HI, BUSGRANT holds U850A's output LO, preventing transients from enabling the Bus Connect Data Buffer. After the few nanoseconds BUSGRANT has no effect on decoder operation.

If the address-bit AF is HI at the input to NOR-gate U850A, the address on the System Address Bus is between 8000hFFFFh. These addresses map only to System ROM; therefore, the access cannot be a Waveform Processor access. The HI AF-bit at the input to U850A holds its output LO and, via inverter U254D, the Bus Connect Data Buffer is disabled.

If either $\overline{\text { MAIN }}$ or MAIN2 are LO, the System Processor is accessing the 4000h-4FFFh or 7000h-7FFFh address space, and WFRAM determines whether the access is to the Waveform RAM space. If WFRAM is disabled LO at the inputs to OR gates U840A and U840B, one of the outputs of those gates will be LO, depending on which signal, MAIN or MAIN2, is also LO. The LO output will be inverted HI by either U254C or U254F, and the output of NOR-gate U850A will be LO. Again via inverter U254D, the Bus Connect Data Buffer is disabled.

If WFRAM is enabled HI , the outputs of both U840A and U840B are HI and are inverted LO by UU254F and U254C, respectively. Since this Is not a System ROM (AF-bit) or a HMMIO access, the rest of the inputs of U850A will be LO and the output of U850A will go HI. The Bus Connect Data Buffer will be enabled by the LO at the output of inverter U254A.

If HMMIO is HI at the input to U874B, the access is for the 6000h-6FFFh address space. Whether or not the access connects the System Processor the Waveform Data Bus depends on System Address Bits A3 and A4.

For 6000h-6FFFh addresses in the eight upper ranges (6018h-601Fh, 6038h-603Fh, etc.), both bits are HI; for the eight lower address ranges ( $6000 \mathrm{~h}-6017 \mathrm{~h}, 6020 \mathrm{~h}-6037 \mathrm{~h}$, etc.), at least one of the bits will be LO. With one or both of the A3 and A4 bits LO at NAND-gate U874D, its output must be HI . This HI is coupled to one input of NAND-gate U874B (the other input of U874B is held HI by HMMIO) and its output is forced LO. This output is connected to the input of U874A, an inverter-configured NAND-gate, and holds the output of the device and the input to NOR-gate U850A HI. The Bus Connect Data Buffer is held disabled as previously described.

If both A3 and A4 are HI, NAND-gate U874D's output goes LO. This LO drives the output of NAND-gate U874B HI and the output of U874A LO. With the other inputs to U850A LO, its output goes HI and enables the Bus Connect Buffer via U254D.

To summarize, the conditions that must be present for the decoding circuitry to produce an enable to the Bus Connect Data Buffer are:

1. BUSGRANT LO - Waveform $\mu \mathrm{P}$ has relinquished the busses;
2. $\overline{\text { MAIN }}$ and MAIN $\overline{\text { M }} \mathrm{HI}$ - This is not a "System RAM" Main Memory access;
3. Address bit AF is LO-This is not a "System ROM" access, and either:
a. HMMIO is LO-The address is not a System $\mu \mathrm{P}$ memory-mapped I/O location, or
b. It is a memory-mapped I/O location and address bits A3 and A4 are HI (the address is within the top eight I/O addresses ranges of the System $\mu \mathrm{P}$ ).

Addresses residing in the System $\mu \mathrm{P}$ memory space should not access the Waveform $\mu \mathrm{P}$ memory space, and are thus excluded from access by U850A and the associated input logic gates. Addresses not excluded will cause a System $\mu \mathrm{P}$ access into the Waveform $\mu \mathrm{P}$ memory space.

## Waveform $\mu$ P ROM

The Waveform $\mu$ P ROM consists of two 8 kilobyte $\times 8$-bit ROM devices connected in parallel to form an 8 kilobyte $\times$ 16-bit storage memory for Waveform $\mu \mathrm{P}$ waveform data handling commands. The Waveform $\mu \mathrm{P}$ "double-fetches" data from this ROM space by reading in two 16-bit bytes of command data during each Waveform $\mu \mathrm{P}$ clock cycle. This method of reading the commands makes the Waveform $\mu \mathrm{P}$ command memory space look like a 4 kilobyte $\times 32$-bit ROM. The 32-bit instruction word formed by the two fetches adequately defines any Waveform $\mu \mathrm{P}$ operation and allows the Waveform $\mu \mathrm{P}$ to execute one instruction for each 2.5 MHz clock cycle.

The chip-select pins of Waveform $\mu \mathrm{P}$ ROMs, U480 and U490, are both connected to a +5 V supply through R376. During normal operation, Waveform KERNEL jumper (P128) is installed, and the chip selects of both ROMs are shorted to ground and are constantly enabled.

The addresses of instructions to be read are determined by the 12 instruction-address bits output from the Waveform $\mu P$ and by the state of the 5 MHz clock. The 12 address bits from U470 are the most significant address bits for any given instruction. The 5 MHz clock applied to ROM address inputs A0 through delay line DL580 and associated components delays the least significant address bit enough delay to provide the needed data-hold time. The state of the 5 MHz clock will be LO to access the first 16 bits of an instruction word. The state of the A0 address line then goes HI , and the second half of the 32-bit instruction is obtained from the next
higher memory location. This address selection scheme is the "double-fetch" of instruction data mentioned previously in the Waveform $\mu \mathrm{P}$ description.

Removing jumper P128 disables the Waveform ROMs and places their outputs into the high-impedance state. The pull-up and pull-down resistors within resistor packs R474 and R590 place a "NOP" (no-operation) instruction byte on the instruction bus. A NOP command causes the Waveform $\mu \mathrm{P}$ to increment through the first 12 bits of its address range on the 16-bit DAD bus and through all the addresses of its IA bus. This "KERNEL" mode allows the Waveform $\mu \mathrm{P}$ address bus and address decoding to be exercised for troubleshooting and diagnostic purposes.

## Address Decode

The Address Decode circuit monitors the Waveform $\mu \mathrm{P}$ address bus to develop the appropriate enabling signals to the memory or $1 / O$ device that is to be accessed.

Block decoding is done by one-of-eight decoder U570, which uses address lines WAC-WAF to separate the addresses below 32 K into eight 4 K blocks. Decoder U570 is enabled when a valid address (WVMA HI) below 32 K (address bit WAF LO) is placed on the memory address bus by either the Waveform $\mu \mathrm{P}$ or the System $\mu \mathrm{P}$. The next three lower address lines (WAE, WAD, and WAC) determine which one of the eight outputs of the Decoder will be selected. Table 3-4 illustrates this address decoding.

Addresses 0000h-1FFFh-Accesses in this 8 k Block are mapped to U350, the Save RAM. U570, a 1-of-8 decoder, outputs a LO at either Y0 or Y1 for all addresses within this block and HIs on Y2-Y7. A LO at either Y0 or Y1 causes AND-gate U580C (functioning as a negative-logic OR gate) to output a LO SAVE enable. This LO is inverted twice via Q244 and Q332 and holds the chip-select input of Save RAM U350 enabled LO. Since this address block is the only block that accesses the SAVE memory, when other address blocks are decoded by U570 (in the descriptions to follow), Y0 and Y1 are HI and U350 disabled via Q244 and Q332.

## NOTE

The chip-select circuit between the $\overline{\text { SAVE }}$ output of U580C and RAM U350 is identical to that for the System $\mu$ P RAM (U664, diagram 1). The circuit determines chip selection during normal operation and isolates the Save RAM chip-select input when power is off.

Table 3-4
Waveform $\mu \mathbf{P}$ Address Decoding

| Address Bits |  |  | Output Signal (Active LO) |
| :---: | :---: | :---: | :---: |
| WAE | WAD | WAC |  |
| LO | LO | LO | (Y0 or Y1) AVE from NAND-gate |
| LO | LO | HI | U580C to enable the SAVE memory |
| LO | HI | LO | (Y2) DISP-Selects display memory |
| LO | H | HI | (Y3) DATA-Selects attribute memory |
| HI | LO | LO | (Y4) ACQ-Selects acquisition memory |
| HI | LO | HI | (Y5) WPCMDN/COEFFSelects either the command or the coefficient memory |
| HI | HI | LO | (Y6) WMMIO-Enables Waveform $\mu \mathrm{P}$ memorymapped I/O Decoder U540 |
| HI | HI | HI | (Y7) WPRAM2-Decoded to enable waveform processor RAM U440 |

The Save RAM is divided into four 8 K pages with only two pages used. Since the 0000h-1FFFh addresses can only address 8 K of memory, the two bits, SVPG0 and SVPG1, select which 8 K page the 0000h-1FFFh addresses (an 8 K address block) map to by controlling address bits AD and AE of U350. These lines, in turn, are controlled by the two lower Waveform Data Bus bits WD0 and WD1 via the Interrupt Latch U550.

Normally, SVPG0 and SVPG1 are always set Hl allowing the 8 K address block to always address the same page. However, when the Vertical mode is ADD or MULT at the same time the Acquire mode is ENVELOPE, additional Save memory space is required. Therefore, the Waveform $\mu \mathrm{P}$ will switch those lines LO to select another page as required. The System $\mu$ P also switches those lines via the Waveform Data Bus when running internal diagnostic checks on the Save RAM.

Writing to or reading from any of the Waveform $\mu \mathrm{P}$ RAM space is done via bidirectional Bus Buffer U352. When Save RAM U350 is selected by the SAVE line going LO, U352 is also enabled via AND-gate U580D. The state of the WWR (waveform write) control line determines the direction of the data transfer.

Addresses 2000h-4FFFh and 6000h-6FFFh-Addresses in these ranges select either Y2 (DISP), Y3 (DATT), Y4 ( $\overline{\mathrm{ACQ}}$ ), or Y6 ( $\overline{\mathrm{WHMMIO}}$ ). $\overline{\mathrm{DISP}}, \overline{\mathrm{DATT}}$, and $\overline{\mathrm{ACQ}}$, are used to select the Display and Display Attribute Memories (diagram 16) and the Acquisition Memory (diagram 8) respectively. WMMIO (Waveform Memory-Mapped I/O) is used to select the Register Decoding Circuitry.

With the output of U580C HI for all accesses in this group, Y0 and Y1 hold Save RAM U350 disabled (see "ADDRESSES 0000h-1FFFh" discussion). The HI SAVE also holds the input to U580D HI; the other input to U580D is held HI by the output of U432A. The output of U432A is HI because one of its inputs is held HI by Y 5 and the other held HI by Y 7 (via OR-gate U132C). The HIs at both inputs to U580D hold the Waveform Data Buffer disabled for all accesses in this group.

When WMMIO ( $6000 \mathrm{~h}-6 \mathrm{FFFh}$ ) is decoded LO, decoder U540 is enabled. U540 operates similarly to U570 and uses address lines WAO-WA4 to produce its various I/O enabling outputs. Address bits WA3 and WA4 are used as chip selects and cause the output of U540 to fall into the eight locations immediately above those of Decoder U884 (diagram 1) for System $\mu \mathrm{P}$ memory-mapped I/O.

The outputs of U540 allow the accessing processor to read the display status ( $\overline{\text { SSREG }}$ ), to read the two-byte address of the last-acquired point ( $\overline{R D M A R O}$ and $\overline{\text { RDMAR1), or to latch }}$ the present interrupt status (COMREG). (See the "Display Status Register" and "Interrupt Latch" descriptions for further explanation.)

Addresses 5000h-5FFFh - This 4 K block of addresses is decoded as an access to the Waveform Processor Coeffi-cient-Temp Memory in RAM U440. With a 5XXXh address, U570 decodes WPCMDN COEPF LO and sets its other 7 outputs HI. The LO at the input to AND-gate U432A holds its output LO, and this LO holds U440 enabled for access. (The HI SAVE disables U350 as previously described).

The LO at the output of U432A is also coupled to the input of U580D. With a LO at the input to this AND-gate, its output is LO and U352, the Waveform Data Buffer, is enabled to connect the Waveform Data Bus to the Waveform Processor RAM.

Addresses 7000h-7FFFh-Addresses in this range select WFRAM2 LO. Assuming BUSGRANT and WFRAM are both LO at the inputs to XOR-gate U130A, both inputs to OR-gate U132C are LO and its output is also LO. This LO forces the output of U432A LO and enables U440 RAM. The same LO also enables the Waveform Data Buffer via U580D to connect the Waveform Data Bus to the Waveform Processor RAM.

The System Processor can also access this address; bus by asserting BUSGRANT and WPRAM HI. The two HI inputs to XOR-gate U130A produce a LO at its output. The Waveform Data Buffer is enabled and the Waveform Data Buffer are enabled as was just described for the Waveform Processor access for this address group. BUSGRANT disables the Address Latches for the Waveform Processor and is inverted to enable the Bus Connect Circuitry to connect the System Address Bus to the Waveform Address Bus. The Bus Connect Data Buffer is enabled to connect the System Data Bus to the Waveform Data Bus.

## Waveform $\mu$ P RAM

The Waveform $\mu \mathrm{P}$ RAM is used for storage and manipulation of waveform-display data. The RAM space is divided up into four memories consisting of the 32 kilobyte $\times 8$-bit "Save Memory" RAM space, the 2 kilobyte $\times 8$-bit "Com-mand-temp" RAM space, the 2 kilobyte $\times 8$-bit "Coefficient" RAM space, and the "Interpolation" RAM space.

The 32 kilobyte $\times 8$-bit Save Memory, U350, is where the Waveform $\mu$ P places acquired waveform data that should be retained with power off. Waveforms stored in the Save RAM are retained for up to three years at room temperature with the power off.

The 8 kilobyte $\times 8$-bit RAM, U440, is where the Com-mand-Temp, Coefficient, and Interpolation RAM spaces reside. The Waveform $\mu \mathrm{P}$ uses the Command-Temp RAM space for storage of commands to the Waveform $\mu \mathrm{P}$ from the System $\mu \mathrm{P}$ and for temporary scratch-pad storage of display calculations in process. The Coefficient RAM space is used only for further scratch-pad storage. Interpolation RAM is used for storing interpolation calculation used for the MEASURE feature of this scope.

Reading from and writing to the Waveform $\mu$ P RAM selected by the Address Decode circuit are controlled by the WRD (waveform read) and $\overline{W W R}$ (waveform write) signals respectively.

## RAM Buffer

The RAM Buffer U352 allows data transfers to and from the Waveform $\mu$ P RAM to take place. The buffer is enabled by U580D when any of the Waveform $\mu \mathrm{P}$ RAM locations are addressed. Buffer direction is determined by the WWR level.

## Display Status Register

Display Status Register U542A allows the controlling processor (System $\mu \mathrm{P}$ or Waveform $\mu \mathrm{P}$ ) to read the status of the Display System operations. The address-decoded SSREG (sub-system status register) line from Decoder U540 enables buffer U542A to place the DISDN (display done) and

ACQDN (acquisition done) signals on the WD bus where they may be read. These status bits are used by the reading $\mu \mathrm{P}$ to determine when to execute the next phase of a display or acquisition sequence.

## Interrupt Latch

The Interrupt Latch (U550) allows the Waveform $\mu \mathrm{P}$ operations to interrupt the System $\mu \mathrm{P}$ for servicing and, when servicing is completed, allows the System $\mu \mathrm{P}$ to reset the interrupt.

To write data into the latch, the controlling $\mu \mathrm{P}$ addresses location 6019h, causing the COMREG line from U540 to enable U550. Data from the WD bus is written into the latch on the rising edge of the $\overline{W W R}$ pulse. The Q output from pin 10 (MDISDN) of the latch is applied to AND-gate U580B (diagram 1) where it either masks the DISDN (display done) interrupt from the System $\mu \mathrm{P}$ when it occurs or lets the interrupt pass. Masking the DISDN interrupt from the System $\mu \mathrm{P}$ permits the Waveform $\mu \mathrm{P}$ to have first access to the Display System for display updates before the System $\mu \mathbf{P}$ sees that the Display System is finished with its last task. The Q output bit on pin 15 is the WPDN (waveform processor done) interrupt and provides the Waveform $\mu \mathrm{P}$ with a way of telling the System $\mu \mathrm{P}$ that it is done with its assigned task and is ready to accept another. The output bit on pin 15 is applied to Display Status Register U542A and is used for write-readback verification of U550 and U542A during the self-check and other diagnostic routines.

The other two Q outputs, SVPG0 and SVPG1 at pins 2 and 7 respectively, control which of four 8 K pages is selected when Save RAM U350 is accessed. See "Address Decode" earlier in this section for more information.

## FRONT PANEL PROCESSOR

The Front Panel Processor (diagram 3) monitors the settings of the pots and switches of the Front Panel (diagram 4) and the Auxiliary Front Panel (diagram 6). The Front Panel $\mu \mathrm{P}$ allows quick system response to changes in front-panel settings without excessive use of time by the System $\mu$ P. The Front Panel Processor system consists of the microprocessor integrated circuit with a built-in RAM, ROM, and A/D converter (for digitizing the potentiometer wiper voltages); the handshake logic between the System $\mu \mathrm{P}$ and the Front Panel $\mu \mathrm{P}$ (to synchronize data transfer between processors); and the data bus interface to provide the actual data transfers between busses.

## Front Panel $\mu \mathbf{P}$

Front Panel $\mu$ P U700 does the reading of the front-panel pots and switches. It continuously scans the front-panel control settings and compares them against the values stored in its internal RAM. When a change is detected, the Front Panel $\mu \mathrm{P}$ issues an interrupt to the System $\mu \mathrm{P}$. The System $\mu \mathrm{P}$ then handles the interrupt and reads the changed data from the Front Panel $\mu \mathrm{P}$ to update its con-trol-setting values. The Front Panel $\mu \mathrm{P}$ also updates the current value list stored in its RAM for further use.

Front Panel $\mu \mathrm{P}$ U700 is externally clocked by the 4 MHz system clock applied to the external clock input (EXTAL). Initially, the LO state of FPRESET on the INT 2 input (pin 18) will clear all the internal registers of the Front Panel $\mu$ P. When FPRESET goes HI, the $\mu \mathrm{P}$ executes the power-up self-test instructions stored in ROM space within the $\mu \mathrm{P}$ integrated circuit. When the self test has completed, the Front Panel $\mu \mathrm{P}$ sends the diagnostic result byte to the System $\mu \mathrm{P}$ and branches to its main program. The main program routine sets up the data direction for the various port lines, sets the ANO-AN3 (analog inputs 0-3) to their analog input mode, and receives the eight front-panel configuration bytes from the System $\mu \mathrm{P}$ that define the manner in which the various front-panel switches and pots operate. It then begins scanning the front-panel pots and switches for their initial settings. After the initial values are determined and stored, the Front Panel $\mu \mathrm{P}$ sends those coded values back to the System $\mu \mathrm{P}$ in an 11-byte message (10 data bytes plus an end-of-message byte) to update the front-panel information held by the System $\mu$ P. It then begins scanning the front-panel controls for changes from the currently stored front-panel values.

To read front-panel pot settings, the internal A/D converter of the Front Panel $\mu \mathrm{P}$ performs an 8-bit, successive-approximation conversion of the analog levels applied to the ANO and AN2 inputs by a selected potentiometer. These analog input signals come from 8-input analog multiplexers U902 on the Front Panel (diagram 4) and U600 on the Auxiliary Front Panel (diagram 6). A specific pot to be read is selected by the multiplexer under control of the MUXSELO, MUXSEL1, MUXSEL2, and MUXINH (multiplexer inhibit) output lines from the Front Panel $\mu$ P. These select signals, in combination with the selected A/D (AN0 or AN2) input, define the pot being read.

To read the front-panel switches, the Front Panel $\mu \mathrm{P}$ first sets one of the front-panel switch-matrix rows LO, using the MUXSELO-MUXSEL2 outputs. It then sets its S/L (shift/load) output on pin 29 LO. The LO does a parallel load of the switch-closure data into shitt registers U904 (diagram 4) and U700 (diagram 6). The shift/load line is then set HI (shift mode), and eight shift clocks (SHCLK) are generated to move the switch-closure data serially onto the SW OUT (front-panel switch data out) or the SW OUT A (auxiliary
front-panel switch data out) lines, where it is read by the Front Panel $\mu$ P. This cycle is then repeated for the seven remaining rows of the matrix to read all the switches.

When the Front Panel $\mu \mathrm{P}$ detects a change in either a switch or a pot setting from its currently stored values, it places a code identifying which control setting changed on its PAO-PA7 outputs, and it then sets the WRTOHOST (write to host) signal HI to clock Handshake Logic flip-flop U861B. The resulting HI on the Q output of the flip-flop is the front-panel interrupt (FPINT) to the System $\mu$ P, telling it that the front-panel settings have been changed.

The System $\mu \mathrm{P}$ handles the interrupt by reading the byte from the Front Panel $\mu \mathrm{P}$; and then, via the Handshake Logic, it resets flip-flop U861B to remove the interrupt and set HOSTDNRD (host done reading) HI. This signals the Front Panel $\mu \mathrm{P}$ that the System $\mu \mathrm{P}$ has read the code identifying the changed control. The Front Panel $\mu \mathrm{P}$ then places the new control-setting value on its output bus and reasserts the front-panel interrupt using the WRTOHOST line to again clock flip-flop U861B.

The System $\mu \mathrm{P}$ then reads the changed-data bytes for the identified control(s) (either three bytes or five bytes depending on whether one or two control changes are being sent) and reasserts HOSTDNRD. Changes of up to two controls are remembered by Front Panel $\mu \mathrm{P}$ U700 so that if the System $\mu \mathrm{P}$ is busy, the control changes are not lost while the Front Panel $\mu \mathrm{P}$ is waiting to make the transfers. If more than two controls are changed before the System $\mu \mathrm{P}$ has time to read the changes, the oldest change is written over and lost.

The WRTOFP (write to front-panel processor) input to U700 at pin 3 is set LO (via the Handshake Logic) when the System $\mu \mathrm{P}$ wants to input data to the Front Panel $\mu \mathrm{P}$. The Front Panel $\mu \mathrm{P}$ then reads one byte of data from the System $\mu P$ in a manner similar to that just described for transfers from the Front Panel $\mu \mathrm{P}$ to the System $\mu \mathrm{P}$. This mode allows the System $\mu \mathrm{P}$ to change the current control configuration list stored in the limited RAM space of the Front Panel $\mu \mathrm{P}$. This list defines how the operation of pots and switches is to be interpreted (for example, momentary contact or toggle switches).

Jumper J155, connected to the $\mathrm{PC}_{7}$ and $\mathrm{PD}_{7}$ inputs, is used to enable diagnostic test routines that verify functionality of U700. The test routines may also be used to troubleshoot the Front Panel Processor system. These tests are explained in the Diagnostics portion of the "Maintenance" section of this manual.

## Handshake Logic

The Handshake Logic circuit, formed by NOR-gates U862A, B, C, and D and flip-flops U861A and B, controls and synchronizes data transfers between the System $\mu \mathrm{P}$ and the Front Panel $\mu$ P.

Data transfers between the two processors are initiated by interrupts that signal the destination processor that service is requested. When the Front Panel $\mu \mathrm{P}$ has changed-value data to give to the System $\mu \mathrm{P}$, it will place the data bytes to be given to the System $\mu \mathrm{P}$ on its $\mathrm{PA}_{0}-\mathrm{PA}_{7}$ (port A -bits 0 through 7) outputs. It then asserts WRTOHOST (write to host) HI, clocking the FPINT (front-panel interrupt) at the Q output of U861B HI.

Depending on what the System $\mu \mathrm{P}$ is doing, it may either service the interrupt request immediately, or it may wait for time to be available. When it responds to the interrupt, it does a read of the Front Panel "register" at address 6209h. The decoded FPREG signal from Trigger Holdoff Decoder U781 (diagram 12) allows OR-gates U862B and U862C to pass the WR or $\overline{\mathrm{RD}}$ signals. For a read, both input pins to U862B are LO, causing the output of U862A to go LO. This enables buffer U751, placing the data from the Front Panel $\mu \mathrm{P}$ on the System $\mu \mathrm{P}$ data bus (FP0-FP7) and, at the same time, resets flip-flop U861B. Resetting U861B removes the front-panel interrupt and sets HOSTDNRD to U700 HI.

When the System $\mu \mathrm{P}$ needs to write to the Front Panel $\mu \mathrm{P}$, it writes data to address 6209 h . This latches data from the System $\mu$ P data bus into register U742. The enable to U742 is via U862C. The latch enable also resets the Q output of flip-flop U861A LO via U862D to produce the WRTOFP (write to front-panel) interrupt to U700. Latching data into U742 immediately frees the System $\mu \mathrm{P}$ to resume other tasks, since it doesn't have to wait for the Front Panel $\mu P$ to service the interrupt.

When U700 services the interrupt by the System $\mu \mathrm{P}$, it sets $\overline{\text { FPRD }}$ (front-panel reading) LO and enables the latched data in register U742 onto the Front Panel data bus. It then reads the data into its intemal registers and asserts FPDNRD (front-panel done reading). FPDNRD going HI clocks the FPDNRD status bit from flip-flop U861A pin 6 Hl to signal the System $\mu \mathrm{P}$ that it is done reading the byte and removes the WRTOFP interupt present on U861A pin 5. Each data byte transfer from the System $\mu \mathrm{P}$ to the Front Panel $\mu \mathrm{P}$ and vice versa is done using the two handshake routines just described.

## Trigger Status Indicators

The Front Panel Trigger Status Indicators provide visual information regarding trigger slope and trigger status to the user. Data written to LED Register U741 from the System $\mu$ P turns on the LED that reflects the current trigger status. A LO output from U741 turns on the associated LED. The LED Register is enabled by a System $\mu \mathrm{P}$ write to address 6208 h . Trigger Holdoff Decoder U781 (diagram 12) produces the decoded LEDREG signal that enables data at the input pins to be latched when the WR clock goes HI .

## FRONT PANEL CONTROLS

The Front Panel is the operator's interface for controlling the user-selectable oscilloscope functions.

All of the Front Panel controls (diagram 4) are "soft" controls in that they are not connected directly into the signal path. Therefore, associated circuits are not influenced by the physical parameters (such as capacitance, resistance, and inductance) of the controls. In addition, converting the analog output levels of the potentiometers to digital equivalent values allows the System $\mu \mathrm{P}$ and the Front Panel $\mu \mathrm{P}$ to handle the data in ways that enhance control operation.

The variables defining the current settings of the control pots and the front-panel switches are stored and continually updated in Nonvolatile RAM U664 (diagram 1) by the System $\mu$. The data remains stored when the oscilloscope is turned off so that when the scope is turned on again the System $\mu \mathrm{P}$ returns to the same front-panel setup that was present when the scope was turned off.

## Front-Panel Switch Scanner

The Front Panel switches are arranged in an electrical array of eight rows and six columns. Switches are placed at row-column intersections, and when a switch is closed, one of the row lines is connected to one of the column lines through an isolation diode. Checking for switch conditions (open or closed) is done by setting a single row line LO and then sequentially checking the six columns to determine if a LO is present on any of the column lines. After each column line in a row is checked, the current row line is reset HI and the next row line is set LO to check the next six columns. A complete check of the front-panel switches consists of setting all eight row lines LO in order and performing a six-column scan for each column to check for a $L O$.

A row is selected for checking by the Front Panel $\mu \mathrm{P}$ ( U 700 , diagram 3) when it switches the MUXSEL lines (0-2) applied to multiplexer U903 to set a row line LO. To check the columns, the processor pulses its $\mathrm{S} / \overline{\mathrm{L}}$ (shift/load) select line to shift register U904 first LO and then HI. This causes a parallel load of the six column-line bits (plus the seventh and eighth bits tied HI by R934) into the shift register. The processor then generates eight shift clocks (SHCLK) to U904, serially shifting the switch data out on the SWOUT (switch data out) line. The serial data bits are applied to the PB0 input (pin 25) of the Front Panel $\mu \mathrm{P}$ to be checked. Any $L O$ bits in the column-line data tell the $\mu \mathrm{P}$ that a switch is closed. Since the Front Panel $\mu \mathrm{P}$ knows which row line it set LO, it can determine from the position of the LO bits in the serial data string which of the switches are closed.

In addition to the front-panel push-button and continuous-rotation switches connected in the switch array, there is a rate switch associated with the Horizontal Position, the CH 1 Vertical Position, the CH 2 Vertical Position, and the Cursor Position potentiometers. These switches are normally closed in the center positioning range of the associated pot. When the pot is rotated in either direction out of this range, the rate switch opens. The open switch signals the Front Panel $\mu \mathrm{P}$ that the associated control function has changed from normal (absolute) positioning to a faster, rate-change positioning mode. Rotating the pot still further into the rate region causes the associated on-screen display position to change at a still faster rate. When the pot position is returned to its center range (rate switch closed), further positioning of the associated display occurs from where the rate function positioning left off.

## Pot Scanning

The Pot Scanning circuitry, working together with the $\mathrm{A} / \mathrm{D}$ converter internal to Front Panel $\mu \mathrm{P}$ U700, produces digital values for the wiper voltages of the front-panel potentiometers and for the voltages monitored by the auxiliary front-panel circuitry. Analog multiplexer U902 selects which of the eight front-panel pots are read. (Trigger Level control R902 and Holdoff control R901 are continuousrotation potentiometers made up of two separate resistive elements each.) Analog multiplexer 4600 (diagram 6) selects the auxiliary front-panel value to be read.

Three MUXSEL control lines to multiplexers U902 and U600 select the pot or value to be read. The analog voltage level at the wiper of the pot selected by $U 902$ is output at pin 3 (AOUTO) and is applied to the Front Panel $\mu \mathrm{P}$ at pin 21 (analog input ANO). Analog voltages selected by multiplexer U600 are applied to analog input AN2. The voltage levels at these inputs are digitized, and the amount and direction of changes from the previously stored values are calculated. Changed values are stored in the internal RAM of U700 for comparison during future scans, and the change data is then relayed to the System $\mu \mathrm{P}$. That change data is used by the System $\mu \mathrm{P}$ to update its current control settings and pot values list and to update the front-panel variables in Nonvolatile RAM U664.

## SYSTEM DAC AND ACQUISITION CONTROL REGISTERS

The System DAC and Acquisition Control Registers circuitry (diagram 5) is used to set various analog reference voltages throughout the instrument and controls such things as preamplifier gain, vertical position and centering, trigger levels, holdoff time, common-mode rejection, graticule illumination, and CCD offsets.

The System DAC portion of the circuitry consists of a data latch that stores the digital value to be converted, a D/A converter that does the actual conversion, a multiplexer system to route the resulting analog voltage to the proper control circuit, and a sample-and-hold system that stores the analog levels between updates. Much of the multiplexing and sample-and-hold circuitry is shown in diagram 6, System DAC (cont) and Auxiliary Front Panel.

The other portion of diagram 5 is the Acquisition Control Registers circuitry, used by the System $\mu \mathrm{P}$ to set up the acquisition and triggering modes. The System DAC portion is described first.

## D/A Converter

The D/A Converter stage, U860, converts the digital value written into registers U850 and U851 by the System $\mu \mathbf{P}$ into two complementary output currents. (Complementary in this case means that the sum of the two currents equals a predefined value.) The digital data bits to be converted are serially clocked into the shift register from data bus line D7 (via U280). Sixteen data bits are sequentially placed on data bus line D7 and clocked into the shift register on the rising edges of 16 WR pulses (clock is via U280A and U280B). As the bits are being loaded into the registers, the DAC output current does not correspond to any useful value, but the multiplexers used to direct that output to the following stages are not enabled during loading. After all 16 bits have been clocked into the register, the inputs to DAC U860 will be at their proper levels and the DAC outputs will be valid levels. One of the multiplexers may then be enabled by the System $\mu \mathrm{P}$ using the DAC MUX enables via register U272.

Only the first 12 bits (DACO through DAC11) of the 16 bits loaded into the registers for are used for conversion data. The next three higher bits are used as 1-of-8 select bits to the four analog multiplexers that route the DAC output voltage to the proper Sample-and-Hold circuit. And finally, the MSB of shift register U851 is used in a writereadback operation that allows the operation of registers U850 and U851 to be checked by the System $\mu$ P during self checks and diagnostics.

The magnitude (range) of the DAC output currents is set by the voltages applied to pins 14 and 15 of U860. Pin $15 \mathrm{~V}_{\text {REF- }}$ is tied to ground through R761. The reference voltage to pin 14 is applied via a voltage divider (R760 and R860) between the +10 V REF supply and the output of the DAC Gain Sample-and-Hold, U660. The System $\mu \mathrm{P}$ enables self-calibration of the gain of U860 via this Sample-and-Hold circuit. Gain changes are explained in the discussion of the DAC Gain Self-Calibration circuit.

DAC I-TO-E CONVERTER. This circuit changes the differential output currents from DAC U860 into a singleended output voltage that is routed to a selected Sample-and-Hold circuit via one of the analog multiplexers.

The output currents from DAC U860 develop a voltage drop across the resistive networks at the inputs to operational amplifier U661C. The equivalent input impedance at both inputs is approximately 200 ohms; so, when both currents are equal (middle range of the DAC), the output voltage of operational amplifier U661C will be close to zero volts. An offset current is added to the non-inverting input node via R666 to precisely set the midrange value to zero volts. The gain of U661C is set by the ratio of R663 to R664, and the (calibrated) output voltage ranges from -1.36 V to +1.36 V .

DAC OFFSET. The DAC Offset level is self-adjusting and is updated via DAC Offset Sample-and-Hold U650 each time the DAC System cycles through its DAC channels to update its control levels.

At the beginning of each DAC-update cycle, the System $\mu \mathrm{P}$ writes 0800 h to DAC input shift registers U850 and U851; this corresponds to zero volts (center of the DAC range). The DAC output currents representing zero volts are converted by the DAC I-to-E Converter U661C to a voltage that is applied to U 650 via multiplexer U651. Any deviation from the desired zero-volt level causes the output of U650 (configured as an inverting integrator) to shift slightly. This applies an offsetting voltage to DAC I-to-E Converter U661C via R666 and R665 to bring its output level back to precisely zero volts.

Capacitor C655 holds the offset level constant between update cycles (every 64 ms ) to keep the proper offset for the entire DAC cycle. By updating the offiset every 64 milliseconds, offset variations that would otherwise occur over time and temperature changes are eliminated.

DAC GAIN. The DAC Gain is set during each DACupdate cycle immediately after DAC Offset is set and keeps DAC gain constant with time and temperature changes.

To set the DAC Gain, the System $\mu \mathrm{P}$ loads OF59h into DAC input registers U850 and U851 and routes the resulting output voltage to DAC Gain Sample-and-Hold U660 via multiplexer U651 pin 2. A digital input of OF59h to the DAC is supposed to produce an output of +1.25 V from U661C. The resulting DAC output is compared to a +1.25 volt reference by operational amplifier U660. Any
deviation from the correct +1.25 V level produces a gaincorrection voltage applied to the DAC via R760. Capacitor C662 maintains the correction voltage between DAC update cycles.

## Multiplexer Select

The Multiplexer Select circuit, composed of addressable latch U272 and the associated decoding gates, provides the enabling signal that selects one of the four 1-of-8 multiplexers to route the DAC output voltage to the Sample-and-Hold circuits. Data applied to the D input of U272 from data bus bit $\overline{\mathrm{D7}}$ (via U280D) is latched to the addressed output pin as determined by the logic levels on the $A, B$, and $C$ select lines (A0 through A2). The input data is written to the addressed output on the falling edge of the enable signal at pin 14 (via U280A and U280C). The logic state written to the output remains latched when the enable signal returns HI. The states of the unaddressed outputs remain unchanged. To enable the latch, NOR-gate U280A (functioning as a negative-logic NAND-gate) needs the DACSEL (DAC select) line LO to produce a HI output. That HI is inverted by U280C to enable the Multiplexer Select register to be written into. That same LO DACSEL is applied to NOR-gate U280D to enable it to pass the data on the D7 line to the D input of U272 and to the DAC input register, formed by U850 and U851.

Multiplexer US51, when enabled by Multiplexer Select Latch U272, routes the analog output voltage from DAC I-to-E Converter U661C to one of eight Sample-and-Hold circuits, depending on the output specified by the logic states on the its select inputs. Selection is determined by three bits clocked into DAC Register U851 as described in the preceding D/A Converter discussion. One of three other multiplexers, shown in diagram 6, may be enabled instead of U651 to pass the DAC output to one of the Sample-and-Hold circuits on their outputs (also shown in diagram 6).

## Sample-and-Hold

The eight Sample-and-Hold circuits shown on diagram 5 (formed by U641A through U641D, U650, U660, U661A, U661B and their associated components) store and buffer the analog voltage levels directed to them by multiplexer U651. Each of the operational-amplifier circuits selectable by U651 (except the DAC Offset and DAC Gain operational amplifiers, U650 and U660 respectively) has a hold capacitor on one input that is charged up to the DAC output voltage level through the selected multiplexer channel. When the multiplexer channel is then deselected, the capacitor holds the voltage at a fixed level so that the associated Sample-and-Hold circuit provides a steady voltage level to the circuit it controls. Voltage gain of the Sample-and-Hold operational amplifiers range from more than 4.5 in the CH 1 and CH 2 Gain-Cal circuits down to 2 in the

Jit 1 Gain and Jit 2 Gain amplifiers and down to about 1 for the CH 1 and CH 2-BAL voltage followers. The Jitter Gain circuits (formed by U661A and U661B) produce a negative 5 V dc offset voltage at their output pins as their gain-setting resistors are referenced to the +5 V supply. The DAC Offset and DAC Gain Sample-and-Hold circuit operations are described in the previous D/A Converter discussion.

## Acquisition Control Registers

Mode control of the analog acquisition system and trigger circuitry is controlled by the System $\mu \mathrm{P}$ via shift registers and a decoder. The System $\mu \mathrm{P}$, through its address decoding circuitry, enables Decoder U271 to produce a shift register clock at one of its eight outputs. These clock signals are used to move serial data from the ACD (acquisition control data) line, U272 pin 5, into one of the various Acquisition Control Registers, of which three are shown in diagram 5 . They are Peak Detector Control Register U530, Gate Array Control Register U270, and Trigger Source Control Register U140. Other registers clocked are the Channel 1 and Channel 2 Control Registers (U510 and U220 on diagram 9), the internal control registers of the CH 1 and CH 2 Preamplifiers (U420 and U320 on diagram 9), and the internal control registers in the $A / B$ Trigger Generator (U150, diagram 11).

The ACD line is shared by all the Acquisition Control Registers; the selected clock determines which register will be loaded with the data being written by the System $\mu \mathrm{P}$. Decoder U271 is enabled when the $\overline{A C Q S E L}$ and $\overline{W R}$ lines are LO and address line A3 is HI. Address lines AO, A1, A2 determine which of the output lines produces the clock signal. A data bit present on the ACD line (previously written to latch U272 in a DAC write cycle) is loaded into the clocked register on the rising edge of the $\overline{W R}$ signal as U271 becomes unenabled and its selected LO output goes HI . Each bit to be loaded must be successively written to U272 then moved into a register by the output clock from U271.

## SYSTEM DAC (cont) AND AUXILIARY FRONT PANEL

The DAC multiplexing and sample-and-hold circuits included in diagram 6 operate similarly to those described in the DAC System (diagram 5) discussion. The analog voltage output from the DAC I-to-E Converter is routed through one of the three additional multiplexers (shown in diagram 6) to several types of hold circuits.

## DAC Multiplexers

DAC Multiplexers U821, U830, and U831 route the analog output voltage from DAC I-to-E Converter U661C (diagram 5) to the various Sample-and-Hold circuits. Operation of each multiplexer is identical to that of Multiplexer U651, previously described in the System DAC circuit discussion. Each multiplexer is individually enabled by a bit from Multiplexer Select Latch U272, and signal routing through the enabled device is controlled by the three select bits applied to it from the three most significant bit outputs of DAC Register U851.

## Sample-and-Hold

A separate Sample-and-Hold circuit is associated with each of the multiplexer outputs. An analog voltage routed from the DAC l-to-E Converter through the selected multiplexer channel charges up the hold capacitor at the input of an operational amplifier in the selected Sample-and-Hold circuit. When that multiplexer channel is deselected, the voltage level is held on the capacitor because of the highimpedance discharge paths presented by the multiplexer output and the operational amplifier input. The individual operational amplifiers are configured as buffers with voltage gains varying from -0.47 to +10 , depending on the requirements of the function that is being controlled. The CH 1 and CH 2 Position Sample-and-Hold circuits also provide a dc offset of their output levels to properly bias the inputs they drive.

## Cal Signal Amplifier

The Cal Signal Amplifier (U610) operates in a manner similar to the Sample-and-Hold circuits just described. It is used to supply test signals to the CAL inputs of the CH 1 and CH 2 Peak Detectors (U440 and U340, diagram 10) for Self Calibration of the acquisition system. The test signal level, stored on capacitor C733, is applied to the input of an amplifier internal to U610 which has dual-differential outputs. The complementary-current outputs for each channel are approximately $6 \mathrm{~mA} \pm 1.25 \mathrm{~mA}$.

## Z-Axis Control

The Z-Axis Control stage consists of Q810, U811, U810A, U810B, five-transistor array U812, and associated components. Multiplexer $U 811$ selects one of three intensity-control voltages-normal, intensified, or readout (output from Sample-and-Hold buffers U820B, U820C, or U820D) and routes it to a current source composed of U810A, U810B, and Q810. The amount of current passed by Q810 controls the display intensity. The transistors in array U812 form an automatic gain compensation circuit for Z-Axis Amplifier U227 (diagram 19).

Selecting an input to pass through multiplexer U811 is done by two active input signals, BRIGHTZ and RO. (The third select input is a permanent LO, so one of the first four inputs only can be selected.) For normal-intensity waveform displays, all select bits will be LO to select input 0 to switch through U811. If the waveform display should be intensified at any time, the BRIGHTZ input will go HI , selecting input 1 . When readout is to be displayed, the RO input will go HI , selecting either input 3 or input 4, depending on the setting of the BRIGHTZ bit. Since inputs 3 and 4 are both connected to the INT-RO (readout intensity) control voltage level, the readout displays are not intensified.

The selected intensity control voltage is applied to U810B, configured as an inverting buffer with a gain of -1 . The output voltage is offset -4.06 V by the voltage divider at pins 3 and 5 of U810 (R814 and R815) and resistor R816 at pin 6. The resulting inverted and shifted output is converted to a current by R812 and applied to the emitter of Q810.

The circuitry of operational amplifier U810A and transistor Q810 is arranged so that the transistor is on with its emitter held at -2.7 V . The -2.7 V level at the emitter is set by the bias on input pin 3 of operational amplifier U810A. The voltage developed at the output of U810B causes a current to flow in R812 and sets the current drive level for the Z-Axis circuit (diagram 19). This Z-INT drive current supplied via U812E from pin 14 may vary from 0 mA to $4 \mathrm{~mA}(-1.36 \mathrm{~V}$ to +1.36 V respectively at the output pin of multiplexer U811).

When the intensity of the selected display is at minimum, the output control voltage from multiplexer U811 will be below -1.36 V . This causes the output of U810B to go to approximately -2.7 V , reducing the emitter current to Q810 to approximately zero. Diode CR810 limits the reverse-bias voltage across the base-emitter junction of Q810 to about 0.6 volts and protects the base-emitter junction from excessive voltage.

Automatic compensation of the Z-Axis Amplifier gain is carried out in five-transistor array U812. Transistors U812B and U812C form the bias network for U812D, one-half of the Z-Drive compensation amplifier. Biasing for the other transistor of the differential pair is supplied by U812A, R817, and a resistor internal to the Z-Axis Amplifier that is tied to the $+5 \mathrm{~V}_{\mathrm{D}}$ supply. The differential amplifier pair is biased so that the total current is divided between the two sides. The resistance value of the internal resistor in the Z-Axis Amplifier is an indication of the gain of that device. Changes in that value that occur between different Z-Axis Amplifiers shift the biasing level of U812E to either increase or decrease the share of the total
current through that transistor by a small amount. The change in current is in the appropriate direction to make the display intensity of different instruments comparable with exactly the same Intensity control settings. Capacitor C817 bypasses high-frequency noise present on the ZGAIN signal line.

The SPOTWOB (spot wobble) signal line, at the output of Operational Amplifier U810B, picks off the various intensity levels. Those levels are used in the Horizontal and Vertical Output Amplifiers (diagram 18) to dynamically correct intensity-related position shifts on the crt (described in the Display Output circuitry discussion).

## Graticule Illumination

The Graticule Illumination circuit, composed of U820A, U520G, and associated components, sets the brightness of the three lamps used to light up the graticule lines etched on the crt faceplate.

Operational amplifier U820A is configured as an inverting integrator. Inverting buffer U520G may be thought of simply as an open-collector transistor following operational amplifier U820. The circuit appears this way because the negative feedback around the loop via U 820 and voltage divider R824-R825 keeps U520G in its linear operating range. Gain around the loop (11) is set by the ratio of R822 to R823 plus 1. The DAC control voltage applied to pin 2 of U820A causes the integrator output to slowly ramp in the opposite direction. This output is inverted by U520G, and it sets the current in the graticule lamps. Between DAC-updates no integration takes place, and the charge held on C822 holds the output of the inverting buffer, and thereby the graticule lighting, constant.

## Auxiliary Front Panel

The Auxiliary Front Panel circuitry provides a means of reading the front-panel bezel push buttons, located directly below the crt, as well as several analog voltages associated with the front-panel BNC input connectors. The circuit consist of analog multiplexer U 600 (used to route the various analog voltages to the A/D converter), parallelloading shift register U700 (used to relay switch-closure data to the Front Panel $\mu \mathrm{P}$, shown in diagram 3), and associated components.

Analog multiplexer U 600 routes one of the eight input levels to the $A / D$ converter internal to Front Panel $\mu P$ U700 (diagram 3), depending on the three-bit code applied to its select inputs. The selected signal may be one of the four probe-coding voltages (developed by the voltage divider formed by the encoding resistance of the probe attached to the input connectors and the associated pullup resistor within R601), the CH1 OVL (overload) or CH2

OVL levels (used to indicate when an excessive voltage is applied to the input connector), or one of the two, 180 degree out-of-phase wipers on the Intensity control (a continuous-rotation pot).

Auxiliary Switch Register U700 performs a parallel load of the status of all of its input bits whenever the Front Panel $\mu \mathrm{P}$ puts out a SHCLK (shift clock) with the $\mathrm{S} / \bar{L}$ (shift/load) select input of the register set LO. Once loaded, the $S / \bar{L}$ input is set $H I$, and the eight bits of switch-closure data are clocked out to the Front Panel $\mu \mathrm{P}$ on the SWOUTA (switch data out-auxiliary Front Panel) line with eight more clocks applied to the clock input of the Auxiliary Switch Register. Switches read include the five menu select switches on the lower edge of the crt bezel, the Intensity Control SELECT switch, the STATUS switch, and the MENU OFF/EXTENDED MENU switch.

## SYSTEM CLOCKS

The System Clocks circuitry (diagram 7) produces the fixed-frequency System clocks signals used throughout the oscilloscope. These clocks are developed from a 40 MHz master clock frequency, and they are used to drive state machines that produce other special-purpose clocks that control the waveform acquisition processes.

## Master Clock

The Master Clock circuit produces 20 MHz and 8 MHz clocks ( $\overline{\mathrm{C} 20 \mathrm{M}}$ and C8M) by dividing down the output from the 40 MHz crystal oscillator circuit, Y611. The oscillator circuit drives both the divide-by-two flip-flop (U612A) and the divide-by-five circuit (flip-flops U612B, U615A, and U615B) in parallel via inverter U513A. The 20 MHz clock is obtained from flip-flop U612A. With its Set, Clear, J, and K inputs all held permanently HI , the flip-flop toggles on each negative-going 40 MHz clock edge to divide the input clock frequency by two.

The divide-by-five circuit is a state machine formed by J-K flip-flops U612B, U615A, and U615B. With the two feedback signals to the J and K inputs of U612B, the flipflop chain sets logic level on the $J$ and $K$ inputs of U615B that allows its Q output to change states only every five 40 MHz input clocks to produce the 8 MHz clock.

Jumper J 132 allows an external clock signal to be substituted for the 40 MHz clock signal to aid in testing and troubleshooting.

## Secondary Clocks

The Secondary Clocks circuit further divides the 20 MHz clock to produce other system clock rates. The flip-flops within U710, along with logic gates U711A, $\mathrm{U} 711 \mathrm{~B}, \mathrm{U} 11 \mathrm{C}$, and U 712 B , produce $10 \mathrm{MHz}, 5 \mathrm{MHz}$, and 2.5 MHz clocks.

Flip-flop U710D and exclusive-OR gate U711C generate the 2.5 MHz clock (CLK3A) that is delayed $3 / 8$ of a cycle ( 150 ns ) with respect to the 2.5 MHz clock at the $3 Q$ output (CLK1A). CLK1A, CLK2A, and CLK3A are used for control-clock generation in the Waveform Processor system (diagram 2). The 10 MHz clock is the reference signal to the Phase Clock Array's phase-lock loop circuit (U381, diagram 11). This clock is available at J133 for use as a trigger signal when troubleshooting the Waveform Processor system with a logic analyzer or test oscilloscope.

The CLK1A, CLK2A, and CLK3A clocks are buffered by U712A, U712C, and U712D to the Waveform $\mu$ P. Buffering these clocks ensures that a fault on the buffered side will not halt operation of the Secondary Clock Generator circuit. Series-damping resistors R713, R715, and R716 reduce ringing in the interconnection cable. The 5 MHz clock is used in the display control circuitry, diagram 17.

## Minimum-Delay 1 MHz Clock

The Minimum-Delay 1 MHz Clock circuit produces a 1 MHz clock (2XPC) whose transitions very nearly coincide with those of the 20 MHz clock. The requirements of the clock timing dictate that the delay between a rising edge of the 20 MHz clock (C20M2 on U720A pin 3) and the 2 MHz TTL4C (TTL-compatible phase 4 clock, originating from Phase Clock Array U470-diagram 11) transitions be less than 50 ns to ensure proper phasing. Since the propagation delay (2XPC-to- TTL4C delay) through the Phase-Clock Array is a significant portion of the 50 ns allowed, the phase of the 2XPC (two-times CCD "C" register clock rate) clock relative to the 20 MHz clock must be optimized for minimum delay.

To obtain minimum delay, U622, U523B, and their associated logic gating are configured as a divide-by-20 counter whose output is synchronized to the 20 MHz clock (plus propagation delay through U523B). Counter U622 and NAND-gate U620C provide division by ten, producing a 2 MHz clock ( 4 XPC ) at pin 11 of U622.

## Theory of Operation-2440 Service

After one run through the counting cycle at power-on, any unknown counter states in divide-by-ten counter U622 are resolved, and the circuit counts in the following manner: If the circuit does not start in the Load condition, it will be in the Count mode (a HI on pin 9 from the output of NAND-gate U620C) and the 20 MHz clocks cause the counter output to increment until it reaches 1100 (binary). At this point the output of U620C will go LO, causing the counter to load the count 0011 (binary) from its inputs with the next clock. Once the counter is loaded, the output of U620C will return HI , and normal counting from a known state commences. When the counter reaches 1100 again, the load-count sequence will be repeated, requiring ten 20 MHz clocks to complete the cycle.

AND-gate U623C watches the three lowest bits of the counter outputs ( $Q_{A}, Q_{B}$, and $Q_{C}$ ). The output of U623C (pin 8) will be HI during the " 7 "' state ( 0111 binary) of each 10 -count cycle and will stay HI for one 20 MHz clock cycle ( 50 ns ). This HI is applied to the K input and the J input (via OR-gate U522B) of flip-flop U523B. With the $K$ and J inputs both HI , the flip-flop toggles when the next 20 MHz clock arrives. Assuming the $\mathbf{Q}$ output of the flip-flop was LO, toggling to a HI applies a HI to the J input via OR-gate U522B. When the output of U623C returns LO (next 20 MHz clock), the $J$ and $K$ input states of the flip-flop will keep the $Q$ output HI with subsequent 20 MHz clocks.

The Q output of U523B will stay HI until the next seven (0111) state from AND-gate U623C arrives, at which time the J and K inputs are again set HI . On the rising edge of the next 20 MHz clock the Q output of flip-flop U523B toggles LO. When the 50 ns pulse from U623C returns LO, the J and K input states will both be LO, and further 20 MHz clocks are prevented from changing the Q output state of the flip-flop. The output remains LO until the next HI state from U623C starts the divide sequence over again. Note that transitions of the 1 MHz signal (2XPC) at pin 9 of U523B are delayed from the $\overline{\mathrm{C} 20 \mathrm{M}}(20 \mathrm{MHz}$ clock) clock rising-edge transitions by only the propagation delay through the flip-flop (about 7 ns ).

## CCD Output-Sample Clocks

The CCD (charge-couple devices) Output-Sample Clocks stage controls signal transfers from the Acquisition CCD-Clock Drivers (diagram 10) to the external CCD Output circuitry (diagram 14). It consists of a state machine synchronized to the 20 MHz clock (and thus the CCD events) and produces clocks to: (1) move sampled data out of the CH1 CCD array, (2) move sampled data out of the CH2 CCD array, (3) reset both the CH 1 and CH 2 CCD array output-charge wells in preparation for the next transfer, and (4) phase-lock the CCD-Data Clock stage. Figure 3-3 illustrates the timing of these clocks and other clocks in the System Clock Generator; it may be of use in following the discussion of circuit operation.

When acquired samples are to be shifted out of the CH1 and CH2 CCD array, the TTL version of the PhaseClock 02 output (TTL2C) from Phase Clock Array U470) will be toggling at 500 kHz . Transitions of the TTL2C clock are resynchronized to the 20 MHz clock (C20M2) by flipflop U720A to correct the phase between the TTL2C clock and the state machine outputs. This correction closely synchronizes charge transfers within the CCD (relative to the 2XPC clock) with the signal transfers out of the CCD.

When the $\overline{\text { SYNC2C }}$ (synchronized phase-4 clock) is LO (pin 5 of flip-flop U720A), the LOAD signal applied to shift registers U730 and U830 (via AND-gate U623B and inverter U513E) will be HI. This HI, along with the HI SYNC2C signal from pin 6 of flip-flop U720A, causes both shift registers to do a parallel load of the fixed logic levels applied to their $D$ input pins. The levels loaded set the $\overline{\mathrm{OS1}}$ (sample $\mathrm{CH} 1-\mathrm{CCD}$ outputs), $\overline{\mathrm{OS} 2}$ (sample $\mathrm{CH} 2-\mathrm{CCD}$ outputs), and the RST (reset CCD output wells) outputs from U730, and the SYNC (sync data clocks) output from U830 all HI. The HI RST level applied back to U621 and the HI output from NAND-gate U620B will be loaded into counter U621 as 0101 binary because of the LO LOAD output of U623B applied to the CT/ $\overline{\mathrm{LD}}$ input pin. This state then stays as is for the remainder of the LO state of the SYNC2C signal.

When the SYNC2C output of flip-flop U720A returns HI, counter U621 is enabled by the HI from AND-gate U623B to count for three, 20 MHz clock cycles ( 150 ns ), reaching the count of 0111 binary. The next clock toggles the QC output of U621 LO (count goes to 1000 binary), and the LOAD output from AND-gate U623B is forced LO. The HI LOAD signal output obtained from inverter U513E, along with the LO SYNC2C from flip-flop U720A pin 6, sets up shift registers U 730 and U830 to shift right. The next 20 MHz clock ( 250 ns after the 2XPC clock toggled) shifts a LO to the OS1 output of U730 (pin 14) and loads a binary 0100 into counter U621 (since the output of NAND. gate U620B is now LO). The fixed HI applied to the SR data input of $\mathbf{U 7 3 0}$ is shifted to the $\mathrm{Q}_{\mathrm{A}}$ output.

After 0100 is loaded into counter U621, the LOAD output of U623B returns HI (since pin 12 of U621 has been set HI by the inputs loaded into the counter). This once again produces a LO LOAD output from inverter U513E and prevents U730 and U830 from shifting. Counter U621 counts four cycles of the 20 MHz clock ( 200 ns ), reaching count 0111. The next 20 MHz clock toggles the $Q_{C}$ output of U621 LO and sets the LOAD line LO once again, enabling shift registers U730 and U830. The next clock ( 250 ns ) shifts the previously loaded LO from the OS1 output right to the $\overline{\mathrm{OS} 2}$ output of U730 and moves a HI from the SR data input into the $\overline{0 S 1}$ output. At the same time, counter U621 is reloaded to 0100 binary to again restart its count.


Figure 3-3. System Clock waveforms.

A similar 250 ns cycle occurs for the $\overline{\mathrm{OS} 2}$ LO state, ending with the LO being shifted to the $Q_{D}$ output of U730. However, when the load is done to U621 this time, the $\overline{O S 2}$ output to NAND-gate U620B is LO, and counter U621 is loaded with 0101 binary (the $D_{A}$ ) input from U 620 B is HI ).

Since U621 now needs one less clock to count to 0111, $\overline{\operatorname{RST}}$ (and thus $\overline{\operatorname{RESET}}$ remains LO for 200 ns (rather than 250 ns as for $\overline{O S 1}$ and $\overline{O S 2}$ ), after which time the next load of U621 will occur. At the end of the reset time, both RST and the DA output of U620B are both LO, so counter U621 loads to 0000 binary. On the same 20 MHz clock, the LO RST level present on the SR data input of U830 is shifted right to the QA ( $\overline{S Y N C}$ ) output. This state (with SYNC LO) lasts one clock cycle ( 50 ns ) only, because $\mathrm{Q}_{\mathrm{C}}$ is still LO, causing LOAD to go HI and, therefore, causing the shift register to again shift right, resulting in SYNC going HI. On the next 20 MHz clock pulse, the TTL2C input is LO, causing SYNC2C to go LO on the clock edge. This starts the whole process over, and it is repeated until all samples have been moved out of the CCD arrays.

AND-gates U731A, U731B, and U731C buffer the outputs of counter U730 and ensure that the counter and the clock circuit will keep running even if a short occurs on the buffered OSAM1, OSAM2, or RESET lines.

## CCD Data Clocks

The CCD Data Clocks (MS11, MS12, $\overline{M S 13}, \overline{M S 14,}$ MS21, MS22, MS23, and MS24) generated by counter U721, shift register U831 and U833, and the associated logic gating, are responsible for multiplexing the eight CCD array output levels (CH 1-1, CH 1-2, CH 1-3, CH 1-4, CH 2-1, CH 2-2, CH 2-3, and CH 2-4) onto the CCD DATA line for digitization by the A/D Converter. Figure 3-3 (shown previously) illustrates timing of the stage.

When the SYNC output from U830 pin 15 goes LO (for 50 ns at the end of the TTL2C cycle), the outputs of NAND-gate U620A and inverter U513D go HI, and the output of AND-gate U623A goes LO. This places counter U721 and shift registers U831 and U833 in their parallel load mode, and the next 20 MHz clock rising edge (start of next TTL2C loads in the fixed logic levels at their D inputs. The data bits ( 1000 binary) loaded into shift register U831 set the MS12 (multiplexer-select CH1 phase-2) output bit (pin 15) HI, with all other output bits LO. The LO MS12 output from inverter U832D is applied to Q873 (diagram 14) to switch the CCD output data from the CH 1 CCD array phase-2 output onto the CCD DATA line, where it is applied to A/D Converter U560 (diagram 15).

That same 20 MHz clock loads counter U721 with 1100 binary and clocks $\overline{\text { SYNC }}$ from pin 15 of U830 HI. With SYNC HI, shift register U831 is in hold mode, and counter U721 is enabled to count via AND-gate U623A. Counter U721 increments from the beginning count of 1100 to 0000 (four, 20 MHz clocks- 200 ns ), at which time the $\overline{\text { SHIFT }}$ output from OR-gate U522A goes LO. This sets up shift registers U831 and U833 (via U620A) to shift and, via U623A, places U721 in load mode. The next 20 MHz clock (at 250 ns ) shifts a new LO from the SR data input of U831 into the $\mathrm{Q}_{\mathrm{A}}$ output and shifts the HI from the $\mathrm{Q}_{\mathrm{A}}$ output to the $Q_{B}$ output (MS22). Counter U721 is also reloaded with 1100 binary for the next count cycle.

Similar 250 ns count cycles shift the HI bit to each output of shift registers U831 and U833 in succession until, during the last 50 ns of the HI state of the MS21 signal (U831 pin 15), $\overline{\text { SYNC }}$ goes LO again. The LO sets up U721, U831, and U833 to load on the next 20 MHz clock. The next clock (concurrent with TTL2C going LO) loads both U721, U831, and U833 and starts the cycle over again. The arrival of the $\overline{\text { SYNC }}$ signal ensures that the presetting load of U721, U831, and U833 always occurs concurrently with TTL2C going LO. The eight multiplexerselect clocks (and their inverted outputs) are thereby synchronized to CCD array output cycles.

The CCD Data Clock circuit also derives the signals used to multiplex the Acquisition Latch Switches. For Envelope mode acquisitions, these switches, in turn, select which byte of min/max data (stored in the Acquisition Latches) the Envelope Min/Max Comparator compares against a newly-acquired byte, A/D converted and output by the A/D Converter. (The Acquisition Latches and Acquisition Latch Switches, as well as the A/D Converter and Envelope Min/Max Comparator are found on diagram 15).

Briefly, the Acquisition Latch Switches need to "know" which CCD, CH 1's or CH 2's, and which CCD "side," minimum or maximum, is supplying the data byte being converted by the A/D Converter. MS11 and MS13, CH1 clocks, and MS21 and MS23, CH 2 clocks, are HI when a data byte from the minimum side of the CCD is being A/D converted; MS12 and MS14, CH 1 clocks, and MS22 and MS24, CH 2 clocks, are HI when a data byte from the maximum side is being converted. (Note that if the last digit of the clock name is odd, it clocks data from the minimum side of a CCD, and if it is even, from the maximum side. Also, note that the first digit indicates the CCD's channel. In other words, MS11 is Multiplexer-Select Clock CH 1, minimum side, MS22 is the Multiplexer-Select Clock for CH 2, maximum side, etc.) Gates U834A-D (diagram 7) logically OR these CCD Data Clocks to derive the multiplexing signals MS12+MS14, MS22+MS24,

MS13 + MS11, and MS23 + MS21 to drive these Acquisition Latch Switches. (For example, MS12 + MS14 indicates that the data is from the minimum side of the CH 1 CCD and is HI if either MS12 OR MS14 is HI.) How these signals multiplex the Acquisition Latch Switches is explained in "A/D Converter and Acquisition Latches" in this section.

The CCD DATA Clock circuit supplies three other clocks used to properly time the transfer of A/D Converted CCD data: SHIFT, derived as previously described, and CLKLATCH and SHIFTD200N, derived from the SHIFT clock. $\overline{\text { SHIFT }}$ drives the shift-right input (pin 2) of shiftregister U642, and C20M1 clocks the SHIFT clock successively through U642's outputs (QA-QD). Since C20M1 is the 20 MHz Clock and two 50 ns clock cycles are required before SHIFT appears at the QB output, CLKLATCH is delayed 100 ns from SHIFT. Four clocks are required to clock SHIFT to the QD output, resulting in a 200 ns delay from SHIFT for SHIFTD200N.

SHIFT clocks the A/D Converter, and CLKLATCH clocks the Acquisiton Latch Switches. The timing offset between the two clocks ensures the data byte output by the converter has stablized before it is latched into the Acquisition Latches. (The A/D Converter, Acquisition Latch Switches, and Acquisition Latches are found on diagram 15.) Similarly, $\overline{\text { SHIFTD200N }}$ is routed to NAND-gated U650B via inverter U835F (both found on diagram 8) for use in controlling the timing of the SAVEACQ signal to the Acquisition Memory. In this case, the time offset ensures that the data written from the Acquisition Latches to that memory has stabilized.

## TIME BASE CONTROLLER AND ACQUISITION MEMORY

Time Base Controller (U670, diagram 8) and its associated gating circuitry generates the control signals and clocks to cause acquisitions in the various modes to occur. It keeps track of how the acquisition is progressing, starts the digitization of the samples by the A/D Converter when the correct number of data points have been acquired, and moves the digitized samples to Acquisition Memory (U600). The Acquisition Memory provides temporary storage of the converted data to permit the Waveform $\mu \mathrm{P}$ to access the data as it is needed to update the display.

## Time Base Controller

Time Base Controller U670 monitors and controls the various acquisition functions. Two different operating
modes of the CCD (charge-coupled devices) arrays must be controlled by U670; these are the FISO mode (fast-in, slow-out) and the Short-Pipe mode. FISO mode is used at sweep speeds faster than $100 \mu \mathrm{~s} / \mathrm{div}$ when the analog sampling must occur at rates faster ( 1 MHz per channel and faster) than the maximum conversion rate of the $A / D$ Converter. The Short-Pipe mode is used for lower frequency signals when the $A / D$ conversion rate is much faster than the signals being sampled.

The major Time Base Controller functions in FISO (fast-in, slow-out) mode:

- Ensure that enough samples are in the CCD array " $B$ " register to fill the "pretrigger" requirements.
- Ensure that the proper number of "post-trigger" samples are moved into the " $\mathrm{B}^{n}$ register after triggering occurs.
- Discard the proper number of unneeded samples at the start of "slow-out" conversion.
- Ensure that exactly 1024 samples are moved to the Acquisition Memory during the "slow-out" conversion process.

Major functions in Short-Pipe mode:

- Ensure that valid data has made it through the "short-pipe" path of the CCD arrays.
- Synthesize the proper sample rate called for by the SEC/DIV setting.
- Ensure that enough samples have been saved in the Acquisition Memory to fill pretrigger requirements before enabling the Triggers.
- Ensure that the proper number of post-trigger samples are stored into the Acquisition Memory after the trigger event.

The instruction registers within Time Base Controller U670 are enabled when TBSEL from the System $\mu \mathrm{P}$ is LO. A register is selected for writing to or reading from by address lines A0, A1, and A2. Setup data from the System $\mu \mathrm{P}$ data bus is buffered to the selected register via bidirectional buffer U641 and written into the selected internal register by the $\overline{W R}$ (write) signal applied to pin 14. Acquisition mode, SEC/DIV setting, trigger position, and several other functions are controlled by the System $\mu \mathrm{P}$ via the commands written to the instruction registers within U670. Status data and register contents may be read out of the Time Base Controller registers by the System $\mu \mathrm{P}$ in a similar manner using the $\overline{\mathrm{RD}}$ (read) signal to reverse the data paths in buffer U641 and the internal circuitry of U670.

The FISO (fast-in, slow-out, pin 36), ROLL (pin 2), and ENVL (envelope, pin 39) outputs are set indirectly by System $\mu \mathrm{P}$ writes to the internal control registers at the start of each acquisition cycle. Control signals are then output by an internal state machine of the Time Base Controller to dynamically control the acquisition circuitry in the required mode and signal acquisition rate (set by FISO). Writing to these "register" locations also allows the System $\mu \mathrm{P}$ to generate several strobes for internal latching and control functions.

A state machine internal to Time Base Controller U670 runs the acquisition process from start to finish. When all internal registers are properly loaded, the System $\mu \mathrm{P}$ writes to location 6022(h), generating a strobe that switches acquisition control to the Time Base Controller. This starts the acquisition system, and samples are taken in the defined mode. For FISO operations, the following occurs.

A counter internal to $\mathbf{U 6 7 0}$ begins counting TTLB1 (TTL version of $B$ clock-Phase 1) clocks to determine when at least enough samples have been transferred into the " $B$ " register of the CCD arrays to fill "pretrigger" requirements. Samples will then continue to be placed in the B register, but no output samples will be saved until the record trigger occurs. (All 1088 locations in the four sides of $8 \times 34$ $B$ register will fill if a record trigger does not occur before that many samples have been taken.) Each TTLB1 clock represents 32 analog samples (four, 8 -sample sides) transferred into the CCD array $B$ register. When the proper number of pretrigger samples have been loaded, U670 will set its EPTHO (end of pretrigger holdoff) line HI. This signal enables Trigger Logic Array U370 (diagram 11), and the state machine in Time Base Controller U670 starts watching the SYNTRIG (synchronized trigger) input (pin 30) from the Phase Clock Array (U470, diagram 11) for the "record" trigger. In the meantime, the Trigger Logic Array will be counting delay clocks (DELCLK) to fulfill any specified delay requirements before a record trigger is permitted to be generated.

When the delay requirements are met, the SYNTRIG is allowed to occur when a trigger event occurs. The counter then watches TTLB1 to determine when the proper number of post-trigger samples have been moved to the B register to meet the post-trigger requirements. Once post-trigger requirements are met, it sets SO (slow-out, pin 38) HI , which stops the sampling process and starts A/D conversion of the analog samples stored in the CCD array B register.

Since the trigger event can occur at any one of the 32 analog samples that are taken between each TTLB1B clock, and since the Time Base Controller only keeps track of the number of pretrigger and post-trigger samples in terms of these 34-sample records, there are usually some samples at the beginning of those in the CCD array

B register that are extra. When the analog samples are serially moved out of the CCD array for digitization, these extra samples must be ignored in order to maintain proper trigger location within the complete record. The CCD Phase Clock Array (U470) knows where the record trigger occurred relative to the TTLB1 pulse (1-of-32 position) and sends this information to U670 on the TLO-TL4 (trigger location bits 0 through 4) lines. This trigger-location number is loaded into the counter and, as the samples are moved out of the CCD array, that number of extra samples is essentially discarded. Those samples are A/D converted but will not be stored because U650B is not yet enabled to gate the SAVEACQ signal used to write the data into the Acquisition Memory.

Once the extra samples have been counted, the ACQUIRE output is set HI. In FISO mode, six more samples are counted out via shift register U750, enabling U650B. Since the instrument is in FISO mode, the output of U512C will be HI and the SAVEACQ signal that is used to save waveform data into the Acquisition Memory (via U501) is controlled by the output of U835F (SHIFTD200N). This input to NAND-gate U650B is a delayed version of the SHIFT ( 4 MHz ) clock. The 200 ns delay provided ensures that the A/D Converter output byte has settled before being written to the Acquisition Memory.

When the Time Base Controller is in control of writing data to the Acquisition Memory, the SAVEACQ clock is routed through U501 of the Mode Control Logic and becomes the $\overline{W E}$ (write enable) clock used to write waveform data into Acquisition Memory U600. That data is obtained from the Acquisition Latches (diagram 15) via buffer U613. The WE signal is also used to increment the Memory Address Counter (U300, U400, and U401), the result being that digitized samples from the Acquisition Latches are saved interleaved in consecutive memory locations. Each address is latched into the Record-Start Address Latches (U502 and U601) as the data-write ends, so that the address of the last-stored sample is always available. This information is used as a pointer when generating waveform displays.

As the digitized samples are moved to Acquisition Memory, an internal counter in Time Base Controller U670 watches the MS23+MS21 and MS22 + MS24 clocks (pins 6 and 28) to determine when 1024 points (or $512 \mathrm{max} / \mathrm{min}$ pairs in Envelope mode) from each CCD array (CH 1 and CH 2) have been stored. When 2048 samples have been saved, the Time Base Controller will set ACQUIRE (pin 24) LO, disabling memory saves, and it will set its ACQDN (acquisition done) status line (pin 25) HI. The Waveform $\mu \mathrm{P}$ (U470, diagram 2) then takes over for transfer of the acquired waveforms to the Waveform $\mu \mathrm{P}$ Save Memory.

When the Waveform $\mu \mathrm{P}$ (U470, diagram 2) reads the HI ACQDN status via U542 (diagram 2), it reads the address
of the last-saved point from the Record-End Latch (U502 and U601). Since the Acquisition Memory addresses are circular (incrementing the Address Counter from its last address goes back to the first address), it knows the record begins at the next address. With TB2MEM LO, the $\overline{\mathrm{ACQ}}$ signal is routed through Mode Logic Switch U501 to become the WP2MEM signal. The $\overline{A C Q}$ signal going LO from the Waveform $\mu \mathrm{P}$ via address decoder U570 enables data buffer U610 to permit the Waveform $\mu \mathrm{P}$ to access the waveform data stored in the Acquisition Memory (see "Waveform Processor System" description).

SHORT-PIPE OPERATION. Short-Pipe operation is similar to FISO in the way mode and setup data is loaded and the way the internal counter is used to keep track of various events. The major differences are: Short-Pipe mode moves input samples directly from the CCD array " $A$ " register input down the first " $B$ " register channel and out of the CCD array through the "C" register. Short-Pipe mode must also synthesize the sample clock rate.

To synthesize the sample rate for the Short-Pipe mode, FISO (from U670 pin 36) is set LO by the System $\mu \mathrm{P}$, thereby enabling the CE2B/N (clock enable 2B divided by N ) input to U512C. The CE2B/N clock (along with the SHIFTD200N clock) then controls saving the waveform data into the Acquisition Memory. In Short-Pipe mode, CCD sampling occurs at a continuous 2 MHz rate, but due to SEC/DIV setting data written to an internal counter in U670, the synthesized CE2B/N clock will only allow every "Nth" point to be saved in Acquisition memory to produce only 50 data points per division in the display. Samples between the saved Nth points are ignored. The synthesized $\overline{C E 2 B / N}$ clock will only enable U650B long enough to save either two or four points and is dependent on the sweep-rate division factor written to the internal counter. This allows effective sample rates down to 1 sample every $2 \mu \mathrm{~s}(100 \mu \mathrm{~s} / \mathrm{div})$ to be achieved. The 2XSDC (two-times-slow-delay clock, U670-pin 29) runs at half of this effective sample rate. This 2XSDC clock divided by two at the Q output of U720B and buffered by U680C to produce SDC. SDC allows the Trigger Array to count one delay period per every four sample intervals.

Since CCD array samples are moved directly from the input to the output via the first B register and since stored samples may occur at a rate different than the sample rate, pretrigger and post-trigger counting is done relative to samples actually stored into the Acquisition Memory. When enough valid pretrigger points have been saved, EPTHO enables the Triggers. Data is saved in bursts of two points (four points in ENVELOPE acquisition mode), one for CH 1 and one for CH 2, at the synthesized rate. When the trigger event occurs, U670 counts the proper number of post-trigger samples. When the post-trigger count is complete, since A/D converted data already is stored in Acquisition Memory, ACQDN is set, Waveform
data bytes are moved to the Save Memory by the Waveform $\mu \mathrm{P}$ and control is given back to the System $\mu \mathrm{P}$.

LOAD LATCHES FLIP-FLOP. In Envelope Mode, Load Latches flip-flop U651A puts out a signal at the beginning of each envelope sampling interval that is HI for four acquisition cycles. That HI LOAD LATCHES signal loads the first eight acquired data points (four min-max pairs) into the Acquisition Latches to be used for min-max comparison to the following waveform samples in that Envelope sampling interval.

The Set input of U651A is HI during Envelope, the output of the flip-flop is controlled by the MS23 clock and the CE2B/N clock (on the $D$ input). The CE2B/N clock is a divided down MS22 clock, with the division factor depending on the SEC/DIV setting. The division factor determines how many waveform samples will be compared for new max and new min data during each envelope sampling interval. Only the maximum and minimum waveform data point values that occur during the envelope sampling interval are transferred to the Acquisition Memory.

For non-envelope acquisitions, ENVL is LO. The Set input of flip-flop U651A is therefore asserted, and U651A will be held in the Set state with the Q output (LOAD LATCHES) held HI. That constant HI signal applied to the Acquisition Latch Switching circuitry causes each data point acquired to be loaded into the Acquisition Latches and transferred into Acquisition Memory,

ROLL LOGIC. In ROLL mode the display is constantly being updated as new data points are available. A means is provided to tell the Waveform $\mu \mathrm{P}$ when new data points are available. An interrupt to the Waveform $\mu \mathrm{P}$ is generated by the Roll Logic flip-flop, U651B. When the ACQUIRE signal from Time Base Controller U670 goes HI, new waveform data points are acquired. The HI state of that signal is clocked to the Q output of flip-flop U651B on the rising edge of the $\overline{C E} 2 \mathrm{~B} / \mathrm{N}$ signal; the same signal that causes the sample data to be saved into the Acquisition Memory in Short-Pipe mode. The PTAVAIL signal at the Q output is an interrupt to the Waveform $\mu \mathrm{P}$. When the Waveform $\mu \mathrm{P}$ services the interrupt request, it sets $\overline{\text { PTACK (point acknowledge) LO via U500B and U500C to }}$ reset the flip-flop in preparation for the next new data points. The saved points are also moved to the Save Memory and then to the Display Memory for a display update.

In NORMAL mode, the ROLL signal is LO, and NANDgate U500B outputs a continuous logic HI that holds the Roll Logic flip-flop in the Reset state (with the $Q$ output LO).

## Memory Mode Control

The Memory Mode Control circuit is made up primarily of Mode Selector Switch U501, a quad 2-to-1 multiplexer that switches control signals between those of Time Base Controller U670 and those of the Waveform $\mu$ P. Selection is done by the TB2MEM signal from AND-gate U731D pin 11.

The $\overline{\mathrm{WE}}$ (write enable) output from Mode Selector Switch U501, pin 12, controls both writing into the Acquisition Memory and incrementing of the Address Counter. With TB2MEM set LO, the WWR (Waveform $\mu \mathrm{P}$ write) signal gated through OR-gate U512D to the 4A input (pin 13) of U501 controls writing to the Acquisition Memory. The $\bar{\sigma} E$ (output enable) derived from the Waveform $\mu \mathrm{P} \overline{\mathrm{WRD}}$ (Waveform $\mu \mathrm{P}$ read signal), controls the output of Acquisition Memory data. It is asserted LO only when the Waveform $\mu \mathrm{P}$ is trying to read Acquisition Memory locations.

With TB2MEM HI, the SAVEACQ signal from NANDgate U650B, is selected as the $\overline{W E}$ signal, and the $\overline{O E}$ is set HI to disable the Acquisition Memory from outputting data. Data buffer U613 is enabled by the LO level of the EOE signal from pin 7 of the Mode Select Switch to connect the Envelope Logic Latch bus to the input bus of the Acquisition Memory.


#### Abstract

When the Waveform $\mu \mathrm{P}$ wants to access the Acquisition Memory, it will set the $\overline{\mathrm{ACQ}}$ line LO to enable its control signals to the inputs of Mode Logic Switch U501 and wait for the delayed ACQUIRE signal from U750 (diagram 8) to go LO (indicating that the Time Base Controller is finished acquiring). When the delayed ACQUIRE goes LO, the output of AND-gate U731D (TB2MEM) goes LO and the Mode Logic Switch select the Waveform $\mu \mathrm{P}$ signals to control the Acquisition Memory. The LO TB2MEM signal also sets the Address Counters to their Load state, and the counter outputs then follow the WAO-WAA (Waveform $\mu \mathrm{P}$ address bits $0-\mathrm{A}$ ) lines, giving direct access to Acquisition Memory data locations by the Waveform $\mu \mathrm{P}$.


## Address Counter

The Address Counter increments the Acquisition Memory address as each point is saved. Each write into Acquisition Memory ends with the WE (write enable) signal going HI , clocking the counter to address the next sequential Acquisition Memory location.

The TB2MEM signal from AND-gate U731D controls the mode of the Acquisition Memory Address Counter (composed of binary counters U300, U400, and U401).

When the TB2MEM signal goes LO, the counters become "transparent." This connects the Waveform $\mu \mathrm{P}$ address bus to the address inputs of the Acquisition Memory so that the Address Counter output follows the WAO-WAA (Waveform $\mu \mathrm{P}$ address bits $0-A$ ) lines. When the TB2MEM signal is HI, the Time Base Controller is in control of the Acquisition Memory, and counter will be in its count mode as the acquired signals are being stored into the Acquisition Memory.

## Acquisition Memory

Acquisition Memory U600 is a random-access memory device (RAM) that provides temporary storage of acquired data points before they are moved into Save Memory. Analog waveform samples from the CH 1 and CH 2 CCD arrays are digitized and moved into Acquisition Memory under control of the Time Base Controller (diagram 8), alternating CH 1 data with CH 2 data. The Waveform $\mu \mathrm{P}$ reads the data out of Acquisition Memory via buffer U610, unscrambles it, and moves it to proper Save Memory locations.

MEMORY INPUT BUFFER. Memory Input Buffer U613 applies the time-multiplexed waveform data bytes from the Acquisition Latches (diagram 15) to the data inputs of the Acquisition Memory inputs at all times except when the Waveform $\mu \mathrm{P}$ is accessing the Memory. Inverter U620D inverts the most-significant bit of the sample data so that range center of the A/D Converter output corresponds to 00 hex (center screen value), thereby creating bipolar data referenced to center screen.

## Record-End Latch

The Record End Latch composed of U502 and U601 continually latches the address of the last Acquisition memory location that was written. The latch is clocked on the rising edge of the $\overline{W E}$ clock (from the SAVEACQ signal or the Waveform $\mu \mathrm{P}$ WWR signal via Mode Logic Switch U501) and provides the Waveform $\mu \mathrm{P}$ with the last address written (the end of the record for a full acquisition) by the Time Base Controller or read by the Waveform $\mu \mathrm{P}$. Since the Acquisition Memory addresses are circular, the start of a FISO record will always be the Record End address plus one. In Short-Pipe mode, the Waveform $\mu \mathrm{P}$ will read those (two for normal, four for envelope) points immediately preceding (and including) the Record End address. The latched address (plus the trigger location data) is placed on the Waveform $\mu \mathrm{P}$ data bus by asserting $\overline{\text { RDMARO }}$ and RDMAR1 (read memory address) lines.

Two-to-one multiplexer U722B applies either triggerlocation bit 4 (TL4) or the Time Base Controller TBTRIG (time base triggered) status bit to latch U502, depending
on whether FISO or Short-Pipe mode is called for. The TBTRIG bit used in Short-Pipe mode tells the Waveform $\mu \mathrm{P}$ when the Time Base Controller detected Record Triggering.

## ATTENUATORS AND PREAMPLIFIERS

The Attenuator and Preamplifier circuitry (diagram 9) allows the operator to select the vertical deflection factors. The Front Panel $\mu \mathrm{P}$ monitors the Channel VOLTS/DIV switches and VOLTS/DIV VAR controls and passes changes to the settings to the System $\mu \mathrm{P}$ which then digitally switches the attenuators and sets the Preamplifier gains accordingly. Vertical Couplings are similarly controlled.

## Channel 1 and Channel 2 Attenuators

The Channel 1 and Channel 2 Attenuators are identical in operation, with corresponding circuitry in each channel performing the same function. Therefore, only the Channel 1 circuitry is described.

An input signal from the Channel 1 input connector is routed through an attenuator network by four pairs of magnetic-latch relay contacts. The position of the relays is set by data placed into Attenuator Control Register U511 by the System $\mu \mathrm{P}$. Relay buffers U510 and U520A and ATTEN CLK circuitry, U520D, Q620, and Q621 provide the necessary drive current to the relay coils.

Four input coupling modes (1 M $\Omega A C, G N D, 1 M \Omega D C$, and $50 \Omega \mathrm{DC}$ ) and three attenuation factors (1X, 10X, and 100X) may be selected by closing different combinations of relay contacts. The relay contacts are magnetically latched and, once set, remain in position until new attenuator settings are loaded into the Attenuator Control Register and clocked by the ATTEN CLK circuitry. (See the "Attenuator Control Register" description for a discussion of the relaylatching procedure.) The three attenuation factors, along with the programmable and variable gain factors of the Vertical Preamplifier, are used to obtain complete range of vertical deflection factors.

The $50 \Omega$ termination resistor has a thermal sensor associated with it that produces a dc voltage (CH 1 OVL ) proportional to the input power. Should the input power exceed the normal safe operating level for the $50 \Omega \mathrm{DC}$ input, the output voltage from the thermal sensor will exceed the normal operating limit. The amplitude of this dc level is periodically checked by the Front Panel $\mu \mathrm{P}$ to detect if an overload condition is present. If an overload occurs, the System $\mu \mathrm{P}$ switches the input coupling to the
$1 \mathrm{M} \Omega$ position to prevent damage to the attenuator, and the error message " $50 \Omega$ OVERLOAD" is displayed on the CRT. At power-off, the input coupling is automatically switched to the $1 \mathrm{M} \Omega$ position to prevent an unmonitored overload condition from accidently occurring.

Compensating capacitor C414 is manually adjusted at the time of calibration to normalize input capacitance of the preamplifier to the attenuator.

A probe-coding ring around the BNC input connector passes probe-coding information (a resistance value to ground) to the Front Panel $\mu \mathrm{P}$ for detection of probe attenuation factors. The readout scale factors are then set to reflect the attenuation factor of the attached probe.

## Attenuator Control Register and Attenuator Clock

The Attenuator Control Register, composed of shift registers U511 and U221, allows the System $\mu \mathrm{P}$ to control the settings of the input coupling and attenuation factors. To set the input coupling mode and attenuation factors for Channel 1 and Channel 2 , a series of eight 16 -bit control words is serially clocked into U221 and U511 (eight bits in each register). Each control word is used to set the position of one of the eight attenuator and coupling relays (four relays are in each attenuator assembly). Each control word will have only the bit corresponding to the specific relay contact to be closed set HI. Relay buffers U510 and U520A (for Channel 1) and U220 and U520B (for Channel 2) are open-collector drivers that invert the polarities of all bits. This results in a LO being applied to only the coil lead associated with the contact to be closed; all other coil leads are held HI.

ATTENUATOR CLK CIRCUIT. To set a relay once the control word is loaded, the System $\mu \mathrm{P}$ generates an ATTN CLK (attenuator clock) to U520D pin 4 via R530 and C530. The strobe pulses the output of U520D LO for a short time. This output pulse attempts to turn on both Q620 and Q621 (relay drivers) via their identical base-bias networks. Due to the lower level from the turned on Darlington relay buffer (coupled through the associated coil diode and either CR610 or CR622 to one of the bias networks), one transistor will turn on harder as the ATTN CLK pulse begins to forward bias the transistors. The more positive collector voltage of the transistor turning on harder is fed through the bias diode (again either CR610 or CR622) to further turn off the opposite transistor. This action results in one transistor being fully on and the other one being fully off. The saturated transistor supplies a current path through the two stacked relay coils to the LO output of either U221 or U511 to close the selected contacts. Once set, the magnetic-latch feature will hold the relay set to this position until opposing data is clocked into
the Attenuator Control Register and strobed into the relay. All coil leads for the remaining relays are set HI, and only the selected relay will be set.

To set the seven remaining Attenuator and coupling relays, the sequence just described is repeated seven more times. Whenever the System $\mu \mathrm{P}$ is informed by the Front Panel $\mu \mathrm{P}$ that the attenuation factor or input coupling has changed, the entire relay-setting procedure is repeated for all eight relays.

The MSB (most-significant bit) of the Attenuator Control Register, ATD15, is routed back to the System $\mu \mathrm{P}$ via CR287 and U380A (diagram 5), allowing diagnostic readback of the register contents.

## Channel 1 Preamplifier

Preamplifier U420 converts the single-ended input signal from the Channel 1 Attenuator to a differential output signal used to drive the Channel 1 Peak Detector (U440, diagram 10). The device provides amplification in predefined increments, depending on the control data written to it from the System $\mu \mathrm{P}$. The Preamplifier also has provisions for signal inversion, variable gain, vertical \%positioning, trigger signal pickoff, and balance control.

The Channel 1 vertical input signal is applied to pin A of Channel 1 Preamplifier U420 via C1005 and R1005. The two series diodes to the -8 V supply, CR410 and CR411, protect the Preamplifier input from excessive negative voltages. The differential Preamplifier signal outputs (+OUT and -OUT) sink 12 mA of common-mode current from the Channel 1 Peak Detector inputs and drive those $75 \Omega$ inputs with a 0.25 mA per division output signal.

Control data from the System $\mu \mathrm{P}$ is clocked into the internal control register of U420 via pin 22 (CD) by the clock signal applied to pin 23 (CC). This data causes the Preamplifier either to multiply the normalized gain ( $5 \mathrm{mV} / \mathrm{div}$ ) by 2.5 or 1 or to divide the normalized gain by 2,4 , or 10 . The resulting sensitivities are $2 \mathrm{mV} / \mathrm{div}$, $5 \mathrm{mV} / \mathrm{div}, \quad 10 \mathrm{mV} / \mathrm{div}$, $\quad 20 \mathrm{mV} / \mathrm{div}$, and $\quad 50 \mathrm{mV} / \mathrm{div}$ respectively.

Four analog control voltages set by the DAC System circuitry (diagrams 5 and 6) modify the differential output signal at pins 9 and 10 of the Preamplifier. CH1-BAL (Channel 1 Balance) is applied to U 420 pin 2 from the sample-and-hold circuit formed by U641B and C648 (diagram 5). This signal is a dc-offset level determined during the auto-calibration procedure. The offset value is stored as a calibration constant in nonvolatile memory and, like the other DAC System outputs, is updated
approximately every 64 ms , holding the Preamplifier in a dc-balanced condition.

The voltage level of the CH1-PA-POS (Channel 1 Preamplifier Position) signal, from the circuit which includes U630A and U630B (diagram 6), vertically positions the channel 1 trace. When the CH1 VERT POS control on the Front Panel is turned, the Front Panel $\mu \mathrm{P}$ detects the change and reports it to the System $\mu \mathrm{P}$. The System $\mu \mathrm{P}$ incorporates the change and causes subsequent DAC System updates to reflect the new value in the analog voltage level of the CH1-PA-POS signal.

A user may change the Channel 1 variable gain by pressing the CH1 VARIABLE button and pressing the appropriate menu choice buttons. The Front Panel $\mu \mathrm{P}$ detects these switch closures and reports them to the System $\mu \mathrm{P}$. The System $\mu \mathrm{P}$ modifies the memory value that is sent to the DAC System to reflect the user-defined variable gain factor in the CH1-GAIN-CAL signal. The memory value that is modified is the calibrated value derived at the time of instrument self-calibration and stored in nonvolatile memory. Selecting the CAL menu choice removes the variable gain modification and returns the calibrated gain setting.

The TRANADJ1 control voltage, applied to U420 pin 6 from U661D (diagram 6), compensates for the variation in Preamplifier high-frequency response that occurs when the preamplifier gain setting is varied. Appropriate control voltages for each gain setting are determined at factory instrument calibration and stored in nonvolatile memory as calibration constants. They are modified only at instrument calibration times.

The network of R525, L460, variable C456, and variable R436 provide additional adjustment of the overall frequency response of the system.

A pickoff amplifier internal to $\mathbf{U 4 2 0}$ conditions the trigger signal and provides the proper signal level at pin 15 to drive the A/B Trigger Generator (U150, diagram 11). The pickoff point for the trigger signal is prior to the addition of the vertical-position offset, so the position of the signal on the CRT has no effect on the trigger operation. However, the pickoff point is after the Preamplifier balance and variable gain have been added to the signal, so both of these functions affect trigger operation.

Common-mode signals are rejected from the trigger signal by the circuitry composed of operational amplifier U 230 B and associated components. The inverting input of U230B (pin 6) is connected to the common-mode point
between + PICK (pin 12) and -PICK (pin 15) of U420. Any common-mode signals present are inverted and applied to a common-mode point between R133 and R235 to cancel the signals from the differential output. A filter network composed of LR421 and a built-in circuit board capacitor reduces trigger noise susceptibility.

The drain voltage for the input FET of the Preamplifier is provided by the circuit composed of VR420, R512, R515, and R516. Resistors R516 and R515 are part of the self-calibration circuitry and are used to match the gain of the CH1-BAL signal (pin 2) with that of the output of the attenuator.

## Channel 2 Preamplifier

Operation of Channel 2 Preamplifier U320 is nearly identical to that of the Channel 1 Preamplifier just described. The exceptions are that the signal obtained from the pickoff reverse-termination return (pin 11) is used to drive the rear-panel CH 2 OUT connector and that the signal from the positive trigger pickoff (pin 12) is used to drive the Video Option Back-Porch Clamp circuit (diagram 21). The output of that clamp circuit is an offset signal, applied to the Channel 2 Preamplifier at pin 3, that is used to remove ac power-supply hum from the display of a video signal applied to the Channel 2 input when the Video option is in use.

The amplified Channel 2 +PRTR signal from U320 pin 11 provides an accurate representation of the Channel 2 signal at the rear-panel CH 2 OUT connector. The + PRTR pickoff signal is applied to the emitter of Q240B via a voltage divider formed by R234, R241, and R240. Transistor Q240B, configured as a diode, provides thermal compensation for the bias voltage of Q240A and reduces dc level shifts with varying temperature. Emitter-follower Q240A provides the drive and impedance matching to the CH 2 OUT connector and removes the diode drop added by Q240B. Clamp diodes CR140 and CR141 protect Q240A should a drive signal be accidentally applied to the CH 2 OUT connector.

## External Trigger Preamplifier

The functions provided by External Trigger Preamplifier U100 are similar to those provided by the Channel 1 and Channel 2 Preamplifiers. The single-ended EXT TRIG 1 and EXT TRIG 2 input signals are buffered by U100 and routed to A/B Trigger Generator U150 (diagram 11) where they are available for selection as the trigger source for either the $A$ or $B$ trigger signal.

External trigger signal sensitivities may be set by the user to allow triggering ranges of either $\pm 0.9$ volts (EXT $\div 1$ ) or $\pm 4.5$ volts (EXT $\div 5$ ). Larger applied voltages on
the external trigger inputs will exceed the control ranges of the Trigger System. The logic levels of control bits applied to U100 pin 30 (GA3) and pin 31 (GA4) from Source Select Control Register U140 (diagram 5) set the gain of the EXT 1 and EXT 2 Preamplifiers respectively.

Dc offsets in the output signal due to any tracking differences between the +5 V and the -5 V supply to U100 are reduced by the Tracking-Regulator circuit composed of U120, Q110, and associated components. Operational amplifier U120 and Q110 is configured so that the output voltage at the emitter of Q110 follows the -5 V supply applied to R210. This tracking arrangement ensures that the supply voltages are of equal magnitude to minimize dc offsets in the output signals.

## PEAK DETECTORS AND CCD/CLOCK DRIVERS

The Peak Detectors and CCD/Clock Driver arrays (diagram 10) form what is essentially a very fast analog shift register. Waveform samples from each Preamplifier (U320 and U420, diagram 9) are loaded īnto the shift register array at a selected sample rate up to 500 Megasamples per second and clocked out of the array at a slower. fixed rate for digitization by the A/D Converter (see diagram 15).

Peak Detectors U340 and U440 are hybrid devices having two modes of operation: "track" and "peak detect." For NORMAL and AVG (average) acquisition modes, the Peak Detectors track the input signal and provide signal gain from the Preamplifiers to the CCD arrays. In the peak-detect mode used for ENVELOPE acquisitions at sweep speeds of 500 ns per division and slower, the Peak Detectors detect and hold the most positive and the most negative amplitude value of the input signal that occurs during each sampling interval. The peak values are amplified as in the NORMAL and AVG modes and applied to the input registers of the CCD arrays to produce a composite waveform of the most positive and most negative waveform amplitudes.

CCD/Clock Drivers U350 and U450 are hybrid devices containing a charge-coupled device (CCD) integrated circuit, a Clock Driver integrated circuit, and a symmetrydelay adjustment integrated circuit. The charge-coupled devices are very fast analog shift registers. Differential signals applied to the inputs of the CCD's from the Peak Detectors are sequentially clocked into the CCD registers at the processor-selected sample rate as determined by the SEC/DIV switch setting. Movement of the analog samples through the CCD arrays is controlled by the Clock Driver circuitry of the devices. Shifting the samples out of the CCD to be digitized is done with the combined clocking action of the internal Clock Drivers and the clock signals
supplied externally to the CCD via Q450, Q460, and Q551. All control logic for the CCD/Clock Drivers, with the exception of the RESET signal from the System Clock circuitry (diagram 7), is derived from Phase Clock Array U470 (diagram 11).

Signal samples from both vertical channels are continuously loaded into and shifted through the CCD arrays until a trigger event occurs. The Time Base Controller (U670, diagram 8) then allows a specific number of further analog samples to be shifted into the arrays depending on the number of post-trigger samples needed to fill the waveform record. That number is determined by the TRIG POSITION setting for the acquisition. When the necessary samples have been loaded into the arrays, sampling is halted. The differential analog samples stored in the CCD arrays are then shifted out of the CCD to the CCD Output circuitry (diagram 14) where they are conditioned and multiplexed to the A/D Converter to be digitized.

## Peak Detectors

The Peak Detectors provide peak detection, gain, and buffering of the CH 1 and CH 2 signals. Peak detection is enabled for ENVELOPE mode acquisitions, and then only when the acquisition rate is 500 ns per division and slower, but signal buffering is provided for all acquisition modes. Operation of both Peak Detectors is the same; therefore, the description is limited to the CH 1 circuitry. A simplified block diagram of the Peak Detector is shown in Figure 3-4.

Two user-selectable bandwidth limiters provide bandwidth reductions to either 20 MHz or 100 MHz for the signal through the Peak Detectors. With the Video Option installed, one of the 20 MHz limiter coils (L531 for CH 1) is adjustable to optimize the 20 MHz response for video signal operation. Without the option, both 20 MHz bandwidth limit coils for each Peak Detector are fixed values. The $100-\mathrm{MHz}$ bandwidth is adjusted by R431 for CH 1. The input stage of the Peak Detector is where bandwidth limiting is switched. Three bandwidth-select bits (FULL, 100 MHZ , and 20 MHZ ) applied from the Peak Detector Control register (U530, diagram 5) control the bandwidth. Only one control bit at a time is set HI, and that bit controls the input amplifier bandwidth accordingly.

The differential signal from the CH 1 Preamplifier is applied to the CH 1 Peak Detector (U440) on input pins 4 and 6. In ENVELOPE acquisition mode, two sets of two fast-peak detectors following the input stage are used to permit continuous peak detection of negative and positive peaks of the input signal. While the PDA fast-peak detector is detecting a negative peak, the PDB peak detector is holding the last peak or resetting and vice versa (see table in Figure 3-4). Each of fast-peak detectors is followed by a slow-peak detector to increase the peak-hold time to the

CCD input register. The outputs of the positive peak detectors are multiplexed to the differential OUTEVEN pins (pins 33 and 35) while the outputs of the negative peak detectors are multiplexed to the differential OUTODD pins (pins 26 and 28).

For NORMAL and AVERAGE acquisition modes, the Peak Detector operates in the track mode. To track the input signal and supply buffering only to the input signal, pin 21 (PD) is set HI and pin 22 (SLOW/FAST is set LO, and the differential peak-detector clock signals (PD1 and PD2) are held at fixed levels (PD1 LO and PD2 HI). The signals bypass the internal peak detector stages and proceed directly to the output stages. The differential outputs at OUTODD and OUTEVEN follow the input signal at a signal level of $200 \mathrm{mV} /$ division. Loading of the outputs is provided by resistor networks inside the CCD/Clock Driver which return to adjustable voltage sources VCC13 and VCC24 provided by the Common-Mode Adjust circuits (discussed later).

Peak detect mode for ENVELOPE acquisitions is turned on by setting $\overline{P D}$ LO at pin 21 and SLOW/FAST HI at pin 22 of Peak Detector U440. The differential ECL peakdetector clock signals (PD1 and PD2) toggle under control of the Phase Clock Array (U470, diagram 11) to control the internal peak detector switching and multiplexing of the positive and negative peaks to the OUTODD and OUTEVEN stages. The table in Figure 3-4 shows timing of the peak detector clocks and illustrates how alternate peaks are applied to the IN13 and IN24 inputs of the CCD.

Bias current for the input stage of U440 is set by R430 on pin 47, and output stage bias is set by R440 on pin 32.

The +CAL and -CAL inputs at pins 8 and 10 are identical to the signal inputs, but they are used only for the application of test signals during calibration or diagnostic testing. Selection of the inputs is controlled by the CALISIG signal. The test signals applied to pins 8 and 10 from the DAC System are used for testing and calibrating the Peak Detectors, the CCD/Clock Drivers, the CCD Output circuits, and the A/D Converter.

## Common-Mode Adjust

The Common-Mode Adjust circuits (U540A and B, Q540, Q640, and associated components) vary, under control of the System $\mu \mathrm{P}$, the common-mode voltage levels at the output of the CH 1 Peak Detector. (Similar circuitry performs the same task for the CH 2 Peak Detector.) These voltages are adjusted at instrument calibration to optimize CCD operation. The CH 1-OUTODD Common-Mode Adjust circuit is described; the remaining Common-Mode Adjust circuits operate identically.


Figure 3-4. Simplified Peak Detector block diagram.

## Theory of Operation-2440 Service

U540A, Q640, and associated circuitry are configured as an operational amplifier capable of high current output. This "op-amp" outputs a supply voltage as VCCODD to the Peak Detector, U440, and as VCC13 to the CCD/Clock Driver, U450. It compares VCCODD/VCC13 with the CM10DD control voltage suplied by the DAC system and varies VCCODD/VCC13 dependent on control voltage. Varying VCCODD/VCC13 controls the commonmode voltage levels at the peak detector outputs which, in turn, optimizes the CCD operation.

The op-amp configuration sources both the load current for the OUTODD Peak Detector's differential output stages, OUTODD+ and OUTODD-, as well as the VCCODD voltage supply to those output stages. Outputs OUTODD+ and OUTODD - always sink a common-mode current of $\mathbf{4 5 \mathrm { mA }}$. This constant current, sourced by R651 and Q640 of the op-amp, flows through internal load resistors inside the CCD/Clock Driver, U450. Since these resistors provide a common-mode load of $50 \Omega$, a constant 2.25 volts is dropped from the VCC13 source at pin 13 to the differential inputs IN13+ and IN13- at pins 11 and 12 of the CCD/Clock Driver.

If the CM10DD voltage set is changed by the System $\mu \mathrm{P}$, operational amplifier U540A compares the VCCODD level with the attenuated CM1ODD level output from the DAC System. The output of U540A drives Q640 to supply more or less current to its collector circuit. The constant 45 mA common-mode current drawn by pin 13 of U450 doesn't change; therefore, the change in current serves to raise or lower the supply voltage to the peak detector output stages at pin 25 of U440.

R651 reduces stress on Q640 by supplying part of the total current sourced to the peak detector outputs, via pin 13, U450, and the Voltage supply for those stages, via pin 24, U440. Emitter resistor R647 current-limit protects Q640 if a short or overload occurs. Resistors R647 and R651 also limit the voltage gain of Q640 to stabilize the feedback loop of the Common-Mode Adjust circuit.

## Charge-Coupled Devices (CCD)

The CCD portion of the CCD/Clock Driver hybrid is a MOS-type integrated circuit that functions as a very fast analog shift register. A signal applied to the input is sampled by being converted to charge packets. These charge packets are then shifted through the CCD registers by MOS-circuit gating at intervals determined by the clock rates applied by the Clock Driver integrated circuit portion of the hybrid. The internal arrangement of the CCD analog shift registers and the total amount of storage space permits the input signal to be sampled at a high clock rate when necessary for the higher frequency signals. The charge packet samples are temporarily stored and then shifted out of the CCD at a much slower rate than the sampling rate. An inexpensive A/D Converter can be used to digitize the signal and slower memory circuits used to
store the digitized samples. This type of operation is called Fast-In-Slow-Out (FISO) and is used at SEC/DIV settings of $50 \mu \mathrm{~s}$ and faster. At SEC/DIV settings of $100 \mu \mathrm{~s}$ and slower, the CCD runs with a constant clock rate of 500 kHz in a mode called Short Pipeline (discussed later).

A simplified diagram of one-quarter of one CCD is shown in Figure 3-5. The quarter shown, called Side 1, is nearly identical to the other three sides (2,3, and 4) of the CCD. Although all four sides of a CCD shift charge packets simultaneously, they take samples 90 degrees out-of-phase with each other, thereby achieving an effective sample rate of 500 Megasamples per second while clocking each CCD side at only an 8 ns rate.

Each of the four sides of each CCD can temporarily store 272 analog samples for a total of 1088 samples per channel. Although only 1024 samples are needed for conversion to the 1024-byte waveform record, the 64 extra samples are needed for proper clock switching between the Fast-In and Slow-Out portions of the FISO cycle.

The CCD has a Serial-Parallel-Serial (S-P-S) architecture. Each side has an 8 sample serial input " $A$ " register, an $8 \times 34$ sample parallel storage " $B$ " register, and an 8 sample serial output " $C$ " register. Two such SPS sections are shown in Figure 3-5.

In addition to the SPS registers, a fourth register is provided between the input node and the $A$ register. This register, called the Lead-in or $L$ register, is what distinguishes each of the four sides of the CCD and causes them to sample $90^{\circ}$ out of phase.

All the registers require two-phase, complementary-gate clocking to move the sample charge packets through the CCD. Hence, there are two A register clocks, two $B$ register clocks, and two C register clocks. There are four $L$ register clocks in order to produce the four sampling phases. There is also a Transfer In (TI) clock to shift samples from the serial $A$ register into the $B$ register and a Transfer Out (TO) clock to move them from the B register to the C register. All gates are driven with bipolar signals of nominally -5 V to +5 V .

Sampling into any of the CCD sides occurs on the falling edge of the first gate in the $L$ register. The interfaces between the $L$ registers and the corresponding $A$ registers are identical. However, by varying the length and clocking of the $L$ register, samples can be taken in different sides on each of the four L clock falling edges while still shifting all samples simultaneously into the A registers. The nomenclature of the sides corresponds to the number of the L clock which samples the charge packets into that side. Hence, a sample is taken first into side 1 , then side 2, and so on.

When charge packets arrive at the end of the C register, they are converted to an output voltage by the


Figure 3-5. Simplified CCD architecture.
output source follower amplifiers. The RESET clock discharges the output wells between output sample intervals so that charge does not accumulate at the input to the source-followers.

In FISO mode, 8 samples are shifted down the serial input of A register at a clock period equal to 0.08 times the SEC/DIV setting. On every eighth clock cycle, the positive A2 clock pulse is replaced by a single positive TI pulse that moves ail the charge packets into a transfer-in register at the head of the B register array. The A register is then empty and ready to accept new serial-in samples. The $B$ register clocks run at $1 / 8$ the speed of the $A$ register clock rate so that the A register will be filled prior to each B register clock. In this way, the B register is filled with samples that are moved in parallel through the array. During this Fast-In portion of the input cycle, unneeded charges that arrive at the output $C$ register due to the way the input signal is continually sampled (until a trigger occurs) are emptied from the CCD through the output diffusions (OD13 and OD24). When the Time Base Controller determines that the proper number of samples have been stored in the CCD after the trigger occurs, the mode changes to Slow-Out. The C register and RESET clocks then toggle at a constant 500 kHz rate to shift take samples out of the CCD to be digitized. The B register clocks pulse once during every eighth $C$ register clock cycle to shift charge packets into the $C$ register.

The Short Pipe mode of the CCD is in effect at SEC/DIV settings of $100 \mu \mathrm{~s}$ and slower. The CCD is operated at a continuous 500 kHz rate. Samples are shifted serially through the CCD via one B register channel only. The TI clock toggles continuously to move the sample charge packets from the first A register position into the active B register channel, shown in Figure 3-5 as the Short-Pipe Path.

All charge packets exit the CCD through the output diffusions (OD13 and OD24) which are biased at approximately 11 volts by operational amplifier U460A.

## Clock Drivers

The Clock Driver integrated circuits internal to the CCD/Clock Driver hybrids develop the two " $A$ " register clocks, the two " $B$ " register clocks, the four " $L$ " register clocks, and the transfer input (TI) and transfer output (TO) clocks for the CCD. The high-speed A, L, and TI drivers are differential class A drivers through thick-film load resistors on the hybrid. The B Register drivers are slower with active pull-up and pull-down totem-pole outputs similar to conventional TTL driver outputs. The TO gate is connected on the hybrid to the B2 gates and driven by the B2 driver output.

The L1 and L3 high-speed clocks are accessible at probe pins 18 and 19 of the hybrid devices. These pins (PL1 and PL3) are isolated from the actual CCD gates by internal 875- $\Omega$ series resistors. Terminate the signals into
$50 \Omega$ to view them. Using the standard $10 \mathrm{M} \Omega$ probe will cause the signals to have a displayed rise time of about 30 ns ; the actual rise time internally is less than 2 ns .

Bias current for the Channel 1 high-speed drivers is set by the feedback circuit of U360B and Q375. The drivers are biased by injecting current into the IS input (pin 37). Increasing the current makes the LO level of the highspeed clocks more negative; decreasing the current raises the LO level. The HI level of the clocks is always within a few hundred mV of the +5 V supply to the hybrid. For controlling the negative clock level, the common-mode level of the L1 and L3 clocks at the PL1 and PL3 outputs is applied to the input of U360A. This level is compared to the midpoint between the +5 V and -5 V supplies. Operational amplifier U360A drives the base of Q375 to a level such that the current injected into IS sets the common-mode level of PL1 and PL3 equal to the voltage at pin 3 of U360A (the voltage supply midpoint value). Since the HI clock levels at PL1 and PL3 are approximately at the +5 V supply level, the LO levels of the clocks then are set to approximately the -5 V supply level. Bias stability is thereby maintained over temperature and component variations.

The logic inputs for the A, L, TI, and B drivers are all ECL levels from U470, the Phase Clock Gate Array. Resistor array R470 provides proper termination for the ECL logic inputs to the CH 1 Clock Drivers. Fine adjustment of clock timing for the $\mathrm{L}, \mathrm{A}$, and TI clocks is necessary to insure that the CCD transfers charge optimally, and that samples are taken at the right times in each of the four sides. The symmetry-delay integrated circuits provide this adjustability. These circuits sit between the ECL logic inputs to the hybrid and the clock driver integrated circuit. They accept the ECL level inputs and produce ECL level outputs which have several nanoseconds of adjustability of both the rising and falling edges. R442 through R449 are the calibration adjustments for the symmetry and delay of the L, A, and TI clocks. The dc level, "V1P," applied to U460B's input by U470, is the internal ECL threshold voltage of U470. This threshold is buffered by U460B and provided as the reference for the ECL inputs to the symmetry-delay integrated circuits. This provides stable logic switching times without the need for true differential ECL logic between U470 and U450.
"C" CLOCK DRIVERS. These are external clock drivers consisting of Q450, Q460, and associated components. They provide the necessary -5 V to +5 V clock swings for the CCD C register gates. Each driver is simply an inverting buffer which accepts TTL inputs from the Phase Clock Array. During the Fast-In portion of the FISO acquisition cycle, the outputs of both drivers are held HI by the Phase Clock Array. During the Slow-Out portion of the cycle, and at SEC/DIV settings of $100 \mu \mathrm{~S}$ and slower, the C Clock Drivers toggle at a 500 kHz rate with a $50 \%$ duty cycle. When toggling, the C2 output is $180^{\circ}$ out-of-phase with the C1 output for normal two-phase clocking.

RESET DRIVER. This driver consisting of Q551 is identical to the C Clock Driver states. It takes the FESET signal input from U731C in the System Clocks circuitry (diagram 7). Like the C Clock Drivers, the Reset driver is driven HI during Fast-in and toggles at other times. The Reset driver output is held HI for only 200 ns of the $2 \mu \mathrm{~s}$ clock period.

## -2 V Regulator

A -2 V supply needed to terminate all of the highspeed ECL signals on the Main circuit board is formed by U580B and Q580. The circuit is a simple series-pass regulator with R585 and R586 developing the -2 V reference for operational amplifier U580B from the -5 V supply. Feedback is through R587. Collector load resistors R486, R487, and R488 limit the power dissipation of Q580 and protect it from possible short circuits of the -2 V supply.

## TRIGGERS AND PHASE CLOCKS

In this scope, the acquisition system continuously acquires input samples. When the user-specified number of "pretrigger" samples have been moved into the CCD arrays, the trigger system is allowed to recognize trigger events. Sampling of the signal input to the CCD arrays continues (with new samples pushing out old samples) until a trigger occurs. After the trigger, the number of "post-trigger" samples needed to fill the waveform record are moved into the CCD arrays and sampling is stopped. The acquired samples are then moved out of the CCD arrays, digitized, stored to memory, and displayed. The acquisition system then begins again to fill the "pretrigger window' for the next acquisition; and, when that has been done, the trigger system is enabled to look for the next trigger event.

The Trigger circuits (diagram 11) detect when the userdefined triggering conditions are met and then allow the acquisition to be completed. When the triggering signal limits defined by the user for slope, level, and variable holdoff are detected by A/B Trigger Generator U150, the resulting trigger output is applied to Trigger Logic Array U370, where triggering conditions of delay mode, delay time or delay events count, and optional trigger sources are taken into consideration. The Trigger Logic Array outputs several trigger-recognition and acquisition-control signals that cause the acquisition system to finish the "post-trigger" portion of the acquisition.

The Phase Locked Loop and CCD Phase Clock circuits (diagram 11) control sampling and shifting operations of the CCD/Clock Driver hybrid. The Phase Locked Loop synthesizes the 500 MHz sample clock driving the CCD Phase Clock Array. The CCD Phase Clock Array uses this "master" clock to generate other CCD clocks in accordance with mode data written to it from the System $\mu \mathrm{P}$.

## A/B Trigger Generator

The A/B Trigger Generator circuit, composed of U150 and associated components, provides for selection and analog-type trigger detection from five input signals for each of the A and B triggers. These are the CH 1 and CH 2 vertical inputs, the EXT 1 and EXT 2 trigger inputs, and the line-trigger input (A trigger only). Two multiplexers internal to U150 select one of these signals as the trigger source for A Trigger and one (excluding the LINE signal) for B Trigger. Source selection depends on the states of the SROA, $\overline{\text { SR1A, }}$ and SR2A (source select-A trigger) lines for the A Trigger and on SR0B, SR1B, and SR2B for B Trigger. The appropriate select bits are written into register U140 by the System $\mu \mathrm{P}$ whenever the operator makes a triggering condition change using the trigger source menus.

Control data from the System $\mu \mathrm{P}$ defining trigger mode, trigger coupling, and trigger slope are clocked serially (one bit at a time) from the CD (control data) line into two storage registers internal to U150. Clocking the $\overline{C C A}$ (control clock A) line moves the setup data to the A control register, while clocking $\overline{C C B}$ moves data to the $B$ control register. When the control data has been loaded, each trigger circuit begins comparing its selected input signal to the user-defined trigger level for that trigger channel.

When the defined triggering criteria are met for either $A$ or $B$, the associated trigger outputs (ATG, $\overline{\text { ATG }}$ for A Trigger: BTG, BTG for B Trigger) will go to their asserted (true) states. The exception is when the A Trigger holdoff has not finished (ATHO is still HI). When the holdoff ends, however, the next trigger event on the selected A Trigger input will assert the A Trigger output gates.

Each differential trigger gate is inverted and current buffered by a pair of differential transistors that allow quick response to the trigger edges by Trigger Logic Array U370.

## Trigger Logic

The Trigger Logic circuit consists primarily of Trigger Logic Array U370. The Trigger Logic Array provides final trigger-source selection; trigger-point delays, delayed either by a specified amount of time or by a specified number of events; and ramp-control signals to the JitterCorrection circuitry for resolving trigger-point ambiguities. The Trigger Logic Array also produces the trigger and external clock signals necessary to control operations of the CCD Phase Clock circuit.

The three enable inputs to U370, E1B (A3), E2B (WR), and E3B (ACQSEL), are all set LO whenever writing to addresses between 6080h and 6087h to enable the address inputs (A0, A1, and A2). The choice of eight addresses between 6080h and 6087h provides for different operating requirements of the Trigger Logic Array.

Depending on the address written to, one of the following actions may occur:

Mode control data may be loaded into the internal mode register.

The internal events and delay counter low-byte or high-byte of the number of events to be counted or delay may be loaded.

Various strobes used for internal control of the Trigger Logic Array may be generated.

Table 3-5 shows the action taken for each address selected.

Table 3-5
Trigger Logic Array Addresses
(6080h-6087h)

| Address Bits |  |  | Circuit Operation <br> Initiated |
| :---: | :---: | :---: | :---: |
| A2 | A1 | A0 |  |
| 0 | 0 | 0 | Restart Acquisition |
| 0 | 0 | 1 | Force Manual Trigger |
| 0 | 1 | 0 | Load Mode Control Data <br> from M0-M7 |
| 0 | 1 | 1 | Latch Delay Counter Low- <br> Byte from M0-M7 |
| 1 | 0 | 0 | Latch Delay Counter High- <br> Byte from M0-M7 |
| 1 | 0 | 1 | Load Delay Counter from <br> Delay Latches |
| 1 | 1 | 0 | Select Events in FISO, <br> Delay by Events, or Short <br> Pipe |
| 1 | 1 | 1 | Reset All Latches |

As previously mentioned, U370 provides final triggermode and source selection, dependent on data written from the System $\mu \mathrm{P}$ to a control register within U370 at address 6082 h . The mode control data byte loaded from the M0-M7 input bus is built by the System $\mu \mathrm{P}$ and applied to the M0-M7 (mode) inputs from serial-input register U270 (diagram 5) via the GAD0-GAD7 bus lines. The data byte defines the A Trigger source, B Trigger source, Record Trigger source, Jitter Trigger source, and whether a single event or multiple events are needed to produce a trigger. Bit definition is shown in Figure 3-6.

After the control data byte is loaded and the acquisition is restarted, Trigger Logic Array U370 waits for EPTHO (end of pretrigger holdoff) to go HI at pin 28, indicating that the acquisition system has sampled the "pretrigger" points
and is ready to complete the acquisition. With EPTHO set HI , the trigger logic begins watching the trigger source (as defined by the control data byte), waiting for a trigger event to occur.

Operation of the Trigger Logic Array is very sequential in the way it functions in the various trigger modes. An example is illustrated in the sequence of events for B RUNS AFTER trigger mode.

1. The System $\mu \mathrm{P}$ loads the "delay count" and "control mode" registers, then starts the acquisition (indicated by setting RSTACQ HI at TP370).
2. The Trigger Logic Array watches for EPTHO at pin 28 to go HI ; signaling that the defined number of pretrigger points have been sampled.
3. With EPTHO HI, the Trigger Logic Array watches MTG and $\overline{M T G}$ (main trigger gate) for an A trigger event to start the delay counter. When a trigger occurs, JTRIG (iitter trigger) is generated, starting the jitter-correction circuits (via the RAMP and RAMP signals).
4. The defined delay count is decremented to zero by the DELCLK (delay clock) signal on pin 67 from Phase Clock Array U470. If the mode were A Delayed by B Events, the B Trigger events would be used to decrement the delay counter.
5. In this example, when the internal Delay count reaches 0 , a RTRIG (record trigger) is generated for B RUNS AFTER. RTRIG is the "record trigger" point on the displayed waveform. If the mode were B TRIG AFTER, the Trigger Logic Array would begin watching for a B Trigger to occur on the DTG and DTG input pins (Delay Trigger Gate).
6. Time Base Controller 4670 (diagram 8) counts the post-trigger samples as they are acquired. When the required count is reached to complete the acquisition, it resets EPTHO to LO and further triggers from the Trigger Logic Array are prevented from being generated.

The Time Base Controller then starts moving digitized samples to the Acquisition Memory and, when finished, tells the System $\mu \mathrm{P}$ that the acquisition is done. The System $\mu \mathrm{P}$ may then restart the whole process again for the next acquisition by writing appropriate data to the various trigger registers.

In external clock mode, the differential EXTCK and EXTCK (external clock) signals to the Phase Clock circuit replace the normal master-clock (MCLK) signal and allows the $B$ trigger events to be used as the events delay source.

## CONTROL DATA BYTE

| A2 | A1 | AO | M7 | M6 | M5 | M4 | M3 | M2 | M1 | MO |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 1 | 0 | JT1 | JTO | RT1 | ATO | ONEVNT | BTO | AT1 | ATO |
| 1 | 1 | 0 | DON'T CARE |  |  |  |  | EVDEL | SELEVENTS | ABTRIG |


| JITTER TRIGGER BITS |  |  |
| :---: | :---: | :---: |
| JT1 | JTO | SOURCE |
| 0 | 0 | A TRIGGER |
| 0 | 1 | B TRIGGER |
| 1 | 0 | END EVENTS |
| 1 | 1 | B TRIGGER |

ONE EVENT BIT

| ONEVNT | EVENTS=1 |
| :---: | :---: |
| 0 | NO |
| 1 | YES |

A TRIGGER BITS

| AT1 | ATO | SOURCE |
| :---: | :---: | :---: |
| 0 | 0 | MAIN INST. TRIGGER |
| 0 | 1 | VIDEO TRIGGER OPTION |
| 1 | 0 | WORD TRIGGER OPTION |
| 1 | 1 | A*B TRIGGER |

SELECT EVENTS BIT

| SELEVENTS | MODE |
| :---: | :---: |
| 0 | FISO ONLY. NO EVENTS |
| 1 | DELAY BY EVENTS OR SHORT PIPE |

RECORD TRIGGER BITS

| RT1 | RTO | SOURCE |
| :---: | :---: | :---: |
| 0 | 0 | A TRIGGER |
| 0 | 1 | END DELAY TIME |
| 1 | 0 | END DELAY EVENTS |
| 1 | 1 | B TRIGGER |

B TRIGGER BIT

| BTO | SOURCE |
| :---: | :---: |
| 0 | DELAYED INST. TRIGGER |
| 1 | WORD TRIGGER OPTION |

deLay by events \& time bit

| EVDEL | MODE |
| :---: | :---: |
| 0 | NOT DELAY BY EVENTS AND TIME |
| 1 | DELAY BY EVENTS AND DELAY BY TIME |

AB COMBINATIONAL TRIGGER

| ABTRIG | SOURCE |
| :---: | :---: |
| 0 | A AND B |
| 1 | INTERNAL MODE ONLY |

Figure 3-6. Trigger Logic Array Control Data Byte.

The $\bar{A}$ TRIG and $\overline{\operatorname{R} \text { TRIG }}$ outputs from Q287 and Q288 are $T T L$-buffered versions of the corresponding trigger signals and are routed to rear-panel BNC connectors.

## Phase Locked Loop

The Phase Locked Loop circuit synthesizes the 500 MHz clock used by the Acquisition System. It consists of Phase/Frequency comparator U381 amplifier U580A, a voltage-tuned tank circuit, and a divide-by-50 counter internal to Phase Clock Array U470. The tank-circuit resonant frequency is set by the value of voltage-controlled capacitors CR580 and CR582. The resulting clock is divided by 50 by the counter and is applied to the phase-frequency detector U381 on the TENREF line. The TENREF signal is compared to the reference clock 10 MHz , and any phase or frequency error appears at the output of U381 as variable width pulses. These pulses are integrated by U580A to produce a dc voltage that represents the phase difference (fast or slow) and magnitude of error between the 10 MHz clock and the divided down master clock. This is the frequency-control voltage and varies the capacitance of varactor diodes CR580 and CR582, part of the tank circuit formed by the circuit board delay line, CR580 and CR582. The tank is tuned by the control voltage so that the master clock frequency is precisely 50 times the reference frequency.

## CCD Phase Clock

The CCD Phase Clock generates properly phased and frequency-related clocks that control most of the Acquisition system. These functions include moving samples into the CCD arrays, shifting within the arrays, jitter-correction control, peak-detection control, and trigger-delay clock generation. These clocks are derived from the 500 MHz master clock generated by the internal oscillator and the Phase Locked Loop circuit.

Two operating modes exist for the CCD arrays; FISO (fast-in, slow-out) and Short-Pipe. The Phase Clock circuit is set up to generate proper clocking signals for either mode by loading data into Gate Array Control Register U270 (diagram 5). This data is applied to U 470 on the CC0-CC4 (chip control 0-4) lines and on the PDOFF (peak detector off) line. The PDOFF line enables/disables the peak-detector output lines (PD1, $\overline{\mathrm{PD1}}, \mathrm{PD} 2$, and $\overline{\mathrm{PD} 2}$ ) and thus peak detection mode (see that description). The CC4 input controls whether the scope uses a non-Delay- or a delayed-by-time trigger source. If Horizontal mode is B and B Trigger Mode is B delay-by-time, is in normal (or delay by time trigger mode. When set high, the phase clock will choose the RTRIG signal as the trigger source for delay by time. If set low, the phase clock will choose JTRIG as the source. The CCO-CC3 inputs control operating mode and clock selection as shown in Table 3-6.

FISO MODE. As explained in the CCD description, each CCD is made up of two identical differential channels using a serial-parallel-serial (SPS) structure. Samples are moved into and shifted within the CCD arrays using properly phased, overlapping clocks. Figure $3-5$ shows a basic CCD structure (see CCD description, diagram 10).

Depending on which of the four sides of the CCD is being acquired, the corresponding sample gate (L1, L2, L3 or L4) will go HI. This moves the present level of the input signal into the input well of the CCD arrays. Before the sample gate returns LO, the $\phi 1 \mathrm{~A}$ (phase A1 register) clock goes HI and the charge is shared by the adjacent cells (input and $\phi 1$ ). When the sample gate returns LO, all charge moves to the $\phi 1$ cell. The $\phi 2 \mathrm{~A}$ clock then goes HI and charge is distributed into both the $\phi 1$ and $\phi 2$ cells. When $\phi 1$ returns LO, all charge will move into the $\phi 2$ cell.

When 8 samples have been acquired in the A register, the TI (transfer into B ) clock moves all 8 samples from the $\phi 1 \mathrm{~A}$ cells in parallel into the B register. The two phases of the B clocks shift samples down the 8 parallel B registers in a manner similar to that just described for the A register but at $1 / 8$ th the rate. The TTLB1 clock (TTL-version of B clock $\phi 1$ ) is output to the Time Base Controller and allows it to keep track of how many samples have been acquired (in multiples of 32). This allows the Time Base Controller to know when the proper number of "pretrigger" points have been acquired and when to enable the Trigger Logic Array.

Once enabled, the Trigger Logic Array begins counting its predefined delay while samples continue to be acquired. The DELCLK (delay clock) output to the Trigger Logic runs at one-half the sample-clock rate, allowing the Trigger Logic to complete any defined delay. When delay is done, the JTRIG and RTRIG signals may be generated. When the JTRIG occurs, the RAMP and RAMP signals from the Trigger Logic start the Jitter-Correction Ramps. The JTRIG signal to U470 causes the TLO and TL1 (trigger location-bits 0 and 1) bits to latch the phase (HI or LO) of the L1 and L2 clocks, defining in which quarter of the cycle the trigger event occurred. The internal slow-ramp logic circuitry of U470 becomes enabled and, on the next two edges of the master clock, asserts the two pairs of slow-ramp (SLRAMP) outputs. These outputs reverse the charge direction of the Jitter-Correction Ramp circuits (diagram 12) and start the Jitter-Correction Counters (diagram 13) on opposite edges of the master clock. See those descriptions for further information on trigger-jitter correction.

Depending on trigger mode, the RTRIG (record trigger) line will be asserted some time after JTRIG occurs. RTRIG is synchronized to the B-register clock and is output to the Time Base Controller on the SYNTRIG (synchronous trigger) line, telling it to start counting post-trigger samples. The RTRIG also loads a register internal to U470

Table 3-6
Phase Clock Array Control Lines (CC3 through CC0)

| SEC/DIV Setting | Control Bits |  |  |  | Mode |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | CC3 | CC2 | CC1 | CCO |  |
| EXT CLK | 1 | 1 | 0 | 0 |  |
| 100 ns and faster | 0 | 1 | 0 | 1 | FISO |
| 200 ns | 0 | 1 | 1 | 0 | FISO |
| 500 ns | 1 | 0 | 0 | 1 | FISO |
| $1 \mu \mathrm{~S}$ | 1 | 0 | 1 | 0 | FISO |
| $2 \mu \mathrm{~s}$ | 1 | 0 | 1 | 1 | FISO |
| $5 \mu \mathrm{~s}$ | 1 | 1 | 0 | 1 | FISO |
| $10 \mu \mathrm{~s}$ | 1 | 1 | 1 | 0 | FISO |
| $20 \mu \mathrm{~s}$ | 1 | 1 | 1 | 1 | FISO |
| $50 \mu \mathrm{~s}$ | 0 | 0 | 0 | 1 | FISO (Short-Pipe Clock Source) |
| $100 \mu \mathrm{~s}$ and slower | 0 | 1 | 1 | 1 | Short-Pipe |

with the present sample count to locate the trigger event (explained later). When the Time Base Controller has completed the post-trigger count, it will set SO (slow out) HI, switching the Phase Clock Array mode from "Fast In" to "Slow Out" mode. The various phase clocks are now derived from the 1 MHz 2XPC clock (from the Time Base Controller) instead of the 500 MHz master clock, and samples are shifted out of the CCD arrays at the A/D conversion rate.

Outputs TLO-TL4 (trigger location bits 0 through 4) define the trigger location within $\pm 1 / 2$ of a sample interval and allow the extra samples taken at the beginning and end of the CCD sample array contents to be discarded. Defining and discarding these samples is done because the trigger event may occur at any of 32 locations within the four A registers. Outputs TL2-TL4 locate the trigger at one of the eight sample positions within the A register, allowing samples before the start of the waveform to be discarded. Outputs TLO and TL1 define trigger position within the sample interval to one of the four sides (L1, L2, L3 or L4) by sampling the phase of the L clocks when the trigger occurred.

SHORT-PIPE MODE. A second acquisition mode, Short-Pipe mode, is used at SEC/DIV settings $100 \mu \mathrm{~s} / \mathrm{div}$ and slower. In Short-Pipe mode, the $\phi \mathrm{A} 2$ clock that transfers samples down the input (A) register is disabled; and instead, the TI (transfer into B array) clock shifts samples straight down the first register of the B array to the output well. Sampling occurs at 2 MHz in Short-Pipe mode ( 500 kHz each side of the CCD array) as the various
phase clocks are derived from the 2XPC clock. Trigger delays are generated at the SDC (slow-delay clock) rate since Short-Pipe mode connects the DELCLK output to the SDC input. Since sampling is occurring at a 2 MHz rate and the SEC/DIV is set so that a sample rate slower than this is required, some of the samples must be discarded. The discrepancy is resolved by Time Base Controller by counting and discarding the proper number of samples between those it allows to be saved. This allows effective sample rates much lower than the actual 2 MHz rate and, by routing the SDC signal to DELCLK, allows the trigger delays to be counted in terms of effective sample events.

In FISO mode, the TTLB1 (TTL-level phase B1) signal runs at $1 / 8$ of the A-register clock rate and is used by the Time Base Controller to keep track of how many FISO samples have been taken. Each TTLB1 clock indicates that 8 sample intervals have occurred. In Short-Pipe mode, the TTLB1 clock runs at the A-register clock rate. By using the TTLB1 count and the TLO-TL4 data, the Time Base Controller (U670, diagram 8) can precisely determine when the acquisition is finished.

TTLC2 is a TTL version of the phase 2 clock for the C (output) register and runs at all times except during RESET. This is one of the signals required by the System Clock Generators for producing correctly timed Output Sample Clocks to the CCD Output circuitry (diagram 14) and the RESET clock to the CCD arrays.

## JITTER CORRECTION RAMPS

The Jitter Correction Ramps located on diagram 12 are a portion of two dual-ramp timing circuits used to detect and measure the time difference between a trigger event and the sample clock. This information is needed when doing acquisitions at SEC/DIV settings greater that 100 ns to correctly place the data points obtained on different trigger events. The Jitter Correction Counters are located on diagram 13.

## Jitter Correction Ramps

Operation of the RAMP1 and RAMP2 circuits is identical; therefore, only the RAMP1 Jitter Correction circuit will be described. Both Jitter Correction Ramps are initiated by the same trigger event, but they are switched to their slow-discharge mode on opposite edges of the sample clock. By switching on opposite edges, the trigger point has two distinct references which define the trigger point, allowing the System $\mu \mathrm{P}$ to detect and correct for metastable states of the trigger recognition logic.

The ramp generator consists of a constant current source used to rapidly charge an integration capacitor when the trigger event occurs and a second current source used to discharge the capacitor (more slowly) after the proper edge of the sample clock occurs. The fastcharge time is the actual time from the trigger event to the appropriate sample-clock edge. The time it takes the slow-discharge mode to discharge C491 gives a numerical representation (counted) of how high the ramp level reached when C491 was fast charging; and therefore, the time of the fast ramp.

Fast charging rate is determined by the constant current source formed by U590A, Q493, and associated components. The charging current is nominally 50 mA through R590, R591, R593 and Q493. The voltage drop across the resistors balances the +7.5 volt reference at pin 2 of U590A and keeps Q493 turned on just enough to maintain the balance at the operational amplifier inputs.

This charge current is switched through either Q491 or Q492, depending on whether the ramp should be ramping down slowly or ramping up quickly. When waiting for a trigger to occur, the SLRMP1 (slow-ramp 1) will be LO, turning Q491 on. Charging current from Q491, which would normally charge integration capacitor C491 (and the 50 pF circuit-board capacitor), is shunted to -5 volts by Q490, which is turned on by a HI RAMP fast ramp) signal applied to its base.

RAMP CLAMPING. The clamping circuit made up of U590B, CR490, and associated components, holds the ramp summing-node voltage (collector of Q490) at zero volts while the circuit is waiting for a trigger to occur (signaled when RAMP and $\overline{\text { RAMP }}$ go to their true states). The
summing-node voltage is applied to U590B on pin 6 where it is compared to the zero-volt clamp level (ground) on pin 5. When the summing node attempts to go below ground while Q490 is on, U590B will conduct more to maintain the balance at the input pins, thereby clamping the summing node at zero volts via R592 and CR490.

Transistor Q380 and its associated components clamp the positive peaks of both ramps at +3.2 volts via CR491. This clamping takes place at SEC/DIV settings slower than $100 \mathrm{~ns} / \mathrm{div}$ because the SLRMP signal doesn't occur soon enough after the RAMP signal starts the ramp to reverse the ramp slope before the +3.2 V level is reached.

RAMP SWITCHING. When Trigger Logic Array U370 (diagram 11) detects that a trigger event has occurred, it sets the RAMP and $\overline{\text { RAMP }}$ signals to their active (true) states. The LO RAMP signal turns Q490 off to allow the integration capacitor to begin a fast charge, and the HI RAMP signal turns Q392 on to reverse bias CR490 and remove the clamp circuit from the summing node.

The charging current now linearily charges C491 and the circuit board capacitance positive (holding STOP1 LO through U 490 ) until the proper edge of next sample clock occurs (see Figure 3-7). This switches the SLRAMP1 and SLRAMP1 signals to their true states, turning off Q491 and turning Q492 on.

With Q492 on, the charging current is routed through R497, producing a HI START1 signal and enabling the RAMP1 Jitter Correction Counter circuit (diagram 13). Since Q491 is now off, C491 begins the slow-ramp discharge through Q495 and R493. When the voltage held on C491 crosses the switching threshold of U490, STOP1 is switched HI to turn off RAMP1 Jitter Correction Counter at the proper count.

At the time of calibration, the JIT1 GAIN (jitter gainramp 1) value is set to the base of the discharge current source transistor, Q495, so that the ratio between charging rate and discharging rate is 1250:1 (approximately 20 mA from the charging current source to approximately $16 \mu \mathrm{~A}$ discharge current from Q495). The slow discharge time of C491 allows the RAMP1 Jitter Correction Counter to convert the peak amplitude of RAMP1 (dependent on the time that C491 was allowed to fast charge) into a count relating trigger-event position to the sampleclock edge.

> After the Jitter Counter has been read, the RAMP, RAMP, SLRAMP1, and SLRAMP1 signals will be reset to their inactive states. This again clamps the summing-node voltage at zero volts and reapplies the charging current to the node in preparation for the next trigger event.

RAMP2. As mentioned earlier, the RAMP2 Jitter Correction circuit is running simultaneously, referenced to


Figure 3-7. Jitter Correction waveforms.
the opposite edge of the sample clock. The RAMP2 Jitter Correction Counter produces a count defining the trigger point relative to the opposite edge of the sample clock. Since both ramps have a possibility of an error in their slow-ramp starting times (due to metastable switching of the SLRAMP1 and SLRAMP2 signals) there will always be a chance of error present in the trigger-position count. The count from both ramps is checked, and the value closest to the nominal midrange count will be used by the System $\mu \mathrm{P}$ when placing the repetitively sampled data points. If both counts are in error, that acquisition is discarded.

## TRIGGER HOLDOFF, JITTER COUNTERS, AND CALIBRATOR

Circuitry shown in diagram 13 performs a variety of functions.

The Trigger Holdoff circuits allow a delay to occur between the occurrence of a triggering event and when the A/B Trigger Generator is allowed to recognize another trigger event. Variable Holdoff can help the user prevent double triggering on aperiodic signals (such as complex digital words).

The RAMP1 and RAMP2 Jitter Correction Counters measure the time difference between the asynchronous trigger event and the actual sampling point of the waveform data. That information is needed by the System $\mu \mathrm{P}$ to place the random samples taken in REPET acquisition mode correctly with respect to data points taken in the previous acquisitions to fill the waveform record.

The Calibrator circuit generates a square-wave output having precise amplitude and frequency characteristics. The CALIBRATOR signal provided at the front-panel connector is useful for adjusting probe compensation and verifying VOLTS/DIV and SEC/DIV calibration.

The Side Board Address Decoder included in the circuitry is used by the System $\mu \mathrm{P}$ to enable the appropriate register or buffer on the Side board to read the Jitter Correction Counters, select the Holdoff Time, and communicate with the Front Panel $\mu \mathrm{P}$.

## Trigger Holdoff

The Trigger Holdoff circuit consists of a trigger-enabled, constant current source (actually one of three selectable sources added to a small permanent source) used to
linearly charge a capacitor (one-of-two selectable cap values). The resulting integrator output is a linear ramp whose slope depends on the current-source and integration-capacitor selection. The ramp is applied to the Holdoff Comparator where it is compared to the userdefinable (front-panel pot) holdoff-reference level. When the charging ramp crosses that level, the ramp rapidly discharges (resets) and ends the holdoff condition.

## Holdoff Select

The Holdoff Select circuit, under System $\mu \mathrm{P}$ control, determines which of the Holdoff Current Sources and which of the integration capacitors will be used to produce the holdoff ramp. Its outputs are set by the microprocessor by writing data into Holdoff Register U762, residing at address 620Ch. Output bits HOO through HO2 (holdoff control bits 0-2) enable their corresponding current-source transistor when HI. Bit HO3 is used for selection of the integration capacitor. The FPRESET bit allows the system processor to reset the Front Panel $\mu \mathrm{P}$ (diagram 3).

Buffer U761, residing at read location 602Ch, allows the System $\mu \mathrm{P}$ to check the holdoff circuit setup and to monitor the status of the A Trigger (ATG) and trigger holdoff (ATHO) bits.

## Holdoff Current Sources

The Holdoff Current Sources provide the constant currents used to charge the integration capacitors (producing a linear ramp). The circuit consists of four transistor current sources, three of which may be turned on or off under control of the Holdoff Select circuit.

The bases of the four current-source transistors, Q761, Q771, Q772, and Q773, are held one diode-drop below +5 V by CR772 and R773. This results in precisely +5 V being present on the emitter of any conducting currentsource transistor. The amount of current is set by the value of emitter resistor(s). Transistor Q773 will always be on while the other three current-source transistors can be turned on or off by the HO control bit via the associated emitter diodes. A LO at the cathode of one of these diodes will disable the associated current source by reverse biasing the transistor junction; a HI at the cathode of a diode enables the charging-current source via the associated emitter resistor.

## Charging Capacitor Selection

The Charging Capacitor Selection circuit composed of Q783, Q782, and associated components, selects the integrating capacitance. The magnitude of the charging current from the selected current source, in combination
with the capacitance value, of the integration capacitor, determines charge rate (slope) of the holdoff ramp; and thereby, the holdoff time. Table 3-7 illustrates the holdoff time as a function of the selected current source and charging capacitor.

Charging current is stored on capacitor C882 when holdoff intervals less than or equal to $10 \mu \mathrm{~s}$ are desired. For longer holdoff periods, capacitor C881 and C885 are placed in parallel with C882 by turning Q782 on. Transistor Q782 turns on when HO3 (holdoff select 3) is LO, turning Q783 off. This pulls the gate of Q782 high and turns it on, placing the parallel combination of C881 and C885 in parallel with C882. Due to the relative capacitance ratios (1000:1), C881 is the dominant integrating element in the three-capacitor parallel combination.

## Holdoff-Ramp Comparators

Two Holdoff-Ramp Comparators, U871 and U881, watch the holdoff ramp. Comparator U871 compares the ramp level to the user-defined reference level while U871 compares it to a predefined "end-ot-holdoff" level.

Initially, a HI on the $\bar{Q}$ output of Holdoff Logic flip-flop U872A keeps Q781 turned on. The integration capacitors are discharged, and all the charging current is being shunted away from the capacitors through Q781. The user-definable holdoff reference applied to U871 pin 2 via R863 will always be more positive than this discharged level, so the output of U871 applied to the Holdoff Logic will be HI. This removes the reset from the Holdoff Logic flip-flop U872A and enables the occurrence of a trigger event (ATG going HI ) to clock it.

When a trigger event occurs, discharge transistor Q781 turns off, allowing the selected integrating capacitors to charge. When the charging ramp reaches the user-defined

HOREF (holdoff reference) level, the output of ramp comparator U871 will go LO. This resets flip-flop U872A of the Holdoff Logic which, in turn, turns Q781 back on.

The low-impedance path through Q781 discharges the integration capacitor very rapidly. When this discharging ramp crosses the -4.6 volt level (defined by R887 and R888), the output of U881 will go LO, resetting the Holdoff Logic circuit. This ends the holdoff pulse and allows the next trigger to be accepted.

Transistor Q781 remains on until the next trigger event, at which time the cycle repeats itself. Propagation delays through the Analog Trigger and the Record Trigger devices ensure that the discharging ramp will always reach the -5 V level before another trigger event can start the next holdoff ramp.

## Holdoff Logic

The Holdoff Logic initiates and controls the holdoff ramp and produces the holdoff pulse controlling the delay between one trigger event and the next. It starts the holdoff ramp when a trigger event is detected, begins ramp discharge when the user-defined HOREF level is reached, and ends the holdoff pulse when the ramp crosses the "end-of-holdoff" level.

Initially, the Set and Reset inputs of U872A will be HI , allowing the flip-flop to watch the ATG (analog trigger) line for a trigger event. While it is waiting, its $\bar{Q}$ output will be $\mathrm{HI}_{\text {, }}$ keeping Q781 on and the integration capacitors discharged.

When an ATG occurs, the HI level at the input of the flip-flop is clocked to the Q output while the $\bar{Q}$ output goes

Table 3-7
Holdoff Delays vs Current Source/Charging Capacitor Combinations

| Charging <br> Capacitor | Holdoff Delay Range |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  | Current Source |  |  |  |  |
|  | $909 \mu \mathrm{~A}$ | $90.0 \mu \mathrm{~A}$ | $9.09 \mu \mathrm{~A}$ | $827 \mu \mathrm{~A}$ |  |
|  | $10 \mathrm{~ns}-$ | $100 \mathrm{~ns}-$ | $1 \mu \mathrm{~s}-$ | D |  |
|  | 100 ns | $1 \mu \mathrm{~s}$ | $10 \mu \mathrm{~s}$ | E |  |
| $1.1 \mu \mathrm{~F}$ | $10 \mu \mathrm{~s}-$ | $100 \mu \mathrm{~s}-$ | $1 \mathrm{~ms}-$ | 10 ms | L |

LO. This LO turns Q781 off and allows the selected current source(s) to charge the capacitors. At the same time, the LO is applied to pin 10 of U872B, forcing its $Q$ output HI. This is the ATHO (analog trigger holdoff) signal and indicates that an analog trigger has occurred. This signal is applied to A/B Trigger Generator U150 (diagram 11) to prevent it from recognizing another trigger until the holdoff time ends.

As the charging ramp reaches the user-defined (frontpanel Holdoff pot) reference level, the output from comparator U871 will go LO. This CROSS (reference crossing) level is applied to U872A and resets the flip-flop. The $\overline{\mathbf{Q}}$ output, now HI, turns Q781 on and begins discharging the ramp at a rapid rate. The $\mathrm{HI} \overline{\mathrm{Q}}$ output from U872A removes the Set level from U872B and allows the ENDHO (end of holdoff) level from U881 to reset the ATHO level LO when the discharging ramp reaches -4.6 volts.

As mentioned earlier, propagation delays in the $A / B$ Trigger Generator and the Trigger Logic Array ensure that another trigger (ATG) will not occur until Q781 has discharged the integration capacitors fully to -5 V . This ensures that holdoff ramps always start from a known point, and thus maintains holdoff stability.

The width of the ATHO pulse represents the time from which one analog trigger event was accepted to when the next trigger event is allowed (next acquisition record). By varying this time (front-panel Holdoff control) the displayed waveform may be adjusted to exclude undesired trigger events (which may cause display instability).

## Jitter Correction Counters

The RAMP1 and RAMP2 Jitter Correction Counters convert the discharge time of their associated Jitter Correction Ramps to binary numbers relating trigger-event positions to the edges of the sample clock. Since operation of both Jitter Correction Counters is identical, only the RAMP1 Jitter Correction Counter will be described.

The RAMP1 Jitter Correction Counter is a twelve-bit counter that is started and stopped by signals from the RAMP1 Jitter Correction circuit. It counts the 40 MHz clock pulses over the interval when the Jitter Correction Ramp is discharging, thus converting the peak value of the ramp to a binary number. Since that value is directly proportional to the time difference between a trigger event and the next sample-clock edge, the number derived by the counter gives a precise time measurement of where the trigger occurred with respect to the sampled data. That information is used by the System $\mu \mathrm{P}$ to correctly place the random-sampled data points obtained in REPET acquisition mode with respect to the previously acquired random data points as the waveform record is filled.

Initially, the upper eight bits of the RAMP1 Counter (composed of U852A and U852B) are held reset by the HI from pin 6 of U841A, and the lower four bits are reset by the LO from pin 5. When the START1 (start counter 1) input goes HI (signaling start of the slow discharge of integration capacitor C491, located on diagram 12), the rising edge of the next 40 MHz clock pulse will enable the counter by clocking the Q output of U841A HI. The Q output of the "stop" flip-flop U841B is LO and enables U851B to pass rising-edge clock pulses to U844 at a $40-\mathrm{MHz}$ rate.

The counter increments until the RAMP1 Jitter Correction circuit detects that the discharge threshold has been crossed. When this occurs, STOP1 (stop counter 1) applied to U841B will go HI . The next rising edge of the 40 MHz clock disables U851B via U841B and stops the counter.

The System $\mu \mathrm{P}$ may then read the counter contents via U752 at address-decoded location 620Eh and via U750 at 620Ah. Counter contents for the B Jitter Correction Counter may be read at location 620Fh and 620Ah.

When the jitter ramps are reinitiated (in preparation for the next trigger event), the START1 and STOP1 signals will return LO. The next rising edge of the 40 MHz clock will reset the Jitter Correction Counter by clocking pin 6 of U841A HI.

## Address Decoder

Address Decoder $\mathbf{U 7 8 1}$ monitors the address bus to determine when various buffers and registers on the Side board are to be enabled for communication with the System $\mu \mathrm{P}$. Table 3-8 illustrates this decoding.

Table 3-8
Side Board Address Decoding

| Address (hex) | Selects or Enables |
| :---: | :--- |
| 6208 | LED Register |
| 6209 | Front-Panel Register |
| 620 A | Read lowest four bits of both Jitter |
|  | counters |
| 620 B | No connection |
| 620 C | Write/Read Holdoff Register |
| 620 D | Set Holdoff Flip-Flop |
| 620 E | Read Jitter Correction Counter 1 |
| 620 F | Read Jitter Correction Counter 2 |

## Calibrator

The Calibrator circuit is composed of U731, U831, Q831, and associated components. Output frequency is set by the CALCLK signal from the Time Base Controller (diagram 8). The output frequency follows the SEC/DIV setting from $50 \mathrm{~ns} / \mathrm{div}$ to $20 \mathrm{~ms} / \mathrm{div}$ and is set to display from 2.5 to 10 calibrator cycles across the ten graticule divisions over those settings. This feature allows quick and easy verification of the acquisition time base rates. The Calibrator circuitry is essentially a voltage regulator that is switched off and on, producing a square-wave output signal at the CALIBRATOR loop.

When the CALCLK (calibrator clock) signal, at the base of U831D (applied via R885) is LO, U831C (configured as a diode) is forward biased. This shunts bias current away from Q831, keeping it turned off. When Q831 is off, the front-panel CALIBRATOR output is pulled to ground potential, through R831, thereby setting the lower limit of the CALIBRATOR square-wave signal.

As the CALCLK signal goes from LO to HI , the base of U831D is pulled HI, reverse biasing U831C. Bias current for Q831 now flows through R834 and R835, turning it on. The voltage at the emitter of Q831 rises to a level of +2.4 volts, determined by the voltage regulator composed of U731, U831A, U831B, Q831, and associated components. This regulated level is divided down to +400 mV p-p, by the resistive divider formed by R832 on the side board and R102 on the main board, and applied to the front-panel CALIBRATOR loop at an effective output impedance of $50 \Omega$.

## CCD OUTPUT

The CCD Output circuits (diagram 14) convert the four differential output signals from each CCD into single-ended signals for subsequent $A / D$ conversion. The single-ended analog voltages are applied to Track-and-Hold circuits where they are held until the time-multiplexed A/D Converter digitizes the stored samples.

## Gain-Cell Amplifiers

There are eight identical Gain-Cell amplifiers (two on each of four Gain-Cell circuit boards) used to convert the eight differential CCD array outputs (four for each channel) to single-ended signals for $A / D$ conversion. Operation of the Channel 1, Side 1 Gain-Cell amplifier is described.

CCDO11 signal outputs from U450 pass to the Gain-Cell board (diagram 14A), where they are applied to the bases of U111A, U111B, U111C and U111D via R113 and R114. Transistors U111A-U111D, along with currentsource transistors Q111 and Q112, form a variable-gain differential- current amplifier. The differential current at the collectors of U111B and U111C is equal to the differential current through U111A and U111D, multiplied by the ratio of the dc current for the Q112 current source to that of the Q111 current source. Since the Q111 current is set by the fixed bias on the its base-emitter circuit, the gain adjustment of the amplifier is controlled by the dc voltage at the base of Q112, which is controlled by the System $\mu \mathrm{P}$ via the DAC system. The gain set is dependent on a calibration constant determined at instrument selfcalibration.

The collectors of U111C and U111D are connected to operational amplifier U118A, which is configured as a differential-input, single-ended output transresistance amplifier. The connection of R115 to the +8.5 V supply causes the output of U118A to be level shifted to +8.5 V . The resulting output at pin 1 of U770A (GC11) is a levelshifted, amplified, single- ended replica of the differential CCD array output signal, with most common-mode interference removed.

## Track-and-Hold Amplifiers and Multiplexers

The Track-and-Hold Amplifiers and Multiplexers allow a single A/D Converter to digitize all the analog samples from all CCD arrays by time-multiplexing the output samples to the single converter. The eight Track-and-Hold circuits are identical; and, for brevity, only the CH 1Side 1 circuitry will be described.

The GCX output from the A30 gain cell board (GC11) is applied directly to sampling switch U560A, an enhancement-mode MOS-FET device. The switch gate is controlled via Q660 by the OSAM1 (Output Sample from Channel 1) logic signal, and is closed when the data being shifted out of the CCD is stable. When OSAM1 is LO, the switch is on, and hold capacitor C774 charges to the signal level of GC11. When OSAM1 is HI, the switch is off, and C774 holds its voltage level. Figure 3-3 (shown previously in the "System Clocks" description) shows the timing of OSAM1 and OSAM2 during the Slow-Out and ShortPipe modes of CCD operation. During Fast-In mode, $\overline{\text { OSAM1 }}$ and OSAM2 are both held LO.

The level stored on Hold capacitor C774 is buffered by operational amplifier U770A. The operational amplifier, along with Q774, converts the applied input sample voltage to output current.

## Theory of Operation-2440 Service

Selection of the CH 1-Side 1 current signal to be digitized by the A/D Converter is controlled by the MS11 (Multiplexer Select-Channel 1-Side 1) line. As shown in Figure 3-3, only one of the eight MS signals will be LO at any time. A LO $\overline{\mathrm{MS} 11}$ signal applied to the base of Q773 will turn that transistor off. The other transistors of CH 1 (Q873, Q770 and Q870) and all of the CH 2 transistors (Q783, Q883, Q780 and Q880) are on to shunt their associated signal currents to ground. Each of the eight shunting transistors will be turned off in sequence to allow its associated signal current to pass to the CCD DATA node via a series common-base transistor (Q775 for Channel 1 -Side 1). The resulting CCD DATA signal is a time-multiplexed combination of all eight CCD output channels (four from CH 1 and four from CH 2 ).

Precise current matching of the signal offsets for the four sides of Channel 1 is achieved by setting the DACgenerated CT11 (Center 11), CT12, CT13 and CT14 voltages at self-calibration. Similar offset matching for CH 2 is done with the CT21, CT22, CT23 and CT24 signals.

## Secondary Supplies

The Secondary Supplies circuit, composed of U861A, U861B, U861C, U861D, and associated components, provides operating voltages used by the CCD Output circuitry. The voltage level of the A2D REF ( -0.5 V analog-to-digital reference) is determined by the current through R861 from operational amplifier U861C and is set by the resistive divider string formed by R763 and R764 from the +10 VREF supply. The other voltage outputs ( +8.5 V and +10 VRA and +10 VRB are set by the various taps on the resistive voltage divider and buffered by operational amplifiers.

## A/D CONVERTER AND ACQUISITION LATCHES

The $A / D$ Converter and Acquisition Latches (diagram 15) circuit consists of eight-bit A/D Converter U560, eight-bit Min-Max Comparator U740 and U732 (for ENVELOPE acquisitions), Acquisition Latches U631, U632, U630, and U640, and latch switching circuitry to direct and latch the acquired data point values.

## A/D Converter

A/D Converter U560 is an 8-bit flash converter that digitized the analog samples from the CCD arrays at an overall conversion rate of 4 MHz .

The A2D REF voltage ( -0.5 V ) is amplified and inverted by $U 880$ to produce the 1.5 V reference voltage used by the A/D Converter. Noise and ripple are filtered from the amplified reference voltage by L770, C570, and C776. The negative side of the reference is tied to ground; therefore, input voltage for conversion may range from 0 V to +1.5 V . The time-multiplexed CCD Data signal current develops a voltage across R880 that is offset by the A2D REF voltage. It is then amplified and inverted by U780 to produce an input signal to the $A / D$ Converter within the 0 V to +1.5 V range needed. The amplified signal is applied to the analog input of U560 after being filtered by L780 and C770.

The input sample is converted on the falling edge of SHIFT, a 4 MHz clock signal. A valid data byte representing the analog input voltage appears on the output of the A/D Converter approximately 20 ns later. That data byte is applied to the 8 -bit Magnitude Comparator formed by U740 and U732, with the four LSBs going to U740 and the four MSBs of the byte going to U732.

## Envelope Min-Max Comparator

For ENVELOPE Mode acquisitions, glitch-catching at the slow SEC/DIV settings is done by the Envelope MinMax Comparator circuit formed by four-bit comparators U740 and U732. At SEC/DIV settings slower than $50 \mu \mathrm{~s}$, analog Peak Detectors U440 and U340 provide more samples than needed to fill the required 50 data points ( 25 min-max pairs) per division, so not all are saved. During each envelope sampling interval ( $1 / 50$ of the SEC/DIV setting at $50 \mu \mathrm{~s}$ and slower), the Min-Max Comparator compares every Peak Detector min/max value from A/D Converter U560 to the last-latched maximum or minimum byte to determine which sample will be saved. If the new byte value is greater than the latched byte value, the MAX output of Comparator U732 (pin 5) will go HI ; if less than the latched value, MIN at pin 7 will go HI . If the A/D output value is equal to the latched value, both connected outputs of Magnitude Comparator U732 will remain LO. The final min byte and max byte obtained from each channel during an envelope sampling interval are saved to the Acquisition Memory as part of the envelope waveform record.

Since the input to the A/D Converter is time multiplexed between CH 1 maximum, CH 2 maximum, CH 1 minimum, and CH 2 minimum values from the Peak Detectors, the latched data applied to the Magnitude Comparator from the Max/Min Latches must also be time multiplexed to maintain the correct relationship for making the comparisons (CH 1 maximum against CH 1 maximum, CH 1 minimum against CH 1 minimum, etc.). The necessary time multiplexing is done by the Envelope Latching Logic circuitry.

## Acquisition Latch Switching

NORMAL MODE ACQUISITIONS. In non-envelope mode, the LOAD LATCHES signal from the Time Base Controller remains in its HI state, With LOAD LATCHES HI at one of the inputs of OR-gates U512A and U512B, the MIN and MAX signals from the Envelope Min-Max Comparators are ignored, and the outputs from the gates are held HI. This causes each sample from the A/D Converter to be clocked directly through the Acquisition Latches.

Output enabling of the four Acquisition Latches is controlled by the MS13+MS11, MS12+MS14, MS23+MS21, and MS22+MS24 multiplexer select lines, which are logically ANDed combinations of the lines that control the multiplexing of the CCD analog samples to $A / D$ Converter U560. The states of these select lines, only one of which may be HI at a time, are latched into the four flip-flops of U520 and U521 by the 20 MHz system clock (C20M1). The $\bar{Q}$ outputs of the flip-flops control output enabling of the four Acquisition Latches. One at a time, their outputs are enabled to apply the acquired data point to the output bus for transfer to the Acquisition Memory input buffer (U613, diagram 8). After one of the Acquisition Latches has been enabled for 100 ns , the rising edge of the CLKLATCH signal clocks the HI state present on the D inputs of the flip-flops of U510 and U511 to the Q output of the enabled flip-flop. That rising edge then clocks the data byte from the A/D Converter through the enabled Acquisition Latch to the input buffer of the Acquisition Memory.

ENVELOPE MODE ACQUISITIONS. In ENVELOPE MODE, the LOAD LATCHES signal input to U512A and U512B (from the Time Base Controller, diagram 8) forces each clock flip-flop in turn to clock the A/D Converter output data byte into its associated latch by holding their D inputs HI during the first four data point conversions in each envelope sampling interval. These first four samples (one byte in each Acquisition Latch) initialize the min/max data in the latches for comparison to the remaining data samples that occur in the envelope sampling interval.

The Acquisition Latch Switching circuitry multiplexes the latched CH 1 and CH 2 maximum and minimum data bytes to the inputs of the Envelope Min-Max Comparator so that each digitized sample from the A/D Converter is compared to the correct previous sample (CH 1 Min to the previous CH 1 Min , etc.). (Note-odd sides of the CCDs are minimums, even sides are maximums.) It also provides the proper enabling and clocking to direct a new maximum or minimum data bytes into the correct Acquisition Latch.

As in NORMAL Mode acquisitions, output enabling of the four latches is controlled by the MS13+MS11, $M S 12+M S 14, M S 23+M S 21$, and MS22+MS24 select
lines. The $\bar{Q}$ outputs of the flip-flops control output enabling of the four latches, causing the Acquisition Latch corresponding with the selected CCD output (CH 1 or CH 2, maximum or minimum) to apply the previously latched data byte to the inputs of the Envelope Min-Max Comparator. A/D Converter output data is thus always being compared to the proper maximum or minimum data value.

When the Envelope Min-Max Comparator detects that the $A / D$ Converter output byte value is either above or below the latched byte value, the MAX or MIN output of U732 will go HI respectively. The HI is passed through U512A (MIN) or U512B (MAX) to the D inputs of flip-flops U510 and U511. Since the A/D Converter output byte value could represent any of the four CCD array channels, the multiplexer select lines that determine what sample is currently being output from the CCD arrays are applied to the reset inputs of U510 (A and B) and U511 (A and B). Only that clocking flip-flop corresponding to the selected data sample is enabled by a HI data select line; all others remain in the RESET state.

When the CLKLATCH ( 4 MHz ) clock occurs, the enabled clocking flip-flop transfers the level at its D input to its Q output, LAxMAX (latch $\mathrm{CH} \times$ max). If that level is a HI (a new max has been found), the current A/D Converter output data byte (the new max) will be latched into the associated Max Latch (either U632 or U631, depending on whether it is CH 1 or CH 2 data), where it then becomes the new comparison level, MIN clocks are produced by U510B and U511A in a similar fashion, latching the new MIN values into either U640 or U630.

## Acquisition Latches

During Envelope Mode, the Acquisition Latches perform as Min-Max latches (U631 and U632 Max; U630 and U640 Min) to hold the maximum and minimum data point values being compared during the sampling interval. These values are compared to each newly converted waveform sample to determine when new maximums or minimums occur. Output enabling and data latching are controlled by the Acquisition Latch Switching as previously described.

## DISPLAY AND ATTRIBUTES MEMORY

The Display and Attributes Memory (diagram 16) is where the Waveform Processor stores waveform and readout data that is to be displayed on the crt. Digital-toAnalog converters (DAC), under control of the Display Control circuits, convert this stored data to the verticaland horizontal-deflection signal currents that drive the Display Output amplifiers.

## Vertical Display RAM

Vertical Display RAM U431 stores the verticaldeflection data for four 512-point waveforms. Data points to be displayed are written from the Save Memory into the RAM by the Waveform $\mu \mathrm{P}$ (diagram 2) on the WD bus (waveform data bus) via bus transceiver U322. The stored waveform display bytes are read sequentially out of the Vertical Display RAM in blocks under control of the Display Counter (diagram 17) and applied to Vertical DAC U142 to produce the analog vertical deflection signal of the displayed waveform.

To write data into the Vertical Display RAM, the Waveform $\mu \mathrm{P}$ puts the data byte to be written onto its WD bus and sets its $\overline{W R D}$ (waveform read) bit HI. This HI enables bus transceiver U322, and the vertical data is applied to I/O (in/out) pins of the RAM. At the same time, the $\overline{\mathrm{DISP}}$ signal is address decoded LO (from decoder U570, diagram 2) for addresses between 8K and 12 K , and the WAB address bit applied to U323B selects the Vertical RAM U431 via U421A. When the Waveform $\mu \mathrm{P}$ generates its write pulse (WWR), it is transmitted through U422A and U422D, writing data into the Vertical Display RAM. This process occurs for each data byte (point) of waveform information.

To display the stored data points, the System $\mu \mathrm{P}$ loads the starting address of the data block to be displayed into the Display Counter and selects the Display Counter to address the Vertical Display RAM (via the Address Multiplexer). The System $\mu \mathrm{P}$ also sets the $\overline{\mathrm{YON}}$ (vertical display on) bit applied to U421A and U421B LO, selecting the Vertical Display RAM and enabling its outputs. As the Display Counter increments, the selected block of data is sequentially clocked out onto the DY bus (vertical-display data bus) and applied to Vertical DAC U142 to produce the vertical deflection signal current to the Vertical Output Amplifiers.

If the Waveform $\mu \mathrm{P}$ needs to read data from the Vertical Display RAM, it outputs an address within 8 K to 10 K address space of the RAM. This address block is decoded by U323B to enable both the Vertical Display RAM (via U421A) and bus transceiver U322. Since the Waveform $\mu \mathrm{P}$ is trying to read data, its WRD (waveform processor read) line will be set LO. This enables the RAM outputs via U323C and U421B and causes buffer U322 to direct the data onto the Waveform $\mu \mathrm{P}$ data bus.

## Horizontal Display RAM

Operation of Horizontal Display RAM U440 is identical to that of the Vertical Display RAM just described. The Horizontal RAM chip select ( $\overline{C S X}$ ) is gated through U323D for addresses between 10 K and 12 K when DISP is LO.

Data that may be stored in the Horizontal Display RAM includes two 512 -point waveforms and $1 \mathrm{~K} \times 8$ of readout information. During a waveform display, the data output from the Horizontal RAM may be routed to either the Vertical DAC or Horizontal DAC, providing for either two more YT displays or two XY displays.

## Attributes RAM

Attributes RAM U430 contains $4 \mathrm{~K} \times 1$ points of data that tell the Z-Axis system (using the BRIGHTZ signal) whether or not a data point read from either the Vertical Display RAM or the Horizontal Display RAM should be intensified. Operation of the RAM is similar to that just described for the Vertical and Horizontal RAMs except that the data path is only one bit wide.

The write enable of the Attribute RAM ( $\overline{\mathrm{WRA}}$ ) is gated by U422C between 12 K and 14 K when DATT is LO from decoder U570 (diagram 17). WRA going LO enables the data from bit WD7 of the data bus to be written to the addressed location. Gate U422A prevents the $\overline{W W R}$ clock from being gated to U422C if the Display Counter is selected (Waveform $\mu \mathrm{P}$ not in control of the address bus).

To read attribute data out of the RAM, the Waveform $\mu \mathrm{P}$ sets WRD LO. This LO, along with the addressdecoded DATT (attribute data) line, enables buffer U423A and places the addressed output bit from the DO output of U430 onto bit WD7 of the data bus.

When displaying data from either (or both) the Vertical RAM or Horizontal RAM (the addresses applied to all three RAM chips are the same), the attribute data for each data point will be applied to the Z-Axis circuit to determine the intensity of each point. A HI bit from the DO output of U430 will intensify the displayed point.

## Horizontal Data Buffers

The Horizontal Data Buffers, U320 and U321, are used to route the data from the Horizontal RAM to either the Horizontal DAC or the Vertical DAC, depending on the type of display being produced.

For normal waveform displays, vertical deflection data may come from either the Vertical or the Horizontal Display RAM. To route data from the Horizontal RAM to the Vertical DAC, the outputs of the Vertical RAM will be disabled ( $\overline{\mathrm{OEY}}$ ), the outputs of the Horizontal RAM will be enabled ( $\overline{O E X}$ goes LO), and buffer U320 will be enabled (XTOVERT goes LO). These three signals are all controlled by the System $\mu \mathrm{P}$ by writing bits XON and XTOVERT HI into Mode Control Register U541 (diagram 17)
and writing a LO to the YON output of the register. Now, data addressed in the Horizontal RAM is applied to the Vertical DAC to produce vertical waveform deflections.

For XY displays, Mode-Control bits XON, YON, and XY are set HI while XTOVERT is set LO. This applies addressed data from the Vertical RAM to the Vertical DAC and applies the addressed data from the Horizontal RAM to the Horizontal DAC via now-enabled buffer U321. A waveform versus waveform (XY) display results.

During readout displays, both U320 and U321 will be disabled, along with the Vertical RAM. Since the readout character-code data is stored in the Horizontal RAM, it will be enabled. Character-code data from the Horizontal RAM is output to the Readout State Machine, where it is converted to the appropriate horizontal- and vertical-deflection codes.

## Readout Buffers

Readout buffers U240 and U140 direct the ten least significant bits (LSB) from the Display Counter to the Horizontal DAC and the Vertical DAC during readout displays, The buffers are enabled by a LO $\overline{\mathrm{RO}}$ signal at their enable inputs.

Four of these bits, Q6-Q9, are applied to the four most significant bits (MSB) of the Vertical DAC input through U140A and are used to select one of the 16 available readout lines for the selected character to be displayed on.

The six LSBs are applied to the six MSBs of the Horizontal DAC and are used to select one of the 64 possible character positions on the selected readout line. Since a maximum of only 40 characters will actually be displayed on any given line, the gain of the Horizontal Output Amplifier increases when readout is being displayed. The center 40 character positions then fill the display horizontally. This action is more fully explained in the Horizontal Output Amplifier description.

## Ramp Buffers

Ramp Buffers U130 and U140 apply the ten LSBs of the Display Counter address (via Address Multiplexer U210, U212, and U221 on diagram 17) to the Horizontal DAC during YT waveform (non-XY) displays. Since the Display Counter address is merely incrementing for waveform displays, a horizontal ramp results at the Horizontal DAC outputs. Each sequentially acquired data point is thus displayed at its corresponding horizontal (timedependent) address on the crt. The buffers are enabled by the COUNTEN (counter enable) bit from the Mode-Control Register.

## Volts Cursor Register

Volts Cursor Register U241 is an address-decoded memory location where the System $\mu \mathrm{P}$ writes the eight MSBs of the vertical-position data for volts-cursor displays. Data written into this register, along with two bits written into the Misc Register U540, define the vertical position of the Volts cursor. Since volts-cursor displays have two cursors, the microprocessor alternately writes the position data for each cursor into the registers just before it is displayed. Data is written into the register on the rising edge of the address-decoded VCURS clock pulse.

Volts-cursor displays are a special type of "waveform" display wherein the vertical deflection data from the Vertical Display RAM is disabled (by turning off the RAM chip select), and the data bits in Volts Cursor Register U241 (and the DYO-DY1 bits from the Misc Register U540, diagram 17) are applied to Vertical DAC U142 instead. Cursor display is automatically selected by the Z-Axis logic when neither WFM nor $\overline{\mathrm{RO}}$ are asserted (not a waveform display and not a readout display). To start the display, the System $\mu \mathrm{P}$ asserts the START bit in the Display Control Register as it would for a waveform display, starting the Display State Machine. The result is a horizontal line displayed on the screen at the level set by the data from the Volts Cursor Register. When displaying cursors on a waveform, the two LSBs from the Misc Register are set to 0 , decreasing the resolution from 1024 levels to 256 levels.

## Time Cursor Register

Time Cursor Register U441 provides a function similar to the Volts Cursor Register. Time-cursor data is written to the register from the system processor on the rising edge of the address-decoded TCURS clock (time-cursor clock). This data is applied to Horizontal DAC U250 (along with the DX0-DX1 bits from the Misc Register) to define the horizontal position of the cursor. A software ramp previously written into Vertical RAM U431 is applied to Vertical DAC U142 as the Display State Machine runs (started in the same way as the volts-cursor display).

For "directed-beam" cursors, such as the " + " made up of individual microprocessor-directed points displayed on screen, both cursor registers are enabled after the System $\mu \mathrm{P}$ writes one dot of XY position data into the registers. To display the addressed point, the processor sets the HZON (host z-axis on) bit in the Misc Register LO, then HI. The processor then calculates the next point of the " + ", writes the position data to the cursor registers, enables the registers, and sets $\overline{H Z O N}$ LO to display that point. This cycle continues until the entire " + " is drawn.

## Theory of Operation-2440 Service

## Vertical DAC

Vertical DAC U142 generates complementary verticaldeflection currents used to drive the vertical deflection system from the digital data applied to its inputs. The data that appears at the DAC inputs is selected by the microprocessor via the Mode-Control Register and determines what type of display will be generated. The exclusive-OR gate U350A inverts bit DY9 during "nonreadout'" displays to create "bipolar" data relative to the vertical (graticule) center of the crt.

## Horizontal DAC

Operation of Horizontal DAC U250 is identical to that of the Vertical DAC and produces the horizontal-deflection signal currents that drive the Horizontal Output Amplifier.

## Diagnostic Buffers

The Diagnostic Buffers, U141 (vertical) and U243 (horizontal), allow the System $\mu \mathrm{P}$ to monitor the data being applied to the Vertical DAC and Horizontal DAC respectively. By forcing known data patterns through the various data paths and observing the data arriving at the DAC inputs, the diagnostic routines can verify functionality of much of the display system hardware. The buffers are enabled during diagnostics via the address-decoded Register Select logic.

## DISPLAY CONTROL

The Display Control System (diagram 17) produces the crt waveform and readout displays from data stored in the Display RAM. The data, originally stored by the Waveform $\mu \mathrm{P}$ or the System $\mu \mathrm{P}$, is read out of the RAM and is used to produce the individual dots that make up both waveform and readout displays. The Display System has two "state machines" for converting the stored data into the horizontal and vertical deflections that produce the waveform dots and readout characters.

For YT waveform displays, the Display State Machine generates 512 linearly spaced points across the face of the crt (horizontally). Each of these points may be displayed at any of 256 vertical positions on the crt. For XY displays, each of the 512 points that make up a waveform may be placed anywhere on the screen in a 256 $\times 256$ matrix.

For readout displays, the face of the crt is vertically divided into 16 character lines each having 40 horizontal character positions on the line. Each of these character positions corresponds to a specific location in the readout
memory space (stored in the Horizontal RAM). To display the readout, the Readout State Machine sequentially reads through the readout memory and displays the required character at the corresponding (memory-mapped) location on the crt screen. Each displayed character consists of a sequence of individual dots produced by the Readout State Machine.

Each of these display types is controlled and initiated by the System $\mu \mathrm{P}$. The acquired waveform data points are written into the Display RAMs by the Waveform $\mu \mathrm{P}$ and the readout data is written in by the System $\mu \mathrm{P}$. Display of this stored data is controlled by the System $\mu \mathrm{P}$ through data latched into the several display registers. The data written to the registers determines what type of display should be produced, how long (number of data points) it should be, and when it should start.

## Register Select

The Register Select stage, composed of U550 and U450D (along with the System $\mu \mathrm{P}$ address decoding), address decodes the three LSBs of the System $\mu \mathrm{P}$ address bus to enable any of eight display "registers" for a read or write. These registers control such things as display mode (how the stored data is displayed, either XY or YT), which waveforms are displayed, and whether or not cursors and readout are to be displayed.

The enable inputs for $\mathbf{U 5 5 0}$ are controlled by the System $\mu \mathrm{P}$. The DISPSEL (display select) is an addressdecoded signal produced on the Processor board when any of the display memory addresses are output by the System $\mu \mathrm{P}$. Negative OR gate U450D provides an enable to U550 whenever the System $\mu \mathrm{P}$ is trying to read or write. Address bit A3 provides the final enable when it is HI .

Once enabled, the three lowest address bits are used to select one of the eight outputs from U550. These outputs, when LO, enable or load one of the eight display registers. Enabling of these individual registers is explained in more detail in the specific register descriptions.

## Mode Control Register

Mode Control Register U541 and associated gating circuits composed of U340, U442, U423B, and U350C, control the operating modes of the various display state machines.

Data from the processor data bus is written into data latch U541 when the MODECON (mode control) bit from U550 returns HI (after the PWRUP reset goes HI). These
latched bits are used as enables to other portions of the display circuitry and control the overall function of the display.

NAND gates U340C and U340D do not allow the $\overline{\text { YON }}$ and $\overline{\mathrm{XON}}$ enables (controlling the vertical and horizontal RAMs respectively) unless the display counter is running (PRESTART + DISPLAY is HI). Exclusive-OR gate U350C and tristate buffer U423B are used to enable horizontaldeflection bit DX1 only when the time cursor is being displayed (both RO and COUNTEN are LO). The remaining bits from the mode-control register are NANDed with the $\overline{\mathrm{DISP}}$ (display running) signal and only affect their associated functions while the Display State Machine is running.

Buffer U542 provides a way for the System $\mu \mathrm{P}$ to read back the data written to the Mode Control Register U541.

## Display Control Register

The operation of Display Control Register U530 is similar to that just described for the Mode Control Register. When enabled (by $\overline{\text { DISCON }}$ ), data from the data bus is written into U530 on the rising edge of the System $\mu \mathrm{P} \overline{\mathrm{WR}}$ (write) clock. These data bits determine how many data points are displayed, whether the display is to be read from memory in envelope mode (ENV), and whether the intensity of each dot should be bright or dim (DOTS).

The buffer U531 provides a way for the System $\mu \mathrm{P}$ to read back the contents of the Display Control Register.

## Miscellaneous Register

Operation of the Miscellaneous Register is identical to that of the Display Control Register just described. The output bits control miscellaneous circuit functions, as the register name implies. The function of each bit is explained in the description of the associated circuitry.

Buffer U540 allows the System $\mu \mathrm{P}$ to read back the contents of the Miscellaneous Register.

## Display Clocks

The state machines of the Display System run on clocks derived from the 5 MHz clock of the Secondary Clock Generator U710 (diagram 7). The Display Clocks circuit provides the signal frequency division and gating logic to properly condition clocks for the Display System circuitry.

The 5 MHz clock signal from the Time Base Controller circuit is buffered and inverted by U413C and is used to drive the Readout State Machine.

The 5 MHz clock is also applied to the counter made up of decade counters U410A and U410B, producing several intermediate clocks at their outputs. The 1 MHz 2QC clock, the 500 kHz 2QA clock, and the 250 kHz clock from U410B are gated together by U411A and produce the SAMPLE clock, having a LO duty cycle of $12.5 \%$.

Buffer U413A inverts the 250 kHz clock used for the ZAxis and Display State Machines.

Gates U411C, U412C, and U412D make up a clocksteering circuit that selects the source for clocks to the counters, depending on display mode. When displaying waveforms, readout, or cursors, the DISPLAY bit applied to U411C is HI. The RO and RO signals, applied to U412C and U412D respectively, do clock selection depending on whether readout or waveform data is to be displayed.

For waveform displays, RO applied to U412C is LO, holding its output to U411C HI. This HI, along with the HI DISPLAY bit, enables U411C, and the output of U411C follows the 250 kHz signal applied to U412D (since $\overline{\mathrm{RO}}$ is HI ). For readout displays, RO and $\overline{\mathrm{RO}}$ are HI and LO respectively. This holds the output of U412D HI, and the output of U411C follows the CLKRAM (clock RAM) signal from the Readout State Machine. To completely disable the Counter clocks, the Display State Machine sets the DISPLAY bit applied to U411C LO.

## Display Counter

The Display Counter stage, made up of U211, U220, and U222, generates the sequential addressing that the Display and Readout State Machines use to read the stored waveform and character data out of the display RAM. Depending on the type of information to be read from RAM (waveform or readout), clocks to the counter are selected by logic to produce waveform and readout displays at the proper refresh rates.

To display stored data, the System $\mu \mathbf{P}$ writes the eight MSBs of the 12-bit starting RAM address into U211 and U220 over the data bus by generating a LO LDCOUNT from the Register Select stage. The 4 LSBs of the address (all LO) are also loaded at the same time into U222. The counter then starts counting at the selected rate. When the count in U222 reaches 15, its $\overline{\text { RCO }}$ (ripple-carry output) goes LO for the last half of the clock cycle and
enables U220. Due to a two-gate propagation delay through U222 to the $\overline{\operatorname{RCO}}$ output, U220 will still be enabled on the rising edge of the next clock. This clocks U220, which is then disabled until U222 counts another 16 clocks. Counting continues, and eventually the $\overline{\mathrm{RCO}}$ output of UZ20 enables U211, causing it to increment in a similar fashion. Counting continues until the Display State Machine determines that the desired display is complete, at which time it shuts off clocks to the counter.

The outputs of the counters change synchronously and are applied to the Multiplexer stage, which selects between these counter outputs and the microprocessor address bus for Display RAM addresses. The MAX output from U222 (occurring on count 15) is used in the Readout State Machine.

## Address Multiplexer

The Address Multiplexer stage, under control of the Display State Machine, selects the address source for the various display RAMs from either the Waveform $\mu \mathrm{P}$ address bus or the Display Counter.

When the Waveform $\mu \mathrm{P}$ is writing acquired data into the display RAMs (Horizontal or Vertical), the Display State Machine selects the Waveform $\mu \mathrm{P}$ address bus (WAO-WAB) as the source for RAM addresses by setting the COUNTSEL (counter select) line LO. When displaying the stored data, COUNTSEL is HI , and the outputs from the Display Counter are routed to the various RAM address lines.

Exclusive-OR gate U350B is used to invert counter bit DCO when displaying envelope data (ENV is HI ). This causes data pairs (max-min) to be read out in reverse (relative to how they were stored) and produces an envelope display that always starts with a MIN point.

## Display State Machine

The Display State Machine determines when display of stored data should start and stop, depending on other conditions in the Display System.

To start a display, the System $\mu \mathrm{P}$ writes a HI for the START bit into Display Control Register U530. This HI is applied to the D input of flip-flop U415A and clocked to its Q output on the falling edge of the 250 kHz clock (rising edge of the $\overline{250 \mathrm{kHz}}$ clock). This latched STARTDIS bit (HI) is then applied to the D input of U414A and to pin 9 of U313. Since the Display Counter has not reached its final value (this is the starting point), the output level of the
three lower AND gates within U313 are LO, thereby enabling the output AND gate (it has inverting inputs). With the previous display cycle finished (as it is for this discussion), the DISDN (display done) bit applied to pin 10 of U313 is also HI. The 250 kHz clock applied to this enabled AND gate causes the output of U313 to go HI on the falling edge to clock the HI STARTDIS bit to the Q output of U414A. This latched signal is the DISPLAY bit that enables the Display Counter clocks (via U411C).

The DISPLAY bit is delayed slightly by the propagation delays of the START bit through the flip-flops and gates. Therefore, the PRESTART bit is written HI to cause the output of U323A to be HI until the DISPLAY bit is latched into flip-flop U414A. The HI PRESTART + DISPLAY bit from U323A selects the counter outputs to address the Display RAMs (via the Address Multiplexer stage). After the DISPLAY bit is latched into U414A, the System $\mu \mathrm{P}$ sets the START and PRESTART bits from the Display Control Register LO. The LO START bit is clocked to the Q output of U415A, disabling the 250 kHz clocks through U313 to U414A, and the LO PRESTART bit allows the DISPLAY signal to control OR-gate U323A.

With the DISPLAY bit to U411C set HI, clocks from either U412C or U412D clock the Display Counter. Which one does the clocking depends on whether the data to be displayed is readout or waveform information. If readout information is being displayed, the $\overline{\mathrm{RO}}$ bit (from the Mode Control Register) applied to U412D will be LO, disabling the 250 kHz clock (output of U412D is held HI). At the same time, R/O applied to U412C is HI, enabling the CLKRAM (clock RAM) signal from the Readout State Machine to clock the address counters.

If waveform data is to be displayed, $\overline{\mathrm{RO}}$ from the Mode Control Register is HI and RO is LO. The LO RO level applied to U412C closes the CLKRAM path (output of U412C is held HI ) while the $\mathrm{HI} \overline{\mathrm{RO}}$ level applied to U412D opens the 250 kHz clock path through U412D and U411C.

The two display-control bits, STOP512 and STOP1024, applied to U313 determine how many data bytes are read from the selected display RAM (Horizontal, Vertical, and Attribute) before stopping the current display cycle. Only one of these two bits is HI at any time. The outputs of the unselected AND gates within U313 are LO, and along with the LO caused by the LO STARTDIS bit, enable the output gate of U313. The selected AND gate watches its appropriate counter bit and, on the falling edge of the bit, causes a clock at the output of U313. This clocks the now LO STARTDIS bit to the $Q$ output of U414A, disabling U411C (and thus clocks to the Display Counter), and resets the DISDN at the $\bar{Q}$ output HI in preparation for the next display cycle.

The DISDN signal is also sent to the System $\mu \mathbf{P}$ Interrupt Logic to tell it when the currently assigned display task is complete. When the processor detects the HI DISDN, it writes data out to the display register to start the next display cycle. The System $\mu \mathrm{P}$, knowing how much waveform and readout data needs to be displayed, does the writing at a rate that keeps the overall display-refresh rate constant.

Displaying a single waveform requires 512 data points be read from RAM, so STOP512 is set HI. A twowaveform display or a single-waveform envelope display will require STOP1024 to be HI. Readout displays may also consist of up to 16 lines of readout, in which case STOP1024 would be set. This is further explained in the Readout State Machine description.

The STOPDIS bit applied to the reset inputs of U414A and U415A provides the System $\mu \mathrm{P}$ with a way to stop any display in process.

## Z-Axis Logic

The Z-Axis Logic determines when to turn the display beam on or off for each of the various display modes. These displays are readout, waveform, cursor-normal, cursor-dashed, and diagnostic (host-forced) Z-Axis on.

> To enable readout or waveform displays, the Display State Machine sets its DISPLAY output HI. This enables U415B, U414B, and U312C.

During readout displays, the $\overline{\mathrm{RZON}}$ (readout Z-Axis on) signal from the Readout State Machine is LO for each point that should be turned on and HI when the display should be blanked. The level of this signal is sampled by U 415 B at a 5 MHz rate. The Q output of U415B controls the Z-Axis through U450B and U223C, and since it is synchronized to the 5 MHz clock used to clock the Readout State Machine, the intensity of each dot is not the same.

For waveform displays, the DOTS bit from Display Control Register U530 will be set HI by the System $\mu \mathrm{P}$. This HI, along with the HI DISPLAY signal from the Display State Machine, enables U312C. As long as a waveform display is taking place, the 250 kHz clock turns the display dots on and off with a $50 \%$ duty cycle via U312C and U223C. When the Display State Machine determines that the waveform display is over, it sets its DISPLAY bit LO, disabling U312C. For nonwaveform displays, the DOTS bit is LO, also disabling U312C.

For cursor displays, the HI DISPLAY signal enables D flip-flop U414B, and the $\overline{250 \mathrm{kHz}}$ clock begins clocking the data from the output of U312B to the Q output of U414B. Since a cursor display is neither a waveform nor a readout display, the DOTS signal applied to inverter U413D is LO while the $\overline{\mathrm{RO}}$ signal applied to NAND-gate U312B is HI . This enables U312B, and the output of U412A then controls the D input signal to flip-flop U414B. That signal is clocked to the Q output and applied to U223C to control the Z-Axis signal $\overline{Z O N}$.

When displaying the inactive cursor (the one not selected for control by the cursor pot), the ACTIVELC (active line cursor) bit from the Misc Register to pin 2 of U412A is set LO. This causes the output of U412A to be HI, and the Z-Axis remains on as long as that particular cursor is being displayed.

When the other (active) cursor is to be displayed, the System $\mu \mathrm{P}$ sets the ACTIVELC bit HI. The output of U412A is then dependent on the DC3 signal from the Display Counter. The DC3 signal has a $50 \%$ duty cycle and changes states every eight characters (for cursors, the character is a single dot), so the resultant cursor display appears as a dashed line.

The $\overline{\mathrm{HZON}}$ (host Z-Axis on) bit applied to U450B from the Misc Register (U540) allows the System $\mu \mathrm{P}$ to turn the Z-Axis on during diagnostics and allows verification of Z Axis functionality. When set LO, $\overline{H Z O N}$ produces a LO at the output of U450B output, and thus at the $\overline{Z O N}$ (Z-Axis on) output of U223C. This keeps the Z-Axis turned on until the $\overline{H Z O N}$ bit is reset HI by the processor.

## Readout State Machine

The Readout State Machine produces the alphanumeric readout on the crt from character-code data stored in the Horizontal RAM. For readout displays, the face of the crt is vertically divided into 16 character lines each having 40 horizontal character positions on the line. Each of these character positions corresponds to a specific location in the readout memory space (stored in the Horizontal RAM). To display the readout, the Readout State Machine sequentially reads through the readout memory and displays the required character at the corresponding (memory-mapped) location on the crt screen. Each displayed character consists of a sequence of individual dots produced by the Readout State Machine.

Since the position of the character on the screen is related directly to the RAM location, the LSBs of the Display Counter are used to position the character on the crt screen. The six LSBs of the counter are applied to the Horizontal DAC and select 1-of-64 character locations on
a line (only the center 40 are displayed) and the next four LSBs are applied to the Vertical DAC to select 1-0f-16 display lines.

Once this rough positioning is done, the Readout State Machine displays a sequence of dots that make up the addressed character, each dot being positioned relative to the rough display position.

Character codes, sequentially read from the Horizontal RAM, are applied to seven address lines of a character ROM (U420). These select the block of dot-position data within the ROM corresponding to that character code. Five more address bits are generated by an incrementing Dot Counter (U416B and U416A) and sequentially clock the XY dot-position data from the selected ROM block. The horizontal and vertical dot-position data is applied to the Horizontal and Vertical DACs and is used to deflect the crt beam relative to the selected on-screen character position.

The operation of the Readout State Machine is ROM based; it proceeds through a sequence of states based on data loaded from a ROM.

Initially, when power is first applied, both the PWRUP (power up) and DISPLAY signals applied to U450A are LO. These states cause a LO at the reset input of presettable counter U231 that resets its output count to zero. The reset state will remain until the instrument power comes up (PWRUP goes HI) and the system processor determines that a display should be produced (it starts the Display State Machine and DISPLAY goes HI).

With the reset removed, presettable counter U231 is enabled to either count (up) or do a parallel load from the four MSBs output from the addressed location within U232 on the next rising edge of the 5 MHz clock. The COUNT/[OAD select line from the data selector U230 determines whether counting or loading will occur.

The LOAD/DECIDE bit output from the addressed ROM location within U232 is applied to the enable input of U230 and determines whether the COUNT/LOAD line is forced LO (U230 disabled by LOAD/DECIDE being HI) or whether one of the decision inputs is selected (via select inputs $A$, $B$ and $C$ of U230). When the LOAD/DECIDE bit from U232 is LO, it indicates that the state machine is at a decision point as to whether counter U231 should count or load (instead of just automatically loading the next state). The condition tested to make this decision is selected by the select inputs to U230 and are as follows:

[^6]D2-AND gate U233A watches for the 12th character address (11).

D3- $\overline{E O C H}$ (end of character) goes LO on the last character dot and causes the next state to be loaded.

D4-EOL (end of line-X9 bit U440, diagram 16) goes $H I$ when readout line is over.

D5-AND gate U223B watches for the 64th character address (63) to indicate that the next character is the beginning of a new line.

ROM U330, addressed in parallel with U232, outputs three bits unique to the state selected and is used to clock the dot counter (U416B and U416A), clock the Display Counter, and to turn on the Z-Axis for readout dots.

The flow chart in Figure 3-8 illustrates oderation of the Readout State Machine.

As the state machine runs, the counter outputs of U231 (the "current-state") are first reset to state " 0 ." The data output from the 04-O7 (outputs 4-7) lines of U232 contain the "next-state" data, 01-03 (outputs 1-3) hold the select data for the data selector U230, and output 00 (output 0 ) is the LOAD/DECIDE bit. In addition, the outputs from U330, used to turn on the Z-Axis if appropriate ( $\overline{R Z O N}$ ), increment the character ROM dot counter U416B-U416A (CKDOTCTC), and clock the Display Counter (CLKRAM) to address the next character, are now at their state 0 condition (all HI ).

The COUNT/LOAD signal from U232 determines what action counter U231 takes when the next 5 MHz clock occurs. If LO, the data from outputs O4-O7 of U232 is loaded to the counter outputs; if HI , the counter increments.

The LOAD/DECIDE line, along with the three channelselect inputs to U230, gives the state machine the ability to determine when certain events have occurred. When the LOAD/DECIDE bit from ROM U232 is HI, indicating that no decisions need be made in the present state, data selector U230 is disabled and the COUNT/LOAD output to U231 are forced LO. On the next 5 MHz clock, the "nextstate' data from U232 (outputs O4-07) is merely loaded into counter U231.

If the "present-state" data output from U232 has the LOAD/DECIDE bit set LO, indicating that some circuit condition needs to be tested to determine what to do next,


Figure 3-8. Readout State Machine flow chart.

## Theory of Operation-2440 Service

data selector U 230 is enabled. The three data bits $(01$ through 03) from U232 define which condition needs to be tested and selects one of the D inputs of U230 to route to U231 via the COUNT/LOAD line. Whether or not the condition being tested for is present at the selected $D$ input determines whether counter U231 counts or loads.

To go from state " 0 " to state " 1 ," data from U 232 is loaded into U231.

The state 1 data from U232 has the LOAD/DECIDE signal set LO, and the next three bits select input D0 of U230 to watch. This is the R/O (readout) line, and it is set HI by the System $\mu \mathrm{P}$ when it wants to start a readout display. If R/O is LO (don't start yet), COUNT/ $\overline{\text { LOAD }}$ is also LO and the "next-state" data from U232 is loaded into counter U231. For state 1 , the next-state data is also 1 , so the state machine just cycles in state 1 until R/O goes HI.

When R/O goes HI, the COUNT/LOAD line follows and the next 5 MHz clock increments the counter to state " 2 ." State 2 has the LOAD/DECIDE bit set HI, so the next clock merely loads the next-state data (which happens to be 3) into U231.

State " 3 " clocks the display RAM (using CLKRAM from U330), enables U230, and selects its D2 input. AND gate U223A, producing the D2 input level, monitors the Display Counter address lines, looking for address 11. Address 11 corresponds to the twelfth character (remember character 0 ) and the first character displayed on the crt. (See Display Output description for further explanation.) If address 11 has not been encountered yet, the next-state data from U232 will be loaded into U231.

This next-state data is 2. Returning to state 2 resets the CLKRAM bit from U330 HI so the next state 3 will clock the Display Counter again. This loop between states 2 and 3 continues to clock the Display Counter until U223A detects address 11. When this occurs, COUNT/LOAD goes HI and the next $\overline{5 \mathrm{MHz}}$ clock increments the state to " 4 ."

State " 4 " resets CLKRAM HI and disables U230. The next clock loads state " 5 ," a 200 ns delay, into U231. The next clock loads state "6."

State " 6 " data from U232 enables U230 and selects its D3 input. This is the EOCH (end of character) bit from the character ROM U420 and will only be LO for the last dot of any given character. As long as $\overline{\mathrm{EOCH}}$ is HI (not the last dot), U231 will increment to state ' 7 " on the next
clock. State 7 disables U230, terminating the test condition.

State " 8 " is loaded from state 7 and turns on the $Z$ Axis via $\overline{R Z O N}$ (readout Z-Axis on) from U330. States " 9 " and " $A$ " (hex) are sequentially loaded from the previous state and also have RZON asserted. These three cycles in sequence turn the Z-Axis on for 600 ns for each readout dot to be displayed.

State " $B$ " is loaded from state " $A$ " and does two things. It turns $\overline{\text { RZON off }}(\mathrm{HI})$ and sets CKDOTCTC (clock dot counter) LO, incrementing the dot counter made up of U416B and U416A. This addresses the next byte of XY deflection data within U420 in preparation for the next dot display cycle.

The next $\overline{5 \mathrm{MHz}}$ clock loads state 5 from state B and resets the CKDOTCTC from U330 HI. State 6 is next loaded from state 5 and is once again checking for $\overline{\mathrm{EOCH}}$ (described earlier).

If $\overline{E O C H}$ is set LO this time (signaling the last dot), counter U231 will be loaded to state "D" (instead of clocked to state 7 as described earlier). State D clocks the Display Counter via CLKRAM, enables U230 and selects its D4 input. This input monitors the EOL signal (X9 bit) from the Horizontal RAM which will be set HI when the last character of a given line of readout information has been displayed. When EOL (end of line) is detected, U231 increments to state "E.' If it is not detected, state 4 will be reloaded from state $D$ data and the next character will be displayed as described before.

State "E" resets the CLKRAM signal from U330 and disables U230. The next $\overline{5 \mathrm{MHz}}$ clock loads state " $F$ " from state E data.

State " $F$ " data clocks the Display Counter via CLKRAM, enables U230 and selects its D5 input. AND gate U223B watches for Display Counter address 63; i.e., the 64th character. If the 64th character is not detected, state $E$ is loaded from the state $F$ data, resetting CLKRAM HI in preparation for the next state F and the associated CLKRAM pulse. The looping between states E and F continues to increment the Display Counter until U223B detects address 63 (the 64th character).

The 64th character is significant in that the next character is the start of the next line. When address 63 is detected, U231 is clocked from state F to state 0 . The routine is now back to where it started, and the next line may be displayed in a similar manner.

## DISPLAY OUTPUT

The Display Output circuits (diagram 18) convert the current outputs from the Horizontal and Vertical digital-toanalog converters (DACs) to the voltage levels used to drive the crt deflection plates. The Display Output circuit includes a vector-generation function that allows the individual dots of a waveform display to be translated into smooth lines connecting the waveform points (vectors on) A Display Mode switching circuit under control of the System $\mu \mathrm{P}$ selects which type of signal is applied to the output amplifiers for the various display types (envelope, dots, vectors, or readout).

## Vertical and Horizontal Input Buffers

Operation of the Vertical and Horizontal Input Buffers is identical; so for brevity, only the Vertical Input Buffer circuit operation is described.

The Vertical Input Buffer, JFET operational amplifier U170 and its associated components, translates the complementary output currents from the Vertical DAC (U142, diagram 16) to an output voltage. Complementary, in this case, means that the sum of the currents is a fixed value; if one current increases, the other decreases by the same amount.

Current from the Vertical DAC output connected to pin 3 of U170 develops a voltage across R163. This voltage causes the output of U170 to move in the same direction until the feedback current through R164 applies an equal voltage to pin 2 of U170. The output voltage of the Input Buffer at pin 6 is the (signed) sum of voltages across R163 $(+)$ and R164 ( - ). The gain of the stage is 1 V per mA (differential).

## Vertical and Horizontal Vector Generators

Operation of the Vertical and Horizontal Vector Generators is similar. For brevity, only the Vertical Vector Generator is described in detail, and the differences in the two Vector Generators pointed out. Each Vector Generator consists of a High-Current Difference Amplifier, a Sample-and-Hold circuit, and an Integrator circuit that transforms the step voltages output from the Sample-and-Hold circuit to smooth transitions (vectors). See Figure 3-9 for a simplified diagram.

The step transitions from Vertical Input Buffer U170 are applied to the High-Current Difference Amplifier, made up of U281, Q182, Q181, and associated components, through R172. Initially (before the first integration occurs), input pin 3 of U281 is referenced to ground through R161; deviation from this ground reference seen at the other


Figure 3-9. Vertical Vector Generator.
input (pin 2) causes the output (pin 6) of U281 to move in the opposite direction. This voltage change is applied to the base of Q181 (via R145) and to the base of Q182 (via series diodes CR193 and CR194 from R145). These transistors are biased in their linear region and act as emitter followers for the signals at their bases. Two series diodes between the bases of the transistors separate the base voltages by 1.2 volts, so the emitters of both transistors are at about the same potential. Negative feedback from the amplifier output (junction of R194-R196) is via R280. The resistance ratio of R280 to R172 sets the voltage gain of the amplifier at -1 . Capacitor C281, from the output of U281 back to the input at R172, provides a fast feedback path to smooth transition spikes.

Sample Switch U270B, Hold Capacitor C260, and Voltage Follower U280 form a sample-and-hold circuit. The output of the High-Current Difference Amplifier at the junction of R194 and R196 is allowed enough time to settle to its new level before the 250 kHz SAMPLE pulse goes LO. At that time, the output of the Difference Amplifier is applied to the input of Voltage Follower U280A, and C260 is charged rapidly to that output voltage level. The SAMPLE pulse returns HI, and the BX output of the data selector goes to its high-impedance state to start the hold time. Voltage Follower U280 has high-impedance FET inputs; therefore, Hold Capacitor C260 discharges very little during the hold time.

The output of Voltage Follower U280 is held at the voltage level across C260; that level causes some value of current to flow through the series combination of R620 and R162 to the input of Integrator U282 (pin 2, the inverting input). The output of Integrator U282 at pin 6 ramps linearly for the duration of the hold cycle. (Actually, it ramps for almost the whole cycle, since the charge on Hold Capacitor C260 reaches the final level slightly before the sample switch is opened to start the hold time.) The time constants of the integrating network composed of R162 and of the series combination of R601 and C180 in parallel with R603 and C470 are such that the output of Integrator U282 reaches the new point position just as the next SAMPLE gate to U270B occurs. (A step change of 1 volt at the input causes a ramp of $-1 / 4 \mathrm{~V}$ per $\mu \mathrm{S}$ (or -1 volt over the $4 \mu$ s cycle hold time.)

The feedback of this "new" point position to U281 through R160 modifies the reference at pin 3 of Difference Amplifier U281 (new reference is one-half the output voltage at U282 pin 6). The next voltage from Input Buffer U170 is applied to the input (pin 2 of U281) of the Difference Amplifier which now amplifies the difference between the present point position on screen (represented by the voltage at pin 3 of U281A) and the new position
(applied to pin 2 of U281A). This difference voltage is sampled and stored on Hold Capacitor C260 where it sets a new current level through R162 and R620 from the output of Voltage Follower U280 to the input (pin 2) of Integrator U282A.

This cycle just described of comparing the old position to the new one, sampling the difference, and ramping to the new position continues for each point of a vector waveform display.

The adjustment associated with Voltage Follower U280 is INT ADJ potentiometer R620. This pot (the integrator adjustment) is used to compensate for charge current introduced from analog switch U270B. A corresponding adjustment is not present in the Horizontal Vector Generator circuit. A VECTOR COMP adjustment is present in both the Vertical and Horizontal Integrator circuits. The pots (R276 vertical and R376 horizontal) are used to adjust for minimum vertical and horizontal offset between the vector and dot displays.

## Mode Select

The Mode Select Switch consists of data selector U290A (horizontal) and U290B (vertical). The switches route the various X -Axis and Y -Axis signal sources to the Horizontal and Vertical Output Amplifiers. The select signals to U290 coming from Miscellaneous Display Register U540 (diagram 17) allow the System $\mu \mathrm{P}$ to switch to the various display modes (Envelope, vectors, dots, and readout). The System $\mu \mathrm{P}$ does this by writing control bits to the 1Q and 2Q output of Display Register U540 (AMP1 and AMPO respectively) which are applied to select input $S E L_{B}(\operatorname{pin} 9)$ of U290B and to $S E L_{A}(\operatorname{pin} 10)$ of U290A.

An envelope waveform display is produced by selecting the XO and YO inputs of U290 to be switched to the Output Amplifiers. The signal applied to the Horizontal Output Amplifier for YT displays is the incrementing count from the Display Counter, and it moves the electron beam horizontally across the face of the crt. In the Vertical circuitry, a sample-and-hold circuit formed by Data Selector U270A and Hold Capacitor C912 bypasses the Vertical Vector Generator circuitry. The 250 kHz signal driving the data selector, derived from the same Clock Divider circuit that supplies the SAMPLE signal (U410A and B, diagram 17), is delayed slightly by the rc combination of R607 and C900. The delay allows the analog signal at the output of the Vertical DAC to settle before the sample from Input Buffer Amplifier U170 is taken. The voltage on C912 is applied to the rc integrator made up of R165 and C166 to produce a min-max envelope with shaded vectors between the successive dots.

To produce a vector display of a waveform, the System Processor selects the X1 and Y1 inputs of U290. This routes the outputs from the Vertical and Horizontal Vector Generators (previously described) to the Horizontal and Vertical Output amplifiers.

For non-vector waveform displays, the X2 and Y2 inputs are routed to the outputs of U290. These signal lines, $V$ DOTS and H DOTS, come directly from the output of the Vertical and Horizontal Input Buffers (U170 and U370B), bypassing the Vertical and Horizontal Vector Generators. Since the data applied to the Horizontal DAC in YT mode is from the incrementing Display Counter, the Y-Axis vertical deflections are displayed versus a linear X-Axis ramp (horizontal time axis). If XY mode is in effect, the data applied to the Horizontal DAC is the digitized waveform data used to provide the $X$-Axis deflection signal. In either YT mode with vectors off or XY mode, a dot waveform display is seen on the CRT.

To display readout, the H READOUT and V READOUT signals at the Y 3 and X 3 inputs are switched to the outputs of U290. The resistive divider formed by R171 and R282 slightly decreases the amplitude of the signal from the Vertical DAC to ensure that all the Readout vertical data points are limited to eight vertical graticule divisions and will appear on screen. Operational amplifier U392B and its associated resistors perform the opposite function on the H READOUT signal from the Horizontal DAC, increasing the gain of that signal. This horizontal expansion causes the center 40 characters of a displayed readout line (out of a possible 64) to horizontally fill the screen. (See the Readout State Machine description for further details.)

## Horizontal and Vertical Output

Operation and circuitry of the Horizontal and Vertical Output are nearly identical. Therefore, only the Horizontal Output circuit operation is described.

The selected horizontal signal from U290A is applied to operational amplifier U392A configured with a variable gain set by R586. (The corresponding buffer in the Vertical Output has a slightly different variable gain range.) Operational amplifier U392D is an inverting amplifier having a gain of about two. Horizontal offset is adjusted with R587.

The output of U392D drives the negative horizontal-deflection plate ( $\mathrm{H}-$ ) of the CRT and operational amplifier U392C. Operational amplifier U392C is configured as an inverting buffer with unity gain, and its output drives the positive horizontal-deflection plate $(\mathrm{H}+)$.

## Spot-Wobble Correction

The Spot-Wobble Correction circuit provides a dynamic correction of spot-shift on the CRT caused by signal intensity changes (CRT electron-beam current changes). Correction is accomplished by injecting offsetting currents that vary linearly with beam-current changes into the Vertical and Horizontal Output.

The beam-current control voltage is inverted by U460A and applied to one end of R583 and R584 while the other end of both potentiometers is connected to the noninverted control signal. Each potentiometer is adjusted over this "differential" range to minimize the associated spot wobble while viewing a special calibration display provided with the Extended Calibration function.

## HIGH-VOLTAGE SUPPLY AND CRT

The High-Voltage Supply and CRT circuit (diagram 19) provides the voltage levels and control circuitry for operation of the cathode-ray tube (CRT). The circuitry consists of the HV Oscillator, the HV Regulator, the +60 V Supply (+61 V Supply for instruments with serial numbers B012402 and below), the Cathode Supply, the Anode Multiplier, the DC Restorer, Focus and Z-Axis Amplifiers, the Auto Focus buffer, the CRT, and the various CRT Control Voltage Circuitry.

## HV Oscillator

The HV Oscillator transforms power obtained from the -15 V unregulated supply into the various AC levels necessary for the operation of the CRT circuitry. The circuit consists primarily of transformer T525 and switching fransistor Q628 connected in a power oscillator configuration. Sinusoidal low-voltage oscillations set up in the primary winding of T525 are raised by transformer action to high-voltage levels in the secondary windings. These AC secondary voltages are applied to the +60 V Supply (+61 V Supply for instruments with serial numbers B012402 and below), the DC Restorer, the Cathode Supply, and the Anode Multiplier circuits that provide the necessary CRT operating potentials.

Oscillation occurs due to the positive feedback from the primary winding (pin 4 to pin 5) to the smaller base-drive winding (pin 3 to pin 6) used to provide base drive to switching transistor Q628. The frequency of oscillation is approximately 50 kHz and is determined primarily by the parallel resonance frequency of the transformer.

OSCILLATION START UP. Initially, when power is applied, the HV Regulator circuit detects that the CRT cathode voltage is too positive and pulls pin 3 of transformer T525 negative. The negative level is applied to the base of switching transistor Q628 through the transformer winding and forward biases it. Charge begins to flow in the primary winding through the transistor collector circuit and produces a magnetic field around the
transformer primary winding. The increasing magnetic field induces an in-phase voltage in the base-drive winding that further supports the base-emitter voltage bias of the transistor. This in-phase feedback causes Q628 to remain on and continue supplying energy to the parallel resonant circuit formed by the winding inductance and interwinding capacitance of the transformer. As the primary voltage peaks, then begins falling, the induced magnetic field begins to decay. This decreases the base-drive voltage through the base-connected winding and begins to turn Q628 off.

As Q628 turns off, the magnetic field around the primary winding continues to collapse, and a voltage of opposite polarity is induced in the base-drive winding. This turns the switching transistor completely off. Once again, as the magnetic field builds and then reverses, the voltage induced in the base-drive winding changes direction, forward biasing Q628. At that point, the primary winding current starts increasing again, and the switching transistor is again turned on hard by the feedback supplied to the base-drive winding. This sequence of events occurs repetitively as the circuit continues to oscillate.

The oscillating magnetic field couples power from the primary winding into the secondary windings of the transformer. The amplitudes of the voltages induced in the secondary windings are a function of the turns ratios of the transformer windings.

## HV Regulator

The HV Regulator consists of U168B and associated components. It monitors the CRT Cathode Supply voltage and varies the bias point of the switching transistor in the HV Oscillator to hold the Cathode Supply voltage at the nominal level. Since the output voltages at the other secondary winding taps are related by turns ratios to the Cathode Supply voltage, all voltages are held in regulation.

When the Cathode Supply voltage is at the proper level (-1900 V), the current through R263 and the $19 \mathrm{M} \Omega$ resistor internal to High-Voltage Module CR565 holds the voltage developed across C260. at 0 V . This is the balanced condition and sets the output of integrator U168B at a level providing correct base drive for Q628 to hold the secondary voltages at their proper levels.

If the Cathode Supply voltage level tends too positive, a slightly positive voltage will develop across C260. This voltage causes the output of integrator U168B to move negative. The negative shift charges capacitor C617 to a different level around which the induced feedback voltage at the base-drive winding will swing. The added negative bias causes Q628 to turn on earlier in the oscillation cycle, delivering more energy per cycle to the resonant transform-
er. The increased energy in the resonant circuit increases the secondary voltages until the Cathode Supply voltage returns to the balanced condition ( 0 V across C260). Opposite action occurs should the Cathode Supply voltage tend too negative.

## +60 Volt Supply ( +61 V Supply for instruments with serial numbers B012402 and below)

The +60 Volt Supply ( +61 V Supply for instruments with serial numbers B012402 and below) circuit provides power to several other circuits on the High-Voltage board. Diode CR411 provides half-wave rectification of the first-tap voltage from the secondary of T525 and stores that charge on C216 and C218 (C317 for instruments with serial numbers B012402 and below). Transistor Q215 (and zener diode VR210 for instruments with serlal numbers B012402 and below) and the associated components form a series pass regulator (buffered zener regulator for instruments with serial numbers B012402 and below). Diode CR315 protects the base-emitter junction of Q215 should a failure reverse-blas the junction. For instruments with serial numbers B012403 and above, transistors Q216 and Q217 along with divider R218 and R219, and other associated components form an error amplifier to control the series pass regulator, For instruments with serial numbers B012402 and below, Q216 and Q217 along with divider R218 and R219 and other associated components form an error amplifier to control the series pass regulator.

## Cathode Supply

The Cathode Supply circuit is composed of a volt-age-doubler and an RC filter network contained within High-Voltage Module CR565. This supply produces the -1900 V accelerating potential to the CRT cathode and the -900 V slot lens voltage. The -1900 V supply is monitored by the HV Regulator to maintain the regulation of all voltages from the HV Oscillator,

The alternating voltage from pin 10 of transformer T525 ( 950 V peak) is applied to a conventional voltage-doubler circuit at pin 7 of the High Voltage Module. On the positive half cycle, the input capacitor of the voltage doubler $(0.006 \mu \mathrm{~F})$ is charged to -950 V through the forward-biased diode connected to ground at pin 9 of the module. The following negative half cycle adds its AC component (-950 V peak) to this stored DC value and produces a total peak voltage of -1900 V across the capacitor. This charges the $0.006 \mu \mathrm{~F}$ storage capacitor (connected across the two doubler diodes) through the second diode (now the for-ward-biased diode) to -1900 V . Two RC filters follow the voltage doubler to smooth out the AC ripple. A resistive voltage divider across the output of the filter network provides the -900 V slot lens potential.

## Anode Multiplier

The Anode Multiplier circuit (also contained in High-Voltage Module CR565) uses voltage multiplication to produce the +14 kV CRT anode potential. Circuit operation is similar to that of the voltage-doubler circuit of the Cathode Supply.

The first negative half cycle charges the $0.001 \mu \mathrm{~F}$ input capacitor (connected to pin 8 of the High Voltage Module) to a positive peak value of +2.33 kV . The following positive half cycle adds its positive peak amplitude to the voltage stored on the input capacitor and boosts the charge on the second capacitor of the multiplier (and those following) to +4.66 kV . Following cycles continue to boost up succeeding capacitors to values $\mathbf{+ 2 . 3 3} \mathbf{k V}$ higher than the preceding capacitor until all six capacitors are fully charged. This places the output of the last capacitor in the multiplier at +14 kV above ground potential. Once the multiplier reaches operating potential, succeeding cycles replenish charge drawn from the Anode Multiplier by the CRT beam. The $1 \mathrm{M} \Omega$ resistor in series with the output protects the multiplier by limiting the anode current to a safe value.

## Focus Amplifier

The Focus Amplifier, in conjunction with the auto-focus circuitry, provides optimum focus of the CRT beam for all settings of the front-panel INTENSITY control. The Focus Amplifier itself consists of two shunt-feedback amplifiers composed of Q145, Q152, and their associated components. The outputs of these amplifiers set the operating points of a horizontally converging quadrapole lens and a vertically converging quadrapole lens within the CRT. The convergence strength of each lens is dependent on the electric field set up between the lens elements.

Since the bases of Q145 and Q152 are held at constant voltages set by their emitter potentials, changing the position of the wiper arms of the ASTIG and FOCUS pots changes the current in the base resistors, R261 and R145. This changes the teedback currents in R245 and R246 and produces different output levels from the Focus Amplifiers; that in turn, changes the convergence characteristic of the quadrapole lenses.

Initially, at the time of adjustment, the FOCUS and ASTIG potentiometers are set for optimum focus of the CRT beam at low intensity. After that initial adjustment, the ASTIG pot normally remains as set, and the FOCUS control is positioned by the user as required when vlewing the displays. When using the FOCUS control, transistor Q152 is controlled as described above; however, an additional current is also supplied to the base node of Q145 from the FOCUS pot through R262. This additional current varies the base-drive current to Q145 and provides tracking between
the two lenses as the FOCUS control is adjusted during use of the instrument.

## Auto Focus

The convergence strengths of the quadrapole lenses also dynamically track changes in the display intensity. The VQ signal, applied to the CRT at pins 5 and 6, is linearly related to the VZ (intensity) signal driving the CRT control grid, and increases the strength of the lenses at higher CRT beam currents. (A higher beam current requires a stronger lens to cause an equal convergence of the beam.) The emitter follower Q500 buffers the VZ signal foffset 15 V by VR316) to the first and second quadrapole lenses. A linear relationship (as opposed to the "ideal" exponential relationship) between the Z-Axis drive (VZ) and quadrapole voltage (VQ) provides adequate dynamic focusing for low to medium Z-Axis drive. The High-Drive Focus adjustment R400 sets the attenuation factor at the output of buffer Q500. Capacitors C409 and C295 compensate for the capacitive loading of the quadrapole elements.

## Z-Axis Amplifler

The high-voltage, high-speed transresistance amplifier U227 produces VZ, the Z-Axis drive signal. The amplifier has two signal inputs: ZINT - a current input that determines the output voltage VZ , and $\overline{Z O N}$-a TTL gating signal that causes VZ to go to its lowest value (approximately 8 V ) when HI. Capacitor C139 supplies current to U227 during VZ transitions, R137 is a current limiter, and C234 is a bootstrap capacitor to speed up VZ edges.

## DC Restorer

The DC Restorer provides CRT control-grid bias and couples both the DC and the low-frequency components of the Z-Axis drive signal to the CRT control grid. This circuit allows the Z-Axis Amplifier to control the display intensity by coupling the low-voltage Z-Axis drive signal (VZ) to the elevated CRT control grid potential (about -1.9 kV ). Refer to Figure 3-10 for the following description.

The DC Restorer circuit operates by clipping an AC voltage waveform at the grid blas and the Z-Axis drive levels. The shaped AC waveform is then coupled to the CRT control grid through a coupling capacitor that restores the DC components of the signal.

GRID BIAS LEVEL. An AC drive voltage of approximately 300 V peak-to-peak is applied to the DC Restorer circuit from pin 7 of transformer T525. The negative half-cycle of the sinusoidal waveform is clipped by CR541, and the positive half-cycle ( 150 V peak) is applied to the junction of CR442, CR644, and R546 via R543. Transistors Q640 and Q641 (Q641 for instruments with serial numbers B012403 and above), and associated components form a voltage clamp circuit that limits the positive swing of the AC waveform at the junction.


Figure 3-10. DC Restorer.

Transistor Q640 is configured as a shunt-feedback amplifier with R645, C639, and R639 (C639 and R639 for instruments with serial numbers B012403 and above) and C643 (C643 for instruments with serial numbers B012402 and below) as the feedback elements. The feedback current through R645 develops a voltage across the resistor that is positive with respect to ground ( +15.6 V for instruments with serial numbers B012402 and below) on the base of the transistor. The value of this additive voltage plus the diode drop across CR644 sets the clamping threshold. Grid Bias potentiometer R100 varies the voltage across base resistor divider R642 and R644 and thus sets the feedback current through R645. For instruments with serial numbers B012402 and below, the adjustment range of the pot can set the nominal clamping level between +45 V and +75 V .

When the amplitude of the $A C$ waveform is below the clamping threshold, diode CR644 will be reverse biased and the AC waveform will be unclamped. For instruments with serial numbers B012402 and below, during the time the diode is reverse biased, transistor Q640 is kept blased in the active region by the charge retained on C643 from the previous cycle. As the amplitude of the AC waveform at the junction of CR442 and CR644 exceeds the voltage of C638 (or at the collector of Q640 for instruments with serial numbers B012402 and below), diode CR644 becomes forward biased, and the AC waveform is clamped at that level. Any current greater than that required to maintain the clamp voltage will be shunted to ground ( +15 V supply for instruments with serial numbers B012402 and bejow) by transistor Q640.

Z-AXIS DRIVE LEVEL. The variable Z-Axis signal (VZ) establishes the lower clamping level of the AC waveform applied to the High Voltage Module. When the amplitude of the waveform drops below the Z-Axis signal level, CR442 becomes forward biased, and the AC waveform Is clamped to the Z-Axis signal level. The VZ level may vary between +8 V and +50 V , depending on the setting of the front-panel INTENSITY control.

The AC waveform, now carrying both the grid-bias information and the Z-Axis drive information, is applied to a DC Restorer circuit in the High-Voltage Module where it is lowered to the voltage level of the CRT control grid (approximately -2 kV ).

DC RESTORATION. The DC Restorer circuit in the High-Voltage Module is referenced to the CRT cathode voltage via a connection within CR565. Capacitor C (labeling shown in fig. 3-10), connected to pin 15 of CR565, initially charges to a level determined by the difference between the Z-Axis signal level and the CRT cathode potential. The Z-Axis signal sets the level on the positive
plate of capacitor C through R443, CR442, and R546; the level on the negative plate is set by the CRT cathode voltage through resistor E and diode A, Capacitor D is charged to a similar DC level through resistor F and R442.

When the AC waveform applied to pin 15 begins its transition from the lower clamped level (set by the Z-Axis signal) towards the upper clamped level (set by the Grid Bias potentiometer), the charge on capacitor C increases. The additional charge is proportional to the voltage difference between the two clamped voltage levels.

When the AC waveform begins its transition from the upper clamped level back to the lower clamped level, diode A becomes reverse biased. Diode B becomes forward biased, and an additional charge proportional to the negative excursion of the AC waveform (difference between the upper clamped level and the lower clamped level) is added to capacitor D through diode B and resistor G. The amount of charge added to capacitor $D$ depends on the setting of the front-panel INTENSITY control, as it sets the lower clamping level of the AC waveform. This added charge determines the potential of the control grid with respect to the CRT cathode.

The potential difference between the control grid and the cathode controls the electron-beam current (the display intensity). With no Z-Axis signal applied (INTENSITY control off), capacitor $D$ will be charged to its maximum negative value since the difference between the two clamped voltage levels is at its maximum value. This is the minimum intensity condition and reflects the setting of the Grid Bias potentiometer. During calibration, the Grid Blas pot is adjusted so that the difference between the upper clamping level (set by the Grid Bias pot) and the "no signal" level of the Z-Axis drive signal (VZ) produces a control grid bias that barely shuts off the CRT electron beam.

As the INTENSITY control is advanced, the amplitude of the square-wave Z-Axis signal increases accordingly. This increased signal amplitude decreases the difference between the upper and lower clamped levels of the AC waveform, and less charge is added to capacitor D. The decreased voltage across capacitor $D$ decreases the potential difference between the control grid and the cathode, and more CRT beam current is present. Increased beam current increases the CRT display intensity.

During the periods that capacitor $C$ is charging and discharging, the control grid voltage is held stable by the long-time-constant discharge path of capacitor $D$ through resistor F. Any charge removed from capacitor D during the positive transitions of the AC waveform will be replaced on the negative transitions.

The fast-rise and fast-fall transitions of the Z-Axis signal are coupled to the CRT control grid through capacitor D. This AC-coupled fast-path signal sends the CRT electron beam to the new intensity level, then the slower DC Restorer path "catches up" to handle the DC and low-frequency components of the Z-Axis drive signal.

Neon lamps DS490 and DS491 prevent arcing inside the CRT by preventing the control grid and cathode from becoming too widely separated in voltage.

## CRT Control Voltages

The CRT Control Voltages circuitry produce the voltages and current levels necessary for the CRT to operate. Operational amplifier U168B, transistor Q269, and associated components form an Edge-Focus circuit that establishes the voltages for the elements of the third quadrapole lens. The positive lens element is set to its operating potential by Edge Focus adjustment pot R300 (via R393). This voltage is also divided by R278 and R277 and applied to the noninverting input of U168B to control the voltage on the other element of the third lens.

The operational amplifier and transistor of the Edge-Focus circuit are arranged as a feedback amplifier with R279 and R179 setting the stage gain. Gain of the amplifier is equal to the attenuation factor of divider network R278 and R277; so, total overall gain of the stage from the wiper of R300 to the collector of Q269 is equal to unity. The offset voltage between lens elements is set by the ratio of R279 and R179 and the +10 V reference applied to R179. Thls arrangement causes the two voltages applied to the third quadrapole lens to track each other over the entire range of Edge Focus adjustment R300,

Other adjustable level-setting circuits include $Y$-Axis Alignment pot R305, used to rotate the beam alignment after vertical deflection. This adjustment controls the amount of current through the Y -Axis alignment coil around the neck of the CRT and is set to produce precise perpendicular alignment between the X - and Y -Axis deflections. The TRACE ROTATION adjustment pot, R1077, is a front-panel control. The effect of the adjustment is similar to the $Y$-Axis Alignment pot, but when adjusted, it rotates both the $X$-Axis and the Y -Axis deflections on the face of the CRT. A final adjustable level-setting control is the Geometry pot R200, adjusted to optimize display geometry.

## SYSTEM I/O

The System I/O circuits (diagram 20) provide methods of getting various types of signals or voltages into and out of the scope. These include a GPIB interface, an interface to the AutoStep Sequencer, Word-Trigger interface, an audio bell, and the probe-power connectors used to supply power to active probes.

## GPIB

The GPIB interface provides an electrical interface adherent to the IEEE 488-1980 Standard using protocols defined in the Tektronix GPIB Codes and Formats Standard.

GPIB data transfers are done under control of U630, a GPIB Controller integrated circuit. The controller automatically produces proper handshaking and data direction control. Data is transferred to and from the GPIB bus through bidirectional buffer U624. Handshaking signals are transferred to and from the GPIB bus via the handshaking bidirectional buffer, U720. Data transfers between the GPIB Controller and the System Processor are through bidirectional buffer U532.

When pawer is first applied, the GPIBRESET signal from register U754 holds GPIB Controller U630 in its reset state. The System Processor then removes the reset and begins to initialize the internal registers of the GPIB Controller. To write data into the registers, the System Processor writes data to the memory-mapped addresses between 6800 h and 6807 h . These addresses produce a LO GPIBSEL and a LO address bit A3 applied to U332B and enable the GPIB Controller, Data is written to the internal register defined by address bits A0-A2.

The GPIB Controller is now initialized and begins watching the handshake lines on the GPIB bus, looking for a data transfer to be initiated by another GPIB device on the bus. Data transfer may also be initiated by the System Processor by writing data into the GPIB Controller data register. In either case, activity on the GPIB bus follows the sequences presented in Figures 3-11 and 3-12.

When data has been read into the controller from the GPIB bus, the GPIBINT (GPIB interrupt) request is asserted, telling the System Processor that GPIB data is available. To receive the data, the System Processor reads the GPIB Controller internal data register, automatically resetting the interrupt request.

Status of the GPIB operations is displayed on the three front-panel GPIB Status LEDs. These LEDs are turned on or off by the System Processor by writing three control bits into GPIB Status Register U754.

The GPIB may be set up to operate with a ThinkJet* printer or any plotter using the Hewlett-Packard Graphic Language ${ }^{*}$ as a listen-only device on the bus. No controller may be used, and the printer/plotter should be the only device other than the 2440 on the bus.

See the Programmers Reference Guide included with this instrument for the GPIB commands and functions implemented in this oscilloscope.


Figure 3-11. GPIB data flow diagram.

The GPIB may be set up to operate with a Think-Jet ${ }^{(0)}$ printer or any plotter using the Hewlett-Packard Graphic Language ${ }^{\circledR}$ as a listen-only device on the bus. No controller may be used, and the printer/plotter should be the only device other than the 2440 on the bus.

## Sequencer Output Circuit

The Sequencer Output circuit drives two output BNC connectors and accepts input from a third BNC connector. The outputs/input are called SEQUENCE OUT, STEP COMPLETE, and SEQUENCE IN, respectively. SEQUENCE OUT steps LO (TTL level) to indicate when a sequence completes execution; STEP COMPLETE steps LO to indicate when a step in a sequence completes. A TTL step from HI to LO (or grounding the input) to SEQUENCE IN restarts a temporarily halted sequence. See the Operators Manual included with this instrument for more information.

The System $\mu \mathrm{P}$ controls the SEQUENCE OUT and STEP COMPLETE output levels via Miscellaneous Register U760 (diagram 1). When a sequence and/or step is complete, the System $\mu \mathrm{P}$ sets SEQOUT and/or STEP COMP HI out of the Miscellaneous Register.

SEQOUT is coupled to Q104 via R300, a $1 \mathrm{k} \Omega$ resistor. A TTL HI voltage level, dropped across the R330 and the
base/emitter of Q104, is great enough to saturate Q104 and provides a LO SEQUENCE OUT at J1903. When SEQOUT is LO, Q104 is off. SEQUENCE OUT at J1903 is pulled up to about +3 V via R108. (The +5 Volt supply is zener-regulated by R105 and VR 105 to provide the +3 Volt collector supplies for Q104 and Q107.)

The circuit action of Q107 and its surrounding circuitry is identical to the Q104 stage with STEP COMP driving the base of Q107 via R108 to provide STEP COMPLETE at J1904. CR104/CR107 provide output protection for Q104/Q107.

To read the SEQUENCE IN at J1905, the System $\mu \mathrm{P}$ periodically sets SEQINCS (Sequence In Chip Select) LO via Miscellaneous Register U884 (diagram 1). SEQINCS is routed to one input of OR-gates U250C and U132A; the other input of OR-gate U250C is connected to the System $\mu \mathrm{P} \overline{\mathrm{WR}}$ (write) line, and the other input of U132A is connected to the System $\mu \mathrm{P} \overline{\mathrm{RD}}$ line. With SEQINCS LO, the $\overline{W R}$ and/or $\overline{R D}$ can drive the output of their respective OR-gate LO, when they are asserted.

After setting SEQINCS LO, the System $\mu$ p next asserts $\overline{\text { WR LO. This LO drives the output of OR-gate U250C LO }}$ to RESET the Q output of D-type Flip-Flop U894B LO. NEXT, $\overline{R D}$ is asserted LO ( $\overline{W R}$ goes H ) to drive the out-


Figure 3-12. GPIB three-wire handshake state diagram.
put of OR-gate U132A LO. This LO enables the upper-four buffers of the Octal Buffer U120. With the Q-output of Flip-Flop U894B connected to the input of one of the enabled buffers, that reset-forced LO obtained at $\overline{W R}$ is coupled to the DO line of the System $\mu \mathrm{P}$ Data Bus. The System $\mu \mathrm{P}$ monitors the DO bit as long as $\overline{R D}$ and SEQINCS are asserted.

The input to inverter U424E is normally pulled up to +5 volts by R120. This HI is inverted LO by U424E and routed to the positive-triggered clock input of Flip-Flop U894B. If, during the time $\overline{R D}$ is asserted, SEQUENCE $\mathbb{N}$ steps LO at J1905, it drives the clock input of U894B HI and the +5 volts hardwired to the D-input of the flip-flop latches to the Q output. With the Quad Buffer still enabled by $\overline{\mathrm{AD}}$, the System $\mu \mathrm{P}$ reads the transition via data bit DO and restarts the temporarily-halted sequence.

## Word Trigger and GPIB Status Control Register

The Word Trigger circuit provides interface and control of the external Word Trigger Probe. Two bits from Control Register U754 are used to set the recognition mode of the Word Trigger Probe. Forty bits of serial data are applied to the W DATA (word data) line and clocked into the serial shift register in the word probe by toggling the W CLOCK (word clock) line. Once loaded, the Word Trigger Probe outputs a trigger pulse each time (and as long as) the set conditions are met.

The WDTTL output is applied to the trigger circuits where, if selected as the trigger source, it produces a scope trigger event. The trigger signal is buffered to the rear panel by U844D, Q720, and the associated components. Output levels are TTL compatible, with the maximum HI level being set by R716 and VR717. Output impedances are 47 ohms LO and 227 ohms HI. Diode CR722, zener VR717, and resistors R717 and R718 provide protection of the output circuit should an out-of-range voltage be applied to the output connector.

The remaining inputs and outputs of Control Register U754 are used to control the GPIB Status LEDs and to reset GPIB Controller U630.

## Bell

The Bell circuit allows the scope to produce an audio tone to draw the operator's attention to certain warning and error conditions. The circuit consists of a free-running oscillator whose signal is gated through the output speaker.

The oscillator consists of timer U274, configured as an astable multivibrator (oscillator), and output transistor Q594, used to buffer the oscillator output. Current flowing in R274 and R276 charges C372 up until it crosses the
trigger level at pin 2 of U274. This sets the output applied to the base of Q594 LO, turning the transistor off, and sets the discharge output at pin 7 to ground potential. Capacitor C372 now discharges through R276 until the threshold level at pin 6 is reached, at which time the output at pin 3 goes HI and the discharge pin goes to a highimpedance state. Capacitor C372 begins to charge through R274 and R276 again, completing the cycle. The cycle continues as long as instrument power is applied, alternately turning Q594 off and on with an approximate $50 \%$ duty cycle.

The BELL line from the Miscellaneous Register (U760, diagram 1) is used to gate this oscillator signal through the speaker to produce the audio output. As long as BELL is LO, transistors Q596, Q558, and Q592 are off, and current is cut off to speaker LS498.

When BELL goes HI, transistor Q596 turns on, which in turn, turns on Q588. With Q588 on, the base of Darlington transistor Q592 is pulled HI. Now, whenever the oscillator transistor Q594 is on, proper biasing conditions for Q592 are established and current flows from the $+5 \mathrm{~V}_{\mathrm{D}}$ supply to ground through Darlington Q592, the speaker LS498, and transistor Q594. When Q594 turns off, current flow is interrupted until the oscillator turns Q594 back on.

Since LS498 is inductive, the current decay portion of its cycle (Q594 off) tends to force pin 1 of the speaker above the $+5 \mathrm{~V}_{0}$ supply level. Diode CR594 becomes forward biased in this case and shunts the decay current back to the $+5 \mathrm{~V}_{\mathrm{D}}$ supply, protecting transistor Q594 from overvoltage conditions.

As long as the BELL line remains HI, the speaker produces an approximate 2 kHz tone. In practice, the System $\mu \mathrm{P}$ sets the BELL line HI for a short time ( $\simeq 4 \mathrm{~ms}$ ), turning Q588 on, starting the tone and rapidly charging C590. When BELL returns LO, C590 gradually discharges through R594. As the capacitor discharges, bias on Q592, and thus current through the speaker, is reduced, causing the sound to gradually fade out in a pleasing "bell-like" tone.

## Probe Power

The Probe Power outputs on the rear panel provide access to three of the instrument power-supply voltages and may be used to power approved voltage- and current-probe accessories. Contact your Tektronix sales representative for a list of approved probe accessories.

## Video Option Control Register

The Video Option Control Register (U750 on diagram 20) is written to by the System Processor (address-decoded location 6012h) to control operational setup of the Video Option. The Video Option Control Register is initialized on power-up and provides for control of the following functions:

1. Selection of trigger field (Field1 or Field2).
2. Choice of triggering on positive- or negative-sync input signals (NEG-SYNC).
3. Selection of correct polarity of the offset signal via the CH2 INV signal.
4. Control of the display functions (VIDEO CLAMP and FAST CLAMP).
5. Enabling the Video Trigger Circuit to trigger the scope.
6. Selection of TV Line Coupling-allowing all lines to produce a trigger signal to the main Trigger circuit of the scope.

## VIDEO OPTION

The Video Option (diagram 21) consists of additional hardware and firmware installed in the host instrument to enhance triggering on and viewing of composite video signals. The Video Option block diagram located in the tabbed foldout pages in the rear of the manual may be an aid in following the Video Option circuit descriptions.

The Video Option circuitry contains both video-signal processing and trigger-generation circuits. The video-signal processing circuits stabilize the input signal and separate the television synchronization signals (horizontal and vertical sync pulses) from the composite video signal. The trigger-generation circuits then count these separated sync pulses to determine when a TV Trigger signal is to be produced.

In the video-signal processing circuits, the gain of the AGC (automatic gain control) Amplifier is automatically adjusted to produce the correct signal amplitude to the Sync Pickoff Comparator for proper sync separation over a wide range of input signal levels. The Trigger BackPorch Clamp adjusts the back-porch level of the input signal through the Fixed-Gain Amplifier on each sync pulse. The feedback to the Fixed Gain Amplifier compensates for level shifting caused by any power-line ripple riding on the composite video signal. The Sync-Tip Clamp circuit monitors the horizontal-sync pulse amplitude and produces the automatic-gain-control voltage that sets the gain of the AGC Amplifier. Sync pulses are separated from the composite video signal by the Sync Pickoff Comparator. The horizontal- and vertical-sync pulses are further separated by the Pulse Stretcher and Field Generator circuits for use in producing the horizontal clock and field-sync signals needed by the Trigger Generation circuitry.

To set up the Video Option operating modes, the System Processor writes control settings to the Video Mode Option Register (diagram 20) in the System I/O cir-
cuitry. The latched setting in the register is held until a different mode is needed. Programmable counters, also under System processor control, count the extracted horizontal sync pulses (lines) until the line number for the selected trigger point is reached. At that point, if the main trigger circuit is finished with holdoff, the TV Trigger Generator circuit produces a TV Trigger to the A/B Trigger Generator to trigger the next storage acquisition.

An additional display function added to Channel 2 is the TV CLAMP feature. When enabled, the circuitry holds the back-porch level of the displayed signal on Channel 2 at ground level. The Channel 2 Vertical Display Clamp circuit checks the back-porch levels of the incoming TV signal on Channel 2 and produces offsetting voltages to the Channel 2 Preamplifier to bring those levels back to ground reference. The circuit action produces a stable vertical signal display of a TV signal by removing power supply ripple that may be present. Either inverted or noninverted signals may be displayed with the TV CLAMP feature.

## Video Signal Processing Circuitry

AGC AMPLIFIER. The AGC (automatic gain control) Amplifier, Q514, U612, and U710B, amplifies the composite-video input signal from the selected trigger channel. Stage gain is controlled by feedback that is derived from the amplitude of the incoming horizontal sync pulses. The amplifier itself is formed by two crossconnected differential amplifier pairs in U612 that permit normal or inverted amplification of the signal. The frontpanel SLOPE/SYNC switch selects whether the amplifier is inverting or noninverting to match the required signal polarity for the sync-separation circuits. For correct operation of the sync separation circuit, the composite-video signal must be sync-negative; therefore, if a "noninverted" signal display has positive sync, the SLOPE/SYNC switch may be pressed to invert the signal (+ SLOPE LED is on for positive-sync input display). Inversion only occurs in the trigger Sync Separator path; the display polarity remains unaffected.

Gain of the AGC Amplifier is controlled by the action of the Trigger Back-Porch Clamp, the Sync-Tip Clamp, and the Automatic Gain-Control circuitry working together to set the channel resistance of FET Q514 and thereby the gain of AGC Amplifier U612. Amplifier gain is automatically adjusted to maintain the sync-tip level at a known point relative to the back-porch amplitude of the signal. This action provides an accurate and stable pickoff point on the signal to the Sync Pickoff Comparator circuit (Q504 and Q510) with input video signals of different or varying amplitudes. The minimum gain of the circuit is decreased (to permits the application of higher amplitude signals) by the use of constant-current diodes CR526 and CR620 as the current sources for the differential amplifiers.

When power is first applied, the operating level of the AGC Amplifier is established by feedback only. With no
signal applied, the channel resistance of Q514 is minimum, setting the gain of the AGC Amplifier to maximum. With maximum gain and no signal, the feedback loops of the Back-Porch Clamp and the Sync-Tip Clamp set the circuit gain as if an average "ground" signal were being received.

The composite-video input signal is applied to one input of the differential AGC Amplifier at pin 3 of U612 and to Dc-Offset Amplifier U710B via a low-pass filter composed of R714 and C714. The low-pass filter averages the signal at the input of U710B so that only the average (dc) signal level appears at the output of U710B and on pin 11 of U612. Since the input signal swings about this average level, the AGC Amplifier output signal will be centered in its linear amplification region.

The base-emitter bias of the differential output transistors within U612 are controlled by the NEG-SYNC signal from Video Option Control Register U750 (diagram 20). When the NEG-SYNC bin is set HI, the transistors connected to pins 2 and 9 will be biased on, with those at pins 6 and 13 biased off. When NEG-SYNC is set LO, the conducting transistors are switched, and the polarity of the output signal driving transistor Q612 is inverted. Common-base transistor Q612 level shifts the output signal from the AGC Amplifier and provides voltage gain to drive U610D.

FIXED GAIN AMPLIFIER. The Fixed Gain Amplifier circuit, formed by U610A, B, and C, Q502, and U710C, provides additional gain to the video signal from the AGC Amplifier. The Trigger Back-Porch Clamp circuit monitors the back-porch level of the resulting signal and injects an offsetting dc level into the Fixed Gain Amplifier via U710C to shift that level to approximately +4.5 V .

Emitter-follower U610D drives one input of a differential amplifier made up of U610A and U610B, while the other input is driven by the output signal of U710C. Transistor U610C and its associated components form the current source for the amplifier. The collector output of U610B drives the input of the Sync Pickoff Comparator.

Transistor Q502 and its associated circuitry act as a start-up circuit that monitors the dc output level of U610B and applies an offset voltage to pin 10 of U710C should that level go below zero volts. This occurs when going from a "no-signal" or low-signal condition to a strong signal. If the dc output level goes below ground, diode CR612 will become forward biased, shutting off Q502. With Q502 off, the -15 V supply applied via resistor R506 will forward bias CR606 to charge C713 negatively. This pulls the output voltage of U710C negative and decreases base drive to U610B. Reducing base drive reduces the collector current so that the collector voltage of U610B returns positive until the above zero-volt output level is restored and CR612 becomes biased off.

SYNC PICKOFF COMPARATOR. The Sync-Pickoff Comparator, composed of Q504 and Q510, switches when the amplitude of a sync pulse crosses the comparator threshold level. The switching threshold is set by the biasing resistors of Q510, R408 and R409, to about 50\% of the sync level to eliminate any video information. The output signal from the collector of Q510 is the composite of all detected sync pulses, and the output of Q504 is an inverted replica of that signal.

SYNC-TIP CLAMP AND AUTOMATIC GAIN CONTROL. Transconductance Amplifier U510, in conjunction with the AGC Amplifier, is used to clamp the sync-tip level. Amplifier U510 is enabled by the bias current supplied by Q512 when sync tips turn that transistor on. This amplifier acts as a weak operational amplifier to set the sync-tip level constant when Q512 is conducting to supply bias current to pin 5 of U510.

The Sync-Tip Clamp holds the negative-sync tips at about +0.5 V , so the resulting sync pulses are approximately 4 V in amplitude. Anytime the negative-sync tips at the collector of U 610 B go below about +0.5 V , input pin 3 of U510 will go below the ground reference at the other input. This causes the output of U510 to go low when enabled, and C512 begins discharging slowly toward -15 V . This decreasing voltage is applied to the gate of FET Q514 to increase the channel resistance and decrease the gain of the AGC Amplifier. Since U510 is a transconductance amplifier, it cart change the voltage across C514 only a small amount during each sync pulse, and a few horizontal-line cycles are needed to reduce the gain of the AGC Amplifier to the new operating level. Between sync tips, when amplifier $U 510$ is disabled, the long time constant of R610 and C512 holds the bias for Q514 (and thus gain of the AGC Amplifier) nearly constant.

Diode CR502 acts to reduce AGC Amplifier gain quickly if the negative-sync-tip amplitude at the collector of U610B drops below -0.8 V . If the diode becomes forward biased, as it might should the signal amplitude go suddenly negative, Q510 will be turned on for a longer time until the signal amplitude returns to a lower level. Amplifier U510 can then increase the channel resistance of Q514 more quickly to reduce gain of the AGC Amplifier and return the synctip amplitude to the correct level.

TRIGGER BACK-PORCH CLAMP. The Trigger BackPorch Clamp circuit formed by U504, U410A, and associated components, is enabled for a short time during each horizontal-sync pulse immediately following the sync tip (during the back-porch time). The output of the Trigger Back-Porch Clamp is used to hold the back-porch level of the composite-video signal to a predetermined dc level. This, in combination with the action of the Sync-Tip Clamp, produces sync pulses that are approximately 4 V in amplitude.

## Theory of Operation-2440 Service

Transconductance Amplifier U504 is enabled by turning transistor U410A off on the falling (trailing) edge of the inverted sync pulse from Q504 (via C308). Bias current to turn on U504 is then supplied through R403. The amplifier will stay enabled until the current supplied by resistor R214 charges C308 back positive enough to bias U410A back on (in approximately $1 \mu \mathrm{~S}$ ). During the time that U504 is enabled, it senses the back-porch level of the composite-video waveform applied to pin 3 via resistive divider R613, R602, and R604. Depending on whether the sensed level is above or below the ground reference level on pin 2, the amplifier output will either charge or discharge capacitor C 713 to a new voltage level. This will slightly change the offset voltage applied to pin 4 of U610B (via U710C), shifting the entire composite-video waveform in the direction required to hold the back-porch level at +4.5 volts (zero volts on pin 3 of U504). During the period between back porches, C713 acts as a hold capacitor to maintain the offset bias on U610B.

PULSE STRETCHER. The Pulse Stretcher lengthens the horizontal-sync pulse width to produce a more symmetrical, faster rise-time clocking pulse. It also removes alternate equalizing and serrated pulses that occur during the NTSC TV signal vertical-sync block from the composite-sync waveform in order to maintain the correct horizontal clock rate.

Transistors U420B, U420C, and associated components form a monostable multivibrator used to stretch the width of the horizontal-sync pulses. The leading edge of each horizontal-sync pulse turns on U420C which, in turn, reverse biases diode CR224 via C325 to turn off U420B. The resulting HI at the collector of U420B keeps U420C biased on (via R421). The output at the collector of U420B remains HI until C325 charges to about +1 volt via R224; then, CR224 becomes forward biased to once again turn U420B on. The collector voltage of transistor U420B then drops to about +0.4 V , at which point diode CR329 conducts to clamp the output at one diode drop above ground. This stretched output pulse from the monostable multivibrator is level-shifted down one diode drop through CR328 to produce the TTL-compatible HORIZCLK signal used to generate trigger signals to the main Trigger circuit of the oscilloscope.

Since the equalizing and serration pulses in the vertical-sync block occur at twice the horizontal-sync rate (see Figures 3-13 and 3-14), every other one must be prevented from triggering the monostable multivibrator to keep the line count correct. The DLY'D HCLK (delayed Horizontal clock) applied to the base of U420B (via R210) holds that transistor on for a period of time between the normal horizontal line-sync pulses. This action effectively removes the unwanted pulses from the HORIZCLK output by preventing them from triggering the multivibrator circuit.

CLOCK FREE RUN. If non-NTSC standard television signals are being used, the vertical-sync block may not be serrated. To maintain the proper horizontal-sync rate during the absence of signal-supplied horizontal pulses, the Clock Free-Run circuit produces "artificial" clock pulses. Therefore, the line count will continue and be correct when the next horizontal-sync pulse does arrive. The signal used as the self-generated HORIZCLK signal is derived from the VCO (voltage-controlled oscillator) output (2XH) of the Phase-Locked Loop circuit. That signal, at twice the horizontal-sync rate, is divided by two at the $Q$ output of flip-flop U220B. It is then wire-ORed into the HORIZCLK signal line via R334 and CR332. If a horizontal-sync pulse is not present to trigger the monostable multivibrator, CR332 will be biased on by the HI HCLK to pass that pulse to the HORIZCLK signal line. When the PhaseLocked Loop (PLL) circuit is locked (synchronized) with the incoming horizontal sync, the HCLK rising edge will slightly lag the incoming sync pulse to prevent jitter of the HORIZCLK signal to U524B.

PHASE-LOCKED LOOP (PLL). Phase-Locked Loop U314 locks onto the horizontal-sync signal to produce a synchronized clock at twice the horizontal-sync rate $(2 \mathrm{XH})$. The 2XH clock is used to extract the various sync- and field-identification signals from the composite-sync waveform. It is also divided and delayed to obtain the DLY'D HCLK (see Figure 3-13) signal used in eliminating alternate equalizing and serration pulses from the HORIZCLK signal and the input to the PLL Phase Comparator inputs.

The 2XH VCO (voltage-controlled oscillator) output is divided by two by flip-flop U220B to produce both the HCLK and HORIZCLK signals at the horizontal-line rate. Horizontal sync from the input signal is applied to the Phase Comparator input of U314 at pin 14 via U308B. The HORIZCLK from the $\bar{Q}$ output of U220B is applied to U314 at pin 3 through U308C.

Phase Comparator output 2 (PC2 OUT at pin 13) of PLL U314, outputs the PLL ERROR signal whenever the leading edges of the $\overline{\text { HORIZCLK }}$ signal on pin 3 and the horizontal-sync pulses on pin 14 do not coincide. The error signal output is integrated by R322, R320, and C322 to produce a voltage (applied to pin 9) used to correct the operating frequency of the VCO. When either no phase errors exist or no signals are present to compare (both phase-comparator inputs at the same level), pin 13 goes to a high-impedance state, and the voltage on C322 maintains the operating frequency of the VCO. Resistors R323 and R324 and capacitor C324 set the operating frequency range of the PLL circuit. A bleeder resistor, R327, reduces the charge on C322 slightly between each error signal output so that the HORIZCLK signal will always lag the horizontal-sync of the input signal by a small amount. This


Figure 3-13. Video Option waveforms.


Figure 3-14. Video Option field-sync identification.
slight lag prevents the possibility of jitter in the HORIZCLK signal going to clock TV Trigger flip-flop U524B.

A similar signal (PLL LOCK) from pin 1 of the Phase Comparator is integrated by R326 and C330. If the PLL is not locked onto the input signal, the PLL LOCK output remains in the LO state long enough to be sensed by the PLL Unlock Detector. The long LO state of the PLL LOCK signal discharges C330 negative enough with respect to the emitter voltage of Q330, that the transistor becomes biased on. The collector voltage of Q330 will then go high, and Vertical Sync flip-flop U310A and Delayed Horizontal Clock flip-flop U220A will both be reset by the HI UNLOCKED signal. With U220A and U310A both reset, the DLY'D HCLK and VERTSYNC signals are held LO, and the equalizing pulses and vertical-sync serrations are no longer prevented from passing through NOR-gate U308B. The PLL Phase Comparator then sees the entire input signal during attempts to lock on so that locking will occur in the proper range. While the unlocked condition exists, the Channel 2 Vertical Display Clamp circuit is held disabled (via R328) by the HI state of TVCLAMP to prevent an invalid offset from being sent to the Channel 2 Vertical Preamplifier.

When lock is achieved, the phase difference between the two input signals becomes very small. The PLL LOCK pulse output level remains in the HI state (no error) long enough that C330 is allowed to charge positive and turn off transistor Q330. UNLOCK then goes LO to remove the resets from flip-flops U310A and U220A, allowing them operate, and TVCLAMP goes LO to enable the Channel 2 Vertical Display Clamp circuit. Unwanted equalizing pulses and the vertical-sync serrations are now prevented from passing to PLL Phase Comparator inputs by the DLY'D HCLK (delayed horizontal clock) and VERTSYNC signals applied to the PLL Phase Comparator Input NOR-gates, U308B and U308C (see Figure 3-13).

The DLY'D HCLK is shifted one-quarter HCLK cycle. When the DLY'D HCLK is HI, the outputs of both NORgates at the inputs to the PLL Phase Comparator are held LO, and the alternate equalizing pulses of composite-sync signal are prevented from passing to the PLL Phase Comparator. The vertical-sync serrations are prevented from passing through NOR-gate U308B by the HI VERTSYNC signal applied during vertical-sync times. Both types of unwanted pulses are thereby eliminated from the Phase Comparator inputs. The remaining sync pulses to be compared with the HORIZCLK signal are then only at the horizontal-sync frequency, and the VCO output frequency shifts slightly as necessary to bring that frequency to precisely twice the horizontal-sync rate $(2 \mathrm{XH})$. The charge on capacitor C322 holds the VCO to that output frequency throughout the vertical-sync period when all serration pulses are disabled from the Phase Comparator input and no comparisons are being made.
delayed horizontal clock. The Delayed Horizontal Clock (DLY'D HCLK) is used to remove alternate equalizing pulses and serration pulses from the composite-sync waveform in order to maintain precise sync for horizontal line counting. The PLL-generated HCLK signal from the Q output of U220B is clocked into U220A by the $\overline{2 X H}$ pulse from NOR-gate U308A (acting as an inverter). The inversion of the two-times clock delays the Q output of flip-flop U220A by one-quarter of a horizontal clock (HCLK) cycle. The quarter-cycle delay enables the HI portion of the output (applied to U420B via R210) to mask the alternate, unwanted equalization and serration pulses (occurring at twice the horizontal-sync rate) from the HORIZCLK output by preventing U420B, in the Pulse Stretcher circuit, from switching during those time periods. The same signal masks the unwanted equalization pulses from the PLL inputs by disabling NOR-gates U308B and U308C from passing signals to compare during the DLY'D HCLK HI state. All the vertical-sync serration pulses are eliminated from the PLL Phase Comparator input by the HI state of the VERTSYNC signal applied to the input NOR-gates.

VERTICAL SYNC. The Vertical Sync circuitry outputs pulses for both the Field 1 and the Field 2 vertical-sync times. These VERTSYNC pulses are used to toggle the Field Sync Generator. The VERTSYNC signal is produced by clocking the level of the COMPSYNC signal on the D input (pin 5) of U310A into that flip-flop using the inverted two-times horizontal clock $\overline{2 \times H}$. Figure 3-14 shows that only during a vertical-sync interval will the COMPSYNC signal be HI on the rising edge of the $\overline{2 \mathrm{XH}}$ clock. At all other (non-vertical sync) times, the COMPSYNC signal will be LO on the rising edge of the 2 XH clock. Thus, the Q output of flip-flop U310A will be clocked HI during verticalsync intervals for VERTSYNC, and it will be clocked LO during the rest of the field.

FIELD-SYNC GENERATOR. The Fieid-Sync Generator produces the FIELD signal used in identifying the individual fields of picture information. For interlaced-scan signals, the signal identifies which field a given line of picture information belongs to (exceptions are explained in the Line Counter description); while, for non-interlaced-scan signals, it toggles to indicate vertical sync. The circuit consists of an Interlace/non-Interlace Detector, a Vertical-Sync Latch (interlaced), and a Vertical-Sync flip-flop (non-interlaced).

To detect whether a signal is interlaced (two verticalsync pulses per frame) or non-interlaced (only one vertical-sync pulse per frame), flip-flop U310B is clocked to transfer the level of the HCLK signal on the $D$ input to the $\bar{Q}$ output by the VERTSYNC clock at the start of a vertical-sync period. For non-interlaced displays, the
vertical-sync rising edge always occurs during a HI portion of the HCLK signal, and the $\bar{Q}$ output of U310B will be clocked HI ; while, for interlaced displays, the $\overline{\mathrm{Q}}$ output will alternate between HI and LO.

The $\bar{Q}$ from pin 12 of U310B controls two other flipflops U430A and U430B, through the circuit action of transistors U420A and Q422. If the output of U310B is not toggling (non-interlaced signals), transistor U420A will be turned off by pull-down resistor R426. This allows the base bias voltage of Q422 to go positive as C426 charges through R429 and R428. Soon, Q422 is biased off and flip-flop U430B becomes reset. The reset on U430B from C426 holds the $\bar{Q}$ output HI to reverse bias CR334 and isolate the $\overline{\mathbf{Q}}$ output from the FIELD signal line. At the same time, the LO TVINTERLACED signal applied to the set input of U430A from the collector of Q422 enables that flip-flop to toggle on the rising edges of the vertical-sync pulses applied to the clock input (pin 3). This toggling is required to reinitialize the counters after they have counted their last lines. The TVINTERLACED signal is also applied to the Processor Miscellaneous Buffer (U854, diagram 1) where it may be read by the System $\mu \mathrm{P}$ to determine whether the video signal is interlaced or non-interlaced. The System $\mu \mathrm{P}$ must be able to determine this information to properly control the line counting.

For interlaced displays, the output from U310B will toggle. This will alternately turn transistor U420A on and off at the vertical-field rate. The first time U420A gets turned on by an interlaced-system signal, it discharges C426 and turns Q422 on. Capacitor C426 will charge positive through R429 and R428 when U420A turns off, but the long time constant of the charging path prevents the charge from getting positive enough to reassert the reset to U430B before the next toggle cycle once again discharges the capacitor. Flip-flop U430A is held set by the HI TVINTERLACED (interlaced) signal asserted from the collector of Q422, and CR336 is reverse biased to isolate U430A from the FIELD signal line. The resulting FIELD signal, as a result of the output of flip-flop U430B, will be HI for all lines in Field 1 and LO for all lines in Field 2 (with a few exceptions that are explained in the Line Counters description).

LINE COUNTERS. Line Counter U530 contains three programmable counters (at decoded addresses 6808h through 680Fh) that are set by the System Processor to determine when the chosen line number in the field selected for triggering is reached. The various control registers of the counter are set up to count horizontal clock pulses (lines) to determine line location in the field.

The Line Counter is enabled whenever its address block is decoded by the system Address Decode circuitry.

To differentiate it from the GPIB circuitry (which also answers for the same block of decoded addresses), the Video Option uses address bit A3 as a second chip select. Specific registers within the Line Counter are addressed using address lines A0-A2 applied to the register-select inputs. Reading and writing of the selected register is controlled by the System $\mu \mathrm{P}$ using the $\overline{W R}$ select line while the E (enable) clock synchronizes transfers to the System $\mu \mathrm{P}$ rate.

Once the proper setup data (defining counter mode and line number) is written to the Line Counter, the enabled counter will begin counting horizontal clock pulses (lines). Counters are alternately started as the FIELD signal toggles, and counters 1 and 2 produce a LO output when their predefined counts are reached. Counter 3 is used to determine the number of LINES in a FIELD (of FIELD 2 if in an interlaced system). The System $\mu \mathrm{P}$ checks the "previous field" line count by reading the counter contents via the data bus.

LINE COUNT ADJUSTMENTS. Depending on the type of signal being triggered upon (System M or non-System M ) and the desired line for trigger, the System $\mu \mathrm{P}$ adjusts both the numbers preloaded to the counters and the field to which the assigned line-count relates. These line-count and relative-field adjustments are required for the following reasons.

1. The HORIZCLK coincident with a switch in the FIELD indicator does not produce a count. Since the FIELD change doesn't enable the opposite counter in time to catch the rising edge of the HORIZCLK (responsible for the change), the preloaded line count must be reduced by one.
2. The counters cannot produce a "zero-count" delay; i.e., the counter output goes LO one count (line) after the counter reaches zero. Even when set to zero, a count must still occur; so the line count must be reduced by one again.
3. The counter outputs merely arm the trigger circuit, with the next line sync producing the actual trigger; therefore, line count must be reduced again by one.

RELATIVE FIELD ADJUSTMENTS. For non-System M television signals (line one coincident with the FIELD sync pulse), the line-adjustment requirements described above require that the first three lines of either field be counted relative to the previous FIELD pulse.

## Theory of Operation-2440 Service

Since, by definition, System-M fields begin numbering lines three lines before the vertical field-sync occurs, and due to the line-adjustment requirements described above, the first six lines of System-M fields must be counted relative to the previous FIELD pulse.

As stated in the "Line Count Adjustments," the trigger arming pulse occurs one line count prior to reaching the selected trigger line. Depending on whether the System Processor has selected the arming pulse relative to Field 1 or Field 2, either NAND-gate U541C or NAND-gate U541D will be enabled by a control bit (FLD1 or FLD2) from Video Option Control Register U750. The selected pulse, when it occurs, is passed through the enabled gate, through U541A and U424D, and appears as a clock pulse at the trigger-arm flip-flop, U524A.

TV TRIGGER GENERATOR. The TV Trigger Generator circuit produces the signal to trigger the Oscilloscope at the designated horizontal line. The output from the Line Counter arms the TV Trigger Generator circuit, enabling a trigger to be produced on the next line-sync pulse. Generation of a TV trigger from the circuit is enabled by a HI TVENA (TV-enable) bit from Video Option Control Register U750 (diagram 20).

In the Video Option, as in the main Trigger Generator a trigger signal is inhibited from being produced during trigger holdoff. For the holdoff period, the ATHO (A-trigger holdoff) signal applied to U424C is HI to hold arming flipflop U524A reset which, in turn, holds trigger flip-flop U524A reset. When the holdoff processing cycle is completed, the ATHO signal goes LO to remove the reset from U524A and enable triggering.

Assuming TV Line Coupling mode is not active, the LINECPL (line coupling) bit applied to U541B pin 5 will be LO, and arming flip-flop U524A will be enabled. When the Line Counter has counted the proper number of lines relative to the Processor-selected field, flip-flop U524A will be clocked. This produces a HI "armed" level applied to the reset input of trigger flip-flop U524A that releases the reset condition of the flip-flop. The next HORIZCLK pulse (line) then clocks a LO to the $\overline{\mathbf{Q}}$ output, TVTG, that defines the trigger point in the acquisition record. The TVTG output is reset HI when trigger holdoff (ATHO) goes HI to reset the flip-flop via U424C and U524A.

When TV Line Coupling mode is selected, the LINECPL bit from the Video Option Control Register will be set HI. This causes flip-flop U524A to be immediately armed when A trigger holdoff ends by forcing a set signal to pin 4 of that flip-flop through NAND-gate U541B. In this mode, a trigger will occur on the first line sync following the end of
each holdoff interval. The resulting display will be stable with respect to horizontal sync pulses but will not be stable with respect to the vertical sync pulses.

CH2 VERTICAL DISPLAY CLAMP. The Channel 2 Display Clamp circuit clamps the back-porch level of the triggered-display signal near the on-screen zero-volt reference. This allows automatic positioning of the display on the crt when probing various points with differing dc levels and removes vertical jitter that would be caused by $60-\mathrm{Hz}$ hum riding on the television signal.

The Channel 2 Pickoff ( CH 2 PO ) signal from the Channel 2 Preamplifier is applied through a low-pass filter formed by R524 and C514. The filter removes all the highfrequency components from the composite video signal, but its purpose is to specifically remove the color-burst modulation from the back-porch of the sync pulses. The filtered sync pulse is then amplified with respect to ground during its back-porch interval either by operational amplifier U514 or by operational amplifier U520, depending on the display polarity chosen by the operator. The selected comparator, when gated on (via U410A and either R410 or R411) during the back-porch interval, produces a dc-offset voltage used to shift the back-porch level of the displayed channel 2 signal to zero volts. Capacitor C522 acts as a hold capacitor to maintain a constant dc offset to the Channel 2 Vertical Preamplifier between back-porch samples. Operational amplifier U710D buffers the offset signal to the Channel 2 Preamplifier.

Offset gain of Channel 2 Preamplifier U320 is set higher when the CH 2 VOLTS/DIV switch is set to $2 \mathrm{mV}, 5 \mathrm{mV}$, $10 \mathrm{mV}, 100 \mathrm{mV}$, or 1 V/Div. At those VOLTS/DIV settings, the FASTCLAMP bit is set LO to turn on U420E. This turns FET Q419 on and places C520 in parallel with C522 thus increasing the size of the hold capacitance. This slows down the loop response at the "more sensitive" offset gain setting of the Channel 2 Preamplifier to prevent oscillation.

CLAMP SWITCHING. The Clamp Switching circuit enables and disables the effect of the Channel 2 Vertical Display Clamp. The clamp circuit operation may be switched to provide correct clamping for either inverted or noninverted video signals.

When display clamping of the Channel 2 signal is not enabled, BCLAMPENA will be set LO, turning U420D on. The HI on the collector of U420D turns on U410B, U410C, and Q420 and turns off Q710 via U710A. Any enabling currents to offset amplifiers U514 or U520 are shunted through U410B and U410C respectively. With FET Q420 on, the input to U710D will be grounded. This disables the

## Theory of Operation-2440 Service

Offset Buffer. With FET Q710 turned off via U710A, the offset line to the Channel 2 Vertical Preamplifier is open circuited, so no trace offsetting can occur.

When the Channel 2 Vertical Display Clamp is enabled, BCLAMPENA will be HI, turning U420D off. The LO on the collector of U420D turns Q420 off, enabling Offset Buffer Amplifier U710D to track the offset level output from the active Offset Amplifier, and the offset signal line to the Channel 2 Vertical Preamplifier is connected to the Offset Buffer by turning on Q710 via U710A.

Selection of either U514 or U520 is controlled by the CH2 INV signal and is dependent on the setting of the invert function in the associated COUPLING/INVERT menu. Since signal offsetting in the Channel 2 Preamplifier is done before the signal is inverted, offset voltages for inverted- and normal-signal displays must be of opposite polarity. Switching between these two offset amplifiers provides the required polarity change and allows the back porch of either display type to be clamped at the ground reference. Depending on the polarity of the CH 2 INV (Channel 2 Invert) signal, either U410E or U410D will be on, turning off either U410B or U410C. U410B will be off when CH2 INV is HI and U410C will be off when it is LO. Bias current from the Trigger Back-Porch Clamp circuit to the offset amplifiers (U514 and U520) is not shunted away by the "off" transistor, and the offset amplifier associated with the off transistor will be biased on during the sync pulse back-porch interval.

Biasing current to enable the selected Offset Amplifier is produced during the back-porch interval when U410A (in the Trigger Back-Porch Clamp circuit) is turned off. Bias current through either R411 or R410 (depending on whether U410B or U410C is off) is supplied via R403. The other offset amplifier will be disabled since its bias current is being shunted through the "on" transistor. The amount of bias current permitted by Transconductance Amplifier U504 to the "on" amplifier provides a signal to the Channel 2 Preamplifier (after buffering by U710D) that vertically offsets the displayed signal on Channel 2.

Since the offset voltage must be maintained throughout the entire horizontal interval, capacitor C522 (and C520 in parallel if FASTCLAMP is not enabled) serves as a hold capacitor between back-porch samples. At some VOLTS/DIV settings the Channel 2 Preamplifier is set for higher offset gain. Transistor Q419 will be turned on for those settings, placing C520 in parallel with C522 to slow down the loop response. This prevents oscillation in the Channel 2 Preamplifier at the more sensitive gain settings.

Offset Buffer Amplifier U710D applies this "stored" offset level to the Channel 2 Preamplifier (via Q710), shifting the back porch of the displayed signal to near the onscreen ground reference (as set with the Vertical POSITION control).

Any time the Phase-Locked Loop is not locked (indicating that a proper TV Trigger signal is not present), the Channel 2 Vertical Display Clamp is turned off via R328 by a HI TVCLAMP signal from the PLL Unlock Detector to prevent sending invalid offsets to the Channel 2 Preamplifier. During the unlocked state of the PLL, FET Q420 is biased on to pull the input to Offset Buffer Amplifier U710D to ground, and FET Q710 is biased off via U710A (acting as an inverter to the TVCLAMP signal) to open circuit the offset signal line to the Channel 2 Preamplifier.

## LOW-VOLTAGE POWER SUPPLY

The low voltages required by the scope are produced by a high-efficiency, switching power supply (diagram 22). This type of supply directly rectifies and stores charge from the ac line supply; then the stored charge is switched through a special transformer at a high rate, generating the various supply voltages.

## AC Power Input

LINE SWITCHING AND LINE RECTIFIER. Ac line voltages of either 115 V or 230 V may provide the primary power for the instrument, depending on the setting of the LINE VOLTAGE SELECTOR switch S1000 (located on the instrument rear panel). POWER Switch S1350 applies the selected line voltage to the power supply rectifier (CR510).

With the selector switch in the 115 V position, the rectifier and storage capacitors C105 and C305 operate as a full-wave voltage doubler. When operating in this configuration, each capacitor is charged on opposite half cycles of the ac input, and the voltages across the two capacitors in series approximates the peak-to-peak values of the source voltage. For 230 V operation, switch S1000 connects the rectifier as a conventional bridge rectifier. Both capacitors charge on both input half cycles, and the voltage across C105 and C305 in series approximates the peak value of the rectified source voltage. For either configuration (with proper line voltage), the dc voltage supplied to the power supply inverter is the same.

SURGE PROTECTION. Thermistors RT717 and RT805 limit the surge current when the power supply is first turned on. As current warms the thermistors, their resistances decrease and have little effect on circuit operation.

Spark-gap electrodes E609 and E616 are surge voltage protectors. If excessive source voltage is applied to the instrument, the spark-gaps conduct, and the extra current quickly exceeds the rating of F1000. The fuse then opens to protect the power supply.

EMI FILTER. A sealed line filter, FL1000, is packaged with the line cord connector. It is effective in reducing noise with frequency components at and beyond 1 MHz . A differential mode filter is made up of R809, C816, R815, L715, L709, R808, R713, and C706 and is effective in reducing switch-mode noise up to 1 MHz . Resistor R1000 ensures that the capacitors in the line filter become discharged a short time after removal of the line cord so as to not present a shock hazard at the line cord connector. A combination common-mode and differential-mode filter is made up of T117, R217, R117, C218, C225, and C328. The line-rectification energy-storage capacitors (C105 and C305) also aid in the operation of this filter circuit. Resistors R410 and R401 bleed charge from the line-rectification capacitors to guarantee that they are discharged within a definite time after power is removed (turned off).

THERMAL SWITCH. Thermal Switch S1020 opens if the temperature of the power supply heatsink becomes abnormally high. High temperatures may indicate blocked ventilation holes or failed components. Opening the switch removes ac-line power from the supply to prevent any further damage from occurring. When the heatsink cools to its normal limits, the switch recloses. Opening of S1020 immediately shuts off the power supply, and the System $\mu \mathrm{P}$ does not perform its normal shutdown routine. Waveforms and front-panel settings are not saved on a thermal shutdown.

## Control Power Supply

The control circuits for the power supply require a separate power supply circuit to operate. This independent power source is made up of Q148, Q240, Q836, and associated components.

Initially, when instrument power is applied, the positive plate of capacitor C244 is charged toward the value of the positive rectified-line voltage through R223. The voltage at the base of Q148 follows at a level determined by the voltage divider composed of R436, R244, CR239, R240, R640, Q836 and the load resistance placed on the supply. When the voltage across C244 reaches about +27 V , the base voltage of Q148 reaches +12.6 V and Q148 turns on, saturating Q240. The +27 V on the emitter of Q240 appears at its collector and establishes the positive volt-
age supply for the +12 V regulator stage formed by Q836, VR929, R240, and R640. With Q240 on, R244 is placed in parallel with R436 and both Q148 and Q240 remain saturated.

The +27 V level begins to drain down as the +12 V Regulator draws charge from C244. If the main power supply doesn't start (and thus recharge C244 via T335 and CR245) by the time the voltage across C244 reaches about +14 V , Q240 turns off. With Q240 off, resistor R244 pulls the base of Q148 low and turns it off also. (Capacitor C244 would only discharge low enough to turn off the transistors under a fault condition.) In this event, C 244 would then charge again to +27 V , and the start sequence would repeat. Normally, the main power converter is delivering adequate power before the +14 V level is reached, and the current drawn through T335 via Q421 and Q423 induces a current in the secondary winding of T335 that charges C244 positive via diode CR245. The turns ratio of T335 sets the secondary voltage to approximately +17 V and, as long as the supply is being properly regulated, C244 is charged to that level and held there.

## Power Conversion

The power converter consists of a buck-type switching Preregulator, producing width-regulated voltage pulses that are filtered to produce a preregulated dc current, and an Inverter stage that chops this preregulated current into ac to drive a power transformer. The transformer has output windings that provide multiple unregulated dc voltages after rectification has taken place. The main Preregulator components are Q421, Q423, CR426, C328, T335, T620, and U233. The fundamental Inverter components are Q521, Q721, T639, and U829B (see Figure 3-15).

PREREGULATOR. The Preregulator control circuit monitors the drive voltage reflected from the secondary to the primary of the inverter output transformer T639 and holds it at the level that produces proper supply voltages at each of the secondary windings.

The Preregulator control circuit consists primarily of control IC U233, gate drive transformer T620, and the associated bias and feedback circuit elements. The voltage at the primary center tap of T639 is attenuated and applied to the voltage-sense input of control IC U233. This IC varies the "on time" of a series switch, depending on whether the sensed voltage is too high or too low. Transistors Q421 and Q423 form this "series switch," and are each active during alternate switching cycles. The ontime duty cycle of the series switch is inversely proportional to the rectified line voltage on C328. In normal operation, the series switch is on about one-half of the time. When the series switch is off, current to T639 is through CR426.


Figure 3-15. PWM Regulator and Inverter.

PREREGULATOR START-UP. As the supply for the Preregulator control IC is established, an internal oscillator begins to run. The oscillator generates a repetitive triangular wave (as shown in Figure 3-16) at a frequency determined primarily by R228 and C227 (with R227 having a minor effect since it controls the discharge time of timing capacitor C227).

As the control power supply turns on, a $50 \mu \mathrm{~A}$ current source internal to U233 begins to charge capacitor C128 positive. This charging level, applied to one of the negative inputs of the PWM comparator, allows drive pulses of greater and greater duty cycle to be generated. These pulses drive the series switching transistors (Q421 and Q423), and their slow progression from narrow to wide causes the various secondary supplies to gradually build up to their final operating levels. This slow bulldup prevents a turn-on current surge that would cause the current-limit circuitry to shut down the supply.

PREREGULATION. Once the initial charging at powerup is accomplished (as just described), the voltage-sensing circuitry begins controlling the Inverter switching action. The voltage level at the primary center tap of T639 is divided by sense string R146-R144, and the resulting voltage is applied to the error amplifier internal to U233 at pin 1. The +5.1 V reference generated by $U 233$ is applied to pin 2 of U233, the other input of the error amplifier. If the sensed level at pin 1 is lower than the reference level at pin 2 (as it always is for the first few switching cycles), the output of the error amplifier is high. This high level is applied to a negative input of the PWM comparator; the other negative input is applied from the soft-start capacitor (described previously).

The lower of the two negative input levels determines the actual negative comparison point of the PWM comparator; and this level determines the point at which the positive-going ramp, applied to the positive input, switches the PWM comparator to initiate the off state of the PWM switch. The PWM series switch is turned on at the beginning of each clock cycle; turn-off occurs when the positive-going ramp crosses the threshold level of the PWM comparator. The lower the level at the controlling (negative) input, the shorter the PWM switch "on time." Depending on the output level sensed, the duty cycle of the drive signal changes (sensed level rises or falls with respect to the triangular waveform applied to the positive PWM comparator input) to hold the secondary supplies at their proper levels.

Optoisolator U155 and resistor R143 form a control network that allows a voltage sensed at the FEEDBACK input to slightly alter the voltage-sense reference applied to pin 1 of U233. The FEEDBACK signal is generated by
the +5 V Inverter Feedback amplifier (U189, diagram 23) and is directly related to the level of the +5 VD supply line. If the FEEDBACK signal goes above its nominal level ( +5 VD is too low), base drive to the shunt transistor (in optoisolator U155) increases. This increase causes additional current to be shunted around R144 (via R143 and phototransistor of U155) and changes the ratio of the sensing divider. The voltage at the center tap of T639 must increase to balance out the changed sense ratio and maintain balance in the error amplifier. Since the output of the error amplifier controls the current to the primary winding of the output transformer, and since the error amplifier sensing depends on a balanced condition, the voltage at the transformer primary increases.

With a higher current applied to the transformer primary, higher voltages appear across the secondary windings of T639 with each cycle. This causes the secondary voltages to return to their nominal levels. As the $+5 \mathrm{~V}_{\mathrm{D}}$ line returns to its nominal level, base drive to the shunt transistor stabilizes at a level that keeps the sensed $+5 \mathrm{~V}_{\mathrm{D}}$ level in regulation. Should the FEEDBACK signal level tend too high, opposite control responses occur. Further information about the FEEDBACK signal is given in the +5 V Inverter Feedback description.

INVERTER. The Inverter circuit alternately switches current through each leg of the primary winding of output transformer T639. The circuit is made up of Q521, Q721, U840D, U829B, and associated components.

A clock pulse from U233 is applied to a TTL-CMOS level shifting buffer (U840D) at the beginning of every switching cycle. The level-shifted clock pulse at the output of U840 clocks U829B, a CMOS D-type flip-flop (configured to toggle with each clock). The Inverter switch transistors, Q521 and Q721, are aiternately turned on and off by the flip-flop outputs and are connected to opposite ends of the primary winding of the output transformer. Driving the inverter switches in alternate fashion produces ac currents in the secondary windings of the output transformer that are rectified, providing the various unregulated dc supply voltages.

## Primary Fault Sensing

Primary current, primary regulated voltage, and primary unregulated voltage are monitored by circuitry to prevent catastrophic failure. Should conditions arise that cause an excessive primary current or an excessive primary regulated voltage, limiting occurs. The excessive primary current and primary regulated voltage functions share much common circuitry, while the low unregulated primary voltage circuitry is entirely independent of the first two fault-sensing circuits.


Figure 3-16. PWM switching waveforms.

PRIMARY OVER-CURRENT SENSING. The primary current of T639 through R727 produces a voltage signal that is filtered by R728 and C728 to remove highfrequency switching spikes. The filtered signal is applied to the inverting input of U840C. The noninverting input of the comparator is set at a level defined by the $+5,1 \mathrm{~V}$ reference from U233 and voltage divider R939-R836. If an excessive-current condition exists (to the point that the inverting input of U840C goes more positive than the noninverting input), the comparator output goes low. The open-collector output of the comparator is "wire-ORed" with the open-collector output of the regulated primary over-voltage comparator (U840B) and drives U840A, connected as an inverting buffer. Buffer U840A drives the clock input of a CMOS flip-flop in U829, configured as a monostable flip-flop, used to shut down supply operation.

PRIMARY OVER-VOLTAGE SENSING. The regulated primary voltage is sensed by the voltage divider R129R128, with C528 providing low-pass filtering to remove high-frequency switching spikes. The attenuated signal is applied to comparator U840B at the inverting input, while the noninverting input is connected to the +5.1 V reference from U233. Should the regulated primary voltage become high enough to raise the inverting input of the comparator more positive than the noninverting input, the comparator output goes to a low level. As previously stated, the output of this comparator is wire-ORed to the output of U840C and drives an inverting clock buffer U840A. This buffer in turn drives the clock input of the monostable flip-flop circuit used to shut down supply operation.

SHUTDOWN TIMER. The Shutdown Timer ensures that the preregulator series switch remains off long enough for energy stored in C128 (the soft-start capacitor) and C244 (the Control Power Supply energy-storage capacitor) to drain down via normal circuit loading should an overcurrent or over-voltage fault occur. Shutdown of the series switch (Q421 and Q423) occurs when the S/D (shutdown) input (pin 10) of U233 goes high. The Shutdown Timer, made up of U829A, R824, C829, R932, CR730, and CR824, controls this input.

Prior to being clocked, U829A (configured as a monostable flip-flop) is in a reset state with its Q output set low. This is the normal operating mode and allows the series switch to be controlled by the regulating functions of U233. Capacitor C829 charges to the Control Power Supply voltage via R824 and CR824 (diode CR824 shunts R932 when charging C829 to provide a relatively fast charging path). When the flip-flop is clocked (indicating a fault-sense from the voltage- or current-sense circuits), the $Q$ output goes high and C829 begins to discharge. With $Q$ high, CR824 becomes reverse biased so that discharge of C829 is through R932, providing a relatively slow discharge compared to the charging time. This ensures
that the Q output of U829A is held high long enough for soft-start capacitor C128 and Control Power Supply capacitor C244 to fully discharge.

The high $Q$ output of U829A, connected to the shutdown input to U233, turns off the PWM switch (Q421 and Q423) immediately and keeps it off until Q returns low (when the Control Power Supply decays and turns U829 off). However, the PWM clock continues to run and the Inverter switches (Q521 and Q721) continue to operate. Since the PWM switch is not operating, energy is not transferred to the Control Power Supply via T335, and C244 discharges below the minimum voltage level required by the Control Power Supply circuit (through the normal circuit load). When this minimum level is reached, the Control Power Supply regulator disconnects from C244, interrupting the power to the control circuitry and stopping the Inverter switches.

Monostable U829A is designed to remain active long enough for the Control Power supply to decay and disconnect. The disconnect level is approximately half of the Control Power Supply voltage and, once disconnected, supply voltage is reestablished in 0.5 to 2 seconds. The time it takes C244 to charge from the "disconnect threshold" to the Control Power Supply "turn-on threshold" is the dominate factor in determining the power supply restarting time when recovering from an over-current or overvoltage fault condition.

Capacitor C829 is once again charged through R824 and CR824 with a relatively short time constant, allowing U829A to be triggered again (if the fault persists) by the time the Control Power Supply restarts.

LINE UP. The Line Up circuit, composed of U834B, U265, and associated components, senses the level of the rectified line voltage and relays its status through the PWRUP circuit to the System $\mu \mathrm{P}$. The signal from voltage divider R325-R835 is low-pass filtered by C835 and is applied to the inverting input of comparator U834B. The noninverting input of the comparator is referenced to the +5.1 V reference from U233. The output of the comparator drives the light-emitting diode of optoisolator U265, so whenever the rectified line-input voltage is below the normal operating level (approximately +178 V ), the lightemitting diode (LED) is off. With the LED off, the output phototransistor of U265 is biased off.

At instrument turn-on, after the rectified line voltage comes up, the control power supply begins supplying power to the control circuitry. At that time, the output of comparator U834 goes LO at pin 7 to turn on the LED in optoisolator U265. This action biases on the output transistor of the optoisolator and switches the LINE UP
signal HI. Through the PWRUP signal circuitry, a HI LINE UP signal tells the System $\mu \mathrm{P}$ that ample line voltage is available for normal instrument operation.

When instrument power is turned off, the rectified line voltage begins dropping. At about 178 V , comparator U834 switches off the LED in U264, and the LINE UP signal goes LO. A LO output tells the System $\mu \mathrm{P}$ that power is dropping, and the $\mu \mathrm{P}$ begins shutting the instrument down in an orderly fashion before the secondary voltages go out of regulation.

## Line Trigger

The Line Trigger circuit, made up of T415, U170A, and the associated components, provides a representation of the input line signal to the Trigger stage that is isolated from the power-line environment.

Since resistors R516 and R518 are large compared to the impedance of the primary winding in T415, the transformer operates in a current-driven mode. The secondary winding of T415 is connected to a transresistance amplifier stage consisting of U170A, C483, and R483. This amplifier presents a very low impedance to the output of the transformer and maintains the integrity of the line voltage signal representation. Capacitor C483 provides a negative-feedback path to high frequencies (relative to 60 Hz ) and reduces noise on the line-frequency signal. The output of the transresistance amplifier drives the oscilloscope trigger circuitry.

## Rectifiers

The Rectifiers convert the alternating currents from the secondary windings of the Inverter output transformer to the various unregulated dc voltages required by the instrument. Rectification is done by conventional diode rectifier circuits, and filtering is done by conventional LC networks.

## LOW-VOLTAGE REGULATORS

The Low-Voltage Regulators (diagram 23) remove ac voltage noise and ripple from the various unregulated dc supply voltages. Each regulator output is automatically current limited if the output current exceeds the requirements of a normally functioning instrument. This limiting prevents any further component damage.

## +10 V and -5 V References

Each of the power supply regulators controls its respective output by comparing the output voltage to a known
reference level. In order to maintain a stable supply voltage, the reference voltage must itself be highly stable. The circuit composed of U180, U170B, U900, and associated components produces the two reference levels used by the regulator circuits.

Resistor R556 and capacitor C664 form an RC filter network that smooths the unregulated $+15 \mathrm{~V}_{\mathrm{A}}$ supply before it is applied to voltage-reference IC U180. The +10 volt output from pin 6 of U180 feeds a low-pass filter composed of R900 and C900. The output of this filter in turn feeds unity-gain buffer amplifier U900, the output of which is the source of the +10 V reference used by the various positive regulators. Low-pass filter R900-C900 provides filtering for the IC voltage reference and provides for a well-defined voltage rise of the $+10 \mathrm{~V}_{\text {REF }}$ voltage at power-up.

Operational amplifier U170B and its associated components make up a -5 V Reference circuit used as the reference for the negative regulators. It is configured as an inverting amplifier with a gain of $1 / 2$ and converts the $+10 \mathrm{~V}_{\text {REF }}$ input to a precision $-5 \mathrm{~V}_{\text {REF }}$ output.

## +15 V Regulator

The +15 V Regulator uses three-terminal regulator U579 and operational amplifier U570A (arranged as the voltage sensor) to achieve regulation of the +15 V supply). The three-terminal regulator holds its output voltage on pin 2 at 1.25 V more positive than the reference input level applied to pin 1. The voltage at the reference pin is established by current in diode CR575 and is controlled by voltage sensor U570A.

Resistors R576 and R575 at the regulator output divide the +15 V level down for comparison to the +10 V reference applied to pin 3 of operational amplifier U570A. At initial power up, when the input voltage at pin 2 (from the divider) is lower than the +10 V reference, the output of amplifier U570A is high, and the output voltage is allowed to rise. As the regulator output reaches +15 V , the amplifier begins sinking current away from the reference pin of the three-terminal regulator via diode CR575. This sets the voltage on the reference pin at its nominal level and holds the output at +15 volts.

Current limiting for the +15 V supply is provided by the internal circuitry of the three-terminal regulator. Diodes CR576 and CR583 protect U570A from transient voltage reversals.

## +8V Regulator

The +8 V Regulator is composed of Q465, Q479, U470A, U470B, and the associated components. The circuit regulates the voltage and limits the supply current.

Initially, as power is applied, the voltage at pin 6 of U470B via R476 is lower than the +8 V reference level applied to pin 5 via divider R465 and R466. The output of U470B is forced HI , reverse biasing diode CR466. With CR466 (and CR465) off, all the current through R565 is supplied as base current to Q465, turning it on. This turns on the pass transistor Q479 at maximum current. This current charges up the various loads on the supply line and the output level moves positive.

As the regulator output rises toward +8 V , this positive-going voltage is applied to the inverting input of U470B through R476. When the output voltage reaches +8 V , the inverting input equals the reference at the noninverting input set by R465 and R466. Then, the output at pin 7 of U470B goes negative, forward biasing diode CR466 and shunting base-drive current away from Q465. This reduces the currents through Q465 and Q479 to levels that maintain a +8 V output. Since base drive source for Q465 is the +15 V supply, via R565, proper relative polarity between the two supplies is assured (preventing component damage in case of a failure on the +15 V supply line).

The over-current limiting circuit is of foldback design and is performed by operational amplifier U470A and its associated components. Under normal current demand conditions, the output of U470A is HI, keeping diode CR465 reverse biased. If the regulator output current exceeds approximately 1.3 A (as it might if a component fails), the voltage drop across R473 (added onto the +8 V output voltage) causes the inverting input of U470A to exceed the +8 V level at the noninverting input, and the output at pin 1 will go LO. This forward biases diode CR465 and reduces the forward bias on Q465 and thereby decreases the bias current to Q479. This in turn reduces the regulator output current through Q479 to decrease the output voltage. As the output voltage drops (applied to U470A pin 3), the output current required to cause limiting also decreases, causing both voltage and current to drop to low values as Q465 becomes biased off.

Pin 2 of U470A is pulled down through R477 to the $-8 \mathrm{~V}_{\mathrm{A}}$ supply so that the output of the foldback circuit becomes immediately HI at power-on. This initial HI holds CR465 biased off thereby preventing a false overcurrent sense and subsequent latchup at start-up as the +8 V regulated output seen on pin 3 of U470A rises from zero volts to its normal operating level.

## +5 V Regulator

Regulation of the +5 V supply is provided by a circuit similar to that of the +8 V Regulator. As long as the relative polarity between the +8 V supply and the +5 V supply is maintained, base drive to Q870 is supplied through R864. The current through Q870 provides base drive for the series-pass transistor Q879.

When voltage-sense amplifier U870B detects that the +5 V remote-sense voltage has reached +5 V , it begins shunting base-drive current away from Q870 via diode CR866 and holds the output voltage constant.

Current limiting for the +5 V supply is done by U870A and associated components. Under normal current demand conditions, the output of U870A is high and diode CR865 is reverse biased. However, should the current through current-sense resistor R873 reach approximately 3 amperes, the voltage developed across R873 (added to the regulated +5 V output) raises the voltage at pin 2 of U870A (via divider R876 and R875) to a level equal to that at pin 3. This causes the output of U870A to go low, forward biasing CR865. Base drive current is then shunted away from Q870, and the output current in Q879 is reduced. Resistor R874 allows the supply to maintain regulation with the remote-sense line disconnected. Resistors R885 and R886 provide enough initial current to the load to prevent an excessive-current latchup of U470A as the power comes up.

## - 15 V Regulator

Operation of the -15 V Regulator, composed of U679, U570B and their associated components, is similar to that of the +15 V Regulator already described. The regulator is referenced to -5 V to allow sensing of the negative output level. Zener diode VR870 allows operational amplifier U570B to operate in its active region. Capacitor C873 is a speed-up capacitor that allows the regulator to respond more quickly to current surges and other transients and provides filtering of zener noise produced by VR870.

## -8 V Regulator

Operation of the -8 V regulator is nearly identical to that of the $+8 \vee$ Regulator, except that it is referenced to -5 V to allow sensing of negative voltages. Zener diode VR380 allows operational amplifiers U270A and U270B to operate in their linear regions.

The $-8 \vee$ Sense input provides for remote sensing of the supply level on the Main board where regulation is the most critical. Since the -8 V level is remotely sensed, the IR drop caused by the impedance in the supply bus lines
going to the main board and a small series resistor in the line (R121 on the Main board) causes the actual output level from the supply regulator to be closer to -8.4 V . (This is the voltage actually required by some of the -8 V load circuits.) Resistor R388 allows the supply to maintain regulation with the remote sense line disconnected. Current limiting of the combined -8 V and -8.3 V supplies occurs at about 3 amperes.

## - 5 V Regulator

Operation of the -5 V Regulator is similar to that of the +5 V Regulator. Current limiting of the -5 V supply occurs at about 3.1 amperes.

## +5 V Inverter Feedback

Operational amplifier U189 and associated components are configured as a frequency-compensated voltagesensing network. The circuit monitors the +5 V digital power supply line from the rectifiers and provides feedback to the Preregulator Control IC (U233) via optoisolator U155 (both on diagram 22). The feedback is used to trim the $+5 \mathrm{~V}_{\mathrm{D}}$ level by controlling the Preregulator. The FEEDBACK signal slightly varies the voltage to the Inverter output transformer and holds the output of the 5 V secondary windings at an optimum level. Output levels of the other secondary windings are related by turns ratio to the $+5 \mathrm{~V}_{0}$ level and are also held at their optimum levels. This technique minimizes power losses in the seriespass transistors and increases regulator reliability.

## Power-Up

The Power-Up circuit, composed of U189A, Q295 and the associated components, provides buffering and level shifting of the LINE UP signal to the System Processor.

Operational amplifier U189A is configured as a comparator referenced to $+10 \mathrm{~V}_{\text {REF }}$. When adequate powerline input voltage is available, the LINE UP signal will be HI. The output of the comparator will be LO, turning off transistor Q295. This results in a HI PWRUP signal to the System $\mu \mathrm{P}$, indicating that the power supplies are stable. When adequate power-line voltage is not available, the LINE UP signal from the Preregulator circuit goes LO, the output level of U189A goes HI and turns Q295 on, resulting in a LO PWRUP signal to the System $\mu \mathrm{P}$. This indicates that the various supply voltages may go out of regulation in about 10 ms .

Capacitor C195 provides a negative-feedback path for high-frequency signals and stabilizes operation of U189A.

## DC-OK Sense

The output of the DC-OK Sense circuit is checked by the System Processor after it receives the PWR UP signal to verify that power supply voltages are within tolerance.

By itself, the resistive summing network made up of R794, R795, R797, R686, R688 and R796 would produce a voltage near zero volts if all supplies were within tolerance. This voltage may vary $\pm 0.19 \mathrm{~V}$, depending on slight variations in the individual supply output levels. The current in resistor R396 is, however, added into the summing node and shifts its operating point approximately 0.19 V positive.

The resulting voltage is compared to ground by comparator U395B and to +0.37 V by comparator U395A, establishing the tolerance window. Both open-collector outputs of the comparator are off, and the DCOK signal is HI , as long as the summing-node voltage falis within this window. Should the summing-node voltage exceed either limit, the associated comparator turns on its output transistor and pulls the DCOK signal LO, indicating that at least one of the power supplies is not operating properly.

# PERFORMANCE CHECK AND FUNCTIONAL VERIFICATION PROCEDURE 

NOTE<br>Perform the SELF-CAL procedure before doing this procedure. Refer to the Self Calibration procedure in Section 5 of this manual. A demonstration procedure of SELF-CAL is given in the 2440 Operators manual in Section 2, and a detailed description of the built-in calibration and diagnostics is given in Appendix A.

## INTRODUCTION

Use this procedure to verify proper operation of instrument controls and to check the instrument's performance against the requirements listed in Section 1. This procedure verifies instrument function and may be used to determine need for readjustment (all internal adjustments should be referred to qualified service personnel). These checks may also be used as an acceptance test.

Do not remove this instrument's cabinet to perform this procedure. All checks are made using the operator-accessible front- and rear-panel controls and connectors.

Within the procedure, there are steps that verify proper operation of instrument controls or functions that are not specified as Performance Requirements in Section 1. These steps use the word "VERIFY" when indicating the characteristic for which to test. The functions tested by these steps ARE NOT Performance Requirements and should not be interpreted as such. Steps to check Performance Requirements use the word "CHECK," rather than "VERIFY."

## PREPARATION

THIS PROCEDURE ASSUMES THAT OPERATORS ARE SUFFICIENTLY ACQUAINTED WITH INSTRUMENT OPERATION TO SET IT UP AS DIRECTED IN THE PROCEDURE STEPS. Familiarization procedures are found in Sections 1 and 2 of the operators manual included with this instrument. Section 5 of that manual is a reference for operation of all front- and rear-panel controls and connectors. Refer to those sections of the Operators manual if instructions for
obtaining the various operation modes of this instrument are needed.

Test equipment items 1 through 28 listed in Table 4-1 are required to perform this procedure. The specific pieces of equipment required to perform the checks within each subsection are listed at the beginning of that subsection. The item numbers in parenthesis next to each piece of equipment refer to the numbered equipment list of Table 4-1. Item 25 and 26 is used for instrument calibration only (see Adjustment Procedure-Section 5).

Before performing this procedure, ensure that the LINE VOLTAGE SELECTOR switch is set for the AC power source being used (see Section 2, Preparation for Use, in this manual). Connect the instrument to be checked and the test equipment to an appropriate power source. Turn the instrument on and ensure that no error message is displayed on the CRT. If an error message is present, have the instrument repaired by a qualified service technician before performing this procedure.

This procedure is divided into subsections (VERTICAL SYSTEM, TRIGGERING SYSTEM, etc.), and further into steps (Verify CH 1 and $\mathrm{CH} 250 \Omega$ Overload Protection, etc.). This arrangement allows verification of the functionality of the instrument's individual sections, as well as its conformance to individual specifications, without requiring performance of the entire procedure. Any number of steps (in any order) can be performed as long as ALL the parts of a step are performed in sequence and in their entirety.

Table 4-1
Test Equipment

| Description | Minimum Specification | Purpose | Examples of Suitable Test Equipment |
| :---: | :---: | :---: | :---: |
| 1. Leveled Sine-Wave Generator (Primary) | Frequency: 250 kHz to above 250 MHz . Output amplitude: variable from 10 mV to 5 V p -p. Output impedance: $50 \Omega$. Reference frequency: 50 kHz . Amplitude accuracy: constant within $3 \%$ of reference frequency as output frequency changes. | Vertical, horizontal, and triggering checks and adjustments. | TEKTRONIX SG 503 Leveled Sine Wave Generator. ${ }^{\text {a }}$ |
| 2. Leveled Sine-Wave Generator (Secondary) | Frequency: 245 kHz to above 500 MHz . Output amplitude: variable from 500 mV to 4 V p-p. Reference frequency: 6 MHz . Amplitude accuracy (at reference): constant within 3\% of indicated amplitude. | Bandwidth and transient response checks and adjustments. | TEKTRONIX SG 504 Leveled Sine-Wave Generator with Leveling Head. ${ }^{\text {a }}$ |
| 3. Calibration Generator | Standard-amplitude signal levels: 5 mV to 50 V . Accuracy: $\pm 0.25 \%, \pm 1 \mu \mathrm{~V}$. Repetition Rate: 1 kHz . High-amplitude signal levels: 1 V to 60 V . Repetition rate: $1 \mathbf{k H z}$. Fast-rise signal level: 100 mV to 1 V . Repetition rate: 100 Hz to 100 kHz . Rise time: 1 ns or less. Flatness: $\pm 0.5 \%$. | Signal source for gain. | TEKTRONIX PG 506 Calibration Generator. ${ }^{\text {a }}$ |
| 4. Time-Mark generator | Marker outputs: 10 ns to 0.5 s . Marker accuracy: $\pm 0.0002 \%$. Trigger output: 1 ms to $0.1 \mu \mathrm{~s}$, time-coincident with markers. | Horizontal checks. | TEKTRONIX TG 501 Time-Mark Generator. ${ }^{\text {a }}$ |
| 5. Function Generator | Range: less than 1 Hz to 80 kHz ; sinusoidal output; amplitude variable to greater than $10 \mathrm{Vp}-\mathrm{p}$ open circuit with dc offset adjust. | Low-frequency checks. | TEKTRONIX FG 502 Function Generator, ${ }^{\text {a }}$ |
| 6. Power Supply | Range: 0 to 20 VDC. | $50 \Omega$ Overload verification. | TEKTRONIX PS 503A Power Supply. ${ }^{\text {a }}$ |
| 7. Digital Voltmeter (DMM) | Range: 0 to 140 V . Dc voltage accuracy: $\pm 0.15 \% .41 / 2$ digit display. | Sequencer Input/Outputs Verification. | TEKTRONIX DM 501A Digital Multimeter. ${ }^{\text {a }}$ |
| 8. GPIB Controller ${ }^{\text {b }}$ | Conform to IEEE-488 (1978) standard. | Check GPIB operation. |  |
| 9. GPIB Cable | Conform to IEEE-488 (1978) standard. | Check GPIB operation. | Tektronix Part Number 012-0630-03. |
| 10. Coaxial Cable (2 required) | Impedance: $50 \Omega$. Length 43 in. Connectors: BNC. | Signal interconnection. | Tektronix Part Number 012-0057-01. |

${ }^{3}$ Requires a TM 500-Series power-module mainframe.
${ }^{\text {b }}$ Due to the variety of equipment capable of controlling the GPIB, a specific Controller is not specified.

Table 4-1
Test Equipment (cont)

| Description | Minimum Specification | Purpose | Examples of Sultable Test Equipment |
| :---: | :---: | :---: | :---: |
| 11. Precision Coaxial Cable | Impedance: $50 \Omega$. Length: 36 in . Connectors: BNC. | Used with Calibration Generator. | Tektronix Part Number 012-0482-00. |
| 12. Termination | Impedance: $50 \Omega$. Connectors: BNC. | Signal termination. | Tektronix Part Number 011-0049-01. |
| 13. 10X Attenuator (2 required) | Ratio: 10X. Impedance: $50 \Omega$. Connectors: BNC. | Vertical and triggering checks. | Tektronix Part Number 011-0059-02. |
| 14. $5 \times$ Attenuator | Ratio: 5X. Impedance: $50 \Omega$. Connectors: BNC. | Vertical and triggering checks. | Tektronix Part Number 011-0060-02. |
| 15. 2 X Attenuator | Ratio: 2X. Impedance: $50 \Omega$. Connectors: BNC. | External triggering checks. | Tektronix Part Number 011-0069-02. |
| 16. 10X Standard Accessory Probe (supplied with instrument) | DC to 250 MHz probe. | Signal input connector. | TEKTRONIX P6136. |
| 17. 1X Probe | DC to 34 MHz probe. | Signal input connector. | Tektronix Part Number 010-6101-03. P6101A. |
| 18. Dual-Input Coupler | Connectors: BNC female-to-dual-BNC male. | Signal interconnection. | Tektronix Part Number 067-0525-02. |
| 19. BNC Female-to-Dual Adapter (2 required) | Connectors: BNC female-to-dual-banana male. | Signal interconnection. | Tektronix Part Number 103-0090-00. |
| 20. Sine-Wave Oscillator | Frequency: adjustable to 60 Hz . Amplitude: adjustable to 3 V p-p into $75 \Omega$. | Check TV triggers for back-porch clamp operation. | TEKTRONIX SG 502 Oscillator. ${ }^{\text {a }}$ |
| 21. Pulse Generator | Period Range: 1 ms to $2 \mu \mathrm{~s}$. Pulse Range: 0.5 ms to $1 \mu \mathrm{~s}$. Amplitude variable from -5 to +5 V , independent pulse top and pulse bottom. | Check Auto Setup. | TEKTRONIX PG 502 Pulse Generator. ${ }^{2}$ |
| 22. Sync and Linearity Test Generator. | Conforms to TV System requirements. | Check TV triggers for back-porch clamp operation. | TEKTRONIX TSG-170A Television Generator. |
| 23. Coaxial Cable (2 required) | Impedance: $75 \Omega$. Length: 42 in. Connectors: BNC. | Signal interconnection. | Tektronix Part Number 012-0074-00. |
| 24. Termination | Impedance: $75 \Omega$. Connectors: BNC. | Signal termination. | Tektronix Part Number 011-0055-00. |
| 25. Alignment Tool | Length: 1 in. shaft. Bit size: 3/32 in. Low capacitance; insulated. | Adjust variable capacitors and resistors. | Tektronix Part Number 003-0675-00. |
| 26. Normalizer | Input Resistance: 1 M $\Omega$. Input Capacitance: 15 pF . | Check input capacitance. | Tektronix Part Number 067-0537-00. |
| 27. Tunnel-Diode Pulser | Rise time: 125 ps or less | Adjust transient response | Tektronix Part Number 067-0681-01. |
| 28. 2.5X Attenuator | Ratio: 2.5X. Impedance: $50 \Omega$. Connectors: BNC. | Adjust transient response | Tektronix Part Number 067-0076-01. |

[^7]
## Performance Check and Functional Verification Procedure

 2440 ServiceBEFORE PERFORMING THE REMAINDER OF THIS PROCEDURE, DO THE "INITIAL SETUP" AT THE BEGINNING OF THE PROCEDURE STEPS. The Initial Setup is a procedure for setting up and storing a complete front-panel setup that can be recalled. When performing almost any step in this procedure, the first part (part a) requires that this stored front-panel setup be recalled and specifies the changes (if any) to be made to that setup. Make ONLY those changes specified; do not change any other control settings (including vertical and horizontal position settings).

## NOTE

This instrument must be powered up for at least 20 minutes before performance requirements can be checked.
"Select" means to press the appropriate front pane button to obtain the stipulated menu on the CRT screen. "Set," when preceded by a menu selection, indicates the stipulated menu function should be turned on or off by pressing the appropriate menu button. The function will appear underlined in the menu when turned on, not underlined when turned off. Control settings not Ilsted do not affect the procedure.

## INITIAL SETUP

a. Select PRGM.

Push: INIT PANEL
Select: TRIGGER MODE
Set: AUTO On
Select: VERTICAL MODE
Set: CH 2 On
Select: CH 1 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF ON
Select: CH 2 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF ON
Set: A SEC/DIV $500 \mu \mathrm{~s}$
b. Select the $A / B$ TRIG button to enable the B Trigger System.
C. Select TRIGGER MODE to display B TRIG mode menu and set TRIG AFTER on. Select the A/B TRIG button to return to the A Trigger System.
d. Select STORAGE ACQUIRE and set REPET ON|OFF ON. Repeatedly press the menu button labeled AVG until a "16" appears above the AVG. Repeatedly press the ENVELOPE button until a " 16 " appears above ENVELOPE. Set NORMAL back on.
e. Select PRGM to display the AUTOSTEP SEQUENCER menu. Press SAVE in the main menu to display the SAVE Sequence menu.
f. Use the arrows under ROLL-CHARS to create a label (use FPNL) for the front-panel setup outlined here in steps 1-3

1. Select the first character for the label. Use the arrow-labeled buttons to select the first letter for the sequence label. Press the $\downarrow$ or $\uparrow$ button to step through the alphabet and digits ( $0-9$ ). Holding down the buttons moves through the characters continuously; a single press moves forward or backward one character. (There is a "blank space" character between the digit 9 and letter A.)
2. When the letter for the first character of the label is displayed, push CURSOR $<>$ to move to the next character. Repeat step 1 to select the letter for the next character of the label.
3. Repeat last step until "FPNL" is spelled out. (Any character can be returned to for editing by continually pushing the CURSOR $<>$ button, since it reverses the selection order after the first and sixth character is selected.)
g. Push the menu button labeled SAVE when the label is complete.

## NOTE

In part $h$, Trigger Mode is set back to AUTO LEVEL. (AUTO LEVEL was initially turned off to make the front-panel changes in parts a through $g$ faster to set.) Throughout the remainder of this Performance Check procedure, the scope is switched to AUTO LEVEL when the initial setup is recalled, providing automatic triggering of displays. If preferred, you can switch to AUTO and use INIT @50\% and/or the TRIGGER LEVEL control to trigger manually. When AUTO is the required mode for a procedure (such as for checking the Trigger Level Readout accuracy, etc.) AUTO is specified in that procedure.

Occasionally, AUTO LEVEL may fail to find a stable trigger if you connect the triggering signal to the front panel between auto-level cycles; if so, push INIT @50\% to obtain the triggered display.
h. Pushing the menu button SAVE saves the label for the sequence and displays the message "SETUP CONTROLS, PUSH PRGM TO CONTINUE." Select TRIGGER MODE and set AUTO LEVEL on. DO NOT CHANGE ANY OTHER FRONT-PANEL SETTINGS AT THIS TIME. Instead, save the current front-panel setup by doing the following:

1. Push the front-panel button PRGM. This will bring up the action selection menu.
2. Do not select any actions. Push the menu button labeled SAVE SEQ to store the sequence under the label "FPNL".
i. Later in this procedure, when instructed to recall the "Initial Front-Panel Setup", perform the following steps:
3. Push the front-panel button PRGM. This will bring up the action selection menu.
4. Push RECALL in the main menu to display the menu used for recalling the front-panel Setup.
5. Use the arrow-labeled buttons to move the underline to the label "FPNL."
6. Push RECALL and the front-panel settings will change to those settings that werestored for FPNL.

## NOTE

Remember this four-step procedure for recalling FPNL.

## NOTE

The following steps turn the Trigger Point Indicator (a small "T" displayed on waveforms) and the BELL on for use in this procedure. These functions cannot be stored in the frontpanel setup, but remain in effect until changed by the operator. Leave these functions turned on for the remainder of this procedure.
j. Press the MENU OFF/EXTENDED FUNCTIONS button twice to display the EXTENDED FUNCTION menu. Press the menu button labeled SYSTEM (menu will change).
k. Press the menu button labeled MISC (menu will change). Set TRIGTON|OFF and BELLON|OFF to ON for the displayed menu.
I. Press MENU OFF/EXTENDED FUNCTIONS to exit the extended functions.

## VERTICAL SYSTEM

## Equipment Required (see table 4-1)

Leveled Sine-Wave Generator (Item 1)
Calibration Generator (Item 3)
Power Supply (Item 6)
$50 \Omega$ Coaxial Cable (Item 10)
$50 \Omega$ Precision Coaxial Cable (Item 11)

$$
50 \Omega \text { Precision Coaxial Cable (Item 11) }
$$

## 10X Attenuator (Item 13)

5X Attenuator (Item 14)
2X Attenuator (Item 15)
1X Probe (Item 17)
Dual-Input Coupler (Item 18)

## 1. Verify CH 1 and CH $250 \Omega$ OVERLOAD Protection.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

## NOTE

Changing Front Panel settings before the scope has recovered from a $50 \Omega$ Overload condition may cause the scope to "lock up". If the scope locks up, remove the cause of the overload and press the POWER switch off and then on.

| Set: | CH 1 VOLTS/DIV | 1 V |
| :--- | :--- | :--- |
|  | CH 2 VOLTS/DIV | 1 V |

Select: VERTICAL MODE
Set: CH 2 Off
Select: CH 1 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
Select: CH 2 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
b. Connect the Power Supply (Power Supply should be turned off) to the CH 1 OR X input connector via a BNC Female-to-Dual Banana adapter and a $50 \Omega$ Coaxial Cable.
c. Using the CH 1 VERTICAL POSITION control, align the trace to the bottom graticule line.
d. Turn on the Power Supply.
e. Adjust the Power Supply output level until the CH 1 trace rises to 1 division above the center graticule line (5V).
f. Select CH 1 COUPLING/INVERT and set $50 \Omega$ ON|OFF to ON.
g. VERIFY - For a period of 1 minute, the readout display does not indicate any overload condition ( $50 \Omega$ OVERLOAD).
h. Set $50 \Omega$ ON|OFF to OFF and the CH 1 VOLTS/DIV to 5 V .

CAUTION

> To prevent damage to the input circuitry when in $50 \Omega$ DC coupling mode, the 20 V Power Supply should be turned off immediately if automatic OVERLOAD switching does not occur within 15 seconds after applying the power source and setting the $50 \Omega$ coupling on in part j.
i. Increase the Power Supply output level until the CH 1 trace rises to the center graticule line ( +20 V ).

## NOTE

When performing part j, setting $50 \Omega$ ON |OFF to ON, note that the Power Supply's current output is adequate to keep the voltage level at +20 V .
J. Set $50 \Omega$ ON|OFF to $O N$.
k. VERIFY-Approximately 10 seconds (no longer than 15 seconds) after CH $150 \Omega$ ON|OFF is set to ON, the readout display indicates " $50 \Omega$ OVERLOAD" and the CH 1 COUPLING switches to GND.
I. Turn the Power Supply off.
m. Disconnect the Power Supply.
n. Clear the $50 \Omega$ OVERLOAD condition by setting CH 1 COUPLING to DC.
O. VERIFY - The readout display no longer indicates " $50 \Omega$ OVERLOAD" and the CH 1 COUPLING/INVERT menu indicates DC on.
p. Select VERTICAL MODE and set CH 1 off and CH 2 on.
q. Repeat $b$ through o using CH 2 control settings and input to verify $50 \Omega$ OVERLOAD protection for CH 2.

## 2. Check CH 1 and CH 2 AC/DC/GND COUPLING/INVERT Modes.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

| Set: | CH 1 VOLTS/DIV | 200 mV |
| :--- | :--- | :--- |
|  | CH 2 VOLTS/DIV | 200 mV |
| Select: | VERTICAL MODE |  |
| Set: | CH 2 | Off |
| Select: | CH 2 COUPLING/INVERT |  |
| Set: | $50 \Omega$ ONJOFF | OFF |
|  | GND | On |

Select: CH 1 COUPLING/INVERT

| Set: | $50 \Omega$ ON $\mid$ OFF | OFF |
| :--- | :--- | :--- |
|  | GND | On |
| Set: | A SEC/DIV | 5 ms |

b. Connect the CALIBRATOR output signal to the CH 1 OR X input connector using a 1 X probe.
c. Set the CH 1 COUPLING/INVERT menu to DC on. (A GND symbol disappears next to the CH 1 scale factor readout.)
d. CHECK-Display for a square wave which steps positive (upwards) approximately 2 divisions from the center horizontal graticule line.
e. Set CH 1 COUPLING to AC (a sine wave symbol appears next to the CH 9 scale factor readout in upper left-hand corner of CRT).
f. CHECK - Display for a tilted square wave of approximately 2 divisions (average) amplitude centered vertically around the center horizontal graticule line.
g. Set $50 \Omega \mathrm{ON} \mid$ OFF to ON (the sine wave symbol is replaced by an ohm symbol next to the CH 1 scale factor readout).

## NOTE

Amplitudes are less than 1 division ( 200 mV ) for checks $h$ and j since the $1 \times$ probe's resistance is significant when compared to the $50 \Omega$ inputs of the scope.
h. CHECK-Display for a square wave which steps positive (upwards) approximately 0.5 division from the center horizontal graticule line. VERIFY - That CH 1 COUPLING automatically switched from AC on to DC on.
i. Set INVERT ON JOFF to ON (an inverted arrow appears left of the CH 1 scale factor readout).
j. CHECK-Displayed square wave now steps downwards from the center horizontal graticule line and is approximately 0.5 division in amplitude.
k. Select VERTICAL MODE and set CH 2 on and CH 1 off. Select CH 2 COUPLING/INVERT to display that menu.

1. Move the $1 X$ Probe from the $\mathrm{CH} 1 \mathrm{OR} X$ input connector to the CH 2 OR $Y$ input connector.
m. Repeat parts $\mathbf{c}$ through $\mathbf{j}$ using the CH 2 OR Y input and controls.
n. Disconnect the test setup.
2. Check CH 1 and CH 2 VOLTS/DIV Display and Readout Accuracies. Check the $A$ and $B$ TRIGGER LEVEL Readout Accuracies.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE
Set
Off
$\begin{array}{ll}\text { Select: } \mathrm{CH} 1 \text { COUPLING/INVERT } \\ \text { Set: } & 50 \Omega \text { ON|OFF }\end{array}$
Select: CH 2 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
Select: BANDWIDTH
Set: 20 MHz On
Select: TRIGGER MODE
Set: AUTO On
b. Connect the Calibration Generator's STD AMPLITUDE output to the CH 1 OR X input connector via a $50 \Omega$ Coaxial Cable. Do not use a Termination.
c. CHECK -CH 1 and CH 2 VOLTS/DIV and TRIGGER LEVEL readout accuracies as follows:

1. Set VOLTS/DIV control to the first position listed in Table 4-2.
2. Set the Calibration Generator STD AMPLITUDE output level to the corresponding Standard Amplitude Out level in Table 4-2. Use the TRIGGER LEVEL control as necessary to obtain a stable display.

## NOTE

To properly verify TRIGGER LEVEL readout accuracy, the Callibration Generator's output must have rising and falling transition times ( $10 \%$ to $90 \%$ ) > 20 ns. No overshoot should appear on the waveform.
3. Verify that the Calibration Generator output meets the requirements noted above.
4. Use the VERTICAL POSITION control to set the bottom of the signal 3 divisions below graticule center.
5. Select CURSOR FUNCTION and set VOLTS on.
6. Using the CURSOR/DELAY control, align the selected cursor (segmented) with the bottom of the displayed waveform.
7. Push the CURSOR SELECT button to select the other cursor (it will change from solid to segmented).
8. Use the CURSOR/DELAY control to align this cursor to the top of the waveform. Take care to use the same reference points (top edge, bottom edge, or center) of the waveform and cursor as in subpart 6.

## NOTE

For VOLTSIDIV Control Settings of $2 \mathrm{mV}, 5 \mathrm{mV}$, and 10 mV , select TRIGGER CPLG and set NOISE REJ on. In addition, connect the Calibration Generator STD AMPLITUDE output to the CH 1 OR X input connector via a $50 \Omega$ cable and a 10 X attenuator for the settings listed above. For all other settings, set NOISE REJ off and remove the 10X attenuator.
9. CHECK - That the voltage reading displayed by the cursor readout is within the limits given in Table 4-2 under the CURSOR VOLTS Readout Accura-cy-NORMAL MODE column.
10. Select STORAGE ACQUIRE and set ENVELOPE on.
11. Using the CURSOR/DELAY control, readjust the cursors as necessary to align them to the top or bottom (discount noise) of the waveform. Press CURSOR SELECT as needed to toggle between the two cursors.
12. CHECK-That the voltage reading displayed is within the limits given in Table 4-2 under the CURSOR VOLTS Readout Accuracy-ENVELOPE MODE column.
13. Set the ACQUIRE menu back to NORMAL on.
14. Set the TRIGGER LEVEL control at the most positive voltage that produces a barely triggered, jittering display for the positive (+) setting for the slope switch.
15. CHECK-The A Trigger Level readings (up-per-right corner of display) are within the limits listed in the ( + ) Peak column under Limits-DC Coupling in Table 4-2.
16. Set the TRIGGER LEVEL control at the most negative voltage that produces a barely triggered, jittering display for negative ( - ) setting for the slope switch.
17. CHECK - The A Trigger Level readings are within the limits listed in the (-) Peak column under Limits-DC Coupling in Table 4-2.
18. Set the TRIGGER LEVEL control for a stable display.
19. Press the $A / B$ TRIG button to set the $B$ Trigger System on.
20. Set HORIZ MODE to B.
21. Set the TRIGGER LEVEL control at the most positive voltage that produces a barely triggered, jittering display for the positive ( + ) setting for the slope switch.
22. CHECK - That the B Trigger Level readings (up-per-right corner of display) are within the limits listed in the $(+)$ Peak column under Limits-DC Coupling in Table 4-2.
23. Set the TRIGGER LEVEL control at the most negative voltage that produces a barely triggered, jittering display for negative (-) setting for the slope switch.
24. CHECK - That the B Trigger Level readings are within the limits listed in the (-) Peak column under Limits-DC Coupling in Table 4-2.
25. Set the HORIZ MODE to A.
26. Press the A/B TRIG button to set the A Trigger System on.
27. Set the VOLTS/DIV control to the next position listed in Table 4-2.
28. Set the Calibration Generator STD AMPLITUDE output level to the corresponding Standard Amplitude Out level in Table 4-2.
29. Use the VERTICAL POSITION control to set the bottom of the signal 3 divisions below graticule center.
30. Repeat subparts 6 through 29 for each VOLTS/DIV Control setting listed in Table 4-2. Skip subparts 26 through 29 when checking the last VOLTS/DIV Control setting in the table.
31. Press A/B TRIG to set the B Trigger System on. Select TRIGGER CPLG and set REJECT NOISE on.
32. Press A/B TRIG to set the A Trigger System on (the A TRIG CPLG menu will be displayed). Set REJECT NOISE on.
33. Set the CH 1 VOLTS/DIV control to 50 mV .
34. Set the Calibration Generator's STD AMPLITUDE output level to 0.2 V .
35. Repeat subparts 14 through 24 , using 147 mV to 253 mV as the limits to check against in subparts 15 and 22 and +47 mV to -47 mV as the limits for subparts 17 and 24.
36. Set the B COUPLING mode back to DC on (B TRIGGER CPLG menu is still displayed from subpart 24).
37. Press the A/B TRIG button to set the A Trigger System on (the A COUPLING menu will be displayed). Set A COUPLING to DC on.
38. Set HORIZONTAL MODE to A.

Table 4-2
Accuracy Limits CH 1 and CH 2 CURSOR VOLTS Readout and $A$ and $B$ TRIGGER Readouts

| VOLTS/ DIV Control | Standard Amplitude Out | CURSOR VOLTS Readout Accuracy |  | TRIGGER LEVEL Readout |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | NORMAL MODE$(2 \%+0.04 \text { div })$ | ENVELOPE MODE$(3 \%+0.04 \text { div) }$ | Limits-DC Coupling |  |
|  |  |  |  | + Peak | -Peak |
| $2 \mathrm{mV}{ }^{\text {a }}$ | 100 mV | 9.72 mV to 10.28 mV | 9.62 mV to 10.38 mV | 8.5 mV to 11.5 mV | $\pm 1.2 \mathrm{mV}$ |
| $5 \mathrm{mV}{ }^{\text {a }}$ | 200 mV | 19.40 mV to 20.60 mV | 19.20 mV to 20.80 mV | 17.2 mV to 22.8 mV | $\pm 2.2 \mathrm{mV}$ |
| $10 \mathrm{mV}{ }^{\text {a }}$ | 500 mV | 48.60 mV to 51.40 mV | 48.10 mV to 51.90 mV | 44.4 mV to 55.6 mV | $\pm 4.0 \mathrm{mV}$ |
| 20 mV | 0.1 V | 97.20 mV to 102.80 mV | 96.20 mV to 103.80 mV | 89.6 mV to 110.4 mV | $\pm 7.2 \mathrm{mV}$ |
| 50 mV | 0.2 V | 194.00 mV to 206.00 mV | 192.00 mV to 208.00 mV | 178.0 mV to 222.0 mV | $\pm 16.0 \mathrm{mV}$ |
| 100 mV | 0.5 V | 486.00 mV to 514.00 mV | 481.00 mV to 519.00 mV | 448.0 mV to 552.0 mV | $\pm 36.0 \mathrm{mV}$ |
| 200 mV | 1 V | 972.00 mV to 1.03 V | 962.00 mV to 1.04 V | 896.0 mV to 1.1 V | $\pm 72.0 \mathrm{mV}$ |
| 500 mV | 2 V | 1.94 V to 2.06 V | 1.92 V to 2.08 V | 1.8 V to 2.2 V | $\pm 160.0 \mathrm{mV}$ |
| 1 V | 5 V | 4.86 V to 5.14 V | 4.81 V to 5.19 V | 4.5 V to 5.5 V | $\pm 360.0 \mathrm{mV}$ |
| 2 V | 10 V | 9.72 V to 10.28 V | 9.62 V to 10.38 V | 9.0 V to 11.0 V | $\pm 710.0 \mathrm{mV}$ |
| 5 V | 20 V | 19.40 V to 20.60 V | 19.20 V to 20.80 V | 17.8 V to 22.2 V | $\pm 1.6 \mathrm{~V}$ |

alnstall a X10 attenuator between the $50 \Omega$ Coaxial Cable and the input channel BNC for this check only.
39. Set the CH 1 VOLTS/DIV control to 1 V and the Calibration Generator's output level to 5 V .
40. Select CH 1 VARIABLE and press and hold down the menu button labeled " $\downarrow$ " until the displayed waveform no longer decreases in amplitude.
41. CHECK - That the amplitude of the displayed waveform is two divisions or less. VERIFY - That a " > " symbol appears immediately left of the CH 1 scale factor readout.
42. VERIFY - That the amplitude of the displayed waveform increases when the menu button labeled " $\dagger$ " is pushed.
43. Press CAL. VERIFY - That the waveform has returned to its original amplitude and that the " $>$ " symbol is no longer displayed.
44. Select CH 1 COUPLING/INVERT and set INVERT ON|OFF to ON.
45. Using the VERTICAL POSITION control, set the bottom of the waveform 3 divisions below graticule center.
46. Repeat subparts 6 through 9 to check INVERT accuracy.
47. Return INVERT ONIOFF to OFF.
48. Select VERTICAL MODE and set CH 2 on and CH 1 off. Move the $50 \Omega$ Coaxial Cable to the CH 2 OR Y input connector.
49. Repeat subparts 1 through 48 (skipping 5) to check the functions and accuracies for CH 2.
50. Select TRIGGER MODE and set AUTO LEVEL on.
51. Remove the $50 \Omega$ Coaxial Cable from the CH 2 OR $Y$ input connector and connect the 5 V standard amplitude signal to CH 1 ORX and CH 2 OR Y input connectors through a Dual-Input Coupler.
52. Using the CH 2 VERTICAL POSITION control, set the bottom of the CH 2 waveform 1.5 divisions below graticule center.
53. Select VERTICAL MODE and set CH 1 on. Use the CH 1 VERTICAL POSITION to superimpose the CH 1 waveform exactly over the CH 2 waveform.
54. Set CH 1 and CH 2 VOLT/DIV controls to 2 V. Set CH 1 and CH 2 off and ADD on.
55. Align the cursors to the top and bottom of the displayed waveform as in subparts 6 through 8.
56. CHECK - That the cursor readout indicates about 10 V .
57. Set CH 1 and CH 2 VOLTS/DIV back to 1 V and set MULT on (ADD will be turned off).
58. Align the cursors to the top and bottom of the displayed waveform as in subparts 6 through 8.
59. CHECK - That the cursor readout indicates about $25 \mathrm{~V}^{2}$.
d. Set MULT off and CH 1 on.
e. Precisely align one voltage cursor to the graticule line 3 divisions above graticule center and the other cursor to the line 3 divisions below graticule center.
f. CHECK - That the voltage reading displayed is within $1 \%$ of 6.00 Volts ( 5.94 to 6.06).
g. Disconnect the test setup.

## 4. Check LF Linearity.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

## Select: VERTICAL MODE

Set: CH 2 Off
Select: CH 1 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
Select: CH 2 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
b. Connect the Calibration Generator's STD AMPLITUDE output to the CH 1 OR X input connector via a $50 \Omega$ Coaxial Cable. Do not use a Termination.
c. Set the Calibration Generator's STD AMPLITUDE output level to 0.2 V .
d. Use the CH 1 POSITION control to center the waveform vertically around the center horizontal graticule line.
e. Use the generator's VARIABLE control to adjust the waveform for exactly 2 vertical divisions on screen (discount trace width).
f. Use the CH 1 POSITION control to align the top of the waveform to the top horizontal graticule line.
g. CHECK - That the amplitude of the displayed waveform is between 1.88 and 2.12 divisions.
h. Use the CH 1 POSITION control to align the bottom of the waveform to the bottom horizontal graticule line.
i. CHECK-That the amplitude of the displayed waveform is between 1.88 and 2.12 divisions.
j. Select STORAGE ACQUIRE and set ENVELOPE on.
k. Repeat parts $d$ through ito check the LF Linearity for the ENVELOPE mode. Discount the noise and the envelope "fill" when performing parts $g$ and $i$ and use 1.84 and 2.16 divisions as limits for those parts.
I. Set the STORAGE ACQUIRE mode back to NORMAL on.
m. Move the $50 \Omega$ Coaxial Cable from the CH 1 ORX input connector to the CH 2 OR Y input connector.
n. Select VERTICAL MODE and set CH 2 on and CH 1 off.
o. Repeat parts d through $\mathbf{k}$ to check $\mathbf{C H} 2$ using $\mathbf{C H} 2$ control settings and menus.
p. Disconnect the test setup.

## Performance Check and Functional Verification Procedure 2440 Service

## 5. Check CH 1 and CH 2 Position Range.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

| Set: | CH 1 VOLTS/DIV | 20 mV |
| :--- | :--- | :--- |
|  | CH 2 VOLT/DIV | 20 mV |
|  | A SEC/DIV | $10 \mu \mathrm{~s}$ |
| Select: | VERTICAL MODE |  |
| Set: | CH 2 | Off |

b. Connect a 50 kHz reference frequency signal from the Leveled Sine-Wave Generator to the CH 1 OR X input connector via a $50 \Omega$ Coaxial Cable and a 5 X Attenuator.
c. Adjust the Leveled Sine-Wave Generator's output level for a 4-division display on screen.
d. Remove the 5 X Attenuator and connect the $50 \Omega$ Coaxial Cable directly to the CH 1 OR X input connector.
e. Rotate the CH 1 POSITION control full clockwise and hold until the waveform no longer moves up screen.
f. CHECK - That the bottom of the waveform is within +0.4 to -0.7 division of the center horizontal graticule line.
g. Rotate the CH 1 POSITION control full counter-clockwise and hold until the waveform no longer moves down screen.
h. CHECK - That the top of the waveform is within +0.7 to -0.4 division of the center horizontal graticule line.
i. Reinstall the 5X Attenuator and move the $50 \Omega$ Coaxial Cable to the CH 2 OR Y input connector.
j. Select VERTICAL MODE and set CH 2 on and CH 1 off.
k. Repeat parts cthrough $h$ to check CH 2's position range, using the CH2ORY input connector and controls.
6. Check CH 1 and CH 2 Bandwidth and Bandwidth Limit ( 20 MHz and 100 MHz ).
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

| Set: | CH 1 VOLTS/DIV | 2 mV |
| :--- | :--- | :--- |
|  | CH 2 VOLTS/DIV | 2 mV |
|  | A SEC/DIV | 100 ns |
| Select: | VERTICAL MODE |  |
| Set: | CH 2 |  |
|  |  |  |

b. Connect the output of the Secondary Leveled Sine-Wave Generator to the CH 1 OR X input connector via a $50 \Omega$ Precision Coaxial Cable, a 10X Attenuator, and a $2 \times$ Attenuator.
C. Set the Leveled Sine-Wave Generator output level for a 6 -division display at the 6 MHz reference frequency, then change the output frequency to 300 MHz .
d. Set A SEC/DIV to 2 ns .
e. CHECK-The display amplitude is 4.2 divisions or greater.
f. Return the A SEC/DIV to 100 ns and set the CH 1 VOLT/DIV control to the next higher setting.
g. Repeat parts c through for all CH 1 VOLTS/DIV settings through 500 mV , removing and/or adding $10 \mathrm{X}, 5 \mathrm{X}$, and 2X Attenuators as necessary to allow adjusting the Leveled Sine-Wave Generator output level to 6 divisions.
h. Return A SEC/DIV to 100 ns .
i. Select VERTICAL MODE and set CH 2 on and CH 1 off.
j. Repeat parts $b$ through $g$ to check CH 2 bandwidth, substituting CH 2 controls and input connector.
k. Set A SEC/DIV to $10 \mu \mathrm{~s}$.

1. Disconnect the Secondary Leveled Sine-Wave Generator from the CH 1 ORX input connector.
m . Connect the output of the Primary Leveled Sine-wave generator to the CH 2 OR Y input connector via a precision $50 \Omega$ Coaxial Cable and any combination of the 10X, 5 X , and 2 X attenuators that reduces the signal amplitude to the level called for in part $n$
n. Set the Primary Leveled Sine-Wave Generator to a $50-\mathrm{kHz}$ reference frequency and adjust the output level for a 6-division display (change 10X, 5X, and 2X Attenuators as required).
o. Select VERTICAL BANDWIDTH and set 20 MHz on. Set the A SEC/DIV to 20 ns .
p. Increase the Leveled Sine-Wave Generator's output frequency until the display amplitude is 4.2 divisions.
q. CHECK - That the Leveled Sine-Wave Generator's output frequency is from 13 MHz to 24 MHz .
r. Set the VERTICAL BANDWIDTH to 100 MHz on and increase the Primary Leveled Sine-Wave Generator's output frequency until the display amplitude is 4.2 divisions.
s. CHECK - That the Leveled Sine-Wave Generator's output frequency is from 80 MHz to 120 MHz .
t. Set the VERTICAL BANDWIDTH to FULL and set $A$ SEC/DIV to $10 \mu \mathrm{~s}$. Move the $50 \Omega$ Precision Coaxial Cable from the CH 2 OR Y input connector to the CH 1 OR X input connector.
u. Select VERTICAL MODE and set CH 1 on and CH 2 off.
v. Repeat parts $\mathbf{m}$ through s to check bandwidth limit for CH 1.
w. Disconnect the test setup.

## 7. Check Common Mode Rejection Ratio

 (CMRR).a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

| Set: | A SEC/DIV | $10 \mu s$ |
| :---: | :---: | :---: |
| Select: | VERTICAL MODE |  |
| Set: | CH 2 | Off |
|  | ADD | On |
| Select: | CH 1 COUPLING/INVERT |  |
| Set: | INVERT ON\|OFF | ON |
| Select: | TRIGGER SOURCE |  |
| Set: | CHAN 1\|2 | 1 |
| Select: | CURSOR FUNCTION |  |
| Set: | VOLTS | On |
| Menu displayed: |  |  |
|  | ATTACH CURSORS TO: |  |
| Set: | ADD | On |
| Select: | STORAGE ACQUIRE |  |
| Set: | AVG | On |

## NOTE

When the Initial Front Panel Setup is recalled in part a, the CH 1 and CH 2 traces will be centered vertically. DO NOT adjust the CH 1 or CH 2 POSITION controls during the remainder of this CMRR check to avoid exceeding the dynamic range of the CH 1 andlor CH 2 Vertical systems. If the controls are accidently adjusted, go back to part a and repeat this check.
b. Connect a 50 kHz reference frequency signal from the Leveled Sine-Wave Generator to the CH 1 OR $X$ and CH 2 OR Y input connectors via a $50 \Omega$ Coaxial Cable and a Dual-input Coupler.
c. Set the Leveied Sine-Wave Generator output level for a 5 -division display of the reference signal on CH 1.
d. Set the CH 1 and CH 2 VOLT/DIV controls to 50 mV .
e. Select VERTICAL MODE and set CH 1 off.
f. Select CH 2 VARIABLE only and, using the menu buttons under the arrow symbols, adjust for minimum ADD display amplitude.
g. Set the A SEC/DIV to 20 ns .
h. Set the Leveled Sine-Wave Generator's output frequency to $\mathbf{5 0} \mathrm{MHz}$.
i. Using the CURSOR/DELAY control, align the movable cursor (segmented) to the top of the ADD waveform.
j. Press CURSOR/SELECT to enable the alternate cursor.
k. Use the CURSOR/DELAY control to align this cursor to the bottom of the ADD waveform. Take care to use the same reference points (top edge, bottom edge, or center) of the waveform and cursor as in part $i$.
I. CHECK - That the cursor readout (upper right corner of display) indicates 50.0 mV or less.
m. Set the Leveled Sine-Wave Generator's output frequency back to 50 kHz .
n. Set the VARIABLE menu back to CAL and return the A TIME/DIV control to $10 \mu \mathrm{~s}$.
o. Select CH 1 COUPLING/INVERT and set INVERT ONJOFF to OFF.
p. Select CH 2 COUPLING/INVERT and set INVERT ONJOFF to ON.
q. Repeat parts f through I to check CMRR with CH 2 inverted. Be sure to use the CH 2 VARIABLE for part $f$ (cursor readout will be in DIV instead of $V$ units if CH 1 VARIABLE is used).
r. Remove the test setup.

## Performance Check and Functional Verification Procedure 2440 Service

8. Check Channel Isolation.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Set: A SEC/DIV 5 ns
Select: CURSOR FUNCTION
Set: VOLT On
(The ATTACH CURSOR menu will be displayed).
NOTE
When the Initial Front Panel Setup is recalled in part a, the CH 1 and CH 2 traces will be centered vertically. DO NOT adjust the CH 1 or CH 2 POSITION controls during the remainder of this Channel Isolation check to avoid exceeding the dynamic range of the CH 1 and/or CH 2 Vertical systems. If the controls are accidently adjusted, go back to part a and repeat this check.
b. Connect the Primary Leveled Sine-Wave Generator to the CH 1 OR X input connector via a $50 \Omega$ Coaxial Cable.
c. Set the Primary Leveled Sine-Wave Generator frequency to 100 MHz and adjust the output level for a 5-division display.
d. Set the CH 1 and CH 2 VOLTS/DIV controls to 50 mV .
e. Using the CURSOR/DELAY control, align the movable cursor (segmented) to the top of the CH 2 waveform.
f. Press CURSOR/SELECT to enable the alternate cursor.
g. Use the CURSOR/DELAY control to align this cursor to the bottom of the CH 2 waveform. Take care to use the same reference points (top edge, bottom edge, or center) of the waveform and cursor as in part e.
h. CHECK - That the cursor readout (upper right corner of display) indicates 5.00 mV or less.
i. Disconnect the generator from $\mathrm{CH} 1 \mathrm{OR} X$ input connector and connect it to CH 2 OR $Y$ input connector. Change the CH 2 VOLTS/DIV to 100 mV .
j. Select TRIGGER SOURCE and set CHAN 1|2 to 2.
k. Set the generator for 5 divisions in CH 2. Return the CH 2 VOLTS/DIV control to 50 mV .

1. Perform parts e-h, checking the CH 1 channel isolation instead of CH 2.
m. Set both VOLTS/DIV controls to 100 mV , the SEC/DIV control to 2 ns. Select TRIGGER SOURCE and set CHAN $1 \mid 2$ to 1.
n. Connect the Secondary Leveled Sine-Wave Generator to the CH 1 OR X input connector via a $50 \Omega$ Coaxial Cable.
o. Set the Secondary Leveled Sine-Wave Generator frequency to 300 MHz and adjust the output level for a 5-division display.
p. Repeat parts $d$ through 1 , using 10.00 mV as the limit for part h, to check 300 MHz channel isolation.
q. Disconnect the test setup.
2. Check the CH 2 Output Voltage Accuracy and Bandwidth.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

| Set: | CH 1 VOLTS/DIV | 20 mV |
| :--- | :--- | :---: |
| Select: | CH 2 COUPLING/INVERT |  |
| Set: | $50 \Omega$ ON/OFF | OFF |
| Select: | TRIGGER SOURCE |  |
| Set: | CHAN 1\|2 | 2 |
| Select: | CURSOR FUNCTION |  |
| Set: | VOLTS | On |
| Menu displayed: ATTACH CURSORS TO |  |  |
| Set: | CH 1 | On |

b. Connect the Calibration Generator's STD AMPLITUDE output to the CH 2 OR Y input connector via a $50 \Omega$ Coaxial Cable. Do not use a Termination.
c. Set the Calibration Generator STD AMPLITUDE output level to 0.5 V .
d. Use the CH 2 VERTICAL POSITION control to align the bottom of the displayed waveform to the graticule line three divisions below graticule center.
e. Use the Calibration Generator's VARIABLE AMPLITUDE control to adjust the CH 2 display for precisely 5 divisions amplitude.
f. Connect the CH 2 SIGNAL OUTPUT connector (on the rear panel) to the CH 1 OR X input connector via a $50 \Omega$ Coaxial Cable. Do not use a Termination.
g. Select VERTICAL MODE and set CH 2 off.
h. Use the CH 1 VERTICAL POSITION control to align the bottom of the displayed waveform to the graticule line three divisions below graticule center.
i. Using the CURSOR/DELAY control, align the movable cursor (segmented) to the top of the CH 1 waveform.
j. Press CURSOR/SELECT to enable the alternate cursor.
k. Use the CURSOR/DELAY control to align this cursor to the bottom of the CH 1 waveform. Take care to use the same reference points (top edge, bottom edge, or center) of the waveform and cursor as in part i.
I. CHECK - That the cursor readout (upper right corner of display) indicates 45.00 to 55.00 mV .
m. Select CH 1 COUPLING/INVERT and set $50 \Omega$ ON|OFF to OFF.
n. Align the cursors to the displayed waveform as in parts $i$ and $k$.
o. CHECK - That the cursor readout indicates 90.00 to 110.00 mV . Set $50 \Omega$ ON ${ }^{2}$ OFF back to ON.
p. Disconnect the $50 \Omega$ Coaxial Cable from the Calibration Generator's output and connect it to the output of a Leveled Sine-Wave Generator.
q. Select CH 2 COUPLING/INVERT and set $50 \Omega$ ON|OFF to ON.
r. Set the A SEC/DIV control to 200 ns .
s. Set the Leveled Sine-Wave Generator output level for a 6 -division display at the 3 MHz reference frequency, then change the output frequency to 50 MHz . Adjust the CH 1 VERTICAL POSITION control as required to view the display.
t. Set the A SEC/DIV control to 5 ns .
u. CHECK-The display amplitude is 4.2 divisions or greater.
v. Disconnect the $50 \Omega$ Coaxial Cable from the CH 2 ORY input connector.
w. Select CH 1 COUPLING/INVERT and set GND on. Set the A SEC/DIV control to $500 \mu \mathrm{~s}$.
$x$. Use the CH 1 VERTICAL POSITION control to align the grounded trace to the center horizontal graticule line.
y. Set the CH 1 VOLTS/DIV to 5 mV and the CH 1 COUPLING to DC.
2. VERIFY - That the trace is within $\pm 2$ divisions of the center graticule line.
aa. Disconnect the test setup.
10. Check Display Versus Graticule Centering and Dot Versus Vector Display Offset. Check VECTOR Response for NORMAL and ENVELOPE Acquisition modes.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE
Set: CH 2
Off
Select: CH 1 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
b. Press the front-panel button labeled SELECT.
c. Set VECTORS ON|OFF to OFF for the displayed menu.
d. CHECK-That the CH 1 trace is no more than 0.1 division above or below the center horizontal graticule line.
e. Select CURSOR FUNCTION and set TIME on. Note that one cursor is displayed 4 divisions left, one 4 divisions right of the center graticule line. Do NOT adjust the placement of the time cursors displayed.
f. CHECK - That each cursor is within $\pm 0.1$ division of the vertical graticule line at which it is located.
g. Press the menu button labeled TIME to turn off the cursors.
h. Connect the STD AMPL OUTPUT of a Calibration Generator to the CH 1 ORX input connector via a $50 \Omega$ Coaxial Cable.
i. Set the AMPLITUDE control of the Calibration Generator for a 0.2 V setting.
j. Select STORAGE ACQUIRE and set AVG on.
k. Press the front-panel button labeled SELECT (next to the INTENSITY control).

1. Toggle the VECTORS ON | OFF button for the displayed menu, between the ON/OFF settings while making the check in the following part.
m. CHECK-That the display shifts no more than $\pm 0.05$ division while performing part 1 .
n. Disconnect the Calibration Generator from the CH 1 OR X input connector.
o. Select PRGM and press the menu button labeled INIT PANEL.
p. Select TRIGGER MODE and set AUTO on.
q. Select STORAGE ACQUIRE and set ENVELOPE on. Repeatedly press the ENVELOPE menu button until CONT (Continuous) appears above the label.
r. Use the CH 1 VERTICAL POSITION control to move the displayed trace up 3 divisions and down 3 divisions to create a 6-division "filled" envelope on screen.
s. Press the SELECT button (next to the INTENSITY control).
t. CHECK - For no more than a 0.06 -division change in amplitude between the "filled" envelope and the nonfilled envelope as VECTORS ON|OFF is switched between the ON and OFF settings for the displayed menu.

## TRIGGERING SYSTEMS

## NOTE

The CH 1 and CH 2 Trigger Level Readout Accuracies are checked in the Vertical Systems subsection.
In this procedure, a "stable trigger" refers to a consistent trigger; that is, one that results in a uniform, regular display triggered on the selected slope ( $\pm$ ). A stably-triggered display should NOT have the trigger point switch between opposite slopes on the waveform, nor should it "roll" across the screen, as successive acquisitions occur. At TIMEIDIV settings of $2 \mathrm{~ms} / D I V$ and faster, the TRIG'D LED is constantly lit if the display is stably triggered (note that, for Tables 4-3 and 4-4, the LED will flash for the $10 \mathrm{~ms} / D / \mathrm{checks}$ ).

## Equipment Required (see table 4-1)

Leveled Sine-Wave Generator (Primary) (Item 1)
Leveled Sine-Wave Generator (Secondary) (Item 2)
Time-Mark Generator (Item 4)
Function Generator (Item 5)
$50 \Omega$ Coaxial Cable (Item 10)
$50 \Omega$ Termination (Item 12)
5X Attenuator (Item 14)
10X Probe (Item 16)
Dual-Input Coupler (Item 18)

## 1. Check A and B Internal Source Trigger

 Sensitivity.
## NOTE

This step checks the CH 1 trigger source for all trigger coupling settings for both $A$ and $B$ Horizontal Modes. The other sources are checked for DC coupling only. Normally, checking all coupling modes for one trigger source is adequate since all the sources share common coupling circuitry; other sources need only be checked in the DC trigger coupling setting to verify their signal paths. However, if a source's trigger sensitivity is very near the limits specified in Table 4-3, this procedure will specify additional checks for the other trigger coupling settings.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE
Set: CH 2 Off
Select: CH 1 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
Select: CH 2 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF

Select: TRIGGER MODE
Set: AUTO ON
b. Connect the sine-wave output of the appropriate generator through a $50 \Omega$ Coaxial Cable and a $50 \Omega$ Termination to the CH 1 OR X input connector. Use the Function Generator for Test Frequencies below 50 MHz . Use the Primary Leveled Sine-wave Generator for the 50 MHz Test Frequencies. Use the Secondary Leveled Sine-wave Generator for the 300 MHz Test Frequencies.
C. Adjust the generator's output frequency to the first Test Frequency setting specified in Table 4-3.
d. Set the SEC/DIV control to the setting used with the Test Frequency.
e. Set the output amplitude of the specified Test Frequency to the level given in Table 4-3 for the A Trigger System with DC Trigger Coupling.

NOTE
When amplitudes of less than 1 division are required, adjust the generator for 10X the specified amplitude with the CH 1 VOLTIDIN set to 100 mV and change the setting to 1 V before making the checks. For amplitudes $\geq$ to 1 division, simply adjust for the required amplitude with the VOLT/DIV set to 100 mV .

Table 4-3
Minimum Display Level for CH 1 or CH 2 Triggering (in divisions)

| Trigger System | Test Frequency | SEC/DIV Setting | TRIGGER COUPLING |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | DC | AC | NOISE REJ | HF REJ | LF REJ |
| A | 60 Hz | 10 ms | 0.35 | 0.35 | - | - | $(0.35)^{\text {b }}$ |
| B | 60 Hz | 10 ms | 0.70 | 0.70 | - | . | $(0.70)^{\text {b }}$ |
| A | 30 kHz | $20 \mu \mathrm{~s}$ | 0.35 | 0.35 | - | 0.5 | a |
| B | 30 kHz | $20 \mu \mathrm{~s}$ | 0.70 | 0.70 | . | 1.0 | a |
| A | 80 kHz | $10 \mu \mathrm{~s}$ | 0.35 | 0.35 | $\cdots$ | - | 0.5 |
| B | 80 kHz | $10 \mu \mathrm{~s}$ | 0.70 | 0.70 | - | $\bullet$ | 1.0 |
| A | 50 MHz | 20 ns | 0.35 | 0.35 | 1.2 | (1.2) ${ }^{\text {b }}$ | 0.5 |
| B | 50 MHz | 20 ns | 0.70 | 0.70 | 2.4 | (2.4) ${ }^{\text {b }}$ | 1.0 |
| A | $300 \mathrm{MHz}^{\text {c }}$ | 2 ns | 1.0 | 1 | 3.0 | (3.0) ${ }^{\text {b }}$ | 1.0 |
| B | $300 \mathrm{MHz}^{\text {c }}$ | 2 ns | 2.0 | 2.0 | 6.0 | (6.0) ${ }^{\text {b }}$ | 2.0 |
| ADD Vertical Mode |  |  |  |  |  |  |  |
| A | $300 \mathrm{MHz}^{\text {c }}$ | 2 ns | 1.5 | 1.5 | 4.5 | - | 1.5 |
| B | $300 \mathrm{MHz}^{\text {c }}$ | 2 ns | 3.0 | 3.0 | 9.0 | . | 3.0 |

${ }^{\text {a }}$ Not necessary to check.
${ }^{6}$ Not triggered at the specified amplitude.
cAt frequencies above 100 MHz , it may be necessary to adjust the LEVEL control for a stable trigger and to make the display visible.
f. Select TRIGGER CPLG to display the A COUPLING menu.

## NOTE

When checking for triggers in parts $g$ and $h$, use the TRIGGER LEVEL control to trigger (or to attempt to trigger) on the waveform.
g. CHECK - For a stable, triggered display on both + and - slopes for all TRIGGER COUPLING settings that are specified at the present Test Frequency.
h. CHECK - For no stable trigger (display free-runs) for any TRIGGER COUPLING setting specifying the footnote "Not Triggered at specified amplitude."

1. Change the generator output amplitude as necessary and repeat parts $g$ through $h$ for any Trigger Coupling setting specifying a different Minimum Display Level for triggering other than the initial setting for that row. (For example, NOISE, HF, and LF settings usually - but not always-require different amplitudes than the initial setting.)
j. Set the generator's output to the next Test Frequency in Table 4-3.
k. Repeat parts d through j (skip part f) to check A Triggers for each test frequency setting in Table 4-3. Change generators (as specified in part b) as needed to obtain the test frequency required. Return the TRIGGER COUPLING menu to DC when completed.
2. Select VERTICAL MODE and set CH 1 off and CH 2 on.
m. Repeat parts $b$ through $k$ to check CH 2 triggers, using CH 2 control settings and input connector. Skip parts f, $h$, and $i$ and check only for DC trigger coupling in part $g$ if the DC trigger sensitivity is NOT near the specified limits; otherwise, check as for CH 1.
n. Select VERTICAL MODE and set ADD on and CH 2 off.
o. Repeat parts $b$ through $k$ to check ADD triggers, using CH 2 control settings and input connector. Skip parts $h$ and $i$ and check only for DC trigger coupling in part g if the DC trigger sensitivity is NOT near the specified limits; otherwise, check as for CH 1.
p. Select VERTICAL MODE and set ADD off and CH 1 on.
q. Set TRIGGER CPLG back to DC and set the HORIZONTAL MODE to B.
r. Press A/B TRIG to select the B Trigger System (the B COUPLING menu will be displayed).
s. Repeat part $b$ through $o$ to check $B$ triggers, using the TRIGGER LEVEL control to trigger the display. Use the generator amplitude settings specified in the Trigger System-B rows of Table 4-3.

## NOTE

When checking 50 MHz and 300 MHz Triggers for the B TRIGGER SYSTEM, the REPET mode acquisitions can require a long time to complete. When setting the B SEC/DN control for those TEST FREQUENCIES, set the HORIZONTAL MODE to A and set the A SEC/DIV control to the SEC/DIV setting specified in the table. This adjustment will set BOTH $A$ and $B$ Acquisition Systems to the specified SECIDIV setting and reduce the time required to complete the $B$ REPET acquisition sequence. Set the HORIZONTAL MODE back to B.
t. Disconnect the test setup.
2. Check Trigger Sensitivity for $A$ and $B$ External Sources.

## NOTE

This step checks the trigger sensitivity of the external sources for the DC trigger coupling setting only. Normally, checking all coupling modes for one trigger source (checked in step 1 of this subsection) is adequate since all the sources share common coupling circuitry; other sources need only be checked in the DC trigger coupling setting to verify their signal paths. However, if a source's trigger sensitivity is very near the limits specified in Table 4-4, this procedure will specify additional checks for the other trigger coupling settings.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE

$$
\text { Set: CH } 2 \quad \text { Off }
$$

Select: CH 1 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
Select: CH 2 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
Select: TRIGGER MODE
Set: AUTO On
b. Connect the sine wave output of the appropriate generator through a $50 \Omega$ Coaxial Cable, a 5X Attenuator, a $50 \Omega$ Termination (install $50 \Omega$ Termination between the 5X Attenuator and the Dual-Input Coupler) and a Dual-Input Coupler to the CH 1 OR X and the EXT TRIG 1 input connectors. Use the Function Generator for Test Frequencies below 50 MHz . Use the Primary Leveled Sine-wave Generator for the 50 MHz Test Frequencies. Use the Secondary Leveled Sine-wave Generator for the 300 MHz Test Frequencies.
c. Select TRIGGER SOURCE and push the EXT menu button. Set A EXT SOURCE 1|2 to 1.
d. Press the A/B TRIG button to select the $B$ Trigger System (the B TRIG SOURCE menu will be displayed). Push the EXT menu button and set B EXT SOURCE 1|2 to 1. Press the A/B TRIG button to return to the $A$ Trigger System.
e. Adjust the generator's output frequency to the first Test Frequency setting specified in Table 4-4.
f. Set the A SEC/DIV control to the setting used with that Test Frequency.
g. Set the CH 1 VOLTS/DIV control to the setting used with that Test Frequency setting.
h. Select TRIGGER CPLG to display the A COUPLING menu.

## NOTE

The Minimum Signal Levels for Triggering for EXT TRIG $\div 5$ are $5 \times$ the levels that are listed in Table 4-4. This procedure obtains the 5 X levels by removing a 5X Attenuator from the test setup after setting the generator's output level as specified in Table 4-4.
i. Set the output amplitude of the specified Test Frequency to the level given in Table 4-4 for the A Trigger System with DC Trigger Coupling.

## NOTE

When checking for triggers in part $j$, use the TRIGGER LEVEL control to trigger (or to attempt to trigger) on the waveform.
j. CHECK - For a stable, triggered display at the DC trigger coupling setting. Press TRIGGER SLOPE to check for both + and - slopes.
k. Remove the 5X Attenuator from the test setup and reconnect the setup.
I. Set CH 1 VOLTS/DIV for an on-screen display.

## Performance Check and Functional Verification Procedure

## 2440 Service

m. Select TRIGGER SOURCE and push the EXT menu button. Set A and B EXT GAIN to EXT $1 \div 5$ on in the menu displayed.
n. Select TRIGGER CPLG and repeat part $j$ to check $A$ EXT $1 \div 5$ coupling.

Table 4-4
Minimum Signal Level for EXT1 or EXT2 Triggering (in millivolts)

| Trigger System | Test Frequency | VOLTS DIV/ Setting | $\begin{aligned} & \text { SEC/ } \\ & \text { DIV } \\ & \text { Setting } \end{aligned}$ | TRIGGER COUPLING |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | DC | AC | NOISE REJ | HF REJ | LF REJ |
| A | 60 Hz | 5 mV | 10 ms | 17.5 | 17.5 | a | a | $(17.5)^{\text {b }}$ |
| B | 60 Hz | 5 mV | 10 ms | 35.0 | 35.0 | a | 2 | (35.0) ${ }^{\text {b }}$ |
| A | 30 kHz | 5 mV | $20 \mu \mathrm{~s}$ | 17.5 | 17.5 | a | 25 | a |
| B | 30 kHz | 5 mV | $20 \mu \mathrm{~s}$ | 35.0 | 35.0 | a | 50 | a |
| A | 80 kHz | 10 mV | $10 \mu \mathrm{~s}$ | 17.5 | 17.5 | ${ }^{2}$ | a | 25 |
| B | 80 kHz | 10 mV | $10 \mu \mathrm{~s}$ | 35.0 | 35.0 | 2 | , | 50 |
| A | 50 kHz | 10 mV | 20 ns | 17.5 | 17.5 | 60 | $(60)^{\text {b }}$ | 25 |
| B | 50 MHz | 10 mV | 20 ns | 35.0 | 35.0 | 120 | (120) ${ }^{\text {b }}$ | 50 |
| A | $300 \mathrm{MHz}^{\text {c }}$ | 50 mv | 2 ns | 50.0 | 50.0 | 150 | $(150)^{\text {b }}$ | 50 |
| B | $300 \mathrm{MHz}^{\text {c }}$ | 50 mV | 2 ns | 100.0 | 100.0 | 300 | $(300)^{\text {b }}$ | 100 |

${ }^{*}$ Not necessary to check.
${ }^{\text {b }}$ Not triggered at specified amplitude.
${ }^{\text {© At frequencles above }} 100 \mathrm{MHz}$, It may be necessary to adjust the LEVEL control for a stable trigger and to make the display visible.
o. If trigger sensitivity was near the specified limits for the EXT 1 or EXT $1 \div 5$ sources with the trigger coupling set to DC on, repeat parts $i$ through $n$ for all other coupling settings in that test frequency row, changing the trigger coupling settings and generator amplitude as required.
p. Set the generator's output to the next Test Frequency in Table 4-4.
q. Select TRIGGER SOURCE and push the EXT menu button. Set A and B EXT GAIN back to EXT 1 in the menu displayed. Reinstall the 5X Attenuator in the test setup.
r. Repeat parts $f$ through $q$ to check the trigger sensitivity for each test frequency in Table 4-4. Use the Function Generator for frequencies below 50 MHz . Change generators (as specified in part b) as needed to obtain the test frequency required.
s. Move the leg of the Dual-Input-Connector connected to the EXT 1 input to the EXT 2 input.
t. Select TRIGGER SOURCE and push the EXT menu button. Set the A EXT SOURCE 1|2 TO 2, Select TRIGGER COUPLING.
u. Repeat parts e through $r$ to check the EXT 2 trigger source, setting EXT $2 \div 5$ and EXT 2 in parts $m$ and $q$, respectively.
v. Select TRIGGER SOURCE and set VERT on (the VERT source will ensure that the A Acquisition System is stably triggered-required for the following B Trigger checks).
w. Press A/B TRIG to select the B Trigger System and set the HORIZONTAL MODE to $B$.
x. Repeat parts $b$ to $u$ to check B Trigger System sensitivity. Use generator amplitude levels in the TRIGGER SYSTEM-B rows for checking the B Trigger sensitivity.

## NOTE

When checking 50 MHz and 300 MHz Triggers for the B TRIGGER SYSTEM, the REPET mode acquisitions can require a long time to complete. When setting the B SECIDIV control for those TEST FREQUENCIES, set the HORIZONTAL MODE to A and set the A SEC/DIV control to the SEC/DIV setting specified in the table. This adjustment will set BOTH A and B Acquisition Systems to the specified SEC/DIV setting and reduce the time necessary to complete the B REPET acquisition sequence. Set the HORIZONTAL MODE back to B.
y. Disconnect the test setup.

## 3. Check A*B Trigger Source.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

| Set: | A SEC/DIV | $10 \mu \mathrm{~s}$ |
| :--- | :--- | :--- |
| Select: | TRIGGER MODE |  |
| Set: | AUTO | On |
| Select: | TRIGGER SOURCE |  |
| Set: | A*B\|WORD | A*B |

Press: A/B TRIG to display the B TRIG SOURCE menu.
Set: CHAN 1/2
2
b. Ensure that the B Trigger Level Readout is set to 0.0 V . Adjust if necessary using the TRIGGER LEVEL control.
c. Press the A/B TRIG button to select the A Trigger System.
d. Select VERTICAL MODE and set CH 20 ff .
e. Connect the output of a Leveled Sine-wave Generator through a $50 \Omega$ Coaxial Cable and a Dual-Input Coupler to the CH 1 OR $X$ and CH 2 OR Y input connectors. Do not use a Termination.
f. Set the generator's frequency to 50 kHz and its amplitude for a 4-division display.
g. Use the TRIGGER LEVEL control to adjust the A Trigger Level Readout while performing parts $h$ through $n$.
h. VERIFY - That for Trigger Level Readout settings of approximately $\leq 0 \mathrm{~V}$, the display is stably triggered with the Trigger indicator (a small "T") approximately centered vertically on the waveform.
i. VERIFY - That for Trigger Level settings between approximately 0 V and 200 mV , the display is stably triggered and the Trigger Indicator moves along the upper-positive going slope of the waveform.
j. VERIFY - That for settings greater (more positive) than approximately 200 mV , the display is not triggered (free-runs). Press A/B TRIG to select the B Trigger System and set SLOPE to - (negative).
k. Press A/B TRIG to select the A Trigger System and set SLOPE to - (negative).
I. VERIFY - That for Trigger Level Readout settings of approximately $\geq 0 \mathrm{~V}$ or more, the display is stably triggered with the Trigger indicator approximately centered vertically on the waveform.
m. VERIFY - That for Trigger Level settings between approximately 0 mV and -200 mV the display is stably triggered and the Trigger Indicator moves along the lower-negative going slope of the waveform.
n. VERIFY - That for settings which are less (more negative) than approximately 200 mV the display is not triggered (free-runs).
0. Set the A Trigger Level Readout for a reading of 0.0 V and SLOPE to + (positive).
p. Press A/B TRIG to select the B Trigger System and set SLOPE to + (positive).
q. Repeat parts $h$ through o to verify the B Trigger System as a source for the A*B composite trigger. Do NOT change the HORIZONTAL MODE to B. Note that the Trigger Level Readout will Indicate B Trigger Level settings for parts $h$ through $o$ and that performance of part j will select the A Trigger System, while part $k$ will select the B Trigger System.
r. Disconnect the test setup.
4. Verlfy the Normal and Single Sequence Trigger Functions.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE
Set: CH $2 \ldots . . . . . . . . . . . . .$. . . Off
Set: A SEC/DIV ............... . . $10 \mu \mathrm{~s}$
b. Connect the Leveled Sine-wave Generator output to the CH 1 OR X input connector through a $50 \Omega$ Coaxial Cable.
c. Set the generator's frequency and amplitude for a $50 \mathrm{kHz}, 4$-division display.
d. Select TRIGGER MODE and set NORMAL on.
e. Using the TRIGGER LEVEL control, VERIFY that the display can be triggered on the positive going slope of the AC waveform for the + (plus) selection of the SLOPE button and on the negative going slope for the (minus) selection of the SLOPE button.
f. VERIFY - That for TRIGGER LEVEL settings outside the range of the display (approximately $\pm 200 \mathrm{mV}$ ), the acquisition stops and the waveform is saved on screen.
g. Trigger the display and set SINGLE SEQUENCE on.
h. VERIFY - That for each press of the STORAGE ACQUIRE button, a waveform is acquired and saved on screen.
i. Disconnect the test setup.

## 5. Check Trigger Noise Rejection.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE

| Set: | CH 2 | Off |
| :--- | :--- | :--- |
| Set: | A SEC/DIV | $10 \mu \mathrm{~s}$ |

b. Connect the sine wave output of the Function Generator through a $50 \Omega$ Coaxial Cable to the CH 1 ORX input connector.
C. Set the Function Generator's frequency to 50 kHz and its amplitude for a 4-division display.
d. Change the CH 1 VOLTS/DIV to 1 V (yieids a 0.4 -division display).
e. Select TRIGGER COUPLING and set NOISE REJECT on.
f. CHECK - For a non-triggered, free-running display for both the + (positive) and - (negative) settings of the SLOPE button.
g. Set the A COUPLING menu back to DC on.
h. Press the A/B TRIG button to select the $B$ Trigger System (the B COUPLING menu will be displayed) and set the HORIZONTAL MODE to B.
i. Set the B COUPLING menu to NOISE REJECT on.
j. CHECK - That the display cannot be stably triggered with the TRIGGER LEVEL control for either positive or negative setting of the SLOPE button.
k. Set the B COUPLING menu to DC on and disconnect the test setup.
6. Check Slope Selection and Verify Line Trigger.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE
Set: CH 2 Off
Select: CH 1 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
Set: CH 1 VOLTS/DIV 5 V
A SEC/DIV 5 ms
Select: TRIGGER SOURCE
Set: LINE On

## WARNING

DO NOT connect the 10X Probe ground lead to the AC (line) power source when performing this step.
b. Connect a 10X Probe to the CH 1 OR X input connector and connect the 10X Probe tip to an AC (line) source.
c. Using the TRIGGER LEVEL control, VERIFY that the display can be triggered on the positive going slope of the AC waveform for the + (plus) selection of the SLOPE button and on the negative going slope for the (minus) selection of the SLOPE button.

NOTE
The Trigger Point Indicator, a small "T" riding on the displayed waveform, indicates the point on which the instrument is triggered for the displayed waveform.
d. Disconnect the test setup.
7. Verify A and B Trigger Position Function.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE
Set: CH 2 Off
Set: CH 1 VOLTS/DIV iv
b. Connect the MARKER OUT signal of the Time Mark Generator to the CH 1 OR X input connector through a $50 \Omega$ Coaxial Cable.
c. Set the Time Mark Generator's marker period to 1 ms .
d. Position the start of the display to the extreme left graticule line using the HORIZONTAL POSITION control.
e. Select TRIG POSITION and set $1 / 8$ on.
f. VERIFY - That the Trigger Point Indicator (a "T" symbol) is positioned on a time marker approximately 2.5 divisions to the right of the extreme left graticule line.
g. Set the TRIGGER POSITION menu to $1 / 4$ and verify that the Trigger Point Indicator moves to a time marker that is approximately at center screen.
h. Use the HORIZONTAL POSITION control to position the time marker with superimposed Trigger Point Indicator to the extreme left graticule line.
i. Set the TRIGGER POSITION menu to $1 / 2$ and verify that the Trigger Point Indicator moves to a time marker that is approximately at center screen

1. Use the HORIZONTAL POSITION control to position the time marker with superimposed Trigger Point Indicator to the extreme left graticule line.
k. Set the TRIGGER POSITION menu to $3 / 4$ and verify that the Trigger Point Indicator moves to a time marker that is approximately at center screen.
2. Set the TRIGGER POSITION menu to $7 / 8$ and verify that the Trigger Point Indicator is positioned on a time marker approximately 2.5 divisions to the right of the center graticule line.
m. Press A/B TRIG to select the B Trigger System and set the HORIZONTAL mode to B. Use the TRIGGER LEVEL control to trigger the display as required.
n. Repeat parts $d$ through $k$ to check the B TRIGGER POSITION function.
o. Disconnect the test setup.

## HORIZONTAL SYSTEM

## Equipment Required (see table 4-1)

Time-Mark Generator (Item 4)
$50 \Omega$ Coaxial Cable (Qty 2) (Item 10)
$50 \Omega$ Precision Coaxial Cable (Item 11)
$50 \Omega$ Termination (Item 12)

1. Check Cursor Readout Accuracies for the A and B Acquisition Systems.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the frontpanel setup:

Set: CH 1 VOLTS/DIV 1 V
Set: CH 2 VOLTS/DIV 2 V
Select: CURSOR FUNCTION
Set: TIME
On
b. Use the CURSOR/DELAY control to align the movable cursor (it will have more dots than the alternate cursor) to the third graticule line to the left of center screen.
c. Press CURSOR SELECT to enable the alternate cursor.
d. Use the CURSOR/DELAY control to align cursor to the third graticule line to the right of center screen.
e. CHECK - That the Cursor Time Readout indicates 2.9700 to 3.0300 ms .
f. Set the HORIZONTAL MODE to B.
g. CHECK - That the Cursor Time Readout indicates 2.9700 to 3.0300 ms .
2. Verity the Sample Rate of the $A$ and $B$ Acquisition Systems and Check the Horizontal Display Accuracy.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the frontpanel setup:

Select: VERTICAL MODE

| Set: | CH 2 | Off |
| :--- | :--- | :--- |
| Set: | CH 1 VOLTS/DIV | 500 mV |
|  | A SEC/DIV | 100 ns |
|  | A/B TRIG | $B$ |

b. Select TRIGGER MODE and set RUNS AFTER on. Set A/B TRIG to $A$.
c. Connect the MARKER OUT signal of a Time Mark Generator to the CH 1 OR X input connector through a $50 \Omega$ Coaxial Cable. Do not use a Termination.
d. Set the Time Mark Generator's marker period to $0.1 \mu \mathrm{~s}$.
e. Push INIT @ $50 \%$ to set the A Trigger level.
f. VERIFY - That one time marker per horizontal division is displayed.
g. CHECK - That the spacing between the time markers nearest the third and ninth vertical graticule lines is 6 divisions, $\pm 0.06$ division.
h. Set HORIZONTAL MODE to B and set the B SEC/DIV control to 100 ns .
i. VERIFY - That one marker per horizontal division is displayed.
j. CHECK - That the spacing between the time markers nearest the third and ninth vertical graticule lines is 6 divisions, $\pm 0.06$ division.
k. Rotate the $A$ and $B$ SEC/DIV control counter-clockwise one position to set both acquisition systems one speed slower.
I. Set the Time Mark Generator's marker period to match the acquisition rate set in the last part.
m. VERIFY - That one marker per horizontal graticule line is displayed.
n. CHECK - That the spacing between the time markers nearest the third and ninth vertical graticule lines is 6 divisions, $\pm 0.06$ division.
o. Set HORIZONTAL MODE to A.
p. VERIFY - That one marker per horizontal division is displayed.
q. CHECK - That the spacing between the time markers nearest the third and ninth vertical graticule lines is 6 divisions, $\pm 0.06$ division.
r. Set HORIZONTAL MODE to B.
s. Repeat parts j through $q$ to verify all A and B acquisition rate settings down to 500 ms .
t. Disconnect the test setup.
3. Verify the DELAY TIME and $\triangle$ DELAY TIME Functions, Check $\triangle$ DELAY TIME Resolution, and Check Accuracy of the Time-Base Reference (using the $\triangle$ DELAY TIME function).
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the frontpanel setup:

## Select: VERTICAL MODE

| Set: | CH 2 | Off |
| :--- | :--- | :--- |
| Set: | CH 1 VOLTS/DIV | 500 mV |
|  | A SEC/DIV | $20 \mu \mathrm{~s}$ |
|  | HORIZONTAL MODE | A INTEN |
|  | B SEC/DIV | 500 ns |
|  | A/B TRIG | B |

b. Select TRIGGER MODE and set RUNS AFTER on. Set A/B TRIG to A.
c. Use the HORIZONTAL POSITION control to align the Trigger Point Indicator (a small "T" on the displayed trace) to the vertical graticule line 3 divisions left of center screen.
d. Connect the MARKER OUT signal of a Time Mark Generator to the CH 1 OR X input connector through a $50 \Omega$ Coaxial Cable. Do not use a Termination.
e. Set the Time Mark Generator's marker period to $20 \mu \mathrm{~s}$. Vertically position the bottom of the CH 1 display to 1 division below center screen.
f. Select DELAY TIME and use the CURSOR/DELAY control to adjust the DELAY TIME Readout for a reading of $120.00 \mu \mathrm{~s}$.
g. VERIFY - That the intensified zone is on the time marker that is 3 divisions right of center screen.
h. Set the HORIZONTAL MODE to B. VERIFY - the B Trigger Point Indicator is on the rising edge of the displayed time marker.
i. Set the HORIZONTAL MODE to A INTEN and use the HORIZONTAL POSITION control to position the A Trigger Point Indicator to the graticule line 4 divisions left of center screen.
j. Use the CURSOR/DELAY control to adjust the DELAY TIME Readout for a reading of $20.00 \mu \mathrm{~s}$ (the intensified zone will be aligned to the time marker 3 divisions left of center screen).
k. Press the $\Delta$ TIME ON|OFF menu button to set $\triangle$ TIME ON.
I. Using the CURSOR/DELAY control, adjust the $\Delta$ DELAY TIME Readout for a reading of $120.00 \mu \mathrm{~s}$.
m. VERIFY - That the $\triangle$ DELAY intensified zone is on the marker 3 divisions right of center screen.
n. Slightly rotate the CURSOR/DELAY control to increase the $\triangle$ DELAY TIME reading the least amount possible.
o. CHECK - That the readout can be advanced in increments at least as small as $0.04 \mu \mathrm{~s}$.

## Performance Check and Functional Verification Procedure

 2440 Servicep. Rotate the CURSOR/DELAY control to set the $\triangle$ DELAY TIME readout to $500 \mu \mathrm{~s}$.
q. Set the HORIZONTAL MODE to $B$, then set the B SEC/DIV control to 5 ns .
r. Use the HORIZONTAL POSITION control to align the two Trigger Point Indicators to the center vertical graticule line.
s. CHECK - That the two time markers displayed are not horizontally separated by more than 1.5 divisions at the points where their rising edges cross the center horizontal graticule line.
t. Disconnect the test setup.
4. Verify the DELAY EVENTS function.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the frontpanel setup:

Select: CH 2 COUPLING/INVERT

| Set: | $50 \Omega$ ON/OFF | OFF |
| :--- | :--- | :--- |
| Set: | CH 1 VOLTS/DIV | 1 V |
|  | CH 2 VOLTS/DIV | 2 V |
|  | A SEC/DIV | 5 ms |
|  | A/B TRIG | $B$ |

b. Select TRIGGER MODE and set RUNS AFTER on.
c. Connect the MARKER OUT signal of a Time Mark Generator to the CH 1 OR X input connector through a $50 \Omega$ Coaxial Cable. Do not use a Termination.
d. Set the Time Mark Generator's marker period to 5 ms .
e. Connect the A TRIGGER OUTPUT (TTL) at the scope's rear panel to the CH 2 OR Y input connector with a $50 \Omega$ Coaxial Cable. Do not use a Termination.
f. Use the VERTICAL POSITION controls to position the CH 1 and CH 2 displays for easy viewing.
g. Select TRIGGER SOURCE and push the EXT menu button.
h. Set B EXT SOURCE 1|2 to 1. Press the A/B TRIG button to return to the $A$ Trigger System.
i. Connect the output of a Leveled Sine-Wave Generator to the EXT TRIG 1 input via a $50 \Omega$ Precision Coaxial Cable and a $50 \Omega$ Termination.
j. Set the Leveled Sine-Wave Generator's amplitude to 3 V and its frequency to 2 MHz .
k. Set the HORIZONTAL MODE to B and set the B SEC/DIV control to $50 \mu \mathrm{~s}$.
I. Use the HORIZONTAL POSITION control to align the Trigger Point Indicators to the graticule line 3 divisions right of center screen.
m. Set the HORIZONTAL MODE to A.
n. Select DELAY EVENTS and set EVENTS ON|OFF to ON. Use the CURSOR/DELAY control to set the EVENTS COUNT to 60001 B TRIGS $(60,001)$.
0. VERIFY - That the falling edge of the A Trigger signal displayed in CH 2 Is 3 divisions left of center screen.
p. Set the HORIZONTAL MODE to B.
q. VERIFY - That the rising edge of the displayed time marker can be aligned to the Trigger Point Indicator approximately 3 divisions right of center screen using the CURSOR/DELAY control.
r. Disconnect test setup.

## ADDITIONAL VERIFICATIONS AND CHECKS

```
Equipment Required (see table 4-1)
    Calibration Generator (Item 3)
    Digital Voltmeter (DMM) (Item 7)
    GPIB Controllera
    GPIB Cable (Item 9)
    50\Omega Coaxial Cable (Qty 2) (Item 10)
    50\Omega Termination (Item 12)
    10X Attenuator (Qty 2) (Item 13)
    1X Probe (Item 17)
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Dual-Input Coupler (18)
BNC Female-to-Dual Banana Adapter (Item 19)
Sine-Wave Oscillator (Item 20)
Pulse Generator (Item 21)
Sync and Linearity Test Generator (Item 22)
$75 \Omega$ Coaxial Cable (Qty 2) (Item 23)
$75 \Omega$ Termination (Qty 2) (Item 24)

Due to the variety of user's equipment capable of controlling the GPIB, a specific controller is not specified.

1. Check Galn Match Between NORMAL and Save Acquisition Modes.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: CH 1 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
Select: STORAGE ACQUIRE
Set: AVG On
Select: VERTICAL MODE
Set: $\quad \mathrm{CH}_{2}$
OHf
b. Connect the Calibration Generator's STD AMPLITUDE output to the CH 1 OR X input connector through a $50 \Omega$ Coaxial Cable. Do not use a Termination. Set the Calibration Generator's output level to 0.5 V and center the displayed square wave on screen.
c. Select CURSOR FUNCTION and set VOLTS on.
d. Using the CURSOR/DELAY control, align the enabled cursor (segmented) to the top of the displayed square wave.
e. Press CURSOR SELECT to enable the alternate cursor (it will change from solid to segmented). Align the cursor to the bottom of the square wave.
f. Note the CURSOR VOLTS readout value.
g. Select STORAGE SAVE to save the display. Realign the cursors to the saved square wave if required.
h. CHECK - That the CURSOR VOLTS readout value is within 12 mV of the value noted in part f .
i. Disconnect the test setup.
2. Verify the Cursor Units and Functions.

## note

This check VERIFIES the functionality of the cursors. The accuracy of the cursor readout is checked in the Vertical and Horizontal Systems subsections of this procedure.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE
Set: CH 2 Off
Select: CH 1 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
Select: tRIGGER MODE
Set: AUTO On
Select: CURSOR FUNCTION
Set: TIME On
b. Use the CURSOR DELAY control to align the enabled time cursor to the vertical graticule line 2 divisions left of center screen.
c. Press the CURSOR SELECT button to enable the alternate cursor (realign the Trigger Point Indicator (small "T") to center screen if necessary) and align it to the graticule line 2 divisions right of center screen.
d. VERIFY - That the cursor readout indicates approximately 2.00 ms .
e. Select CURSOR UNITS and set $\triangle \mid$ ABS to ABS. VERIFY - That the cursor readout indicates approximately 1.00 ms .
f. Return $\Delta \mid$ ABS to $\Delta$ and set DEGREES on. Press the NEW REF menu button.
g. VERIFY - That the cursor readout indicates approximately $360.00^{\circ}$ and that TIME CURSOR REF = indicates approximately 2.00 ms .
h. Set $\Delta \mid$ ABS to ABS. VERIFY - That the cursor readout indicates approximately $180.00^{\circ}$.
i. Set \% on. VERIFY - That the cursor readout indicates approximately $50.00 \%$.
j. Set SEC on and $\Delta \mid$ ABS to $\Delta$.
k. Select CURSOR FUNCTION and set 1/TIME on. VERI-FY-That the cursor readout indicates approximately 500.00 Hz .
I. Set VOLTS on. Select CURSOR UNITS and set dB on.
m . Use the CURSOR DELAY control to align one volt cursor to the graticule line 2 divisions above center screen and the other volt cursor to the line 2 divisions below center screen. Use the CURSOR SELECT button to toggle between cursors.
n. Press the NEW REF menu button. VERIFY-That the cursor readout indicates 0.0 dB .
0. Align the enabled cursor to the center horizontal graticule line. VERIFY - That the cursor readout indicates approximately -6.00 dB .
p. Connect the CALIBRATOR signal to the CH 1 OR X input connector through a 1X Probe.
q. Vertically center the display (do not position horizontally). Use the TRIGGER LEVEL control to trigger the display.
r. Set the CURSOR UNITS menu to VOLTS and select the CURSOR FUNCTION menu. Set V@T on.
s. Position one time cursor to 1 division left of center screen; position the other time cursor to 1 division right of center screen. VERIFY - That the cursor readout indicates approximately 400.00 mV .
t. Set the CURSOR FUNCTION menu to SLOPE. VERI-FY-That the cursor readout indicates approximately $400.00 \mathrm{~V} / \mathrm{s}$.
u. Disconnect test setup.

## 3. Verlfy STORAGE SAVE Functions.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: TRIGGER MODE
Set: AUTO On
b. Use the VERTICAL POSITION controls to position the CH 1 trace 2 divisions above graticule center and the CH 2 trace 2 divisions below graticule center.
c. Select VERTICAL MODE and set ADD on (ADD trace will be at graticule center).
d. Select STORAGE SAVE and press the menu button labeled CH 1 (the menu will change from SAVEREF SOURCE to SAVEREF DESTINATION).
e. Press the menu button labeled REF1 (the menu will change back to SAVEREF SOURCE). Press CH 2, REF2, ADD, REF3, REF, REF1, and REF4 in that order (menu will change for each button push) to store CH 2 in REF2, ADD in REF3, and REF1 in REF4.
f. Select VERTICAL MODE and set CH 1, CH 2, and ADD off.
g. Select STORAGE DISPLAY REF and press the REF1, REF2, and REF3 buttons. VERIFY - That the REF1 trace is displayed 2 divisions above, the REF2 trace 2 divisions below, and the REF3 trace at center screen.
h. Press the HORIZ POS REF menu button (menu will change) and set REF1P on for the displayed menu. VERIFY - That the HORIZONTAL POSITION control can position the REF1 trace horizontally. Repeat verification for REF2 and REF3.
i. Set REF HPOS REF|LOCK to LOCK. VERIFY - That the HORIZONTAL POSITION control now positions all displayed REF traces simultaneously.
j. Press the STORAGE DISPLAY REF menu button to return to that menu. Set REF1 off and REF4 on. VERIFY - That the REF4 trace replaces the REF1 trace.

## 4. Verify Auto Setup.

## NOTE

In this step, certain parts will require that you do an Auto Setup on a waveform to verify specific, although approximate, values for amplitude and time-related waveform characteristics. These values are specific to the waveform that Auto Setup was performed on, which was deliberately chosen due to its amplitude, DC offset, and timing characteristics. Therefore, do NOT expect Auto Setup to return the same values for waveforms with different characteristics. Waveforms with different characteristics may require changes to the VOLTSIDIV and SEC/DIV settings in Auto Setup to size the waveform on screen, thereby yielding different amplitudes, periods, pulse widths, etc. on screen.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Set: A SEC/DIV $20 \mu s$
Select: VERTICAL MODE
Set: CH 2 Off
b. Connect the output of the Pulse Generator to the CH 1 ORX input connector through a $50 \Omega$ Coaxial Cable, followed by a 10X Attenuator.
c. Set the Pulse Generator's output for a $\mathbf{5 0 0} \mathbf{~ m V}$ pk-pk amplitude with the peak levels $\pm 250 \mathrm{mV}$ around the ground-reference indicator. (The ground-reference indicator is a small " + " at the left side of the screen).
d. Set the Pulse Generator period for $100 \mu \mathrm{~s}$ ( 5 divisions) and the pulse duration (positive duration) for approximately $25 \mu \mathrm{~s}$ ( 1.25 divisions).

## NOTE

At this point, you should have a rectangular waveform with a $25 \%$ duty cycle (1/4 of the time HI, 3/4 of the time LO) centered vertically on screen. (That is, its peaks should be equidistant from the center horizontal graticule line while its ground-reference indicator (" + ") should be aligned to that same line.
e. Vertically position the waveform so that the ground-reference indicator (" + ") is 2 divisions below the center horizontal graticule line. Then set the CH 1 VOLTS/DIV to $\mathbf{2 0 ~ m V}$, so that the waveform is no longer contained vertically on screen.

## Performance Check and Functional Verlfication Procedure 2440 Service

f. Push the front-panel button labeled AUTO to do an Auto Setup on the input waveform for CH 1.
g. VERIFY - That the scope displays the Auto Setup menu and the message "AUTOSETUP WORKING: PLEASE WAIT" as it acquires information about the CH 1 waveform.
h. VERIFY - That the Auto Setup mode is VIEW (from the recalled front-panel setup).
i. VERIFY (after the message is removed) - That the ground-reference indicator for the waveform (" + ") is approximately aligned to the horizontal graticule line at center screen, and that the entire waveform is contained vertically within the graticule area. (The trigger point indicator, a small " $T$ " riding on the waveform, should be approximately at horizontal center screen.)
J. Vertically reposition the ground-reference indicator to 2 divisions below the center horizontal graticule line, then return the CH 1 VOLTS/DIV to 20 mV (same set up as part e).
k. Select VERTICAL MODE and set CH 2 on. Then, disconnect the test setup at CH 1 and reconnect the Pulse Generator to both CH 1 OR X and CH 2 OR Y input connectors through the $50 \Omega$ Coaxial Cable, followed by the 10X Attenuator, followed by a Dual-Input Coupler.

1. Now, position the ground-reference indicator for CH 2 to 2 divisions above the center horizontal graticule line; then set CH 2 VOLTS/DIV to 20 mV .
m. Push AUTO. VERIFY - That the scope scales both the CH 1 and CH 2 waveforms so that the CH 1 waveform is contained within the top half of the screen and the CH 2 waveform is contained within the bottom half. (Slightly adjust the vertical position knobs to see which is the CH 1 waveform and which is the CH 2 waveform.)
n. Set PERIOD on in the Auto Setup menu. VERIFY - That the menu entry RES HI|LO appears with the setting LO selected.
2. Disconnect the test setup at CH 1 ORX and $\mathrm{CH} 2 \mathrm{OR} Y$ input connectors, remove the Dual-Input Coupler from the setup, and reconnect the setup to the CH 1 OR X input connector. (Same connection as in part b.)
p. Select VERTICAL MODE and set CH 2 off.
q. Push the AUTO button. VERIFY - That between 1 and 2 cycles of the waveform are displayed on screen, with the amplitude contained within about $\pm 2.25$ divisions of center. (The amplitude is about 2.5 divisions for this particular input waveform.) The trigger-point indicator is near the beginning of the 20 -division waveform record, and the Trigger SLOPE is positive (" + ").
r. Set RES HI|LO to HI in the Auto Setup menu.
s. Push AUTO. VERIFY - That the waveform is displayed with higher vertical resolution (more amplitude than in part $q$, about 5 divisions for this particular input waveform) and that the amplitude is contained vertically on screen. Also verify that about 1-2 cycles is included in the ENTIRE 20-division waveform record. Use the HORIZONTAL POSITION control to view the entire waveform. The trigger-point indicator is near the beginning of the record; the Trigger SLOPE is positive (" + ").
t. Set RES HI|LO to LO and PULSE on in the Auto Setup menu.
u. Push AUTO. VERIFY - That the positive $1 / 4$-cycle of the waveform (that is, the pulse) is displayed on screen and that the amplitude is contained vertically within approximately $\pm \mathbf{2 . 2 5}$ divisions of center screen. (The amplitude is about 2.5 divisions for this particular input waveform.) The trigger-point indicator is near the beginning of the 20 -division waveform record, and the Trigger SLOPE is positive (" + ").
v. Set the A SEC/DIV to $20 \mu \mathrm{~s}$, then set the Pulse Generator to produce a COMPLEMENT pulse; that is, one with a negative $1 / 4$-cycle pulse duration.
w. Push AUTO. VERIFY - That the negative $1 / 4$-cycle of the waveform (in this case the pulse is negative-going) is displayed on screen and that the amplitude is contained vertically within approximately $\pm 2.25$ divisions of center screen. (The amplitude is about 2.5 divisions for this particular input waveform.) The trigger point indicator is near the beginning of the record; the Trigger SLOPE is negative ("-").
x. Set the RES HI|LO to HI.
y. Push AUTO. VERIFY - That the negative $1 / 4$-cycle of the waveform is displayed over about 10 of the 20 divisions in the waveform record, with the amplitude contained vertically on screen. (The amplitude is about 5 divisions for this particular input.) The trigger point indicator is near the beginning of the record; the Trigger SLOPE is negative ("-").
3. Set the RES HI|LO to LO and the EDGE کIL to 5 .
aa. Push AUTO. VERIFY - That the rising (positive-going) edge of the waveform is displayed on screen with the trigger-point indicator at center screen. (Waveform amplitude is about 2.5 divisions for this particular input waveform).
ab. Set EDGE $\sim \mid$ to
ac. Push AUTO. VERIFY - That the falling (negative-going) edge of the waveform is displayed on screen with the trigger-point at center screen. (The amplitude is about 2.5 divisions for this particular Input waveform).
ad. Set the RES HI|LO to HI.
ae. Push AUTO. VERIFY - That the falling (negative-going) edge of the waveform is displayed over about 10 of the 20 divisions in the waveform record with the same triggering as for RES LO setting. (The amplitude is about 5 divisions for this particular input waveform.)
af. Disconnect the test setup.

## 5. Verify MEASURE for SNAPSHOT and Continuous-Update Modes.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

Select: VERTICAL MODE
Set: CH 2 Off
Select: CH 1 COUPLING INVERT
Set: $\quad 50 \Omega$ ON|OFF Off
Select: CH 2 COUPLING INVERT
Set: $50 \Omega$ ON|OFF Off
b. Connect the STD OUTPUT of the Calibration Generator to the CH 1 OR X and CH 2 OR $Y$ input connectors via a $50 \Omega$ Coaxial Cable and a Dual-Input Coupler.
C. Set the output of the generator to 0.5 V .
d. Push AUTO to do an AUTO setup on the CH 1 waveform. Since AUTOsetup executed in VIEW mode, there should be several cycles of the square wave displayed on screen.
e. Set PERIOD on in the Auto Setup menu. Push AUTO.
f. Push MEASURE (next to PRGM, which is right of AUTO) to display that menu.
g. Select SETUP in the menu. Set METHOD to HIST and MARK ON|OFF to ON.
h. Push MEASURE again and select SNAPSHOT. VERIFY - That the SNAPSHOT menu is displaying values for 20 parameters approximately agreeing with the expected values. For instance, P-P (peak-to-peak) and TOP should be about 500 mV , and DUTY (duty cycle) should be about $50 \%$.
i. Set the Calibration Generator to 0.2 V .
j. Push INIT@50\% to set the A Trigger level.
k. Push menu item AGAIN. VERIFY - That SNAPSHOT readout updates the parameters ( $\mathrm{P}-\mathrm{P}$ and TOP are now about 200 mV ).

1. Select VERTICAL MODE and set CH 2 on. Set the CH 2 VOLT/DIV to the same setting as CH 1.
m. Push MEASURE and select SNAPSHOT. Push TARGET CH 2 in the menu displayed.
n. VERIFY - That the parameter values are now displayed for CH 2 (screens read "SNAPSHOT OF CH 2").
2. Select VERTICAL MODE and set CH 2 off.
p. Push MEASURE and set WINDOW ON IOFF to ON.
q. Select MEAS TYPE in the menu and use the direction arrows in the displayed menu to move the underline to PK-PK and press the ON button to display the parameter. Repeat for BASE, FREQ, and PERIOD. VERIFY - That as each is turned on the value displayed approximately agrees with the expected values ( $200 \mathrm{mV}, 0 \mathrm{~V}, 1 \mathrm{kHz}$, and 1 ms , respectively).
r. VERIFY - That two X's (MARKs) bracket one cycle of the squarewave to indicate where FREQ and PERIOD are being measured (MARKs are displayed for time measurements only).
s. Push CURSOR FUNCTION and set TIME on in the menu displayed.
t. Use the CURSOR/DELAY knob to adjust the active cursor to the center of one positive $1 / 2$-cycle of the waveform.
u. Push CURSOR SELECT to select the alternate cursor. Adjust it to the center of the following negative $1 / 2$-cycle of the waveform.
v. VERIFY - That the BASE and PK-PK values displayed are still approximately correct, but the values for FREQ and PERIOD are replaced with the message "NEED 3 EDGES".
w. Adjust the active cursor to the same $1 / 2$-cycle as the other cursor. VERIFY - That the PK-PK value drops to approximately 0 V .
$x$. Use the CURSOR/DELAY and SELECT controls to bracket slightly more than one cycle (3 EDGES) of the waveform. All 4 parameters should be as verified in part q.
y. Disconnect the test setup.

## Performance Check and Functional Verification Procedure

 2440 Service
## 6. Verify Operation of the AutoStep Sequencer.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the front-panel setup:

## Select: VERTICAL MODE

| Set: | CH 2 | Off |
| :--- | :--- | :--- |
| Set: | ASEC/DIV | 50 ms |
|  |  |  |
| Select: | TRIGGER MODE |  |
| Set: | AUTO | On |

b. Press the PRGM front-panel button. VERIFY - The AUTOSTEP SEQUENCER menu is displayed.
c. Press the SAVE menu button. This calls up a sub-menu for labeling the front-panel setup with a 1-6 character name so it can be recalled later.
d. VERIFY - That a sequence can be labeled and that label saved by doing the following:

Use the arrows under ROLL-CHARS to create a label (use TEST1) for the front-panel setup as outlined here in steps 1-3:

1. Select the first character for the label. Use the arrow-labeled buttons to select the first letter for the sequence label. Press the $\downarrow$ button to step forward in the alphabet and digits (0-9) and the $\dagger$ button to step backwards. Holding down the buttons moves through the characters continuously; a single press moves forward or backward one character. (There is a "blank space" character between the digit 9 and letter A.)
2. When you have displayed the letter for the first character of the label, push CURSOR $<>$ to move to the next character. Repeat part 1 to select the letter for the next character of your label.
3. Repeat the last step until "TEST1" is spelled out. (You can return to any character by continually pushing CURSOR $<>$, since it reverses the selection order after the first and sixth character is selected.)
e. Push menu button labeled SAVE when the label is complete.
f. VERIFY - That, when SAVE is pushed, the scope displays a message indicating "SEQUENCE TEST1 STEP $1^{\text {" }}$ and the remaining memory in percent.
g. Position the CH 1 trace to the graticule line 3 divisions above graticule center. Push PRGM to advance to sequencer step 1 actions.
h. VERIFY - That the SET STEP ACTIONS for Step 1 is displayed.
i. Use the arrow buttons to move the underline to the "<N>" following the ACTION called REPEAT. Push $Y \mid N$ to toggle the action to $Y$ (" $Y$ " stands for Yes or On).
j. Now move the underline to the ACTION called BELL, and turn BELL on (set to Y). Using the same procedure, turn PAUSE on also.
k. Push NEXT STEP. VERIFY - That the on-screen message indicates STEP 2.
I. Position the CH 1 trace to the graticule line 1 division above graticule center. Push PRGM to advance to sequencer step 2 actions.
m. VERIFY - That REPEAT, PAUSE, and BELL are the only actions on.
n. Push $Y \mid N$ to turn REPEAT off. Push NEXT STEP.
o. The message should now say STEP 3. Position the CH 1 trace to the graticule line 1 division below graticule center. Push PRGM to advance to sequencer step 3 actions.
p. VERIFY - That PAUSE and BELL are the only actions on. Push NEXT STEP to advance to sequencer step 4.
q. Position the CH 1 trace to the graticule line 3 divisions below graticule center. Push PRGM to advance to sequencer step 4 actions. PAUSE and BELL should be the only action on.
r. Push SAVE SEQ to save the sequence. VERIFY - That the main AUTOSTEP SEQUENCER menu is returned and the message "SEQUENCE SAVED" is displayed.
s. Push RECALL to display the menu for recalling sequences. VERIFY - That TEST1 appears in the list of CURRENT SEQUENCES.
t. Use the arrow buttons to move the underline (select) TEST1.
u. Push RECALL. VERIFY - That the BELL rings and the setup stored as step 1 is displayed. The CH 1 trace should be located 3 divisions above graticule center.
v. Push PRGM (front-panel button). VERIFY - That the BELL rings and the setup stored as step 2 is displayed. The CH 1 trace should be located 1 division above graticule center.
w. Push PRGM. VERIFY - That the BELL rings and the setup stored as step 3 is displayed. The CH 1 trace should be located 1 division below graticule center.
$x$. Push PRGM. VERIFY - That the BELL rings and the setup stored as step 4 is displayed. The CH 1 trace should be located 3 divisions below graticule center.
y. Push PRGM. VERIFY - That the BELL rings and the sequence loops back to display step 1 of the sequence.
z. Connect the STEP COMPLETE output BNC (located on rear panel) to the banana plug inputs of a Digital Voltmeter (DMM) via a $50 \Omega$ Coaxial Cable and a BNC Female-to-Dual Banana Adapter. When connecting the BNC Female-to-Dual Banana Adapter to the DMM, put the side with the bump marked "GND" to the LOW or ( - ) input jack.
aa. Set the DMM to the 20 DC VOLTS range. CHECK - That the DMM reading is $\leq 0.5 \mathrm{~V}$.
ab. Push PRGM to advance to sequence step 2. CHECKThat the DMM reading momentarily jumps to a level $\geq 2.5 \mathrm{~V}$ and $\leq 3.5 \mathrm{~V}$ before returning to the level measured in subpart aa.
ac. Move the $50 \Omega$ Coaxial Cable from the STEP COMPLETE output to the SEQUENCE OUT output BNC. CHECK - That the DMM reading is $\geq 2.5 \mathrm{~V}$ and $\leq 3.5 \mathrm{~V}$.
ad. Push PRGM once to advance to sequence step 3. Wait until step 3 is loaded and then push PRGM again to advance to step 4.
ae. CHECK - That the DMM reading is $\leq 0.5 \mathrm{~V}$.
af. Disconnect the $50 \Omega$ Coaxial Cable from the SEQUENCE OUT output BNC.
ag. Connect the square wave output of a generator (such as Item 19) capable of outputting nominal TTL levels to the SEQUENCE IN input BNC via a $50 \Omega$ Coaxial Cable. Set the output frequency of the generator to 10 Hz .
ah. VERIFY - That the scope continuously loops through sequencer steps 1 to 4 in response to the generator input.
ai. Disconnect the $50 \Omega$ Coaxial Cable from the SEQUENCE IN BNC.
aj. Push EXIT. VERIFY - That the RECALL menu is returned.
ak. Push EXIT. VERIFY - That the main AUTOSTEP SEQUENCER menu is returned.

## 7. GPIB Functionality Verification.

a. Press the instrument's POWER button twice to power the instrument OFF and then ON.
b. VERIFY - That all three GPIB STATUS lights illuminate during the instrument's power-up sequence.
c. VERIFY - The GPIB STATUS SRQ light is still illuminated when the power-up sequence is finished.
d. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the frontpanel setup:
e. Push SETUP OUTPUT (the button to the lower right of SEC/DIV control) and press the menu button labeled SETUP (menu will change).
f. Press the OUTPUT SETUP menu button labeled MODE to display that menu.
g. Set T/L on. VERIFY - That the ADDR light is off.
h. Set L/ONLY on. VERIFY - That the ADDR light is on.
i. Set T/ONLY on. VERIFY - That the ADDR light remains on.
j. Push SETUP OUTPUT and press the menu button labeled SETUP.
k. Press the OUTPUT SETUP menu button labeled MODE to display that menu.
I. Set T/L on.
m. Push SETUP OUTPUT and press the menu button labeled SETUP.
n. Press the menu button labeled ADDR to select that menu.
O. Press the menu button labeled $\dagger$ or $\downarrow$ to set the GPIB ADDRESS to 1. The $\dagger$ increments the address and the $\downarrow$ decrements it.
p. Press SETUP OUTPUT and press the menu button labeled SETUP. Press the menu button labeled TERM (menu will change).

## NOTE

At this point in this step, the use of a GPIB compatible Controller is necessary to send commands or queries over the GPIB to the 2440 and receive responses back from the 2440.

Due to the variety of controller types, the following parts of this step only give some examples of commands you can have your controller send to the 2440 over the GPIB Bus to verify the GPIB interface in this instrument.
q. Set either EOI or LF/EOI on accoring to the specification of the GPIB Controller.
r. Turn on the GPIB Controller and enter a program that can deliver commands and queries to, as well as receive response from, the scope. Below are some limited commands your program could perform using the GPIB controller:

1. Ask for the user to enter the 2440's GPIB address. (This was set to 1 in part o.)
2. Have the user send the command RQS ON.
3. Have the user send the command LOCK ON to verify the LOCK light illuminates. Next send the command LOCK OFF to the 2440 and verify that the LOCK light is extinguished,
4. Have the user send commands with the GPIB Controller to set up the front panel controls. Some examples are:
```
VMOde ADD:ON
CH1 VOLts:1,COUpling:GND, INVert:ON BWLimit TWEnty
```

5. Have the user send a query to the 2440 (i.e. VMOde?) to verify the 2440 sends back the response.

NOTE
Refer to the 2440 Programmers Reference Guide for sample programs for several different Controllers.
s. Connect the GPIB Controller to the oscilloscope's rear-panel GPIB CONNECTOR using the GPIB cable.
t. Run the program entered for subpart r .
u. After you have sent commands over the GPIB to the 2440, press STATUS to verify that the front panel STATUS readout indicates the control setting changes sent over the GPIB Controller.
v. Press the MENU OFF/EXTENDED FUNCTIONS button.
w. Disconnect the test setup.
8. Check A TRIGGER and RECORD TRIGGER Outputs for Loglc Polarity and Minimum HI/LO (50 $\Omega$ loads).
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITIAL SETUP" at the start of this procedure). Make the following changes to the frontpanel setup:

Select: CH 1 COUPLING/INVERT

| Set: | $50 \Omega$ ON\|OFF | OFF |
| :--- | :--- | :--- |
|  |  |  |
| Select: | CH 2 COUPLING/INVERT |  |
| Set: | $50 \Omega$ ON\|OFF | OFF |
| Set: | CH 1 VOLTS/DIV | 200 mV |
|  | CH 2 VOLTS/DIV | 200 mV |
| Select: | TRIGGER SOURCE |  |
| Set: | LINE | On |

b. Connect the RECORD TRIGGER OUTPUT (rear panel) to the CH 1 OR X input connector via a $50 \Omega$ Coaxial Cable and a $50 \Omega$ Termination.
c. Connect the A TRIGGER OUTPUT (rear panel) to the CH 2 OR Y input connector via a $50 \Omega$ Coaxial Cable and a $50 \Omega$ Termination.
d. Using the CH 1 and CH 2 VERTICAL POSITION controls, position the CH 1 waveform to the top-half of the screen and the CH 2 to the bottom-half for easy viewing.
e. CHECK - That both of the waveforms are displayed with their falling edges aligned to the Trigger Point Indicator (a small " T " riding on each waveform).
f. Select CURSORS FUNCTION and set VOLTS on.
g. Select CURSOR UNITS and set $\Delta \mid A B S$ to ABS.
h. Use the CURSOR/DELAY control to align the Voltage cursor to the top flat portion of the CH 1 waveform.
i. CHECK - That the Cursor Readout indicates a voltage $\geq 450 \mathrm{mV}$.
j. Align the Voltage cursor to the bottom flat portion of the CH 1 waveform.
k. CHECK - That the Cursor Readout indicates a voltage $\leq 150 \mathrm{mV}$.

1. Press the CURSOR FUNCTION button twice to display the Attach Cursors menu and set CH 2 on for the displayed menu.
m. Repeat parts $h$ through $k$, aligning the cursor to the CH 2 waveform instead of the CH 1.
n. Disconnect the test setups.

## 9. Check Square-Wave Flatness (Video Option 05 only).

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the frontpanel setup:

Select: CH 1 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
Select: CH 2 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF

| Set: | CH 1 VOLTS/DIV | 200 mV |
| :--- | :--- | :--- |
|  | CH 2 VOLTS/DIV | 50 mV |
|  | A SEC/DIV | 2 ms |

Select: VERTICAL MODE
Set: CH 2 Off
b. Connect the fast-rise, positive going square-wave output of the Calibration Generator to the CH 1 OR X input connector via a $50 \Omega$ Coaxial Cable and a $50 \Omega$ Termination. The square wave should step from - 1 V to 0 V .
c. Set the generator to produce a $60-\mathrm{Hz}$, five-division display and use the CH 1 POSITION control to center the display as required.
d. Set the CH 1 VOLTS/DIV control to 50 mV .
e. CHECK-Display front-corner aberrations are within 1\% ( 0.2 division or less). Exclude the first 20 ns Immediately following the positive going transition from the measurement.
f. Select VERTICAL MODE and set CH 2 and CH 1 off.
g. Move the $50 \Omega$ Coaxial Cable from the CH 1 OR X input connector to the CH 2 OR Y input connector.
h. CHECK-Display front-corner aberrations are within $1 \%$ ( 0.2 division or less). Exclude the first 20 ns immediately following the positive going transition from the measurement.
I. Set the CH 2 VOLTS/DIV control to 5 mV .
j. Install a 10X attenuator between the $50 \Omega$ Coaxial Cable and the $50 \Omega$ Termination, and reconnect the setup.
k. CHECK-Display front-corner aberrations are within 1\% ( 0.2 division or less). Exclude the first 20 ns immediately following the positive going transition from the measurement.
I. Select VERTICAL MODE and set the CH 2 VOLTS/DIV control to 50 mV , then set CH 1 on and CH 2 off.
m. Move the test setup from the $\mathrm{CH} 2 \mathrm{OR} Y$ input connector to the CH 1 OR X input connector. Set the CH 1 VOLTS/DIV control to 5 mV .
n. CHECK-Display front-corner aberrations are within 1\% ( 0.2 division or less). Exclude the first 20 ns immediately following the positive going transition from the measurement.
0. Set the CH 1 VOLTS/DIV control to 200 mV and set the A SEC/DIV control to $10 \mu \mathrm{~s}$.
p. Remove the 10X attenuator and reconnect the test setup.
q. Set the Calibration Generator to produce a $15-\mathrm{kHz}$, 5-division display.
r. Repeat parts d through $n$ to check square-wave flatness at 15 kHz .
s. Disconnect test setup.

## 10. Check Frequency Response Flatness (FULL and 20 MHz BANDWIDTH Modes) (VIdeo Option 05 only).

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step i in "INITIAL SETUP" at the start of this procedure). Make the following changes to the frontpanel setup:

Select: CH 1 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
Select: CH 2 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF

| Set: | CH 1 VOLTS/DIV | 10 mV |
| :--- | :--- | :--- |
|  | CH 2 VOLTS/DIV | 10 mV |
|  | A SEC/DIV | $20 \mu \mathrm{~s}$ |

Select: VERTICAL MODE
Set: CH 2 Off
Select: BANDWIDTH
Set: 20 MHz On
b. Connect the output of a Leveled Sine-Wave Generator to the CH 1 OR X input connector via a $50 \Omega$ Coaxial Cable, two 10X attenuators, and a $50 \Omega$ Termination.
C. Set the generator to produce a $50-\mathrm{kHz}$, five-division display.
d. Increase the generator output frequency to 5 MHz and set the A SEC/DIV control to 200 ns.
e. CHECK-Display amplitude is between 4.80 and 5.05 divisions.
f. Set the BANDWIDTH LIMIT menu to FULL. Set the A SEC/DIV control back to $20 \mu \mathrm{~s}$.
g. Repeat parts c and d .
h. CHECK-Display amplitude is between 4.95 and 5.05 divisions.
i. Increase the generator frequency to 10 MHz and set the A SEC/DIV control to 50 ns .
J. CHECK-Display amplitude is between 4.90 and 5.05 divisions.
k. Increase the generator frequency to 30 MHz and set the A SEC/DIV control to 20 ns.
I. CHECK-Display amplitude is between 4.85 and 5.10 divisions.
m. Set the CH 1 VOLTS/DIV control to 50 mV and the A SEC/DIV to $20 \mu \mathrm{~s}$. Set the BANDWIDTH LIMIT menu to 20 MHz .
n. Remove one of the 10X attenuators from the test setup.
o. Repeat parts c through I .
p. Set the CH 1 VOLTS/DIV control to 200 mV and the A SEC/DIV control to $20 \mu \mathrm{~s}$. Set the BANDWIDTH LIMIT menu to 20 MHz .
q. Remove the last 10X attenuator from the test setup.
r. Repeat parts $\mathbf{c}$ through I.
s. Move the $50 \Omega$ Coaxial Cable from the CH 1 OR X input connector to the CH 2 OR Y input connector. Insert the two 10X attenuators back into the test setup.
t. Select VERTICAL MODE and set CH 2 on and CH 1 off. Return the A SEC/DIV control to $20 \mu \mathrm{~s}$.
u. Select BANDWIDTH and set 20 MHz on.
v. Repeat parts c through r using the CH 2 VOLTS/DIV control.
w. Disconnect the test setup.

## 11. Check Video Back-Porch Clamp (CH 2 only) (Video Option 05 only).

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITAL SETUP" at the start of this procedure). Make the following changes to the frontpanel setup:

Select: CH 1 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF

Select: CH 2 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
Set: CH 1 VOLTS/DIV 500 mV
CH 2 VOLTS/DIV $\quad 50 \mathrm{mV}$
A SEC/DIV
5 ms
Select: TRIGGER SOURCE
Set: LINE
On
Select: BANDWIDTH
Set: 20 MHz On
b. Connect the output of the Sine-Wave Oscillator to the CH 2 OR Y input connector via a $75 \Omega$ Coaxial Cable.
c. Connect the composite sync output of a Video Sync Generator to the CH 1 ORX input connector via a $75 \Omega$ Coaxial Cable and a $75 \Omega$ Termination. Select VERTICAL MODE and set CH 1 off.
d. Set the Sine-Wave Oscillator to produce a $60-\mathrm{Hz}$, six-division display. Slightly adjust the output frequency of the oscillator to stabilize the $60-\mathrm{Hz}$ display.
e. Set the A SEC/DIV control to $100 \mu \mathrm{~s}$. Select TRIGGER SOURCE and set CHAN $1 \mid 2$ to 1.
f. Select SET VIDEO and set CLAMP ON |OFF to ON and TV LINE on.
g. CHECK - The amplitude of the sine wave is 1 division or less.

## NOTE

An easy method of checking the expanded $60 \cdot \mathrm{~Hz}$ sine wave's amplitude is to observe the vertical "jitter" of the top of the Trigger Point Indicator (a small " $T$ " riding on the sine wave). The top of the " $T$ " should not jitter more than 1 division.
h. Set the CH 1 VOLTS/DIV control to 100 mV and the A SEC/DIV control back to 5 ms .
i. Set CLAMP ON|OFF to OFF for the displayed menu. Select TRIGGER SOURCE and set LINE on.
j. Repeat parts d through g.
k. Set the CH 2 VOLTS/DIV control to 200 mV and the A SEC/DIV control back to 5 ms .
I. Set CLAMP ON|OFF to OFF for the displayed menu. Select TRIGGER SOURCE and set LINE on.
m. Repeat parts d through g.
n. Disconnect the test setup.

## 12. Check Back-Porch Clamp Reference (CH 2 only) (Video Option 05 only).

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITAL SETUP" at the start of this procedure). Make the following changes to the frontpanel setup:

## Select: VERTICAL MODE

Set: CH 1 Off
Set: CH 2 VOLTS/DIV 50 mV
ASEC/DIV $\quad 1 \mu s$
Select: BANDWIDTH
Set: 20 MHz On
Select: CH 2 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
b. Connect a $\mathbf{1 0 0 \%}$ modulated, composite video signal to the CH 2 OR Y input connector via a $75 \Omega$ Coaxlal Cable and a $75 \Omega$ Termination. Do NOT adjust the CH 2 POSITION control.
c. Select SET VIDEO and set CLAMP ON|OFF to ON.
d. CHECK - That the back-porch level is within 1 division of the center graticule line.
e. Disconnect the test setup.
13. Check Sync Separation ( $\pm$ SLOPE) Video Option 05 only).
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITAL SETUP" at the start of this procedure). Make the following changes to the frontpanel setup:

Select: VERTICAL MODE

| Set: | CH 2 | Off |
| :--- | :--- | :--- |
| Set: | CH 1 VOLTS/DIV | 50 mV |
|  | A SEC/DIV | $2 \mu \mathrm{~s}$ |
|  | TRIGGER SLOPE | - (Minus) |
| Select: | BANDWIDTH |  |
| Set: | 20 MHz | On |
| Select: | CH 1 COUPLING/INVERT |  |
| Set: $50 \Omega$ ON\|OFF | OFF |  |

b. Connect the square-wave output of a Pulse Generator to the CH 1 OR X input connector via a $50 \Omega$ Coaxial Cable and a $50 \Omega$ Termination.
c. Set the amplitude for a 3-division pulse, stepping negative from ground.
d. Use the HORIZONTAL POSITION control to position the Trigger Point Indicator (small " $T$ " riding on the waveform) to the vertical graticule line 4 divisions left of graticule center.
e. Adjust the generator's PERIOD control for a 7.5-division (approximately $15 \mu \mathrm{~s}$ ) period for the displayed square wave.
f. Adjust the generator's PULSE DURATION control until the negative going portion of the square wave is approximately 1 horizontal division in duration.
g. Switch the A SEC/DIV control to 500 ns .
h. Select CURSOR FUNCTION and set TIME on.
i. Use the CURSOR/DELAY control to align the left-most cursor to the falling edge of the negatlve going pulse (aligned to the graticule line in part d).
J. Press CURSOR SELECT to select the right-most cursor and adjust it for a readout of $2.000 \mu \mathrm{~s}$.
k. Adjust the generator's PULSE DURATION until the negative-going portion of the square wave is aligned to the two cursors (i.e. is equal to $2.000 \mu \mathrm{~s}$ ).
I. Select TRIGGER CPLG and set VIDEO on.
m. Select SET VIDEO and set TV LINE on.
n. Return the A SEC/DIV control to $2 \mu \mathrm{~s}$. Press CURSOR SELECT and use the CURSOR/DELAY control to realign the left-most cursor to the falling edge of the pulse.

## Performance Check and Functional Verification Procedure

 2440 Serviceo. Press CURSOR SELECT and use the CURSOR/DELAY control to adjust the right-most cursor for a readout value of $13.000 \mu \mathrm{~s}$.
p. Set the CH 1 VOLTS/DIV control to 200 mV .
q. Adjust the generator to reduce the PERIOD of the waveform. Reduce the period until the display is stably triggered, but any further decrease in period causes an unstable display.
r. CHECK - That the negative-going edge of the second negative pulse is located between the two cursors.
s. Adjust the generator to return the waveform PERIOD to 7.5 divisions.
t. Select CH 1 COUPLING/INVERT and set INVERT ON|OFF to ON. Switch TRIGGER SLOPE to + (plus).
u. Adjust the generator to reduce the PERIOD of the waveform. Reduce the period until the display is stably triggered, but any further decrease in period causes an unstable display.
v. CHECK - That the positive-going edge of the second negative puise is located between the two cursors.
w. Disconnect the test setup.

## 14. Check VIDEO Trigger Modes.

a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see step $i$ in "INITAL SETUP" at the start of this procedure). Make the following changes to the frontpanel setup:

Select: VERTICAL MODE
Set: CH 2 Of

| Set: | CH 1 VOLTS/DIV | 200 mV |
| :--- | :--- | :--- |
|  | A SEC/DIV | $100 \mu \mathrm{~s}$ |
|  | TRIGGER SLOPE | - (Minus) |

Select: BANDWIDTH
Set: 20 MHz On
Select: CH 1 COUPLING/INVERT
Set: $50 \Omega$ ON|OFF OFF
Select: TRIGGER CPLG
Set: VIDEO On
Select: SET VIDEO
Set: FIELD 1 On
b. Push the front-panel button labeled "MENU OFF/EXTENDED FUNCTIONS" twice to display the Extended Functions menu. Select SYSTEM and the menu will change. Select VIDEO OPT in the menu. Set TV SYS M|NON/M to M and CNT RST BOTH|F1 to F1.
c. Connect the composite sync output of a Sync Generator to the CH 1 OR X input connector via a $75 \Omega$ Coaxial Cable and a $75 \Omega$ Termination.

## NOTE

For NTSC composite sync input signals, the first field will have 263 lines, while the second field will have 262. The scope will display the line number in the extreme upper-right corner of the screen and the TVF (TV Field) number immediately to the right of the line number.
d. Adjust the TRIGGER LEVEL control for a line number reading of 1 and a field number reading of TVF1.
e. CHECK - That for the readout Trigger Point Indicator (a small "T" riding on the displayed waveform) Indicates the scope is triggered on the first line of field 1.
f. Rotate the TRIGGER LEVEL control slightly counterclockwise while performing the CHECK during the following part.
g. CHECK - That the readout indicates the highest line number of the previous field for the multi-field input signal. For example, using an NTSC signal, the readout should indicate "TVF2 262".
h. CHECK - That for the readout Trigger Point Indicator (a small " $T^{\text {" }}$ riding on the displayed waveform) indicates the scope is triggered on the last line of field 2.
i. Continue to rotate the TRIGGER LEVEL control counterclockwise while performing the CHECK during the following part.
j. CHECK - That the readout indicates progressively lower line numbers are being displayed for field 2 and that eventually the readout indicates the highest line number of the previous field for the multi-field input is being displayed. For example, using an NTSC signal, the readout should indicate "TVF1 263".
k. CHECK - That for the readout Trigger Point Indicator (a small "T" riding on the displayed waveform) indicates the scope is triggered on the last line of field 2.
I. Select SET VIDEO and set ALT on.
m. Use the TRIGGER LEVEL control to set the readout to "TVFLD 1", indicating that the first lines of both fields are displayed.
n. CHECK - That for the readout Trigger Point Indicator (a small "T" riding on the displayed waveform) indicates the scope is triggered on the first lines of both fields.

## Performance Check and Functional Verification Procedure

2440 Service

## NOTE

By switching A VIDEO COUPLING (SET VIDEO menu) between FIELD 1, FIELD 2, and ALT, it is easier to see which line for which field the scope is triggered on for ALT VIDEO COUPLING.
0. Rotate the TRIGGER LEVEL control slightly counterclockwise while performing the CHECK during the following part.
p. CHECK - That the readout indicates the highest line number common to both fields for the multi-field input signal. For example, using an NTSC signal, the readout should indicate "TVFLD 262".
q. CHECK - That for the readout Trigger Point Indicator (a small "T" riding on the displayed waveform) indicates the scope is triggered on the last line COMMON to both fields. See the NOTE following part $n$ above.
r. Push the front-panel button labeled "MENU OFF/EXTENDED FUNCTIONS" ${ }^{n}$ wice to display the Extended Functions menu. Select SYSTEM and the menu will change. Select VIDEO OPT in the menu. Set CNT RST BOTH|F1 to F1.
s. Select SET VIDEO and set to FIELD 1. Repeat parts d to $g$ to check that the line count displayed in step $e$ is "TVF1 1" (set in step d) and continues to "TVF2 525" in step g (set in step f).
t. Disconnect the test setup.

## 15. Verify Teksecure Erase Memory Function (For Instruments with Serial Numbers B011821 and above)

> CAUTION
> PERFORMANCE OF THIS STEP (15) IS OPTIONAL. If performed, it will erase from sequencer memory the Initial Setup established and stored at the beginning of this procedure. Any other sequences, stored reference waveforms, and waveforms saved on screen will be irretrievably lost.

This step uses the front panel to verify that the Teksecure Erase Memory feature erases sequencer and reference memories, as well as any waveforms currently saved on screen. It also verifies that the current front-panel setup is changed to the default values normally established when an INIT PANEL is performed.
a. Recall the Initial Front-Panel Setup, labeled "FPNL" (see Step $i$ in "INITIAL SETUP" at the start of this procedure).

## Select: TRIGGER MODE

Set: AUTO On

Select: VERTICAL MODE
Set: CH 2 Off
Set: CH 1 VOLTS/DIV 5 V
A SEC/DIV $\quad 100 \mu s$
b. Save CH 1 trace in REF memory 1: Position the CH 1 trace to the graticule line 3 divisions above center screen, then push STORAGE SAVE to display the SAVEREF SOURCE menu. Now push CH 1 in the menu and, when the menu changes, push REF1.
c. Reposition CH 1 trace and save in REF memory 2: Position the CH 1 trace to the graticule line 1 division above center screen. Now push CH 1 and, when the menu changes, push REF2.
d. Reposition CH 1 trace and save in REF memory 3: Position the CH 1 trace to the graticule line 1 division below center screen. Now push CH 1 and, when the menu changes, push REF3.
e. Reposition CH 1 trace and save in REF memory 4: Position the CH 1 trace to the graticule line 3 divisions below center screen. Now push CH 1 and, when the menu changes, push REF4.
f. Reposition CH 1 trace and display REF memories 1-4: Push ACQUIRE and move the "live" CH 1 trace to the bottom of the graticule. Push DISPLAY REF, and then set REF1 through REF4 on to display the saved CH 1 traces. Five traces should now be displayed.
g. Display Teksecure Erase Memory menu: Push the front-panel button labeled "MENU OFF/EXTENDED FUNCTIONS" twice to display the Extended Functions menu. Next, push SYSTEM and, when the menu changes, push PANEL. Now push the TEKSECURE ERASE MEMORY to display that menu.
h. Execute Teksecure Erase Memory: Push ERASE. The instrument screen will blank momentarily and then the message "RUNNING SELF TEST" will appear.

## NOTE

If the SELF TEST fails and causes the Extended Diagnostics menu to be displayed, continue with part i of this procedure. Otherwise, skip to part j to verify the memory status.

Performance Check and Functional Verification Procedure 2440 Service
i. Failure of the SELF TEST that runs when Erase Memory is executed-even for reasons not related to internal RAM memory blocks - causes the Extended Diagnostics menu to be displayed, rather than the Teksecure Status menu. If this is not the case, continue this procedure at part $j$. If the Extended Diagnostics menu is displayed, do the following:

1. Push the MENU OFF/EXTENDED FUNCTIONS button once to force display of the Teksecure Status menu.
2. Perform part $j$ and determine the Erase Memory status as instructed.
3. If status is determined ERASED, continue this procedure at part $k$; otherwise, perform part $g$ again to access the Teksecure Erase Memory menu, and push ERASE to execute another Erase Memory. Then, if the Erase Memory Status menu is not already displayed, push the MENU OFF/EXTENDED FUNCTIONS button once to force the display of the Teksecure Status menu. Now perform part $j$, and, if the status is not ERASED, refer the instrument to qualified service personnel for repair.

## NOTE

Even if the Erase Memory status is determined successfully, the failure that resulted in the SELF TEST fallure should be serviced. After completing this procedure, run the Self Calibration procedure, followed by the Self Diagnostics procedure. (See Sections 5 and 6 of this manual for instructions on how to perform these procedures). If both are not successful, refer the instrument to qualified service personnel.
j. VERIFY - Internal memory status: After the SELF TEST is completed, confirm that the message ERASED appears immediately following the TEKSECURE ERASE MEMORY STATUS caption, as well as after each of the captions for the individual blocks of RAM memory. If FAILED appears after any caption, perform parts $g$ and $h$ again to reexecute an Erase Memory. If status is still FAILED, this verification fails and the instrument should be referred to qualified service personnel for repair.
k. VERIFY - Front-panel and screen status: Confirm that CH 1 is set to 100 mV (was set to 5 V in part a) and that the A SEC/DIV is set to 1 ms (was set to $100 \mu \mathrm{~s}$ in part a). Confirm that the four traces that were saved in and displayed from REF memories 1-4 are no longer displayed, and that the "live" CH 1 trace is displayed at or near center screen.
I. VERIFY - Reference Memory status: Push DISPLAY REF. Confirm that the status "EMPTY" is displayed above the REF $1-4$ labels in that menu. Now use the menu buttons to first display and then remove each REF memory. Confirm that each memory displays an invalid "waveform;" that is, a horizontal line at center screen that is broken by (alternates with) full-screen fill areas.
m. VERIFY - Sequencer Memory Status: Push PRGM to display the AUTOSTEP SEQUENCER menu; then push RECALL to switch to the menu for recalling sequences. Confirm that the label FPNL (the label for the Initial Setup sequence), is no longer listed for recall. Further, confirm that no other sequences are listed for recall.

Confirmation of parts j through m constitutes a verification of the Teksecure Erase Memory feature.

# ADJUSTMENT PROCEDURE 

INTRODUCTION

## IMPORTANT—PLEASE READ BEFORE USING THIS PROCEDURE

This procedure is used to return the instrument to conformance with its "Performance Requirements" as listed in the "Specification" (Section 1). It can also be used to optimize the performance of the instrument. As a general rule, these adjustments should be performed every 2000 hours of operation or once a year if used infrequently.

The Adjustment Procedure consists of three subsections. The first subsection is "Internal Adjustments." Step 1 of this subsection, "Display Adjustments," uses display test patterns generated internally by the instrument. Steps 2 through 6 require external generators to provide signals for the test displays. In all steps of the "Internal Adjustments" internal controls must be adjusted (cabinet removal is required). An internal jumper must also be pulled off to enable the menu choices for the Extended Calibration menu. This menu must be enabled to perform "Display Adjustments" as well as the Attenuators and Triggers adjustments called out in the "External Calibration" subsection of this procedure.

The second subsection is "Self Calibration." SELF CAL is a fully automatic procedure initiated by the user from the front panel. No external signals or internal adjustments are required, and beyond starting the procedure, no further action is needed for the user to do a SELF CAL. The instrument cabinet must be installed to obtain a proper SELF CAL, and the Self Calibration subsection must be done and passed before going on to the third subsection of the Adjustment Procedure.

Subsection three is "External Calibration." Here, the user inputs test signals for the Attenuator and Trigger calibration and initiates the semiautomatic routines that use those signals. The internal jumper disabling the Extended Calibration (EXT CAL) menu must be removed to enable the EXT CAL menu choices (as was necessary for the

Display Adjustments in 'Internal Adjustments' subsection). The instrument cabinet must be installed and the instrument operating at an ambient temperature between $+20^{\circ} \mathrm{C}$ and $+30^{\circ} \mathrm{C}$ for valid calibration of the Attenuators and Trigger circuits.

## CALIBRATION SEQUENCE AND PARTIAL PROCEDURES

To completely calibrate this instrument, all steps of this procedure should be performed, completely and in sequence. Individual steps in either the Internal Adjustments or External Calibration subsections can be omitted if a complete calibration is not needed. Individual substeps (parts) in "Display Adjustments" (Internal Adjustments subsection) can be skipped by advancing to the next display.

While a Self Calibration must be performed before doing the External Adjustments, it can also be performed any time the instrument is installed in its cabinet, optimizing the instrument's performance for the existing environment. The internal jumper removed for performance of the Internal Adjustments and External Calibration does not affect Self Calibration.

## WARM-UP TIME REQUIREMENTS

This oscilloscope requires adequate warm-up time in a $20^{\circ} \mathrm{C}$ to $30^{\circ} \mathrm{C}$ environment before performing the calibration routines and adjustments in this procedure. Calibration performed before the operating temperature has stabilized may cause an erroneous calibration. The adjustment procedure indicates the duration of the warmup periods and the points in the procedure at which they should be allowed.

## PRESERVATION OF INSTRUMENT CALIBRATION

Both the Internal Adjustments and External Calibration subsections require enabling the EXTENDED CALIBRATION menu. Since the internal calibration constants stored can be altered by the user if the EXTENDED CALIBRATION menu is enabled, this menu is disabled by the installation of an internal jumper. REINSTALLATION OF THE INTERNAL JUMPER TO PREVENT INADVERTENT ALTERING OF INTERNAL CALIBRATION

CONSTANTS BY USERS IS RECOMMENDED. Performance of a Self Calibration only, without performance of either of the other two subsections, does not require the removal of the jumper or cabinet.

## NOTE

The Extended Calibration menu can also be accessed via the GPIB (General Purpose Interface Bus). See "Extended Calibration" in Appendix A of the Operators Manual for further information.

## INTERNAL ADJUSTMENTS

Equipment Required (See Table 4-1):<br>Primary Leveled Sine-Wave Generator (Item 1)<br>Secondary Leveled Sine-Wave Generator (Item 2)<br>Calibration Generator (Item 3)<br>Coaxial Cable (Item 10)<br>Precision Coaxial Cable (Item 11)<br>$50 \Omega$ Termination (Item 12)

## 1. Display Adjustments.

a. Remove the cabinet from the instrument (see "Removal and Replacement Procedure" in the "Maintenance" section of this manual). Remove jumper J156 from P156 on the Side Board (on right side of instrument near the front).

## NOTE

Operation (for more than a few minutes) of the scope without its cabinet installed requires that cooling be provided for the components on the Main board. Use a small fan to direct air across the finned heatsinks on that board. The fan used should have the same airflow capability as the fan used in the scope. The CFM (cubic feet per minute) specification for the instrument's fan is 35 CFM at $\mathrm{OH}_{2} \mathrm{O}$ (essentially, open air). Do NOT remove the fan from the scope for use in cooling the Main board, as critical components in other sections of the instrument may overheat.
b. Connect the instrument to a suitable power source and power it ON. Allow a 10 minute warm up before performing the rest of this subsection.
c. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice (two presses are necessary if any menu is presently displayed, one press if no menu is displayed) to display the EXT FUNCT Functions menu.
d. Press the menu button labeled CAL/DIAG (menu will change).
e. Press the menu button labeled EXT CAL to display the EXT CAL menu.
f. Press the menu button labeled ADJUSTS (Display 1 will appear).
g. ADJUST-The ASTIG and FOCUS front panel controls for best definition of the displayed dot.
h. Press any menu button to advance to Display 2.

## NOTE

All adjustment controls associated with Displays 2 and 3 that are not designated front panel controls are located between the fan and the high-voltage shield on the left side board of the instrument.
i. ADJUST-R100 (Grid Bias control) as necessary to display two dots. Continue to adjust R100 just until one dot disappears, leaving the other dot displayed.
j. Press any menu button to advance to Display 3.
k. ADJUST-The ASTIG and FOCUS front panel controls and R300 (Edge Focus control) for most uniform focus over the entire displayed pattern.
I. ADJUST-The TRACE ROTATION front panel control to align the horizontal lines of the displayed pattern parallel to the horizontal graticule lines.
m. ADJUST-R305 (the Y-AXIS control) to align the vertical lines of the displayed pattern parallel to the vertical graticule lines.
n. REPEAT-Parts 1 and $m$ to obtain best overall alignment.
o. ADJUST-R200 (Geometry control) for the least curvature overall of the display lines at the vertical and horizontal edges of the crt screen.
p. ADJUST-R300 (Edge Focus control) for best focus along the edges of the crt screen.
q. Set the INTENSITY control (front panel) for maximum brightness of the display. ADJUST-R400 (Hi-Drive Focus) for best overall focus of the displayed pattern.
r. Return the INTENSITY control to approximately the same setting in effect prior to part $p$ and repeat parts $p$ and $q$ for best focus compromise between the two intensity settings.
s. Press any menu button to advance to Display 4. Note that all adjustment controls associated with this display are located on the top circuit board near the rear of the instrument (see Figure 5-1).
t. ADJUST-R583 (Vertical Spot-wobble control) and R584 (Horizontal Spot-wobble control) for maximum overall definition of the displayed dot pattern (only one dot visible at each graticule line intersection where a dot is displayed).

## NOTE

When the Spot-wobble compensation is badly out of adjustment, three dots will be visible at each of the 33 dot locations. ADJUST-R583 or R584 to align the dots in either a vertically or horizontally oriented line, then use the other control to adjust for only one dot at each dot location (all three dots superimposed).
u. Press any menu button to advance to Display 5. Note that all adjustment controls associated with this display are located on the top circuit board near the rear of the instrument (see Figure 5-1).

## NOTE

The display generated by performing part $s$ is composed of a "rectangle'" of dots, a small "cross'" of 5 dots, and a large "cross" of 2 vectors. Calibration for this display consists of aligning the small cross to the large one (parts $v$ and $w$ ), then aligning both crosses to the center graticule lines (parts $x$ and $y$ ), and finally, adjusting the horizontal sides of the rectangle for 6 divisions of separation and the vertical sides for 8 divisions of separation (parts $z$ and aa). See Figure 5-2 (a and b).


Figure 5-1. Adjustment locations for Displays 4 through 6.


Typical display (No. 5) needing adjustment. Arrows designate display components and. procedure steps affecting those components.


Typical display (No. 5) when horizontal and vertical offsets, gains and vector compensations are correctly adjusted.

Figure 5-2 (a and b). Display 5-Vertical and Horizontal Gain, Offset, and Vector Compensation adjustments pattern.
v. ADJUST-R276 (Vertical Vector Compensation control) to align the 3 vertically oriented dots of the small cross pattern to the vertical vector of the large cross pattern.
w. ADJUST-R376 (Horizontal Vector Compensation control) to align the 3 horizontally oriented dots of the small cross pattern to the horizontal vector of the large cross pattern.
x. ADJUST—R585 (Vertical Offset control) to precisely align the horizontal vector of the displayed pattern to the center horizontal graticule line.
y. ADJUST-R587 (Horizontal Offset control) to precisely align the vertical vector of the displayed pattern to the center vertical graticule line.
2. ADJUST-R580 (Vertical Gain control) to space the horizontal sides of the rectangle exactly 6 divisions apart.
aa. ADJUST-R586 (Horizontal Gain control) to space the vertical sides of the rectangle exactly 8 divisions apart.
ab. Press any menu button to advance to Display 6. Note that the adjustment control associated with this display is located on the top circuit board near the left rear corner of the instrument (see Figure 5-1).
ac. ADJUST-R620 (Integrator Time control) for best front corner (minimum roll-up or roll-off) of the highfrequency (filled) portion of the display. See Figure 5-3 for further detail.
ad. Push any menu button to exit display 6.


Figure 5-3. Display 6-Integrator Time adjustment pattern.

## 2. CCD Clocks Adjustment.

a. Determine if CCD clocks need adjustment:

- If doing this adjustment procedure after a repair that required replacing either or both CCD's (U450 and U350 on schematic diagram 10) or Peak Detectors (U440 and U340, also on diagram 10) or the CCD Phase Clock Generator (U470 on schematic diagram 11), the CCD clocks will need adjustment; skip to part b and continue this procedure.
- If doing this adjustment procedure as part of routine maintenance, or after a repair that did not require replacing the components just mentioned, do the following to determine if clock adjustment is adequate: perform part $c$ to preset the instrument's front-panel controls (skip making the TRIGGER SOURCE setting). Next do part $h$ and subparts 1-3 of part $i$ to set up the instrument and the test generator for checking clock adjustments. Now, do part $r$, subparts 1-3. If part $r$ is passed for both channels, CCD clock calibration is good; skip to step 3, "CH 1 and CH 2 Input Capacitance Adjustment". If part $r$ is not passed, continue this procedure at part $b$.
b. Preset clock adjustments: Center all adjustment controls shown in Figure 5-4 so they are halfway between full clockwise and full counter-clockwise rotation.
c. Initialize front-panel controls: Push the SETUP PRGM front-panel button; then push the menu button labeled INIT. Push the TRIGGER SOURCE front-panel button and set LINE on (underline it) in the menu.

NOTE
This procedure for adjusting clocks assumes frontpanel settings set by the PRGM INIT feature; change those settings only when directed to by this procedure.

## d. Preset Common-Mode counts:

1. Display GN-DAC counts: Set CH 1 VOLTS/DIV control to 50 mV , and set the SEC/DIV to 500 ns . Rotate the CH 1 POSITION knob to move the display up off screen. Push MENU OFF/EXTENDED FUNCTIONS twice; then push the SPECIAL menu button, and, when the menu changes, push CCD ADJ. Now, push the ADJ T1 A2 menu button to display the A and T clock adjustment numbers (T1 A2 will be underlined).
2. Display menu for adjusting CM counts: Push MENU OFF/EXTENDED FUNCTIONS twice; then push the SPECIAL menu button, and, when the menu changes, push FORCE DAC. The menu for adjusting the CM counts should now be at the bottom of the screen, with the various CCD counts for the four CH 1 CCD sides and the message "TESTING CHANNEL $1^{\prime \prime}$ displayed above that menu. (See Figure 5-5.)


Figure 5-4 (SN B010250 \& Above). CH 1 and CH 2 CCD Clock Adjustments (shown centered, as after doing part b).

## CCD CLOCK ADJUSTMENTS

CH 2


Figure 5 -4 (SN B010249 \& Below). CH 1 and CH 2 CCD Clock Adjustments (shown centered, as after doing part b).


Figure 5-5. CCD counts display and CM adjustment menu.
3. Set CM/GN-DAC counts, CH 1 sides 1 and 3, at 500 ns: Repeatedly push the left-most menu button until the common-mode count for CM1O is displayed. Rotate the INTENSITY knob to set the CM1O count to 4095 (maximum count), and then do the following:

- If either GN-DAC counts for side 1 and 3 are below 500, refer the instrument to service personnel for repair.
- If the GN-DAC counts for both side 1 and side 3 are within 500-3200, push WRITE TO CAL STORE and skip to subpart 4.
- If the GN-DAC counts for either or both side 1 and 3 are above 3200 counts, reduce the CM1O count (CM1O stands for CommonMode count, CH 1, Odd sides) just enough to bring both counts to $\leqslant 3200$, and then push WRITE TO CAL STORE. If CM1O must be reduced to below 1500 counts to bring both GN-DAC counts to within limits, or if both counts cannot be brought to within limits, refer the instrument to service personnel for repair.

4. Set CM/GN-DAC counts, CH 1 side 2 and 4, at $\mathbf{5 0 0}$ ns: Push the left-most menu button to move to CM1E (Common-Mode count, CH 1, Even sides); then rotate the INTENSITY knob to set this count to 4095. Now check, and set to within limits if necessary, the GN-DAC counts for sides 2 and 4 as was just done for sides 1 and 3 in subpart 3.
5. Set CM/GN-DAC counts, CH 2 all sides, at 500 ns : Rotate the CH 1 POSITION knob to return the CH 1 trace to center screen. Push VERTICAL MODE and set CH 2 on and CH 1 off in the menu. Set CH 2 VOLTS/DIV to 50 mV and rotate the CH 2 POSITION knob to move the CH 2 trace up off screen. Now, return to the CM counts menu: push MENU OFF/EXTENDED FUNCTIONS twice; then push SPECIAL; then push FORCE DAC. The menu for adjusting the CM counts should now be at the bottom of the screen, with the CCD counts for CH 2 CCD sides and the message "TESTING CHANNEL $2^{\prime \prime}$ displayed above that menu. Push the left-most menu button until CM20 appears; then repeat subparts 3 and 4 , adjusting the CH 2 common-mode counts, CM2O instead of CM1O, and CM2E instead of CM1E.
6. Turn off CCD counts display: Vertically position CH 2 back to center screen. Next, push MENU OFF/EXTENDED FUNCTIONS twice; then push SPECIAL; then push CCD ADJ. Now, push the ADJ T1 A2 menu button to turn off the A and T clock adjustment numbers.
7. Match CH 1 CM counts at $\mathbf{2 0 0} \mathbf{n s}$ and 100 ns to 500 ns : Push VERTICAL MODE and set CH 1 on and CH 2 off. Push MENU OFF/EXTENDED FUNCTIONS twice; then push the SPECIAL menu button, and, when the menu changes, push FORCE DAC. Note the CM1O and CM1E counts obtained in subpart 4. (Use the left- and right-most menu buttons to display CM1O and CM1E.) Now change the SEC/DIV setting to 200 ns , and use the INTENSITY control to set CM1O and CM1E to the values just noted. When finished, push WRITE TO CALSTORE, followed by the A HORIZONTAL MODE button. Change the SEC/DIV to 100 ns and match CM1O and CM2E to the 500 ns values also.
8. Match CH 2 CM counts at 200 ns and 100 ns to 500 ns: Push VERTICAL MODE and set CH 2 on and CH 1 off. Return the SEC/DIV to 500 ns . Repeat subpart 7 for CH 2 , adjusting CM2O and CM2E, rather than CM1O and CM1E. Remember to push WRITE TO CALSTORE followed by A HORIZONTAL MODE after each CM adjustment.
e. Do a SELF CAL and verify initial CCD gain: Skip to, and perform, the procedure found under SELF CALIBRATION in this section. (At this stage of instrument adjustment, SELF CALIBRATION may take several minutes to run rather than the 10 seconds mentioned in the SELF CAL procedure.) If instrument passes the SELF CAL (see NOTE in SELF CAL procedure), skip to part fof this procedure and continue. If, after redoing a SELF CAL as directed in parts e and fof the SELF CAL procedure, any test level except level 7000 has FAIL status, quit this procedure and refer the instrument to service personnel.

If only test level 7000 failed, verify that $C C D$ gain test 7210-30 passed: repeatedly push the down-arrow menu button to move down the underline pointer at test level 0000 until it is under test level 7000 . Push RUN/SEL, and when the menu changes, use the down-arrow button to underline 7200. Push RUN/SEL. Test levels 7210, 7220, and 7230 should all have PASS status (ignore 7240 and 7250); if so, push MENU OFF/EXTENDED FUNCTIONS to remove diagnostic ment and continue with subpart $f$; if not, quit this procedure and refer the instrument to qualified service personnel for repair.
f. Check CH 2 and CH 1 LF-linearity and positioneffect, and fine-adjust CM counts:

1. Set up instrument for check: Set A SEC/DIV to $50 \mu \mathrm{~s}$. Next, push COUPLING/INVERT and set $50 \Omega$ ON:OFF to ON for both CH 1 and CH 2. Push ACQUIRE and set REPET ONIOFF to ON. Push TRIGGER SOURCE and set to VERT in the menu. Connect the + FAST RISE output of a Calibration Generator to the CH 2 input connector via a $50-\Omega$ cable. Set the generator, output for a 1 ms period and for exactly 2 vertical divisions (discount trace width) of amplitude. Vertically center the display.
2. Make linearity check: Rotate the CH 2 POSITION knob to align the bottom of the waveform to the horizontal graticule mark 2.5 divisions above the center horizontal graticule line (the top of the waveform will be off screen). Now push SAVE, vertically reposition the waveform to center screen, and check that the amplitude of the saved waveform is between 1.9 and 2.1 divisions. Push ACQUIRE and repeat the linearity check, this time aligning the top of the waveform to the mark 2.5 divisions below the center horizontal graticule line before pushing SAVE. Push ACQUIRE when finished.
3. Make position-effect check: Set SEC/DIV to 5 ns . Adjust the amplitude of the calibration generator for 5 divisions, vertically center the pulse, and
horizontally align its rising edge to center screen. Position the top of the waveform to 3.5 divisions below center graticule. Push ACQUIRE and set ENVELOPE to CONTinuous. Check that the vertical width of the trace between 5 ns and 15 ns after the step transition is less than 0.4 division. (Push MENU OFF/EXTENDED FUNCTIONS to turn off menu so the waveform can be easily seen.) Set A SEC/DIV to 500 ns . Push ACQUIRE and set back to NORMAL.
4. Fine-adjust CM counts: If both LF-linearity checks in subpart 2, as well as the position-effect check in subpart 3 , were passed, skip to subpart 5. If either of the LF-linearity checks and the positioneffect check failed, refer the instrument to qualified service personnel for repair. Otherwise, display the menu for adjusting the CM counts: Push MENU OFF/EXTENDED FUNCTIONS twice; then SPECIAL; then push FORCE DAC. Then, do the following:

- If either of the LF-linearity checks failed but the position-effect check passed, rotate the INTENSITY control to reduce CM2E by about 150 counts; then push WRITE TO CALSTORE; then push the A HORIZONTAL MODE front-panel button. Next, push the downward arrow menu button to display CM2O and reduce it by about 150 counts also; then push WRITE TO CALSTORE, followed by the A HORIZONTAL MODE button.
- If only position-effect check failed, repeat CM2E/CM2O adjustments as just described for the LF-linearity check failure except increase, rather than reduce, CM2E and CM2O by about 150 counts.

If you had to reduce/increase the CM counts, change the SEC/DIV setting to 200 ns and set CM2O and CM2E to the new values just set for the 500 ns setting. Switch to 100 ns and repeat. (Use the two left-most menu buttons to select between CM2O and CM2E; remember to always push WRITE TO CALSTORE, followed by the A HORIZONTAL MODE button after adjusting any CM count.) When finished, return the SEC/DIV setting to $50 \mu \mathrm{~s}$ and repeat subparts 2, 3, and 4 until the LF-linearity and position-effect checks pass or until CM count is below 1500. (Always match the CM counts at 200 and 100 ns when they are changed at 500 ns .) If any CM count must be reduced below 1500, the instrument should be referred to qualified service personnel for repair.
5. GN-DAC counts check: SEC/DIV should be set to 500 ns . Push MENU OFF/EXTENDED FUNCTIONS twice; then SPECIAL; then CCD ADJ. Push ADJ TI A2 to display the GN-DAC counts. (" TESTING CHANNEL $\mathbf{2 n}^{\prime \prime}$ should be displayed.) Check that the GN-DAC counts for all four sides (1-4) are within $1000-3200$. If one or more GN-DAC counts are outside this range, change test-selectable resistors R690 and R881 (located on Time Base board) to one of the three pairs of values given in Table 5-1. Resistors must be changed as a pair. If the out-of-limit GN-DAC counts are greater than 3200, increase R690 and R881 to next higher pair of values listed; if the GN-DAC counts are less than 1000, decrease the resistors to the next lower pair of values. Recheck GN-DAC counts and increase/decrease resistors to the next pair in table as required. If GNDAC counts cannot be brought to within limits with values pairs given in Table 5-1, refer instrument to qualified service personnel for repair.

Table 5-1
Test Selectable Resistor Values
(R690 and R881)

| R690 | PART NUMBER | R881 | PART NUMBER |
| :---: | :---: | :---: | :---: |
| $100 \Omega$ | $321-0097-00$ | $301 \Omega$ | $321-0143-00$ |
| $107 \Omega$ | $321-0100-00$ | $348 \Omega$ | $321-0149-00$ |
| $110 \Omega$ | $321-0101-00$ | $374 \Omega$ | $321-0152-00$ |

6. Check LF-linearity and position effect, and fine-adjust CM counts for CH 1: Push the ADJ TI A2 menu button to turn off the GN-DAC counts display. Set the SEC/DIV to $50 \mu \mathrm{~s}$. Move the $50-\Omega$ cable at CH 2 to the CH 1 input connector. Push VERTICAL MODE, set CH 2 off and CH 1 on in the menu. Adjust the generator for exactly 2 vertical divisions (discount trace width) amplitude, vertically centered on screen. Now do subparts 2-5, using CH 1 controls instead of CH 2 controls and adjusting CM1O/CM1E where CM20/CM2E are indicated. ("TESTING CHANNEL 1" will be displayed when subpart 5 is performed.) Any time R609 and R881 must be changed to bring either channel's GN-DAC counts within limits, subpart 5 must be reperformed for the other channel. If the resistors must be changed to a higher pair of values for one channel, only to require a lower pair for the other channel, or if both channels cannot be brought to within the GN-DAC count limits, refer this instrument to qualified service personnel for repair.
7. Remove setup: Push ACQUIRE and set REPET ONIOFF to OFF. Disconnect the cable from the CH 1 input connector.

## g. Check for correct CCD operation:

1. Display GN-DAC counts: Push MENU OFF/EXTENDED FUNCTIONS twice; then push SPECIAL; then push CCD ADJ. Now, push the ADJ T1 A2 menu button to display the A and T clock adjustment numbers ( $T 1$ A2 will be underlined). The various CCD counts for the four CH 1 CCD sides should be on screen, with the message "TESTING CHANNEL $1^{\prime \prime}$ displayed near the bottom of the screen.
2. Verify CH 1 counts are within limits: Set the SEC/DIV control to 500 ns . Verify that the various counts for each of sides 1-4 are within the limits listed below. If any count is outside the limit listed, refer the instrument to service personnel.

| SIDE | OFFSET <br>  <br> PLUS MINUS | GN-DAC | GAX | GIN | GAIN |
| :--- | :---: | :---: | :---: | :---: | :---: |
| LIMIT |  |  |  |  |  |
| $1-4$ | $\leqslant 10 \leqslant 10$ | $500-3500 \leqslant 115$ | $\geqslant 80$ | $\geqslant 100$ |  |

3. Verify CH 2 counts are within limits: Push VERTICAL MODE and set CH 2 on and CH 1 off in the menu displayed (message will change to "TESTING CHANNEL $2^{\text {n }}$ ). Verify that the various counts for each of the CH 2 sides 1-4 are within the limits listed for subpart 2. If any count is outside the limit listed, refer the instrument to service personnel.
4. Turn off display of GN-DAC counts: Redo subpart 1, pushing ADJ T1 A2 menu button to remove the display (the underline below T1 A2 is also removed.)
h. Prepare instrument for adjusting $\mathrm{L}, \mathrm{TI}$, and A clocks:
5. Turn off display vectors: Push the front-panel button SELECT, and when the menu changes, push the menu button to set VECTORS ONIOFF to OFF (OFF should be underlined).
6. Set input coupling: Push CH 1 COUPLING/INVERT and set 50 OHMS ON:OFF to ON (the coupling mode should already be set to DC) in the menu displayed. Push CH 2 COUPLING/INVERT and set 50 OHMS ON:OFF to ON in that menu.

## For SN B010250 \& Above

3. Input test signal: Connect the output of the secondary Leveled Sine-wave Generator (Item 2) to the CH 1 and CH 2 input connectors via a precision $50-\Omega$ BNC cable and a dual-input coupler.

## For SN B010249 \& Below

3. Input test signal: Connect the output of the primary Leveled Sine-wave Generator (Item 1) to the CH 1 and CH 2 input connectors via a precision $50-\Omega$ BNC cable and a dual-input coupler.

## i. Set up to adjust the L clocks:

1. Set up Vertical mode, Trigger source, and acquisition rate: Push the VERTICAL MODE frontpanel button and turn CH 1 on in the menu displayed. Leave CH 1 on also; both channel's VOLTS/DIV setting should be 50 mV . Next, rotate the CH 2 POSITION knob to move the CH 2 trace up off screen. Push TRIGGER SOURCE, and then push the EXT menu button. When the menu changes, set A EXT SOURCE $1: 2$ to 2 (underline the ${ }^{*} 2^{\circ}$ ). Set the SEC/DIV control to 200 ns .

## NOTE

The following two subparts set up an "aliased" display on screen that is used in adjusting the $L$ clocks. At the 200-ns per division setting specified in subpart 2, the acquisition rate will be lower than is required to properly display the $250-\mathrm{MHz}$ sine wave specified in the same subpart. However, by slightly varying the generator output frequency as needed, an "aliased" display is created. The aliased sine wave appears as if it is untriggered and as if its frequency is much lower than the $250-\mathrm{MHz}$ sine wave output by the generator. Use a generator with a highly stable frequency output, such as the TEKTRONIX SG 503.

## For SN B010250 \& Above

2. Set up test signal: Set the generator output level for about a 6-division display at a frequency of 6 MHz , then change the output frequency to 250 MHz . Readjust for a 6 divisions amplitude if necessary, and vertically center the display.

## For SN B010249 \& Below

2. Set up test signal: Set the generator output level for about a 6-division display at a frequency of 1 MHz , then change the output frequency to 250 MHz . Readjust for a 6 divisions amplitude if necessary, and vertically center the display.
3. Alias display: Vary the generator output frequency slightly (if required) until only one or two cycles of the untriggered sine wave are displayed (about $\pm 100 \mathrm{kHz}$ ).

At this point, the display should appear similar to Figure 5-6 (except "live", not "frozen"); although offset (spacing) between the sides varies from instrument to instrument. Since the instrument is set up to auto-level trigger but given no trigger signal (EXT source), it freezes the display on screen about once every second. This makes it easier to see the results when making a clock adjustment.


Figure 5-6. CCD sides 1-4 for CH 1 before L-clock adjustment. Note menu shows all sides are ON.
4. Display CCD sides menu: Push the MENU OFF/EXTENDED FUNCTIONS button twice to return
to the Extended Functions menu; push SPECIAL and, when the menu changes, push CCD sides.
5. Check/match coarse frequency response between channels: Set sides 2, 3, and 4 off in the menu, leaving only side 1 on (underlined sides are on). Rotate the CH 2 POSITION knob to move the CH 2 display back on screen. Check that the difference between the amplitudes of the CH 1 and CH 2 displays is no more than 1 division. If mismatched by more than 1 division, adjust R436, C456, and R525 for CH 1 and R263, C257, and R410 for CH 2 until the amplitudes match. (The CH 1 adjustments are located near the front of the instrument on the Main board between the CH 1 Preamp IC, U420, and the shaft to the POWER ON OFF switch; the CH 2 adjustments are located between the CH 1 Preamp IC, U420 and the CH 2 Preamp IC, U320.) Position the CH 2 display off screen and turn back on all four sides when finished.

## For SN B010250 \& Above

## NOTE

When a procedure part or subpart requires an adjustment, pay particular attention to whether CH 1 or CH 2 is to be adjusted. Both CH 1 and CH 2 have an LIS adjustment, an A2S adjustment, etc., so be sure you are setting the adjustment for the channel specified by the part; be sure you are not setting the equivalent adjustment for the alternate channel. Use Figure 5-4 to locate the adjustments.

## For SN B010249 \& Below

## NOTE

When a procedure part or subpart requires an adjustment, pay particular attention to whether CH 1 or CH 2 is to be adjusted. Both CH 1 and CH 2 have an LIS adjustment, an A2D adjustment, etc., so be sure you are setting the adjustment for the channel specified by the part; be sure you are not setting the equivalent adjustment for the alternate channel. Use Figure 5-4 to locate the adjustments.
j. Align the odd-numbered CH 1 CCD sides: Set SIDE 2 and SIDE 4 to OFF in the menu. Set the CH 1 L1S adjustment for the best alignment of the two sides displayed (sides 1 and 3). Push A HORIZONTAL MODE, and readjust if necessary.
"Best Alignment" occurs when both sides are merged into a single side containing twice as many dots or samples. Figure 5-7 ( $a$ and b) shows typical "before and after" displays for adjustment of any two CCD sides; here, sides

1 and 3 for CH 1 . When setting the L clocks to align any two given sides, set for equal alignment between the rising and falling portions of the sine wave; expect some mismatch of alignment between the peaks of the sides.

## NOTE

Pushing A HORIZONTAL MODE causes the instrument to make firmware corrections based on the new adjustment just made for the $L$ clock. These corrections may change the alignment slightly; in subparts $j$-n, repeatedly alternate between making the adjustment and pushing A MODE until no change is noted when the button is pushed.
k. Align the even-numbered CH 1 CCD sides: Set SIDE 2 and SIDE 4 back on, and set SIDE 1 and SIDE 3 to OFF. Set the CH 1 L2S adjustment for the best alignment of the two sides displayed. Push A HORIZONTAL MODE when finished.
I. Align CH 2 even sides and odd sides: Rotate the VERTICAL POSITION knobs to position the CH 1 display up off screen and the CH 2 back on screen. Repeat parts j
and k , using the CH 2 L-clock adjustments to align the CH 2 CCD sides. Be sure to adjust the CH 2 L1S and L2S adjustments and not the equivalent CH 1 L-clock adjustments that were just set. See Figure 5-4 for adjustment locations.
m. Align CH 1 sides to CH 2 sides: Turn on SIDE 2 and turn all remaining sides off. Rotate the CH 1 POSITION knob to return CH 1 on screen positioned so that its ground reference indicator (a small " ${ }^{*}$ " at the left edge of the screen) is on the center horizontal graticule line. Use the CH 2 POSITION knob to superimpose its ground reference indicator on CH 1's. Now, adjust CH 1 L2D for best alignment of the CH 1 and CH 2 sides. You may adjust CH 2 L2D if good alignment is not achieved. (If such is the case, alternate between the CH 1 and CH 2 L1D adjustments until best alignment is achieved.) Remember to push A HORIZONTAL MODE after making each adjustment.
n. Align an even CH 1 CCD side to an odd: Set SIDE 1 and SIDE 2 on and all remaining sides OFF. Position the CH 2 display up off screen. Now, adjust CH 1 L1D for best alignment of sides. Push A HORIZONTAL MODE.


Figure 5-7 (a and b). Sides 1 and 3 before adjustment of L1S and after. Similar results should be obtained when adjusting any
pair of sides with the L-clocks adjustments. (Best alignment that can be achieved varies from instrument to instrument.)
o. Align an even CH 2 CCD side to an odd: Position CH 1 up off screen and CH 2 on. Adjust the CH 2 L1D for best alignment of SIDE 1 and SIDE 2. Push A HORIZONTAL MODE.
p. Check CH 1 and CH 2 L-clock adjustment: Position both channels back on screen, and turn on all four CCD sides. Verify that each channel displays good alignment of its four sides. Repeat parts j through o as necessary to fine-tune the alignment.

## q. Adjust the $\mathbf{A}$ and $\mathbf{T}$ clocks:

## For SN B010250 \& Above

1. Coarse adjust the CH 1 A and T clocks: Vertically position the CH 2 display off screen. Look at Figure 5-8 and note the stray samples labeled there. If the CH1 display has similar "stray samples"-samples obviously offset from the wellaligned samples-adjust the CH 1 A and T clocks to align these stray samples. Begin with TID and TIS, and if necessary you can adjust A2S. Push A HORIZONTAL MODE after making each adjustment, iterating between making the adjustment and pushing $A$ MODE as was done for the $L$ clock adjustment.

## For SN B010249 \& Below

1. Coarse adjust the CH 1 A and T clocks: Vertically position the CH 2 display off screen. Look at Figure 5-8 and note the stray samples labeled there. If the CH 1 display has similar "stray samples"-samples obviously offset from the wellaligned samples-adjust the CH 1 A and T clocks to align these stray samples. Begin with TID and TIS, and if necessary you can adjust A2D and A2S. Push A HORIZONTAL MODE after making each adjustment, iterating between making the adjustment and pushing $A$ MODE as was done for the $L$ clock adjustment.
2. Coarse adjust the CH 2 A and T clocks: Vertically position the CH 2 display on screen; position the CH 1 display off screen. Repeat subpart 1, but use the CH 2 A and T clock adjustments instead of those for CH 1. See Figure 5-4 for adjustment locations.
3. Display the $A$ and $T$ clock-adjustment counts: Set CH 1 on and CH 2 off in the VERTICAL MODE menu. Leave CH 1 vertically positioned off
screen. Push the MENU OFF/EXTENDED FUNCTIONS button twice; then push SPECIAL; then push CCD ADJ. Now, push the ADJ T1 A2 menu button to display the A and T clock adjustment numbers (T1 A2 will be underlined).

## NOTE

After coarse adjustment performed in subparts 1 and 2, the adjustments outlined in subparts 4 through 7 are often not needed. When performing these subparts, adjust only if the specified check is failed.


Figure 5-8. CH 1 with L-clocks correctly adjusted, but with stray samples.

## For SN B010250 \& Above

When making an adjustment after a failed check, start by adjusting TID and then TIS, continuing with A2S only if needed. Adjustment of these controls is best determined by trial: Start with TID and "rock" that adjustment back and forth to see if it improves the out-of-limit number(s), without moving the in-limit numbers out of limit. Continue with TIS and A2S as required; make the minimum number of adjustments that puts all the numbers within limits.

## For SN B010249 \& Below

When making an adjustment after a failed check, start by adjusting TID and then TIS, continuing with A2S and A2D only if needed. Adjustment of these controls is best determined by trial: Start with TID and "rock" that adjustment back and forth to see if it improves the out-of-limit number(s), without moving the in-limit numbers out of limit. Continue with TIS and the remaining two adjustments as required; make the minimum number of adjustments that puts all the numbers within limits.

## For SN B010250 \& Above

4. Check CH 1 clocks at 100 ns and adjust if needed: Set the SEC/DIV to 100 ns . If required, adjust (see NOTE below) the CH1 TIS, TID, and A2S adjustments so that all four sides (numbered 1-4 at extreme left) have GN-DAC counts within 700-3500, GAIN MIN counts greater than 92, and the CLIP LIMIT counts greater than 112 for any two sides and greater than 109 for the remaining two sides. (It doesn't matter which two sides are greater than 112 and which are greater than 109, just as long as at least two are greater than 112 and two are greater than 109. Also, all sides can be greater than 112.) See Figure 5-9.

## For SN B010249 \& Below

4. Check CH 1 clocks at 100 ns and adjust if needed: Set the SEC/DIV to 100 ns . If required, adjust (see NOTE below) the CH1 TIS, TID, A2D, and A2S adjustments so that all four sides (numbered 1-4 at extreme left) have GN-DAC counts within 700-3500, GAIN MIN counts greater than 92, and the CLIP LIMIT counts greater than 112 for any two sides and greater than 109 for the remaining two sides. (It doesn't matter which two sides are greater than 112 and which are greater than 109, just as long as at least two are greater than 112 and two are greater than 109. Also, all sides can be greater than 112.) See Figure 5-9.
5. Check CH 1 clocks at 200 ns and adjust if needed: Set the SEC/DIV to 200 ns . If required, adjust as for 100 ns setting, except two sides must be greater than 119 and the remaining sides greater than 115 (GN-DAC and CLIP LIMIT requirements are the same as for 100 ns ). If adjustment is made, recheck at 100 ns when finished and readjust as necessary.


Figure 5-9. Display for adjusting CCD A and T clocks. Note this is the same display for presetting the CM counts, except no CM count adjustment menu is displayed.
6. Check/adjust CH 1 A and T clocks at 500 ns : Set the SEC/DIV to 500 ns . If required, adjust as for the 100 and 200 ns settings, except two sides must be greater than 122 and the remaining sides greater than 119 (GN-DAC and CLIP LIMIT requirements are the same as for 100 ns ). Recheck at 100 ns and 200 ns when finished and readjust as necessary.

## For SN B010250 \& Above

7. Check/adjust CH 2 A and T clocks: Push VERTICAL MODE and set CH 1 off and CH 2 on in the menu displayed. Use the CH 2 POSITION knob to move the CH 2 display up off screen. Now, repeat subparts 2-4 making the CH 2 TIS, TID, and A2S adjustments (only if needed) instead of the CH 1 adjustments (see Figure 5-4).

## For SN B010249 \& Below

7. Check/adjust CH 2 A and T clocks: Push VERTICAL MODE and set CH 1 off and CH 2 on in the menu displayed. Use the CH 2 POSITION knob to move the CH 2 display up off screen. Now, repeat subparts 2-4 making the CH 2 TIS, TID, A2D, and A2S adjustments (only if needed) instead of the CH 1 adjustments (see Figure 5-4).
8. Turn off display for adjusting $A$ and $T$ clocks: Set both CH 1 and CH 2 on in the VERTICAL MODE menu. Vertically position both CH 1 and CH 2 waveforms back on screen. Restore the CCD ADJ menu by pushing MENU OFF/EXTENDED FUNCTIONS twice; then SPECIAL; then CCD ADJ. Push ADJ T1 A2 menu button to turn off the display of the $A$ and $T$ clock adjustment numbers (underline is removed).
9. Do a SELF CAL: Skip to, and perform, the procedure found under SELF CALIBRATION in this section. (At this stage the instrument may take several minutes to run.) If the instrument passes the SELF CAL (see NOTE in SELF CAL procedure), skip to part $r$ of this procedure and continue. If, after redoing a SELF CAL as directed in parts e and $f$ of the SELF CAL procedure, any test level has FAIL status, quit this procedure and refer the instrument to qualified service personnel for repair.
r. Check CH 1 and CH 2 A and T clocks' overall adjustment:
10. Set up for checking CCD side alignment: The SEC/DIV control should be set to 200 ns . Adjust generator frequency to display about 2 cycles on screen.
11. Verify good alignment of, and between, CH 1 and CH 2 waveforms: Push SAVE and use the CH 1 and CH 2 POSITION controls to position the CH 1 and CH 2 for easy viewing. Check that the four sides of both the CH 1 and CH 2 waveforms are well-aligned and appear as single sine wave in each channel (see Figure 5-10). Now use the VERTICAL POSITION knobs to superimpose the CH 1 and CH 2 waveforms. Check that the CH 1 and CH 2 waveforms are well aligned; i. e., the superimposed sine waves should look like a "fatter" version of the CH 1 and CH 2 sine waves.

NOTE
Mainly check the falling and rising parts of the sine wave, rather than the peaks, since the amplitude may differ somewhat between channels as the instrument has not been completely adjusted.


6603-56
Figure 5-10. Typical CH 1 and CH 2 displays after clock adjustment.
3. Check sample dispersion: Now, push STORAGE ACQUIRE and vertically position the CH 1 and CH 2 display about 1 division apart. Adjust the frequency of the test generator for about a third of a cycle display in each channel. Push SAVE to capture a rising or falling portion of the waveform. (Watch the untriggered display until the desired portion is on screen and quickly push SAVE to capture; push ACQUIRE and repeat if unsuccessful.) Check to see that the dispersion of the samples on each section is no greater than one vertical division for each channel, and that there is no more than $1 / 2$ division of difference between the two channels (see Figure 5-11).


Figure 5-11. Checking sample dispersion.
4. If either CH 1 or CH 2 fail the checks just performed, redo parts $\mathrm{i}-\mathrm{q}$ to improve adjustment of L, A, and T clocks to meet checks. (Push STORAGE ACQUIRE to return to a "live" display.)

For SN B010250 \& Above (Step s and subparts only)
s. Adjust the 100 ns L clocks:

1. Set up instrument: Set the SEC/DIV to 100 ns . Vertically position the CH 2 display up off the screen.
2. Set up test signal: Set the generator output level for about a 4-division display at a frequency of 1 MHz , then change the output frequency to 500 MHz . Readjust for a 4 division amplitude if necessary, and vertically center the display.
3. Alias display: Vary the generator output frequency slightly (if required) until only one or two cycles of the untriggered sine wave are displayed (about $\pm 100 \mathrm{KHz}$ ).
4. Adjust CH $1 \mathbf{1 0 0} \mathrm{~ns} L$ clock: Set the CH 1 L2D100 adjustment for the best alignment of all 4 sides (minimum sample dispersion). Push A HORIZONTAL MODE, and readjust if necessary. Continue to iterate until no change is noted when $A$ HORIZONTAL MODE is pushed.
5. Adjust CH 2100 ns L clock: Vertically position the CH 1 display up off screen, and position the CH 2 display back on screen. Set the CH 2 L2D100 adjustment for the best alignment of all 4 sides (minimum sample dispersion). Push A HORIZONTAL MODE, and readjust if necessary. Continue to iterate until no change is noted when A HORIZONTAL MODE is pushed.
t. Disconnect test setup.

## 3. CH 1 and CH 2 Input Capacitance Adjustment (C414 and C311).

a. If a menu is displayed, press the MENU OFF/EXTENDED FUNCTIONS button to remove it from the screen. Select SETUP PRGM and press the menu button labeled INIT PANEL. Make the following changes to the front panel setup:

Set: A SEC/DIV $100 \mu$ S
b. Connect the HIGH AMPLITUDE output of the Calibration Generator to the CH 1 input connectors via a precision $50 \Omega$ BNC cable, a $50 \Omega$ terminator, and an adjustable normalizer.
c. Set the generator output level for a 6 division display at a frequency of 1 kHz .
d. Set the normalizer for a square front corner over approximately the first $40 \mu \mathrm{~s}$ ( 0.4 division) of the positive portion of the waveform.
e. Change the CH 1 VOLTS/DIV control to 50 mV and adjust the generator amplitude for a 6 division display.
f. ADJUST-C414 (near the front edge of the Main board) for the same waveform front corner as noted in part d.
g. Repeat parts $c$ through $f$ until no change is observed in the waveform front corner between the 50 mV and 100 mV settings for the CH 1 VOLTS/DIV control.
h. Move the input signal to CH 2. Select VERTICAL MODE and set CH 2 on and CH 1 off.
i. Repeat parts c through g to adjust the CH 2 input capacitance, adjusting C311 in part f and using the CH 2 VOLTS/DIV control for parts $e$ and $g$.
j. Disconnect the test setup.

## 4. Transient Response Adjustment.

a. Set up to adjust transient response:

1. Initialize front panel: Push the SETUP PRGM front-panel button; then push the menu button labeled INIT.

## NOTE

Subpart 1 initializes the front-panel controls to known settings. Make only the changes outlined in the following procedure parts to avoid incorrect setups.
2. Modify initial control settings: Set CH 1 VOLTS/DIV to 20 mV and the SEC/DIV control to $5 \mu \mathrm{~s}$. Push the CH 2 COUPLING/INVERT front-panel button and set $50 \Omega$ ONIOFF to ON in the menu. Repeat for CH 1. Now, push STORAGE ACQUIRE and set REPET ONIOFF to ON in the menu.
3. Set up test signal: Connect the HI-AMPLitude output of a pulse generator to the CH 1 input through a $50-\Omega$ precision cable, a tunnel-diode pulser, and a 2.5 X attenuator. Set the generator's frequency to 100 kHz and the amplitude to maximum. Now, set the Trigger Level control of the TD Pulser to minimum (full counterclockwise rotation); then slowly rotate control clockwise just until a pulse five divisions in amplitude appears on screen. (Use the minimum Trigger Level setting that triggers the puise.) Vertically center the display. Increase the SEC/DIV setting to 2 ns and push the INIT@50\% front-panel button.
b. Adjust CH 1 transient response: Adjust R436, C456, and R525 for best front-corner. (These adjustments are located near the front of the instrument on the Main board between the CH 1 Preamp IC, U420, and the shaft to the POWER ON OFF switch.)
c. Adjust CH 2 transient response: Disconnect the test signal at the CH 1 input and move to the CH 2 input. Push VERTICAL MODE and set CH 2 on and CH 1 off. Set CH 2 VOLTS/DIV to 20 mV and vertically center the display as required. Now, adjust R263, C257, and R410 for best front-corner. (These adjustments are located near the front of the instrument on the Main board between the CH 1 Preamp IC, U420 and the CH 2 Preamp IC, U320.)
d. Verify CH 2 and CH 1 bandwidth at $20 \mathrm{mV} /$ division:

1. Set up the instrument for bandwidth verifications: Change the SEC/DIV control to 5 ns . Disconnect the pulse generator output from the CH 2 input. Now, connect the output of the secondary Leveled-sine Wave Generator (Item 2) to the CH 2 input through the output head and a 10X attenuator. Set the test generator for a reference 6 -division, $6-\mathrm{MHz}$ signal display vertically centered on screen.
2. Verify CH 2 bandwidth: Switch the SEC/DIV control to 2 ns ; then increase the test generator frequency until the amplitude decreases to 4.4 divisions on screen. The frequency should be greater than or equal to 310 MHz . Write down the frequency and the channel tested for use in the following subparts.

## nOTE

If the frequency at 4.4 division is not greater than or equal to 310 MHz , readjust the transient response for the appropriate channel until the 310 MHz or greater bandwidth is obtained.
3. Verify CH 1 bandwidth: Return the SEC/DIV setting to 50 ns ; push VERTICAL MODE and set CH 1 on and CH 2 off in the menu displayed. Move the signal from the CH 2 input to the CH 1 input, and set the test generator for a reference 6 division, $6-\mathrm{MHz}$ signal, vertically centered on screen. Switch the SEC/DIV control to 5 ns ; then increase the test generator frequency until the amplitude decreases to 4.4 divisions on screen. The frequency should be greater than or equal to 310 MHz (see NOTE for subpart 2). Write down the frequency and the channel tested for use in the following subparts.
e. Match CH 1 bandwidth at remaining VOLT/DIV settings:

## NOTE

The following subparts attempt to match each channel's frequency response for all other VOLTS/DIV settings to that for the 20 mV setting. In some cases, you may not be able to adjust the number of divisions specified in the subpart (either 3.7 or 4.4 divisions) at the frequency obtained for the $20-m V$ setting in part $f$; if this is the case, just adjust as close as possible and check that the number of divisions obtained is $\geqslant 4.4$ ( 3.7 for subpart 3) up to 310 MHz .

1. Display menu for matching bandwidth: Push MENU OFF/EXTENDED FUNCTIONS twice; then push the SPECIAL menu button, and, when the menu changes, push FORCE DAC. Now, push the left-most menu button until TRN1 is displayed near the lower-left corner of the screen.
2. Set up CH 1 for adjusting 1-V bandwidth: Set the CH 1 VOLT/DIV to 1 V . Remove the 10 X attenuator and connect the generator's leveling head directly to the CH 1 input. Return the SEC/DIV to 50 ns and set the generator for the 5 division, $6-\mathrm{MHz}$ reference signal. Change the SEC/DIV setting to 2 ns and increase the generator frequency to that written down for subpart 3 of part d.
3. Adjust the 1-V bandwidth: Rotate the INTENSITY knob to increase or decrease the waveform's amplitude to set to 3,7 divisions. Push WRITE TO CALSTORE menu button when finished.
4. Set up CH 1 for adjusting $100-\mathrm{mV}$ bandwidth: Set the CH 1 VOLT/DIV to 100 mV . Return the SEC/DIV to 50 ns and set the generator for the 6 -division, $6-\mathrm{MHz}$ reference signal. Change the SEC/DIV setting to 2 ns and increase the generator frequency to that written down for subpart 3 of part d.
5. Adjust the $100-\mathrm{mV}$ bandwidth: Rotate the INTENSITY knob to increase or decrease the waveform's amplitude to set to 4.4 divisions. Push WRITE TO CALSTORE menu button when finished.
6. Set up CH 1 and adjust the $50-\mathrm{mV}$ bandwidth: Install a 10 X attenuator between the generator's leveling head and the CH 1 input, and set the CH 1 VOLT/DIV to 50 mV . Repeat subparts 4 and 5 , using the 50 mV VOLTS/DIV setting instead of 100 mV .
7. Adjust the $10 \mathrm{mV}, 5 \mathrm{mV}$, and 2 mV bandwidth: Install a 5 X attenuator between the 10X attenuator and the CH 1 input. Perform subparts 4 and 5 for the $50-\mathrm{mV}, 10-\mathrm{mV}, 5-\mathrm{mV}$, and $2-\mathrm{mV}$ settings to match the bandwidth for each of those settings. Remember to push WRITE TO CALSTORE after making the TRN1 adjustment at each VOLTS/DIV setting.
f. Match CH 2 bandwidth remaining VOLTS/DIV settings: Push VERTICAL MODE and set CH 2 on and CH 1 off. Move the test signal from the CH 1 input to the CH 2 input, removing both the 5 X and 10X attenuators. Now repeat subparts 1-7 of part e, selecting and setting TRN2 instead of TRN1 in subpart 1, setting the generator to the frequency written down for subpart 2 of part d instead of for subpart 3, and setting the CH 2 VOLTS/DIV control instead of the CH 1 in subparts 2-7.
g. Disconnect the test setup and push MENU/OFF EXTENDED FUNCTIONS to exit the menu.

## 5. $\mathbf{1 0 0 ~ M H z}$ Bandwidth Limit Filter Adjustment

 (Non-TV Options Only).a. If a menu is displayed, press the MENU OFF/EXTENDED FUNCTIONS button to remove it from the screen. Select SETUP PRGM and press the menu button labeled INIT PANEL. Make the following changes to the front panel setup:
$\left.\begin{array}{lcl}\text { Set: } & \text { A SEC/DIV } & 50 \mathrm{~ns} \\ & \text { CH } 1 \text { VOLTS/DIV } & 10 \mathrm{mV}\end{array}\right)$
b. Connect the positive-going, FAST RISE output of the Calibration Generator to the CH 1 input via a precision $50 \Omega$ cable and a 10 X attenuator.
c. Set the generator output level for a 5 division display at a frequency of 100 kHz .
d. ADJUST-R431 for as flat a response as possible. This potentiometer is located on the Main circuit board.
e. Move the test setup to the CH 2 input connector.
f. Select VERTICAL MODE and set CH 2 on and CH 1 off.
g. Set CH 2 VOLTS/DIV to $\mathbf{1 0} \mathrm{mv}$.
h. Repeat parts c and d, adjusting R233 for part d.
i. Disconnect the test setup.

## 6. 20 and 100 MHz Bandwidth Limit Filter Adjustment (TV-Option 05 Only)

a. If a menu is displayed, press the MENU OFF/EXTENDED FUNCTIONS button to remove it from the screen. Select SETUP PRGM and press the menu button labeled INIT PANEL. Make the following changes to the front panel setup:

| Set: | A SEC/DIV | 50 ns |
| :--- | :---: | :--- |
|  | CH 1 VOLTS/DIV | 10 mV |
| Select | BANDWIDTH |  |
| Set: | 20 MHz | On |
|  |  |  |
| Select CH | 1 COUPLING/INVERT |  |
| Set: | $50 \Omega$ ONIOFF | ON |
|  |  |  |
| Select |  |  |
| STORAGE ACQUIRE |  |  |
| Set: | REPET ONIOFF | ON |
|  | AVG | On (8) |

b. Connect the positive-going, FAST RISE output of the Calibration Generator to the CH 1 input via a precision $50 \Omega$ cable and a 10 X attenuator.
c. Set the generator output level for a 5 division display at a frequency of 100 kHz .

NOTE
Adjust the coils in the following parts so their slugs are out approximately the same amount.
d. ADJUST-L531 for as flat a response as possible. This coil is located on the Main circuit board.
e. Move the test setup to the CH 2 input connector.
f. Select VERTICAL MODE and set CH 2 on and CH 1 off.
g. Set the CH 2 VOLTS/DIV control to 10 mV .
h. Repeat parts c and d for CH 2, adjusting L431 for part d.
i. Set the A SEC/DIV control to $100 \mu$ s.
j. Connect the Leveled Sine-wave Generator output via a $50 \Omega$ precision cable and two 10X attenuators to the CH 2 input connector.
k. Set the generator to produce a $50 \mathrm{kHz}, 5$ division display.
I. Increase the generator output to 5 MHz and set the SEC/DIV control to 500 ns .
m . Check that the display amplitude is between 4.80 and 5.05 divisions.
n. Select BANDWIDTH and set $100 \mathbf{~ M H z}$ on. Set the A SEC/DIV control back to 50 ns .
o. Select VERTICAL MODE and set CH 1 on and CH 2 off.
p. Repeat parts b through $h$ to adjust the 100 MHz bandwidth limit, adjusting R431 and R233 in part d (adjust R431 when adjusting for CH 1, R233 for CH 2). These resistors are located on the Main board.
q. Disconnect the test setup.

## 7. Video Input Gain Adjustment (TV-Option 05 Only)

NOTE
In part a, you will connect the ground lead of a X10 probe to pin 5 of J125 on the processor board. Be sure you are connecting to the correct pin. Pin 1 is marked with a square pad, and all odd-numbered pins are in the same row as pin 1. Pin 5 is the second pin up from pin 1.
a. First, power the scope off. Then, perform subparts b-f of part 3 of the Removal and Replacement procedure in Section 6 to access the processor board of the instrument. Connect a X10 probe to the CH 2 input; then connect the ground lead of that probe to pin 5 of J125 of the processor board and the probe tip to the cathode of CR502. (CR502 is immediately above Q504 on the processor board; see the Processor Board drawing in the Diagrams section to locate CR502.) Power the scope back on.
b. Set up the scope: if a menu is displayed, press the MENU OFF/EXTENDED FUNCTIONS button to remove it from the screen. Select SETUP PRGM, and press the menu button labeled INIT PANEL. Make the following changes to the front-panel setup:

$$
\begin{array}{lll}
\text { Set: } & \text { A SEC/DIV } & 2 \mu \mathrm{~s} \\
& \text { CH } 1 \text { VOLTS/DIV } & 500 \mathrm{mV} \\
& \text { CH } 2 \text { VOLTS/DIV } & 2 \mathrm{~V} \\
& \text { TRIGGER SLOPE } & - \text { (minus) }
\end{array}
$$

## Select BANDWIDTH <br> Set: $\quad 20 \mathrm{MHz}$ On <br> Select TRIGGER MODE <br> Set: AUTO On

c. Connect the Full-Field Signal output of the video signal generator to the CH 1 input of the scope via a $75 \Omega$ cable and a $75 \Omega$ terminator.
d. Set the generator output for a field square wave producing a 100 IRE pedestal output for all lines. One line of video, with sync tip and color burst, should be displayed on screen in CH 1. (See top waveform in Figure 5-12.)
e. ADJUST-R419 while watching the output signal on the bench scope. First turn R419 all the way clockwise. Now, slowly rotate the adjustment counter-clockwise until the IRE pedestal appears on both the rising and falling edge of the waveform and the bottom of the waveform
moves up slightly. Adjustment is correct when the output is not overdriven, with the IRE pedestal missing on the rising and edges, or underdriven, with excessive aberrations on the bottom of the waveform. (See bottom waveform in Figure 5-12.)
f. Disconnect the test setup. Perform, in reverse order, subparts b-f in part 3 of the Removal and Replacement procedure to return the processor board to its normal position.


Figure 5.12 Input and output (after adjustment) waveforms.

## SELF CALIBRATION

## Equipment Required: <br> None

## 1. Self Calibration

a. Turn the instrument POWER ON and allow a 10 minute warm-up period. Note that the instrument's cabinet should be in place when performing this subsection of this procedure. (If an Internal Calibration was performed and J 156 removed, do not reinstall J 156 prior to reinstalling the cabinet unless an External Calibration is NOT to be performed after execution of a Self Calibration.)
b. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice (two presses are necessary if any menu is presently displayed, one press if no menu is displayed) to display the Extended Functions menu.
c. Press the menu button labeled CAL/DIAG (menu will change).
d. Press the menu button labeled SELF CAL. "RUNNING" will be displayed in the lower right corner of the crt screen for approximately 10 seconds as the instrument performs its automatic calibration routine.

## NOTE

After successful completion of the automatic calibration routine, "RUNNING" will disappear from the CRT screen and "PASS" will be displayed above the SELF CAL menu button label. Press the MENU OFF/EXTENDED FUNCTIONS button to return the instrument to control settings in effect before the Self Calibration was initiated. If the automatic calibration routine is NOT successful (errors are detected), the EXTENDED DIAGNOSTICS menu will be displayed with accompanying error messages. Perform the following parts only if the instrument fails the Self Calibration; otherwise, Self Calibration has been completed.
e. Press the MENU OFF/EXTENDED FUNCTIONS button to turn off the EXTENDED DIAGNOSTICS menu.
f. Repeat parts b through d. If the instrument displays the EXTENDED DIAGNOSTICS menu again, refer the instrument to qualified personnel for servicing; otherwise, Self Calibration has been successfully completed.

## EXTERNAL CALIBRATION

## Equipment Required (see Table 4-1):

Calibration Generator (Item 3)

## NOTE

J156 must be removed (see step 1, part a of Internal Adjustments) and a Self Calibration executed before this subsection can be performed. After performance (or partial performance) of this subsection, the cabinet should be removed and J156 reinstalled. Installation of this jumper will prevent inadvertent loss of the Calibration constants established by performance of this procedure. See the introduction of this procedure for further detail.

## 1. Attenuator Gain Adjustments.

a. Press the MENU OFF/EXTENDED FUNCTIONS button-twice, if a menu is presently displayed-to call up the Extended Functions menu.
b. Press the menu button labeled CAL/DIAG. (The menu will change.)
c. Press the menu button labeled EXT CAL to display the EXT CAL menu. Then press the menu button labeled ATTEN.
d. Set the Calibration Generator for a DC output. (See the generator Operators manual.)

## NOTE

Do not attempt to calibrate CH 1 and CH 2 simultaneously via a dual-input coupler. The resulting reduction of the scope's input impedance can degrade the calibration-signal amplitude, leading to inaccurate calibration.
e. Connect the STD OUTPUT of the Calibration Generator to the CH 1 input connector through a $50-\Omega$ cable.
f. Press the menu button that is labeled ATTEN GAIN. ("CONNECT CH1 TO 0.2 VDC " will appear.) Set the generator output to 0.200 volts.
g. Press the ATTEN GAIN button again. ("RUNNING" will be displayed near the lower right corner of the screen.)
h. When the display changes from "CONNECT CH1 TO 0.2 VDC " to "CONNECT CH1 TO 2.0 VDC, " change the generator output to 2.000 volts and press the ATTEN GAIN button.
i. When the display changes from "CONNECT CH1 TO 2.0 VDC " to "CONNECT CH1 TO 20.VDC" change the generator output to 20.00 volts and press the ATTEN GAIN button.
j. When the display changes from "CONNECT CH1 TO 20.VDC" to "CONNECT CH2 TO 0.2VDC" disconnect the STD OUTPUT of the Calibration Generator from CH 1 and connect it to the CH 2 input connector.
k. Change the generator output to 0.2 volts and press the ATTEN GAIN button.
I. Repeat Steps $h$ and $i$, substituting CH 2 for CH 1 .

## NOTE

When the sequence is finished, "RUNNING" will disappear from the CRT screen. If the calibration was successful, the ATTEN GAIN label will be marked "PASS." If the calibration was NOT successful, the label will be marked "FAIL." Perform Steps $m$ and $n$ only if the instrument fails the Attenuator Gain calibration sequence; otherwise, go to Step 0 .
m. Recheck the test setup and ensure that the Calibration Generator is set for a DC output. Reperform the Self Calibration subsection of this procedure.
n. Repeat parts a through i. If the instrument fails the Attenuator Gain Calibration sequence again, refer the instrument to qualified personnel for servicing; otherwise, Attenuator Gain Calibration has successfully been completed.
o. Disconnect the test setup.

## 2. Channel Delay Adjustments.

a. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice to display the Extended Functions menu. (Two presses are necessary if any menu is presently displayed, one press if no menu is displayed.)
b. Press the menu button labeled CAL/DIAG (menu will change).
c. Press the menu button labeled EXT CAL to display the EXT CAL menu. Then press the menu button labeled ATTEN.
d. Connect the FAST RISE OUTPUT of a Calibration Generator to the CH 1 and CH 2 input connectors through a $50-\Omega$ cable, a 10 X attenuator, and a dual input coupler.
e. Set the Calibration Generator for a FAST RISE output. (See the generator Operators manual).
f. Press the menu button that is labeled ATTEN GAIN. "CONNECT BOTH CHANNELS TO A FAST RISE SIGNAL VIA A TERMINATED COAX AND A DUAL INPUT CONNECTOR" will appear.) Set the generator output to MAX.
g. Press the RUN button. ("RUNNING" will be displayed near the lower right corner of the screen.)

## NOTE

After successful completion of the Channel Delay Calibration sequence, "RUNNING" will disappear from the CRT screen and "PASS" will be displayed above the CHAN DLY menu button label. If the calibration routine is NOT successful, "FAIL" will be displayed above the CHAN DLY button label. Perform the following parts only if the instrument fails the Channel Delay Calibration sequence; otherwise, Channel Delay Calibration is complete.
h. Recheck the test setup and ensure that the Calibration Generator is set for a fast rise output. Reperform the Self Calibration subsection of this procedure.
i. Repeat parts a through g. If the instrument fails the Channel Delay Calibration sequence again, refer the instrument to qualified personnel for servicing; otherwise, Channel Delay Calibration has successfully been completed.
j. Disconnect the test setup.

## 3. Trigger Adjustments.

a. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice (two presses are necessary if any menu is presently displayed, one press if no menu is displayed) to display the Extended Functions menu.
b. Press the menu button labeled CAL/DIAG (menu will change).
c. Press the menu button labeled EXT CAL to display the EXT CAL menu.
d. Connect the STD OUTPUT of a Calibration Generator to the EXT TRIG 1 and EXT TRIG 2 input connectors through a $50 \Omega$ cable and a dual input coupler.
e. Set the Calibration Generator for a DC output (see the generator Operators manual).
f. Press the menu button labeled TRIGGER ("CONNECT TRIGS TO GND" will be displayed) and set the generator output to 0.2 mV (~GND).
g. Press the TRIGGER button again ("RUNNING" will be displayed near the lower right corner of the screen).
h. When the display changes from "CONNECT ... TO GND" to "CONNECT ... TO 0.5 V " change the generator output to 0.5 V and press the TRIGGER button.
i. When the display changes from "CONNECT ... TO 0.5 V " to "CONNECT ... TO 2.0 V " change the generator output to 2 V and press the TRIGGER button.

## NOTE

After successful completion of the Trigger Calibration sequence, "RUNNING" will disappear from the CRT screen and "PASS" will be displayed above the TRIGGER menu button label. If the calibration routine is NOT successful, "FAIL" will be displayed above the TRIGGER button label. Perform the following parts only if the instrument fails the Trigger Calibration sequence; otherwise, Trigger Calibration is complete.
j. Recheck the test setup and ensure that the Calibration Generator is set for a DC output. Reperform the Self Calibration subsection of this procedure.
k. Repeat parts a through $i$. If the instrument fails the Trigger Calibration sequence again, refer the instrument to qualified personnel for servicing; otherwise, Trigger Calibration has been successfully completed.
I. Disconnect the test setup.

## 4. Ramp (REPET) Calibration.

a. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice (two presses are necessary if any menu is presently displayed, one press if no menu is displayed) to display the Extended Functions menu.
b. Press the menu button labeled CAL/DIAG (menu will change).
c. Press the menu button labeled EXT CAL to display the EXT CAL menu.
d. Press the menu button labeled REPET. The EXT CAL menu will display "RUNNING" momentarily and then display "PASS" or "FAIL." The calibration for REPET is then complete.

## 5. CTE Calibration.

a. Press the MENU OFF/EXTENDED FUNCTIONS button once or twice to display the Extended Functions menu. (Two presses are necessary if any menu is presently displayed, one press if no menu is displayed.)
b. Press the menu button labeled CAL/DIAG (menu will change).
c. Press the menu button labeled EXT CAL to display the EXT CAL menu. Then press the menu button labeled CTE CAL. A short-synopsis of the next calibration step will be displayed.

## NOTE

The message "THIS MUST BE THE LAST STEP" also appears in the menu. It is a reminder that the CTE Calibration must be done after any adjustment of the CCD clocks or Transient response. (See steps 2 and 4 under "Internal Adjustments" in this section).
d. Connect the FAST RISE OUTPUT of a Calibration Generator to the CH 1 and CH 2 input connectors through a $50-\Omega$ cable, a 5 X attenuator, and a dual input coupler.
e. Set the Calibration Generator for a FAST RISE output at a 100 kHz frequency. Set the generator amplitude to maximum. (See the generator Operators manual as required).
f. Press the menu button that is labeled EXECUTE. ("RUNNING" will appear in the lower right corner as the calibration executes.)

## NOTE

After successful completion of the CTE Calibration sequence, "RUNNING" will disappear from the CRT screen, the instrument will switch to the Extended Calibration menu, and "PASS" will be displayed above the CTE CAL menu button label. If the calibration routine is NOT successful, "FAIL" will be displayed above the CTE CAL button label. Perform the following parts only if the instrument fails the CTE Calibration sequence; otherwise, Channel Delay Calibration is complete.
g. Recheck the test setup and ensure that the Calibration Generator is set for a fast rise output. Reperform the Self Calibration subsection of this procedure.
h. Repeat parts a through f. If the instrument fails the CTE Calibration sequence again, refer the instrument to qualified personnel for servicing; otherwise, CTE Calibration has successfully been completed.
i. Disconnect the test setup.

## MAINTENANCE

This section presents descriptive information about instrument calibration as well as preventive maintenance, corrective maintenance, and troubleshooting information. Circuit board removal procedures are included in the "Corrective Maintenance" subsection. An extensive diagnostics procedures table (Table 6-6) is in the "Diagnostics" subsection at the back of this section.

## INSTRUMENT CALIBRATION

This oscilloscope uses automatic internal routines to calibrate itself as much as possible. These automatic routines minimize manufacturing and end-user costs associated with calibration and enhance the accuracy of the instrument during use.

Instead of the usual numerous manual potentiometer "tweaks" that require extensive servicing, the scope makes wide use of digital calibration techniques. The extensive digital-to-analog (DAC) subsystem of the scope and the built-in computer firmware are used to calculate and adjust more than 100 voltages that control gain, offset, and other parameters of circuit operation affecting accuracy. The automatic SELF CAL uses no external test equipment and takes less than 10 seconds to complete. The ease of use of SELF CAL allows it to be done at any time to ensure accurate measurements in the present testing environment.

Adjustments that remain are not automatic and require manual adjustment of components and/or user-supplied external standard test signals. The display system and CCD output amplifier gains require manual "tweaking," but the instrument provides the necessary test signals internally. The vertical attenuator and trigger amplifier calibrations require external signals, but the instrument performs the adjustments internally. Finally, the CCD clocks, input capacitance, bandwidth limit filters, and transient response adjustments which affect high frequency performance require both external signals and internal manual adjustments.

## Calibration Levels

Instrument calibration occurs at several levels. These levels are the fully automatic SELF CAL, the semiautomatic EXTENDED CAL, the manual adjustments, and dynamic calibration.

## Self Calibration

Almost all of the internal measurement systems are calibrated by performing the SELF CAL procedure. These automatic adjustments include the gain and offset settings for the vertical acquisition system and the internal trigger system. No adjustments are required for the time base or horizontal subsystems.

Maximum instrument accuracy can be assured by doing a SELF CAL just before making critical measurements. Continued accuracy is maintained by running SELF CAL whenever the operating temperature has changed more than five degrees Celsius since the last SELF CAL.

## Extended Calibration

Semiautomatic calibration of the vertical attenuators (ATTEN) and external trigger amplifiers (TRIGGER) is supported by this level of calibration. The technician must connect standard DC voltage levels to the input connectors. The scope then automatically calibrates the vertical input attenuators' gain and the external trigger amplifier's gain and offset using the supplied dc voltages. During the ATTEN calibration, the accuracy of the internal 10-V Calibration Reference is verified against the standard amplitude voltage applied to the attenuators.

The EXT CAL routines also provide automatic REPET calibration and the display signals for the manual adjustments needed for the Display System and CCD output amplifier calibrations. REPET calibration adjusts the timing of the jitter correction ramps. The jitter correction ramps are used to measure the time between the randomly acquired samples and the trigger point. That time difference is used to place the waveform samples correctly with respect to the trigger point in the repetitive acquisition mode waveform record.

## Manual Adjustments

Adjustments requiring internal access to the scope are limited to the display system, CCD output amplifier gains, input capacitance, 100 MHz bandwidth limiter (and 20 MHz bandwidth limiter with the Video Option), CCD clocks, and transient response. These adjustments are made during factory calibration and should not require readjustment during normal operation. Replacement of parts during repair of the instrument that affect these calibrations will, however, require readjustment of the affected circuitry. The ADJUSTS calibration routine in the EXTENDED CALIBRATION procedures provides display patterns and brief instructions for the technician to follow in calibrating the display system and CCD output amplifier gains.

## Dynamic Adjustments

As the instrument operates, it continuously corrects for minor offsets in the acquisition system and jitter correction ramp timing. These "dynamic" adjustments are totally automatic and require no user action.

## Recommended Adjustment Intervals

Perform the ATTEN and TRIGGER parts of the Extended Calibration procedure every 2000 hours, or once a year if the instrument is used infrequently. Readjustment of the Display System and rerunning the REPET calibration step is not normally needed unless parts are replaced that affect those calibrations. It is NOT necessary to reperform any portion of the Extended Calibration to maintain maximum measurement accuracy over the specified operating temperature range of the instrument.

## NATIONAL BUREAU OF STANDARDS TRACEABILITY

Traceability to the National Bureau of Standards (NBS) requires that the stated accuracy of an instrument be established by calibration with equipment whose accuracies have been directly or indirectly established by NBS certified references.

For this oscilloscope, traceability is established in the Extended Calibration routine by calibrating the attenuators
(ATTEN) and external trigger amplifiers (TRIGGER) with an NBS traceable voltage reference. As the fine gain adjustment of the attenuators is made, the relative accuracy of the internal 10-V Calibration Reference is also checked by normalizing it to the external voltage source provided by the technician. If the fine gain of the attenuators requires an adjustment of more than approximately $2 \%$, the ATTEN calibration fails. Barring internal component problems, a failure indicates either that the internal reference is faulty or that the applied voltage is not a valid standard reference voltage.

Passing the ATTEN calibration step using an NBS traceable voltage standard ensures that the internal, nonadjustable 10-V Calibration Reference is also traceable. Subsequently passing the SELF CAL procedure (which uses the traceable 10-V Calibration Reference to provide the calibration voltages) then makes this scope an NBS traceable instrument. Traceability is maintained for subsequent performances of SELF CAL by referencing all calibration calculations to the traceable internal voltage reference.

## VOIDING CALIBRATION

Factory calibration of this scope is done using NBS traceable sources. An internal jumper installed at the time of calibration prevents the user from inadvertently running the EXT CAL routines and voiding the traceable calibration of the instrument. Removing the jumper and attempting to do the ATTEN and TRIGGER calibration without an accurate standard amplitude voltage source will result in a failed calibration. In the case of a failure, the stored constants for the attenuator gain calibration are not replaced; therefore, the previous degree of accuracy is maintained by the instrument. However, a FAIL label remains displayed over the affected EXT CAL menu choice, and the scope will fail subsequent power-on tests and enter Extended Diagnostics (EXT DIAG) until the calibration is passed.

Power-on or Self Diagnostics (SELF DIAG) tests that detect a system, subsystem, or device failure that may affect instrument calibration are noted by a FAIL label on the test along with the calibration status of UNCALD in the EXT DIAG menu display. Calibration failures are of two types: soft errors caused by gain or offset parameter drifts beyond tolerance-usually caused by a large change in
operating temperature since the last SELF CAL was done, or hard failures caused by component problems in the instrument's circuitry that prevent calibration.

## Soft Errors

These errors appear as a loss of SELF CAL and are noted by the UNCALD label appearing above the SELF CAL choice in the main CAL/DIAG menu. Running the SELF CAL routine and obtaining a PASS status clears up any soft calibration errors and revalidates the instrument calibration.

## Hard Failures

A hard failure affecting calibration may also be indicated by the loss of SELF CAL, but running the SELF CAL routine does not produce a PASS status for SELF CAL or any failed test in EXT DIAG. Loss of ATTEN or external TRIGGER calibration is noted by the UNCALD label appearing above those choices in the EXT CAL menu. A loss of calibration for either ATTEN or TRIGGER indicates a possible nonvolatile memory failure. In either case, instrument calibration should be considered void, and the scope must be referred to a qualified service person for servicing.

## STATIC-SENSITIVE COMPONENTS

The following precautions apply when performing any maintenance involving internal access to the instrument.


Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. Table 6-1 lists the relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

When performing maintenance, observe the following precautions to avoid component damage:

1. Minimize handling of static-sensitive components.
2. Transport and store static-sensitive components or assemblies in their original containers or on a metal rail. Label any package that contains static-sensitive components or assemblies.
3. Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while handling these components. Servicing static-sensitive components or assemblies should be performed only at a static-free work station by qualified service personnel.
4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.
5. Keep the component leads shorted together whenever possible.
6. Pick up components by their bodies, never by their leads.

Table 6-1
Relative Susceptibility to Static-Discharge Damage

| Semiconductor Classes | Relative <br> Susceptibility <br> Levels $^{\mathbf{a}}$ |
| :--- | :---: |
| MOS or CMOS microcircuits or <br> discretes, or linear microcircuits <br> with MOS inputs (Most Sensitive) |  |
| ECL | 1 |
| Schottky signal diodes | 2 |
| Schottky TTL | 3 |
| High-frequency bipolar transistors | 4 |
| JFET | 5 |
| Linear microcircuits | 6 |
| Low-power Schottky TTL | 7 |
| TTL | 8 |

Voltage equivalent for levels (voltage discharged from a 100 pF capacitor through a resistance of $\mathbf{1 0 0} \mathbf{~ o h m s}$ ):

$$
\begin{array}{lll}
1=100 \text { to } 500 \mathrm{~V} & 4=500 \mathrm{~V} & 7=400 \text { to } 1000 \mathrm{~V} \text { (est) } \\
2=200 \text { to } 500 \mathrm{~V} & 5=400 \text { to } 600 \mathrm{~V} & 8=900 \mathrm{~V} \\
3=250 \mathrm{~V} & 6=600 \text { to } 800 \mathrm{~V} & 9=1200 \mathrm{~V}
\end{array}
$$

7. Do not slide the components over any surface.
8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.
9. Use a soldering iron that is connected to earth ground.
10. Use only approved antistatic, vacuum-type desoldering tools for component removal.

# PREVENTIVE MAINTENANCE 

## INTRODUCTION

Preventive maintenance consists of cleaning, visual inspection, and checking instrument performance. When performed regularly, it may prevent instrument malfunction and enhance instrument reliability. The severity of the environment in which the instrument is used determines the required frequency of maintenance. An appropriate time to perform preventive maintenance is just before instrument adjustment.

## GENERAL CARE

The cabinet minimizes accumulation of dust inside the instrument and should normally be in place when operating the oscilloscope. The instrument's front cover protects the front panel and crt from dust and damage. It should be installed whenever the instrument is stored or transported.

## INSPECTION AND CLEANING

The scope should be visually inspected and cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket, preventing efficient heat dissipation. It also provides an electrical conduction path that could result in instrument failure, especially under highhumidity conditions.


Avoid the use of chemical cleaning agents which might damage the plastics used in this instrument. Use a nonresidue-type cleaner, preferably isopropyl alcohol or a solution of $1 \%$ mild detergent with $99 \%$ water. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

## Exterior

INSPECTION. Inspect the external portions of the instrument for damage, wear, and missing parts; use Table 6-2 as a guide. Instruments that appear to have been dropped or otherwise abused should be checked thoroughly to verify correct operation and performance. Repair deficiencies that could cause personal injury or lead to further damage to the instrument immediately.


To prevent getting moisture inside the instrument during external cleaning, use only enough liquid to dampen the cloth or applicator.

CLEANING. Loose dust on the outside of the instrument can be removed with a soft cloth or small soft-bristle brush. The brush is particularly useful for dislodging dirt on and around the controls and connectors. Dirt that remains can be removed with a soft cloth dampened in a mild detergent-and-water solution. Do not use abrasive cleaners.

Two plastic light filters, one blue and one clear, are provided with the oscilloscope. Clean the light filters and the crt face with a soft lint-free cloth dampened with either isopropyl alcohol or a mild detergent-and-water solution.

## Interior

To access the inside of the instrument for inspection and cleaning, refer to the "Removal and Replacement Procedure" in the "Corrective Maintenance" part of this section.

INSPECTION. Inspect the internal portions of the scope for damage and wear, using Table 6-3 as a guide. Deficiencies found should be repaired immediately. The
corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the instrument; it is important, therefore, that the cause of overheating be corrected to prevent recurrence of the damage.

If any electrical component is replaced, conduct a Performance Check for the affected circuit and for other closely related circuits (see Section 4). If repair or replacement work is done on any of the power supplies, verify that the affected power supply meets the voltage and ripple tolerance requirements under Specification in Section 1 of this manual.

To prevent damage from electrical arcing, ensure that circuit boards and components are dry before applying power to the instrument.

CLEANING. To clean the interior, blow off dust with dry, low-pressure air (approximately 9 psi). Remove any remaining dust with a soft brush or a cloth dampened with a solution of mild detergent and water. A cotton-tipped applicator is useful for cleaning in narrow spaces and on circuit boards. If these methods do not remove all the dust or dirt, the instrument may be spray washed using a solution of $5 \%$ mild detergent and $95 \%$ water as follows:

Exceptions to the following cleaning procedure are the CH 1 and CH 2 Attenuator assemblies. Clean these assemblies only with isopropyl alcohol as described in Step 4 of the cleaning procedure. In addition, all other Front Panel controls are sealed and require no maintenance.

1. Gain access to the parts to be cleaned by removing easily accessible shields and panels (see "Removal and Replacement Procedure').
2. Spray wash dirty parts with the detergent-and-water solution; then use clean water to thoroughly rinse them.
3. Dry all parts with low-pressure air.
4. Clean switches with isopropyl alcohol and wait 60 seconds for the majority of the alcohol to evaporate. Then complete drying with low-pressure air.
5. Dry all components and assemblies in an oven or drying compartment using low-temperature $\left(125^{\circ} \mathrm{F}\right.$ to $150^{\circ} \mathrm{F}$ ) circulating air.

Table 6-2
External Inspection Check List

| Item | Inspect For | Repair Action |
| :--- | :--- | :--- |
| Cabinet, Front Panel, <br> and Cover | Cracks, scratches, deformations, damaged <br> hardware or gaskets. | Touch up paint scratches and replace <br> defective components. |
| Front-panel Controls | Missing, damaged, or loose knobs, buttons, <br> and controls. | Repair or replace missing or defective <br> items. |
| Connectors | Broken shells, cracked insulation, and <br> deformed contacts. Dirt in connectors. | Replace defective parts. Clear or wash out <br> dirt. |
| Carrying Handle | Correct operation. | Replace defective parts. |
| Accessories | Missing items or parts of items, bent pins, <br> broken or frayed cables, and damaged con- <br> nectors. | Replace damaged or missing items, frayed <br> cables, and defective parts. |

Table 6-3
Internal Inspection Check List

| Item | Inspect For | Repair Action |
| :--- | :--- | :--- |
| Circuit Boards | Loose, broken, or corroded solder connec- <br> tions. Burned circuit boards. Burned, bro- <br> ken, or cracked circuit-run plating. | Clean solder corrosion with an eraser and <br> flush with isopropyl alcohol. Resolder defec- <br> tive connections. Determine cause of <br> burned items and repair. Repair defective <br> circuit runs. |
| Resistors | Burned, cracked, broken, blistered. | Replace defective resistors. Check for <br> cause of burned component and repair as <br> necessary. |
| Solder Connections | Cold solder or rosin joints. | Resolder joint and clean with isopropyl <br> alcohol. |
| Capacitors | Damaged or leaking cases. Corroded solder <br> on leads or terminals. | Replace defective capacitors. Clean solder <br> connections and flush with isopropyl <br> alcohol. |
| Semiconductors | Loosely inserted in sockets. Distorted pins. | Firmly seat loose semiconductors. Remove <br> devices having distorted pins. Carefully <br> straighten pins (as required to fit the |
| socket), using long-nose pliers, and reinsert |  |  |
| firmly. Ensure that straightening action |  |  |
| does not crack pins, causing them to break |  |  |
| off. |  |  |

## LUBRICATION

There is no periodic lubrication required for this instrument.

## SEMICONDUCTOR CHECKS

Periodic checks of the transistors and other semiconductors in the oscilloscope are not recommended. The best check of semiconductor performance is actual operation in the instrument.

## PERIODIC READJUSTMENT

To ensure accurate measurements, check the performance of this instrument every 2000 hours of operation, or if used infrequently, once each year. In addition, replacement of components may necessitate readjustment of the affected circuits.

Complete Performance Check and Adjustment procedures are given in Sections 4 and 5. The Performance Check Procedure can also be helpful in localizing certain troubles in the instrument. In some cases, minor problems may be revealed or corrected by readjustment.

## TROUBLESHOOTING

## INTRODUCTION

Preventive maintenance performed on a regular basis should reveal most potential problems before an instrument malfunctions. However, should troubleshooting be required, the following information is provided to facilitate location of a fault. In addition, the material presented in the "Theory of Operation" and "Diagrams" sections of this manual may be helpful while troubleshooting.

## TROUBLESHOOTING AIDS

## Diagnostic Firmware

The operating firmware in this instrument contains diagnostic routines that aid in locating malfunctions. When instrument power is applied, power-up tests are performed to verify proper operation of the instrument. If a failure is detected, this information is passed on to the operator in the form of a CRT readout error message. The failure information directs the troubleshooter to the area of failing circuitry. If the failure is such that the processor can still execute the diagnostic routines, the user can call up specific tests to further check the failing circuitry. The specific diagnostic routines are explained later in this section.

## Schematic Diagrams

Complete schematic diagrams are located on tabbed foldout pages in the "Diagrams" section. Heavy black lines that enclose portions of the circuitry represent the circuit board on which the enclosed circuitry is mounted. The assembly number and name of the circuit board are shown near either the top or the bottom edge of the diagram.

Functional blocks on schematic diagrams are outlined with a wide grey line. Components within the outlined area perform the function designated by the block label. The "Detailed Block Diagram Description" in the "Theory of Operation" uses these functional block names when describing circuit operation, aiding in cross-referencing between the two circuit descriptions and the schematic diagrams.

Component numbers and electrical values of components in this instrument are shown on the schematic diagrams. Refer to the first page of the "Diagrams" section for the reference designators and symbols used to identify components. Important voltages and waveform
reference numbers (enclosed in hexagonally-shaped boxes) are also shown on each diagram. Waveform illustrations are located adjacent to their respective schematic diagram.

## Circuit Board Illustrations

Circuit board illustrations showing the physical location of each component are provided for use in conjunction with each schematic diagram. Each board illustration is found in the "Diagrams" section on the back of a foldout page, preceding the first schematic diagram(s) to which it relates.

The locations of waveform test points are marked on the circuit board illustrations with hexagonally outlined numbers corresponding to the waveform numbers on both the schematic diagram and the waveform illustrations.

## Circuit Board Locations

The placement of each circuit board in the instrument is shown in a board locator illustration. This illustration is located on the foldout page along with the circuit board illustration.

## Circuit Board Interconnections

A circuit board interconnection diagram is provided in the "Diagrams" section to aid in tracing a signal path or power source between boards. All wire, plug, and jack numbers are shown along with their associated wire or pin numbers.

## Power Distribution

Power distribution is traceable through the schematic diagrams in the "Diagrams' section. The low-voltage power supplies originate on the Power Supply board and are schematically illustrated in diagrams 22 and 23. The high-voltage and +61 V power supplies, originating on the High Voltage board, are shown in diagram 19. Any power supply can be tracked back to its diagram and forward to other circuitry illustrated on different diagrams.

Power is distributed to the different circuit boards through interconnect assemblies consisting of one or more connectors. The diagrams showing these assemblies (or partial assemblies) provide the interconnecting assembly (wire, plug, and/or jack) numbers, as well as the number
for the individual pins or wires distributing the supplies. By referencing the numbers for the assembly and its connector wire(s), the diagram showing that section of the power distribution path immediately preceding the section illustrated (on a given diagram) can be determined.

If power is carried to another interconnect assembly and on to another circuit board, that distribution is shown. The other interconnect assembly and conductors are labeled as previous described, except the an individual connector number indicates the diagram showing the succeeding distribution path section rather than the preceding section. This method allows the tracing of power distribution either up the path towards the originating supply, or away (further down the distribution path) from that supply.

In some cases, the diagram showing an interconnect assembly carrying power to a circuit board may not illustrate all of that circuit board. Arrows pointing to diagram numbers indicate other schematic diagrams (illustrating other parts of the circuit board) where the supplies are routed. Further, any diagram showing a partial circuit board will indicate the number of the diagram where the interconnect assembly(ies) routing power supplies to that board is illustrated. This method allows tracing power distribution back to an interconnect assembly, at which point further distribution tracing can occur.

As a further aid to power supply distribution, the "Diagrams" section contains an interconnect diagram. This diagram shows all of the interconnections between the various circuit board assemblies, including the power supplies. This diagram can also be an aid in power distribution tracing.

## Grid Coordinate System

Each schematic diagram and circuit board illustration has a grid border along its left and top edges. A table located adjacent to each diagram lists the grid coordinates of each component shown on that diagram. To aid in physically locating components on the circuit board, this table also lists the grid coordinates of each component on the circuit board illustration.

Near each circuit board illustration is an alphanumeric listing of all components mounted on that board. The second column in each listing identifies the schematic diagram in which each component can be found. These component-locator tables are especially useful when more than one schematic diagram is associated with a particular circuit board.

## Troubleshooting Charts

The troubleshooting charts contained in the "Diagrams" section are to be used in conjunction with the Extended Diagnostics of Table 6-6 (at the back of this section) as an aid in locating malfunctioning circuitry. To use the charts, begin with the initial Troubleshooting Guide shown in Figure 6-6. This guide will help identify problem areas and will direct you to the appropriate procedures for further troubleshooting.

## Component Color Coding

Information regarding color codes and markings of resistors and capacitors is located on the color-coding illustration (Figure 9-1) at the beginning of the "Diagrams" section.

## Semiconductor Lead Configurations

Figure 9-2 in the "Diagrams" section shows the lead configurations for most types of semiconductor devices used in the instrument. Vendor changes and performance improvement changes may result in changes of case styles or lead configurations. If the device in question does not appear to match a configuration shown in Figure 9-2 examine the associated circuitry or consult a manufacturer's data sheet to obtain the pin nomenclature.

## Multipin Connectors

Multipin connector orientation is indexed by two triangles; one on the holder and one on the circuit board. Slot numbers are usually molded into the holder. When a connection is made to circuit board pins, ensure that the index on the holder is aligned with the index on the circuit board (see Figure 6-1).


Figure 6-1. Multipin connector.

## TROUBLESHOOTING EQUIPMENT

The equipment listed in Table 4-1 of this manual, or equivalent equipment, may be useful when troubleshooting this instrument.

## TROUBLESHOOTING TECHNIQUES

In the following list of troubleshooting procedures, the first two steps use diagnostic aids inherent in the instrument's operating firmware. These built-in tests can locate many circuit faults to aid in isolating the problem circuitry. The next four procedures are check steps that ensure proper control settings, connections, operation, and adjustment. If the trouble is not located by these checks, the remaining steps will aid in locating the defective component. When the defective component is located, replace it using the appropriate replacement procedure given under "Corrective Maintenance" in this section.


Before using any test equipment to make measurements on static-sensitive, current-sensitive, or voltage-sensitive components or assemblies, ensure that any voltage or current supplied by the test equipment does not exceed the limits of the component to be tested.

## 1. Power-up Tests

This scope performs automatic verification of the instrument. If a failure occurs, refer to the "Calibration and Diagnostics" discussion later in this section for interpreting the failure.

If a problem is found, the associated troubleshooting procedure may be used to isolate the problem. The troubleshooting procedures are found in Table 6-6 (located in the "Diagnostics" subsection). See Figure 6-6 (also in the Diagnostics subsection) for the Initial Troubleshooting Guide.

## 2. Diagnostic Test Routines.

The instrument firmware contains diagnostic routines that may be selected by the user from the front panel to further clarify the nature of a suspected failure. The desired test is selected using the MENU buttons after entering the Extended Diagnostics Mode. Entry into the Diagnostic Mode and its uses are explained in the "Calibration and Diagnostics' discussion later in this section.

## 3. Check Control Settings

Incorrect control settings can give a false indication of instrument malfunction. If there is any question about the correct function or operation of any control, refer to either the "Operating Information" in Section 2 of this manual or to the scope's Operators Manual.

## 4. Check Associated Equipment

Before proceeding, ensure that any equipment used with the scope is operating correctly. Verify that input signals are properly connected and that the interconnecting cables are not defective. Check that the ac-power-source voltage to all equipment is correct.

## 5. Visual Check

## WARNING

To avoid electrical shock, disconnect the instrument from the ac power source before making a visual inspection of the internal circuitry.

Perform a visual inspection. This check may reveal broken connections or wires, damaged components, semiconductors not firmly mounted, damaged circuit boards, or other clues to the cause of an instrument malfunction.

## 6. Check Instrument Performance and Adjustment

Check the performance of those areas where trouble appears to exist. The trouble condition observed may be the result of a lack of calibration. Complete Performance Check and Adjustment procedures are given in Sections 4 and 5 of this manual respectively.

## 7. Isolate Trouble to a Circuit

To isolate problems to a particular area, use any symptoms noticed to help locate the trouble. Refer to the Extended Diagnostics table (Table 6-6) in the "Calibration and Diagnostics" discussion in this section as an aid in locating a faulty circuit.

## 8. Check Power Supplies

## WARNING

For safety reasons, an isolation transformer must be connected whenever troubleshooting in the Preregulator and Inverter Power Supply sections of the instrument.

When trouble symptoms appear in more than one circuit, first check the power supplies; then check the affected circuits by taking voltage and waveform readings. Check first for the correct output voltage of each individual supply; then measure ac ripple to check that it is within the Total Peak-to-Peak Ripple specification. Table 6-4 lists the power supply voltage level and ripple limits for each supply.

These voltages are measured between the power supply test points (most of which are located on the Side Board near the Front Panel $\mu \mathrm{P}$ ) and ground. Voltage ripple amplitudes must be measured using an oscilloscope. Before measuring ac ripple, set the STORAGE ACQUIRE mode of the 2440 to SAVE. Use a 1 X probe having as short a ground lead as possible to minimize stray pickup.

## NOTE

The oscilloscope used to measure ripple must be bandwidth limited to 20 MHz . Use of a higher bandwidth oscilloscope without 20 MHz bandwidth limiting will result in higher readings.

Table 6-4
Power Supply Voltage and Ripple Limitsa

| Power <br> Supply | Reading <br> (Volts) | P-P <br> Ripple <br> (mV) |
| :--- | :---: | :---: |
| +61 V | 59.05 to 62.95 | 100 |
| +15 V | 14.74 to 15.26 | 10 |
| +10 V Ref | 9.97 to 10.03 | 10 |
| +8 V | 7.85 to 8.15 | 10 |
| +5 V | 4.91 to 5.09 | 10 |
| +5 VD | 4.83 to 5.17 | 150 |
| digital) | -4.95 to -5.05 | 10 |
| -5 V | -7.85 to -8.15 | 10 |
| -8 V | -14.74 to -15.26 | 10 |
| -15 V |  | 350 |
| -15 V unreg | -1855 to -1945 |  |
| -1900 V |  |  |

${ }^{\circ}$ At $25^{\circ} \mathrm{C}$.

If the power-supply voltages and ripple are within the listed ranges in Table 6-4, the supply can be assumed to be working correctly. If the supply is not within specified ranges, the fault may or may not be located in the power supply circuitry. A defective component elsewhere in the instrument can create the appearance of a power-supply problem and may also affect the operation of other circuits. Use the power supply troubleshooting charts to aid in locating the problem.

## 9. Check Circuit Board Interconnections

After the trouble has been isolated to a particular circuit, again check for loose or broken connections, improperly seated semiconductors, and heat-damaged components.

## 10. Check Voltages and Waveforms

Often the defective component can be located by checking circuit voltages or waveforms. Typical voltages are listed on the schematic diagrams. Waveforms indicated on the schematic diagrams by hexagonally outlined numbers are shown adjacent to the diagrams. Waveform test points are shown on the circuit board illustrations.

## NOTE

Voltages and waveforms indicated on the schematic diagrams are not absolute and may vary slightly between instruments. To establish operating conditions similar to those used to obtain these readings, set up the Test scope and the 2440 under test as indicated near the waveform illustrations for a schematic diagram.

## 11. Check Individual Components

WARNING

To avoid electric shock, always disconnect the instrument from the ac power source before removing or replacing components.


When checking semiconductors, observe the staticsensitivity precautions located at the beginning of this section.

To accurately check components, it is often necessary to remove or partially disconnect the component from the circuit board, in order to isolate it from surrounding circuitry. Partial specifications (resistor tolerance, transistor type, etc.) for most components can be found by referencing the component designation number in the "Replaceable Electrical Parts." Also see Figure 9-1 for component value identification and Figure 9-2 for semiconductor lead configurations.

## 12. Repair and Adjust the Circuit

If any defective parts are located, follow the replacement procedures given under "Corrective Maintenance" in this section. After any electrical component has been replaced, the performance of that circuit and any other closely related circuit should be checked. If work has been done on the power supplies, a complete check of the regulated voltages should be done to verify that the supply voltages are in tolerance. A check of the Display ADJUSTS calibration and a SELF CAL should verify that the instrument meets Performance Requirements if the voltages are all correct.

## CORRECTIVE MAINTENANCE

## INTRODUCTION

Corrective maintenance consists of component replacement and instrument repair. This part of the manual describes special techniques and procedures required to replace components in this instrument. If it is necessary to ship your instrument to a Tektronix Service Center for repair or service, refer to the "Repackaging for Shipment" information in Section 2 of this manual.

## MAINTENANCE PRECAUTIONS

To reduce the possibility of personal injury or instrument damage, observe the following precautions:

1. Disconnect the instrument from the ac-power source before removing or installing components.
2. Verify that the line-rectifier filter capacitors are discharged prior to performing any servicing.
3. Use care not to interconnect instrument grounds which may be at different potentials (cross grounding).
4. When soldering on circuit boards or small insulated wires, use only a 15-watt, pencil-type soldering iron.
5. Use an isolation transformer to supply power to the 2440 if removing the shield and troubleshooting in the power supply.

## OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts can be obtained through your local Tektronix Field Office or representative. However, many of the standard electronic components can usually be obtained from a local commercial source. Before purchasing or ordering a part from a source other than Tektronix, Inc., please check the "Replaceable Electrical Parts" list for the proper value, rating, tolerance, and description.

## NOTE

Physical size and shape of a component may affect instrument performance, particularly at high frequencies. Always use direct-replacement components, unless it is known that a substitute will not degrade instrument performance.

## Special Parts

In addition to the standard electronic components, many special parts are used in this scope. These components are manufactured or selected by Tektronix, Inc. to meet specific performance requirements, or are manufactured for Tektronix, Inc. in accordance with our specifications. The various manufacturers can be identified by referring to the "Cross Index-MFR Code Number to Manufacturer" at the beginning of the "Replaceable Electrical Parts" list. Most of the mechanical parts used in this instrument were manufactured by Tektronix, Inc. Order all special parts directly from your local Tektronix Field Office or representative.

## Ordering Parts

When ordering replacement parts from Tektronix, Inc., be sure to include all of the following information:

1. Instrument type (include modification or option numbers).
2. Instrument serial number.
3. A description of the part (if electrical, include its full circuit component number).
4. Tektronix part number.

## MAINTENANCE AIDS

The maintenance aids listed in Table 6-5 include items required for performing most of the maintenance procedures in this instrument. Equivalent products may be substituted for the examples given, provided their characteristics are similar.

## INTERCONNECTIONS

Interconnections in this instrument are made with pins soldered onto the circuit boards. Several types of mating
connectors are used for the interconnecting pins. The following information provides the replacement procedures for the various types of connectors.

## End-Lead Pin Connectors

Pin connectors used to connect the wires to the interconnect pins are factory assembled. They consist of machine-inserted pin connectors mounted in plastic holders. If the connectors are faulty, the entire wire assembly should be replaced.

## Multipin Connectors

When pin connectors are grouped together and mounted in a plastic holder, they are removed, reinstalled, or replaced as a unit. If any individual wire or connector in the assembly is faulty, the entire cable assembly should be replaced. To provide correct orientation of a multipin connector, an index arrow is stamped on the circuit board, and either a matching arrow is molded into or the numeral 1 is marked on the plastic housing as a matching index. Be sure these index marks are aligned with each other when the multipin connector is reinstalled.

## TRANSISTORS AND INTEGRATED CIRCUITS

Transistors and integrated circuits should not be replaced unless they are actually defective. If removed from their sockets or unsoldered from the circuit board during routine maintenance, return them to their original board locations. Unnecessary replacement or transposing of semiconductor devices may affect the adjustment of the instrument. When a semiconductor is replaced, check the performance of any circuit that may be affected.

Any replacement component should be of the original type or a direct replacement. Bend transistor leads to fit their circuit board holes, and cut the leads to the same length as the original component. See Figure 9-2 in the "Diagrams" section for lead-configuration illustrations.


After replacing a power transistor, check that the collector is not shorted to the chassis before applying power to the instrument.

Table 6-5
Maintenance Aids

| Description | Specification | Usage | Example |
| :---: | :---: | :---: | :---: |
| 1. Soldering Iron | 15 to 25 W . | General soldering and unsoldering. | Antex Precision Model C. |
| 2. Torx Screwdrivers | Torx tips \#T7, \#T9, \#T10, \#T15, and \#T20. | Assembly and disassembly. | Tektronix Part Numbers: 003-1293-00 <br> 003-0965-00 <br> 003-0814-00 <br> 003-0966-00 <br> 003-0866-00. |
| 3. Nutdrivers | 1/4 inch, $7 / 32$ inch, $5 / 16$ inch, $1 / 2$ inch, and 9/16 inch. | Assembly and disassembly. | Xcelite \#7, \#8, \#10, \#16, and \#18. |
| 4. Open-end Wrench | 9/16 inch and 1/2 inch. | Channel Input and Ext Trig BNC Connectors. | Tektronix Part Numbers: 9/16 in. 003-0502-00 1/2 in. 003-0882-00. |
| 5. Hex Wrenches | 0.050 inch, $1 / 16$ inch. | Assembly and disassembly. | Allen Wrenches. |
| 6. Long-nose Pliers |  | Component removal and replacement. | Diamalloy Model LN55-3. |
| 7. Diagonal Cutters |  | Component removal and replacement. | Diamalloy Model M554-3. |
| 8. Vacuum Solder Extractor | No static charge retention. | Unsoldering static sensitive devices and components on multilayer boards. | Pace Model PC-10. |
| 9. Contact Cleaner and lubricant | No-Noise R. | Switch and pot cleaning and lubrication. | Tektronix Part Number: 006-0442-02. |
| 10. Pin-Replacement Kit |  | Replace circuit board connector pins. | Tektronix Part Number: 040-0542-00. |
| 11. IC-Removal Tool |  | Removing DIP IC packages. | Augat T114-1. |
| 12. Isopropyl Alcohol | Reagent grade. | Cleaning attenuator and front-panel assemblies. | 2-isopropanol. |
| 13. Isolation Transformer ${ }^{\text {a }}$ |  | Isolate the instrument from the ac power source for safety. | Tektronix Part Number 006-5953-00. |
| 14. $1 \times$ Probe |  | Power supply ripple check. | TEKTRONIX P6101 Probe (1X) Part Number 010-610103. |

[^8]The chassis-mounted power supply transistor is insulated from the chassis by a heat-transferring mounting block. Reinstall the mounting block and bushings when replacing these transistors. Use a thin layer of heattransferring compound between the insulating block and chassis when reinstalling the block.

To remove socketed dual-in-line packaged (DIP) integrated circuits, pull slowly and evenly on both ends of the device. Avoid disengaging one end of the integrated circuit from the socket before the other, since this may damage the pins.

To remove a soldered DIP IC when it is going to be replaced, clip all the leads of the device and remove the leads from the circuit board one at a time. If the device must be removed intact for possible reinstallation, do not heat adjacent conductors consecutively. Apply heat to pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

Use rosin-core wire solder containing 63\% tin and 37\% lead. Contact your local Tektronix Field Office or representative to obtain the names of approved solder types.

When soldering on circuit boards or small insulated wires, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron may cause etched circuit conductors to separate from the board base material and melt the insulation on small wires. Always keep the soldering-iron tip properly tinned to ensure best heat transfer from the iron tip to the solder joint. Apply only enough solder to make a firm joint. After soldering, clean the area around the solder connection with an approved flux-removing solvent (such as isopropyl alcohol) and allow it to air dry.

Only an experienced maintenance person, proficient in the use of vacuum-type desoldering equipment should attempt repair of any circuit board in this instrument. Many integrated circuits are static sensitive and may be damaged by solder extractors that generate static charges. Perform work involving static-sensitive devices only at a static-free work station while wearing a grounded antistatic wrist strap. Use only an antistatic vacuum-type solder extractor approved by a Tektronix Service Center.

## SOLDERING TECHNIQUES

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used to remove or replace parts. General soldering techniques, which apply to maintenance of any precision electronic equipment, should be used when working on this instrument.

## wanning

To avoid an electric-shock hazard, observe the following precautions before attempting any soldering: turn the instrument off, disconnect it from the ac power source, and wait at least three minutes for the line-rectifier filter capacitors to discharge.

The following techniques should be used to replace a component on a circuit board:

1. Touch the vacuum desoldering tool to the lead at the solder connection. Never place the iron directly on the board; doing so may damage the board.

## NOTE

Some components are difficult to remove from the circuit board due to a bend placed in the component leads during machine insertion. To make removal of machine-inserted components easier, straighten the component leads on the reverse side of the circuit board.
2. When removing a multipin component, especially an IC, do not heat adjacent pins consecutively. Apply heat to the pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

Excessive heat can cause the etched circuit conductors to separate from the circuit board. Never allow the solder extractor tip to remain at one place on the board for more than three seconds. Solder wick, spring-actuated or squeeze-bulb solder suckers, and heat blocks (for desoldering multipin components) must not be used. Damage caused by poor soldering techniques can void the instrument warranty.
3. Bend the leads of the replacement component to fit the holes in the circuit board. If the component is replaced while the board is installed in the instrument, cut the leads so they protrude only a small amount through the reverse side of the circuit board. Excess lead length may cause shorting to other conductive parts.
4. Insert the leads into the holes of the board so that the replacement component is positioned the same as the original component. Most components should be firmly seated against the circuit board.
5. Touch the soldering iron to the connection and apply enough solder to make a firm solder joint. Do not move the component while the solder hardens.
6. Cut off any excess lead protruding through the circuit board (if not clipped to the correct length in Step 3).
7. Clean the area around the solder connection with an approved flux-removing solvent. Be careful not to remove any of the printed information from the circuit board.

## REMOVAL AND REPLACEMENT PROCEDURE

Read these instructions completely before attempting any corrective maintenance.

## WARNING

To avoid electric shock, disconnect the instrument from the ac power source before removing or replacing any component or assembly.

The exploded view drawing in the "Replaceable Mechanical Parts" list at the rear of this manual may be helpful during the removal and installation of individual components or subassemblies. Figure 6-2 illustrates the locations of the circuit boards referred to in this procedure. Individual circuit boards are illustrated in the "Diagrams" section of this manual; those illustrations are useful in location of the components referred to in this procedure.

As a further aid in component location, this procedure specifies the location of most of the components to be disconnected. The component side of a circuit board is referred to as the "top" side of the board; the edge nearest the Front Panel is the front edge. The remaining sides and edges follow from this orientation.


Figure 6-2. Circuit Board Location.

## 1. Cabinet Removal

a. Disconnect the power cord from any ac power source.
b. Disconnect the power cord from its receptacle at the instrument's Rear panel.
c. Grasp the power cord plug (female end), rotate the power cord retainer $1 / 4$ turn, and pull it to remove the cord from the Rear panel.
d. Grasp the handle hubs (at right and left side of the instrument) and pull outward. Rotate the hubs to position the front of the handle away from the front of the instrument.
e. Install the protective Front cover over the Front panel. Push on the cover to lock the cover's side tabs around the Front panel's trim band.
f. Set the instrument so it rests on the Front cover.
g. Remove the four screws inside the four rear feet at the instrument's back panel.

## WARNING

Dangerous potentials exist at several points throughout this instrument. If it is operated with the cabinet removed, do not touch exposed connections or components. Some transistors may have elevated case voltages. Disconnect the ac power source from the instrument and verify that the line-rectifier filter capacitors have discharged before cleaning the instrument or replacing parts (see label on the Low Voltage Power Supply cover).
h. Grasp the handle hubs (at right and left sides of the instrument) and pull outward. While hoiding the hubs outward, pull straight up from the rear of the cabinet to remove the cabinet from the instrument.

Reverse parts a through $h$ to install the cabinet.

## WARNING

The line-rectifier capacitors normally retain a charge for several minutes after the instrument is powered off and can remain charged for a longer period if a bleeder resistor or other power supply problem occurs. Before beginning any cleaning or work on the internal circuitry of the instrument, discharge the capacitors by connecting a shorting strap in series with a 1 kJ , 5 watt resistor across the capacitors. Connect one end of the shorting strap/resistor combination to upper-most terminal of S1020 (the terminal connected through a wire to W310). Connect the other end to pin 11 of T117 (the pin protruding from the side of the transformer, near its right-rear corner). Measure across those two connections with a voltmeter to ensure the capacitors are discharged.

## 2. Timebase/Display Board Removal

a. Perform Step 1 to remove the cabinet.
b. Set the instrument on a flat, smooth surface, with its underside facing down and the Front panel facing forward.
c. Disconnect the ribbon-cable connector from J 100 of the Timebase/Display board. J 100 is located at the rightfront corner of the Timebase/Display board.
d. Disconnect the ribbon cable connector at J141 of the Main board. J141 is located at the lower right-rear corner of the instrument.
e. Disconnect the ribbon cable connector at J 121 of the Timebase/Display board. J 121 is located at the rightrear corner of the board, under the ribbon cable disconnected in part d.
f. Disconnect P117 and P148 from J117 and J148. J 117 and J148 are located on the Timebase/Display board, at the right-rear corner and center-rear edge, respectively.
g. Remove the three mounting screws securing the Timebase/Display board to the Center chassis and Power Supply.
h. Using a $7 / 32$ inch nutdriver, rotate the two black plastic retaining latches counterclockwise $1 / 4$ turn to unlock them. The two retaining latches are located near the left-front and left-rear corners of the Timebase/Display board.
i. Grasp the left edge of the Timebase/Display board and rotate it (and the Top chassis) upward about 45 degrees. While supporting the Top chassis, disconnect the ribbon cable connector at J 131 (left-front corner of the Timebase/Display board) and the flex cable at J 125 (rightrear corner of the Processor board on the underside of the Top chassis).
j. Continue to rotate the Top chassis until it is at a 90 degree angle to the top of the instrument.
k. Rotate the black retaining latch (center-left edge of the Timebase/Display board) $1 / 4$ turn counterclockwise to release the board from the Top chassis.
I. Grasp the left edge of the board and pull it slightly away from the Top chassis until it clears the head of the retaining latch unlocked in part k. Pull up on the board until the right edge of the board slips out of the four channel notches on the Top chassis.

Reverse parts a through I to install the board to the Top chassis and to secure the Top chassis to the Center chassis. Take care to fit the right edge of the board to the four channel notches when installing the board on the Top chassis.

## 3. Processor Board Removal

a. Perform Step 1 to remove the cabinet.
b. Set the instrument on a flat, smooth surface, with its underside facing down and the Front panel facing forward.
c. Remove the three mounting screws securing the Timebase/Display board to the Center chassis and Power Supply.
d. Using a $7 / 32$ inch nutdriver, rotate the two black retaining latches counterclockwise $1 / 4$ turn to unlock them. The two retaining latches are located near the left-front and left-rear corners of the Timebase/Display board.
e. Grasp the left edge of the Timebase/Display board and rotate it (and the Top chassis) upward about 45 degrees. While supporting the Top chassis, disconnect the ribbon cable connector at J 131 (left-front corner of the Timebase/Display board) and the flex cable at J125 (right rear corner of the Processor board on the underside of the Top chassis).
f. Continue to rotate the Top chassis until it is at a 180 degree angle to the top of the instrument. The top of the Processor board is now exposed.
g. Disconnect the ribbon-cable connector from J103 and the flex cable connector from J207 of the Processor board. J103 and J207 are located at the left-front corner of the board.
h. Disconnect the ribbon cable connector at J123 of the Processor board (instruments with Option 05 installed only). J123 is located at the rear quarter section of the board near the center.
i. Disconnect the ribbon cable connectors at J181 and J 120 of the Processor board. J181 and J120 are located at the left rear corner of the board.
j. Rotate the black retaining latch (center-right edge of the Processor board) $1 / 4$ turn counterclockwise to release the board from the Top chassis.
k. Grasp the right edge of the board and pull it slightly away from the Top chassis until it clears the head of the retaining latch unlocked in part $\mathbf{j}$. Pull up on the board until the left edge of the board slips out of the four channel notches on the Top chassis.

Reverse parts a through $k$ to install the board on the Top chassis and to secure the Top chassis to the Center chassis. Take care to fit the edge of the board to the four channel notches when installing it on the Top chassis.

## 4. Front Panel Board Removal

a. Perform Step 1 to remove the cabinet from the instrument.
b. Set the instrument on a flat, smooth surface, with its underside facing down and the Front panel facing forward.
c. Pull straight out on the INTENSITY control knob to remove it from its shaft.
d. Using a small, flat-bladed screwdriver, gently pry loose and remove the top trim cover.
e. Remove the four screws exposed by part d.
f. Turn the instrument over to expose the bottom of the trim ring and remove the two screws securing the front feet to the instrument. Remove the feet from the trim ring.
g. Remove the two remaining screws securing the trim ring.
h. Grasp the edges of the trim ring and pull forward to remove it from the Front casting.
i. Turn the instrument over so its top side is up.
j. Remove the three mounting screws securing the Timebase/Display board to the Center chassis.
k. Using a $7 / 32$ inch nutdriver, rotate the two black retaining latches counterclockwise $1 / 4$ turn to unlock them. The two retaining latches are located near the left-front and left-rear corners of the Timebase/Display board.
I. Grasp the left edge of the Timebase/Display board and rotate it (and the TOp chassis) upward about 45 degrees. While supporting the Top chassis, disconnect the flex cable at J125 (right-rear corner of the Processor board on the underside of the Top chassis).
m . Continue to rotate the Top chassis until it is at a 180 degree angle to the top of the instrument.
n. Disconnect the ribbon cable connector from J166 on the Low Voltage Power Supply board and push it towards the rear of the instrument. J166 is located at the left-front section of the board near the front corner of the Center chassis.
o. Disconnect the ribbon cable connector from J150 at the front of the Side board.
p. Remove the anode lead from its retainer and dress it away from the lower square hole in the Main chassis. Take care not to separate the male end of that lead from the female end.
q. Disconnect the ribbon cable connector from J152 of the Main board. J 152 is located in front of the High Voltage shield, at the lower left side of the instrument.
r. Carefully route the connectors disconnected in parts 0 and q to the inside of the instrument.
s. Gently push the backside of the Front Panel Control assembly until it is removed from the Front casting.
t. To remove the Front Panel Control board from the Front panel, perform the following subparts:
(1) Using a $1 / 16$ inch allen wrench, remove the CH 1 and CH 2 VOLTS/DIV control knobs, as well as the A and B SEC/DIV control knob.
(2) Pull straight out on the remaining five control knobs to remove them from their shafts.
(3) Turn the Front panel face down and remove the four mounting screws from the Front Panel Control board. Separate the Front panel from the board.

Reverse parts a through to assemble the Front panel assembly and install it on the instrument. Take care to align the GPIB Status indicators to their holes in the trim ring when installing that band.

## 5. Main Board and Gain-Cell Board Removal

a. Perform Step 1 to remove the cabinet from the instrument.
b. Perform parts a through $h$ of Step 4 to remove the Front Panel trim ring.
c. Pull the Front Panel assembly forward until it is clear of the Front casting and the face of the Front casting is accessible (it is not necessary to disconnect the cables connecting the assembly to the main instrument).
d. Remove the six screws securing the Main board to the Front casting. The screws are located on the face of the casting and are adjacent to the four BNC connectors.
e. Disconnect the two flex cable connectors at J104 and J108, and the ribbon cable connector at J105. J104, J 105 , and J 108 are located near the right-front corner of the board.
f. Disconnect the three ribbon cable connectors from J111, J113 (TV Trigger option only), and J141 at the left edge of the board.
g. Disconnect the cable connector from J107, located near the right-rear corner of the board, and from J106, located near center-front edge of the board.
h. Remove the screw securing the end of the Power switch's extension shaft to the Front casting.
i. Grasp the large extension shaft near where it joins to the small shaft of the power switch and pull it upwards from the Main board to disconnect it. Lift up and back (towards the rear of the instrument) to remove the extension shaft from the Front casting.

## NOTE

When installing the extension shaft to the Power switch, push the small shaft to put the switch in the IN position. Insert the shaft into the Front casting, align the extension shaft to the small shaft, and push the button end of the switch until the two shafts are coupled.
j. Using a $7 / 32$ inch nutdriver, rotate the seven black retaining latches $1 / 4$ turn counterclockwise to release them.
k. Disconnect the flex cable connector from J114 and the two retaining latches. J114 is located in left-rear corner of the board.
I. Remove the two mounting screws securing the Main board to Main chassis.
m . Lift the board up from the instrument and back from the Front casting to complete the board removal.
n. GAIN CELL BOARD REMOVAL: If one (or more) of the four Gain-Cell boards (mounted on right-rear corner of the Main board) is to be removed, turn the Main board over. Then desolder the 13 pins (two groups-one of five pins, the other of eight) that connect the Gain-Cell board to the main board, working from the bottom of the board. When the pins are free the board can be removed. To reinstall, remount and resolder.

Reverse parts a through $m$ to install the Main board.

## 6. Side Board Removal

a. Perform Step 1 to remove the cabinet from the instrument.
b. Set the instrument on a flat, smooth surface with the Side board facing up and the Front panel facing forward.
c. Disconnect the ribbon cable connectors from J111 and J 141 of the Main board.
d. Disconnect the ribbon cable connectors from J100 of the Timebase/Display board and J 103 of the Processor board. The two connectors are attached to the same ribbon cable.
e. Disconnect the ribbon cable connectors from J121 of the Timebase/Display board and J120 of the Processor board. The two connectors are attached to the same ribbon cable.
f. Disconnect the ribbon cable connector from J150 of the Side board.
g. Perform parts j through I of Step 4 to access the inside of the instrument.
h. Disconnect the ribbon cable connector from J102 at the right front corner of the Low Voltage Power Supply board and route the cable to the outside of the instrument.
i. Rotate the Top chassis back to the normal (installed) position. Using a 7/32 inch nutdriver, rotate the two retaining latches $1 / 4$ turn clockwise to temporarily secure it to the instrument.
j. Rotate the black retaining latch (near the front of the Side board) $1 / 4$ turn counterclockwise to unlock it.
k. Remove the mounting screw (center of the Side board) securing the Side board to the Main chassis.
I. Lift the front of the Side board up until it clears the retaining latch and then pull the board forward, until it clears the channel notch at its rear edge, to complete the removal.

Reverse parts a through I to install the Side board in the instrument. Take care to fit the rear edge of the board to the channel notch when reinstalling to the chassis.

## 7. High Voltage Power Supply Board Removal

a. Perform Step 1 to remove the cabinet from the instrument.
b. Set the instrument on a flat, smooth surface with the High Voltage Supply board facing up and the Front panel facing forward.

## WARNING

The CRT anode lead may retain a high-voltage charge after the instrument is powered off. To avoid electrical shock, ground the CRT anode lead to the metal chassis after disconnecting the plug. Reconnect and disconnect the anode-lead plug several times, grounding the anode lead to chassis ground each time it is disconnected to fully dissipate the charge.
c. Remove the anode lead from the retaining hook that secures it to the Main chassis.
d. Disconnect the CRT lead (male end) from the High Voltage Module lead.
e. Remove the single screw securing the High Voltage Power Supply and lift the High Voltage shield off.

## WARNING

The five mounting posts on the side of the High Voltage module (U565) may retain a high-voltage charge after the instrument is powered off. To avoid electrical shock, discharge these posts to the metal chassis through an appropriate shorting strap.
f. Discharge the five posts on the side of the High Voltage module to the metal chassis.
g. Disconnect the cable connectors from J172 and J173, located at the front edge of the board, and from J 162 and J 176 , located the rear edge of the board.
h. Disconnect the remaining ribbon connector from J105 on the Main board.
i. Pry outward on either one of two retaining latches securing the fan on its mounting posts. As the latch clears the edge of the fan, pull the fan outward and away from the instrument to remove. The latches are located at opposite corners; one at the bottom corner nearest the rear, the other at the top corner nearest the front, of the instrument.
J. Perform parts j through I of Step 4 to access the inside of the instrument.
k. Disconnect the crt connector from the back of the crt.
I. Rotate the two black retaining latches (near the front- and rear-left corners of the High Voltage Power Supply board) $1 / 4$ turn counterclockwise to uniock them.
m . While holding its nut (located between the crt shield and the adjacent Main chassis) stationary, remove the mounting post (near the center of the board) securing the High Voltage Power Supply board to the Main chassis.
$n$. Lift the left edge of the board up to clear the retaining latches. Pull the board to the left, until its right edge clears the two channel notches, to complete the removal.

Reverse parts a through $n$ to install the High Voltage Power Supply board. Take care to fit the left edge of the board to the channel notches when reinstalling the board.

## 8. Low Voltage Power Supply Assembly Removal

a. Perform Step 1 to remove the cabinet from the instrument.
b. Disconnect the ribbon cable connector at J 113 of the Main board to access the mounting screw at the center of the Side board. Remove that screw.
c. Remove the mounting screw at the center of the Side board. Note that for instruments with Option 05 installed, it is necessary to disconnect the ribbon cable connector at J113 of the Main board to access the mounting screw.
d. Disconnect the ribbon cable connector at J 148 of the Timebase/Display board.
e. Perform parts j through I of Step 4 to access the inside of the instrument.
f. Disconnect the ribbon cable connectors at J102 (right front corner of the Low Voltage Power Supply Supply board) and J166 (left front corner of the same board).
g. Disconnect the flex cable connector from J207 at the left front corner of the Processor board.
h. Remove the six screws and two extension posts securing the Low Voltage Power Supply cover (hereafter referred to as "the cover') to the Low Voltage Power Supply bracket.
i. Remove the screw securing the cover to the Center chassis.
j. Remove the two screws securing the cover to the Rear chassis. One screw is located immediately below the GPIB Connector, the other immediately below the PLOTTER X OUTPUT BNC.
k. Lift the cover off the Low Voltage Power Supply bracket to remove.
I. Disconnect the four cable connectors from P30, P60, P70, and P80 (located near the rear of the Low Voltage Power Supply board). Note the color coding of the cables to guide in reconnection of same.
m . Using a $7 / 32$ inch nutdriver, rotate the two black retaining latches (near the left and right front corners of the Low Voltage Power Supply board) $1 / 4$ turn counterclockwise to unlock them. Repeat for the two latches located near the middle of the right and left edges of the board.
n. Remove the mounting screw securing the Low Voltage Power Supply assembly to the Main chassis. The screw is located near the right-front corner of the board.
o. Carefully route the disconnected cables away from the top side of the Low Voltage Power Supply assembly.
p. Grasp the front of the Low Voltage Power Supply bracket and lift up until the Low Voltage Power Supply board is clear of the retaining latches unlocked in part m .
q. Pull the board towards the front of the instrument (until its rear edge clears the two channel notches) while lifting upwards to complete the removal of the assembly.

Reverse parts a through $q$ to assemble the Low Voltage Power Supply assembly and secure it to the instrument. Take care to fit the board to the channel notches when reinstalling the board.

## 9. Cathode Ray Tube Removal

## WARNING

Use care when handling a crt. Breakage of the crt may cause high-velocity scattering of glass fragments (implosion). Protective clothing and safety glasses (preferably a full-face shield) should be worn. Avoid striking the crt on any object which may cause it to crack or implode. When storing a crt, place it in a protective carton of set it face down on a smooth surface in a protected location. When stored face down, it should be placed on a soft, nonabrasive surface to prevent the ort face plate from being scratched.
a. Perform Step 1 to remove the cabinet from the instrument.
b. Perform parts c through i of Step 4 to remove the trim band from the instrument.
c. Remove the implosion shield from the crt faceplate.

## WARMING

The crt anode lead may retain a high-voltage charge after the instrument is powered off. To avoid electrical shock, ground the crt anode lead to the metal chassis after disconnecting the plug. Reconnect and disconnect the anode-load plug several times, grounding the anode lead to chassis ground each time it is disconnected to fully dissipate the charge.
d. Remove the anode lead from the retaining hook that secures it to the Main chassis.
e. Disconnect the crt anode lead (male end) from the high-voltage module lead. Discharge the crt anode lead by grounding its tip to the metal chassis.
f. Disconnect the cable from J172 at the right-front corner of the High Voltage Power Supply board.
g. Perform parts j through 1 of Step 4 to access the inside of the instrument.
h. Disconnect the crt connector from the back of the crt.
i. Disconnect the single cable from the crt (accessed through a hole in the top of the crt shield).
j. Disconnect the ribbon cable at J 148 of the Timebase/Display board.
k. Disconnect the flex cable at J 104 of the Main board.
I. Remove the eight screws (two at each corner) securing the crt frame to the Front casting.
m . Remove the crt frame from the Front casting. Guide the flex cable disconnected in part $k$ through its slot in the Front casting while removing the crt frame.
n. Grasp the face of the crt and pull it forward, while guiding the crt anode lead and the other cable (disconnected in part f) through their holes in the crt shield. It may be necessary to reposition the ribbon cable (disconnected in part j) as the removal of the crt is completed.

Reverse parts a through $n$ to install the crt. When installing the crt frame (removed in part m ) to the casting, refer to Figure 6-3 for the method of installation.

## 10. Menu Switch Removal

a. Perform Step 1 to remove the cabinet from the instrument.
b. Disconnect the flex cable at J104 of the Main board.
A. Install the four short screws at the locations indicated.
B. Insert the four long screws in the locations numbered 1 through 4.
C. Alternately tighten the screws, following the numbered sequence illustrated, until the face of the crt is just flush with the crt frame.
D. Using a torque screwdriver, alternately tighten the screws to 7 to 9 inch/pounds. Again, follow the numbered sequence illustrated.


Figure 6-3. Installation sequence for installing the crt frame screws.
c. Perform parts cthrough i of Step 4 to remove the trim band from the instrument.
d. Perform parts $k$ through $m$ of Step 9 to remove the crt frame from the instrument.
e. Carefully pull the adhesive-backed switch from the front of the crt frame.
f. Pull the switch through the hole in the crt frame to complete the removal.

Reverse parts a through e to install the Menu switch to the crt frame and the frame to the instrument. Use care to align the switch to the locating studs on the crt frame when pressing the switch back on the frame.

## 11. Scale Illumination Board Removal

a. Perform parts a through e of Step 10.
b. Disconnect the Scale Illumination board cable from $J 106$ (located near the front edge of the Main board).
c. Remove the Scale Illumination board and the attached light reflector while guiding the cable (disconnected in part b) through its hole in the Front casting.
d. Separate the Scale Illumination board from the light reflector to complete the disassembly.

Reverse parts a through d to install the Scale illuminatlon board to the instrument.

## 12. Attenuator Removal Procedure

a. Perform Step 1 to remove the cabinet from the instrument.
b. Perform parts b through s of Step 4 to access the inside of the instrument. Skip parts $n, p$, and $q$. When performing part r of Step 4, route the cable disconnected in part 0.
c. Insert the tip of a short screwdriver through the large slot in the front casting (above and right of the associated input BNC connector). Remove the screw securing the front of the Attenuator to the Main board.
d. Insert the tip of a screwdriver through the hole in the Low Voltage Power Supply board that is directly above the Attenuator to be removed. Remove the screw securing the rear of the Attenuator to the Main Board.
e. Rotate the Timebase/Display board to its mounting position and temporarily secure it by rotating the two black retaining lugs $1 / 2$ turn clockwise to lock them. The two retaining latches are located near the left-front and leftrear corners of the Timebase/Display board.
f. Remove the two screws securing the rear Attenuator shield to the heatsink. Remove the small shield.
g. Unsolder the two Attenuator output leads from the variable-capacitor lead and the resistor-capacitor pair lead exposed in part f.
$h$. Unplug the multipin connector from the Main board (at P147 for the CH 1 and P146 for the CH 2 Attenuator).
I. Remove the two screws (one is immediately lower left and the other upper right of the associated input BNC connector) securing the Attenuators to the front casting.
j. Remove the two screws securing the small bar to the bottom of the front casting.
k. Grasp the front end of the Attenuator assembly by its BNC connector and the rear end by the rear edge of the Attenuator shield.
I. Gently lift the Attenuator straight up from the Main board until the Attenuator pins clear their Main board plugs underneath the Attenuator assembly. Lift the rear of the Attenuator assembly up and towards the rear of the instrument until the Attenuator clears the braided shield cable mounted in the front casting.

Reverse parts $\mathbf{b}$ through I to reinstall the Attenuator. When performing part $b$, reverse parts $b$ through $s$ of Step 4 to reinstall the front panel and secure the Timebase/Display board and Front Panel assembly to the instrument.

## DIAGNOSTICS AND INTERNAL CALIBRATION ROUTINES

## INTRODUCTION

This subsection describes function and operation of the internal diagnostics and calibration routines. Where calibration routines make use of internal diagnostics, the interaction is explained. Status and other messages resulting from running the diagnostics or calibration routines are also detailed, and special conditions, such as the impact of power loss while certain diagnostic or calibration routines are running, are discussed.

In addition to the diagnostics and calibration routines, the Special Diagnostic menu and the features it accesses are also covered, including how they relate to the internal diagnostic routines. Information on how to run the diagnostics from the GPIB interface is included, followed by a table of Diagnostic/Troubleshooting procedures for this instrument.

## OVERVIEW

This instrument supports two types of internal diagnostic tests and calibration routines. Self Calibration (SELF CAL) and Extended Calibration (EXT CAL) calibrate the analog subsystems of the scope to meet specified performance requirements. Any detected faults in the control system and/or in the self-calibrating hardware result in a "FAIL" message that labels the failed calibration type (SELF or EXT). Both SELF and EXT CAL make use of some of the diagnostic routines that comprise the Extended Diagnostics.

Self Diagnostics (SELF DIAG) and Extended Diagnostics (EXT DIAG) are the two types of diagnostic routines used to detect and isolate system operation faults in this instrument. The tests are based on a multi-level scheme. First the highest system level, the kernel, is tested, and then lower-level subsystems are progressively tested. Each lower-level subsystem tested follows a higher-level system that tested good. When the SELF DIAG detect a system fault, they isolate the fault to one of the upperlevel subsystems immediately above the kernel. EXT DIAG can then be used to isolate the failure to lower-level subsystems and to test those subsystems, down to the lowest possible level.

In addition to the calibration and diagnostic routines just mentioned, there are the "Special" diagnostic features, useful for instrument troubleshooting, and Service Routines which are usually used with the Extended Diagnostics to isolate instrument failures.

## CALIBRATION ROUTINES

## SELF CAL

When the system runs the Self-Calibration routine, it generates test voltages to the Peak Detectors via the Cal Amplifier and DAC system. These voltage are used to set the gains, offsets and/or centering, and balance of the CCD Samplers, Peak Detectors, and Preamplifiers. The system uses iterative calculations to modify these voltages until converged solutions are reached; these converged solutions become the calibration constants stored in NVRAM (nonvolatile RAM) and are used to maintain calibration.

When SELF CAL is run, there is some interaction between the calibration routines for the different analog circuits calibrated, This interaction is minimized by using calibration constants obtained from the last SELF CAL run as starting values for calculating the new calibration constants when a new SELF CAL is run. If you are running a SELF CAL after a "COLD START" (see "SPECIAL Routines" in this section), the previous calibration constants are discarded; therefore, the SELF CAL tests are done twice to assure a converged solution. (The time required to perform the SELF CAL procedure from a COLD START is, therefore, obviously longer than the normal SELF CAL.)

SELF CAL can be run from the front panel using the EXTENDED FUNCTIONS menu or by the GPIB routines for automatically calibrating the internal analog systems. SELF CAL routines take about 10 seconds and calibrate most of the analog system. A SELF CAL may be performed by the user at any time (scope should be warmed up). Recommended times are when the ambient operating temperature changes by a significant amount since the last SELF CAL was run (see Level 7000-9000 Tests under "Diagnostic Test and Calibration Failures") and before a measurement is made which requires the highest possible level of accuracy.

## EXT CAL

Extended Calibration is an interactive procedure requiring a Calibration Generator that produces accurate dc voltages and a fast-rise pulse. The dc voltages are used to verify the internal 10-V Calibration Reference and to adjust the gain of the Vertical system Preamplifiers and the gain and offset of the Trigger circuitry. The fast-rise pulse is used to determine a calibration constant that nulls the delay between channels.

The ADJUSTS routines generate test waveforms or voltage levels to be used in setting the gains for the CCD output amplifiers and the vertical and horizontal gain and offset for the CRT drive signal. Additional adjustments optimize the CRT display, including edge focus, geometry, CRT bias, etc. Since no two CRTs are exactly alike, these tests must be user-interactive.

The REPETitive calibration sets the slope of two internal timing ramps in the feedback system that locates points of repetitively-acquired data. REPETitive calibration is a coarse adjustment and should only be run after a COLD START. During instrument operation, a continuous fine adjustment maintains the calibration.

Other manual adjustments are: the CCD clocks; the CH 1 and CH 2 input capacitance; the $100-\mathrm{MHz}$ bandwidth limit; the transient response; and (when the Video Option is installed) the $20-\mathrm{MHz}$ bandwidth limit.

Extended Calibration via the GPIB makes it possible to calibrate any individual subsystem listed in the 7000-9000 levels of the Extended Diagnostics menu. This list includes all the subsystems normally calibrated collectively during during SELF CAL, as well as those adjusted in the various EXT CAL procedures when they are accessed from the front panel.

## Calibration Operation

The steps and equipment needed to completely calibrate this instrument are found in Section 5, "Adjustments Procedure". Further information is found at the beginning of this section under "Instrument Calibration".

CAL/DIAG menu. All calibration routines are accessed by selecting CAL/DIAG from the EXTENDED FUNCTION menu (they can also be run via the GPIB). The EXTENDED FUNCTIONS menu is selected by the MENU/EXTENDED FUNCTIONS button when no other menus are displayed. Pressing the bezel button under the CAL/DIAG menu label produces the following menu display:

$$
\begin{array}{cccc}
\text { <status }> & \text { <status }> & \text { <status> } & \text { <warm-up-msg> } \\
\text { SELF } & \text { EXT } & \text { SELF } & \text { EXT } \\
\text { CAL } & \text { CAL } & \text { DIAG } & \text { DIAG }
\end{array}
$$

Pushing SELF CAL runs the previously described routine that calibrates this scope's analog subsystems. If the SELF CAL is successful, the PASS status is displayed above the SELF CAL button label in the CAL/DIAG menu. Failing SELF CAL causes the scope to enter the EXT DIAG menu (see Figure 6-5). If the CAL/DIAG menu is recalled, the FAIL status is displayed.

Pushing EXT CAL displays the EXT CAL menu:

$$
\begin{aligned}
& \text { <status }><\text { status }><\text { status }><\text { status }> \\
& \text { ATTEN TRIGGER REPET CTE } \\
& \text { CAL ADJUSTS }
\end{aligned}
$$

Selecting ATTEN produces yet another menu:


Pushing ATTEN GAIN, CHAN DLY, TRIGGER, REPET, CTE CAL, or ADJUSTS begins execution of the corresponding semi-automatic calibration routine. Completion of the ATTEN GAIN and TRIGGER calibrations requires the input of correct dc voltages, while the CHAN DLY and CTE calibration requires a fast-rise pulse.

EXT CAL routines can be aborted at any time by pressing the MENU OFF/EXTENDED FUNCTIONS button, but once a calibration routine (except ADJUSTS) has been started, it must be successfully completed or the status will be FAIL.

## NOTE

Extended Calibration is considered a service function; therefore, the EXT CAL menus are normally disabled to make them unusable by the scope operator. The cabinet must be removed and Jumper $J 156$ must be removed (diagram 13) to enable the menus. Disabling is done to prevent accidental loss of calibration by scope operators.

The <STATUS> message above the CAL labels indicates the results of the last test run for the calibration type above which it appears in the CAL/DIAG menu. When
a failure occurs, <STATUS $>$ is not immediately updated; rather, a new test must be run to determine current status:
a. During SELF CAL, some tests under levels 7000-9000 of the Extended Diagnostics are run. If any of these sublevel tests fails, the scope enters the EXT DIAG menu and indicates the level failed. Furthermore, the status label for SELF CAL in the CAL/DIAG menu is updated.
b. For internal component failures that would cause EXT CAL to fail, the status is updated when EXT CAL is run, either from the front panel or GPIB, or upon instrument power on.

For calibration, <status> can be:

UNCALD: Instrument has not been calibrated.
FAIL: $\quad$ Hardware errors were detected during calibration (calibration may not be valid).

PASS: The instrument was successfully calibrated.
<warm-up-msg>. The actual message displayed is the warning "NOT WARMED UP". This message is displayed for approximately ten minutes after power-on to warn that calibration of the instrument during this period is not recommended.

The "NOT WARMED UP" message is displayed after every power-on, even if the scope is turned off and then right back on. In this case, calibration may be performed one minute after completion of the power-on routine.

## NOTE

Running an EXT CAL for ATTEN and/or TRIG calibration without inputting the correct DC voltage levels causes the "FAIL" message to appear above the ATTEN and/or TRIG menu labels but does NOT change the ATTEN and/or TRIGGER calibration. See the LEVEL 7000-9000 test information under "Diagnostic Test and Calibration Failures" for the test levels that run when EXT CAL is executed.

## DIAGNOSTIC ROUTINES

The two main types of internal diagnostic routines are Self Diagnostics (SELF DIAG) and Extended Diagnostics
(EXT DIAG). Both types can be executed from scope menus. The Self Diagnostics, as well as those subtests below the 7000-9000 level that run when EXT CAL is executed, are a subset of the Extended Diagnostics.

## EXT DIAG

The Extended Diagnostics include all of the automatic test routines internal to the scope. Although the EXT DIAG are run when SELF DIAG runs, the individual tests can be performed at several levels from the EXT DIAG menu and its submenus (see "Operation" below).

EXT DIAG. The Extended Diagnostics are set up in a multi-level structure, the hierarchy of which is:

| 0000 | Top Level of the Extended <br> Diagnostics. When run, the Self <br> Diagnostics are done (see "Self <br> Diagnostics" in this section). |
| :--- | :--- |
| $1000-9000$ | Second level (first level under top <br> level). When any of these nine <br> levels run, all sublevel tests below <br> the running second level are <br> done. All eight of these second <br> level tests (and their sublevel <br> tests) run when level 0000 is <br> executed (executing level 0000 <br> runs the Self Diagnostics). |
| x100-x900 $\quad$Third Level, where $x$ is the most <br> significant digit of the second <br> level test the third level is under. <br> When run, any sublevel tests are <br> also run. |  |
| xy10-xy90 $\quad$Fourth Level, where $x$ indicates <br> the second level and $y$ the third <br> level test the fourth level is under. |  |

CAPABILITY OF EXT DIAG. The hierarchical structure just detailed allows selective testing and fault isolation/location of instrument subsystems from the highest to the lowest levels. The second levels are those subsystems immediately below the kernel and levels three and four are progressively lower subsystems of those sub-kernel systems. Status (FAIL, PASS, or blank for not tested) appears at the top and second levels in the EXT DIAG menu if Self-Diagnostics are run; lower levels must be selected and run to determine individual status of lower subsystems.

Any individual test selected can be made to loop to isolate signal path problems with external test and measurement equipment, once the area of failure has been determined by the automatic tests.

Any of the Extended Diagnostics tests may be accessed either individually or in selected groups using the EXT DIAG control menu. The tests use internal feedback and the digitizing capabilities of the instrument to minimize the need for applying external signals or for using external test equipment to troubleshoot. Testing of a failed area down to the lowest functional level possible (in some cases to the failed component) provides direction for further troubleshooting with service routines and/or conventional methods. Troubleshooting a failure may be based on assumptions made possible by running selected tests to verify good circuit blocks, thereby eliminating those blocks from consideration as a failed area.

SECOND LEVEL TEST DESCRIPTIONS. When the second-level (1000-9000) test is run, the following systems are tested:

Test $1000 \quad$ System ROM is checked to

Test 2000 Read/Write and Addressing tests are performed on registers.

Test 3000

Test 4000

Test $5000 \quad$ Waveform processor is checked.
Test 6000 Checksums of NVRAMS are

Test 7000-9000

Front panel processor is checked. done to validate the stored calibration constants and waveform data.
System RAM is checked for write-read capability to all addresses.

Calibrated analog circuits are tested to see if they will pass with the present calibration constants.

It is important to realize that, although status of the tests is indicated at the sublevels immediately below the kernel ( 1000,2000 , etc.), the tests are also run at any lower levels (3rd, 4th, etc.) in order to check out the indicated circuits. The only exceptions are as follows:

1. Levels 3700 and 3800 may only be executed from EXT DIAG and then only if internal jumper J 156 is removed.
2. CKSUM-NVRAM tests at level 6000 are only executed at power-on. When selected from EXT DIAG, only the flag status is changed.
3. The ATTENUATOR test at the 8700 level, the EXT TRIG OFFSET and GAIN tests (9114-17, 9124-27, 9213-16, 9223-26), and the REPET test (9300) are not run when Self Diagnostics are run. Neither are these tests run from the EXT DIAG menu. These tests are run when EXT CAL is run for ATTEN, TRIG, and/or REPET respectively.

## SELF DIAG

The Self-Diagnostic routine runs the 1000-9000 level tests from the Extended Diagnostics. As mentioned, these diagnostic routines test the function of all subsystems immediately below the kernel level (the kernel being the "highest" level) and the lower-level systems below each subsystem. The tests of subsystems immediately below the kernel are shown as levels $1000-9000$ when the EXT DIAG menu is displayed (see Figure 6-5). See the descriptions under "Second-Level Tests" for details on the circuits tested.

BINARY CODE FOR FAILED TESTS. In most cases, the EXT DIAG menu is the major tool in determining causes of internal failures. In the case of a failure that keeps the scope from displaying its EXT DIAG menu, the TRIGGER LEDs flash a binary code that indicates the FIRST test that failed:

As Self-Diagnostic tests run, the Trigger LEDs flash indicating that the self tests are being run. In a normal sequence with no failures, the tests run quickly, and the length of time that an LED is lighted is short. If a failure occurs, the Trigger LEDs flash a binary code of the FIRST failed test (see Figure 6-4 for the binary codes of the LEDs). This failure display is important, since it can be the only troubleshooting clue available if the scope cannot display the extended diagnostics menu.

For example, if test 2130 should fail, the following sequence of LED flashes occur to indicate the failed test number:

1. All the LEDs are lit at the start of Self Diagnostic routine to verify they can be turned on.


Figure 6-4. Trigger LED binary coding for diagnostic tests.
2. The LED's flash, indicating that tests are being run.
3. When the test failure occurs, all the Trigger LEDs are lighted and held on momentarily, indicating a failure has been found.
4. For the first number of the failed test, the READY LED turns on for a binary 2 (the failed test is in the 2000 level); all the LEDs are then turned on to delimit the first digit of the failed test from the second digit to follow.
5. The second number of the test number (one) is shown by turning on the TRIG'D LED for the binary code for 1 , then all the LEDs are again turned on as the code digit delimiter.
6. The third number of the failed test (three) is shown by turning on both the TRIG'D and the READY LEDs. Their binary values are summed $(1+2)$ to obtain the third number of the failed test (three), and all the LEDs are again lit to separate the digits.
7. The fourth and final number of the failed test is 0 , and all the LEDs light to identify the end of the failed test code.
8. After flashing out the coded number of the first failed test, the diagnostics continue on with the remaining tests, if they can be run. Any additional failures found will NOT be flashed on the Trigger LEDs.

If you miss the code the first time (as is usual unless you are expecting a failure), Self Diagnostics must be run
again. If a failure prevents display of the EXT DIAG menu, you must turn off the scope and turn it back on again to rerun the tests. It takes a little practice to read the failure codes from the LEDs.

If it can, the scope displays the Extended Diagnostics menu if a failure is found (or if the Self Diagnostics were run from that menu). The display of test selections in the Extended Diagnostics menu is a hierarchically structured set of tests in lists containing the test numbers, test names, and last status of the test results. If the test has not been run since the last COLD START, no status will be displayed. If an upper level test in the set (such as REG) is run, all tests in the REG test hierarchy will be done and labeled with a PASS or FAIL status. Menu operation is covered in "Diagnostics Operation".

## Diagnostics Operation

Diagnostics are runnable from the front-panel or via the GPIB. The Self-Diagnostics are also executed when the instrument is powered up. For both the Self and Extended Diagnostics, front-panel access is from the same CAL/DIAG menu used to access the calibration features:

$$
\begin{array}{cccc}
\text { <status> } & \text { <status> } & \text { <status> } & \text { <warm-up> } \\
\text { SELF } & \text { EXT } & \text { SELF } & \text { EXT } \\
\text { CAL } & \text { CAL } & \text { DIAG } & \text { DIAG }
\end{array}
$$

Pushing SELF DIAG or powering up the scope causes the Self Diagnostics to run. These routines take about 30 seconds. First the TRIGGER status LED's flash as previously described. Then, if all tests are passed, the scope displays the main EXT DIAG menu if SELF DIAG was run from that menu, or returns to scope mode at power-down if SELF DIAG was run due to power-on. If passed when run from the CAL/DIAG menu, the scope returns to that menu and indicates the PASS status above the SELF DIAG button label. Failure of a test always returns the EXT DIAG menu regardless of what caused the SELF DIAG to run. The EXT DIAG menu is exited by pressing the MENU OFF/EXTENDED FUNCTIONS frontpanel button.

DIAGNOSTIC MENUS. Since the diagnostics routines are layered into a multi-level, hierarchical structure, the diagnostic menus are also layered this way. In each menu, there is one higher level test displayed, along with several equal sublevels. The menus are used to either run the higher (top) level test or to select a menu for one of the sublevels displayed. The select sublevel test can then be run as the top level of the submenu selected. Examination of the EXT DIAG menu should illustrate the structure:

## Maintenance-2440 Service

Pushing EXT DIAG displays the main Extend Diagnostics menu (see Figure 6-5). In this menu, the top level test is listed as "EXTENDED DIAGNOSTICS" and its level number is " 0000 ". The status at the time the test was last run is also indicated on the display line. All the other tests listed are one level below this level (1000-9000) and are indented to indicate their subordinance. The bottom three lines appear in this main menu and all submenus for use in selecting and running tests.

UP/DOWN ARROWS. The up-arrow and down-arrow buttons move an underscore pointer through the displayed list of diagnostic tests. Moving the pointer to a diagnostic below the top-level test line and then pressing the RUN/SEL button selects a submenu of tests available at the next level down with that diagnostic. Moving the pointer up above the top-level test line returns to the next level of hierarchy in the menu (if not in the main diagnostic menu; at the top-test 0000)-of the main menu, pressing the up-arrow button returns the CAL/DIAG menu).

A press of RUN/SEL with the pointer at the top line (top level) causes all the tests at and below that diagnostic level to be run. An individual test can be selected by using the arrow keys to move the pointer to the desired test, then pressing the RUN/SEL button twice (once to select it, and once to run it). The cumulative result of any test run will be displayed on test completion at the right of the title line. This will be either PASS, FAIL, or blank if an attempt was made to run a non-automatic test.


Figure 6-5. Main EXT DIAG Menu.

## NOTE

A diagnostics name in the Extended Diagnostics menu followed by an asterisk is not testable. The asterisk indicates either that the test is run only during an EXT CAL or run at power-on SELF DIAG only. The PASS/FAIL status is the result of the last EXT CAL or the last power-on check. A FAIL label on an asterisked test is accompanied by the "RUN SELF CAL THEN RUN EXT CAL" diagnostic message above the bezel button labels. An UNCALD label also appears above the uncalibrated selection of the EXT CAL selection in the CAL DIAG menu.

MODE. The MODE button rolls through four mode choices for running the selected test. The choices are RUN ONCE, RUN CONTINUOUS, RUN UNTIL FAIL, and RUN UNTIL PASS. If RUN CONTINUOUS is chosen before starting the selected test, it will be continually executed until the HALT button is pressed.

## NOTE

If one of the continuous MODEs is chosen, pressing the HALT button will stop the test as soon as it completes AS LONG AS THE HALT LABEL IS SOLIDLY DISPLAYED above the button. If level 4000 is run, the display will be flashing and the HALT button is ignored (instrument must be powered down, and then up, to stop execution).

RUN UNTIL PASS and RUN UNTIL FAIL modes may also be stopped using the HALT button. In addition, all tests (except a looping Front-Panel $\mu \mathrm{P}$ test) can be aborted with the MENU OFF/EXTENDED FUNCTIONS button. If an asterisked test (not presently testable) is selected, the mode switches to RUN ONCE and RUN ONCE, and the test does not run.

HALT_Pressing HALT causes all diagnostic test activity to stop at the finish of the current test in progress. It is especially used to halt a test running in a continuous mode.

Remember that, when using any Extended Diagnostic menus, the top (default) level test in the menu is the only one that can be run from the menu displayed. For example, moving the pointer to underline " 3000 SYS RAM" in the main menu and pressing RUN/SEL selects (displays) the System RAM submenu with 3000 SYS RAM underlined and at the top level. Pressing RUN/SEL runs the 3000 level test. Moving to, say, "3500 A11U440" (a sub-
level in the displayed menu) and pressing RUN/SEL selects another lower-level submenu where the 3500 level test is the top level. This process can be continued until the lowest levels are reached.

STATUS. The status for the test at the time the last test is run appears next to the test names. For diagnostics <status> can be:

| (blank) | test has not been executed. |
| :--- | :--- |
| FAIL | test failed on last attempt. |
| PASS | test passed on last attempt. |

The <status> appearing on the test lines requires some interpretation. If <status> is for the top-level test (see above) for ANY EXT DIAG menu, PASS means ALL the sublevel tests THAT RUN when the top level is run passed; FAIL means at least ONE of the sublevel tests THAT RUN failed. If the operator has entered an EXT DIAG menu and not yet run the top level test, the status is blank.

For any sublevel test displayed below the top level in a menu, STATUS is FAIL if any test in the submenus below that test was failed the last time it was run, whether or not it normally runs when the test in question runs (it is PASS if all are passed). In the case of a failed EXT CAL test, the upper-level tests which the failed test ran under will have FAIL status in the menus in which they appear as sublevel tests.

To illustrate the difference in interpretation just described, if the ATTENUATOR test, level 8700 , failed at the last time the EXT CAL was run, SELF DIAG (level 0000) will pass if run because SELF and EXT DIAG do not run EXT CAL tests. However, level 8000 in the EXT DIAG menu will have FAIL status, since one of the submenus under level 8000 has FAIL status. If level 8000 is underlined and RUN/SEL used to select and then run the level 8000 test, it will pass, again because the 8700 EXT CAL test is not run.

To summarize, the top level status applies to all the tests that run under it, if the top level is run, or is blank if not run. Status on a sublevel test in menus applies to all tests in the submenus that fall under that sublevel test in the menu hierarchy, whether actually accessing and running the sublevel test would run those tests or not.

## NOTE

The status for sublevel tests in the EXT DIAG menus can also be blank. Blank status indicates that the results of the tests below the sublevels is unknown, such as when a COLD START has been performed.

## Diagnostic Test and Calibration Failures

Failures of the diagnostic tests run as a result of executing Extended or Self Diagnostics, as well as those run due to performance of SELF or EXT CAL, are now discussed. Some tests are run only under special circumstances (such as only as the result of running an Extended Calibration or when an internal jumper is removed). The circumstances are described as the individual levels are discussed.

LEVELS 1000-5000. Tests in the 1000-5000 levels are hardware tests that run when Self Diagnostics or Extended Diagnostics are run. If the instrument fails a 1000-5000 level test, the instrument displays the message "HARDWARE PROBLEM-SEE SERVICE MANUAL" in the Extended Diagnostics menu. The second level test that failed will be indicated by the FAIL status on the test line. This message remains displayed until POWER-ON Self Diagnostics pass. Running and passing the failed test, either from the Extended Diagnostic menu or via running Self-Diagnostics from the CAL/DIAG menu, does not remove the message. Hardware failures should be referred to qualified service personnel.

Test levels 3700 and 3800 test the RAM devices that store the internal calibration constants. Loss of power while these tests run can result in the loss of these constants. To prevent such loss, this instrument will only run those tests if an internal jumper, J156 (see Diagram 18), is removed before the tests are run. Run these tests only if necessary; this would normally be if a 6000 NVRAM failure has occurred and testing of device functionality is desired. In the event calibration constants are lost, SELF CAL and any calibrations labeled "FAIL" or "UNCAL" must be performed.

LEVEL 6000 Tests. The LEVEL 6000 diagnostics test the calibration constants, last front-panel setup, waveform, and Sequencer data stored in NVRAM. These tests are only run as Self Diagnostics at power on. Failure of a 6000 subset diagnostic test indicates a checksum failure of the stored data in the nonvolatile RAM. If test 6100 fails, tests 6200, 6300, and 6400 in the subset are not done.

The causes of a failure in the 6100-6300 bracket may be non-fatal to continued instrument operation, and normal (or near-normal) operation may be recovered by the user (also see "COLD START" under "SPECIAL Diagnostics" in this section):
a. LEVEL 6100. If the calibration constants are lost, this test will fail and the instrument will do a "Cold Start". The Extended Diagnostic menu will be entered and the message "RUN SELF CAL THEN RUN EXT CAL" will be displayed in that menu. Service personnel should perform the self calibration routine, plus the ATTEN, TRIGGER, and REPET Extended Calibrations. Unexplained loss of calibration constants indicates need for corrective maintenance.
b. LEVEL 6200. Loss of the stored power-off frontpanel settings (failure of FP-LAST test 6200) causes the scope to do an INIT PANEL on power-up (see Table 6-7 for the INIT settings). Recovery of normal operation is done by pressing MENU OFF/EXTENDED FUNCTIONS to exit EXTENDED DIAGNOSTICS and resetting the frontpanel controls to the required settings for the measurement to be made. The "FAIL" condition for test $\mathbf{6 2 0 0}$ will be reset to PASS and the scope will not enter EXTENDED DIAGNOSTICS on the next power-up if permanent failure of the memory has not occurred.
c. LEVEL 6300-6400. Checksum failures of these levels indicate that waveform data and/or scaling information, or front-panel setups stored as sequences, are invalid. This may have occurred due to a memory failure or battery backup failure, or due to loss of power during the time the information was stored. Scope may be usable; recovery of operation is as for level 6200, above. The "FAIL" condition for test 6200 will be reset to PASS and the scope will not enter EXTENDED DIAGNOSTICS on the next power-up if permanent failure of the memory has not occurred.

LEVEL 7000-9000 Tests. Test failures at this level can be due to hardware or other causes:
a. A FAIL status (or PASS, for that matter) of the ATTENUATOR test ( 8700 level), the EXT TRIG OFFSET(9114-17 and 9124-27 levels) and/or GAIN tests (9213-16 and 9223-26 levels), and/or the REPET test ( 9300 level) are the result of the test(s) run at the time an Extended Calibration of the affected area(s) was last performed. These tests are not run when Self Diagnostics are run and are followed by an asterisk "*" after their test name to indicate this. (Neither can these tests be run from the EXT DIAG menu; however, since the FAIL status at the second level (8000 and/or 9000) might or might not be
the result of the sublevel Extended Calibration test, the EXT DIAG can be used to determine if it was an EXT CAL test that failed.)


#### Abstract

Although these tests are not run at the Self-Diagnostic level, a failed status will result in the instrument displaying the Extended Diagnostics menu when the Self Diagnostics are run at power-on (Self-Diagnostics can PASS, however, since these tests are NOT actually run). The message "RUN SELF CAL THEN RUN EXT CAL" will be displayed in the menu. The message can only be removed by running the Extended Calibration for the failed test (either ATTEN, TRIG, or REPET). Extended Calibration is a service function and should be referred to qualified service personnel.


## NOTE

In the case of an invalid standard voltage being applied during the ATTEN or TRIG Extended Calibrations, this instrument does not change its calibration and its accuracy is unchanged. The previously described conditions for a failed extended calibration are exhibited, however, and a valid Extended Calibration is required to remove the message from the Extended Calibration menu.
b. The remaining tests that run below the 7000-9000 level are executed when either a SELF CAL is performed or Self or Extended Diagnostics are run. (When run due to a SELF CAL, the system flags these appropriate tests as failed if a converging solution cannot be found; when run due to performing Self or Extended diagnostics, the system widens the limit values stored as calibration constants and tests if converging solutions could be found and a SELF CAL passed if it was run.) Failure of these tests causes the second level status to fail for the affected area and, if Self Diagnostics was run because of power on, the EXT DIAG menu is displayed indicating the failed status. The Extended Diagnostics can then be used to determine if the failed test is SELF CAL or EXT CAL related.

If the failure is not an EXT CAL related test(s), a hardware failure can still not be assumed unless SELF CAL is performed and a failure occurs in the same test or tests. Failure may only indicate that calibration is inaccurate for the current ambient temperature. This is because the tests are run somewhat differently when they are run as a result of running Self or Extended Diagnostics than when they are run as a result of running a SELF CAL, as was just mentioned.

When SELF CAL runs, the old values are modified and new values are calculated for the calibration constants;
these new values are stored and then used to run the tests. One of the criteria for modifying these constants is ambient temperature.

When the tests are run due to SELF or EXT DIAGNOSTICS, the old values are NOT modified. If the ambient temperature has changed sufficiently to affect calibration, the tests run may not be able to converge to the correct limits (even though they are wider than those of SELF CAL). This indicates that a SELF CAL should be done to move the calibration constant values to the new "in-calibration" limits to compensate for the present instrument conditions, whereupon the SELF DIAG test should pass. Failure to pass the SELF CAL procedure as outlined in Section 5 of this manual indicates a probable hardware failure and this instrument should be referred to qualified service personnel.

## NOTE

If power is lost while SELF CAL is running, the calibration constants are invalidated. Normally, invalidating the constants causes the instrument to do a Cold Start to replace the invalidated constants with nominal values. If power interruption during SELF CAL causes the invalidation, however, the scope locks itself into the EXT DIAG menus and can only be exited by pressing the "up arrow" button. Pressing this button locks the scope into the CAL/DIAG menu, where the user must execute a SELF CAL before the menu can be exited. Running the SELF CAL validates and preserves the calibration constants.

## Special Diagnostics

The Special Diagnostic Features menu is accessed by pressing the menu button labeled SPECIAL in the EXTENDED FUNCTIONS. The features in this menu are normally disabled to prevent operators (non-service personnel) from operating them, and, if the SPECIAL menu button is pressed, the message "DISABLED-SEE MANUAL" is displayed. If J156 (located on the A13 board and shown in diagram 13) is removed, "WARNING: SERVICE ONLY-SEE MANUAL" is displayed in the SPECIAL menu and the menu is enabled to allow the features to be used for servicing the scope.

COLD START. COLD START eliminates all the previous calibration constants and restores them to known nominal values. A COLD START is especially useful for removing scrambled data from the NVRAM and is needed to permit a valid SELF CAL (and subsequent testing) to be performed if the data scrambled is the instrument's
calibration constants. After a COLD START, a SELF CAL and the ATTENuator, TRIGGER, and REPET EXT CAL must be performed to return the instrument to its previous state.

A COLD START can be initiated in three ways. One, $\$ 156$ can be removed and the SPECIAL Diagnostics menu can be used to COLD START the scope as an aid in servicing it. Second, a COLD START is done upon power-up if the Lithium battery that backs up the System NVRAM is changed or fails, or if the NVRAM is relaced. Third, if the internal calibration constants are corrupted, the instrument fails test level 6100 and, the next time it's powered up and the Self Diagnostics are run, a COLD START is performed. (The only exception is when the instrument detects that an interruption of power during SELF CAL caused the constants to become corrupted-see NOTE under LEVEL 7000-9000 Tests failures earlier in this subsection.) The latter two COLD STARTS described here can occur whether J156 is installed or removed.

After a COLD START, the instrument displays the EXT DIAG menu, where the test level numbers, test names, and last status of the test results is displayed. If the test has not been run since the last "COLD START," no status will be displayed, If an upper level test in the set (such as REG) is run, all tests in the REG test hierarchy will be done and labeled with a PASS or FAIL status. Menu operation is covered in "Diagnostics Operation".

FORCE DAC. Pressing this menu button accesses a menu that lets service personnel vary selected adjustment constants to aid in troubleshooting certain internal circuits. It is especially useful for facilitating troubleshooting of the digital-to-analog converter circuitry and all the output sample-and-hold circuits of the DAC System. The routines in Table 6-6 indicate how this feature is used.

CAL PATH ONiOFF. When ON, the calibration signal path to the Peak Detectors is closed. If large offset errors have driven the display off-screen, switching CAL PATH ON eliminates the Attenuators and Preamplifiers from the input signal path and places the calibration reference level on the display. If that brings the display back on screen, the offset problem may be isolated to the Attenuators or Preamplifiers; if not, then the problem may be in the Peak Detectors or CCDs.

## Service Routines

The Service Routines are menu, GPIB interface, or jumper initiated routines for exercising the hardware, usually in a looping mode, that allow a service person to
troubleshoot an internal fault using external testing and measuring equipment. Where possible, the Extended Diagnostics routines are used for looping to allow access to them from both the front-panel EXTENDED FUNCTIONS menu and the GPIB interface.

Jumper-initiated tests include Kernel Mode for the System $\mu \mathrm{P}$ and the Waveform $\mu \mathrm{P}$, Waveform $\mu \mathrm{P}$ Bus Control Mode, Bus Isolate Mode, System $\mu \mathrm{P}$ Chip Select test, Resets for the System $\mu \mathrm{P}$ and the Waveform $\mu \mathrm{P}$, a Front Panel $\mu \mathrm{P}$ internal diagnostics test, and a Front Panel Multiplexer test. A description of these tests and how they are used is included in Table 6-6, Extended Diagnostics.

Troubleshooting routines (written by a system programmer) that systematically exercise specific firmware or hardware functions can be implemented via the GPIB interface. This type of external testing provides a tool for troubleshooting the scope that may be changed as needed by controller programming.

Use of the Service Routines provide service personnel with signals and procedures that enable fault isolation and restoration of an instrument to a functional level that is supported by the Extended Diagnostics and/or other routines.

## DIAGNOSTICS OPERATION VIA THE GPIB INTERFACE

Operation of the GPIB interface is described in the Programmers Reference Guide supplied with this instrument. This additional information describes use of the diagnostic commands. Operation of any of the four Cal/Diagnostic modes is selected by using the keywords SELFCal, EXTCal, SELFDiag, or EXTDiag as arguments with the TESTType command via a GPIB controller. The selected TESTType will start when the EXEcute command is received. See Appendix A of the Programmers Reference Guide for the definition of the GPIB calibration and diagnostics commands.

## SELF CAL

If TESTType SELFCal is selected, the Self Calibration portion of the test sequence will run in its entirety when the EXEcute command is received. A service request (SRQ) will be issued when the sequence is finished if the OPC mask is on. The status byte received by the controller will indicate if the test completed either with error or with no error. See the Programmers Reference Guide for a list of the status bytes.

If an error occurs during SELFCal, it is reported to the controller when the ERRor? query is issued to the instrument. ERRor? returns a string of error numbers (up to nine) resulting from the last EXEcute command. These numbers will be the highest order in the hierarchy of the SELF CAL routine; so, to locate the exact test that failed in the tree, the TESTNum must be set to a lower level and the ERRor? query reissued until the lowest detection level of the failure is reached. The ERRor? query returns 0 if no errors have occurred. This method of failure location is used for errors generated by any of the calibration or diagnostics sequences.

## EXT CAL

The EXTCAL TESTtype allows specifying the calibration sequence (TESTNum) to be performed. The calibration routine specified may be any steps or sub-steps of the EXT CAL or SELF CAL routines. The user is responsible for assuring that any externally required test equipment has been connected and programmed and that pauses in the procedure to make manual adjustments or equipment changes are terminated via a menu button push or a GPIB STEp command to advance to the next step in the sequence. The external calibration sequence numbers to be used as the numerical argument for TESTNum are listed in Table 6-6 under the "Test Number" column heading. The valid test numbers for Calibration are 7000 to 9300 in the table. Error handling is the same as in SELFCal.

## SELF DIAG

Invoking the TESTType SELFDiag causes execution of the entire self-diagnostic sequence when an EXEcute command is received. Error handling is the same as in SELFCal.

When Self Diagnostics is called via the GPIB, completion and/or failure will cause an SRQ to be issued by the instrument. The status bytes returned on a poll indicate a successful completion or failure of the Self Diagnostics sequence. Errors can then be queried via the GPIB and traced to the lowest level of the Extended Diagnostics in the same manner as from the front panel. Failure of Self Diagnostics when run from the GPIB does not put the instrument into the Extended Diagnostics menu as it does when run from the front panel.

## EXT DIAG

TESTType EXTDiag allows a specific TESTNum to be selected for execution upon receiving an EXEcute command. Error handling and reporting is the same as in SELFCal. Looping a test is done by issuing the LOOp command prior to the EXEcute command, and the HALt command stops the looping test.

## DIAGNOSTIC PROCEDURES

The various tests resident in the scope are organized into a tree structure with a test number designating each node. The root node is 0000 . A summary of the way in which the tests are performed and the type of test made follows the test number and test name in Table 6-6.

## NOTE

FAIL and PASS flags in the Extended Diagnostics menu show the results of the last test run. If a defective device that has previously caused a FAIL flag to be set is replaced, the test must be run again to obtain a PASS indication in the menu.

These troubleshooting procedures are broken down into several types. The Troubleshooting Procedures of Table $6-6$ provides a description of the tests made, and in many cases, the troubleshooting procedure used in case of a test failure. Other areas of the scope require more extensive troubleshooting trees. These areas are: the Low Voltage Power Supply, the Video Option, the Display System, and the Time Base and System Clocks. Troubleshooting trees are located in the "Diagrams" section of this manual. Some of the troubleshooting procedures are very general in that they don't lead the troubleshooter directly to a specific faulty component or components. In those cases, it is up to the troubleshooter to analyze the information obtained from the tests made to determine the actual fault. Figure $6-6$ is a flow chart that shows the initial troubleshooting steps as an aid in determining where to start.


Figure 6-6. Initial troubleshooting chart.

Table 6-6
2440 Troubleshooting Procedures

## INITIAL INDICATIONS

## TESTS FOR

LIFE

1. Are TRIGGER LEDs flashing? If all lights are flashing, suspect Waveform $\mu \mathrm{P}$ ROM U480 or U490 (diagram 2) or their selects.
2. Is there activity from GPIB LEDs during turn-on? If the three LEDs above the crt (LOCK, SRQ, and ADDR) all light then go through a binary counting pattern (test number 2170), the diagnostics are working, and the instrument is alive. Go to Procedure 2.
3. After 30 seconds of turn-on, press MENU OFF and cycle the SLOPE switch. If the + and Slope LEDs light alternately, the System $\mu \mathrm{P}$ is alive, and the operating system is active. Go to Procedure 2.
4. Did the attenuator relays click? If the relays clicked, the power-on seff tests -jere running.
5. If any of the signs-of-life occurred, then assume that there is some "life in the box" and go to Procedure 2; otherwise, go to Procedure 8.
6. If the menus are normal (can focus, adjust intensity, etc.), then go to Procedure 3.
7. If there are no displays then go to Procedure 5.
8. If there is a display, but the display is incorrect (no intensity control, out of focus, etc.), a dot only, a vertical or horizontal streak, then it is an analog problem. Go to Procedure 6.
9. If portions of the readout are missing or wrapped over, but the power-on test runs, the front-panel controls and the EXT DIAG menus may still be useful. Attempt to use the diagnostics to determine the failed tests. Also, read the binary code of the first failed test that is flashed by the Trigger LEDS during the power-on sequence. Use that information as a starting point for troubleshooting, using the steps indicated for the failed test in Procedure 7, "EXTENDED DIAGNOSTICS". The most probable cause of a failure of this type is a bus problem or bad IC on a bus causing a stuck bit in Display circuitry of the Time Base/Display board (schematic diagrams 16 and 17). The busses to suspect are the ones connected to the IC indicated by the failed test.

## POWER-ON DIAGNOSTICS

NOTE: THIS IS NOT SELECTABLE, IT EXECUTES AT POWER-ON.

1. If all the power-on tests pass, go to Procedure 4. If not, then go to Procedure 7.

## 4

OPERATIONAL PROBLEMS (Not detectable by diagnostics)

Phase Clock Array Outputs A10U470 (schematic diagram 11)

1. Check A10U470 (Phase Clock Array) at pins 11, 12, 13, 14 and 15 for output clocks.
2. If no outputs, the problem is probably $U 470$ or the input circuit to $U 470$ at pins 65 and 67 ; i.e., CR580 or C582.
3. If the Phase Clock Array is working, the problem is in the Time Base.

Table 6-6 (cont)

TIMING ERROR
AT $50 \mu \mathrm{~s} / \mathrm{div}$ AND FASTER

Phase-Locked Loop Circuit (schematic diagram 11).

1. Check the $10-\mathrm{MHz}$ input to U381 pin 6. If there is no $10-\mathrm{MHz}$ clock at TP174 then go to the Timebase troubleshooting chart (located in the "Diagrams" section) and troubleshoot the System Clocks.

## NOTE

Use 2440 CURSOR function of 1/TIME to measure the frequency. The cursor position difference will read out directly in frequency.
2. Check U381 pin 9 for 10 MHz .

Frequency too low at pin 9:
a. Check that U381 pin 3 has negative pulses and that the voltage at U381 pin 12 is positive with respect to U381 pin 3. The VCO CTL voltage at TP581 can be as high as +12 V .

Frequency too high at pin 9:
b. Check that U381 pin 12 is ramping negative with respect to U381 pin 3 (average not absolute) and TP581 can be as negative as -0.6 V .
c. If these conditions are not true, the problem is probably Phase/Frequency Detector U381 or amplifier U580.

MISSING DATA

## POINTS

IN REPET

Jitter Correction Troubleshooting (schematic diagrams 12 and 13):
On the scope under test, select REPET acquisition mode, AUTO LEVEL, VERT trigger, DC Trigger COUPLING, and set the SEC/DIV setting to 5 ns . Then select ACQUIRE and connect a probe from the CH 1 input to TP291 (TTLB1) (found above A10U450, the CH 1 CCD , on the main board).

If there are bands of missing data points every two divisions, or only a few data points are placed every two divisions or the waveforms are distorted, the problem may be in the Jitter Correction circuitry.

The Jitter Correction circuit has both analog and digital circuits. First check the digital portion to insure that it is working. If that is ok, then assume that the problem is in the analog portion of the Jitter Correction circuit.

## DIGITAL SECTION TROUBLESHOOTING

1. Check that START1 and START2 are present at U841 pin 2 and U842 pin 2 (located on the Side board and shown on diagram 13) respectively and that they are coincident.
a. Test the collector of Q492 and Q391 (located on the Main board and shown on diagram 12) for the START pulses.
If missing:
b. Check for SRAMP1 and SRAMP1 at the bases of Q492 and Q491.
c. Check for SRAMP2 and SRAMP2 at the bases of Q391 and U390.
d. Check for RAMP and $\overline{\text { RAMP }}$ at the bases of Q392 and Q490.

If any gating signals are absent, backtrack to U470 and/or U370 (on diagram 11) and locate the defective component.

Table 6-6 (cont)
2. Check that STOP1 and STOP2 are present at U841 pin 12 and U842 pin 12 (on the Side board). These signals are not coincident and should be jittering with respect to one another. If missing, backtrack to U490 and/or U390 (located on the Main board and shown on diagram 12) to locate the defective component.
3. While triggering on the START1 pulse, check for gated signal (by STOP1) at U852 pin 1 on the Side board. Check at U853 pin 1 for gated signal while triggering on the START2 pulse. If either gated signal is missing, check the gating components to locate the problem.
4. While triggering on the START1 pulse, check for activity (fast to slow) at the Jitter Counter (U844 and U852) outputs (pins 14, 13, 11 and 12 on U844; pins 3, 4, 5, 6, 11, 10, 9, and 8 on U852). Observe that each output pin on the ICs should be switching slower than the preceding one as the counters count down. Replace the counter if found defective.
5. Check that the inputs to U750 and U752 are gated to the outputs of U752. The only time they are the same is if both pin 1 and 19 are low. If a WORD trigger probe is not available, the following setup may be used making use of the A and B Trigger Mode to obtain coincident triggering.

## HORIZONTAL

| A and B SEC/DIV | 200 ns |
| :--- | :--- |
| MODE | B |

## VERTICAL

MODE
COUPLING
VOLTS/DIV
POSITION

TRIGGER
A TRIGGER SOURCE
A LEVEL
SLOPE
MODE
B TRIGGER SOURCE
MODE

CH 1 and CH 2
DC
2 V
Traces to graticule center

Now connect the EXT1 to U750 and U752 pin 1 and EXT2 to U750 and U752 pin 19. The inputoutput pairs may now be checked, and they should compare at the " T " of the trigger point.

## ANALOG SECTION TROUBLESHOOTING

1. Connect a probe from CH 1 of the scope under test to the TTLB1 test point on its main board. Select REPET, set the scope under test to $2 \mathrm{~ns} / \mathrm{div}$ and obtain a stable trigger.
2. Set the test scope to $500 \mu \mathrm{~s} / \mathrm{div}$.

With the test scope:
3. Make sure that the signal at the collector of Q491 and Q390 stabilizes at about 800 mV . This is the baseline stabilization circuit. The waveforms shown next to the schematic diagrams are useful to make waveform comparisons.
4. Check for a fast ramp that corresponds to RAMP and $\overline{\text { RAMP }}$ from U370. This ramp should rise from the stabilization level to a maximum and start down at the same time that the START1 (or START2) pulse steps high, and that the STOP1 (or STOP2) pulse steps high when the descending ramp crosses 0 V . If not, troubleshoot the circuitry to determine the problem. These ramps should be linear both in rise and fall times.


#### Abstract

GPIB GPIB Test for Activity (schematic diagram 20): 1. Press the OUTPUT menu button, then SETUP, then MODE. Select L/ONLY and see if the ADDR LED is on. Select T/L and see if the ADDR LED is off. Select T/ONLY and see if the ADDR again is on. 2. If the LEDs follow the above, GPIB IC U630 is at least responding to the System $\mu \mathrm{P}$, and the problem is probably in GPIB Bus Buffers U720 or U624. 3. If the LEDs do not follow the above pattern, troubleshoot bidirectional buffer U532 or U630 (assuming the LEDs do the 0 through 7 binary count during REG test section of EXT DIAG).


FRONT PANEL PROBLEMS

Front Panel and Auxiliary Front Panel (schematic diagrams 4 and 6):
If there is a front panel problem and the Extended Diagnostics have not detected anything, the problem is not in the Front Panel Processor or its handshake logic with the System $\mu$ P.

On the Front Panel $\mu \mathrm{P}$ (U700), do the following checks:
NOTE
When probing around the Front Panel $\mu P$ circuitry, it is possible to cause bad data to be written to the System $\mu P$ and/or the Front Panel $\mu P$ by inadvertent grounding of pins or accidental shorting of pins together. If this should occur, many trouble symptoms may be present. To cure these symptoms, turn off the scope and turn it on again. This rewrites all RAM space in the System and Front Panel microprocessors with correct operating data.

1. Check pins 26, 27, 28, 29, 30, and 15 for active output signal switching. These signals are all asynchronous, so a stable display pattern is not possible (without going to SAVE mode on the test scope).
2. If the signals checked in Step 1 are active, go to Step 3. If these signals are not actively switching, perform the Front Panel MUXTEST to check that the $\mu$ P drives the MUXSEL signal lines in a tight looping routine. In the MUXTEST, only the MUXSEL signal output lines are being driven. No output will be seen on the $\mathbf{S} \pi$ or SHCLK lines (pins 29 and 30 respectively).
3. Check pin 24 for active AOUTO return signal from the Front Panel pots.
4. If the return signal line is active, go to Step 5. If it is not active, showing the different voltage levels from the Front Panel pots, troubleshoot Front Panel Pot Scanner U902 (an 8-to-1 multiplexer). Problems with a single pot output rather that a total failure of the Pot Scanner may be checked out using the MUXTEST mentioned in Step 2.
5. Check pin 25 for active return signal from the Front-Panel Switches.
6. If the SW/OUT signal line is active, the Switch Scanner circuitry is working. If it is not active, troubleshoot 1-of-8 decoder U903 and serial shift register U904 for correct operation.
7. Check pin 22 (AOUT2) for an active return signal from the Auxiliary Front Panel INTENSITY pot and Front Panel BNC connectors. Individual signal voltage levels may be checked using the Front Panel MUXTEST if the signal line is active. If switching levels are not present on the AOUT2 signal line, troubleshoot 8-to-1 multiplexer U600.
8. Check pin 9 (SWOUTA) for an active signal when one of the Auxiliary Front Panel buttons is pressed (bezel, SELECT, STATUS, MENU OFF). Otherwise, a HI is being shifted out of serial shift register U700. If the SWOUTA signal does not show a square pulse when one of the buttons is pressed, troubleshoot U700.

## Table 6-6 (cont)

## Front Panel MUXTEST:

An intermittent failure or noisy front panel pot can produce inconsistent control changes. To test individual pots for smooth operation and full range control limits, the Front Panel MUX SELECT test may be used to provide stable triggering.

1. Turn the power off and connect pins 2 and 3 of $J 155$ together.
2. Ground the MUXINH signal at the end of R815 nearest the front of the $\mathbf{2 4 4 0}$ to DGND.
3. Connect the test scope to observe the AOUTO signal at R800 pin 8. Trigger the test scope on MUXSEL2 at R800 pin 4. Set the SEC/DIV switch to $100 \mu \mathrm{~s}$ and the VOLTS/DIV to 2 V .
4. Power on the 2440. When it does the power-on test, it will signal a test failure of 4300 on the Trigger LEDs, and there will be no display on the 2440 crt .
5. Rotate the following rate position pots:

CH 1 Vertical Position
CH 2 Vertical Position
Horizontal Position Cursor/Delay Position
6. Check that the pots go into the rate region at both extremes of rotation and that the voltage level for each pot moves smoothly from one amplitude level to the other (approximately 0.5 V to 5 V total range) as the pot is rotated. See the test waveform illustration to identify the portion of the waveform associated with the control being rotated.


Figure 6-7. Mux Test waveforms.
7. Rotate the following infinite rotation pots:

Trigger Level Control
Holdoff Control

Table 6-6 (cont)
8. Check that both sides of the pot have equal output range (approximately 0 V to 5 V ) and that the voltage level for each side of each pot moves smoothly from one extreme to the other as the pot is rotated through the continuous range (not its end-switching region).
9. Connect the test scope to observe the AOUT2 signal at R809. This signal is from the Auxiliary Front Panel circuitry.
10. Momentarily short the shell of each of BNC input connectors to its coded-probe-switching ring and observe that the voltage level for that connector goes from 5 V to 0 V .
11. Rotate the infinite rotate INTENSITY pot and check for smooth voltage level changes on both sides of the pot (from approximately 0 V to 5 V ).
12. The two remaining analog levels are the CH 1 and CH 250 ohm overloads. Check that they are approximately 3 V each.

Bell Circuit (schematic diagram 20):
Remove the word trigger probe, then:

1. Connect a probe to the emitter of A12Q592. Then select the B TRIGGER SOURCE menu and press the BEZEL switch for WORD. The voltage should go close to +4 V with about a 1 V p-p, 2 kHz square wave superimposed upon it (peak of 5 V ).

If the 4 Vdc is not present, check the signal path back to A 12 U 760 pin 16 . If the $\mathbf{2} \mathbf{~ k H z}$ is missing, check back to the oscillator circuit A12U274.

## CALIBRATOR PROBLEMS

Calibrator (schematic diagram 13):

## NOTE

Make sure that you have not made the mistake of viewing the Calibrator signal output with a $10 \mathrm{M} \Omega$ probe and have the channel in $50 \Omega$ input termination.

The calibrator circuit can be split into two parts. The source of the signal (CALCLK input at W122 pin 2) and the analog output stage on circuit board A13.

1. Check for a 3 V square-wave signal at the forward end of R831 ( $100 \Omega$ resistor under A13U831 near the cable connector). If present, the problem is in U831, U731, Q831, or one of the parts in that output amplifier circuit.
a. Check U831 pin 8 for a signal.
b. Check U831 pin 2 for +2.4 V .
c. Check U831 pin 1 for +5.1 V .
d. Check emitter of Q831 is the same as the base of Q831.
2. Check for a $3 \vee$ square wave at A11U680 pin 18. If present, the problem is a defective cable connection from A11 to A13 boards.
3. Check for a square-wave signal at A11U680 pin 2. If present, replace A11U680.
4. Replace A11U670.

Table 6-6 (cont)

| VIDEO OPTION | Video Option (schematic diagram 21): <br> If Video triggers are selected and the menu says not installed, then the diagnostics have detected a problem (if the option is installed). See Table 6-7, the Video Option troubleshooting table. |
| :---: | :---: |
| WORD TRIGGER | Word Trigger (schematic diagram 20): |
|  | 1. Make sure the Word Trigger probe connector is properly installed (connector is on the 2440 rear panel). |
|  | 2. Select TRIG POSITION to $1 / 8$, SEC/DIV to $100 \mu \mathrm{~s}$, and VOLTS/DIV to 2 V . Probe A12U754 pin 5 for clock pulses. If not present, verify A12U754 pin 1 (RESET) is HI and A12U754 pin 11 has clock pulses. Replace A12U754 if the signals at pins 1 and 11 are ok. |
|  | 3. Verify that the flex connector at the back of the A12 board is installed correctly. If ok, then the WORD RECOGNIZER probe is possibly defective. Try the probe on another 2440 to verify its operation. |

DAC SYSTEM FAILURE

DAC System (schematic diagrams 5 and 6):
Symptoms are CCD and Peak Detectors gain fails SELF CAL, and Trig Level fails SELF CAL.

1. Check TP650 (found on the Main Board) for 0 V .
2. Check TP660 (also on the Main Board) for +1.25 V .
3. If the test point voltages are good, the DAC SYSTEM is operating normally to this point. Troubleshoot the DAC multiplexers (U831, U821, U960, and U830) and the individual DAC output ports (schematic diagrams 5 and 6).
4. If the levels at TP650 and TP660 are bad, check DAC multiplexer U651, the DAC inputs (U800 pins 1 through 12), and current-to-voltage converter U661C. Should see U661C having an output of 32 dc levels, switching from one to the next each 2 ms , and then repeating. The maximum output level is $\pm 1.36 \mathrm{~V}$. This output signal should be present at the input to each of the DAC multiplexers (pin 3), and each multiplexer output pin should have a steady dc voltage level present.
5. Check that only one DAC MUX enable at a time from U272 is LO.
6. Use the FORCE DAC test to check suspected output ports for correct control range.

## Force DAC Test

1. Press the SPECIAL menu choice under Extended Functions and then press FORCE DAC.

## NOTE

The SPECIAL menu choices are normally disabled to the user and press of the SPECIAL menu button calls up the display "DISABLED-SEE MANUAL". To enable the choices for servicing, the cabinet must be removed and Jumper A13/156 (EXT CAL DIS on diagram 13) must be removed.
2. The first and second bezel buttons are used to select through the DAC values to be tested. The INTENSITY knob sets the values.
3. Test suspected DAC circuits for correct voltage limits over the control range using the test points and values given in the following Force DAC Ranges table.

Table 6-6 (cont)

| Force DAC Ranges |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DAC <br> Output | DAC Output Location | FORCE DAC Values/ DAC Voltage After Cold Start | Voltage Range |  | Effect of Increasing Value |
|  |  |  | 0 | 4095 |  |
| $\begin{aligned} & \text { CH1Bal } \\ & \text { CH2Bal } \end{aligned}$ | $\begin{aligned} & \hline \text { U641-7 } \\ & \text { U641-1 } \end{aligned}$ | 2048/-0.50 | -1.37 | 1.36 V | Trace shifts down |
| CH1Gain CH2Gain | U641-8 U641-14 | 1540/-4.37 V | -6.48 V | 1.58 V | Gain decreases |
| 1 POS | U630-1 | 2048/5 Va | -4.35 V | -5.66 V | Trace moves up |
| GN11 <br> GN12 <br> GN13 <br> GN14 <br> GN21 <br> GN22 <br> GN23 <br> GN24 | U841-1 <br> U841-7 <br> U841-8 <br> U841-14 <br> U951-1 <br> U951-7 <br> U951-8 <br> U951-14 | 2048/-0.50 Vb | -1.37 | +1.36 | The channel and CCD side indicated by the DAC output is offset from remaining sides. ${ }^{c}$ |
| CT11 <br> CT12 <br> CT13 <br> CT14 <br> CT21 <br> CT22 <br> CT23 <br> CT24 | U840-1 <br> U840-7 <br> U840-8 <br> U840-14 <br> U950-1 <br> U950-7 <br> U950-8 <br> U950-14 | 2048/-0.50 V ${ }^{\text {d }}$ | +4.76 | +12.1 | The channel and CCD side indicated by the DAC output is offset from remaining sides. ${ }^{e}$ |
| CM10 | U631-1 U631-7 | $\begin{aligned} & 1650 /-0.27 \mathrm{Vf} \\ & 2000 /-0.04 \mathrm{~V} \\ & 2200 /-0.10 \mathrm{~V} \\ & 1650 /-0.27 \mathrm{~V} \\ & 2000 /-0.04 \mathrm{~V} \\ & 2200 /-0.10 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & +4.76 \\ & +4.76 \\ & +4.76 \\ & +4.76 \\ & +4.76 \\ & +4.76 \end{aligned}$ | $\begin{aligned} & +12.1 \\ & +12.1 \\ & +12.1 \\ & +12.1 \\ & +12.1 \\ & +12.1 \end{aligned}$ | CH 1 CCD Sides 1 and 3 offset from 2 and 4. <br> CH 1 CCD Sides 2 and 4 offset from 1 and 2. |

aDAC values for CH 1 and CH 2 POS are not written after a COLD START until an acquisition occurs: Tum off EXT DIAG menu and press ACQUIRE; then return to FORCE DAC.
bEach GNxx DAC output has a unique constant for each SEC/DIV setting between 100 and $\mathbf{1 0 0} \mathbf{n s}$. Each of these constants is set to 2048 when the instrument is cold started.

CFor example, GN23 is the GN DAC output for side 3 of the CH 2 CCD; so side 3 is offset from sides 1, 2, and 4.
${ }^{\text {deach CTxx DAC output has a unique constant for each SEC/DIV setting in both Normal and Envelope Acquire modes. Each of these }}$ constants is set to 2048 when the instrument is cold started.
${ }^{\circ}$ For example, CT14 is the CT DAC output for side 4 of the CH 1 CCD; so side 4 is offset from sides 1, 2, and 3.
'Each CMxx DAC output constant varies with SEC/DIV setting: The first value given is for $\mathbf{5 0} \mathbf{n s}$; the second for 100 ns ; and the third for $\mathbf{2 0 0} \mathbf{n s}$. SEC/DIV should be set accordingly when checking for correct voltage limits over DAC range.

Table 6-6 (cont)

${ }^{9}$ Each TRNx DAC output has a unique constant for each VOLT/DIV setting between $\mathbf{2} \mathbf{~ m V}$ and $\mathbf{5 0} \mathbf{~ m V}$. Each of these constants is set to $\mathbf{2 0 0}$ when the instrument is cold started.
nLimit at a DAC count of approximately 2000.
iDACG (DAC Gain) interacts with DACO (DAC Offset); therefore, the DACG range can be limited if DACO is not centered. Changing either DACG or DACO causes the remaining DAC System outputs to be invalid until the correct settings for DAC Gain and Offset are rewritten into the DAC System.

Table 6-6 (cont)
HOLDOFF Trigger Holdoff Circuitry (schematic diagram 13):
PROBLEMS

## SEQUENCER OUTPUT PROBLEMS

Run Extended Diagnostic test 2600 for the SIDE-BOARD registers U761 and U762. If that fails, troubleshoot the indicated failure.

If not, troubleshoot the Trigger Holdoff circuitry.

1. Check the emitter voltages for logical HI/LO as follows:

| SEC/DIV | Q761 | Q771 | Q772 | Q783 |
| :---: | :--- | :--- | :--- | :--- |
| 500 ns | HI | LO | LO | -15 V |
| $1 \mu \mathrm{~S}$ | LO | HI | LO | -15 V |
| $10 \mu \mathrm{~S}$ | LO | LO | HI | +5 V |

If these levels are not correct, suspect the corresponding emitter diode, or the transistor emitterbase junctions as being defective. Observe that Q783 has no emitter diode, so suspect the transistor itself or Q782.

Some triggering failures are an indication of possible problems with the ATHO (A trigger holdoff signal). If ATHO is stuck HI, no triggers will be permitted by A/B Trigger Logic Array U150; if stuck LO, the triggering will be unstable.
2. Check the signals around flip-flop U872 for proper action of that device (see the test waveforms associated with the circuit next to schematic diagram 13).

Test scope: Select ENVELOPE 1 and AUTO TRIGGER MODE. Scope under test: Select $5 \mathrm{~ns} /$ div, trigger on the CAL signal, and set HOLDOFF to minimum.

Sequencer Output circuitry (schematic diagram 20).
SEQUENCE OUT doesn't switch LO at the end of a sequence or back HI when the sequence is exited after completion:

1. Create a sequence with one step and no PAUSE. The front-panel setup is arbitrary for the step (see Operators Manual for operating the Sequencer).
2. RECALL the sequence. Check that Q104's collector is HI before the sequence is recalled, switches LO at the end of a sequence, and switches back $H I$ when the sequence is exited (see Operators Manual for operating the Sequencer).

If the collector switches properly, the problem is an open component in the R104-J125/P125-Flex Cable-J1903 path.
3. If collector doesn't switch, either the transistor, its collector supply, or its base drive is bad (CR104 may also be shorted). Isolate base drive to Q104 via R300 to determine whether drive or output circuitry is bad. The driving signal comes from I/O register block of schematic diagram 1.

## SEQUENCER OUTPUT PROBLEMS

Sequencer Output circuitry (schematic diagram 20).
STEP OUT doesn't switch LO at the end of a sequence step or back HI at the start of the next sequence step:

1. Create a sequence containing at least two steps. The front panel setup is arbitrary for both steps, but set PAUSE on in the ACTIONS menu associated with the first step (see Operators Manual for operating the Sequencer).

## Table 6-6 (cont)

2. Check that Q107's collector switches LO at the end of a step (should stay LO at end of PAUSE'd step 1) and back HI when the sequence is restarted (push PRGM).

If the collector switches properly, the problem is an open component in the R107-
J125/P125-Flex Cable-J1904 path.
3. If collector doesn't switch, either the transistor, its collector supply, or its base drive is bad (CR107 may also be shorted). Isolate base drive to Q107 via R108 to determine whether the drive or output circuitry is bad.
The drive signal comes from I/O register block of schematic diagram 1.

GPIB CAPABILITY AVAILABLE FOR EXTENDED DIAGNOSTICS
Extended Diagnostics test may be run via the GPIB interface to track down failed devices when the Front Panel is locked up due to a front-panel failure or when there is no display visible. The importance of this is that the initial step of locating all problem areas is simplified when the 2440 can do it itself.

1. If the hardware and software are available to interface a 2440 to a GPIB controller, then run the Extended Diagnostics test. Troubleshoot any failed diagnostics test as indicated in Procedure 7.
2. If GPIB interface is not available, go to Procedure 6 to troubleshoot the display problem.

DISPLAY TROUBLESHOOTING
No Intensity (HV Supply and CRT, schematic diagram 19):
If there is no GPIB capability, troubleshooting is going to be more difficult if no display is available. The steps in this table address the analog problems not detectable by the Extended Diagnostics in any case. Digital failures of the Display System are covered in the troubleshooting tables in the "Diagrams" section at the back of this manual.

1. Press STATUS to set READOUT level.
2. If no display is present, check the crt intensity grid voltage (V1000 pin 3), the grid bias adjust, the crt cathode and heater circuits, and the crt anode HV.

## WARNING

A High Voltage probe is required to measure the grid, cathode, and anode voltage of the crt.
3. If no voltages are present, troubleshoot the HV power supply. The -15 V Unreg supply is fused by F961 (schematic diagram 23) which will be open if a component failure in the HV power supply caused excessive loading.
4. If crt voltages are good, and still no intensity, turn off the 2440 and check the crt heater for continuity from pins 1 to 14 . If open, change the crt.
5. Does intensity vary with the Grid Bias Adjust? If not, troubleshoot the DC Restorer circuit. If it does, check the signal from U227 at pin 13.
6. Check input to U227 $\overline{Z O N}$ on pin 3. If input ok, check supply voltages to U227. If all ok, change U227.
7. If $\overline{Z O N}$ not present, troubleshoot the Z-Axis Logic circuitry, U223C and input gates and signals (schematic diagram 17).
8. If all ok in the crt and Z-Axis circuitry, go to the "No Display" troubleshooting tree at the back of this manual. Also, check that the Power-on Self Test completes without hanging. (See "System $\mu \mathrm{P}$ Halts in Power-up Test" following "No Intensity Control.')

No Intensity Control

1. Check signal output of U227 at pin 13. Is the waveform correct (see waveform 145 on schematic diagram 19), and does its amplitude vary with the DISP INTENSITY control? If yes, then check the signal path components to the junction of CR442 and R546 for continuity.
2. If the signal at U227 pin 13 does not vary with the DISP INTENSITY control, check CR135 for open or short.
3. Check the ZINT signal on pin 2 of U227. Does it vary correctly with the DISP INTENSITY control? If yes, suspect U227. If no, then use the FORCE DAC test to verify the INTENSITY pot and the DAC SYSTEM.
4. If the INTENSITY pot changes the DAC settings in the FORCE DAC test, the pot and potscanning circuitry are ok; if not, troubleshoot the Front Panel.
5. Check the suspected DAC outputs at the points indicated in the FORCE DAC test table. If DAC outputs are ok, troubleshoot Intensity multiplexer A10U811 (schematic diagram 6) and its select signals, and the Z-axis signal amplifiers (A10U810 and A10U812). Troubleshoot DAC circuit if the DAC outputs are bad (see the DAC System troubleshooting procedure).
6. Check the DISDN signal at U414A pin 6 and the PRESTART + DISPLAY signal at U323A pin 3 for correct operation (schematic diagram 17). If not correct, troubleshoot the Readout State Machine (see the "No Display" troubleshooting tree at the back of this manual).

SYSTEM $\mu$ P HALTS IN POWER-UP TEST

Test 3000-TRIG and READY LEDs on or Test 6000_READY and ARM LEDs on, and the 2440 Self Test has halted.

Problem is probably in the Display State Machine circuitry (schematic diagram 17) or the DISDN signal path to the System $\mu$ P Interrupt circuit. Check that the DISDN signal is correct at U414 pin 6 (waveform 126 on schematic diagram 17); if not, troubleshoot the Display State Machine (see NO DISPLAY troubleshooting chart in the "Diagrams" section for typical Display State Machine waveforms). If the DISDN signal is ok, check the DISDN signal path to U580 pin 4 for continuity.

Test 8000 —plus (+) LED on and Self Test has halted.

1. "Running Self Test" message is displayed, but nothing else is occurring.

Check the ACQDN signal at A11U670 (Time Base Controller).
2. No display is seen.

Check operation of the Readout State Machine.

Table 6-6 (cont)


#### Abstract

FOCUS If all the focus voltages and adjustments are correct in the following checks and proper focusing cannot be attained, suspect a defective crt. Check all the crt voltages and EXT CAL Display ADJUSTS for the crt to verify their accuracy before changing a suspected crt.

No Focus at Any Intensity: 1. Check the ASTIG adjustment. 2. Check junction of R262 and R145 for a voltage swing of 0 to 15 V as the FOCUS pot is adjusted from one extreme to the other. If not correct, troubleshoot pot, connectors between the pot and the junction, and the 15 V supply to the FOCUS pot. 3. Check at the collector of Q152 for a voltage swing of -175 V to -115 V as the FOCUS pot is adjusted from one extreme to the other. 4. Check for -300 V at the junction of R248 and R247. If not correct, check CR611, CR610, C618 and the 150 V peak ac supply.


## WARNING

## An HV probe is required for the following step.

5. Check the intensity grid, cathode, and anode voltages for correct levels. If not correct, troubleshoot faulty circuit.

Poor Focus at High Intensity:

1. Check the HIGH DRIVE FOCUS adjustment.
2. Check the wiper of R400 for a varying voltage as the DISP INTENSITY is increased to high intensity levels. If not correct, check Q500, CR500 and VR316 for shorts or opens.
3. If the output of R400 tracks the display intensity changes, check R395, R297, C295, and P174.

## Poor Edge Focus:

1. Check the EDGE FOCUS adjustment.
2. Check the collector of Q269 for a voltage swing of -131.8 V to -111.8 V as the EDGE FOCUS pot is adjusted from one extreme to the other. Check the wiper of R300 for a voltage swing of 0 to 50 V as the pot is adjusted from one extreme to the other. If not correct, check the pot and the +61 V supply.

DEFLECTION | Display Output (schematic diagram 18): |
| :--- |
| PROBLEM |
| Vertical Deflection Bad (Horizontal stripe only) or Horizontal Deflection Bad (Vertical stripe only). |
| 1. Press PRGM and then press the fifth menu selection button to do a PANEL INIT. |
| 2. Connect the CALIBRATOR output signal to the CH 1 BNC using one of the supplied 10X |
| coded probes. Set the 2440 VOLTS/DIV setting to 200 mV . Press SAVE on the 2440 , |
| then MENU OFF. |

Table 6-6 (cont)
3. Trigger the test scope on the $\overline{Z O N}$ signal at U223 pin 8 (schematic diagram 17). Set the test scope Trigger Coupling to HF Reject and Slope to - (minus).
4. Use the test scope to compare the circuit signals at the points indicated in schematic diagram 18 to the corresponding waveforms shown next to the diagram. (The HOLDOFF control will be of some use in obtaining a stable display if using an analog scope. If using a 2440 as the test scope, press SAVE to obtain a stable display, if necessary, for viewing.)
5. Troubleshoot as necessary if incorrect waveforms are found. If none of the waveforms are correct, problem is either U170 or bad input from the Vertical Display DAC, (U142) for bad vertical deflection. For bad horizontal deflection, problem is either U370B or bad input from the Horizontal Display DAC, U250. If bad input signals, troubleshoot the Display and Attributes Memory and Display DACs (schematic diagram 16). See "Distorted Display" troubleshooting chart at the back of this section.
6. If the waveform at U 170 pin 6 is correct (or U370B pin 7 for the horizontal signal), but not correct at the integrator output, check that the sample switch (U270B) is getting the SAMPLE drive signal. Troubleshoot the Vertical or Horizontal vector generator circuitry.
7. Is display switching correctly for dots, envelope, vector, and readout displays? If not, check multiplexer U290 and select signals (AMP0 and AMP1).

## EXTENDED DIAGNOSTICS

If unfamiliar with the use or operation of the extended diagnostics routines of this scope, the calibration and diagnostics information supplied in the Diagnostics subsection of this section may prove very useful.

| 0000 | Running extended diagnostics at this level runs all tests. It is equivalent to SELF DIAG in the |
| :--- | :--- |
| EXTENDED | CAL/DIAG menu. A failed test is indicated by a FAIL label in the main Extended Diagnostics menu. Go |
| DIAGNOSTICS | to the lower testing levels of a failed test to isolate the failure. |

## 1000 System ROM A12U670, A12U680, A12U682, A12U690, and A12U692 (schematic diagram 1)

SYS-ROM

## Testing Method:

Run from this level, all ROM tests are selected in turn, or an individual test numbers $\mathbf{1 1 0 0 - 1 5 0 0}$ may be selected and run.

These tests compute the cyclic redundant word for the contents of the ROM. The resulting value is compared to the stored value of the first word of the ROM (the previously computed CRCC). A correct match indicates a good ROM.

If marked FAIL in the main Extended Diagnostic menu, go to the next level and run the test to determine the failed ROM or ROMs.

[^9]Table 6-6 (cont)
For tests 1200-1500, the sublevel test number and the numerical suffix in the test label indicate the page and ROM device the test is run on. For instance, the sublevel test "1320 ROM0.1-5" is run on page 5 of 16 possible pages, where page 5 is part of ROM0.1 (U682).

The System Processor drives the System Address Decode circuitry to select the device and page from the System ROM. U890B provide the ROM0.0-3 chip select signals for selecting the ROM device accessed, and, if the ROM selected is one of the four paged ROMs, U860 supplies the page-selecting address bits, PAGE-BIT2 and PAGE-BIT3. Using test 1320 again as an example, U890B sets ROM0.0 LO to select ROM0.1 (U682), and U860 sets Page Bits 3 and 2 to LO (0) and HI (1), respectively, to select the second address page within the ROM device (the second page of that device is the 5th page of the 16 pages available for System ROM).

## NOTE

The page number associated with the sublevel test labels are based on viewing the 16page memory as having the following sequence: the first four pages (pages 0-3) are located in the first four 16-Kbyte address spaces of ROM0.0-ROM0.3, respectively; the second four pages (4-7) in the second four 16-Kbyte address spaces, respectively; etc. That is why, in the previous example, the label for test level 1320 is "ROMO.1-5" where " -5 " indicates the fifth page. Page 5 is the fifth page for the entire paged-System ROM; it is the second page (or 16-kbyte memory space) for U682.

Troubleshooting Procedure:

1. A failed ROM test indicates a defective ROM. Check that the correct ROMs are installed in the correct sockets.

Check out the supply voltages and the chip select to a failed ROM to verify them.
2. A failure of most or all paged ROM indicates a paging chip select problem. The last condition is probably not detectable as the System $\mu \mathrm{P}$ is unable to obtain it operating instructions from the ROM. The System $\mu$ P Kernel test (given in Procedure 8) may be used to check that the microprocessor is operating and to check the chip-select addressing circuitry for correct operation.

| 1100 ROM1 | Base page ROM, A12U670 |
| :--- | :--- |
| 1210 ROM0.0- | 1st quarter of A12U680 ( page 0) |
| 1220 ROM0.0-4 | 2nd quarter of A12U680 ( page 4 ) |
| 1230 ROM0.0-8 | 3rd quarter of A12U680 ( page 8) |
| 1240 ROM0.0-C | 4th quarter of A12U680 ( page C ) |
| 1310 ROM0.1-1 | 1st quarter of A12U682 ( page 1) |
| 1310 ROM0.1-5 | 2nd quarter of A12U682 ( page 5) |

Table 6-6 (cont)

| 1310 ROM0.1-9 | 3rd quarter of A12U682 ( page 9 ) |
| :--- | :--- |
| 1310 ROM0.1-D | 4th quarter of A12U682 ( page D ) |
| 1410 ROM0.2-2 | 1st quarter of A12U690 ( page 2 ) |
| 1410 ROM0.2-6 | 2nd quarter of A12U690 ( page 6 ) |.

Table 6-6 (cont)

| $\begin{aligned} & 2110 \\ & \text { DIAGO } \end{aligned}$ | Page Control Register (PCREG) A12U860 (schematic diagram 1): |
| :---: | :---: |
|  |  |
|  | Testing Method: |
|  | Sets PCREG (bit D7) $=0$ and tests for $=0$ (stuck at one). Sets PCREG (bit D7) $=1$ and tests for $=$ 1 (stuck at zero). If both tests pass, the result flag is set to PASS; otherwise, it is set to FAIL. |
|  | If test = FAIL then look for failure using the following steps: |
|  | 1. On the test scope, connect CH 1 to J 125 pin 15. Select Slope, + (plus); Trigger Source, CH 1; Trigger Level, 1 V ; CH 1 and CH 2 input coupling, DC; CH 1 and CH 2 VOLTS/DIV, 2 V . This step provides a positive, TTL-level trigger strobe (or pulse) for validation of the signal being tested while a test is running. The test scope setup will be used in each of the Registers troubleshooting procedures. |

Now using CH 2 probe:
2. Run test 2110 in CONTINUOUS mode and check for clock activity at U860 pin 11 (clocks on LO-to-HI transition close to the end of the trigger strobe pulse); if not, troubleshoot its clocking circuitry (U884, U862, and U866).
3. Check that U860 pin 19 clocks from LO-to-HI and remains HI after the trigger strobe pulse returns to LO. If not, replace U860.
4. Test for a chip select at U854 pins 1 and 19 (LO enables). If not correct, troubleshoot System Address Decode circuitry (U884, U862, and U866).
5. While selected, check that U854 pin 11 is set to the state of U860 pin 19. If DIAGO failed and the chip selects to U854 and the signal to U854 pin 11 are ok, then U854 is probably defective.

Interrupt Register A12U654 (schematic diagram 1) and DCOK logic circuitry A16U395 and associated components (schematic diagram 23):

## Testing Method:

The power supply sends a TTL signal to the interrupt register to inform the System $\mu \mathrm{P}$ of the logic AND of the power supply voltages. DCOK tests INTREG (bit 7 ). If $=1$, the test result $=$ PASS; otherwise, the result $=$ FAIL.

## Troubleshooting Procedure:

If test $=$ FAIL then look for failure using the following steps:

1. Set up the test scope as per Step $\mathbf{1}$ of the $\mathbf{2 1 1 0}$ troubleshooting procedure.

Now using CH2 probe:
2. Run test 2120 in CONTINUOUS MODE and check for INTREG chip select on pins 1 and 19 of Interrupt Register U654. If not present, troubleshoot the System Address Decoding circuitry (U884, U862, U866A, U870B, and associated components) for proper inputs and outputs.
3. While the test is running, test U654 pin 17 for steady-state HI value. If HI and DCOK fails, then replace U654. If LO, then check the power supply voltages and the DCOK AND circuit. If supply voltages are not correct, troubleshoot the low-voltage power supply and regulators; if voltages are correct, troubleshoot A16U395 and associated components (schematic diagram 23).

Processor Miscellaneous Out and Processor Miscellaneous in Registers (A12U750 and A12U854)
Page Control Register A12U860 (schematic diagram 1), OR-gate A12U332D (schematic diagram 2), and Interrupt Register A12U654:

Testing Method:
To test for stuck at 1, PCREG U860 is written the pattern x00xxxxx to clear BUS REQUEST and BUSTAKE bits. Then INTREG (bit 6 ) is tested for $=0$, and the PASS/FAIL results are set accordingly.

The PCREG is set for a BUSTAKE ( $\mathbf{x} 1 \mathrm{x} x \mathrm{x} \times \mathrm{x} \mathrm{x}$ ). This time the INTREG (bit 6 ) should $=1$. The result is set to FAIL if the test fails.

## Troubleshooting Procedure:

If test $=$ FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:
2. Run test 2130 in CONTINUOUS MODE and check for $\overline{\text { NTREG }}$ chip select at U654 pin 1 and 19. If not present, troubleshoot the System Address Decoding circuitry (U884, U862, U866A, U870B, and associated components) for proper inputs and outputs.
3. Check that BUSTAKE on PCREG U860 pin 16 has LO-to-HI and HI-to-LO transitions on alternate PCREG chip selects. If not, suspect problem with U860.
4. Check INTREG U654 pin 15 for a LO-to-HI transition when BUSTAKE on PCREG U860 pin 16 is set from LO-to-HI; if not, then check U332D (schematic diagram 2) for correct gating. Diagnostic Bit 1 (schematic diagram 1):

Testing Method:
This is the first test for the PMISCOUT and PMISCIN registers. The byte to PMISCOUT U760 is set to 00000000 and PMISCIN (bit 4) is tested for $=0$. The test result flag is set PASS or FAIL. PMISCOUT is then set to 10000000 and PMISCIN (bit 4) is again tested. If the test fails, the test result is set to FAIL.

## Troubleshooting Procedure:

If test $=$ FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:
2. Run test 2140 in CONTINUOUS MODE and check for chip select at $U 760$ pin 11. If not present, troubleshoot the System Address Decoding circuitry (U884, U862, U866A, U870B, and associated components) for proper inputs and outputs.
3. Test U760 pin 19 for a LO-to-HI transition between chip selects. If missing, replace U760; if ok, suspect U854.

Table 6-6 (cont)

Interrupt Latch (COMREG) A12U550 and Display Status Register (SSREG) A12U542 (schematic

Testing Method:
A BUSTAKE is executed (previously tested) and the $4 Q$ output of U550 (pin 15) is set LO. SSREG U542 bits 0 and 1 (pins 16 and 18) are then tested to see if they are LO, and the test results are set accordingly.

NOTE
The inputs of U542 (pins 2 and 4) are wired together.
Pin 15 of U550 is then set HI and SSREG bits 0 and 1 are tested for HI . If the test fails, the test result is set to FAIL.

Troubleshooting Procedure:
If test $=$ FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using CH 2 probe:
2. Run test 2150 in CONTINUOUS mode and check that U550 pin 1 (COMREG) is set LO during the period that the clock line (WWR) to U550 at pin 9 has a LO-to-HI transition. This may be done by saving the COMREG signal in REF1 and displaying it at the same time as the clock pulse on U550 pin 9 is acquired. If these signals are not coincident, then troubleshoot the cause and correct the problem. See Figure 6-8 for typical register test waveforms.


Figure 6-8. Typical Register test waveforms.

Table 6-6 (cont)
3. Check that U550 pin 15 has a LO-to-HI transition after the second clock pulse goes LO-to-HI. If no transition, change U550; if ok, check chip enable of U542 on pin 1 (SSREG) to be LO after $\overline{W R R}$ on U550 pin 9 goes LO-to-HI. If ok, then suspect U550. If the enable is defective, troubleshoot and correct the problem.

## 2160

 WPDNWaveform $\mu$ P Done A12U550 (schematic diagram 2):

## Testing Method:

A BUSTAKE is executed (previously tested) and pin 10 of Interrupt Latch U550 is set LO. Then pin 14 (bit 2) of PMISCIN register U854 (schematic diagram 1) is tested for a LO, and the test results are set accordingly.

Then pin 10 of U550 is set HI , and U854 pin 14 is tested for a HI. If test fails, the test result is set to FAIL.

## Troubleshooting Procedure:

If test = FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using CH 2 probe:
2. Run test 2160 in CONTINUOUS mode and check that U550 pin 1 (COMREG) is set LO during the period that the clock to U550 pin 9 (WRR) has a LO-to-HI transition. This may be done by saving the COMREG signal in REF1 and displaying while acquiring the clock pulse on U550 pin 9 . If these signals are not coincident, then troubleshoot the cause.
3. Check that U550 pin 10 has a HI-to-LO transition on the first enable and a LO-to-HI transition after the second clock pulse goes LO-to-HI. If bad, change U550; if good, check chip enable at U854 pins 1 and 19 is LO after U550 pin 10 goes from LO-to-HI. If ok, then suspect U854. If the enable is defective, troubleshoot and correct the problem.

2170
DIAG2

Diagnostic Bit 2 Word Trigger Register A12U754 (diagram 20):

## Testing Method

WDREG U754 pin 19 (DIAG2) is set to 0xxxxxxxx and PMISCIN A12U854 pin 5 (bit D6) (schematic diagram 1) is tested for 0 . The test result is to PASS or FAIL accordingly.

WDREG U754 pin 19 (DIAG2) is then set to $1 x x x x x x x x$ and PMISCIN U854 pin 5 (bit D6) is tested for 1. If the test fails, the test result is set to FAIL.

WDREG also drives the GPIB LEDS on the front panel. Bit patterns $x x x x x 000$ to $x x x x x 111$ are sent in a binary sequence with a 50 ms delay between patterns. The register is then reset to entry values.

## Troubleshooting Procedure:

If test $=$ FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

## Table 6-6 (cont)

Now using CH 2 probe:
2. Check that U754 pin 1 RESET is HI .
3. Run test 2170 in CONTINUOUS mode and check the clock line to A12U754 at pin 11 for LO-to-HI transitions. Since this is the register that provides the strobe to WORD TRIG, there should be four clock pulses, one at each end of the trigger strobe and two under it. If not, troubleshoot the clock source to isolate the problem.
4. Test that U754 pin 19 has a LO-to-HI transition on the third strobe. If there is no LO-to-HI transition, replace U754. If there is, then test A12U854 pin 15 for the same signal as at $\mathbf{U 7 5 9}$ pin 19. If present, replace U854; if not, find the open.

Video Option Mode Register A12U750 (schematic diagram 20):
FLD2

## Testing Method:

TVREG U750 is set $=00000000$ and PMISCIN A12U750 pin 3 (schematic diagram 1) is tested for 0. The test result is set accordingly.

TVREG U750 pin 2 (bit DO) is then set to 1 and PMISCIN (bit D7) is tested. If the test fails, the test result is set to FAIL.

Troubleshooting Procedure:
If test $=$ FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:
2. Run test 2180 in CONTINUOUS mode and check the clock line to A12U750 TVREG, pin 11 (schematic diagram 20) for LO-to-HI transitions. There should be two clock pulses under the trigger strobe. If not, troubleshoot the clock source back through Decoder A12U884 (schematic diagram 1) to isolate the problem.
3. Test that U750 pin 2 (FLD2) has a LO-to-HI transition on the second strobe. If there is no LO-toHI transition, replace U750. If there is, then test U854 pin 17 (schematic diagram 1) for the same signal as at U750 pin 2. If present, replace U854; if not, find the open.

## 2190

 MWPDNMiscellaneous Register A12U760 (schematic diagram 1):
Testing Method:
A BUSTAKE is executed (previously tested), Interrupt Latch bit D2 is set true (WPDN) and PMISCOUT Register U760 pin 2 (the mask for WPDN), is set to 0.

INTREG U654 pin 18 (bit $D 0$ ) is tested for 0 and the test result is set accordingly.
PMISCOUT U760 pin 2 (bit D0) is set to 1 which should unmask the WPDN that is already set true. INTREG (bit 0 ) is tested for 1 . If test fails, the test result is set to FAIL.

Troubleshooting Procedure:
If test $=$ FAIL then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:
2. Run test 2190 in CONTINUOUS mode and check that A12U550 pin 1 COMREG (schematic diagram 2) is set LO during the period that the clock line U550 pin 9 has a LO-to-HI transition. This may be done by saving the COMREG signal in REF1 (if using a 2440 as the test scope) and displaying it while acquiring the clock pulse on U550 pin 9 . If these signals are not coincident, then troubleshoot the cause.
3. Check that U550 pin 2 has a LO-to-HI transition on the second clock pulse. If bad, change U550. If ok, store in REF1 and display it while testing output of A12U880 pin 6 (schematic diagram 1). If ok then replace U654; if not, check the inputs to U880 on pins 4 and 5, and if those are ok, replace U880.

2200
TB-DSP

Display Control Registers (schematic diagram 17):
Testing Method:
Running the test from this level will test all the Display Control registers. These tests will utilize four bit patterns to detect faults. If marked FAIL at this level, go to the lower levels in the menu to test for the failed register. The four bit patterns sent in each of the register tests are as follows:

Test 1-10100101 is sent to the input latch and read back via the output buffer. Test result is set to fail if not a match.

Test 2—01001011 is sent and read back. Test result is set to fail if not a match.
Test 3-10010110 is sent read back. Test result is set to fail if not a match.
Test 4-00101101 is sent and read back. Test result is set to fail if not a match.
NOTE
DISCON (bit 0) will not change, as it has the main board diagnostics as its input.

Misc Registers A11U532 and A11U540 (schematic diagram 17):
MISC
Testing Method:
The MISC register is two components; latch U532 and read-back buffer U540. The test result is set to PASS and the test is done; any failure sets it to FAIL.

If run from this level, all four tests are selected in turn. One may execute any single test by selecting 2211 to 2214. The test involves writing four unique patterns (see test 2200) to U532 and reading them back from U540. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

## Table 6-6 (cont)

Troubleshooting Procedure:
If test = FAIL for all tests, then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:
2. Run test 2210 in CONTINUOUS Mode and check U532 pin 1 for MISC to be LO during the time of the trigger strobe. If not, troubleshoot the Register Select circuitry (U550 and U450D) for proper operation.
3. Check U532 pin 19 for clock pulse activity ( $\overline{\mathrm{WR}}$ strobe from System $\mu \mathrm{P}$ ).
4. If 1 and 2 above are ok, then select a pattern test and check that the data lines are the same states as the pattern; i.e., 10100101 would have the $\mathrm{D} 7 \mathrm{pin}=1, \mathrm{D} 6 \mathrm{pin}=0$, etc.

NOTE
Must select test mode of RUN ONCE for stability.
If ok, repeat steps 2 and 3 for U540, and replace U540 if steps 2 and 3 pass.

Mode Control Register A11U541 and A11U542 (schematic diagram 17):
Testing Method:
The MODECON register is two components, latch U541 and read-back buffer U542. The test result is set to PASS, any failure sets it to FAIL.

If run from this level, all four tests are selected in turn. One may execute any one test by selecting 2221 to 2224. The test involves writing four unique patterns (see test 2200) to U541 and reading them back from U542. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

## Troubleshooting Procedure:

If test $=$ FAIL for all test then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the $\mathbf{2 1 1 0}$ troubleshooting procedure.

Now using the CH 2 probe:
2. Check U541 pin 1 for PWRUP $=\mathrm{HI}$; if not, troubleshoot Power Up circuitry (schematic diagram 23).
3. Run test 2220 in CONTINUOUS mode and check U541 pin 11 for clock pulse MODECON activity.

NOTE
First clock pulse is the write to U541, the second is the read from U542.
4. If 2 and 3 above are ok, then select a pattern test and check that the data lines are the same states as the pattern; i.e., 10100101 would have the D7 pin $=1, \mathrm{D} 6 \mathrm{pin}=0$, etc. If ok, replace U542.

Table 6-6 (cont)

2230 Display Control Register A11U530 and A11U531 (schematic diagram 17):
DISCON
Testing Method:
The DISCON (display control) register is two components, latch U530 and read-back buffer U531. The test result is set to PASS, any failure sets it to FAIL.

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2231 to 2234. The test involves writing four unique patterns (see test 2200) to U530 and reading them back from U531. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

NOTE
The readback bit (bit 0) is the main board diagnostic bit and will not be tested.
Troubleshooting Procedure:
If test $=$ FAIL for all test then look for failure using the following steps:

1. Set up the test scope as per Step 1 of the 2110 troubleshooting procedure.

Using the CH 2 probe:
2. Run test 2230 in CONTINUOUS mode and check U530 pin 1 for $\overline{\text { DISCON }}=$ LO during the time of the trigger strobe. If not, troubleshoot the Register Select circuit (U550 and U450D) for proper operation.
3. Check U530 pin 11 for clock pulse activity (WR strobe from System $\mu \mathrm{P}$ ).
4. If 2 and 3 above are ok, then select a pattern test and check that the data lines are the same states as the pattern; i.e., 10100101 would have the D7 pin $=1$, D6 pin $=0$, etc. If ok, replace U531.

Display Memory Bus Registers:
Running this test will test all the Display bus registers. There are seven tests in this section. The first two write a pattern to one register and read back from another as in the previous section.

The next three tests deal with the " Q " bus of the display state machine and require strobing of data and shifting of bits for readout.

The remaining two tests use initialized data in U441 and U440 (display and readout memory will be written with our standard four patterns in the first four bites of each memory).

If marked FAIL in the Extended Diagnostic menu, go to the next lower level of diagnostics and run those tests to determine the problem register.

## Table 6-6 (cont)


#### Abstract

2310 VCURS

Volts Cursors Register A11U241 (schematic diagram 16) Testing Method: The Volts Cursors Register test checks two components; latch U241 readback is via Diagnostic Buffer U141. The test result is set to PASS, any failure sets it to FAIL.

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2311 to 2314. The test involves writing four unique patterns (see test 2200) to U241 and reading them back from U141. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.


## Troubleshooting Procedure:

If test $=$ FAIL for all tests then look for failure using the following steps:

1. Check U241 pin 1 to be LO (VCURSEN).
2. Check VCURS clock to U241 at pin 11 for activity (save to REF1 and display for timing).
3. Select one pattern and check each output relative to the REF1 clock pulse for the proper level for that bit/pattern. If incorrect, replace U241.
4. Check U141 pins 1 and 19 for the YDIAG pulse after the clock pulse to U241. If ok, replace U141. If not present, replace U550 (schematic diagram 17).

2320 TCURS

Time Cursor Register A11U441 (schematic diagram 16):

## Testing Method:

The TCURS test checks two ICs; U441 is a latch and the read back is Diagnostic Buffer U243. The test result is set to PASS, any failure sets it to FAIL.

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2321 to 2324. The test involves writing four unique patterns (see test 2200) to U441 and reading them back from U243. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test fails and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

## Troubleshooting Procedure:

If test $=$ FAIL for all test then look for failure using the following steps:

1. Check U441 pin $\mathbf{1}$ to be LO (TCURSEN).
2. Check U441 pin 11 (TCURS) for clock activity (save to REF1 and display for timing).
3. Select one pattern and check each output relative to the REF1 clock pulse for the proper level for that bit/pattern. If incorrect, replace U441.
4. Check U243 pins 1 and 19 for the XDIAG pulse after clock pulse to U441. If ok, replace U243; if not present, replace U550 (schematic diagram 17).

## Table 6-6 (cont)

Ramp Buffer A11U130 (schematic diagram 16):
Testing Method:
If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2331 to 2334.

This test requires the display state machine to be operative. There is no "good" way to ensure that it is functional, and there have been no previous tests to help to find that out. Therefore, if this test fails, it could be for several reasons other than U130. If the power-on Self Test starts to run but halts at test level 3000 or test level 6000 (as indicated by the lighted Trigger LEDs), the problem may be in the Display State Machine circuit (schematic diagram 17) or the DISDN signal path to the System $\mu$ P Interrupt circuit. Use the Display Troubleshooting Chart to troubleshoot the Display State Machine and check that the DISDN signal at U414 pin 5 is correct.

Initialization:
DISCON $=01100000$. Significant bits are b2, b5, b6, and b7 ( $\overline{\text { STOPDIS }}$, enable "Q" bus, not ENV mode).

MODECON $=\mathbf{0 0 0 0 1 0 0 0}$. Significant bit is b3 (U140 lower half).
MISC $=00100000$. Significant bit is $\mathbf{b 5}$ (ZAXIS OFF).
The test result = PASS
The test is to load a pattern into the display counters, U220 and U211, with the LDCOUNT strobe (data loaded to U222 is fixed). Their outputs are selected by U221, U212, U210 holding U414A in the reset mode and not PRESTART. Since the STOPDIS line is LO, the display counters are selected as the source to the Q bus (U210, U212, U221). The inputs to U130 are the bits Q1..Q5 where Q1..Q3 = 0 . and Q4, Q5 are the b0, b1 data of pattern. To read back properly, shift the pattern left 3 bits and use only the lower 5 bits of XDIAG (U243).

Test 1. 10100101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 2. 01001011 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 3. 10010110 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 4. 00101101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Troubleshooting Procedure:
NOTE
Q0 through Q3 = 0. Q4 through Q11 map to D0 through D7; i.e., Q4 $=d 3$. By knowing which test FAILs and the bit pattern one may easily determine the problem bit(s) (look for the bit column in the failed tests that are the same).

If 2 or 3 tests fail, then there is a bus problem of some sort and they must be examined. If all four tests FAIL, then the problem can be in several locations.

1. $\overline{\text { LDCOUNT might not be strobing the data into Display Counters U220 and/or U211 (schematic }}$ diagram 17).
2. U414A may not be resetting, or U323 pin 3 might be HI due to a failure.
3. Address Multiplexers U221, U212, and U210 may not be operating properly.
4. Ramp Buffer U130 (schematic diagram 16) may be defective.

Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.
Now using the CH 2 probe:

1. Run test 2230 in CONTINUOUS mode and verify the LDCOUNT strobe pulse at pin 11 of U222, U220, and U211.
2. Verify that after LDCOUNT strobe, that the outputs of U222, U220, and U211 are stable and of the correct level for the test selected.
3. Verify that U323 pin 3 is LO.
4. Verify the outputs of U221, U212, and U210 are stable and correct after the $\overline{\text { LDCOUNT }}$ strobe to the previous bus.
5. Verify the chip enable to U130 pins $\mathbf{1}$ and 15 is LO. If ok to here, replace U130.

Readout Buffer U140 (diagram 16):
Testing Method:

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2341 to 2344.

This test requires the display state machine to be operative. There is no "good" way to insure that it is functional and there have been no previous tests. Therefore, if this test fails, it could be for several reasons other than U140.

Initialization:
DISCON $=01100000$. Significant bits are b2, b5, b6, and b7 (STOPDIS, enable "Q" bus, not ENVELOPE mode).

MODECON $=00001000$. Significant bit is b3 (U140 lower half).
MISC $=00100000$. Significant bit is b5 (ZAXIS OFF).
The test result $=$ PASS .

The test is to load a pattern into the display counters, U220 and U211, with the LDCOUNT strobe. The counter outputs are switched to the Q bus through U221, U212, U210 by holding U414A in the reset mode (PRESTART + DISPLAY is LO). The inputs to U140 (lower half) are the bits Q6 through Q8 where Q1 through Q3 $=0$. Q4 and Q5 are the b0 and b1 data of the pattern. To read back properly, one shifts the pattern left 3 bits and use bits 4, 5, and 6 of XDIAG (U243); the test result is set to FAIL if the test fails.

## Table 6-6 (cont)

Test 1. 10100101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 2. 01001011 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 3. 10010110 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 4. 00101101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Then MODECON is set to 00010000 to select the top half of U 140 and the pattern is shifted left 2 bits. YDIAG (U141) bits $4,5,6$, and 7 are tested, and the test result is set to FAIL if the test fails.

Test 1. 10100101 is loaded and read back via U141. Test result is set to FAIL if not a match on bits 0 through 5.

Test 2. 01001011 is loaded and read back via U141. Test result is set to FAIL if not a match on bits 0 through 5.

Test 3. 10010110 is loaded and read back via U141. Test result is set to FAIL if not a match on bits 0 through 5.

Test 4. 00101101 is loaded and read back via U141. Test result is set to FAIL if not a match on bits 0 through 5.

NOTE
Q0 through Q4 = 0. Q4 through Q11 map to D0 to D7. i.e., Q7 = D3. By knowing which test FAlLs and the bit pattern one may easily determine the problem bit(s) (look for the bit column in the failed tests that are the same).

If 2 or 3 tests fail, then there is a bus problem of some sort, and the busses must be examined. If all four tests FAIL, then the problem can be in several locations.

1. LDCOUNT might not be strobing the data into U220 and/or U211 (Display Counters, schematic diagram 17).
2. Flip-fiop U414A may not be resetting, or OR-gate U323 pin 3 might be HI due to a failure.
3. The busses into or out of Address Multiplexers U221, U212, U210 may not be operating properly.
4. Readout Buffer U140 may be defective.

Troubleshooting Procedure:
Set up the $\mathbf{2 4 3 0}$ test scope as in Step 1 of the 2110 troubleshooting procedure.
Now using the CH 2 probe:

1. Run test 2340 and verify the LDCOUNT strobe pulse at pin 11 of U222, U220, and U211.
2. Verify that after LDCOUNT strobe, that the outputs of Address Multiplexers U222, U220, U211 are stable and of the correct level for the test selected.

Table 6-6 (cont)
3. Verify that U323 pin 3 is LO.
4. Verify the outputs of U221, U212, and U210 are stable and correct after the LDCOUNT strobe to the previous bus.

5a. Verify the $\overline{\mathrm{RO}}$ chip enable to U 140 pin 1 is HI for about half of the Trigger strobe positive period, and then that it goes LO and stays LO for the remaining time. This LO selects inputs Q6 through Q9 of U140.

5b. Verify the COUNTEN chip enable to U140 pin 19 has a HI-to-LO transition; then, before the time that U140 pin 1 goes LO, U140 pin 19 goes HI. While U140 pin 19 is LO, inputs Q6, Q7, Q8 are selected. If ok to here, replace U140.

Readout Buffer U240 (diagram 16):
Testing Method:
If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2351 to 2354.

This test requires the display state machine to be operative. There is no "good" way to insure that it is functional, and there have been no previous tests to help find that out. Therefore, if this test fails, it could be for several reasons other than U240.

Initialization:
DISCON $=01100000$. Significant bits are b2, b5, b6, and b7 (STOPDIS, enable "Q" bus, not ENV mode).

MODECON $=00010000$. Significant bit is b3 (U240).
MISC $=00100000$. Significant bit is b5 (ZAXIS OFF).
The test result $=$ PASS.
The test is to load a pattern into the display counters, U220 and U211, with the LDCOUNT strobe. The counter outputs are switched to the Q bus through U221, U212, U210 by holding U414A in the reset mode (PRESTART + DISPLAY is LO). The inputs to U240 are the bits Q0 through Q5 where Q0 through Q3 $=0$. Q4 and Q5 are the b0, b1 data of pattern. To read back properly, one shifts the pattern left 6 bits and uses bits 6 and 7 of XDIAG (U243); the test result is set to FAIL if the test fails.

Test 1. 10100101 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 2. 01001011 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 3. 10010110 is loaded and read back via U243. Test result is set to fail if not a match on bits 0 through 5.

Test 4. 00101101 is loaded and read back via U243. Test result is set to FAIL if not a match on bits 0 through 5.

## NOTE

Q0 through Q3 = 0, and Q4 through Q11 map to D0 to D7. i.e., $Q 7=$ D3. By knowing which test FAlLs and the bit pattern, one may easily determine the problem bit(s) (look for the bit column in the failed tests that are the same).

If 2 or 3 tests fail, then there is a bus problem of some sort that must be examined. If all four tests FAIL, then the problem can be in several locations.

1. $\overline{\text { LDCOUNT }}$ might not be strobing the data into U220 and/or U211.
2. Flip-flop U414A may not be resetting, or U323 pin 3 might be HI due to a failure.
3. Address Multiplexers U221, U212, and U210 may not be operating properly.
4. Readout Buffer U240 may be defective.

## Troubleshooting Procedure:

Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.
Now using the CH 2 probe:

1. Run test 2350 in CONTINUOUS mode and verify the LDCOUNT strobe pulse at pin 11 of U222, U220, and U211.
2. Verify that after LDCOUNT strobe, the outputs of Address Multiplexers U222, U220, U211 are stable and of the correct level for the test selected.
3. Verify that U323A pin 3 is LO.
4. Verify the outputs of U221, U212, and U210 are stable and correct after the LDCOUNT strobe to the previous bus.
5. Verify the $\overline{\mathrm{RO}}$ chip enable to U 240 pins 1 and 15 is LO. If ok to here, replace U 240 .

## Vertical Buffer U322 (diagram 16):

U322

## Testing Method:

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2361 to 2364. The contents of the first four bytes of U322 have been written and will now be tested against the values that were thought to be written, any failure to match will cause that test to fail. U322 is decoded by reading address 2000 h .

Set test result $=$ PASS.
If contents of 2000h not equal to 10100101, then test result $=$ FAIL.
If contents of 2001h not equal to 01001011, then test result $=$ FAIL.
If contents of 2002 h not equal to 10010110 , then test result $=$ FAIL.
If contents of 2003h not equal to 00101101, then test result $=$ FAIL.

## Troubleshooting Procedure:

Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.
Using the CH 2 probe:

1. Run test 2360 in CONTINUOUS mode and check U322 pin 19 for a negative strobe $\overline{\text { YSEL }}$ at $10 \mu \mathrm{~s}$ from the LO-to-HI transition of the trigger pulse. If not present, troubleshoot U323 and the inputs to it.
2. Check for activity on the $\overline{W R D}$ signal line of U322 (pin 1); if no activity, check for open back to A12U564 (schematic diagram 2).
3. Check that the data pattern for the test is correct at the input and output pins of U322. The data is stable during the YSEL strobe on pin 19, and the data bit level must be read in coincidence with it as other activity is also taking place on the WD bus. A Word Recognizer probe would be useful to make these checks, but it is not necessary.
4. If the input and output data patterns of U322 do not match, replace U322. If they match each other, but are not correct, suspect a problem with Vertical RAM U431. Run test 2361 through test 2364 to see if all patterns fail. If all do not fail, troubleshoot for a bad bit of the failing test or tests.
5. Check pin $20(\overline{\mathrm{DEY})}$ and pin $18 \overline{(\mathrm{CSY})}$ of U 431 for a negative strobe coincident with the $\overline{\text { YSEL }}$ strobe. If either is not present, troubleshoot U421 and the input signals to it.
6. Check that pin 21 of $\mathrm{U} 431(\overline{\mathrm{WE})}$ is HI during the HI portion of the trigger strobe (displayed on CH 1 of the test scope). The data writes of the test patterns occur during the LO portion of the trigger strobe, and that activity can be seen. If the WE signal is not correct, troubleshoot U422 and the input signals to it.
7. Replace U431.

## 2370

Horizontal Buffer (diagram 16):

## Testing Method:

If run from this level, all four tests are selected in turn, or one may execute any one test by selecting 2371 to 2374. The contents of the first four bytes of U314 have been written and will now be tested against the values that were thought to be written, any failure to match will cause that test to fail. U314 is decoded by reading address 2800 h .

Set test result $=$ PASS.
If contents of 2800h not equal to 10100101 , then test result $=$ FAIL.
If contents of 2801 h not equal to 01001011 , then test result $=$ FAIL.
If contents of 2802 h not equal to 10010110 , then test result $=$ FAIL.
If contents of 2803h not equal to 00101101, then test result $=$ FAIL.

Troubleshooting Procedure:
Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.

Table 6-6 (cont)

Using the CH 2 probe:

1. Run test 2370 in CONTINUOUS mode and check U314 pin 19 for a negative strobe $\overline{\text { XSEL }}$ at $10 \mu \mathrm{~s}$ from the LO-to-HI transition of the trigger pulse. If not present, troubleshoot U323 and the inputs to it.
2. Check for activity on the $\overline{W R D}$ signal line of U314 (pin 1); if no activity, check for open back to A12U564 (schematic diagram 2).
3. Check that the data pattern for the test is correct at the input and output pins of U314. The data is stable during the XSEL strobe on pin 19, and the data bit level must be read in coincidence with it, as other activity is also taking place on the WD bus.
4. If the input and output data patterns of U314 do not match, replace U314. If they match each other, but are not correct, suspect a problem with Horizontal RAM U431. Run test 2371 through test 2374 to see if all patterns fail. If all do not fail, troubleshoot for a bad bit of the failing test or tests. A Word Recognizer probe would be useful for making these checks but is not necessary.
5. Check pin $20 \overline{(D E X)}$ and pin 18 (CSX) of $U 440$ for a negative strobe coincident with the $\overline{X S E L}$ strobe. If either is not present, troubleshoot U421 and the input signals to it.
6. Check that pin 21 of U 440 (WE) is HI during the HI portion of the trigger strobe (displayed on CH 1 of the test scope). The data writes of the test patterns occur during the LO portion of the trigger strobe, and that activity can be seen. If the WE signal is not correct, troubleshoot U422 and the input signals to it.
7. Replace U440.

2400 TB-DSP

Running the test at this level will execute the Time Base Controller (U670) tests for Short-Pipe (SISO) and FISO modes.

The test causes Time Base Controller U670 to simulate all the necessary states to get an acquisition in Short-Pipe and FISO modes.

## 2410 <br> U670 FISO

Time Base Controller A11U670 (schematic diagram 8):
Running the test executes the Time Base Controller in FISO mode.
Troubleshooting Procedure:
Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.

Now using the CH 2 probe:

1. Run test 2410 in the CONTINUOUS mode. Set the Sec/Div setting of the test scope to $1 \mu \mathrm{~s}$ and connect the CH 2 probe to pin 19 of bidirectional buffer U641 (TBSEL); save CH 2 into REF1 and Display REF1.
2. Position CH 2 down to allow room and connect the CH 2 probe to U641 pin 1; save CH 2 into REF2 and Display REF2. The LO TBSEL pulse should be coincident to a HI $\overline{\mathrm{RD}}$ pulse; if not, then troubleshoot the TBSEL or the RD signal line.

Table 6-6 (cont)
3. Position CH 2 down to aliow room to display the signal and probe $\mathbf{U} 641$ pin 11 through 18 . While the REF1 signal TBSEL is LO and REF2 signal $\overline{\mathrm{RD}}$ is HI , compare the results to 01100101 where U641 pin 11 is D7 and U641 pin 18 is D0. If they do not compare, replace U641.
4. Test the output of U 670 pin 26 for a square wave with a period of about $200 \mu \mathrm{~s}$. If not correct, replace U670.
5. If present, test for the square wave at U680 pin 16; replace U680 if TIMER signal is missing.
6. If all checks were ok, suspect A12U542 (schematic diagram 2).

Time Base Controller A11U670 (schematic diagram 8):
Troubleshooting Procedure:
Set up the test scope as in Step 1 of the 2110 troubleshooting procedure and run test 2420 in the CONTINUOUS mode on the scope under test.

Now using the CH 2 probe:

1. Position the trigger strobe ( CH 1 ) near the top of the cr and connect the CH 2 probe to pin 19, TBSEL, of U641. Adjust the Sec/Div setting of the test scope to $1 \mu \mathrm{~s}$. Verify that there is a negative TBSEL pulse during the positive trigger strobe. Save the CH 2 waveform in REF1 and display REF1.
2. Position the CH 2 display down to allow room and connect the CH 2 probe to $U 641$ pin 1. Save CH 2 into REF2 and display REF2. The TBSEL pulse should be coincident to a HI RD pulse; if not, then troubleshoot the chip select or $\overline{\mathrm{RD}}$ signal line.
3. Position the CH 2 display down to allow room and probe $U 641$ pin 11 through 18 while REF1 signal is LO and REF2 signal is HI. Compare the results to 01000000 where U641 pin 11 is D7 and U641 pin 18 is D0. If they do not compare, replace U641.
4. Test the output of U670 at pin 26 for a square wave signal (TIMER) with a period of about 200 $\mu \mathrm{s}$; if not present, replace U670.
5. If present, test for the square wave at U680 pin 16 and replace U 680 if missing.
6. If all checks were ok, suspect A12U542 (schematic diagram 2).

The MAIN board has five shift-register tests. These are in two groups. The first group includes Gate Array U270, Peak-Detector U530, Attenuators U511 and U221 (acting as one 16-bit register), Trig U140. The second group has the System-DAC U850 and U851 (acting as one 16-bit register).

From this level, the initialization and all five tests are selected in turn. An individual test may be run by selecting test numbers 2510 to 2560.

There is one diagnostic bit for readout off the main board and that is the logic-AND of the MSB of all the shift registers. The shift registers are preset to 10100101 , or 1010010110100101 and the diagnostic bit is tested to see if a " 1 " is being read out for the MSB. If the diagnostic bit is not $=\mathbf{1}$, then either one of the registers is not loading or the diagnostic bit is stuck. In any event, no further meaningful data is possible, so the test stops. If initialization is successful, each bit is shiffed out, register by register, and compared against what it should be by shifting the initial pattern and comparing the MSB. After any register is tested, it is reinitialized so the next register may be tested. Discon (input $=$ U531 pin 18 , output $=U 531$ pin 17) is the diagnostic bit from the main board.

## Table 6-6 (cont)

| 2510 INIT | Acquisition Control Shift Registers A10U270 (Gate Array), A10U530 (Peak Detector), A10U140 (Trig <br> Control), DAC Input Shift Register A10U850/U851 (schematic diagram 5), and Attenuator Shift Regis- <br> ter A10U221/U511 (schematic diagram 9): |
| :--- | :--- |
|  | Testing Method: |
|  | For this test to pass, the MSB of the five output registers above must be high. If one of the registers <br> didn't have the correct pattern strobed in, the test fails. |

Troubleshooting Procedure:
Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.
Run test 2510 in CONTINUOUS mode.

Using the CH 2 probe:

1. Check A10U380 pin 3 (schematic diagram 5) for a HI level during the HI period of the trigger strobe. If ok, then check for the same signal at A11U531 pin 18 (schematic diagram 17). If correct and test is failing, replace U531 and run SELF DIAG.
2. Check U 380 pins 1 and 2. If both are HI during the trigger strobe HI and pin 3 does not follow, then replace U380. If neither pin 1 nor 2 is HI , then suspect DAC Select Multiplexer U272 or its input gating.
3. If $\mathbf{U} 380$ pin 2 is LO, then run test 2560 and troubleshoot using the procedure given for that number.
4. If U380A pin 1 is LO, then find which cathode of the input diodes (CR185, CR186, CR286, or CR287) is LO. Run the test number for the suspected Shift Register and check the inputs (clocks, data, and power) to it (look at the information given with the test number for the troubleshooting procedure for each Shift Register). If they are all ok, replace the suspected Shift Register; if not, troubleshoot the bad input.

## 2520

ATTEN

Attenuator Shift Registers A10U221/A10U511 (schematic diagram 9):
Testing Method:
For this test, the MSB of A10U511 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails.

## Troubleshooting Procedure:

Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.
NOTE
For the following, set the Trigger Position of the test 2430A to 3/4. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.

Run test 2520 in CONTINUOUS mode. Using the CH 2 probe:

1. Check U511 pin 9 and U 221 pin 9 for +5 V (registers not held reset). If not +5 V , then repair.
2. Check Shift Register U221 at pin 8 for activity (ATT SR CLOCK line). If clock is missing, troubleshoot Control Register Clock Decoder A10U271 (diagram 5).

Table 6-6 (cont)
3. Check U221 pins 1 and 2 for activity (ACD line is the data input). If ACD missing, troubleshoot the signal path to and gating on the inputs of DAC Multiplexer Select register U272 (diagram 5).
4. Check U221 pin 13 for activity; replace U221 if inactive.
5. If checks good to this point and the test still fails, replace U511.

```
2530
Acquisition Control Register A10U530 (schematic diagram 5):
```

PEAK
DETECTOR

```
Testing Method:
For this test, the MSB of A10U530 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails.
```


## Troubleshooting Procedure:

Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.

## NOTE

For the following, set the Trigger Position of the test scope to $3 / 4$. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.

Run test 2530 in CONTINUOUS mode. Using the CH 2 probe:

1. Check U 530 pin 9 for a HI level. If LO, then check R531 and source of +5 V .
2. Check U530 pin 8 for activity (PD SR CLK signal line); if inactive, repair.
3. Check $\mathbf{U} 530$ pins 1 and 2 for activity (ACD line is the data input). Repair if inactive.
4. If all inputs are good, replace U530.

## 2540

GATE ARRAY

Acquisition Control Register A10U270 (schematic diagram 5):

## Testing Method:

For this test, the MSB of U270 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails.

## Troubleshooting Procedure:

Set up the test scope as in Step 1 of the 2100 troubleshooting procedure.

## NOTE

For the following, set the Trigger Position of the test 2430A to 3/4. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.

Run test 2540 in CONTINUOUS mode. Using the CH 2 probe:

1. Check U270 pin 9 for a HI level. If not +5 V , check R269 and source of the +5 V .
2. Check U270 pin 8 for activity (GA SR CLK signal line); if inactive, repair.
3. Check U270 pins 1 and 2 for activity (ACD line is the data input). Repair if inactive.
4. If all inputs are good, replace U270.
```
2550 Acquisition Control Register A10U140 (schematic diagram 5):
TRIG
```


## Testing Method:

```
For this test, the MSB of A10U140 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails.
```

Troubleshooting Procedure:
Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.

## NOTE

For the following, set the Trigger Position of the test 2440 to $3 / 4$. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.

Run test 2550 in CONTINUOUS mode. Using the CH 2 probe:

1. Check U140 pin 9 for a HI level ( $\overline{\mathrm{RESET}})$. If LO, repair.
2. Check $\mathbf{U 1 4 0}$ pin 8 for activity (TRIG CONT CLK line). If inactive, repair.
3. Check U140 pins $\mathbf{1}$ and $\mathbf{2}$ for activity (ACD line is the data input); repair if inactive.
4. If all inputs are good, replace U140.

## 2560

SYSTEM DAC

DAC Input Shift Registers A10U850/A10U851 (schematic diagram 5):

## Testing Method:

For this test, the MSB of A10U851 (pin 13) will be compared with what the MSB should be with each shift of the register. If one of the bits differs from the loaded-in pattern, the test fails.

Troubleshooting Procedure:
Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.
NOTE
For the following, set the Trigger Position of the test 2440 to 3/4. If using an analog scope for testing, use the appropriate holdoff and trigger level to view the signals of interest.

Run test 2560 in the CONTINUOUS mode. Using the CH 2 probe:

1. Check U850 pin 9 and U851 pin 9 for HI level. If not +5 V , check R850 and source of the +5 V .
2. Check U850 pin 8 and U851 pin 8 for clock activity. If clocks are inactive, then:
a. Check U280B pin 5 to have a LO gate present; replace U272 if pin 5 is stuck either HI or LO.
b. Check U280B pin 6 for clocking signals during the HI period of the trigger strobe.
c. Replace U280 if not gating correctly; troubleshoot clock signals if not present.
3. Check the data input to 4850 at pins 1 and 2. The signal should be a train of pulses during the HI period of the trigger strobe. If the data input signal is not present, test signals around U280D and correct.

## Table 6-6 (cont)

4. Check U850 pin 13 that the first 8 -bits of the 16 -bit pattern comes out as the second is shifted into U850 at pins 1 and 2 . (A Sec/Div setting of 0.5 ms on the test scope is good for viewing the data pattern, and the latched data on pin 13 is much easier to view than the input data pulses). If the data is not shifting through U850, then replace U850.
5. If the data is coming through U850, check U851 pins 1 and 2 to verify that it is ok there. Check pin 13 of U851 for a data pattern of 1010010110100101. (Each bit is approximately 0.2 ms wide, so a 0.4 ms wide pulse is two bits.)
6. Replace U851 if not shifting the signal through.

Holdoff Register A11U762 (schematic diagram 13):
Testing Method:
From this level, all four tests are selected in turn. Individual test may be called by selecting test numbers 2610 to 2640 . The test involves writing 4 unique patterns to U762 and reading them back from U761. The four patterns test for all stuck-at(s) and for lines shorted to other lines. By knowing which test FAILs and the bit pattern, one may easily determine a bus problem by observing which bits are the same in the failed tests.

The HOREG register is two integrated circuits; U762 is a latch and the read back is U761. If all tests pass, the test result is set to PASS; any failure sets it to FAIL.

## NOTE

Bit 3 of the test patterns is not allowed to be set LO as it would reset the GPIB chip and we cannot restart it from the diagnostic routines.

Test 1. 10101101 is sent to U 762 and read back via U761. Test result is set to FAIL if not a match.
Test 2. 01001011 is sent to U762 and read back via U761. Test result is set to FAIL if not a match.
Test 3. 10011110 is sent to U762 and read back via U761. Test result is set to FAIL if not a match.
Test 4. 00101101 is sent to U762 and read back via U761. Test result is set to FAIL if not a match.

## Troubleshooting Procedure:

If the failure occurs for all tests:
Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.
Now using CH2 probe:

1. Check that U762 pin $1 \overline{\text { HOREG }}$ is LO about $12 \mu \mathrm{~s}$ after the trigger strobe. If $\overline{\text { HOREG }}$ is absent, test the inputs of U781. Replace U781 if the inputs are ok; if not ok, troubleshoot that problem.
2. Check that U762 pin 9 ( $\overline{\mathrm{WR}}$ clock) has a LO-to-HI transition during the enable time. (Save enable in REF1 and display it while looking at the clock.) Clock line is the write line; if missing, suspect open run or connection.
3. Check the outputs U762 (pins 15, 12, 10, 7, and 5) for the proper levels for the pattern that is being looped on. Replace U762 if incorrect.
4. Check U761 pin 1 to be enabled after the clock to $\mathbf{U 7 6 2}$ pin 9 . If present, then the problem is possibly U762.

All RAM tests are non-destructive. The Display RAM is tested first, and, if found good, the contents of the other RAMs are stored in the Display RAM as they are tested. The contents are returned after the test is complete.
From this level (3000), all eight RAM tests are selected in turn. An individual RAM test may be run by selecting test levels 3100 to 3800 .

## NOTE

An internal jumper, A13J156, must be removed before test levels 3700 and 3800 may be run. If the jumper is removed and test levels 3700 and 3800 are run, loss of power during while they are running can result in loss of internal calibration constants. In that event, a partial recalibration is required (see information regarding power loss while running SELF CAL under "Diagnostics" in this section). Run these tests only if necessary.

```
3100 A11U431 3500 A11U600
3200 A11U440 3600 A12U440
3300 A12U350 3700 A12U664
3400 A11U430 3800 A12U664
```

Each RAM test (levels 3100-3800) is comprised of the four following subparts:
A logic one is shifted left through a field of logic zeros while incrementing the address (the " - " TRIGGER SLOPE LED is lit).

A logic one is shifted right through a field of logic zeros while decrementing the address (the " + " TRIGGER SLOPE LED is lit).

A logic zero is shifted left through a field of logic ones while incrementing address (the " - " TRIGGER SLOPE LED is lit).

A logic zero is shifted right through a field of zeroes while decrementing the address (the " + " TRIGGER SLOPE LED is lit).

Running level 3000 causes all four parts of the test to be performed on all 8 RAMs (sublevels 3100-3800), while running an individual sublevel test causes the four-part test to be performed on the corresponding RAM device.

Running a sublevel test from $3 \times 10$ to $3 \times 40$ (where $\times=1-8$ ) runs the part (out of four parts) indicated by the test label (for instance, "3340 1-0S" runs the test that shifts logic 0 left in a field of logic ones for an incrementing address on U350).

RAM A11U431 (schematic diagram 16):

## Troubleshooting Procedure:

If test = FAIL then look for failure and correct using the following steps:

## Using the CH 1 probe:

1. Run test 3110 in CONTINUOUS mode and check for activity on the chip select line to U431 ( $\overline{\mathrm{CSY}}$, pin 18). If active, trigger the test scope on the signal. If no chip select, work backwards and find problem.

## Using the CH 2 probe:

2. Check for activity on the write enable line to U431 ( $\overline{W E}$, pin 21) and note that it is LO at the same time as the chip select line. If no signal present, work backwards and find the problem.
3. Check for activity on the output enable line to U431 ( $\overline{\mathrm{DEY}}, \mathrm{pin} 20$ ). If none, work backwards and find the problem.
4. Check the data I/O pins of U431 (pins $9,10,11,13,14,15,16$, and 17) for activity when test 3100 is selected. If no activity when $\overline{\mathrm{DEY}}$ (output enable) is LO (pin stuck HI or LO), then suspect U322; otherwise suspect U431.

Table 6-6 (cont)

RAM A11U440 (schematic diagram 16):
Troubleshooting Procedure:
If test $=$ FAIL then look for failure and correct using the following steps:
Run test 3210 in CONTINUOUS mode.
Using the CH 1 probe:

1. Check for activity on the chip select line $U 440(\overline{\mathrm{CSX}}$, pin 18 , and trigger the scope on the CH 1 signal. If none, work backwards and find problem.

Using the CH 2 probe:
2. Check for activity on the write enable line $U 440$ pin 21, and note that it is LO at the same time as the chip select line. If none, work backwards and find the problem.
3. Check for activity on the output enable line $\mathbf{U 4 4 0}$ pin 20. If none, work backwards and find the problem.
4. Check the data I/O pins U440 (pin 9, 10, 11, 13, 14, 15, 16, and 17) for activity when test 3210 is selected. If no activity (stuck HI or LO) when output enable is LO, then suspect U314; otherwise suspect U440.

RAM A12U350 (schematic diagram 2):

Troubleshooting Procedure:
If test $=$ FAIL then look for failure and correct, using the following steps:
Select test 3310 and RUN CONTINUOUSLY.

## Using the CH 1 probe:

1. Check for activity on the pin 20 chip select line to U350, and trigger the scope on the signal if active. If no chip select, work backwards through the chip select circuitry and find problem.
2. Check for activity on the write enable line to U350 ( $\overline{\mathrm{WRR}}, \mathrm{pin} 27$ ) and note that it is LO at the same time as the chip select line. If no activity, work backwards and find the problem.
3. Check for activity on the output enable line to U350 ( $\overline{\mathrm{WRD}}, \mathrm{pin} 22$ ). If no activity, work backwards and find the problem.
4. Check the data I/O pins U350 (pins $9,10,11,13,14,15,16$, and 17) for activity when test 3400 is selected. If no activity (stuck HI or LO) when output enable is LO, then suspect buffer U352; otherwise suspect U350.

RAM A11U430 (schematic diagram 16):
Troubleshooting Procedure:

Run test 3410 in CONTINUOUS mode.
Using CH 1 probe: if not, repair.

Using the CH 2 probe: suspect U423A or U422B.
3. If the checks in Steps $\mathbf{1}$ and $\mathbf{2}$ are ok, replace $\mathbf{U 4 3 0}$.

ACQUIRE RAM A11U600 (schematic diagram 8):

If test $=$ FAIL then look for failure and correct using the following steps:

1. Check the write enable to U 430 ( $\overline{\mathrm{WRA}}$, pin 8) for activity and trigger on the signal if active. If no activity, troubleshoot OR-gate U422A and U422C and their input signals. Check that pin 10 is LO;
2. Check for activity at the data input to $U 430$ ( DI , pin 11) timed with the enable pulse. If no signal,

Troubleshooting Procedure:
If test = FAIL then look for failure and correct, using the following steps:
Run test 3510 in CONTINUOUS mode.

1. Check for LO on chip select line U600 pin 18. Repair if not LO.
2. Check for activity on the write enable line to U 600 ( $\overline{\mathrm{WE}}$, pin 21). If no activity, work backwards and find the problem.
3. Check for activity on the output enable line to $U 600(\overline{O E}$, pin 20$)$. If no activity, work backwards and find the problem.
4. Check the data $/ / O$ pins of U600 (pins $9,10,11,13,14,15,16$, and 17) for activity when test 3500 is selected. If no activity (stuck HI or LO) when the output enable is LO, then suspect buffer U610; otherwise suspect U600.
5. Check the address lines (MAO-MAA) for activity. If no activity on any lines, troubleshoot the WE and TB2MEM signals to U300, U400, and U410. If an address line is stuck, troubleshoot that problem.

3600
A12U440

CMD/TMP RAM A12U440 (schematic diagram 2):
NOTE
If tests 3300 through 3600 all fail, the most likely faults are: a stuck data line to A12U352, a bad select signal to A12U352, or Waveform Data Buffer A12U352 itseff.

Table 6-6 (cont)

Troubleshooting Procedure:
If test = FAIL then look for failure and correct, using the following steps:
Run test 3610 in the CONTINUOUS mode.

Using the CH 1 probe:

1. Check for activity on the chip select line to A12U440 (pin 20), and trigger the scope on the signal if active. If no activity, work backwards through U250C and find the problem.

Using the CH 2 probe:
2. Check the data $I / O$ pins of $U 440$ (pins $11,12,13,15,16,17,18$, and 19 ) for activity. If no activity when output enable is LO, then suspect U440; otherwise check U352.

3700 or $3800 \quad$ A12U664 (schematic diagram 2)

## NOTE

The test of RAM device A12U644 is divided into two test levels, 3700 and 3800. The sections of U644 that may be accessed depends on the condition of the BUSREQ output of A12U860. With BUSREQ set HI, the $8 K \times 8$ memory space corresponding to addresses 7000 H to 8 FFFH is the only space available; with BUSREQ set LO, the $24 \mathrm{~K} \times 8$ memory space corresponding to addresses 0000 H to 5FFFH are both available. Level 3700 tests the 7000 H to $8 F F F H$ block while level 3800 tests the 0000H-5FFF block resulting in the entire $32 K \times 8$ RAM being tested. The Troubleshooting Procedure that follows applies to both test levels.

Troubleshooting Procedure:

## NOTE

If the System Ram data bus, chip selects, or output enable lines are defective, the System $\mu P$ cannot run the the diagnostics testing. Therefore, if test $3700 / 3800$ fails, the most likely problem is U664. If the diagnostics tests do not run, the Kernel test will have to be used to isolate a system bus or address decoding problem. An NV RAM failure due to stored data being scrambled requires a "COLD START" to reload the NV RAM with correct nominal values. The COLD START should be followed by a SELF CAL and then an EXTENDED CAL of ATTEN, TRIGGERS, and REPET to return it to a completely calibrated state.

If test $=$ FAIL, look for failure and correct using the following steps:
Run test 3710 or 3810 in CONTINUOUS mode.

Using the CH 1 probe:
Check for a LO on pin 20 . If it is HI , check back to the source of the problem starting with Q960.
Check for a HI on chip select 2 (pin 26). If not HI , check back to the source of the problem start with U424A.

Table 6-6 (cont)

Using the CH 2 probe:
Check for activity on the write enable line pin 27.
Check for activity on the output enable line pin 22.
Check the data $\mathrm{I} / \mathrm{O}$ pins (pins $11,12,11,15,16,17,18,18$ ) for activity.
Check the data I/O pins (pins 11, 12, 13, 14, 15, 16, 17, 18,) of U660 for activity. If not active, check its write enable and output enable lines (pins 1, 19).

## 4000

Front Panel $\mu$ P A13U700 (schematic diagram 3):

## FPP

## Testing Method:

The Front Panel Processor test first sets all test results to NULL. Any failure to complete all the tests will result in a locked front panel. Depending on the nature of the failure, the Trigger LEDS may be latched in the first number of the test level that failed, the failure code may be flashed out on the LEDs (if it is the first failed test), or it may make it through the diagnostic, but with the FPP test marked FAIL. That information will help to isolate which circuitry may be defective and gives the starting point in troubleshooting a failure. It will be necessary to turn off the scope and turn it back on again to repeat the diagnostic testing from the front panel; however, testing may be done using GPIB diagnostic test commands.

The Front Panel $\mu \mathrm{P}$ internal diagnostics require that the $\mu \mathrm{P}$ be reset. Therefore, the structure of the FPP tests is such that the processor is initialized when completed. This requires that ALL of the tests be run in order. Therefore, all tests will be run even though it appears that only a sub-test is being executed.

Test Steps:
4100 U861 pin 9 should be reset to its LO state via U862B and U862A.
4200 U861 pin 6 should be reset to its HI state via U862C and U862D.
4300 U861 pin 9 (WR TO HOST) should clock pin 9 HI.
4400 U700 (Front Panel $\mu$ P) checks its internal RAM, ROM, Timer, and A/D. Any failure will set the test result to FAIL.

4500 U861 pin 6 (FPDNRD) should clock pin 6 LO.
4600 U742 and U751. Four bit patterns are written to the FPP and echoed back. If these are not returned properly, the test result = FAIL.

Troubleshooting Procedure:
Failure of one of the Front-Panel $\mu \mathrm{P}$ tests may be indicated only by flashing out the failed test number on the Trigger LEDs, but if the diagnostic testing can continue past the failure, the Extended Diagnostic menu will be seen with the FPP test marked FAIL. The usual result of a Front Panel $\mu \mathrm{P}$ failure is a locked up front panel (the button and pots will not be functional). To rerun the diagnostic testing from the front panel to check the Trigger LEDs for the failed test number, it is necessary to turn off then turn back on the scope.

Troubleshooting Front-Panel $\mu \mathrm{P}$ A13U700:

1. Check pin 5 for the 4 MHz clock.
2. Check pin 4 for +5 V , pin 1 for ground.
3. Check pins $8,14,16,17,19,31$, and 32 for +5 V and pins 6,7 , and 20 for ground.
4. Perform the Front Panel $\mu \mathrm{P}$ test if all the checks in steps 1,2 , and 3 were ok. If not, troubleshoot any problem area found by the checks.

## Front Panel $\mu \mathrm{P}$ Test:

1. Turn off power and short pins 1 and 2 of $J 155$ together. (The pins must remain shorted together during power-on.) This places the Front-Panel $\mu \mathrm{P}$ in the continuous self-diagnostic mode (Test 4400). Connect a test scope to view the signal present on pin 14 of U700.
2. Turn the power back on and observe the signal at pin 14. See test waveform illustration of Figure 6-9 for correct waveshape and timing.


Figure 6-9. Front Panel $\mu \mathrm{P}$ diagnostics test.
3. If the test waveform is not present and the supply voltage, the ground, and the clock are correct, change the Front-Panel $\mu \mathrm{P}$; it is possibly defective.

If the Front-Panel $\mu \mathrm{P}$ checks out ok, turn off the power and remove the jumper connected for the preceding Front Panel diagnostic test. Turn the scope back on and perform the following circuit checks for any of the Front Panel tests that failed when running the Extended Diagnostics via the GPIB. Use the circuit checks to isolate the problem in the associated circuitry. IF THE FPP DIAGNOSTICS TEST FAILED, THE ONLY WAY TO RUN THESE TESTS WILL BE VIA GPIB, AS THE FRONT PANEL WILL NOT RESPOND TO BUTTON PRESSES. To gain access to the scope via the GPIB when the EXT DIAG menu is being displayed, a MENU OFF command must be sent to exit extended diagnostics.

Table 6-6 (cont)

NOTE
Since the Front Panel $\mu P$ is being reset in this test, there is no way to HALT if one chooses a CONTINUOUS loop mode and runs the tests from the front panel. However, to allow access to these features for any possible troubleshooting, looping has not been disabled. ONCE A TEST IS INVOKED IN CONTINUOUS MODE, A POWER OFFION CYCLE MUST BE USED TO EXIT FROM THE FRONT PANEL. Via the GPIB, the tests may be started and halted by sending the appropriate commands.

Set up the test scope as in Step 1 of the 2110 troubleshooting procedure.
Run tests 4100 through 4600 in CONTINUOUS mode. Use the CH 2 probe for the following checks while the specific test is selected and running.

4100 A13U861 pin 9 (FPINT):

1. Check U 862 pin 1 for $0.2 \mu \mathrm{~s}$ negative strobe during the HI period of the trigger strobe. If not present, replace U862.
2. Check U861 pin 9 for a HI-to-LO transition. If not occurring, replace U861.

## 4200 A13U861 pin 6 ( $\overline{\text { FPDNRD }}):$

1. Check U861 pin 1 for a negative strobe during the HI period of the trigger strobe. If not present, replace U862.
2. Check U861 pin 6 for a LO-to-HI transition from the strobe at U861 pin 1. If occurring, replace U861.

4300 A13U700 pin 12 (WR TO HOST):

1. Check that U861 pin 9 has a HI pulse. If not, select $50 \mathrm{~ms} / \mathrm{div}$ and ENVELOPE acquisition mode on the test scope; then, run test 4000 for the scope under test. At pin 12 of U700, check for a strobe occurring near the falling edge of the trigger strobe. If the strobe is ok, replace U861. If missing, test for 4 MHz at U 700 pin 5 and replace U 700 if the 4 MHz clock is ok.

If the 4 MHz clock is missing, troubleshoot the clock source. Restore the prior test scope setup as for test 2110 (a good use for the AUTOSTEP SEQUENCER).

## 4400 DIAG BYTE A13U700:

1. Check that the enable pulse to U751 (pins 1 and 19) is present and save to REF1. If not present, check for an open between U862A pin 1 and U751 pins 1 and 19.
2. Display REF1 and probe U751 pin 18, 16, 14, and 12. These should all be LO during the time U751 is enabled. If not LO, it indicates either a problem in U700 or an invalid DC voltage level at one of the U700 inputs. If one of these four diagnostic bits is HI and the supply pins, etc., are ok, replace U700.

4500 A13U700 pin 13 (FPDNRD):

1. Select the $1 / 2$ TRIG POSITION and set the Sec/Div setting to 1 ms on the test scope. Check for the FPDNRD clock pulse to U861 at pin 3 (leads the trigger strobe rising edge about $120 \mu \mathrm{~s}$ ). If missing, replace U700.

Table 6-6
2440 Troubleshooting Procedures (cont)
2. Check for LO at U861 pin 6; replace U861 if pin 6 is HI .
3. Check A12U654 pin 13 for LO. Replace A12U654 if pin 13 is LO and test is failing.

4600 A13U742/A13U751:

1. Check for a pattern of 10100101 at U742 pin 19, 16, 15, 12, 9, 6, 5, and 2 at the rising edge of the trigger strobe (Word Recognizer Probe is useful for this check). If not, and U742 pin 11 is LO, then replace U742. If U742 pin 11 is HI, replace U700.
2. Check the enable pulse at U751 pins 1 and 19. Save and move to REF1.
3. Display REF1 and check for a 10100101 pattern coincident with the enable pulse at $U 751$ pins $17,15,13,11,8,6,4$, and 2 . If not ok, replace U700.
4. Display REF1 and check for a 10100101 pattern coincident with the enable pulse at U751 pins $3,6,7,9,12,14,16$, and 18. If not ok, replace U751.

Battery A12BT800 (NVRAM keep-alive battery) (schematic diagram 1):
Testing Method:
There is no hardware exercised for this test. The operating system is informed by the front panel processor if the battery voltage is either high or low. The "test" is to read a memory location where the System $\mu$ P has stored the status after checking with the FPP. If the status is unknown, the result is NULL. If the test "passes," it means that it is not defective in that direction.

Troubleshooting Procedure:
4710 HIGH:

1. Measure the drop across A12R900, for a voltage in the range, 2.4 V to 3.7 V . If the battery voltage is in range, proceed to step 2, otherwise proceed to step 3.
2. Check the voltage at A 13 U 700 , pin 21 , in the range of 2.4 V to 3.7 V . If the voltage is correct, replace A 13 U 700 . If the voltage is not correct, backtrack and check the voltage follower, A12U940A. If A12U940A is ok, proceed to step 3, otherwise replace A12U940A and retest.
3. If the above steps do not fix the overvoltage condition, then check the $+\mathbf{5 V D}$ supply in the range of 4.75 V to 5.25 V .

## 4720 LOW:

There is a sub-menu, defining three battery tests:

```
4720 /FPP/BATT-STATUS/LOW
```

4721 BT800
4722 U664BT
4723 U360BT
Only U664BT and U350BT are actually used. If either NVRAM modules, A12U664 or A12U350 internal battery voltage is too low, a data write is prevented and a FAIL is placed on the NVRAM module, 4722 U664BT and/or 4723 U350BT. Should a FAIL occur for 4721 BT800, then the voltage detection circuitry (A12U940A, A13U700, A12R900, A12R801) is defective.

## 4721 BT800:

Measure the voltage at the junction of A12R900 and A12R801. The voltage should be in the range, 2.4 V to 3.7 V . If the voltage is low, check the resistors, A12R900 and A12R801, and the +5 VD supply. If the voltage measured is correct, then check voltage for range at A12U940A, and at A13U700, pin 21.

Table 6-6
2440 Troubleshooting Procedures (cont)

|  | 4722 U644BT: <br> Check A12U664 pin 28 (VCC) for a voltage in the range 4.75 V to 5.25 V (5\% power supply accura- <br> cy). If voltage is below, problem is in the low-voltage power supply. Otherwise, if the voltage is <br> correct, then replace A12U664. <br> 4723 U350BT: <br> Check A12U350 pin 28 (Vcc) for a voltage in the range 4.75 V to 5.25 V (5\% power supply accura- <br> cy). If voltage is below, problem is in the low-voltage power supply. Otherwise, if the voltage is <br> correct, then replace A12U350. |
| :--- | :--- |
| 5000 WP U470 | Waveform $\mu \mathrm{P}$ A12U470 (schematic diagram 2): <br> Testing Method: |
| The nature of these tests is such that all tests must be executed in order and may not be individually <br> executed. Therefore, any attempt to execute one test will result in all tests being executed. <br> The Waveform Processor test first sets all test results to NULL. Any failures will be fatal in terms of |  |
| instrument operation; however, the last test that was executed will be set FAlL and should help in |  |
| diagnosing the cause of the problem. |  |
| The Waveform $\mu P$ command memory has been checked out by this time as well as the bus struc- |  |
| ture that permits the System $\mu \mathrm{P}$ to control the Waveform $\mu \mathrm{P}$ bus. |  |

## Testing Method:

The version number in the header is preset to "?" and is filled in by this test. If the test fails, the "?" will remain in the header for further indication of an error. A Waveform $\mu \mathrm{P}$ reset causes the Waveform $\mu \mathrm{P}$ to read the version number bytes of the Waveform $\mu \mathrm{P}$ code. If the version number is incorrect, the Waveform $\mu \mathrm{P}$ code is incompatible with the System $\mu \mathrm{P}$ code and may not execute properly.

## Troubleshooting Procedure:

If test 5300 fails, replace Waveform $\mu \mathrm{P}$ ROMs U480 and/or U490 with the correct ones for the version of System $\mu \mathrm{P}$ code being used.

## 6000 <br> CK SUM-NVRAM

Nonvolatile RAM Checksum A12U664 (schematic diagram 1):
Testing Method:
Some of the CRCCs (check sums) are computed at power-down and will be valid only at power-up. Therefore, executing tests 5000 through 5003 will only display the flags that resulted from power-up diagnostics.

## note

FAIL and PASS flags in the Extended Diagnostics menu show the results of the last test ran. If a defective device that has previously caused a FAIL flag to be set is replaced, the test must be run again to obtain a PASS indication in the menu.

When the instrument is SELF CALIBRATED, a CRCC is calculated and stored for the Calibration Constants in NV RAM.

When power-down is executed, the values of the front-panel variables have a CRCC calculated and stored.

When a waveform is saved, the CRCC is calculated for the waveform and headers and saved.
On power-up, all of these are recalculated and compared to the stored CRCC word. If they do not agree, that test fails.

## 6100 Calibration Constants: <br> CONSTANTS

If FAIL, the calibration constants have been lost and a COLD START is executed. The instrument must be recalibrated to return to calibrated operation after a COLD START.

A failure of 6100 is serious to the normal operation of the scope, and the cause of the failure should be found and corrected to prevent reoccurrence.

1. Check BT800 and the components that connect and disconnect the battery from the NV RAM at power-off and power-on respectively.

## WARNING

If replacing the lithium battery, avoid personal injury by observing proper methods for handling and disposal. Improper handling may cause fire, explosion, or severe burns. Don't attempt to recharge and don't crush, disassemble, heat the battery above $212^{\circ} \mathrm{F}\left(100^{\circ} \mathrm{C}\right)$, incinerate, or expose contents of the battery to water. Dispose of battery in accordance with local, state, and national regulations.
2. Test several times by cycling the power after the instrument has completed its self testing. If the test continues to fail, check the PWRUP line to $\mathbf{U 6 4 0}$ pin 2, and ensure that it is reset LO when the power line voltage drops below the minimum line voltage. If this line does not go LO soon enough, the power-down routines will not calculate the current check sums before the power is completely lost.

## 6200

## FP-LAST

Front Panel Control Settings:
Troubleshooting Procedure:

If the last front-panel setup has been lost, the instrument will be set up in the INIT PANEL configuration in the AutoStep Sequence menu (push PRGM).

If this event is due to a component failure, the RAM test, 3700 and/or 3800 , or BATT-STATUS test 4700 should also have failed. Check NVRAM device U664 and associated circuitry or the Battery circuit as appropriate.

The reference waveform memories will be declared EMPTY if the WFM-HEADERS do not check correctly. These waveforms are stored in A12U350. Therefore, if the problem is due to failed components, the RAM test (3300) or BATT-STATUS (4700) should have failed.

## 6400

## PRGM

State of the AutoStep Sequencer memory:
Testing Method:

Each time an AutoStep Sequence is modified, a CRCC (check sum) is calculated and stored. At power-up, a CRCC is calculated again and compared with the last value stored. If there is a discrepancy, the FAIL flag is set and all the pointers for the AutoStep Sequences are initialized so that the sequences are lost.

The most likely cause of a PRGM failure is a loss of power while memory is being reclaimed after a sequence has been deleted. If, rather, this event is due to a component failure, the RAM test, 3700 and/or 3800, or BATT-STATUS test 4700 should also have failed. Check NVRAM device U664 and associated circuitry or the Battery circuit as appropriate.

Table 6-6 (cont)

Testing Method:
These tests, if passed, indicate that the hardware is functional.
IF A SELF DIAG OR EXTENDED DIAG TEST FAILS, ONE CANNOT ASSUME THE HARDWARE IS DEFECTIVE UNLESS THE SAME TEST FAILS A SELF CAL. The reason that SELF CAL must be run to assure a hardware failure is that SELF CAL computes new values of the constants for each test and uses them in the subsequent tests; whereas, diagnostic tests use previously stored constants for making the tests. If those stored values are not valid for the present operating temperature of the scope, the test may not be able to converge to a solution.

The CCD has two classes of adjustments, centering and gain. In addition, several CCD parameters are measured and stored for use in Dynamic Calibration. Centering must be performed in all four acquisition modes because of offset differences in the different paths. Gain is performed in Short-Pipeline and FISO modes.

Troubleshooting Procedure:

The CCDs are a good suspect if any of the 7000 -series diagnostic tests failed. The Extended Diagnostics menu should be examined to determine if the problem is in only one or in both of the channels.

If both channels fail:

1. Check the CCD clocks. To determine if a clock problem is internal or external to the CCD/Clock Driver hybrid, compare the collector voltages of Q450 and Q460 to Waveform illustration 67 (associated with schematic diagram 10). If either of the clock waveforms is different, check the base of the associated transistor(s). If the base voltage is switching correctly, change the defective transistor. If not switching, trace back to the clock source from U470, the Phase Clock Array (on diagram 11), and check there. If the clocks are not correct there, change U470.
2. If the clocks are running correctly at the collectors of Q450 and Q460, check to see if pins 2, 3, 5 , and 6 of R470 are switching correctly (compare pins 2, 3, 4, and 5 to waveforms 68 through 71 on diagram 10). If not switching correctly, check the outputs of U470 for correct clock. If not present there, troubleshoot the Phase Clock Array (U470); if ok there, find the open.

If a single channel fails:

1. Change the associated CCD/Clock Driver U450 or U350. If the problem is not corrected, troubleshoot the CCD Output circuitry.

NOTE
If any CCD or Peak Detector is changed, do not run a SELF CAL until the CCD OUTPUT Gain has been set using the EXT CAL ADJUSTS, test pattern number 6. Adjust the $\pm 2$ division gain for the changed channel both Side 1 and Side 2 according to the directions given in the display.

## NOTE

Steps 1-6 troubleshoot only that section of the CCD OUTPUT (schematic diagram 14) that processes the plus/minus signal pair (CCDO11+/CCDOD11-) that is output by side 1 of the CH 1 CCD . The references to components and signals in these steps only apply to that channel and side. See schematic diagram 14 to determine the corresponding components for troubleshooting the sections processing the remaining signal pairs for CH 1 CCD side 1 (CCDOD12+/CCDOD12-, CCDOD13+/CCDOD13-, and CCDOD14+/CCDOD14-), and those for the CH 2 CCD side 2 (CCDOD21+/CCDOD21-, CCDOD22+/CCDOD22-, CCDOD23+/CCDOD23-, and CDOD24+/CCDOD24-).

1. Input the 2440 calibrator signal to the channel that is not operating properly. If neither is working, start with CH 1. (CH 1, side 1 components are referenced; see NOTE above.) Set the bad channel to $100 \mathrm{mV} / \mathrm{div}$, DC coupled, with $50 \Omega$ termination off. Adjust the screen waveform so the ground dot on the scope under test is 2 divisions below center screen if possible. Set the input coupling of the other channel to ground. Turn the A SEC/DIV to $5 \mu \mathrm{~s}$.
2. Verify that pin 3 (CCDOD11+) of A30 (Gain Cell Board) looks similar to waveform 104 (on schematic diagram 14), with center screen being at +5 V . If this waveform does not appear, troubleshoot the CCD/Clock Drivers. Verify that pin 2 (CCDOD11-) of A30 resembles waveform 105. Again, if this waveform does not appear, go to the CCD/Clock Driver troubleshooting.
3. Examine pin 18 of A30. The waveform here should have an offset of +7.5 V , which is shown at center screen on waveform 106 for diagram 14. If this waveform does not look right, check the components on A30 for failures.
4. Compare pin 1 of A30 to waveform 107. If this waveform does not appear, check to see that pin 3 of U560 is switching between 0 and +15 V ; if it is, then the switch (U560) is bad. If it is not switching, check to see if the base of Q660 (Q670) is switching between 0.5 V and 0 V ; if it is, the transistor is bad. If it is not switching, trace OSAM1 back to the Time Base board.
5. Observe the waveform at pin 1 of U770. It should be similar to waveform 110 , except that an offiset of up to $\pm 1.3 \mathrm{~V}$ may appear. If this is not the case, check the $+10 \mathrm{~V}_{\mathrm{RA}}$ supply and the centering voltage ( $7.5 \mathrm{~V} \pm 1.3 \mathrm{~V}$ ). If the voltages are correct, check U 770 and its associated transistors and other components for failure.
6. Check the collector of Q773. It should look like waveform 109, where center screen corresponds to ground; if not, check that the base of Q773 is switching on and off. If base is switching but the collector is not, check the transistor for a collector-to-emitter short. If it is not switching on the base, trace the MS11 signal back to the Time Base board. The timing relationships of the $\overline{O S A M}$ and the $\overline{M S}$ signals are shown in waveform 45 through 51 of the System Clocks schematic (diagram 7).

Table 6-6 (cont)

7300 EFFICIENCY

CCD/CLOCK DRIVERS A10U350 and A10U450 (schematic diagram 10):
Testing Method:
This test measures the transfer efficiency of the CCD by comparing the gain of columns 2 and 16 of the CCD B register arrays. To do this, a $\pm 4$ division input is applied to the Peak Detector calibration inputs and acquired. Efficiency loss and apparent offset for the gain are both calculated and stored for use in dynamic data correction. Efficiency loss of more than $6 \%$ will cause an error to be fiagged. Testing is performed at two SEC/DIV settings ( $2 \mu \mathrm{~s}$ and 500 ns ) on all four CCD channels.

Troubleshooting Procedure:
If all other tests are ok, the most probable cause of failure is a defective CCD; replace the failed CCD.

## 7400

PEAK DETECTORS A10U340 (CH 2) and A10U440 (CH 1) (schematic diagram 10):
PD-OFFSET

## Testing Method:

This test is to check the match of the offsets of the two paths through the peak detectors. A 0 V cal signal input (DAC value $=2048$ ) is acquired and the $A$ and $B$ peak detector and $D$ and $C$ peak detector pairs (see Figure $3-5$ in Section 3 of this manual) are matched by iteratively adjusting the appropriate PDOS (peak-detector offset) DACs and remeasuring the difference until offsets are matched. If matching cannot be accomplished within 1/2 DL for calibration or 1 DL for diagnostics, the test terminates due to acquisition count, and the test result is set to FAIL; otherwise, it passes.

The SPECIAL menu choices under Extended Functions provide a diagnostic switch to divide the signal acquisition path. CAL PATH ON:OFF turns on or off the calibration signal path to the Peak Detectors. It is a useful diagnostics device in the event that large offset errors have driven the display off-screen. Switching CAL PATH ON eliminates the Attenuators and Preamplifiers from the input signal path and places the calibration reference level on the display. If that brings the display back on screen, then the offset problem may be isolated to the Attenuators or Preamplifiers; if not, then the problem may be in the Peak Detectors or CCDs. With CAL PATH ON, the FORCE DAC test may be used to check the operation of the Peak Detectors and CCDs using the CURS (CAL) adjustment.

## Troubleshooting Procedure:

1. Do a COLD START and use the FORCE DAC test to determine if the DAC system can control the PD-OFFSET voltages (PD11, PD13, PD21, and PD23) correctly. If not, troubleshoot the DAC system.
2. If the DAC system is functioning normally, the most probable cause of a failure is a faulty Peak Detector. Replace the Peak Detector of the failing channel

## NOTE

If any CCD or Peak Detector is changed, do not run a SELF CAL until the CCD OUTPUT Gain has been set using the EXT CAL ADJUSTS, test pattern number 6. Adjust the $\pm 2$ division gain for the changed channel, Side 1 and Side 2, according to the directions given in the display.

Table 6-6 (cont)

Preamplifiers A10U320 (CH 2) and A10U420 (CH 1) (schematic diagram 9):
Testing Method:
The PA tests, if passed, indicate that the analog acquisition circuitry is functional.
IF A SELF DIAG OR EXTENDED DIAG TEST FAILS, ONE CANNOT ASSUME THE HARDWARE IS DEFECTIVE UNLESS THE SAME TEST FAILS A SELF CAL. The reason that SELF CAL must be run to assure a hardware failure is that SELF CAL computes new values of the constants for each test and uses them in the subsequent tests; whereas, diagnostic tests use previously stored constants for making the tests. If those stored values are not valid for the present operating temperature of the scope, the test may not be able to converge to a solution.

The Preamplifier has constants for Position Offset, Position Gain, Balance, Normal and Invert Gain, and Max Variable Gain. There is some interaction between adjustments. This effect is addressed by always using the previously stored constants in any setup and executing SELF CAL twice from a COLD START to assure an iterative solution of the calibration constants.

## Troubleshooting Procedure:

1. If SELF CAL fails, the calibration constants will most likely not be close enough to an operationally good value for the portions of the Preamp that work to function properly. Do a COLD START to replace the stored calibration constants with nominal values.

NOTE
After a COLD START, the scope will need partial recalibration after it is repaired to return it to correct adjustment.
2. If the 8000 level is flagged FAIL, there will be failure at one or more of the lower level tests. This is the case because one failure that misbiases the Preamp can cause several SELF CAL tests to fail.
3. After doing a COLD START, use the FORCE DAC test to determine if the DAC system can control the Preamp DAC voltages correctly for the tests that are flagged FAIL. Troubleshoot the DAC system for those DAC outputs showing no or improper control.
4. Check that the Preamp is responding to the DAC control voltage being changed. These are respectively for CH 1 and CH 2 :

1POS and 2POS to pin 17 for position input.
CH1G and CH2G to pin 18 for gain control.
CH 1 B and CH 2 B to pin 2 for balance.

Table 6-6 (cont)

The check is set up by first doing a COLD START (to again set the calibration constants to known values), and then applying a 4-division signal to the CH 1 and CH 2 vertical inputs (or to the bad channel if only one is bad). Observe the signal on the crt, if possible; otherwise, use a test scope to probe the vertical signal path to check for correct response. Since the Preamp outputs are not accessible, use the output of the Peak Detectors to verify the signal through the Preamp. The side 3 Peak Detector output for CH 1 may be checked on R441 and R540; and for the CH 2 side 3 output, check at R244 and R341.

Use either the Front Panel Controls or the Force DAC test to check the VARIABLE GAIN and VERTICAL POSITION. Balance may be varied only using the Force DAC function. Varying the channel balance should appear as a dc offset change to the vertical signal level. Prior to making any adjustments after a COLD START (either with the Front Panel controls or the Force DAC function), the signal at the output of the Peak Detectors should have a +8.7 V dc level with an ac signal (replica of the input signal) of approximately 0.5 V peak-to-peak.
5. The Preamplifier operating mode is set by a serial data word sent from the System $\mu \mathrm{P}$. The CD input, pin 22, is the serial data input. A TTL-level logic swing should be present on this line whenever the Attenuators, Preamps, or A/B Trigger Generator operating modes are being set up. If there are no FAIL flags under these major test categories, the CD circuitry is most likely functioning properly. The $\overline{C C}$ input, pin 23, is the control clock input, and it should have a TTL-level logic swing on it only when the particular hybrid, in this case the Preamp hybrid, is being set up. Check that this line is high initially and pulses LO eight times for each Preamp load cycle. (The eight pulses may be separated into several groups of pulses.)
6. The Preamps have bypassed and decoupled voltage supplies. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual.
7. If the Preamp hybrid itself is suspected of being defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact.

Table 6-6 (cont)

## 8100

 POSITION OFFSETAcquisition System Position Offset:
Testing Method:
Position Offset is calculated at 50 mV per division only. Position offset must be performed for all four acquisition modes to compensate for the common-mode offsets in the CCD arrays that are not corrected by CCD centering. After the hardware is set up and the CCD constants set for the particular mode of operation, the Preamplifier is balanced by executing the balance routine, but only changing the DAC settings-not the cal constants. This assures an accurate position measurement.

The Position Offset is then calculated by acquiring a ground level signal and comparing the Acquisition Memory value to what a ground acquisition should be (center screen is 00 h ). If the value is not within $1 / 2 \mathrm{DL}$ for calibration or 1 DL for diagnostics, the position DAC outputs (CH1-PA-POS and/or CH2-PA-POS) are adjusted to compensate. When the acquisition is within limits, the test result is set to PASS. If the position offset cannot be adjusted to within specification, the acquisition count for an abort is taken, and the test result is set to FAIL.

Troubleshooting Procedure (refer to test $\mathbf{8 0 0 0}$ for more information):

1. Check that the decoupling network, R420/C423 or R222/C222 is functional.
2. Use the FORCE DAC test to determine if the CH1-PA-POS and/or CH2-PA-POS voltages are being controlled by the DAC System. If not, troubleshoot the DAC System.
3. Use the SPECIAL menu choice of CAL PATH ON to determine whether the offset error is prior to the Peak Detectors or after. Troubleshoot in the appropriate direction to locate the source of the offset error.
4. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual.
5. If the Preamp hybrid itself is suspected of being defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact.
6. Swap Peak Detector hybrids between channels to see if the problem channel reverses. If so, replace the faulty Peak Detector.

Preamplifier Position Gain A10U420 and A10U320 (schematic diagram 9):
Testing Method:

Position Gain is calculated at 50 mV per division only, using the stored Position Offset calibration constant. The DAC counts corresponding to +4 divisions of Position Offset are added to the Position Offset constant and an acquisition is made. After storing the results, a corresponding -4 division acquisition is made, and the two values of acquisition memory are checked for eight divisions of change in the calibration limits. The Position Gain constant is then calculated as a result of the data taken and stored as a Position Gain calibration constant. A Position Gain constant more than 20\% different from the nominally expected value will cause the test to fail.

NOTE
POSITION GAIN is not an iterative calibration as the gain is directly calculated.

## Table 6-6 (cont)

Troubleshooting Procedure (refer to test 8000 for more information):

1. Check that the decoupling network, R420/C423 or R222/C222 is functional.
2. Use the FORCE DAC test to determine if the CH1-PA-POS and/or $\mathrm{CH} 2-\mathrm{PA}-\mathrm{POS}$ voltages are being controlled by the DAC System. If not, troubleshoot the DAC System.
3. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual.
4. If the Preamp hybrid itself is suspected to be defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact.
5. Swap Peak Detector hybrids between channels to see if the problem channel reverses. If so, replace the faulty Peak Detector.

Preamplifier Balance A10U420 and A10U320 (schematic diagram 9):

## Testing Method:

Balance is performed in all five Preamplifier ranges, and on both channels simultaneously. Balance is calculated by first taking a ground acquisition in non-invert. Then an acquisition is made in INVERT, and a new balance DAC voltage is calculated that will keep the trace shift between non-invert and INVERT within limits for calibration or diagnostics. This is done until balance is within specification or until the maximum number of acquisitions has been reached. If the result is within specification prior to acquisition abort, the test result is set to PASS; otherwise, it is set to FAIL.

Balance Test Limits:

| Range | 50 mV | 20 mV | 10 mV | 5 mV | 2 mV |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Cal limit | $1 / 2 \mathrm{DL}$ | $1 / 2 \mathrm{DL}$ | 1 DL | 1 DL | 2 DL |
| Diag limit | 1 DL | 1 DL | 2 DL | 2 DL | 4 DL |

Troubleshooting Procedure (refer to test 8000 for more information):

1. Check that the biasing network associated with the balance input, pin 2, and pins 4, 20, and 25 is functional and that the voltage levels are approximately those indicated on the schematic diagram in the service manual.
2. Use the FORCE DAC test to determine if the CH1-BAL and/or CH2-BAL voltages are being controlled by the DAC System. If not, troubleshoot the DAC System.
3. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual.
4. If the Preamp hybrid itself is suspected of being defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact.
5. Swap Peak Detector hybrids between channels to see if the problem channel reverses. If so, replace the faulty Peak Detector.

Table 6-6 (cont)


#### Abstract

$8400 \quad$ Testing Method: PREAMP GAIN and 8500 PREAMP INVERT GAIN During calibration, gain constants are computed by using the Balance control to position +2.5 and -2.5 divisions and computing the next gain DAC value until the result is set to be within specifications. For diagnostics, the swing is reduced to $\pm 1.5$ divisions to allow for thermal drifts that occur due to temperature changes between power off and power on. The effects of thermal drift are especially noticeable at high vertical sensitivities. Limits are 1 DL for calibration and 2 DL for diagnostics. Gain is done for all five Preamplifier ranges in both normal and invert modes. Both Preamplifier channels are tested simultaneously. Since the transfer function of the gain control is non-linear, correction is done iteratively either until the gain is within specifications or until the maximum number of acquisitions allowed for the test has been reached. If the result is found prior to a test abort, the test result is set to PASS; otherwise, it is set to FAIL.


Troubleshooting Procedure (refer to test $\mathbf{8 0 0 0}$ for more information):

1. COLD START and use the Force DAC test to check that the DAC system is controlling the CH1-GAIN-CAL and CH2-GAIN-CAL voltages correctly. If not ok, troubleshoot the DAC system.
2. Check that the bypassing components in series with the power supplies are not open. Also check that the dc bias voltages at the Preamp are approximately the levels indicated on the schematic diagram in the service manual.
3. If the Preamp hybrid itself is suspected of being defective and the other channel is fully functional, swap Preamp hybrids between channels to see if the problem moves to the other channel. If so, replace the defective Preamp. If not, check the hybrid mount connections of the defective channel for corrosion or contamination that may be causing a poor contact.
4. Swap Peak Detector hybrids between channels to see if the problem channel reverses. If so, replace the faulty Peak Detector.

## 8600

PREAMP
VAR MAX

## Testing Method:

In this test, the change in Preamplifier control which will yield an attenuation of 2.75 from the Calibrated VOLTS/DIV setting is measured on both channels at 50 mV per division in normal mode. This is done by re-performing the 50 mV noninverted gain test seeking a value of +2.5 divided by +2.75 $(+0.91)$ division and -2.5 divided by $-2.75(-0.91)$ division on the output. The difference between the resulting gain control DAC setting and the gain control DAC calibration constant is the Var Max value. Inability to achieve an attenuation factor of $\mathbf{2 . 7 5}$ is a test failure.

Troubleshooting Procedure (refer to test $\mathbf{8 0 0 0}$ for more information):
See the Troubleshooting Procedure for tests 8400 and 8500.

Table 6-6 (cont)

## ATTENUATORS

Channel 1 and Channel 2 Attenuators AT400 and AT300 (schematic diagram 9):

## Testing Method:

THIS TEST IS ONLY PERFORMED USING EXTENDED CALIBRATION. With the Preamplifier set to 50 mV non-inverted, the Preamplifier gain test is repeated interactively using standard dc test voltages applied to the CH 1 and CH 2 inputs. By adjusting the Preamplifier balance to give -2 divisions, the output is swung between -2 (input grounded), and +2 (input set to 0.2 V per div), divisions. The gain control DAC is adjusted to achieve an output within specifications. The difference between the resulting control DAC setting and the gain calibration constant measured at 50 mV per division (non-inverted) is the attenuator gain constant. If a solution cannot be found, or if the resulting solution is more than a $2 \%$ gain error, the test result is set to FAIL. If the test fails, an attenuator gain of 0 (nominal) is stored for the calibration constant under the assumption that the test setup may be in error. The test is repeated for all three vertical attenuators ( $1 \mathrm{X}, 10 \mathrm{X}$, and 100 X ) using input test voltages of 0.2 Vdc , 2 Vdc , and 20 Vdc.

## Troubleshooting Procedure:

1. Check that the correct test voltages are used for the ATTEN calibration step.
2. Check that one audible click is heard when changing the VOLTS/DIV setting between 50 mV and 100 mV (10X attenuation) and between 500 mV and 1 V (100X attenuation). Also check that one audible click is heard when changing the Vertical input coupling between DC and AC, and when turning the fifty ohm input ON and OFF. Several clicks will normally be heard when switching in and out of GND Coupling.
3. If one and only one audible click was heard for each of the first four front-panel changes above, then the circuitry that drives the four mag-latch relays in each attenuator is functioning properly by switching the individual relays to the opposite latched position (the audible click).
4. Connect the output of a Standard Amplitude Calibrator to the vertical input of the failing channel using coaxial cable with no terminator. Set the Standard Amplitude Generator output and the VOLTS/DIV setting on the scope to the values given in the following table and check the signal path between the Attenuator and the Preamplifier input of the failed channel. With a 10X probe on the test scope, view the signal at the Preamp input pin. Use NOISE REJ Trigger Coupling and $20-\mathrm{MHz}$ Bandwidth on the test scope to clear up the trace noise and obtain a stable trigger. If only one channel is bad, the other channel of the scope may be used to view the signal. The signal amplitude out of the Attenuator and into the Preamp should be approximately 50 mV peak-to-peak for each attenuator setting in the three ranges. A possible, but unlikely, source of a failure that is not in the signal path between the Attenuator and the Preamp is a shorted capacitor (C414 or C311) connecting to the Attenuator.

ATTENUATOR CHECK

| Signal In | VOLTS/DIV | Signal Out |
| :---: | :---: | :---: |
| 50 mV | 2 mV to 50 mV | 50 mV |
| 0.5 V | 100 mV to 500 mV | 50 mV |
| 5 V | 1 V to 5 V | 50 mV |

5. If one channel shows PASS flags on all the ATTEN tests, swap the Preamps between channels to determine if the Preamplifier inputs are ok. If that swaps the problem, replace the faulty Preamp. If the problem remains in the same channel, replace the defective Attenuator.

## Table 6-6 (cont)

6. If none or only some audible clicks were heard, and assuming the Attenuator Register and Preamplifier tests passed the Power-on SELF TEST or a subsequent EXTENDED DIAGNOSTIC test, troubleshoot the magnetic-latch buffers (U510 and U220) and the latching circuitry (Q620, Q621, U520, and associated components) on diagram 9.
7. Check the ATTEN CLK line for the presence of a signal at the times when an audible click should be heard.
8. Shift Registers U221 and U511 are assumed functional with proper input signals if there is a PASS flag present at the 2520 level of the Extended Diagnostics menu after performing the EXT DIAG diagnostics test. Otherwise, troubleshoot the Shift Registers for the source of failure.

## 9000 <br> TRIGGERS

A/B Trigger Generator A10U150 (schematic diagram 11):
Testing Method:
The Triggers tests, if passed, indicate that the analog trigger circuitry is functional.
If a SELF DIAG OR EXTENDED DIAG TEST FAILS, ONE CANNOT ASSUME THE HARDWARE IS DEFECTIVE UNLESS THE SAME TEST FAILS A SELF CAL. The reason that SELF CAL must be run to assure a hardware failure is that SELF CAL computes new values of the constants for each test and uses them in the subsequent tests. Whereas, diagnostic tests use previously stored constants for making the tests. If those stored values are not valid for the present operating temperature of the scope, the test may not be able to converge to a solution.

Triggers have constants for offset and gain. The value of Level DAC output that caused the trigger to change state is assumed to be the upper hysteresis level in plus slope and the lower hysteresis level in negative slope.

NOTE
TRIGGER MODE is set to $A$ and $B$ to program ATG output to be the AND of A and B triggers. Thus ATG may be tested as an indication that triggering has occurred. This requires that BOTH A AND B TRIGGERS MUST BE FUNCTIONAL TO GET EITHER TEST RESULT TO PASS.

## Troubleshooting Procedure:

External and Internal Trigger Path (common circuitry):

1. For this test to result in a PASS flag, several major circuit blocks must work correctly.

Common to both the external trigger signal path and the internal trigger signal path is A/B Trigger Generator A10U150 (schematic diagram 11) with the following related input signals:
a. ATHO (A Trigger Holdoff) from the Trigger Holdoff circuit (schematic diagram 13) to A/B Trigger Generator U150 through a level shitting resistor string of R225 and R134. The level at U150 pin 15 is less than +3.3 V for logic LO and greater than +4.0 V for logic HI . The input must be logic HI for a trigger output to occur. If the ATHO signal is not correct, see the "HOLDOFF PROBLEMS" in Procedure 4.
b. A TRIG LEVEL and B TRIG LEVEL from the DAC System (schematic diagram 6) via A10U640A (A TRIG LEVEL) and A10U640D (B TRIG LEVEL) and filter networks R250-C250 or R162-C160 is another. These voltage levels should be adjustable from -1.3 V to +1.3 V using the FORCE DAC function.

## Table 6-6 (cont)

c. ACD (Acquisition Control Data), A TRIG CLOCK, and B TRIG CLOCK are the signals that load the internal shift register of U150 with MODE, CPLG, and SLOPE requirements for the trigger signal. These lines should have TTL level voltage swings, and the A TRIG CLOCK clock and B TRIG CLOCK signal lines should only have transitions when the associated A or B Trigger MODE, CPLG, or SLOPE are changed. The ACD data line (U150 pin 46) should be checked for the presence of voltage transitions.
d. Six $\overline{\text { SR }}$ data lines set up the A TRIG SOURCE and B TRIG SOURCE selections. Shift Register A10U140 (schematic diagram 5) provides these signals, and it is tested by test 2510 of the Extended Diagnostics. The signals are assumed correct for a PASS flag at that diagnostic level. If a FAIL flag is present, follow the Troubleshooting Procedure under that diagnostic level.
2. High speed ECL level shift stages, Q250 and Q251 for MAIN GATE and Q150 and Q151 for DELAY GATE, are common paths for both Internal and External trigger sources. These stages should have an ECL input swing of less than +3.4 V for logic LO and greater than +4.0 V for logic HI. The output swing should be greater than -1.6 V for logic LO and less than -1.1 V for logic HI.
3. Trigger Logic Array A10U370 is also common to both the external and internal trigger signal paths. Related signal inputs that must be correct are:
a. EPTHO (End Pretrigger Holdoff) from Timebase Controller A11U670 (schematic diagram 8) via buffer U680E on the Timebase board. EPTHO must be TTL high for a trigger to occur. If that is not occurring, see the Timebase and System Clocks troubleshooting chart in the Diagrams pages at the back of this manual.
b. $\overline{W R}, \overline{A C Q S E L}, A 0-A 3$, and GAD0-GAD7 are the digital control and data lines. These signals are tested by test number 2510 of the Extended Diagnostics and, if a PASS flag is present, are assumed to be correct. Otherwise refer to that diagnostics troubleshooting procedure for a failure of 2510.
4. The ATG path from Trigger Logic Array U370 to data bus bit DO is also a common path. The AND logic function of the A Trigger Gate and the B Trigger Gate is performed within Trigger Logic Array U370. The path from A/B Trigger Gate inputs, through a logic ANDing gate, to the Trigger Logic Array Output (pin 63, ATG) is asynchronous and direct, delayed only by the propagation delay of the internal logic gate structures. The ATG signal has a TTL voltage level swing. The ATG output signal path is through R368 and W110 to buffer U851C (schematic diagram 13) and then through tristate buffer U761 to the DO bit of the System $\mu \mathrm{P}$ data bus. This path through buffer U761 is not tested by test 2000 (Register Tests) of Extended Diagnostics, so it must be verified from U370 through U761 to be operational. ATG also clocks Trigger Holdoff flip-flop U872A.

## EXTERNAL TRIGGER PATH—EXCLUSIVE:

5. EXTERNAL TRIGGER PREAMP A10U100 (schematic diagram 9) is only in the External Trigger Signal path. It should be verified to be functional if FAIL flags appear only at Extended Diagnostics levels with EXT labels.
a. There are only two mode control bits that set up U100. These bits are assumed to be correct if level 2510 of Extended Diagnostics shows a PASS flag. These two bits set up the 1X or 5X attenuation for each EXT TRIG channel.
b. Q110, U120, and associated circuitry produce $\mathrm{a}+5 \mathrm{~V}$ source that tracks the instrument -5 V source. The voltage level at U100 pins 17 and 44 should be verified to be +5 V . The decoupled -5 V power supply voltage at pin 7 of U 100 must be present for this circuit and for the circuit of U100 to function properly.
c. The voltage at U100 pins 25 and 36 should be verified to be +5 V to test for defective decoupling components (L210/C211 and L120/C112).

## INTERNAL TRIGGER PATH—EXCLUSIVE:

6. CH 1 and CH 2 PREAMPS U420 and U320, U230A, U230B, and associated components (schematic diagram 9) supply the Internal CH 1 TRIG and CH 2 TRIG signals, and should be verified for functionality if FAIL flags appear only on Extended Diagnostics levels with CH 1 or CH 2 labels.
a. Operational Amplifiers U230B and U230A and associated components form common-mode level-trimming amplifiers for the CH 1 and CH $2 \pm$ PICK outputs respectively. Since the CH 1 and CH 2 trigger signals originate from the -PICK outputs of the CH 1/CH 2 PREAMPs (U420 and U320), improper operation of these bias-trimming amplifiers will result in a diagnostic FAIL flag. When operating properly, the arithmetic average of the +PICK and -PICK bias voltages should be at or very near 0 V . If this is not the case, the amplifier circuitry needs to be repaired. (Note that the two circuits interact with each other.)
b. If a channel PREAMP is suspected of having a defective -PICK output and the other channel shows no Diagnostics FAIL flags, swap PREAMPs to see if the problem moves to the other channel. If it does, replace the defective PREAMP.

9100
TRIGGER
OFFSET

Trigger Signal Offset:
Testing Method:
A ground signal is provided to the trigger from the CH 1 or CH 2 pickoff (internal triggers) or from an external source (EXT1, EXT2 external triggers). This is done by grounding the attenuator or by providing a short at the EXT TRIG inputs.

The trigger level DAC is moved in two binary searches to determine where the upper and lower hysteresis levels are while holding the "other" trigger level in such a state that should be "triggered." The constant is then set to the hysteresis level that represents the triggering point for the desired slope at zero input. The test is repeated for both A and B triggers for all input paths. For EXT TRIG inputs, levels are measured for both the $1 X$ and 5 X (attenuated by a factor of five) amplifier ranges. An additional offset for the trigger slope is obtained by measuring the trigger in minus ( - ) slope with a CH 1 input and computing the difference between the obtained value and that measured in plus ( + ) slope.

## Troubleshooting Procedure:

1. Run test 9100 in CONTINUOUS mode.
2. Starting with the signal path for ATG at pin 2 of A13U761 (schematic diagram 13), work backwards toward the trigger signal source using a test oscilloscope to check that the proper signals are present with the proper bias levels and voltage swings.
3. Use the troubleshooting comments under 9000 level as a guide.
4. ATG signal should be present at TTL level voltage swings.
5. MAIN and DELAY GATE signals to Trigger Logic Array A10U370 (schematic diagram 11) should be present at ECL voltage level swings.
6. A TRIG LEVEL and B TRIG LEVEL signals, at pins 13 and 37 of A10U150 respectively, should have several levels: $\pm 1 \mathrm{~V}$ swings, $\pm 0.5 \mathrm{~V}$ swings, and voltage swing levels that approach a final level of gain iteratively as the binary search is done.

Table 6-6 (cont)
7. CH 1 and CH2 TRIGGER signals should be at or near $O$ V. (LR421/LR220 can be open and not cause a FAIL flag to appear at this diagnostic test level since this test only requires $\mathrm{CH} 1 / \mathrm{CH} 2$ trigger signal to be near 0 V , which is the case with these components open. However, a FAIL flag will appear at the 9200 diagnostic level.)
8. EXT1 and EXT2 TRIG signals are provided externally, and the external signal paths to the Trigger Source Select function within A/B Trigger Generator U150 are not tested by running test 9200 CONTINUOUS Mode. If FAIL flags only appear at EXT diagnostic levels, the EXT source inputs of U150 are most likely functional, and the problem is either External Trigger Preamp U100 and related bias circuitry, or the BNC and R1001/R1003 signal path from the front panel.

## 9200 <br> trigger gain

## Trigger Signal Gain:

## Testing Method:

Trigger gain is measured for both $A$ and $B$ triggers and for CH 1 and CH 2 inputs. Trigger gain is set by positioning the input signal to +2 divisions using the CH 1 and CH 2 Preamplifier balance control. The trigger level is then determined by binary search using the same routine which is used for trigger offset. The same is done for -2 divisions. These results are then used to compute the trigger gain.

Trigger Gain for the External Triggers is done in Extended Calibration of the TRIGGER circuits. A ground signal and externally supplied dc voltages are used to get a four-division level swing in both Ext Trig Preamp gain ranges. If gain cannot be measured, an error is flagged. On the External Triggers, a nominal gain value is stored if the test fails, on the assumption that the external setup may be faulty. The test(s) that failed will be marked FAIL in the Extended Diagnostic menu.

## Troubleshooting Procedure:

1. Run test 9200 in CONTINUOUS mode.
2. Starting with the signal path for ATG at pin 2 of A13U761 (schematic diagram 13), work backwards toward the trigger signal source using a test oscilloscope to check that the proper signals are present with the proper bias levels and voltage swings.
3. Use the troubleshooting comments under 9000 level as a guide.
4. The ATG signal should be present at TTL level voltage swings.
5. MAIN and DELAY GATE signals to Trigger Logic Array A10U370 (schematic diagram 11) should be present at ECL voltage level swings.
6. A TRIG LEVEL and B TRIG LEVEL signals, at pins 13 and 37 of A10U150 respectively, should have several levels: $\pm 1 \mathrm{~V}$ swings, $\pm 0.5 \mathrm{~V}$ swings, and voltage swing levels that approach a final level of gain iteratively as the binary search is done.
7. CH 1 and CH 2 TRIGGER signals should have two levels separated by 100 mV centered approximately around 0 V . (LR421/LR220 can be open and cause a FAIL flag to appear only at this diagnostic test level while the 9100 TRIGGER OFFSET level shows a PASS flag since that test only requires $\mathrm{CH} 1 / \mathrm{CH} 2$ trigger signal to be near 0 V , which is the case with these components open.)
8. EXT1 and EXT2 TRIG signals are provided externally and this signal path to the Trigger Source Select function within A/B Trigger Generator U150 is not tested by running test 9200 in CONTINUOUS mode. If FAIL flags only appear at EXT diagnostic levels, the EXT source inputs of U150 are most likely functional and the problem is either External Trigger Preamp U100 and related bias circuitry, or the BNC and R1001/R1003 signal path from the front panel.

| 9300 | This routine is not a test. Enough samples are acquired to calibrate the Jitter Correction Gain in |
| :--- | :--- |
| REPET | Extended Calibration. |

Troubleshooting Procedure:

1. Use the Jitter Correction Troubleshooting procedure to locate the source of the failure.
8 DEAD START

| POWER | Low Voltage Power Supply (schematic diagram 22) and Low Voltage Regulators (schematic |
| :--- | :--- |
| SUPPLIES |  |

1. Test for proper voltages on the SIDE BOARD. Check $+15 \mathrm{~V},+10 \mathrm{~V},+8 \mathrm{~V},+5 \mathrm{~V},+5 \mathrm{VD}$, $-15 \mathrm{~V},-10 \mathrm{~V},-8.3 \mathrm{~V}$ (should measure -8.6 V ), -8 V , and -5 V for proper levels. If any of the voltages are incorrect, troubleshoot the bad supply. The +5 VD supply is fused by F269 (schematic diagram 22) and the -15 V Unreg supply to the HV Oscillator is fused by F961 (schematic diagram 23). Both of these fuses are located under ribbon cables attaching to the power supply board and are hidden from view until the cables are disconnected.

A Control Electronics Troubleshooting chart for the Low Voltage Power Supply is located in the "Diagrams" section of this manual.

## WARNING

If troubleshooting the Low Voltage Power Supply with the ac power connected, use of an isolation transformer is necessary to prevent damage to equipment and possible personal injury due to electrical shock.
2. Check that PWRUP signal on U640 pin 2 (processor board) is HI and that the $\overline{\mathrm{RESET}}$ signal on U640 pin 37 is HI after the power on. If not, troubleshoot the Power Up (schematic diagram 23) and Power Up Reset circuitry (schematic diagram 1).

## PROCESSOR System Clocks (schematic diagram 7): <br> CLOCKS

1. Check System $\mu \mathrm{P}$ A12U640 pin 38 (schematic diagram 1) for 8 MHz . If not there, check System Clocks for the defective component(s) (schematic diagram 7). Check that $\mathrm{J} 132 \mathbf{( 4 0 ~ M H z}$ oscillator/External clock jumper, schematic diagram 7) is properly installed.
2. Check Front Panel Processor A13U700 at pin 5 (schematic diagram 3) for the 4 MHz clock. If not there, check System Clocks for the defective clock circuit (schematic diagram 7).
3. Repair clocks. Go to the System Clock Troubleshooting chart (located in the "Diagrams" section of this manual).
4. If clocks are working, and the scope still gives no signs of life, use the System $\mu \mathrm{P}$ Kernel Test to verify operation of the System $\mu \mathrm{P}$ addressing and chip-select circuitry.
[^10]Table 6-6 (cont)

In version 1.7 software, an abort will cause the Trigger LEDs to flash, but no coded flashing is done. The abort codes for version 2 software and possible causes of an abort are shown in the following table:

| CODE | Meaning | Possible Cause |
| :---: | :---: | :---: |
| 1 | Abort code initialized to this value at power-on. | Bad ROM/RAM. Firmware bug. |
| 2 | Unknown code received from Front Panel $\mu \mathrm{P}$. | Front Panel $\mu \mathrm{P}$ data path to System $\mu \mathrm{P}$ bad. |
| 3 | Too many bytes received from Front Panel $\mu \mathrm{P}$. | Front Panel $\mu \mathrm{P}$ data path to System $\mu \mathrm{P}$ bad or handshake logic bad. |
| 4 | Software Interrupt 2 or Software Interrupt 3 instruction executed. ${ }^{\text {a }}$ | Bad ROM/RAM. Firmware bug. |
| 5 | GPIB terminator value for query response scrambled. | Bad ROM/RAM. Firmware bug. (May require a COLD START.) |
| 6 | GPIB event code to be reported is unknown. | Bad ROM/RAM. Firmware bug. (May require a COLD START.) |
| 7 | GPIB delimiter found by scanner has changed and is invalid. | Bad ROM/RAM. Firmware bug. (May require a COLD START.) |

${ }^{\text {a }}$ SWI2 and SWI3 are not used in the software instructions. If executed, they were not as valid instructions.

Use the System $\mu \mathrm{P}$ Kernel Test to verify the ability of the System $\mu \mathrm{P}$ to function.
System $\mu$ P A12U640 (schematic diagram 1) Kernel Test:

1. With the power off, move jumper J126 from pins 1 and 2 to pins 2 and 3 of P126. This disables the System $\mu \mathrm{P}$ Data Bus Driver, and allows the data bus lines to be pulled up and down to a single-byte instruction. The instruction (CLRB) continually fetches and executes the CLRB instruction to step through the entire 64 K of addresses.
2. Move jumper J 127 (Waveform Processor Bus control) from the NORMAL position (pins 1 and 2 connected) to the BUSTAKE position (pins 2 and 4 connected). This places the Waveform Processor Bus under control of the System $\mu \mathrm{P}$. In the mode, the basic operation of the System $\mu \mathrm{P}$ can be checked, and all the address decoding circuitry can be verified.
3. Connect CH 1 of a test scope to TP840. Display that signal and use it as a trigger source for the test scope. This point is the AF address bit (the MSB) of the address bus.
4. Turn the power on and check that the RESET signal on U844 pin 8 is HI ; if not, troubleshoot the Power Up Reset circuitry (schematic diagram 1) and the Power Up circuitry (schematic diagram 23).
5. Adjust the test scope to view the AF signal. It should be a TTL-level square wave with a $\mathbf{5 0 \%}$ duty cycle.

Using the CH 2 probe:
6. Check each address line in order (from AF to A0) for a valid TTL-level signal, with each lower address line having a frequency of exactly twice the frequency as the address above it. Any loss of the 50\% duty cycle and/or distortion indicates a shorted address line. Check both the input and output pins of Address Buffers U732 and U632 to verify that they are working correctly, and to determine if address lines are shorted after the buffers. Waveform numbers 6, 7, 8, 9, 10, and 11 on schematic diagram 1 may be used to compare against the observed waveforms.
7. If a fault is found, if may be necessary to isolate the System $\mu \mathrm{P}$ address bus from the Waveform $\mu \mathrm{P}$ address bus to determine what circuitry is causing the problem. See the BUS ISOLATE and the WAVEFORM $\mu \mathrm{P}$ KERNEL MODE procedures following the SYSTEM $\mu \mathrm{P}$ CHIP SELECT TEST.

System $\mu \mathrm{P}$ Chip-Select Test:

1. From the Kernel mode, momentarily short the pins of J 129 together to reset the processor. This forces ROM0.0 to be switched in. Set the test scope to $10 \mathrm{~ms} /$ div to view one whole cycle of the AF period, and set the Trigger Slope so that AF is shown LO during the first half of the display. While AF is LO, addresses from 0000 h to 7FFFh are being executed; while HI, addresses from 8000h to FFFFh are executed.
2. Move jumper J 127 (shown on schematic diagram 2) to connect pins 2 and 4. This causes the "BUSTAKE" condition so that the System $\mu \mathrm{P}$ has access to the Waveform $\mu \mathrm{P}$ memory space. In this mode, most of the processing system can be verified.

Using the CH 2 probe:
3. Look for a LO chip-select signal, at the point designated in the following table, that occurs during the correct portion of the AF waveform period. Waveforms 20, 21, 22, 23, 24, and 25, may be used as comparison waveforms for the chip selects output from Address Decoder U570 (schematic diagram 2-Waveform $\mu \mathrm{P}$ ).

| Chip <br> Select | Test <br> Point | Bus | Address <br> Range (hex) | Position Within <br> the AF Period |
| :--- | :--- | :--- | :--- | :--- |
| $\overline{\text { SAVE }}$ | U580-8 | WP | $0000-1 F F F$ | First 1/8th |
| $\overline{D I S P}$ | U570-13 | WP | $2000-2 F F F$ | Third 1/16th |
| $\overline{\text { DATT }}$ | U570-12 | WP | $3000-3 F F F$ | Fourth 1/16th |
| $\overline{A C Q}$ | U570-11 | WP | $4000-4 F F F$ | Fifth 1/16th |
| CMD/TEMP | U250-8 | WP | $5000-57 F F$ | Twelfth 1/32nd |
| $\overline{\text { COEFF }}$ | U250-11 | WP | $5800-5 F F F$ | Thirteenth 1/32nd |
| $\overline{\text { HMMIO }}$ | U870-6 | BOTH | $6000-6 F F F$ | Seventh 1/16th |
| NVRAM | U840-6 | SYS | $7000-77 F F$ | Sixteenth 1/32nd |
| $\overline{\text { SYSRAM }}$ | U840-3 | SYS | $7800-7 F F F$ | Seventeenth 1/32nd |
| $\overline{\text { ROM0.X }}$ | U890-4 | SYS | $8000-B F F F$ | Third 1/4th |
| $\overline{R O M 1 ~}$ | U890-5 | SYS | C000-FFFF | Last 1/4th |

Table 6-6 (cont)
4. Check the host memory-mapped $\mathrm{I} / \mathrm{O}$ selects at the outputs of U 830 to verify that selects are generated and only during the time HMMIO is LO.
5. With the power off, check that no two of the select outputs are shorted together. If shorted, troubleshoot the cause and repair.

NOTE
If the problem is that one of the selects is not being generated, the SELF TEST will be able to determine that a group of registers fail. However, if two or more of the select lines are shorted together, any addressed devices will try to respond at the same time and bus contention will occur. The result is that the normal SELF TEST diagnostics testing won't work.
6. Check each of the System $\mu \mathrm{P}$ data bus lines (D7-D0) on the outputs of Data Bus Buffer U650. Look for open bus lines (no activity) and hung bus lines (stuck HI or LO). If a fault is found, it will be necessary to determine if it is on the System Bus or the Waveform $\mu \mathrm{P}$ bus. Use the BUS ISOLATE mode to assist in checking for a fault location.

## BUS ISOLATE MODE

1. Move jumper J 127 to the BUS ISOLATE position (pins 2 and 4 connected). This electrically disconnects the Waveform $\mu \mathrm{P}$ bus from the System $\mu \mathrm{P}$ bus to isolate the different parts of the processing system from each other.
2. Recheck the faulty data bus line to determine if it is still faulty (problem on the System $\mu \mathrm{P}$ data bus) or the fault is gone (problem on the Waveform $\mu \mathrm{P}$ data bus).
3. Check that no data bus activity is occurring during the Waveform $\mu \mathrm{P}$ address space (see Figure $6-10$ to compare against). Faulty address decoding can cause response from an incorrectly addressed device.
4. Check that the data bus is at the "float" level during periods of inactivity (waiting for a response from devices that are on the Waveform $\mu \mathrm{P}$ bus). A HI or a LO in the idle period indicates a stuck data bus.
5. If no faults are found on the System $\mu \mathrm{P}$ data bus, the problem data line may be on the Waveform $\mu \mathrm{P}$ bus. Use the Waveform $\mu \mathrm{P}$ Kernel mode to check for faults while the busses are isolated.


Figure 6-10. System $\mu \mathrm{P}$ data bit $\mathrm{D7}$ in the Bus isolate mode.

## Table 6-6 (cont)

WAVEFORM $\mu \mathrm{P} \quad$ Waveform $\mu \mathrm{P}$ Kernel Mode:
This mode is used when a fault has been found on either the System $\mu \mathrm{P}$ data bus or the System $\mu \mathrm{P}$ address bus while in the BUS CONNECT mode or when SELF TEST 5100 (RUN TASK) fails in the Extended Diagnostics menu.

1. Turn off the power and place the processor system in the BUS ISOLATE mode (see the preceding steps).
2. Remove jumper J128 (Waveform $\mu \mathrm{P}$ Kernel Mode) and jumper 185 (Waveform $\mu \mathrm{P}$ Reset Release). Both are located on the Processor board near Waveform $\mu \mathrm{P}$ U470.
3. With the power on in the Kernel mode, the Instruction Data Bus lines are pulled up or pulled down in a command that causes the U470 to address every instruction in its memory sequentially and continually. Instruction address bus lines and data address bus lines can be checked for activity. All the Instruction address bus lines and the data address bus lines with the exception of the top five (WAA through WAE) increment with the periods shown in the following tables. WAA through WAE will be fixed random values because page switching of the memory is not done and is not set to any known state in the Kernel test.

Waveform $\mu \mathrm{P}$ Instruction Bus Address Lines Waveform $\mu \mathrm{P}$ Data Bus Address Lines

| Signal | Location | Period |
| :---: | :--- | :---: |
| IA9 | TP580 | $409.6 \mu \mathrm{~S}$ |
| IA8 | U490-22 | $204.8 \mu \mathrm{~S}$ |
| IA7 | U490-23 | $102.4 \mu \mathrm{~S}$ |
| IA6 | U490-1 | $51.2 \mu \mathrm{~S}$ |
| IA5 | U490-2 | $25.6 \mu \mathrm{~S}$ |
| IA4 | U490-3 | $12.8 \mu \mathrm{~s}$ |
| IA3 | U490-4 | $6.4 \mu \mathrm{~s}$ |
| IA2 | U490-5 | $3.2 \mu \mathrm{~S}$ |
| IA1 | U490-6 | $1.6 \mu \mathrm{~S}$ |
| IAO | U490-7 | 800 ns |
| CLK2D | U490-8 | 200 ns |


| Signal | Location | Period |
| :--- | :--- | ---: |
| WAB | U562-9 | 1.6384 ms |
| WAA | TP562 | $819.2 \mu \mathrm{~S}$ |
| WA9 | U562-5 | $409.6 \mu \mathrm{~S}$ |
| WA8 | U562-2 | $204.8 \mu \mathrm{~S}$ |
| WA7 | U364-19 | $102.4 \mu \mathrm{~S}$ |
| WA6 | U364-16 | $51.2 \mu \mathrm{~s}$ |
| WA5 | U364-15 | $25.6 \mu \mathrm{~s}$ |
| WA4 | U364-12 | $12.8 \mu \mathrm{~s}$ |
| WA3 | U364-9 | $6.4 \mu \mathrm{~S}$ |
| WA2 | U364-6 | $3.2 \mu \mathrm{~s}$ |
| WA1 | U364-5 | $1.6 \mu \mathrm{~s}$ |
| WAO | U364-2 | 800 ns |

4. The Instruction Memory Data lines into the Waveform $\mu \mathrm{P}$ can also be checked to determine if any of the lines are shorted or open. Check against the schematic to see which lines (ID0 through IDF) are normally pulled up or normally pulled down for the Kernel test.

Table 6-7

## Video Option Troubleshooting

VIDEO
OPTION FAULT

Video Option (schematic diagram 21):
If VIDEO is pressed and an error message of "VIDEO OPTION NOT INSTALLED OR FAULTY" is displayed, then the power-on SELF TEST has detected a problem (assuming the Video Option is installed). During the power-on SELF TEST, a byte is written to Line Counter A12U530 (schematic diagram 21) and read back. If the byte read back is not what is expected, a flag is set to indicate that the test failed. When the SET VIDEO button is pressed, that flag is checked to see if the Video Option checked ok at power-up. If the test was not ok, the error message is displayed and the warning bell is sounded. If no error message is displayed, but test 2180 (FLD2) fails either at power-on or during a subsequent SELF TEST, troubleshoot as indicated in Table 6-6 Procedure 7 "Extended Diagnostics" for that failure.

Troubleshooting Procedure:

1. Check A12U830 pin 3 (schematic diagram 1) tor two negative strobes about $10.5 \mu \mathrm{~s}$ apart. (Viewing scope Sec/Div at $2 \mu \mathrm{~s}$, trigger on negative slope of the signal.) If not present, replace U830.

NOTE
The GPIBSEL signal also selects the Video Option registers. If communication via the GPIB interface is ok, then the select signals to Data Bus Buffer U532 (schematic diagram 20) and the buffer itself are ok. Suspect a problem with Programmable Line Counter U530 (schematic diagram 21).
2. Check U332C pin 8 (schematic diagram 20) for the same negative strobes as at U830 pin 3 . If not present, replace U332.
3. Check pins 2, 3, 4, 5, 6, 7, 8, and 9 of Data Bus Buffer U532 for activity (not stuck HI or LO) occurring at the same time as the negative strobe on U332C pin 8 . If stuck, troubleshoot the bad bus line.
4. Check that pin 14 of $U 530$ is at +5 V and that pin 1 is ground. If not, troubleshoot the cause.
5. Check that pin 8 of U530 is HI and that activity is occurring on pins $10,11,12,13,15,16$, and 17. If no activity, troubleshoot the problem.
6. If all inputs to U530 ok, replace U530.

Auto triggering or unstable trigger in VIDEO CPLG:
INITIAL SETUP

Apply a negative-sync, flat-field, video signal to the CH 2 input. Select the correct protocol (System M or Nonsystem M) for the applied signal using the Extended Functions menus.

Set the following controls:

| SLOPE/SYNC | - (negative sync) |
| :--- | :--- |
| VERTICAL. MODE | CH 2 |
| TRIGGER MODE | AUTO LEVEL |
| TRIGGER CPLG | VIDEO |
| TRIGGER SOURCE | CH 2 |
| SEC/DIV | $20 \mu \mathrm{~S}$ |
| A TRIGGER HO | 0 (no HO symbol displayed) |
| VOLTS/DIV | 1 V |

Press SET TV and select:
A TV COUPLING
TV LINE
CLAMP
OFF

1. Check the TVTG signal at U524B pin 8. If signal is present and no triggering is occurring, troubleshoot the Trigger Logic Array, A10U370 (schematic diagram 11).
2. If signal is absent, check the ATHO signal line at U424C pin 5 for HI-to-LO and LO-to-HI transitions. If not there, troubleshoot the Holdoff circuit (schematic diagram 13) as indicated in Table 6-6 in "HOLDOFF PROBLEMS".
3. If the ATHO signal is ok, check U424C pin 6 for an inverted ATHO signal; if not present, replace U424.
4. Check that U541B pin 6 has a positive pulse coincident with ATHO transitions. If not, replace U541.
5. Check that U524A pin 5 has a positive pulse coincident with the ATHO transitions. Check that U524A pin 3 is HI . If pin 3 is HI and pin 5 does not follow the ATHO transitions, replace U524.
6. Check pin 8 of U524B for a negative (TVTG) pulse coincident with the LO-to-HI ATHO transitions. If not present, check that the TVENA signal on pin 12 is HI and that the HORIZCLK input on pin 11 (see waveform 163) is ok. If those signals are correct, replace U524; if not correct, troubleshoot the source of the problem.
7. Check the test waveforms shown for schematic diagram 21 (waveforms 159 through 168). Troubleshoot the circuitry indicated by an incorrect waveform (see the following troubleshooting procedures).

## SIGNAL PROCESSING PROBLEM

See INITIAL SETUP in VIDEO Trigger Problem for control settings and signal application. Set the test scope Sec/Div setting to $5 \mu$ s and the Volts/Div to 2 V .

1. Check $\mathbf{U} 610$ pin 5 for a horizontal line sync signal having the negative sync tip at about 0.5 V and a back-porch level of +4.5 V . If correct, check pin 6 of U 420 B for the correct signal (see waveform 162). If not correct there, troubleshoot the Sync Pickoff Comparator (Q504 and Q510) and Pulse Stretcher circuits.
2. Check that U750 pin 16 (schematic diagram 20) is LO with negative sync selected and HI with positive sync selected. If not, troubleshoot U750.
3. Is the TVRC signal present at U612 pin 3 (waveform 159)? If not, troubleshoot the source of the TVRC signal (Q140 and U150) and the connecting signal path.
4. Set the Input Coupling on the scope to GND and check that the dc levels at U612 pins 3 and 13 are about the same. If not, troubleshoot U710B and associated circuitry.
5. Set the Input Coupling to $D C$ and check that the negative sync tip amplitude at $U 610$ pin 9 is about 50 to 75 mV (from back-porch level to negative tip) with about a -3 V dc offset. If yes, the AGC amplifier and Sync Tip Clamp circuit are ok. Troubleshoot the Fixed Gain Amplifier, the Sync Pickoff Comparator, the Trigger Back-Porch Clamp, and associated circuitry. If the signal is not correct at pin 9 of U610 with the correct TVRC signal applied, troubleshoot the AGC amplifier and Sync Tip Clamp, and associated feedback circuitry.
6. Set Input Coupling to GND and check that U510 pin 6 is within 1 V of ground level. If not, troubleshoot U510 and associated circuitry.
7. Set the Trigger CPLG to VIDEO, Trigger SOURCE to CH 2, Trigger SLOPE to -(neg-sync), A VIDEO COUPLING to FIELD1-Line count to 10, CH 2 input coupling to DC, SEC/DIV to $200 \mu \mathrm{~s}$, VIDEO CLAMP OFF, and VOLTS/DIV to 1 V (for a two-division signal amplitude). Connect a negative sync composite video signal to the CH 2 input.
8. Check pin 13 of U314 for narrow positive pulses that coincide with the horizontal sync pulses of the applied video signal. If not present, suspect the Phase Locked Loop circuitry and its input and output signals.
9. Check Q330, CR324, CR326, CR325, and VR234 for opens or shorts.
10. Check U308B pin 3 for a LO pulse coincident with the Horizontal Sync of the applied video signal. If not present, check for the presence of the COMPSYNC signal at U310A pin 5 (waveform 169). If COMPSYNC is ok, but the signal at U308B pin 3 is not, troubleshoot U420 and associated circuitry. If both are missing, troubleshoot back through the Video Option input and signal processing circuitry to find the problem.
11. Check the following signals: $2 \times H$ at U314 pin 4, $\overline{2 \times H}$ at U308A pin 9, $\overline{\text { HORIZCLK }}$ at U220B pin 12, HCLK at U220B pin 13, DLY'D HCLK at U220A pin 1 (held LO when the PLL is unlocked), VERTSYNC at U310A pin 1. Troubleshoot the cause of any missing signals. (See Figure 3-14 in Section 3 for typical waveforms.)

## Table 6-7 (cont)

INCORRECT LINE COUNTING

See INITIAL SETUP in VIDEO Trigger Problem for control settings and signal application. Set the test scope Sec/Div setting to $5 \mu$ s and the Volts/Div to 2 V .

1. Check that the correct protocol and Counter Restart choices are selected for the applied Video signal. (TV OPT under the EXTENDED FUNCTIONS-SYSTEM choices.)
2. Check that the $\overline{\text { HORIZCLK }}$ signal at U220B pin 12 is stable. If not, troubleshoot that problem.
3. Check that the FIELD signal at U424E pin 13 is stable and correct (waveform 164). If not, troubleshoot that problem. (Is the trigger signal amplitude excessive, causing erratic triggering?)
4. If the FIELD and $\overline{\text { HORIZCLK }}$ signals are ok, suspect a problem with Line Counter U530, NANDgate U541, or U424.
5. Check that the FLD1 signal at U541 is HI when FLD1 is selected and alternates HI-to-LO when ALT is selected. If not, troubleshoot A12U750 (schematic diagram 20). (This assumes that the FLD2 diagnostic test passed the power-on diagnostics.)
6. Check Line Counter outputs at pin 27 and pin 3 for a LO-to-HI transition during the vertical sync pulse time. (View the composite video on channel 2 of the test scope and use the channel 1 probe to check the signal at pin 27 and pin 3 . Trigger the test scope on the channel 1 signal. Use delayed sweep to view the signals if using an analog test scope.)
7. If not correct, replace U530.
8. Check that the clock at pin 8 of U424D is stable and has a LO-to-HI transition. If no transition, replace U424.

TV CLAMP PROBLEM

## NOTE

The Video Option must have a composite-sync or composite-video signal source applied for the Channel 2 Display Clamp to function properly. Clamping action is unpredictable if an incorrect signal is applied. The CLAMP circuit remains on, even if VIDEO COUPLING is not selected, and may be used to clamp a Channel 2 display if the selected VIDEO source signal is a composite-sync or composite-video signal.

1. Set the Trigger CPLG to TV. Trigger SOURCE to CH 2, Trigger SLOPE to - (neg-sync), A COUPLING to FIELD1-Line count to 50, CH 2 input coupling to DC, SEC/DIV to $5 \mu \mathrm{~s}$, CLAMP OFF, and VOLTS/DIV to 1 V (for a two-division signal amplitude). Connect the negative sync composite video signal to the CH 2 input in series with a dc offset voltage source. Set the offset level for 0 V offset.
2. Is the display triggered and stable? If not, the CLAMP circuit will not be properly enabled in any case, and some other problem may exist. Check that the collector of Q330 is LO. If not LO, either the PLL (U314) is not locked or Q330 or its associated circuitry is defective; go to PHASELOCKED LOOP PROBLEM troubleshooting.
3. If the display is triggered correctly, check that the back-porch level of the displayed video signal is at approximately ground level. If not, run SELF CAL and check again. If there is a large offset present, troubleshoot CH 2 Preamp U320 and U230 (schematic diagram 9).
4. Set the offset voltage for -1.5 V offset, and verify that the back-porch level is offset from ground -1.5 V .
5. Set CLAMP ON. Is the back-porch level clamped to ground level? If so, the VIDEO clamp is functioning.

Table 6.7 (cont)
6. Did the CH 2 signal display change vertical position by any amount when CLAMP was turned on? If not, check that BPCLAMP is HI with CLAMP ON. Troubleshoot A12U750 (schematic diagram 20) if not correct.
7. Check that pin 3 of U410A has a 10 V positive pulse at the beginning of the back porch of the applied video signal (waveform 165). If not, troubleshoot U410A and associated components.
8. Set the test scope BW Limit to 20 MHz and the Volts/Div to 50 mV . Check $\mathbf{U 5 2 0} \mathrm{pin} 3$ for a CH 2 PO signal that is a replica of the applied video signal. If not present, troubleshoot the CH 2 Preamplifier Pickoff circuitry and the signal path between it and pin 3.
9. Check that pin 6 of U520 is approximately 0 V with the CLAMP OFF and approximately -130 mV with the CLAMP ON. If not switching correctly between CLAMP ON and CLAMP OFF, troubleshoot U410C, Q420, and U520.
10. Switch CH 2 INVERT ON check pin 6 of U520 again as in step 9. If not correct, troubleshoot U514, U410B, U410E and the CH 2 INV signal (should be HI with CH 2 INVERT ON).
11. Check U710D pin 14 for approximately 0 V with CLAMP OFF and approximately -130 mV with CLAMP ON. If not correct, replace U710. Check that the Source of Q710 follows pin 14 of U710D for CLAMP ON and CLAMP OFF. If not, troubleshoot Q710, U710A, and associated components.

## FRONT-PANEL SETTINGS FOR INIT PANEL

Table 6-8 lists the front-panel settings which are returned when INIT PANEL is executed from the AutoStep menu (PRGM).

Table 6-8
INIT PANEL States

|  | AUTOSETUP Controls |
| :--- | :--- |
| CURSOR Controls |  |
| Mode | VIEW |
| RESolution | CURSOR POSITION |
| CURSOR/DELAY Knob |  |
| CURSOR FUNCTION | All off |
| VOLTS UNITS | VOLTS |
| TIME UNITS | SEC |
| SLOPE UNITS | VOLTS/SEC |
| CURSOR Mode | $\Delta$ |
| ATTACH CURSORS TO: | CH 1 |
| X-Axis Cursor Position | $\pm 3$ divisions |
| Y-Axis Cursor Position | $\pm 3$ divisions |
| TIME Cursor Position | $\pm 4$ divisions |
| VOLTS Ref Value | 1.0 V |
| TIME Ref Value | 1.0 SEC |
| SLOPE Ref Value | $1.0 \mathrm{~V} / \mathrm{SEC}$ |


| DELAY Controls |  |
| :--- | :--- |
| DELAY by EVENTS | OFF |
| $\Delta$ TIME | OFF |
| DELAY TIME | $40 \mu \mathrm{~s}$ |
| $\triangle$ DELAY Time | 0.0 |
| DELAY EVENTS Count | 1 |
|  |  |
| DEVICES/SETUP (OUTPUT) |  |
|  |  |
| DEVICES |  |
| HPGL PLOTTER | OFF |
| THINKJET PRINTER | ON |
|  |  |
| SETUP |  |
| Print SETTINGS | ON |
| Print TEXT | ON |
| Print GRAT | ON |
| Print WFM | ON |
| PGSIZE | US |

Table 6-8 (cont)

| GPIB SETUP (OUTPUT) |  | MEASURE Controls |  |
| :---: | :---: | :---: | :---: |
| DEBUG | OFF | MARK | OFF |
| LONG | ON | DISPLAY | OFF |
| LOCK | LLO | WINDOW | OFF |
| PATH | ON | METHOD | MIN/MAX |
| RQS Mask | ON | LEVEL (units) | \% |
| OPC Mask | ON | LEVEL (settings) |  |
| CER Mask | ON | PROXIMAL | 10\%/0.4 volts |
| EXR Mask | ON | MESIAL | 50\%/1.3 volts |
| EXW Mask | ON | MESIAL2 | 50\%/1.3 volts |
| INR Mask | ON | DISTAL | 90\%/2.4 volts |
| USER Mask | OFF | TARGET | CH 1 |
| PID Mask | OFF | STORAGE Mode Controls |  |
| DEVDEP Mask | ON |  |  |
| Data Encoding (ENCDG) | BINARY | STORAGE Mode | SAVE |
| Data Target | REF 1 | ACQUIRE Mode | NORMAL |
| Data Source | CH 1 | REPET | OFF |
| FASTXMIT | OFF | AVG Number | 2 |
| FASTXMIT | 1 | ENVELOPE Number | 1 |
| CURVE ONLY | OFF | SAVE ON $\triangle$ | OFF |
| START | 256 | REF1 through REF4 | OFF |
| STOP | 512 |  |  |
| LEVEL | 0 | TRIGGER Controls |  |
| HYSTERESIS | 5 | A/B TRIG set for | A |
| DIRECTION | PLUS | A TRIG MODE | AUTO LEVEL |
| SETUP ATTRIBUTE | 0 | B TRIG MODE | RUNS AFTER |
| DT | OFF | SOURCE (both) | CH 1 |
| HORIZONTAL Mode Controls |  | COUPLING (both) | DC |
| MODE | A | SLOPE (both) | + (plus) |
| A SEC/DIV | 1 ms | TRIG POSITION | $1 / 2$ (512) |
| EXT CLK Expansion |  | LEVEL (both) | 0.0 |
| Factor | 1 | EXT GAIN (both) |  |
| EXT CLK | OFF | HOLDOFF | Minimum |
| POSITION Waveform | LIVE | VERTICAL MODE Controls |  |
| POSITION Reference | REF 1 |  |  |
| POSITION set to | Midscreen | CH 1 | ON |
| POSITION REF mode | INDependent | VOLTS/DIV (both) | 100 mV |
| INTENSITY Controls |  | VARIABLE (both) COUPLING (both) | CAL DC |
| SELECT | DISP | $50 \Omega$ (both) | OFF |
| READOUT Intensity | 50\% | INVERT (both) | OFF |
| DISP Intensity | 40\% | POSITION set to | Mid screen |
| GRAT Illum | 0\% | Display Mode | YT |
| INTENS Level | 80\% | BANDWIDTH | FULL |
| VECTORS | ON | SMOOTH | OFF |

Table 6-8 (cont)

| VIDEO OPTION Setup (SET TV) |  | WORD RECOGNIZER (SET WORD) |  |
| :---: | :---: | :---: | :---: |
| Interlaced Coupling | FIELD1 | Word Match | Don't care |
| Noninterlaced Coupling | FIELD1 |  | (all X ) |
| TV SYNC | - (minus) | RADIX | HEX |
| CLAMP | OFF | CLOCK | ASYNC |
| Line Count | 525 |  |  |
| Line Start | PREFLD |  |  |

## OPTIONS AND ACCESSORIES

## OPTIONS DESCRIPTION

This section contains a general description of available options for the 2440 Digital Storage Oscilloscope at time of manual publication. The options are:

Options A1-A-5
Option 1R
Option 03
Option 05
Option 11

International Power Cords
Rackmounting
Word Recognizer Probe
Video Option
Probe Power

Operating instructions for the Video Option and the Word Recognizer Probe optional accessory are found in the Options section of the Operators Manual. A complete list of standard accessories supplied with the instrument and a list of suggested optional accessories, each identified by part number, are included in this section.

Additional information about instrument options, option availability, and other accessories can be obtained from the current Tektronix Products Catalog or by contacting your local Tektronix Field Office or representative.

## OPTIONS A1-A5 <br> INTERNATIONAL POWER CORDS

Instruments are shipped with the detachable powercord configuration ordered by the customer. Descriptive information about the international power-cord options is provided in Section 2, "Preparation for Use." The following list identifies the Tek Option number for the available power cords.

| Option A1 (Universal Euro) <br> Power cord $(2.5 \mathrm{~m})$ | $161-0104-06$ |
| :--- | :---: |
| Option A2 (UK) |  |
| Power cord $(2.5 \mathrm{~m})$ | $161-0104-07$ |
| Option A3 (Australian) |  |
| Power cord (2.5 m) | $161-0104-05$ |
| Option A4 (North American) |  |
| Power cord (2.5 m) | $161-0104-08$ |
| Option A5 (Switzerland) |  |
| Power cord (2.5 m) | $161-0154-00$ |

## OPTION 1R RACKMOUNTED 2440

When the 2440 Digital Oscilloscope is ordered with Option 1R, it is shipped in a configuration that permits easy installation into a 19 -inch-wide equipment rack. An optional rackmounting kit may be ordered to convert the standard 2440 to a rackmounted instrument. Installation instructions for rackmounting are provided in the documentation supplied with the rackmounting kit and the 1R Option.

The rear-support kit also is supplied for use when rackmounting the 2440 . Using this rear-support kit enables the rackmounted instrument to meet all electrical and environmental specifications of the standard instrument.

Connector-mounting holes are provided in the front panel of the rackmounted instrument. These holes enable convenient accessing of the rear panel BNC connectors and directing the Vertical Channel and External Trigger input connectors to rear access in an electronics equipment rack. The selection of signals that are routed through the rackmounting front panel is left to the user. Additional cabling and connectors required to implement any through-panel access must be user supplied; however, the necessary items may be separately ordered from Tektronix, Inc.

## OPTION 03—WORD RECOGNIZER PROBE

The Word Recognizer (WR) Probe is available as an option or can be ordered as an optional accessory. In either case, it is used to trigger the instrument on userselected parallel TTL data word. The WR recognizes a 16-bit word, plus a 17 th qualifier bit. Each bit is selectable as $0,1, X$ (don't care). Recognition can be either synchronous with an external clock signal (rising or falling edge) or asynchronous.

For instruments purchased either with or without Option-03, the required hardware and firmware for using the Word Recognizer Probe is included in the standard 2440 Digital Oscilloscope; it is only necessary to purchase the Word Recognizer Probe optional accessory. Instruments purchased with Option-03 include the WR Probe.

## OPTION 05 VIDEO OPTION

Option 05 provides an aid in examining composite video signals. With the Video Option installed, all basic instrument functions remain the same. Changes to any of the control menus by the installation of Option 05 are detailed in the description of the affected menus in Section 3 of the Operators Manual, "Controls, Connectors, and Indicators." Features of this option include a sync separator, backporch clamp circuitry, TV trigger coupling modes, and adjustment for closer tolerance on the $20-\mathrm{MHz}$ BANDWIDTH LIMIT. This option permits the user to trigger on a specific line number within a TV field and provides sync-polarity switching for either sync-negative or sync-positive composite video signals. Circuit descriptions and schematics for the Video Option are located in the appropriate sections in this Service Manual.

## OPTION 11 PROBE POWER

Option 11 provides two probe-power connectors on the rear panel of the instrument. Voltages supplied at the PROBE POWER connectors meet the power requirements of standard Tektronix active oscilloscope probes.

## STANDARD ACCESSORIES

The following standard accessories are provided with each instrument:

| 2 Probes, 10X, 1.3 meter, |  |
| :--- | :--- |
| $\quad$ with accessories | P6137 |
| 1 Accessory pouch, snap | $016-0692-00$ |
| 1 Accessory pouch, ziploc | $016-0537-00$ |
| 1 Operators manual | $070-6599-00$ |
| 1 Programmers Reference Guide | $070-6601-00$ |
| 1 Pocket Programmers Guide | $070-6602-00$ |
| 1 User Reference Guide | $070-6600-00$ |
| 1 Fuse, 5 A, 250 V, AGC/3AG | $159-0014-00$ |
| 1 CRT Filter, Blue Plastic (installed) | $378-0199-03$ |
| 1 CRT Filter, Clear Plastic | $378-0208-00$ |
| 1 Front Cover | $200-3199-01$ |
| 1 CCIR Graticule (with Video Option) | $378-0199-04$ |
| 1 NTSC Graticule (with Video Option) | $378-0199-05$ |

## RACKMOUNTING ACCESSORIES

The following accessories are available to rackmount an instrument that is not purchased as a 1R option:

Part Number
Rackmounting Conversion Kit
016-0825-01
Rackmounting Rear-Support Kit
(included in the conversion kit)
016-0096-00

## OPTIONAL ACCESSORIES

The following optional accessories are recommended for use with this oscilloscope:

## Part Number

| Service Manual | $070-6603-00$ |
| :--- | :--- |
| Word Recognizer Probe | $010-6407-01$ |
| Color Plotter | HC100 |
| Oscilloscope Camera | C-5C Option 01 |
|  | C7, Option 03, Option 30 |
| SCOPE-MOBILE Cart | K212, K213 |
| Carrying Strap | $346-0199-00$ |

## REPLACEABLE ELECTRICAL PARTS

## PARTS ORDERING INFORMATION

Replacement parts are avaliable from or through your local Tektronix, Inc. Field Office or representative.

When ordering parts, include the following information in your order: part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

## LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the electrical parts list. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

## CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfg. Code Number to Manufacturer Cross Index for the electrical parts list is located immediately after this page. The cross index provides codes, names, and addresses of manufacturers of components listed in the electrical parts list.
ABBREVIATIONS
Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the parts list)


Read: Resistor 1234 of Assembly 23


Read: Resistor 1234 of Subassembly 2 of Assembly 23

The circuit component's number appears on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the mechanical parts list. The component number is obtained by adding the assembly number prefix to the circuit number.

The electrical parts list is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the electrical parts list.

## TEKTRONIX PART NO. (column two of the parts list)

Indicates part number to be used when ordering replacement part from Tektronix.

## SERIAL NO. (columns three and four of the parts list)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

## NAME \& DESCRIPTION (column five of the parts list)

In the parts list, an item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. For further item name identification, the U.S. Federal Catalog handbook H6-1 can be utilized where possible.

## MFR. CODE (column six of the parts list)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

## MFR. PART NO. (column seven of the parts list)

Indicates actual manufacturer's part number.

## CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

| Mtr. Code | Manufacturer | Address | City, State, Zip Code |
| :---: | :---: | :---: | :---: |
| S3774 | OSHINO ELECTRIC LAMP WORKS LTD | 52 MINAMI SHINAGAWA 2 CHORE SHINAGAWA KU | TOKYO JAPAN |
| S4091 | SANYO ELECTRIC CO LTD |  | OSAKA JAPAN |
| S4246 | JAPAN SERVO CO LTD | $\begin{aligned} & 7 \text { KANDA } \\ & \text { MITOSHIRO-CHO CHIYODA-KU } \end{aligned}$ | TOKYO JAPAN |
| TKOIO | TAJIMI ELECTRONICS CO LTD | $\begin{aligned} & 29-1,2-C H O M E \text { EBISU-MINAMI, } \\ & \text { SHIBUYA-KU } \end{aligned}$ | TOKYO, JAPAP 101 |
| TK0515 | EVOX-RIFA INC | 100 TRI-STATE INTERNATIONAL SUITE 290 | LINCOLNSHIRE IL 60015 |
| TK0891 | MICONICS | 1 FAIRCHILD AVE | PLAINVIEW NY 11803 |
| TK1 163 | POLYCAST INC | 9898 SW TIGARD ST | TIGARD OR 97223 |
| TK1177 | BELL INDUSTRIES (DIST) | 6024 SW JEAN ROAD | LAKE OSWEGO OR 97034 |
| TK1312 | LEMO USA INC | 335 TESCONI CIR PO BOX 11006 | SANTA ROSA CA 95406 |
| TK1326 | NORTHWEST FOURSLIDE INC | 18224 SW 100TH CT | TUALATIN OR 97062 |
| TK1725 | GREENPAR CONNECTTORS LTD | PO BOX 15 HARLOW | ESSEX CM20 2ER ENGLAND |
| TK1727 | PHILIPS NEDERLAND BV AFD ELONCO | POSTBUS 90050 | 5600 PB EINDHOVEN THE NETHERLANDS |
| TK1743 | UNITRODE (UK) LTD | 6 CRESSWELL PARK BLACKHEATH | LONDON SE 3 9RD ENGLAND |
| TK1913 | WIMA <br> THE INTER-TECHNICAL GROUP IND | ONE BRIDGE ST PO BOX 23 | IRVNGTON NY 10533 |
| TK2073 | TOCOS AMERICA INC | 565 W GULF ROAD | ARLINGTON HEIGHTS IL 60005 |
| TK2292 | SENSOR AND SWITCHES INC DIV OF DESCO CORP OF COLUMBUS OHIO | PO BOX 3297 | LEXINGTON OH 44904 |
| TK2319 | COLLMER | 14368 PROTON RD | DALLAS TX 75244 |
| TK2425 | CHUNG HING INDUSTRY CO LTD <br> PHONE: 5-564114/8 <br> FAX: 852-5-713679 | 1ST FLOOR, SUNRIDGE IND BLDG 10 HONG MAN STREET | CHAWAN HONG KONG |
| TK2515 | FEE FIL-MAG USA | 4787 CARDIN STREET | SAN DIEGO CA 92111-1416 |
| TK2540 | SONY CORPORATION OF AMERICA COMPONENT PRODUCTS DIVISION SEMICONDUCTOR DIVISION | 10833 VALLEY VIEW STREET | CYPRESS CA 90630-0016 |
| TK6051 | CITIZEN ELECTRONICS CO LTD | 4126 E LA PALMA | ANAHEIM CA 92807-1814 |
| OBOA9 | DALLAS SEMICONDUCTOR CORP | 4350 BELTWOOD PKWY SOUTH | DALLAS TX 75244 |
| 0CVK3 | ALLEGRO MICROSYSTEMS INC INTEGRATED CIRCUITS DIV | 115 NE CUTOFF | WORCHESTER MA 01606 |
| OH1N5 | MARCON AMERICA CORP | 998 FIRST EDGE DRIVE | VERNON HILLS IL 60061 |
| OJR03 | ZMAN MAGNETICS INC | 7633 S 180th | KENT WA 98032 |
| O.JR04 | TOSHIBA AMERICA INC ELECTRONICS COMPONENTS DIV | 9775 TOLEDO WAY | IRVNE CA 92718 |
| OJ7N9 | MCXINC | 30608 SAN ANTONIO ST | HAYWARD CA 94544 |
| 0.J9R2 | HARISON ELECTRIC CO LTD | ASAHIMACHI 5-CHOME IMABARI | EHIME JAPAN |

## CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

| Mfr. Code | Manufacturer | Address | City, State, Zlp Code |
| :---: | :---: | :---: | :---: |
| OMS63 | QUALITY TECHNOLOGIES CORP | 610 N MARY AVENUE | SUNNYVALE CA 94086 |
| ONOKO | CALOGIC CORP | 237 WHITNEY PLACE | FREMONT CA 94539 |
| 00779 | AMP INC | 2800 FULLING MILL <br> PO BOX 3608 | HARRISBURG PA 17105 |
| 00853 | SANGAMO WESTON INC COMPONENTS DIV | SANGAMO RD PO BOX 128 | PICKENS SC 29671-9716 |
| 01295 | TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP | 13500 N CENTRAL EXPY <br> PO BOX 655012 | DALLAS TX 75265 |
| 01537 | motorola <br> COMMUNICATIONS AND ELECTRONICS INC | 2553 N EDGINGTON ST | FRANKLIN PARK IL 60131-3401 |
| 02113 | COILCRAFTINC | 1102 SILVER LAKE RD | CARY IL 60013-1658 |
| 04222 | AVX CERAMICS DIV OF AVX CORP | 19TH AVE SOUTH <br> P O BOX 867 | MYRTLE BEACH SC 29577 |
| 04713 | MOTOROLAINC SEMICONDUCTOR PRODUCTS SECTOR | 5005 E MCDOWELL RD | PHOENIX AZ 85008-4229 |
| 05292 | ITT COMPONENTS DIV |  | CLIFTON NJ |
| 05828 | GENERAL INSTRUMENT CORP GOVERNMENT SYSTEMS DIV | 600 W JOHN ST | HICKSVILE NY 11802 |
| 07716 | TRW INC <br> TRW IRC FIXED RESISTORS/BURLINGTON | 2850 MT PLEASANT AVE | BURLINGTON IA 52601 |
| 09922 | BURNDY CORP | RICHARDS AVE | NORWALK CT 06852 |
| 1 CH 66 | PHILIPS SEMICONDUCTORS | 811 E ARQUES AVENUE PO BOX 3409 | SUNNYVALE CA 94088-3409 |
| 1W344 | UNITED CHEMI-CON INC | 9801 W HIGGINS SUITE 430 | ROSEMONT IL 60018-4704 |
| 11236 | CTS CORP <br> BERNE DIV <br> THICK FILM PRODUCTS GROUP | 406 PARR ROAD | BERNE IN 46711-9506 |
| 11502 | INTERNATIONAL RESISTIVE CO INC | GREENWAY RD PO BOX 1860 | BOONE NC 28607-1860 |
| 12697 | CLAROSTAT MFG COINC | LOWER WASHINGTON ST | DOVER NH 03820 |
| 12954 | MICROSEMI CORP - SCOTTSDALE | 8700 E THOMAS RD POBOX 1390 | SCOTTSDALE AZ 85252 |
| 14552 | MICROSEMI CORP | 2830 S FAIRVIEW ST | SANTA ANA CA 92704-5948 |
| 14936 | GENERAL INSTRUMENT CORP DISCRETE SEMI CONDUCTOR DIV | 600 W JOHN ST | HICKSVILLE NY 11802 |
| 15454 | KETEMA <br> RODAN DIVISION | 2900 BLUE STAR STREET | ANAHEIM CA 92806-2591 |
| 17856 | SLLICONIXINC | 2201 LAURELWOOD RD | SANTA CLARA CA 95054-1516 |
| 18796 | MURATA ERIE NORTH AMERICAN INC STATE COLLEGE OPERATIONS | 1900 W COLLEGE AVE | STATE COLLEGE PA 16801-2723 |
| 19701 | PHILIPS COMPONENTS DISCRETE PRODUCTS <br> DIV RESISTIVE PRODUCTS FACILITY AIRPORT ROAD | PO BOX 760 | MINERAL WELLS TX 76067-0760 |

## CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

| Mfr. <br> Code | Manufacturer | Address | City, State, Zip Code |
| :---: | :---: | :---: | :---: |
| 22526 | DU PONT EI DE NEMOURS AND CO INC DU PONT ELECTRONICS DEPT | 515 FISHING CREEK RD | NEW CUMBERLAND PA 17070-3007 |
| 24165 | SPRAGUE ELECTRIC CO | 267 LOWEL R ROAD | HUDSON NH 03051 |
| 24355 | ANALOG DEVICES INC | RT 1 INDUSTRIAL PK PO BOX 9106 | NORWOOD MA 02062 |
| 24546 | BRADFORD ELECTRONICS | 550 HIGH ST | BRADFORD PA 16701-3737 |
| 25088 | SIEMENS CORP | 186 WOOD AVE S | ISELIN NJ 08830-2704 |
| 25403 | PHILIPS COMPONENTS DISCRETE PRODUCTS DIV DISCRETE SEMICONDUCTOR GROUP | GEORGE WASHINGTON HWY | SMITHFIELD RI 02917 |
| 27014 | NATIONAL SEMICONDUCTOR CORP | 2900 SEMICONDUCTOR DR | SANTA CLARA CA 95051-0606 |
| 31918 | ITT SCHADOW INC | 8081 WALLACE RD | EDEN PRAIRIE MN 55344-2224 |
| 32997 | BOURNS INC TRIMPOT DIV | 1200 COLUMBIA AVE | RIVERSIDE CA 92507-2114 |
| 33095 | SPECTRUM CONTROLINC | 2185 W WEIGHT ST | ERIE PA 16505 |
| 34333 | SILICON GENERAL INC | 11651 MONARCH ST | GARDEN GROVE CA 92641-1816 |
| 34371 | HARRIS CORP <br> HARRIS SEMICONDUCTOR PRODUCTS GROUP | 200 PALM BAY BLVD PO BOX 883 | MELBOURNE FL 32919 |
| 50101 | FREQUENCY SOURCES INC SEMICONDUCTOR DIV SUB OF LORAL CORP | 16 MAPLE RD | CHELMSFORD MA 01824-3737 |
| 50139 | ALLEN-BRADLEY CO ELECTRONIC COMPONENTS | 1414 ALLEN BRADLEY DR | EL PASO TX 79936 |
| 50434 | HEWLETT-PACKARD CO OPTOELECTRONICS DIV | 370 W TRIMBLE RD | SAN JOSE CA 95131-1008 |
| 51406 | MURATA ERIE NORTH AMERICA INC HEADQUARTERS AND GEORGIA OPERATIONS | 2200 LAKE PARK DR | SMYRNA GA 30080 |
| 52769 | SPRAGUE-GOODMAN ELECTRONICS INC | 134 FULTON AVE | GARDEN CITY PARK NY 11040-5352 |
| 53387 | MINNESOTA MINING MFG CO | PO BOX 2963 | AUSTIN TX 78769-2963 |
| 54937 | DEYOUNG MANUFACTURING INC | 12920 NE 125TH WAY | KIRKLAND WA 98034-7716 |
| 56845 | DALE ELECTRONICS INC | 2300 RIVERSIDE BLVD <br> PO BOX 74 | NORFOLK NE 68701-2242 |
| 57668 | ROHM CORP | 8 WHATNEY <br> PO BOX 19515 | IRVINE CA 92713 |
| 59660 | TUSONIXINC | 7741 N BUSINESS PARK DR PO BOX 37144 | TUCSON AZ 85740-7144 |
| 6L334 | DIODES INC | 9957 CANOGA AVENUE | CHATSWORTH CA 91311 |
| 61545 | AMP KEYBOARD TECHNOLOGIES INC SUB OF AMP INC | 76 BLANCHARD RD PO BOX 543 | BURLINGTON MA 01803-5125 |
| 61857 | SAN-O INDUSTRIAL CORP | 85 ORVILLE DR PO BOX 511 | BOHEMIA LONG ISLAND NY 11716-2501 |
| 62786 | HITACHI AMERICA LTD HITACHI PLAZA | 2000 SIERRA POINT PARKWAY | BRISBANE CA 94005 |

# CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER 

| Mfr. <br> Code | Manufacturer | Address | City, State, Zip Code |
| :---: | :---: | :---: | :---: |
| 64537 | KDI ELECTRONICS INC SUBSIDIARY OF KDI CORP | 31 FARINELLA DR | EAST HANOVER NJ 07936 |
| 65786 | CYPRESS SEMICONDUCTOR CORP | 3901 N 1ST ST | SAN JOSE CA 95134-1506 |
| 66302 | VLSI TECHNOLOGYINC | 1109 MCKAY DR | SAN JOSE CA 95131-1706 |
| 66958 | SGS SEMICONDUCTOR CORP | 1000 E BELL RD | PHOENIX AZ 85022-2649 |
| 7W718 | MARQUARDT SWITCHES INC | 2711 ROUTH 20 EAST | CAZENOVIA NY 13035-1219 |
| 71400 | BUSSMANN <br> DIV OF COOPER INDUSTRIES INC | 114 OLD STATE RD <br> PO BOX 14460 | ST LOUIS MO 63178 |
| 71590 | CRL COMPONENTS INC | HWY 20 W PO BOX 858 | FORT DODGE IA 50501 |
| 75042 | IRC ELECTRONIC COMPONENTS PHILADELPHIA DIV TRW FIXED RESISTORS | 401 N BROAD ST | PHILADELPHIA PA 19108-1001 |
| 75498 | MULTICOMP INC | 3005 SW 154TH TERRACE \#3 | BEAVERTON OR 97006 |
| 76854 | OAK/GRIGSBY <br> AN OAK INDUSTRIES INC CO | 88 N DUGAN ROAD PO BOX 890 | SUGAR GROVE IL 60544-0890 |
| 80009 | TEKTRONIXINC | 14150 SW KARL BRAUN DR PO BOX 500 | BEAVERTON OR 97077-0001 |
| 81483 | INTERNATIONAL RECTIFIER | 9220 SUNSET BLVD | LOS ANGELES CA 90069-3501 |
| 81855 | EAGLE-PICHER INDUSTRIES INC ELECTRONICS DIV | COUPLES DEPT C AND PORTER STS PO BOX 47 | JOPLIN MO 64801 |
| 84411 | AMERICAN SHIZUKI CORP OGALLALA OPERATIONS | 301 WEST O ST | OGALLALA NE 69153-1844 |
| 91637 | DALE ELECTRONICS INC | $\begin{aligned} & 2064 \text { 12TH AVE } \\ & \text { PO BOX } 609 \end{aligned}$ | COLUMBUS NE 68601-3632 |


| Component Number | Tektronix <br> Part No. | Serial Effective | No. Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A10 | 671-0365-00 | B010100 | 8010185 | CIRCUIT BD ASSY:MAIN | 80009 | 671036500 |
| A10 | 671-0365-02 | B010186 | B010825 | CIRCUIT BD ASSY:MAIN | 80009 | 671036502 |
| A10 | 671-0365-03 | B010826 |  | CIRCUIT BD ASSY:MAIN (STANDARD) | 80009 | 671036503 |
| A10 | 671-0365-03 |  |  | CIRCUIT BD ASSY:MAIN (2440M) | 80009 | 671036503 |
| A11 | 671-0366-0 | B010100 | B010504 | CIRCUIT BD ASSY:TIME BASE DISPLAY | 80009 | 671036600 |
| A11 | 671-0366-01 | B010505 | B010649 | CIRCUIT BD ASSY:TIME BASE DISPLAY | 80009 | 671036601 |
| A11 | 671-0366-02 | B010650 |  | CIRCUIT BD ASSY:TIME BASE (STANDARD) | 80009 | 671036602 |
| A11 | 671-0366-02 |  |  | CIRCUIT BD ASSY:TIME BASE (2440M) | 80009 | 671036602 |
| A12 | 670-9746-17 |  |  | CIRCUIT BD ASSY:PROCESSOR (STANDARD ONLY) | 80009 | 670974617 |
| A12 | 670-9746-25 |  |  | CIRCUIT BD ASSY:PROCESSOR (OPTION 05 ONLY) | 80009 | 670974625 |
| A13 | 671-0125-00 |  |  | CIRCUIT BD ASSY:SIDE | 80009 | 671012500 |
| A14 | 614-0752-00 |  |  | FRONT PNL ASSY:STANDARD (STANDARD) | 80009 | 614075200 |
| A14 | 614-0753-00 |  |  | FRONT PNL ASSY:TV OPT 05 (OPTION 05) | 80009 | 614075300 |
| A15 | 175-9270-01 |  |  | FLEX CKT ASSY:GPIB,POLYMIDE | 80009 | 175927001 |
| A16 | 670-9902-01 | B010100 | B012402 | CIRCUIT BD ASSY:LV PWR SPLY | 80009 | 670990201 |
| A16 | 670-9902-04 | B012403 | B012656 | CIRCUIT BD ASSY:LV POWER SUPPLY | 80009 | 670990204 |
| A16 | 670-9902-05 | B012657 | B013269 | CIRCUIT BD ASSY:LV POWER SUPPLY | 80009 | 670990205 |
| A16 | 670-9902-06 | B013270 | B013320 | CIRCUIT BD ASSY:LV POWER SUPPLY | 80009 | 670990206 |
| A16 | 670-9902-07 | B013321 |  | CIRCUIT BD ASSY:LV POWER SUPPLY (STANDARD ONLY) | 80009 | 670990207 |
| A16 | 670-9902-01 | B010100 | B010107 | CIRCUIT BD ASSY:LV PWR SPLY | 80009 | 670990201 |
| A16 | 670-9902-04 | B010108 | B010110 | CIRCUIT BD ASSY:LV POWER SUPPLY | 80009 | 670990204 |
| A16 | 670-9902-05 | B010111 | B010118 | CIRCUIT BD ASSY:LV POWER SUPPLY | 80009 | 670990205 |
| A16 | 670-9902-06 | B010118 | B010118 | CIRCUIT BD ASSY:LV POWER SUPPLY | 80009 | 670990206 |
| A16 | 670-9902-07 | B010119 |  | CIRCUIT BD ASSY:LV POWER SUPPLY (2440M ONLY) | 80009 | 670990207 |
| A17 | 670-9748-00 | B010100 | B012402 | CIRCUIT BD ASSY:HV POWER SPLY | 80009 | 670974800 |
| A17 | 670-9748-01 | B012403 | B012656 | CIRCUIT BD ASSY:HV POWER SUPPLY | 80009 | 670974801 |
| A17 | 670-9748-02 | B012657 | B013269 | CIRCUIT BD ASSY:HV POWER SUPPLY | 80009 | 670974802 |
| A17 | 670-9748-03 | B013269 | B013320 | CIRCUIT BD ASSY:HV POWER SUPPLY | 80009 | 670974803 |
| A17 | 670-9748-04 | B013321 |  | CIRCUIT BD ASSY:HV POWER SUPPLY (STANDARD ONLY) | 80009 | 670974804 |
| A17 | 670-9748-00 | B010100 | B010107 | CIRCUIT BD ASSY:HV POWER SPLY | 80009 | 670974800 |
| A17 | 670-9748-01 | B010108 | B010110 | CIRCUIT BD ASSY:HV POWER SUPPLY | 80009 | 670974801 |
| A17 | 670-9748-02 | B010111 | B010118 | CIRCUIT BD ASSY:HV POWER SUPPLY | 80009 | 670974802 |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mif. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A17 | 670-9748-03 | B010118 B010118 | CIRCUIT BD ASSY:HV POWER SUPPLY | 80009 | 670974803 |
| A17 | 670-9748-04 | B010119 | CIRCUIT BD ASSY:HV POWER SUPPLY (2440M ONLY) | 80009 | 670974804 |
| A18 | 670-7280-0 |  | CIRCUIT BD ASSY:SCALE ILLUM | 80009 | 670728000 |
| A30 | 671-0367-00 |  | CIRCUIT BD ASSY:CCD OUT | 80009 | 671036700 |
| A31 | 671-0367-00 |  | CIRCUIT BD ASSY:CCD OUT | 80009 | 671036700 |
| A32 | 671-0367-00 |  | CIRCUIT BD ASSY:CCD OUT | 80009 | 671036700 |
| АЗ3 | 671-0367-00 |  | CIRCUIT BD ASSY:CCD OUT | 80009 | 671036700 |


| Component Number | Tektronix Part No. | Effective | No. Dscont | Name \& Doscription | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A10 | 671-0365-00 | B010100 | B010185 | CIRCUT BD ASSY:MAIN | 80009 | 671036500 |
| A10 | 671-0365-02 | B010186 | B010825 | CIRCUIT BD ASSY:MAIN | 80009 | 671036502 |
| A10 | 671-0365-03 | B010826 |  | CIRCUIT BD ASSY:MAIN (STANDARD) | 80009 | 671036503 |
| A10 | 671-0365-03 |  |  | CIRCUIT BD ASSY:MAIN (2440M) | 80009 | 671036503 |
| A10AT300 | 119-2342-06 | B010100 | B010488 | ATTENUATOR,VAR:PROGRAMMABLE 1X-100X | 80009 | 119234206 |
| A10AT300 | 119-2342-08 | B010489 | B011594 | ATTENUATOR,VAR: $1 \mathrm{X}-100 \mathrm{X}, \mathrm{CHANNEL} 2$ | 80009 | 119234208 |
| A10AT300 | 119-2342-10 | B011595 |  | ATTENUATOR,VAR:1X-100X,CHANNEL 2 (2440 ONLY) | 80009 | 119234210 |
| A10AT300 | 119-2342-08 |  |  | ATTENUATOR,VAR: $1 \mathrm{X}-100 \mathrm{X}$, CHANNEL 2 (2440M ONLY) | 80009 | 119234208 |
| A10AT400 | 119-2342-05 | B010100 | B010488 | ATTENUATOR,VAR:PROGRAMMABLE 1X-100X | 80009 | 119234205 |
| A10AT400 | 119-2342-07 | B010589 | B011594 | ATTENUATOR,VAR: $1 \mathrm{X}-100 \mathrm{X}, \mathrm{CHANNEL} 1$ | 80009 | 119234207 |
| A10AT400 | 119-2342-09 | B011595 |  | ATTENUATOR,VAR:1X-100X,CHANNEL 1 ( 2440 ONLY) | 80009 | 119234209 |
| A10AT400 | 119-2342-07 |  |  | ATTENUATOR,VAR:1X-100X,CHANNEL 1 (2440M ONLY) | 80009 | 119234207 |
| A10C101 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C102 | 281-0786-00 |  |  | CAP,FXD,CERAMIC:MLC;150PF,10\%,100V | 04222 | SA101A151KAA |
| A10C110 | 290-0943-02 |  |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C111 | 290-0943-02 |  |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C112 | 290-0943-02 |  |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| Aloc120 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C122 | 290-0943-02 |  |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C140 | 290-0943-02 |  |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C141 | 290-0943-02 |  |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C142 | 290-0943-02 |  |  | CAP.FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C143 | 281-0798-0 |  |  | CAP,FXD,CER DI:51PF,1\%,100V | TK1743 | CGB510GEN |
| A10C144 | 281-0798-0 |  |  | CAP,FXD,CER DI:51PF,1\%,100V | TK1743 | CGB510GEN |
| A10C150 | 281-0909-0 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C160 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C161 | 290-0246-00 |  |  | CAP,FXD,TANT:DRY;3.3UF,10\%,15V | 12954 | D3R3EA15K1 |
| A10C162 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C169 | 290-0943-02 |  |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1 W344 | SME25VB47RM5X11 |
| A10C172 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C189 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C190 | 290-0943-02 |  |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C201 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SAt05C223MAA |
| A10C202 | 290-0943-02 |  |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C205 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C210 | 290-0943-02 |  |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |


| Component Number | Tektronix Part No. | Serial No. Effective Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A10C211 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| Al0C212 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C213 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C214 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC; $0.022 \mathrm{UF}, 20 \%, 50 \mathrm{~V}$ | 04222 | SA105C223MAA |
| A10C215 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X 11 |
| A10C216 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C220 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C222 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0,022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C223 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C225 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C230 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C231 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C232 | 281-0909-- |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C233 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C240 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C241 | 290-0246-00 |  | CAP,FXD,TANT:DRY;3.3UF,10\%,15V | 12954 | D3R3EA15K1 |
| A10C242 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C243 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C250 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| At0C257 | 281-0218-00 |  | CAP,VAR,CER DI:1-5PF, +2-2.5\%,100V | 59660 | 513-011A1-5 |
| A10C260 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C263 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C264 | 283-0203-00 |  | CAP,FXD,CER DI:0,47UF,20\%,50V | 04222 | SR305C474MAA |
| A10C265 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C272 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C280 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C281 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C282 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C283 | 281-0909- |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C287 | 281-0763-0 |  | CAP,FXD,CERAMIC:MLC;47PF, $10 \%, 100 \mathrm{~V}$ | 04222 | SA102A470KAA |
| A10C288 | 281-0763-00 |  | CAP,FXD,CERAMIC:MLC;47PF,10\%,100V | 04222 | SA102A470KAA |
| A10C290 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C311 | 281-0064-0 |  | CAP,VAR,PLASTIC:0.25-1.5PF,600V | 52769 | ER-530-013 |
| A10C316 | 281-0909-00 | B010250 | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C319 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C320 | 281-0909-00 | B010100 B010476 | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C321 | 281-0786-00 | B010557 | CAP,FXD,CERAMIC:MLC; 150 PF, $10 \%, 100 \mathrm{~V}$ (STANDARD) | 04222 | SA101A151KAA |
| A10C321 | 281-0786-00 |  | CAP,FXD,CERAMIC:MLC;150PF,10\%,100V (2440M) | 04222 | SA101A151KAA |
| A10C322 | 281-0909-00 | B010250 | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| А10С330 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |


| Component Number | Tektronix Part No. | Serial No. Effective Dscont | Name \& Description | Mfr. <br> Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A10C340 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C341 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C350 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C361 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C367 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C370 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C371 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C372 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C375 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C380 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C390 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C391 | 281-0798-00 |  | CAP,FXD,CER DI:51PF,1\%,100V | TK1743 | CGB510GEN |
| A10C410 | 283-0203-00 |  | CAP,FXD,CER DI:0.47UF,20\%,50V | 04222 | SR305C474MAA |
| A10C412 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C414 | 281-0064-00 |  | CAP,VAR,PLASTIC:0.25-1.5PF,600V | 52769 | ER-530-013 |
| A10C420 | 281-0909-00 | B010100 B010476 | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C421 | 281-0786-00 | B010557 | CAP,FXD,CERAMIC:MLC;150PF,10\%,100V (STANDARD) | 04222 | SA101A151KAA |
| A10C421 | 281-0786-0 |  | CAP,FXD,CERAMIC:MLC; 150 PF,10\%,100V (2440M) | 04222 | SA101A151KAA |
| A10C422 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C423 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C430 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C431 | 281-0093-0 |  | CAP,VAR,CER DI:5.5-18PF,350V | 33095 | 53-717-001 A5.5 |
| A10C432 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C440 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C441 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C456 | 281-0218-0 |  | CAP,VAR,CER DI: $1-5$ PF, $+2-2.5 \%, 100 \mathrm{~V}$ | 59660 | 513-011A1-5 |
| A10C462 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C463 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C464 | 283-0203-00 |  | CAP,FXD,CER DI:0,47UF,20\%,50V | 04222 | SR305C474MAA |
| A10C465 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C467 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C468 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C471 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C472 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C473 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C474 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C480 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1 W344 | SME25VB47RM5X11 |
| A10C481 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C483 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |

Replaceable Electrical Parts

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 CAP，FXD，MTLZD：0．47UF，10\％，50V



 CAP．FXD，MTLZD：0．47UF，10\％，50V





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| FWWEzzosolvs | こてご๐ |  |  | 00－6060－182 | 00sjolv |
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| Wrwezzosolvs | てくでロ |  |  | 00－6060－182 | z6t50ry |
| N3501s850 |  |  |  | 00－8620－182 | 16 tOOL |
| WWEzzosolvs | 己己でo | 109＇\％0z＇ปก |  | 00－6060－182 | 06t3oly |
| WWWEzzosolvs | こでヤ0 |  |  | 00－6060－182 | 88t5014 |
| buwezzosorvs | 己てzヤo |  |  | 00－6060－182 | p8bjolv |
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| Component Number | Tektronix Part No. | Seria Effective | No. Decont | Name \& Description | Mifr. Code | Mitr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A10C645 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C646 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C647 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C648 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C649 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C650 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C651 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0,47UF, $10 \%, 50 \mathrm{~V}$ | TK1913 | MKS 2 .47/50 |
| A10C652 | 290-0943-02 | B010186 | B010825 | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5 ${ }^{\text {P11 }}$ |
| A10C652 | 281-0909-00 | B010826 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V (STANDARD) | 04222 | SA105C223MAA |
| A10C652 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V (2440M) | 04222 | SA105C223MAA |
| A10C653 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C654 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0,022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C655 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C656 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C660 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C661 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C662 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C663 | 285-1362-00 |  |  | CAP,FXD,PLASTIC:560PF,2.5\%,100V | TK1913 | FKP2 560 PF 2.5 |
| A10C664 | 285-1362-0 |  |  | CAP,FXD,PLASTIC:560PF, $2.5 \%, 100 \mathrm{~V}$ | TK1913 | FKP2 560 PF 2.5 |
| A10C685 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C686 | 290-0943-02 |  |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A100690 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A100701 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C711 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A100730 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C731 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C732 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A100733 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C734 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C735 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0,47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A100740 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0.47UF, $10 \%, 50 \mathrm{~V}$ | TK1913 | MKS 2 .47/50 |
| A10C741 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A100742 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C743 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C744 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C745 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C746 | 281-0909-0 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C747 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C748 | 285-1301-01 |  |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |


| Component Number | Tektronix <br> Part No. | Serial No. Effective Dscont | Name \& Description | Mfr. Code | Mtr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A10C751 | 281-0814-00 |  | CAP,FXD,CERAMIC:MLC: $100 \mathrm{PF}, 10 \%, 100 \mathrm{~V}$ | TK1743 | CGB101KEN |
| A10C752 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C753 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C760 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C761 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C762 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C763 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A100765 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C768 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A100770 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C771 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C774 | 285-1362- |  | CAP,FXD,PLASTIC:560PF,2.5\%,100V | TK1913 | FKP2 560 PF 2.5 |
| A10C780 | 281-0909-0 |  | CAP.FXD.CERAMIC:MLC;0,022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C781 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0,022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C784 | 285-1362-00 |  | CAP,FXD,PLASTIC:560PF,2.5\%,100V | TK1913 | FKP2 560 PF 2.5 |
| A10C809 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C810 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C812 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C813 | 281-0763-00 |  | CAP,FXD,CERAMIC:MLC;47PF,10\%,100V | 04222 | SAi02A470KAA |
| A10C817 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C820 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C821 | 285-1301-01 |  | CAP,FXD,MTLZD:0,47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C822 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C823 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C824 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C825 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C826 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C830 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C832 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C834 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C835 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C840 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C843 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS $2.47 / 50$ |
| A10C844 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C850 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C851 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A10C870 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C872 | 285-1362-00 |  | CAP,FXD,PLASTIC:560PF,2.5\%,100V | TK1913 | FKP2 560 PF 2.5 |
| A10C880 | 281-0909-00 |  | CAP.FXD,CERAMIC:MLC;0.022UF;20\%,50V | 04222 | SA105C223MAA |
| A10C882 | 285-1362-00 |  | CAP,FXD,PLASTIC:560PF,2.5\%,100V | TK1913 | FKP2 560 PF 2.5 |


| Component Number | Tektronix Part No. | Serial No. Effective Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A10C950 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A10C951 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC; $0.022 \mathrm{UF}, 20 \%, 50 \mathrm{~V}$ | 04222 | SA105C223MAA |
| A10C955 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C956 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C957 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C958 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C960 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS $2.47 / 50$ |
| A10C961 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF.10\%,50V | TK1913 | MKS $2.47 / 50$ |
| A10C965 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C966 | 285-1301-01 |  | CAP,FXD,MTLZD:0.47UF,10\%,50V | TK1913 | MKS 2 .47/50 |
| A10C1005 | 283-0000-00 |  | CAP,FXD,CER DI:0.001UF, $+100-0 \%, 500 \mathrm{~V}$ | 51406 | DD06450Y5U102P5 |
| A10C1006 | 283-0000-0 |  | CAP,FXD,CER DI: $0.001 \mathrm{UF},+100-0 \%, 500 \mathrm{~V}$ | 51406 | DD06450Y5U102P5 |
| A10CR140 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST:40V, $150 \mathrm{MA,4NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A10CR141 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR220 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR221 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR222 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR223 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR224 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR225 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR226 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR227 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, 150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR228 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST; $40 \mathrm{~V}, 150 \mathrm{MA,4NS}$,2PF | 27014 | FDH9427 |
| A10CR270 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST; $40 \mathrm{~V}, 150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A10CR285 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR286 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR290 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR291 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR292 | 152-0951-00 |  | DIODE,SIG:SCHTKY;60V,2.25PF | 66958 | 1N6263 |
| A10CR310 | 152-0323-01 |  | DIODE,SIG:,550, 1,25VF,225MA,25PA,2.0PF | 14552 | MT5127 |
| A10CR311 | 152-0323-01 |  | DIODE,SIG:,;50V, 1.25VF,225MA,25PA,2.0PF | 14552 | MT5127 |
| A10CR392 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR410 | 152-0323-01 |  | DIODE,SIG:;50V, 1.25VF,225MA,25PA,2.0PF | 14552 | MT5127 |
| A10CR411 | 152-0323-01 |  | DIODE,SIG:;50V, $1.25 \mathrm{VF}, 225 \mathrm{MA}, 25 \mathrm{PA}, 2.0 \mathrm{PF}$ | 14552 | MT5127 |
| A10CR420 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR421 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR490 | 152-0951-00 |  | DIODE,SIG:SCHTKY; 60V,2.25PF | 66958 | 1N6263 |
| A10CR491 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, 150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR500 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR501 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mitr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A10CR502 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR503 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR521 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR530 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, $150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A10CR551 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR552 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR553 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, $150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A10CR580 | 152-0650-00 |  | DIODE,SIG:,WC;30V,2.3PF@C25,C3/25=5.25 | 50101 | U11-4101 |
| A10CR581 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST:40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR582 | 152-0650-00 |  | DIODE,SIG:,WC;30V,2.3PF@C25,C3/25=5.25 | 50101 | U11-4101 |
| A10CR590 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST:40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR591 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR600 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR601 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, $150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A10CR602 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR610 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR612 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR613 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR614 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR620 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR621 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR622 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR701 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, 150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR702 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR771 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, 150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR774 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR780 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR784 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR810 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR870 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| At0CR874 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, 150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR880 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10CR884 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A10J104 | 131-3176-00 |  | CONN,BOX:PCB,SIP; FEMALE,STR, 1 X 6,0.1 CTR | 00779 | 382440-1 |
| A10,105 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB;;MALE,STR (QUANTITY OF 7) | 22526 | 48283-018 |
| A10J106 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 2) | 22526 | 48283-018 |
| A103107 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 4) | 22526 | 48283-018 |
| A10.108 | 131-3152-0 |  | CONN,HDR:PCB,;MALE,STR, $2 \times 8,0.1$ CTR | 53387 | 2516-6002UB |


| Component Number | Tektronix <br> Part No. | Serial No. Effective Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A10.111 | 131-3181-00 |  | CONN,HDR:PCB,;MALE,RTANG, $2 \times 20,0.1$ CTR | 22526 | 69155-440R |
| A10J113 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 8) | 22526 | 48283-018 |
| A101114 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 4) | 22526 | 48283-018 |
| A10J135 | 131-0608-00 | B010186 | TERMINAL,PIN:PRESSFIT/PCB;;MALE,STR (STANDARD) | 22526 | 48283-018 |
| A10.135 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (2440M) | 22526 | 48283-018 |
| A10141 | 131-3182-0 |  | CONN,HDR:PCB,;MALE,RTANG, $2 \times 25,0.1$ CTR | 53387 | 2550-5002UB |
| A10J145 | 131-0608-0 | B010186 | TERMINAL,PIN:PRESSFIT/PCB;;MALE,STR (STANDARD) | 22526 | 48283-018 |
| A10J145 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (2440M) | 22526 | 48283-018 |
| A10J146 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 3) | 22526 | 48283-018 |
| A10J147 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB;;MALE,STR (QUANTITY OF 3) | 22526 | 48283-018 |
| A10,152 | 131-3152-00 |  | CONN,HDR:PCB,;MALE,STR, $2 \times 8,0.1$ CTR | 53387 | 2516-6002UB |
| A10,157 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A10」190 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,:MALE,STR (QUANTITY OF 12) | 22526 | 48283-018 |
| A10J191 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB;;MALE,STR (QUANTITY OF 3) | 22526 | 48283-018 |
| A101192 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 12) | 22526 | 48283-018 |
| Al0.J2001 | 131-0679-02 |  | CONN,RF RCPT:BNC,550 OHM,FEMALE,STR | TKO10 | BNC340-BR-1 |
| A10,2002 | 131-0679-02 |  | CONN,RF RCPT:BNC,;50 OHM,FEMALE,STR | TKO10 | BNC340-BR-1 |
| A10, 2004 | --------- |  | (PART OF A10AT400) |  |  |
| A10.J2005 | -------- |  | (PART OF A10AT300) |  |  |
| A10, 2006 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A10,2006 | 131-2716-01 |  | TERMINAL,CAL: | TK1163 | ORDER BY DESC |
| A10L120 | 108-0538-0 |  | COIL,RF:FIXED,2.7UH | O.JR03 | 108-0538-0 |
| A10L150 | 108-0538-00 |  | COIL,RF:FIXED,2.7UH | O.JR03 | 108-0538-00 |
| A10L200 | 108-0538-00 |  | COIL,RF:FIXED,2.7UH | OJR03 | 108-0538-00 |
| A10L210 | 108-0538-00 |  | COIL,RF:FIXED,2.7UH | O.JR03 | 108-0538-00 |
| A10L220 | 108-0538-00 |  | COIL,RF:FIXED,2.7UH | O.JR03 | 108-0538-00 |
| A10L250 | 108-1309-00 |  | COIL,RF:FXD,70NH,15\% | O.JR03 | 108-1309-00 |
| A10L260 | 108-0538-00 |  | COIL,RF:FIXED,2.7UH | O.RR03 | 108-0538-00 |
| A10L261 | 108-0538-00 |  | COIL,RF:FIXED,2.7UH | O.JR03 | 108-0538-00 |
| A10L270 | 108-0538-00 |  | COIL,RF:FIXED,2.7UH | 0.JR03 | 108-0538-00 |
| A10L332 | 108-0262-00 |  | COIL,RF:FIXED,505NH | O, R03 | 108-0262-00 |
| A10L340 | 108-0538-0 |  | COIL,RF:FIXED,2.7UH | OJR03 | 108-0538-00 |
| A10L431 | 114-0266-00 |  | COIL,RF:VARIABLE,370-575NH,FORM | O.JR03 | 114-0266-0 |



| Component Number | Tektronix Part No. | Serial No. Effective Dscont | Name \& Description | Mfr. <br> Code | Mr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A10Q251 | 151-0188-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A10Q270 | 151-0188-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A10Q271 | 151-0190-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA | 04713 | 2N3904 |
| A10Q287 | 151-0223-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;15V,500MA | 04713 | MPS2369A |
| A10Q288 | 151-0223-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;15V,500MA | 04713 | MPS2369A |
| A10Q290 | 151-0367-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;25V,30MA,1.0GHZ | 04713 | SPS 8811 |
| A10Q291 | 151-0367-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;25V,30MA,1.0GHZ | 04713 | SPS 8811 |
| A10Q356 | 151-0188-00 | B010250 | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A10Q372 | 151-0188-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A10Q375 | 151-0188-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A10Q380 | 151-0188-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A10Q390 | 151-0188-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A10Q391 | 151-0188-0 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A10Q392 | 151-0367-0 |  | TRANSISTOR,SIG:BIPOLAR,NPN;25V,30MA,1.0GHZ | 04713 | SPS 8811 |
| A10Q393 | 151-0192-05 |  | TRANSISTOR,SIG:BIPOLAR,NPN:25V,100MA | 04713 | SPS8801RLRP |
| A10Q446 | 151-0188-0 | B010250 | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A10Q450 | 151-0221-08 |  | TRANSISTOR,SIG:BIPOLAR,PNP;12V,80MA | 04713 | MPS4258RLRP |
| A10Q460 | 151-0221-08 |  | TRANSISTOR,SIG:BIPOLAR,PNP;12V,80MA | 04713 | MPS4258RLRP |
| A10Q490 | 151-0367-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;25V,30MA,1.0GHZ | 04713 | SPS 8811 |
| A10Q491 | 151-0188-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A10Q492 | 151-0188-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A10Q493 | 151-0188-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A10Q494 | 151-0188-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A10Q495 | 151-0192-05 |  | TRANSISTOR,SIG:BIPOLAR,NPN;25V,100MA | 04713 | SPS8801RLRP |
| A100530 | 151-0622-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,1.0A,50MHZ | 04713 | MPS6727 |
| A10Q540 | 151-0622-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V, 1.0A,50MHZ | 04713 | MPS6727 |
| A10Q551 | 151-0221-08 |  | TRANSISTOR,SIG:BIPOLAR,PNP;12V,80MA | 04713 | MPS4258RLRP |
| A10Q580 | 151-0622-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,1.0A,50MHZ | 04713 | MPS6727 |
| A10Q620 | 151-0622-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP:40V, 1.0A,50MHZ | 04713 | MPS6727 |
| A100621 | 151-0622-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,1.0A,50MHZ | 04713 | MPS6727 |
| A100630 | 151-0622-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,1.0A,50MHZ | 04713 | MPS6727 |
| A10Q640 | 151-0622-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,1.0A,50MHZ | 04713 | MPS6727 |
| A10Q660 | 151-0223-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;15V,500MA | 04713 | MPS2369A |
| A100670 | 151-0223-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;15V,500MA | 04713 | MPS2369A |
| A10Q770 | 151-0223-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;15V,500MA | 04713 | MPS2369A |
| A10Q771 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |
| A10Q772 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V, 100MA | 04713 | MPS6523RLRP |
| A10Q773 | 151-0223-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;15V,500MA | 04713 | MPS2369A |
| A10Q774 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |
| A10Q775 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |


| Component Number | Tektronix Part No. | Serial No. Effective Dscont | Name \& Description | Mifr. Code | Mitr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A100780 | 151-0223-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;15V,500MA | 04713 | MPS2369A |
| A100781 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |
| A100782 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |
| A10Q783 | 151-0223-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN:15V,500MA | 04713 | MPS2369A |
| A100784 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |
| A100785 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |
| A100810 | 151-0190-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA | 04713 | 2N3904 |
| A100870 | 151-0223-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;15V,500MA | 04713 | MPS2369A |
| A100871 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |
| A100872 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |
| A100873 | 151-0223-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;15V,500MA | 04713 | MPS2369A |
| A10Q874 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |
| A100875 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |
| A10Q880 | 151-0223-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;15V,500MA | 04713 | MPS2369A |
| A100881 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |
| A10Q882 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |
| A10Q883 | 151-0223-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN:15V,500MA | 04713 | MPS2369A |
| A100884 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |
| A10Q885 | 151-0216-04 |  | TRANSISTOR,SIG:BIPOLAR,PNP;25V,100MA | 04713 | MPS6523RLRP |
| A10Q970 | 151-0190-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA | 04713 | 2N3904 |
| A10Q980 | 151-0190-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA | 04713 | 2N3904 |
| A10R102 | 321-0657-07 |  | RES,FXD,FILM: 60 OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T9 | 57668 | RB14BZE 60E |
| A10R110 | 321-1700-04 |  | RES,FXD,FILM: 10.44 K OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T2 | 19701 | 5033RC10K440B |
| A10R111 | 315-0301-00 |  | RES,FXD,FILM:300 OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R112 | 315-0752-00 |  | RES,FXD,FILM:7.5K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R120 | 315-0562-00 |  | RES,FXD,FILM:5.6K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R121 | 308-0755-00 | B010100 B010174 | RES,FXD,WW:0.75 OHM,5\%,2W | 91637 | CPF-2-0R75JT |
| A10R121 | 308-0836-00 | B010175 | RES,FXD,WW:1.2 OHM,5\%,1W FUSIBLE | 11502 | SP-20F-1.2 OHM |
| A10R130 | 321-0275-0 |  | RES,FXD,FILM:7.15K OHM, 1\%,0.125W,TC=TO | 19701 | 5043ED7K150F |
| A10R131 | 321-0333-00 |  | RES, FXD,FILM:28.7K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CMF55116G28701F |
| A10R132 | 321-0085-00 |  | RES,FXD,FILM: 75 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-9 |
| A10R133 | 321-0275-00 |  | RES,FXD,FILM:7.15K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED7K150F |
| A10R134 | 315-0471-0 |  | RES,FXD,FILM:470 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R135 | 321-0287-00 |  | RES,FXD,FILM:9.53K OHM, 1\%,0.125W,TC= $=$ TO | 19701 | 5033ED9K530F |
| A10R136 | 315-0471-00 |  | RES,FXD,FILM:470 OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| Alor140 | 321-0193-00 |  | RES,FXD,FILM: 1 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-15t-1 |
| A10R141 | 321-0063-00 |  | RES,FXD,FILM:44.2 OHM, 0.5\%,0.125W,TC=T0 | 57668 | CRB14 FXE 44.2 |
| A10R142 | 315-0103-0 |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R143 | 321-0193-00 |  | RES,FXD,FILM: 1 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | TK1727 | MR25 2322-151-1 |
| A10R144 | 315-0180-0 |  | RES,FXD,FILM:18 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |


| Component Number | Toktronix Part No. | Serial Effective | No. Dscont | Name \& Description | Mfr. Code | Mitr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A10R145 | 315-0471-00 |  |  | RES,FXD,FILM:470 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R146 | 315-0272-0 |  |  | RES,FXD,FILM: 2.7 K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R150 | 315-0122-00 |  |  | RES,FXD,FILM:1.2K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R151 | 315-0750-00 |  |  | RES,FXD,FILM:75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R160 | 315-0750-00 |  |  | RES,FXD,FILM:75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R161 | 315-0750-00 |  |  | RES,FXD,FILM: 75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R162 | 315-0470-00 |  |  | RES,FXD,FILM:47 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R163 | 315-0102-00 |  |  | RES,FXD,FILM:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R165 | 315-0750-00 |  |  | RES,FXD,FILM: 75 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R170 | 315-0302-00 | B010100 | B010185 | RES,FXD,FILM:3K OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R171 | 315-0103-00 | 8010100 | B010185 | RES,FXD,FILM:10K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R171 | 313-1182-00 | B010186 |  | RES,FXD,FILM:1.8K OHM 5\%,0.2W (STANDARD) | 91637 | CCF501G18000J |
| A10R171 | 313-1182-00 |  |  | RES,FXD,FILM:1.8K OHM 5\%,0.2W (2440M) | 91637 | CCF501G18000J |
| A10R182 | 315-0560-00 |  |  | RES,FXD,FILM:56 OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R183 | 315-0102-00 |  |  | RES,FXD,FILM:1K OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R184 | 315-0181-00 |  |  | RES,FXD,FILM: 180 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R185 | 315-0390-00 |  |  | RES,FXD,FILM: 39 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R186 | 315-0181-00 |  |  | RES,FXD,FILM: 180 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R188 | 307-0546-00 |  |  | RES NTWK,FXD,Fl:5,75OHM,5\%,0.15W | 11236 | 750-61-R75 OR 7 |
| A10R201 | 315-0101-00 |  |  | RES,FXD,FILM: 100 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R202 | 315-0272-0 |  |  | RES,FXD,FILM:2.7K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R210 | 321-1700-04 |  |  | RES,FXD,FILM:10.44K OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T2 | 19701 | 5033 RC 10 K 440 B |
| A10R219 | 315-0101-0 |  |  | RES,FXD,FILM: 100 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R215 | 321-0054-0 |  |  | RES,FXD,FILM: 35.7 OHM $, 0.5 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-9 |
| A10R216 | 321-0122-0 |  |  | RES,FXD,FILM: 182 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CMF55116G182ROF |
| A10R220 | 301-0361-00 |  |  | RES,FXD,FILM:360 OHM, $5 \%, 0.5 \mathrm{~W}$ | 19701 | 5053CX360ROJ |
| A10R222 | 315-0121-00 |  |  | RES,FXD,FILM: 120 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R225 | 315-0471-00 |  |  | RES,FXD,FILM:470 OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R230 | 321-0310-00 |  |  | RES,FXD,FLLM:16.5K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043EDt6K50F |
| A10R231 | 321-0310-00 |  |  | RES,FXD,FILM:16.5K OHM, 1\%,0.125W,TC = TO | 19701 | 5043ED16K50F |
| A10R232 | 321-0252-00 |  |  | RES,FXD,FILM:4.12K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED4K120F |
| A10R233 | 311-2234-00 |  |  | RES,VAR,TRMR:CERMET;5K OHM,20\%,0.5W | TK2073 | GF06UT2 502 ML |
| A10R234 | 321-0062-00 |  |  | RES,FXD,FILM: 43.2 OHM, $0.5 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-9 |
| A10R235 | 321-0275-00 |  |  | RES,FXD,FILM:7,15K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED7K150F |
| A10R236 | 321-0310-00 |  |  | RES,FXD,FILM: 16.5 K OHM, 1\%,0.125W,TC= $=$ TO | 19701 | 5043ED16K50F |
| A10R237 | 321-0310-0 |  |  | RES,FXD,FILM:16.5K OHM, 1\%,0.125W,TC= T0 | 19701 | 5043ED16K50F |
| A10R238 | 315-0750-00 |  |  | RES,FXD,FILM: 75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R240 | 321-0139-00 |  |  | RES,FXD,FILM:274 OHM, 1\%,0.125W,TC=T0 | TK1727 | MR25 2322-151-2 |
| A10R241 | 321-0201-00 |  |  | RES,FXD,FILM:1.21 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ To | TK1727 | MR252322-151-1K |


| Component Number | Tektronix <br> Part No. | Serial No. Effective Dscont | Name \& Description | Mfr. Code | Mtr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A10R242 | 315-0750-0 |  | RES,FXD,FILM: 75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R243 | 315-0750-00 |  | RES,FXD,FILM: 75 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R244 | 321-0357-00 |  | RES,FXD,FILM: 51.1 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED51K10F |
| A10R245 | 315-0911-0 |  | RES,FXD,FILM:910 OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R250 | 315-0470-0 |  | RES,FXD,FILM: 47 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R251 | 315-0222-00 |  | RES,FXD,FILM:2.2K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R252 | 315-0750-0 |  | RES,FXD,FILM: 75 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R253 | 315-0750-0 |  | RES,FXD,FILM: 75 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R255 | 315-0750-00 |  | RES,FXD,FILM: 75 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R260 | 315-0750-00 |  | RES,FXD,FILM:75 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R261 | 315-0103-00 |  | RES,FXD,FILM: 10 K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R262 | 315-0101-00 |  | RES,FXD,FILM: 100 OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R263 | 311-2229-00 |  | RES,VAR,NONWW:TRMR, 250 OHM,20\%,0.5W | TK2073 | GF06UT2 251 ML |
| A10R265 | 313-1332-00 | B010186 | RES,FXD,FILM:3.3K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-33000J |
| A10R267 | 315-0912-00 |  | RES,FXD,FILM:9.1K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R268 | 315-0362-00 |  | RES,FXD,FILM:3.6K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R269 | 315-0103-00 |  | RES,FXD,FILM: 10 K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R270 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R271 | 315-0152-00 |  | RES,FXD,FILM:1.5K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R273 | 315-0102-00 |  | RES,FXD,FILM: 1 K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R274 | 315-0102-00 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R275 | 315-0560-00 |  | RES,FXD,FILM: 56 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R276 | 313-1102-00 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000J |
| A10R278 | 315-0750-00 |  | RES,FXD,FILM: 75 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| Al0R279 | 315-0750-0 |  | RES,FXD,FILM: 75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R280 | 315-0102-0 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R281 | 315-0470-00 |  | RES,FXD,FILM:47 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R282 | 315-0470-00 |  | RES,FXD,FILM: 47 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R283 | 322-3105-00 |  | RES,FXD:METAL FILM; 121 OHM, 1\%,0.2W | 91637 | CCF501G121ROF |
| A10R284 | 315-0750-0 |  | RES,FXD,FILM: 75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R285 | 307-0542-0 |  | RES NTWK, FXD, FI:(5) 10 K OHM, $5 \%, 0.125 \mathrm{~W}$ | 11236 | 750-61-R10K |
| A10R286 | 315-0560-0 |  | RES,FXD,FILM: 56 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R287 | 315-0560-0 |  | RES,FXD,FILM: 56 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R288 | 315-0560-0 |  | RES,FXD,FILM: $56 \mathrm{OHM}, 5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R289 | 315-0750-0 |  | RES,FXD,FILM: 75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R290 | 315-0102-00 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R291 | 315-0102-0 |  | RES,FXD,FILM: 1 K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R292 | 315-0151-0 |  | RES,FXD,FILM: $150 \mathrm{OHM}, 5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R293 | 315-0151-00 |  | RES,FXD,FILM: 150 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R294 | 315-0102-00 |  | RES,FXD,FILM:1K OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |


| Component Number | Tektronix Part No. | Effective | No. Dscont | Name a Description | Mir. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A10R295 | 315-0302-00 |  |  | RES,FXD,FILM:3K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R296 | 315-0152-0 |  |  | RES,FXD,FILM:1.5K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R297 | 315-0103-00 |  |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R298 | 315-0101-00 |  |  | RES,FXD,FILM:100 OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R299 | 315-0104-00 |  |  | RES,FXD,FILM:100K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| At0R320 | 321-0085-00 |  |  | RES,FXD,FILM: 75 OHM, 1\%,0.125W,TC = TO | TK1727 | MR25 2322-151-9 |
| A10R340 | 321-0143-00 |  |  | RES,FXD,FILM:301 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-3 |
| A10R341 | 322-3143-00 |  |  | RES,FXD,FILM:301 OHM, 1\%,0.2W,TC=TO | 91637 | CCF501G301ROF |
| A10R342 | 322-3143-00 |  |  | RES,FXD,FILM:301 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CCF501G301ROF |
| A10R343 | 321-0357-00 |  |  | RES,FXD,FILM:51.1K OHM, 1\%,0.125W,TC=TO | 19701 | 5043ED51K10F |
| A10R344 | 322-3143-00 |  |  | RES,FXD,FILM:301 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF501G301ROF |
| A10R345 | 322-3143-0 |  |  | RES,FXD,FILM:301 OHM, 1\%,0.2W,TC=T0 | 91637 | CCF501G301ROF |
| A10R346 | 311-2234-00 |  |  | RES,VAR,TRMR:CERMET; 5 K OHM, $20 \%, 0.5 \mathrm{~W}$ | TK2073 | GF06UT2 502 ML |
| A10R347 | 311-2234-0 |  |  | RES,VAR,TRMR:CERMET;5K OHM,20\%,0.5W | TK2073 | GF06UT2 502 M L |
| A10R348 | 311-2234- |  |  | RES,VAR,TRMR:CERMET; 5 K OHM, $20 \%, 0.5 \mathrm{~W}$ | TK2073 | GF06UT2 502 M L |
| A10R349 | 311-2234-0 |  |  | RES,VAR,TRMR:CERMET;5K OHM,20\%,0.5W | TK2073 | GF06UT2 502 M L |
| A10R353 | 315-0103-00 |  |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R354 | 315-0302-0 |  |  | RES,FXD,FILM:3K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R355 | 315-0302-0 |  |  | RES,FXD,FILM:3K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| AtOR356 | 311-2231-00 | B010100 | B010249 | RES,VAR,TRMR:CERMET;1K OHM,20\%,0.5W | TK2073 | GF06UT2 102 M L |
| A10R356 | 311-2234-00 | B010250 |  | RES,VAR,TRMR:CERMET:5K OHM,20\%,0.5W | TK2073 | GF06UT2 502 M L |
| A10R357 | 311-2234-00 |  |  | RES,VAR,TRMR:CERMET;5K OHM,20\%,0.5W | TK2073 | GF06UT2 502 ML |
| A10R358 | 311-2234-00 |  |  | RES,VAR,TRMR:CERMET;5K OHM,20\%,0.5W | TK2073 | GF06UT2 502 ML |
| A10R359 | 311-2234-00 |  |  | RES,VAR,TRMR:CERMET;5K OHM,20\%,0.5W | TK2073 | GF06UT2 502 M L |
| A10R361 | 315-0750-0 |  |  | RES,FXD,FILM:75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R368 | 315-0560-0 |  |  | RES,FXD,FILM: 56 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R370 | 307-0488-0 |  |  | RES NTWK,FXD,Fl: 5100 OHM, $20 \%, 0.75 \mathrm{~W}$ | 11236 | 750-61R100 OHM |
| A10R371 | 307-0546-0 |  |  | RES NTWK,FXD,Fl:5,750HM, 5\%,0.15W | 11236 | 750-61-R75 OR 7 |
| A10R372 | 315-0221-00 |  |  | RES,FXD,FILM:220 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R373 | 315-0103-00 |  |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R374 | 315-0103-00 |  |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R375 | 315-0221-00 |  |  | RES,FXD,FILM:220 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R376 | 315-0181-00 |  |  | RES,FXD,FLM: 180 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R377 | 315-0181-00 |  |  | RES,FXD,FILM:180 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R378 | 321-0385-00 | B010100 | B010185 | RES,FXD,FILM:100K OHM,1\%,0.125W,TC=T0 | 19701 | 5043ED100KOF |
| A10R378 | 322-3385-0 | 8010186 |  | RES,FXD:METAL FILM;100K OHM,1\%,0.2W (STANDARD) | 91637 | CCF501G10002F |
| A10R378 | 322-3385-00 | B010186 |  | RES,FXD:METAL FILM; 100 K OHM, $1 \%, 0.2 \mathrm{~W}$ (2440M) | 91637 | CCF501G10002F |
| A10R379 | 321-0385-00 | B010100 | B010185 | RES,FXD,FILM:100K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED100K0F |
| A10R379 | 322-3385-00 | B010186 |  | RES,FXD:METAL FILM; 100 K OHM, $1 \%, 0.2 W$ (STANDARD) | 91637 | CCF501G10002F |


| Component Number | Tektronix Part No. | Serial No. Effective Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
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| A10R379 | 322-3385-00 | B010186 | RES,FXD:METAL FILM; 100 K OHM,1\%,0.2W (2440M) | 91637 | CCF501G10002F |
| A10R380 | 315-0122-00 |  | RES,FXD,FILM:1.2K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R381 | 315-0362-00 |  | RES,FXD,FILM:3.6K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R382 | 315-0511-00 |  | RES,FXD,FILM:510 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R383 | 313-1511-00 |  | RES,FXD,FILM:510 OHM,5\%,0.2W | 91637 | CCF50-2-510ROJ |
| A10R384 | 315-0102-0 |  | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R385 | 315-0511-00 |  | RES,FXD,FILM:510 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R386 | 315-0121-00 |  | RES,FXD,FILM: 120 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R387 | 315-0222-00 |  | RES,FXD,FILM:2.2K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R389 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED10K00F |
| A10R390 | 315-0301-00 |  | RES,FXD,FILM:300 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R391 | 315-0390-0 |  | RES,FXD,FILM:39 OHM,5\%,0,25W | TK1727 | SFR25 2322-181 |
| A10R392 | 321-0450-0 |  | RES,FXD,FILM:475K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED475KOF |
| A10R393 | 315-0222-0 |  | RES,FXD,FILM:2.2K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R394 | 315-0302-00 |  | RES,FXD,FILM:3K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R395 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R396 | 315-0302-00 |  | RES,FXD,FILM:3K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R397 | 315-0152-00 |  | RES,FXD,FILM:1.5K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R398 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R399 | 315-0101-00 |  | RES,FXD,FILM:100 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R410 | 311-2229-00 |  | RES,VAR,NONWW:TRMR,250 OHM,20\%,0.5W | TK2073 | GF06UT2 251 M L |
| A10R420 | 315-0121-00 |  | RES,FXD,FILM: 120 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R425 | 315-0101-00 |  | RES,FXD,FILM: 100 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R430 | 321-0252-00 |  | RES,FXD,FILM:4.12K OHM,1\%,0.125W,TC=TO | 19701 | 5043ED4K120F |
| A10R431 | 311-2234-00 |  | RES,VAR,TRMR:CERMET; 5 K OHM,20\%,0.5W | TK2073 | GF06UT2 502 ML |
| A10R435 | 315-0911-00 |  | RES,FXD,FILM:910 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R436 | 311-2229-00 |  | RES,VAR,NONWW:TRMR,250 OHM,20\%,0.5W | TK2073 | GF06UT2 251 M L |
| A10R437 | 313-1332-00 | B010250 | RES,FXD,FILM:3.3K OHM,5\%,0.2W | 91637 | CCF50-2-33000.J |
| A10R438 | 313-1332-00 | B010250 | RES,FXD,FILM:3.3K OHM,5\%,0.2W | 91687 | CCF50-2-33000J |
| A10R440 | 321-0143-00 |  | RES,FXD,FILM:301 OHM, 1\%,0.125W, TC = T0 | TK1727 | MR25 2322-151-3 |
| A10R441 | 321-0357-00 |  | RES,FXD,FILM:51.1K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED51K10F |
| A10R442 | 311-2234-00 |  | RES,VAR,TRMR:CERMET;5K OHM,20\%,0.5W | TK2073 | GF06UT2 502 ML |
| A10R443 | 311-2234-00 |  | RES,VAR,TRMR:CERMET; 5 K OHM, $20 \%, 0.5 \mathrm{~W}$ | TK2073 | GF06UT2 502 ML |
| A10R444 | 311-2234-0 |  | RES,VAR,TRMR:CERMET; 5 K OHM, $20 \%, 0.5 \mathrm{~W}$ | TK2073 | GF06UT2 502 ML |
| A10R445 | 311-2234-00 |  | RES,VAR,TRMR:CERMET;5K OHM,20\%,0.5W | TK2073 | GF06UT2 502 ML |
| A10R446 | 311-2231-0 | B010100 B010249 | RES,VAR,TRMR:CERMET; 1 K OHM,20\%,0.5W | TK2073 | GF06UT2 102 M L |
| A10R446 | 311-2234-0 | B010250 | RES,VAR,TRMR:CERMET;5K OHM, $20 \%, 0.5 \mathrm{~W}$ | TK2073 | GFo6UT2 502 ML |
| A10R447 | 311-2234-00 |  | RES,VAR, TRMR:CERMET; 5 K OHM, $20 \%, 0.5 \mathrm{~W}$ | TK2073 | GF06UT2 502 ML |
| A10R448 | 311-2234-00 |  | RES,VAR, TRMR:CERMET;5K OHM,20\%,0.5W | TK2073 | GF06UT2 502 ML |
| A10R449 | 311-2234-00 |  | RES,VAR,TRMR:CERMET;5K OHM,20\%,0.5W | TK2073 | GF06UT2 502 ML |


| Component Number | Tektronix Part No. | Serial No. Effective Dscont | Name \& Description | Mfr. Code | Mirr. Part No. |
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| A10R452 | 315-0152-00 |  | RES,FXD,FILM:1.5K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R453 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R454 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R455 | 315-0471-00 |  | RES,FXD,FILM: 470 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R456 | 313-1471-00 |  | RES,FXD,FILM:470 OHM,5\%,0.2W | 91637 | CCF50-2-470ROJ |
| A10R461 | 315-0152-00 |  | RES,FXD,FILM:1.5K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R463 | 322-3252-00 |  |  | 91637 | CCF501G41200F |
| A10R464 | 322-3289-00 |  | RES,FXD:METAL FILM; 10 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50G10001F |
| A10R466 | 313-1683-00 | B010374 | RES,FXD,FILM: 68 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-68001J |
| A10R467 | 321-0385-00 |  | RES,FXD,FILM: 100 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED100K0F |
| A10R468 | 321-0385-00 |  | RES,FXD,FILM: 100 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19704 | 5043ED100KOF |
| A10R469 | 313-1102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.2W | 91637 | CCF50-2-10000 |
| A10R470 | 307-0488-00 |  | RES NTWK, FXD,F1:5 100 OHM, $20 \%, 0.75 \mathrm{~W}$ | 11236 | 750-61R100 OHM |
| A10R471 | 315-0101-00 |  | RES,FXD,FILM: 100 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R477 | 315-0750-0 |  | RES,FXD,FILM:75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R478 | 315-0750-0 |  | RES,FXD,FILM: 75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R479 | 313-1102-0 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000 |
| A10R480 | 315-0102-0 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R481 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R482 | 322-3105-00 |  | RES,FXD:METAL FILM:121 OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G121ROF |
| A10R483 | 315-0202-00 |  | RES,FXD,FILM:2K OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R484 | 315-0750-00 |  | RES,FXD,FILM: 75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R485 | 315-0750-00 |  | RES,FXD,FILM: 75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R486 | 315-0180-0 |  | RES,FXD,FILM:18 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R487 | 315-0180-00 |  | RES,FXD,FILM:18 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R488 | 315-0180-00 |  | RES,FXD,FILM: 18 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R489 | 321-0289-0 |  | RES,FXD,FILM: $10,0 \mathrm{~K}$ OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED10K00F |
| A10R490 | 315-0151-00 |  | RES,FXD,FILM: 150 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R491 | 315-0151-00 |  | RES,FXD,FILM: 150 OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R492 | 315-0104-00 |  | RES,FXD,FILM:100K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R493 | 321-0450-00 |  | RES,FXD,FILM:475K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043 ED 475 KOF |
| A10R494 | 315-0301-0 |  | RES,FXD,FILM:300 OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R495 | 315-0390-00 |  | RES,FXD,FILM:39 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R496 | 315-0222-00 |  | RES,FXD,FILM:2.2K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R497 | 315-0121-00 |  | RES,FXD,FILM: 120 OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R498 | 315-0222-0 |  | RES,FXD,FILM:2.2K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R499 | 315-0132-0 |  | RES,FXD,FILM:1.3K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R500 | 315-0101- |  | RES,FXD,FILM: 100 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R501 | 315-0101-0 |  | RES,FXD,FILM: 100 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R502 | 315-0272-0 |  | RES,FXD,FILM:2.7K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mtr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A10R510 | 315-0103-0 |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R512 | 301-0361-0 |  | RES,FXD,FILM:360 OHM,5\%,0.5W | 19701 | 5053CX360ROJ |
| A10R515 | 321-0054-0 |  | RES,FXD,FILM:35.7 OHM,0.5\%,0.125W,TC=T0 | TK1727 | MR25 2322-151-9 |
| A10R516 | 321-0122-00 |  | RES,FXD,FILM: $182 \mathrm{OHM}, 1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CMF55116G182ROF |
| A10R520 | 321-0130-00 |  | RES,FXD,FILM:221 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED221ROF |
| A10R522 | 313-1220-00 | B010250 | RES,FXD,FILM:22 OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-22R00J |
| A10R523 | 315-0220-00 |  | RES,FXD,FILM:22 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R525 | 311-2229-00 |  | RES,VAR,NONWW:TRMR, 250 OHM, $20 \%, 0.5 \mathrm{~W}$ | TK2073 | GF06UT2 251 ML |
| A10R530 | 315-0101-00 |  | RES,FXD,FILM: 100 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R531 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R532 | 315-0151-00 |  | RES,FXD,FILM:150 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R533 | 315-0472-00 |  | RES,FXD,FILM:4.7K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R534 | 315-0150-0 |  | RES,FXD,FILM: 15 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R535 | 321-0289-0 |  | RES,FXD,FILM:10.0K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED10K00F |
| A10R536 | 321-0328-00 |  | RES,FXD,FILM:25.5K OHM,1\%,0.125W,TC=T0 | 91637 | CMF55116G25501F |
| A10R541 | 321-0357-0 |  | RES,FXD,FILM:51.1K OHM,1\%,0.125W,TC=T0 | 19701 | 5043ED51K10F |
| A10R543 | 315-0750-00 |  | RES,FXD,FILM:75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R544 | 315-0750-0 |  | RES,FXD,FILM: 75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R545 | 321-0289-0 |  | RES,FXD,FILM:10.0K OHM,1\%,0.125W,TC=T0 | 19701 | 5043ED10K00F |
| A10R546 | 315-0472-0 |  | RES,FXD,FILM:4.7K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R547 | 315-0150-00 |  | RES,FXD,FILM:15 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R550 | 315-0681-00 |  | RES,FXD,FILM:680 OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R551 | 315-0151-00 |  | RES,FXD,FILM: 150 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R555 | 315-0102-00 |  | RES,FXD,FLLM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R556 | 315-0471-00 |  | RES,FXD,FILM:470 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R557 | 315-0152-00 |  | RES,FXD,FILM:1.5K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R558 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R564 | 313-1102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.2W | 91637 | CCF50-2-10000 J |
| A10R565 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED10K00F |
| A10R566 | 321-0260-00 |  | RES,FXD,FILM:4.99K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033ED4K990F |
| A10R567 | 322-3385-00 |  | RES,FXD:METAL FILM; $100 \mathrm{~K} \mathrm{OHM}, 1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10002F |
| A10R568 | 322-3385-00 |  | RES,FXD:METAL FILM; 100 K OHM,1\%,0.2W | 91637 | CCF501G10002F |
| A10R570 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R571 | 315-0750-00 |  | RES,FXD,FILM:75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R572 | 315-0750-0 |  | RES,FXD,FILM:75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R573 | 315-0750-0 |  | RES,FXD,FILM:75 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R574 | 315-0101-0 |  | RES,FXD,FILM:100 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R575 | 315-0101-0 |  | RES,FXD,FILM: 100 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R580 | 315-0132-0 |  | RES,FXD,FILM:1.3K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R581 | 315-0511-0 |  | RES,FXD,FILM:510 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |


| Component Number | Tektronix Part No. | Serlal No. Effective Dscont | Name \& Description | Mitr. Code | Mrr. Part No. |
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| A10R584 | 315-0511-00 |  | RES,FXD,FILM: 510 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R585 | 321-0318-00 |  | RES,FXD,FILM:20.0K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033ED20K00F |
| A10R586 | 321-0335-0 |  | RES,FXD,FILM: 30.1 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033RD30K12FB29 |
| A10R587 | 315-0103-0 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R588 | 315-0101-00 |  | RES,FXD,FILM:100 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R591 | 322-3172-00 |  | RES,FXD,FILM:604 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CCF501G604ROF |
| A10R592 | 315-0152-00 |  | RES,FXD,FILM:1.5K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R593 | 322-3172-0 |  | RES,FXD,FILM: 604 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF501G604ROF |
| A10R594 | 322-3172-00 |  | RES,FXD,FILM:604 OHM, 1\%,0.2W,TC = T0 | 91637 | CCF501G604ROF |
| A10R595 | 321-0289-00 |  | RES,FXD,FLLM:10,0K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED10K00F |
| A10R596 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED10K00F |
| A10R598 | 315-0152-00 |  | RES,FXD,FILM:1.5K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R599 | 322-3289-00 |  | RES,FXD:METAL FILM; 10 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50G10001F |
| A10R600 | 307-0706-00 |  | RES NTWK,FXD,FI:4,10K OHM, $2 \%, 0.2 \mathrm{~W}$ EA | 50139 | 2088103 |
| A10R601 | 307-0542-00 |  | RES NTWK,FXD,FI:(5) 10 K OHM, $5 \%, 0.125 \mathrm{~W}$ | 11236 | 750-61-R10K |
| A10R612 | 315-0471-00 |  | RES,FXD,FILM:470 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R613 | 315-0561-00 |  | RES,FXD,FILM:560 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R614 | 315-0391-00 |  | RES,FXD,FILM: 390 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| AtOR615 | 315-0103-0 |  | RES,FXD,FILM: 10 K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R622 | 307-0108-0 |  | RES,FXD,CMPSN: 6.8 OHM, $5 \%, 0.25 \mathrm{~W}$ | 50139 | CB68G5 |
| A10R623 | 315-0471-0 |  | RES,FXD,FILM:470 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R624 | 315-0561-00 |  | RES,FXD,FILM:560 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R625 | 315-0391-00 |  | RES,FXD,FILM: 390 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R626 | 321-0264-0 |  | RES,FXD,FILM:5.49K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED5K490F |
| A10R627 | 321-0264-00 |  | RES,FXD,FILM:5.49K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED5K490F |
| A10R628 | 321-0295-00 |  | RES,FXD,FILM:11.5K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED11K50F |
| A10R631 | 315-0151-00 |  | RES,FXD,FILM:150 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R632 | 315-0472-0 |  | RES,FXD,FILM:4.7K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R633 | 315-0150-0 |  | RES,FXD,FILM:15 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R634 | 321-0264-0 |  | RES,FXD,FILM:5.49K OHM,1\%,0.125W,TC=TO | 19701 | 5043ED5K490F |
| A10R635 | 321-0328-00 |  | RES,FXD,FILM:25.5K OHM,1\%,0.125W,TC=TO | 91637 | CMF55116G25501F |
| A10R636 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM,1\%,0.125W,TC=T0 | 19701 | 5043ED10K00F |
| A10R637 | 321-0289-00 |  | RES,FXD,FILM: 10.0 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED10K00F |
| A10R639 | 321-0260-00 |  | RES,FXD,FILM:4.99K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033ED4K990F |
| A10R640 | 321-0328-00 |  | RES,FXD,FILM:25.5K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CMF55116G25501F |
| A10R641 | 321-0328-00 |  | RES,FXD,FILM:25.5K OHM, 1\%,0.125W,TC= TO | 91637 | CMF55116G25501F |
| A10R642 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, 1\%,0.125W,TC= T0 | 19701 | 5043ED10K00F |
| Al0R643 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED10K00F |
| A10R646 | 315-0472-00 |  | RES,FXD,FILM:4.7K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R647 | 315-0150-00 |  | RES,FXD,FILM: 15 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A10R648 | 315-0153-00 |  | RES,FXD,FILM:15K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R649 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED10K00F |
| A10R650 | 313-1560-00 | B010826 | RES,FXD,FILM:56 OHM,5\%,0.2W (STANDARD) | 91637 | CCF50-2-56R00J |
| A10R650 | 313-1560-00 |  | RES,FXD,FILM:56 OHM,5\%,0.2W (2440M) | 91637 | CCF50-2-56R00J |
| A10R651 | 315-0151-00 |  | RES,FXD,FILM: 150 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R652 | 321-0344-00 |  | RES,FXD,FILM:37,4K OHM, 1\%,0,125W,TC = TO | 19701 | 5033ED 37K40F |
| A10R653 | 321-0289-00 |  | RES,FXD,FILM:10.OK OHM, 1\%,0.125W,TC = To | 19701 | 5043ED10K00F |
| A10R654 | 315-0102-00 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R655 | 321-0332-07 |  | RES,FXD,FILM:28.0K OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=\mathrm{T} 9$ | TK1727 | MPR24-2322-141 |
| A10R656 | 321-0926-07 |  | RES,FXD,FILM:4K OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=\mathrm{T} 9$ | TK1727 | MPR24-2322-141 |
| A10R660 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R661 | 321-0289-00 |  | RES,FXD,FILM: 10.0 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED10K00F |
| A10R662 | 321-0289-00 |  | RES,FXD,FILM: 10.0 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED10K00F |
| A10R663 | 321-0155-00 |  | RES,FXD,FILM: 402 OHM, 1\%,0,125W,TC = TO | TK1727 | MR25 2322-151-4 |
| A10R664 | 321-0155-00 |  | RES,FXD,FILM: $402 \mathrm{OHM}, 1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-4 |
| A10R665 | 321-0128-00 |  | RES,FXD,FILM:210 OHM, $1 \%, 0,125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-2 |
| A10R666 | 313-1682-00 |  | RES,FXD,FILM:6.8K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-68000 J |
| A10R667 | 313-1202-00 |  | RES,FXD,FILM: 2 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-20000J |
| A10R668 | 313-1102-00 |  | FES,FXD,FILM:1K OHM,5\%,0.2W | 91637 | CCF50-2-10000J |
| A10R669 | 313-1202-00 |  | RES,FXD,FILM:2K OHM,5\%,0,2W | 91637 | CCF50-2-20000 J |
| A10R670 | 313-1750-00 |  | RES,FXD,FILM: 75 OHM,5\%,0.2W | 91637 | CCF50-2-75R00J |
| A10R671 | 313-1102-00 |  | RES,FXD,FILM:1K OHM, 5\%,0.2W | 91637 | CCF50-2-10000J |
| A10R672 | 313-1202-00 |  | RES,FXD,FILM:2K OHM,5\%,0.2W | 91637 | CCF50-2-20000J |
| A10R673 | 313-1102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.2W | 91637 | CCF50-2-10000 J |
| A10R674 | 313-1202-00 |  | RES,FXD,FILM:2K OHM,5\%,0.2W | 91637 | CCF50-2-20000J |
| A10R675 | 322-3126-00 |  | RES,FXD,FILM:200 OHM, 1\%,0.2W, TC = To | 91637 | CCF501G200ROF |
| A10R676 | 313-1202-00 |  | RES,FXD,FILM: 2 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-20000 J |
| A10R677 | 313-1102-00 |  | RES,FXD,FILM: 1 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000 J |
| A10R678 | 313-1202-00 |  | RES,FXD,FILM:2K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-20000J |
| A10R680 | 313-1202-00 |  | RES,FXD,FILM:2K OHM,5\%,0.2W | 91637 | CCF50-2-20000 J |
| A10R681 | 322-3126-00 |  | RES,FXD,FILM:200 OHM, 1\%,0.2W,TC = TO | 91637 | CCF501G200ROF |
| A10R682 | 313-1202-00 |  | RES,FXD,FILM:2K OHM,5\%,0.2W | 91637 | CCF50-2-20000J |
| A10R683 | 322-3210-00 | B010100 B010373 | RES,FXD:METAL FILM;1.5K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G15000F |
| A10R683 | 322-3216-00 | B010374 | RES,FXD,FILM 1.74 K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF501G17400F |
| A10R684 | 313-1102-00 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000 J |
| A10R685 | 313-1202-00 |  | RES,FXD,FILM:2K OHM,5\%,0.2W | 91637 | CCF50-2-20000J |
| A10R686 | 313-1202-00 |  | RES,FXD,FILM: 2 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-20000 |
| A10R687 | 321-0239-00 |  | RES,FXD,FILM:3.01K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | 2322-151-3KO1 |
| A10R690 | 322-3172-00 |  | RES,FXD,FILM: $604 \mathrm{OHM}, 1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF501G604ROF |


| Component Number | Tektronix <br> Part No. | Serial Effective | No. Dscont | Name \& Description | Mfr. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A10R700 | 315-0101-00 |  |  | RES,FXD,FILM: 100 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R710 | 307-0446-00 |  |  | RES NTWK,FXD,Fl:10K OHM, $20 \%$,(9)RES | 11236 | 750-101-R10K |
| A10R726 | 321-0295-00 |  |  | RES,FXD,FILM: 11.5 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED11K50F |
| A10R730 | 321-0264-00 |  |  | RES,FXD,FILM:5.49K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED5K490F |
| A10R731 | 321-0295-00 |  |  | RES,FXD,FILM:11.5K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ To | 19701 | 5043ED11K50F |
| A10R732 | 321-0295-00 |  |  | RES,FXD,FILM: 11.5 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED11K50F |
| A10R734 | 321-0289-0 |  |  | RES,FXD,FILM:10.0K OHM, 1\%,0.125W,TC = TO | 19701 | 5043ED10K00F |
| A10R735 | 321-0260-00 |  |  | RES,FXD,FILM:4.99K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033ED4K990F |
| A10R736 | 321-0289-00 |  |  | RES,FXD,FILM: 10.0 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043EDTOK00F |
| A10R740 | 321-0311-00 |  |  | RES,FXD,FILM: 16.9 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED16K90F |
| A10R741 | 321-0289-00 |  |  | RES,FXD,FILM:10.0K OHM. $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED10K00F |
| A10R742 | 321-0289-00 |  |  | RES,FXD,FILM: 10.0 K OHM, $1 \%, 0,125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED10K00F |
| A10R743 | 321-0289-00 |  |  | RES,FXD,FILM: $10.0 \mathrm{KOHM}, 1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED10K00F |
| A10R750 | 315-0153-00 |  |  | RES,FXD,FILM: 15 K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R751 | 321-0344-00 |  |  | RES,FXD,FILM: 37.4 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033ED 37K40F |
| A10R752 | 321-0289-0 |  |  | RES,FXD,FILM:10.0K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED10K00F |
| A10R753 | 321-0289-0 |  |  | RES,FXD,FILM: 10.0 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED10K00F |
| A10R760 | 315-0753-00 |  |  | RES,FXD,FILM: 75 K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R761 | 321-0296-00 |  |  | RES,FXD,FILM: 11.8 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED11K80F |
| A10R762 | 321-0193-00 | B011392 |  | RES,FXD,FILM: 1 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-1 |
| A10R763 | 321-0210-00 |  |  | RES,FXD,FILM: 1.50 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033ED1K50F |
| A10R764 | 321-0282-00 | B010100 | B011391 | RES,FXD,FILM: 8.45 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED8K450F |
| A10R764 | 321-0277-00 | B011392 |  | RES,FXD,FILM: 7.50 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED7K500F |
| A10R766 | 313-1102-00 |  |  | RES,FXD.FILM:1K OHM $, 5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000 |
| A10R771 | 322-3210-00 | B010100 | B010373 | RES,FXD:METAL FILM: 1.5 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G15000F |
| A10R771 | 322-3216-00 | B010374 |  | RES,FXD,FILM: 1.74 K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF501G17400F |
| A10R772 | 322-3126-00 |  |  | RES,FXD,FILM:200 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF501G200ROF |
| A10R773 | 313-1202-00 |  |  | RES,FXD,FILM:2K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-20000 |
| A10R774 | 322-3126-00 |  |  | RES,FXD,FILM:200 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF501G200ROF |
| A10R775 | 322-3210-00 | B010100 | $B 010373$ | RES,FXD:METAL FILM; 1.5 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G15000F |
| A10R775 | 322-3216-00 | B010374 |  | RES,FXD,FILM:1.74K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF501G17400F |
| A10R777 | 313-1102-00 |  |  | RES,FXD,FILM: 1 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000 J |
| A10R778 | 313-1102-00 |  |  | RES,FXD,FILM:1K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000 J |
| A10R779 | 313-1202-0 |  |  | RES,FXD,FILM:2K OHM, 5\%,0.2W | 91637 | CCF50-2-20000J |
| A10R781 | 322-3210-0 | B010100 | B010373 | RES,FXD:METAL FILM; 1.5 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G15000F |
| A10R781 | 322-3216-0 | B010374 |  | RES,FXD,FILM: 1.74 K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF501G17400F |
| A10R782 | 322-3126-0 |  |  | RES,FXD,FILM: 200 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CCF501G200ROF |
| A10R783 | 313-1202-00 |  |  | RES,FXD,FILM: 2 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-20000 |
| A10R784 | 322-3126-00 |  |  | RES,FXD,FILM: 200 OHM, $1 \%, 0.2 W, T C=$ TO | 91637 | CCF501G200ROF |
| A10R785 | 313-1202-00 |  |  | RES,FXD,FILM:2K OHM, 5\%,0.2W | 91637 | CCF50-2-20000. |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A10R786 | 313-1202-00 |  | RES,FXD,FILM:2K OHM,5\%,0.2W | 91637 | CCF50-2-20000. |
| A10R788 | 313-1202-00 |  | RES,FXD,FILM:2K OHM,5\%,0.2W | 91637 | CCF50-2-20000J |
| A10R789 | 313-1202-00 |  | RES,FXD.FILM:2K OHM,5\%,0.2W | 91637 | CCF50-2-20000 |
| A10R790 | 313-1750-00 |  | RES,FXD,FILM:75 OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-75ROO |
| A10R800 | 315-0102-00 |  | RES,FXD,FILM: 1 K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R809 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R810 | 307-0706-00 |  | RES NTWK,FXD,Fl:4,10K OHM, 2\%,0.2W EA | 50139 | $208 \mathrm{B103}$ |
| A10R811 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R812 | 321-0148-00 |  | RES,FXD,FILM: 340 OHM, 1\%,0.125W,TC $=$ T0 | TK1727 | MR25 2322-151-3 |
| A10R813 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R814 | 321-0296-00 |  | RES,FXD,FILM:11.8K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ To | 19701 | 5043ED11K80F |
| A10R815 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, 1\%,0.125W,TC=TO | 19701 | 5043ED10K00F |
| A10R816 | 321-0311-00 |  | RES,FXD.FILM:16.9K OHM, 1\%,0.125W,TC = TO | 19701 | 5043ED16K90F |
| A10R817 | 315-0101-00 |  | RES,FXD,FILM: 100 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R818 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, 1\%,0.125W,TC=TO | 19701 | 5043ED10K00F |
| A10R820 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R821 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R822 | 315-0102-00 |  | RES,FXD,FILM:1K OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R823 | 315-0101-00 |  | RES,FXD,FILM: 100 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R824 | 315-0912-0 |  | RES,FXD,FILM:9.1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R825 | 315-0103-0 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R828 | 315-0103-0 |  | RES,FXD,FILM: 10 K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R830 | 321-0289-00 |  | RES,FXD,FILM: 10.0 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED10K00F |
| A10R831 | 321-0289-00 |  | RES,FXD,FILM: 10.0 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED10K00F |
| A10R832 | 321-0311-00 |  | RES,FXD,FILM:16.9K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED16K90F |
| A10R833 | 321-0311-00 |  | RES,FXD,FILM:16.9K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED16K90F |
| A10R840 | 321-0311-00 |  | RES,FXD,FILM: 16.9 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED16K90F |
| A10R841 | 321-0289-00 |  | RES,FXD,FILM: 10.0 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED10K00F |
| A10R850 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R851 | 315-0102-0 |  | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R852 | 315-0102- |  | RES,FXD,FILM:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R853 | 315-0102-0 |  | RES,FXD,FILM: 1 K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R855 | 315-0103-00 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R856 | 315-0103-00 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R857 | 315-0103-00 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R860 | 315-0123-00 |  | RES,FXD,FILM:12K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R861 | 322-3164-00 |  | RES,FXD,FILM: 499 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF501G499ROF |
| A10R863 | 313-1102-00 |  | RES,FXD,FILM: 1 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000 J |
| A10R868 | 315-0102-00 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| Al0R871 | 322-3210-0 | B010100 B010373 | RES,FXD:METAL FILM; 1.5 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G15000F |


| Component Number | Tektronix Part No. | Serlal Effective | No. Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A10R871 | 322-3216-00 | B010374 |  | RES,FXD,FILM:1.74K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CCF501G17400F |
| A10R872 | 322-3126-00 |  |  | RES,FXD,FILM:200 OHM, 1\%,0.2W,TC=T0 | 91637 | CCF501G200ROF |
| A10R873 | 322-3210-00 | B010100 | 8010373 | RES,FXD:METAL FILM; 1.5K OHM,1\%,0.2W | 91637 | CCF501G15000F |
| A10R873 | 322-3216-00 | B010374 |  | RES,FXD,FILM:1.74K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF501G17400F |
| A10R875 | 313-1102-0 |  |  | RES,FXD,FILM:1K OHM,5\%,0.2W | 91637 | CCF50-2-10000J |
| A10R879 | 313-1202-00 |  |  | RES,FXD,FILM:2K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-20000J |
| A10R881 | 322-3210-00 | B010100 | B010373 | RES,FXD:METAL FILM:1.5K OHM,1\%,0.2W | 91637 | CCF501G15000F |
| A10R881 | 322-3216-0 | B010374 |  | RES,FXD,FILM:1.74K OHM,1\%,0.2W,TC = To | 91637 | CCF501G17400F |
| A10R882 | 322-3126-0 |  |  | RES,FXD,FLM: 200 OHM, 1\%,0.2W,TC=T0 | 91637 | CCF501G200ROF |
| A10R883 | 322-3210-00 | B010100 | B010373 | RES,FXD:METAL FILM;1.5K OHM,1\%,0.2W | 91637 | CCF501G15000F |
| A10R883 | 322-3216-00 | B010374 |  | RES,FXD,FILM:1.74K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF501G17400F |
| A10R884 | 313-1102-00 |  |  | RES,FXD,FILM:1K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000J |
| A10R885 | 313-1202-00 |  |  | RES,FXD,FILM:2K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-20000J |
| A10R891 | 313-1202-00 |  |  | RES,FXD,FILM:2K OHM,5\%,0.2W | 91637 | CCF50-2-20000 J |
| A10R950 | 322-3289-00 |  |  | RES,FXD:METAL FILM:10K OHM, $1 \%, 0.2 W$ | 91637 | CCF50G10001F |
| A10R951 | 322-3311-00 |  |  | RES,FXD,FILM:16.9K OHM, 1\%,0.2W,TC= To | 56845 | CCF-50-2-1692F |
| A10R952 | 322-3311-00 |  |  | RES,FXD,FILM:16.9K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 56845 | CCF-50-2-1692F |
| A10R953 | 322-3289-0 |  |  | RES,FXD:METAL FILM; 10 K OHM, 1\%,0.2W | 91637 | CCF50G10001F |
| A10R954 | 322-3289-00 |  |  | RES,FXD:METAL FILM; $10 \mathrm{~K} \mathrm{OHM}, 1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50G10001F |
| A10R955 | 322-3311-0 |  |  | RES,FXD,FILM:16.9K OHM. $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 56845 | CCF-50-2-1692F |
| A10R956 | 322-3289-0 |  |  | RES,FXD:METAL FILM: 10 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50G10001F |
| A10R957 | 322-3311-- |  |  | RES,FXD,FILM:16.9K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ T0 | 56845 | CCF-50-2-1692F |
| A10R1001 | 315-0240-00 |  |  | RES,FXD,FILM:24 OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R1002 | 315-0101-00 |  |  | RES,FXD,FILM: 100 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R1003 | 315-0240-00 |  |  | RES,FXD,FILM: 24 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R1004 | 315-0101-00 |  |  | RES,FXD,FILM: 100 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10R1005 | 315-0474-00 |  |  | RES,FXD,FILM:470K OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A10R1006 | 315-0474-00 |  |  | RES,FXD,FILM:470K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A10S600 | 260-1421-00 |  |  | SWITCH,PUSH:1 BTN, 2 POLE,INSTRUMENT ID | 71590 | 2KAA010000512 |
| A10S800 | 260-1421-00 |  |  | SWITCH,PUSH:1 BTN, 2 POLE,INSTRUMENT ID | 71590 | $2 \mathrm{KAA010000512}$ |
| A10S801 | 260-1421-0 |  |  | SWITCH,PUSH:1 BTN, 2 POLE,INSTRUMENT ID | 71590 | $2 \mathrm{KAA010000512}$ |
| А10т370 | 120-0478-0 |  |  | XFMR,TOROID: 5 TURNS,BIFILAR | OJR03 | 120-0478-00 |
| A10T371 | 120-0478- |  |  | XFMR,TOROID: 5 TURNS,BIFILAR | OJR03 | 120-0478-0 |
| A10TP163 | 131-0608- |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A10TP173 | 131-0608-0 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A10TP174 | 131-0608-0 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A10TP231 | 131-0608-- |  |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A10TP281 | 131-0608-0 |  |  | TERMINAL,PIN:PRESSFIT/PCB,MALE,STR | 22526 | 48283-018 |
| A10TP284 | 131-0608-0 |  |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A10TP288 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB;;MALE,STR | 22526 | 48283-018 |


| Component Number | Tektronix <br> Part No. | Serial <br> Effective | No. Dscont | Name \& Description | Mtr. <br> Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A10TP291 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A10TP370 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A10TP568 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A10TP581 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,MALE,STR | 22526 | 48283-018 |
| A10TP585 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,MMALE,STR | 22526 | 48283-018 |
| A10TP612 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A10TP650 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A10TP660 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A10TP832 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A10U100 | 155-0238-00 |  |  | MICROCKT,LINEAR:TRIGGER PREAMP | 80009 | 155023800 |
| A10U120 | 156-1149-01 |  |  | IC,LINEAR:BIFET,OP-AMP | 27014 | LF351N |
| A10U140 | 156-0651-0 |  |  | IC,DIGITAL:LSTTL,SHIFT REGISTER | 01295 | SN74LS164N |
| A10U150 | 155-0239-02 |  |  | MICROCKT,LINEAR:TRIGGER | 80009 | 155023902 |
| A10U190 | 156-1663-0 |  |  | IC,DIGITAL:FTTL,GATE;TRIPLE 3-INPUT | 04713 | MC74F11N |
| A10U220 | 156-1245-0 |  |  | IC,LINEAR:BIPOLAR, TRANSISTOR ARRAY | 0СVK3 | ULN2003A |
| A10U221 | 156-0651-00 |  |  | IC,DIGITAL:LSTTL,SHIFT REGISTER | 01295 | SN74LS164N |
| A10U230 | 156-0158-07 |  |  | IC,LINEAR:BIPOLAR,OP - AMP | 01295 | MC1458P |
| A10U270 | 156-0651-00 |  |  | IC,DIGITAL:LSTTL,SHIFT REGISTER | 01295 | SN74LS164N |
| A10U271 | 156-0469-00 |  |  | IC,DIGITAL:LSTTL,DEMUX/DECODER | 01295 | SN74LS138 |
| A10U272 | 156-0874-02 |  |  | IC,DIGITAL:LSTTL,LATCH | 04713 | SN74LS259N |
| A10U280 | 156-0383-00 |  |  | IC,DIGITAL:LSTTL,GATES | 01295 | SN74LS02N |
| A10U320 | 165-2235-02 |  |  | MICROCKT,HYBRID:ASSEMBLED LOW NOISE | 80009 | 165223502 |
| A10U340 | -------- |  |  | MICROCKT,HYBRID:PK DETECTOR ASSY |  |  |
| A10U350 | -------- | B010100 | B010999 | MICROCKT,HYBRID:DRIVER/CCD ASSY |  |  |
| A10U350 |  | B011000 |  | MICROCKT,HYBRID:CCD DRIVER ASSY |  |  |
| A10U360 | 156-1191-01 |  |  | IC,LINEAR:BIFET,OP-AMP;6MV VOS | 01295 | TLO72ACP |
| A10U370 | 230-0028-50 |  |  | WAFER,SILICON:TRIGGER LOGIC ARRAY | 80009 | 230002850 |
| A10U380 | 156-2290-00 |  |  | IC,DIGITAL:ECL, TRANSLATOR | 04713 | MC10H125P |
| A10U381 | 156-0518-00 |  |  | IC,LINEAR:ECL,MISC;PHASE-FREQUENCY | 04713 | MC12040(P OR L) |
| A10U390 | 156-1126-01 |  |  | IC,LINEAR:BIPOLAR,COMPARATOR | 01295 | LM311P |
| A10U420 | 165-2235-02 |  |  | MICROCKT,HYBRID:ASSEMBLED LOW NOISE | 80009 | 165223502 |
| A10U440 | --------- |  |  | MICROCKT,HYBRID:PK DETECTOR ASSY |  |  |
| A10U450 | -------- | B010100 | B010999 | MICROCKT,HYBRID:DRIVER/CCD ASSY |  |  |
| A10U450 | -------- | B011000 |  | MICROCKT,HYBRID:CCD DRIVER ASSY |  |  |
| A10U460 | 156-1191-01 |  |  | IC,LINEAR:BIFET,OP-AMP;GMV VOS | 01295 | TL072ACP |
| A10U470 | 230-0027-50 |  |  | INTERGRATED CKT;PHASE CLOCK ARRAY | 80009 | 230002750 |
| A10U490 | 156-1126-01 |  |  | IC,LINEAR:BIPOLAR,COMPARATOR | 01295 | LM311P |
| A10U510 | 156-1245-00 |  |  | IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY | 0CVK3 | ULN2003A |
| A10U511 | 156-0651-0 |  |  | IC,DIGITAL:LSTTL,SHIFT REGISTER | 01295 | SN74LS164N |
| A10U520 | 156-1245-0 |  |  | IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY | оСVК3 | ULN2003A |


| Component Number | Tektronix <br> Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A10U530 | 156-0651-00 |  | IC,DIGITAL:LSTTL,SHIFT REGISTER | 01295 | SN74LS164N |
| A10U540 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL074CN |
| A10U560 | 156-1303-00 |  | IC,MISC:DMOS,ANALOG SWITCH | ONOKO | SD5000N |
| AlOU570 | 156-1303-00 |  | IC,MISC:DMOS,ANALOG SWITCH | ONOKO | SD5000N |
| At0U580 | 156-0158-07 |  | IC,LINEAR:BIPOLAR,OP-AMP | 01295 | MC1458P |
| At0U590 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL074CN |
| A10U600 | 156-0513-03 |  | IC,MISC:CMOS,ANALOG MUX | 04713 | MC14051BCP |
| A10U610 | 165-2024-0 |  | MICROCKT,HYBRID:CURSOR AMPLIFIER | 80009 | 165202400 |
| A10U630 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL074CN |
| A10U631 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL074CN |
| A10U640 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL074CN |
| AloU641 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL074CN |
| A10U650 | 156-1492-0 |  | IC,LINEAR:BIFET,OP-AMP | 24355 | AD542.JH |
| A10U651 | 156-0513-03 |  | IC,MISC:CMOS,ANALOG MUX | 04713 | MC14051BCP |
| A10U660 | 156-1492-0 |  | IC,LINEAR:BIFET,OP-AMP | 24355 | AD542JH |
| A10U661 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL074CN |
| A10U700 | 156-0789-00 |  | IC,DIGITAL:LSTTL,SHIFT REGISTER | 01295 | SN74LS165N |
| A10U770 | 156-1272-00 |  | IC,LINEAR:BIPOLAR,OP-AMP | 01295 | NE5532P |
| A10U780 | 156-1272-00 |  | IC,LINEAR:BIPOLAR,OP-AMP | 01295 | NE5532P |
| A10U810 | 156-1191-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL072ACP |
| A10U819 | 156-0513-03 |  | IC.MISC:CMOS,ANALOG MUX | 04713 | MC14051BCP |
| A10U812 | 156-0048-00 |  | IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY | 04713 | MC3346P |
| A10U820 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL074CN |
| A10U821 | 156-0513-03 |  | IC,MISC:CMOS,ANALOG MUX | 04713 | MC14051BCP |
| A10U830 | 156-0513-03 |  | IC,MISC:CMOS,ANALOG MUX | 04713 | MC14051BCP |
| A10U831 | 156-0513-03 |  | IC,MISC:CMOS,ANALOG MUX | 04713 | MC14051BCP |
| A10U840 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL074CN |
| A10U841 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL074CN |
| A10U850 | 156-0651-00 |  | IC,DIGITAL:LSTTL,SHIFT REGISTER | 01295 | SN74LS164N |
| A10U851 | 156-0651-00 |  | IC,DIGITAL:LSTTL,SHIFT REGISTER | 01295 | SN74LS164N |
| A10U860 | 156-1589-00 |  | IC,CONVERTER:BIPOLAR,D/A;12 BIT,CURRENT | 24355 | DAC312-040P |
| A10U861 | 156-1200-01 |  | IC,LINEAR:BIFET,OP - AMP | 01295 | TL074CN |
| A10U870 | 156-1272-0 |  | IC,LINEAR:BIPOLAR,OP-AMP;DUAL,HIGH OUTPUT | 01295 | NE5532P |
| A10U880 | 156-1272-0 |  | IC,LINEAR:BIPOLAR,OP-AMP;DUAL,HIGH OUTPUT | 01295 | NE5532P |
| A10U950 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL074CN |
| A10U951 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL074CN |
| A10U960 | 156-0513-03 |  | IC,MISC:CMOS,ANALOG MUX | 04713 | MC14051BCP |
| A10VR200 | 152-0166-00 |  | DIODE,ZENER:;,6.2V,5\%,0.4W | 04713 | SZ11738RL |
| A10VR298 | 152-0278-00 |  | DIODE,ZENER:,;3V,5\%,0.4W | 04713 | 1N4372ARL |
| A10VR390 | 152-0662-00 |  | DIODE,ZENER:,:5V.1\%,0.4W | 04713 | SZG195RL |


| Component Number | Tektronix Part No. | Serial No. Effective Dscont | Name \& Description | Mfr. Code | Mitr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A10VR391 | 152-0662-00 |  | DIODE,ZENER:;5V,1\%,0.4W | 04713 | SZG195RL |
| A10VR420 | 152-0166-00 |  | DIODE,ZENER:;$; 6.2 \mathrm{~V}, 5 \%, 0.4 \mathrm{~W}$ | 04713 | SZ11738RL |
| A10VR492 | 152-0662-00 |  | DIODE,ZENER:;5V,1\%,0.4W | 04713 | SZG195RL |
| A10VR493 | 152-0662-00 |  | DIODE,ZENER:;5V,1\%,0.4W | 04713 | SZG195RL |
| A10W110 | 131-0586-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD $\times 0.225 \mathrm{~L}$ | 24546 | OMA0207 |
| A10W221 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES, $0.094 \mathrm{OD} \times 0.225 \mathrm{~L}$ | 24546 | OMA0207 |
| A10W470 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| Alow511 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD $\times 0.225 \mathrm{~L}$ | 24546 | OMA0207 |
| Atow762 | 131-0566-00 | B010100 B011391 | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A10XU100 | 136-0764-0 |  | SOCKET,HYBRID:PCB,;STR,48 POS,0.05 CTR | 00779 | 54973-1 |
| A10XU150 | 136-0764-0 |  | SOCKET,HYBRID:PCB,;STR,48 POS,0.05 CTR | 00779 | 54973-1 |
| A10XU320 | 136-0763-0 |  | SKT,PL-IN ELEK:26 LINE CONT IMPD HYBRID | 00779 | 54977-1 |
| A10XU340 | 136-0764-0 |  | SOCKET,HYBRID:PCB,;STR,48 POS,0.05 CTR | 00779 | 54973-1 |
| A10XU350 | 136-0764-0 |  | SOCKET,HYBRID:PCB,;STR,48 POS,0.05 CTR | 00779 | 54973-1 |
| A10XU370 | 136-0813-00 |  | SKT,PL-IN ELEK:CHIP CARRIER,68 CONTACTS | 53387 | 2-0068-05400-00 |
| A10XU420 | 136-0763-0 |  | SKT,PL-IN ELEK:26 LINE CONT IMPD HYBRID | 00779 | 54977-1 |
| A10XU440 | 136-0764-0 |  | SOCKET,HYBRID:PCB,;STR,48 POS,0.05 CTR | 00779 | 54973-1 |
| A10XU450 | 136-0764-0 |  | SOCKET,HYBRID:PCB,;STR,48 POS,0.05 CTR | 00779 | 54973-1 |
| A10XU470 | 136-0813-00 |  | SKT,PL-IN ELEK:CHIP CARRIER,68 CONTACTS | 53387 | 2-0068-05400-00 |


| Component Number | Tektronix <br> Part No. | Serial Effective | No. Dscont | Name \& Description | Mfr. Code | Mtr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A11 | 671-0366-00 | B010100 | B010504 | CIRCUIT BD ASSY:TIME BASE DISPLAY | 80009 | 671036600 |
| A11 | 671-0366-01 | B010505 | B010649 | CIRCUIT BD ASSY:TIME BASE DISPLAY | 80009 | 671036601 |
| A11 | 671-0366-02 | B0t0650 |  | CIRCUIT BD ASSY:TIME BASE (STANDARD) | 80009 | 671036602 |
| A11 | 671-0366-02 |  |  | CIRCUIT BD ASSY:TIME BASE (2440M) | 80009 | 671038602 |
| A11C130 | 290-0967-00 |  |  | CAP,FXD,ELCTLT:22UF,+50-10\%,25V | OH1N5 | CE02W1E220C |
| A11C131 | 290-0967-00 |  |  | CAP,FXD,ELCTLT:22UF,+50-10\%,25V | OH1N5 | CE02W1E220C |
| A11C150 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C152 | 281-0786-00 |  |  | CAP,FXD,CERAMIC:MLC;150PF,10\%,100V | 04222 | SA101A151KAA |
| A11C154 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C166 | 281-0786-0 |  |  | CAP,FXD,CERAMIC:MLC;150PF,10\%,100V | 04222 | SA101A151KAA |
| A11C180 | 285-1344-0 |  |  | CAP,FXD,PLASTIC:1000PF,100V,5\% | TK1913 | FKP2 1000 PF 5 |
| A11C181 | 290-0808-00 |  |  | CAP,FXD,TANT:DRY; $2.7 \mathrm{THF}, 10 \%, 20 \mathrm{~V}$ | 24165 | 173D275X9020V |
| A11C182 | 290-0808-00 |  |  | CAP,FXD,TANT:DRY; $2.7 \mathrm{TH}, 10 \%, 20 \mathrm{~V}$ | 24165 | 173D275X9020V |
| A11C199 | 281-0771-00 |  |  | CAP,FXD,CER DI:2200PF,20\%,200V | 04222 | SA102C222MAA |
| A11C213 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC; 0.022 UF,20\%,50V | 04222 | SA105C223MAA |
| A11.C223 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC; $0.022 \mathrm{UF}, 20 \%, 50 \mathrm{~V}$ | 04222 | SA105C223MAA |
| A11C231 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C240 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11-243 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11-250 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11 C260 | 285-1342-00 |  |  | CAP,FXD,PLASTIC:FILM \& FOIL;220PF,5\%,100V | TK1913 | FKP2 220 PF 5 P |
| A11C261 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C264 | 285-1342-00 |  |  | CAP,FXD,PLASTIC:FILM \& FOIL;220PF,5\%,100V | TK1913 | FKP2 220 PF 5 P |
| A11-270 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C281 | 281-0762-00 |  |  | CAP,FXD,CER DI:27PF,20\%,100V | 04222 | SA102A270MAA |
| A11 C282 | 290-0808-00 |  |  | CAP,FXD, TANT:DRY; 2.7 T , $10 \%, 20 \mathrm{~V}$ | 24165 | 173D275X9020V |
| A11C284 | 290-0808-00 |  |  | CAP,FXD,TANT:DRY:2.7UF.10\%,20V | 24165 | 173D275X9020V |
| A11C290 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC:0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C291 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A110292 | 281-0909-0 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C312 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C313 | 281-0909-0 |  |  | CAP,FXD,CERAMIC:MLC; $0.022 \mathrm{UF}, 20 \%, 50 \mathrm{~V}$ | 04222 | SA105C223MAA |
| A11C323 | 281-0909-0 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C324 | 281-0909-00 |  |  | CAP,FXD.CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C331 | 281-0909-0 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11c340 | 281-0909-0 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C341 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C342 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C350 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |


| Component Number | Tektronlx <br> Part No. | Serial No. Effective Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A11C390 | 283-0594-0 |  | CAP,FXD,MICA DI:0.001UF,1\%,100V | TK0891 | RDM15FA102F03 |
| A11C392 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C400 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C401 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C402 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0,022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C414 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C415 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C416 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C420 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C422 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C450 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C460 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C490 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022 UF,20\%,50V | 04222 | SA105C223MAA |
| A11C500 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C510 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C511 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C513 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C520 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C521 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A116522 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C523 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A1tC531 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C532 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C540 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11-541 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C550 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C551 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C555 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C560 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C570 | 290-1045-00 |  | CAP,FXD,ELCTLT:4.7UF,10\%,35V | 24165 | 173D475X9035W |
| A11C580 | 281-0909-00 | B010330 | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V (STANDARD ONLY) | 04222 | SA105C223MAA |
| A11C580 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V (2440M ONLY) | 04222 | SA105C223MAA |
| A11C595 | 281-0810-00 |  | CAP,FXD,CERAMIC:MLC;5.6PF, $+1-0.5 \mathrm{PF}, 100 \mathrm{~V}$ | 04222 | SA102A5R6DAA |
| A11C601 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| At1C610 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C611 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C612 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C620 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11-621 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |


| Component Number | Tektronix Part No. | Effective | No. Dscont | Name \& Description | Mir. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A11C622 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C623 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C630 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11-631 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11-632 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C640 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C642 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C643 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C670 | 281-0909-00 | B010170 | B010504 | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V (STANDARD) | 04222 | SA105C223MAA |
| A11C680 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C691 | 281-0909-0 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11-692 | 290-1045-00 |  |  | CAP,FXD,ELCTLT:4,7UF,10\%,35V | 24165 | 173D475X9035W |
| A11-694 | 290-1045-00 |  |  | CAP,FXD,ELCTLT:4.7UF,10\%,35V | 24165 | 173D475X9035W |
| A11C700 | 290-0967--0 |  |  | CAP,FXD,ELCTLT:22UF, $+50-10 \%, 25 \mathrm{~V}$ | OH1N5 | CE02W1E220C |
| A11C701 | 290-0967-00 |  |  | CAP,FXD,ELCTLT:22UF, $+50-10 \%, 25 \mathrm{~V}$ | OHIN5 | CE02W1E220C |
| A11C702 | 290-0967-00 |  |  | CAP,FXD,ELCTLT:22UF, $+50-10 \%, 25 \mathrm{~V}$ | OH1N5 | CE02W1E220C |
| A116703 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC:0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C711 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C712 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC; $0.022 \mathrm{UF}, 20 \%, 50 \mathrm{~V}$ | 04222 | SA105C223MAA |
| A11C720 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC; $0.022 \mathrm{UF}, 20 \%, 50 \mathrm{~V}$ | 04222 | SA105C223MAA |
| A11C730 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC; $0.022 \mathrm{UF}, 20 \%, 50 \mathrm{~V}$ | 04222 | SA105C223MAA |
| A11C731 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C732 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C740 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC; $0,022 \mathrm{UF}, 20 \%, 50 \mathrm{~V}$ | 04222 | SA105C223MAA |
| A11C770 | 281-0785-00 |  |  | CAP,FXD,CERAMIC:MLC;68PF,10\%,100V | 04222 | SA102A680KAA |
| A11C772 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C774 | 285-1300-01 |  |  | CAP,FXD,MTLZD:0.1UF,10\%,63V | TK1913 | MKS2 0.1/63/10 |
| A11C776 | 285-1300-01 |  |  | CAP,FXD,MTLZD:0.1UF,10\%,68V | TK1913 | MKS2 0.1/63/10 |
| A11C820 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C832 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C833 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C834 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C835 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C881 | 281-0758-00 | B010330 |  | CAP,FXD,CER DI:15PF,20\%,100V (STANDARD ONLY) | 04222 | SA102A150MAA |
| A11C881 | 281-0758-00 |  |  | CAP,FXD,CER DI:15PF,20\%,100V (2440M ONLY) | 04222 | SA102A150MAA |
| A11C890 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C892 | 281-0777-00 |  |  | CAP,FXD,CERAMIC:MLC:51PF, $5 \%, 100 \mathrm{~V}$ | 04222 | SA102A510JAA |
| A11C900 | 281-0770-00 |  |  | CAP,FXD,CER DI:1000PF,20\%,100V | 04222 | SA101C102MAA |
| A11C901 | 281-0762-00 |  |  | CAP,FXD,CER DI:27PF,20\%,100V | 04222 | SA102A270MAA |


| Component Number | Tektronlx <br> Part No. | Serial Effective | INo. Dscont | Name \& Description | Mfr. Code | Mtr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A11C003 | 281-0791-00 |  |  | CAP,FXD,CERAMIC:MLC; 270 PF,10\%,100V | 04222 | SA102C271KAA |
| A11C907 | 281-0791-00 |  |  | CAP,FXD,CERAMIC:MLC;270PF,10\%,100V | 04222 | SA102C271KAA |
| A11C912 | 285-1343-00 |  |  | CAP,FXD,PLASTIC:330PF,100V,5\% | TK1913 | FKP2 330 PF 5 P |
| A11C020 | 281-0823-00 |  |  | CAP,FXD,CER DI:470PF,10\%,50V | 04222 | SA101A471KAA |
| A11C925 | 281-0791-0 |  |  | CAP,FXD,CERAMIC:MLC; 270 PF, $10 \%, 100 \mathrm{~V}$ | 04222 | SA102C271KAA |
| A11C930 | 281-0909-0 |  |  | CAP,FXD,CERAMIC:MLC;0,022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C932 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11-934 | 281-0909-0 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11C935 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A11CR190 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST; 40V,150MA,4NS,2PF | 27014 | FDH9427 |
| Al1CR191 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST; 40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A11CR193 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A11CR194 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST; $40 \mathrm{~V}, 150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A11CR280 | 152-0141-02 |  |  | DIODE,SIG: ULTRA FAST;40V, $150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| Alt ${ }^{\text {cren } 281}$ | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V, $150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{FF}$ | 27014 | FDH9427 |
| A11CR283 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST; $40 \mathrm{~V}, 150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A11CR284 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST; 40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A11CR671 | 152-0141-02 | B010170 | B010504 | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (STANDARD) | 27014 | FDH9427 |
| A1tCR672 | 152-0141-02 | B010170 | $B 010504$ | DIODE,SIG:ULTRA FAST;40V,150MA,4NS,2PF (STANDARD) | 27014 | FDH9427 |
| A11J100 | 131-3182-0 |  |  | CONN,HDR:PCB,:MALE,RTANG, $2 \times 25,0.1$ CTR | 53387 | 2550-5002UB |
| A11J117 | 131-0589-0 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 4) | 22526 | 48283-087 |
| A11J121 | 131-3181-00 |  |  | CONN,HDR:PCB; MALE,RTANG, $2 \times 20,0.1$ CTR | 22526 | 69155-440R |
| A11J131 | 131-3182-00 |  |  | CONN,HDR:PCB, MALE,RTANG, $2 \times 25,0.1$ CTR | 53387 | 2550-5002UB |
| A11J132 | -------- |  |  | WIRE,ELECTRICAL:22 AWG,BARE, 12.0 L |  |  |
| A11J148 | 131-0589-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR (QUANTITY OF 5) | 22526 | 48283-087 |
| Al1J513 | 131-0589-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 2) | 22526 | 48283-087 |
| A11L692 | 108-0538-00 |  |  | COIL,RF:FIXED,2.7UH | OJR03 | 108-0538-00 |
| A11L694 | 108-0538-00 |  |  | COIL,RF:FIXED,2.7UH | 0.JR03 | 108-0538-00 |
| A11L770 | 108-0538-00 |  |  | COIL,RF:FIXED,2.7UH | O.JR03 | 108-0538-00 |
| A11L800 | 108-0538-00 |  |  | COIL,RF:FIXED,2.7UH | O.JR03 | 108-0538-00 |
| A1 1-801 | 108-0538-00 |  |  | COIL,RF:FIXED,2.7UH | O.JR03 | 108-0538-00 |
| A11L802 | 108-0538-00 |  |  | COIL,RF:FIXED,2.7UH | O.JR03 | 108-0538-00 |
| A11L803 | 108-0538-00 |  |  | COIL,RF:FIXED,2.7UH | OUR03 | 108-0538-00 |
| A11Q181 | 151-0188-00 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A11Q182 | 151-0190-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA | 04713 | 2N3904 |
|  | 151-0188-00 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |


| Componemt Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mif. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A11Q286 | 151-0190-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA | 04713 | 2N3904 |
| A11R132 | 315-0103-00 |  | RES,FXD,FILM:10K OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R133 | 315-0103-00 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A11R140 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043EDTOK00F |
| A11R141 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM,1\%,0.125W,TC= $=$ TO | 19701 | 5043ED10K00F |
| A11R145 | 321-0126-00 |  | RES,FXD,FILM:200 OHM, 1\%,0.125W,TC=T0 | TK1727 | MR25 2322-151-2 |
| A11R151 | 321-0816-00 |  | RES,FXD,FILM: 5 K ОНM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033RD5K000F |
| A11R152 | 321-0816-00 |  | RES,FXD,FILM:5K OHM, 1\%,0.125W,TC = TO | 19701 | 5033RD5K000F |
| A11R153 | 315-0271-0 |  | RES,FXD,FILM:270 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R155 | 321-0816-00 |  | RES,FXD,FILM:5K OHM, 1\%,0.125W,TC=TO | 19701 | 5033RD5K000F |
| A11R156 | 321-0816-00 |  | RES,FXD,FILM: 5 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033RD5K000F |
| Al1R160 | 321-0816-00 |  | RES,FXD,FILM: 5 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033RD5K000F |
| A11R161 | 321-0816-00 |  | RES,FXD,FILM:5K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033RD5K000F |
| A11R162 | 321-0222-00 |  | RES,FXD,FILM:2.00K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033ED2K00F |
| A11R163 | 321-0193-00 |  | RES,FXD,FILM: 1 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-1 |
| A11R164 | 321-0193-00 |  | RES,FXD,FILM: 1 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | TK1727 | MR25 2322-151-1 |
| A11R165 | 321-0210-00 |  | RES,FXD,FILM:1.50K ОHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033ED1K50F |
| A11R171 | 321-0193-00 |  | RES,FXD,FILM: 1 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | TK1727 | MR25 2322-151-1 |
| A11R172 | 321-0816-00 |  | RES,FXD,FILM: 5 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033RD5K000F |
| A11R192 | 321-0165-0 |  | RES,FXD,FILM: 511 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-5 |
| A11R193 | 315-0512-0 |  | RES,FXD,FILM:5.1K OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R194 | 321-0001-0 |  | RES,FXD,FILM: 10 OHM, 1\%,0.125W,TC=T0 | 91637 | CMF55116G10R00F |
| A11R196 | 321-0001-00 |  | RES,FXD,FILM: 10 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CMF55116G10ROOF |
| A11R199 | 321-0193-0 |  | RES,FXD,FILM: 1 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-1 |
| A11R223 | 315-0560-- |  | RES,FXD,FILM: 56 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R230 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R232 | 315-0101-00 |  | RES,FXD,FILM: 100 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A11R262 | 315-0271-00 |  | RES,FXD,FILM:270 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A1 1R272 | 321-0097-00 |  | RES,FXD,FILM: 100 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-9 |
| A11R274 | 321-0097-00 |  | RES,FXD,FILM: 100 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-9 |
| A11R276 | 311-2234-00 |  | RES,VAR,TRMR:CERMET;5K OHM, 20\%,0.5W | TK2073 | GF06UT2 502 M L |
| A11R280 | 321-0816-0 |  | RES,FXD,FILM: 5 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033RD5K000F |
| A11R282 | 321-0244-- |  | RES,FXD,FILM:3.40K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | 2322-151 3K40 |
| A11R288 | 315-0512-0 |  | RES,FXD,FILM:5.1K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A11R312 | 315-0101-0 |  | RES,FXD,FILM: 100 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A11R330 | 315-0103-00 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A11R361 | 321-0165-00 |  | RES,FXD,FLM : 511 OHM, 1\%,0.125W,TC=T0 | TK1727 | MR25 2322-151-5 |
| A11R362 | 321-0193-00 |  | RES,FXD,FILM: 1 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | TK1727 | MR25 2322-151-1 |
| A11R363 | 321-0193-00 |  | RES,FXD,FILM: 1 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | TK1727 | MR25 2322-151-1 |
| A11R364 | 321-0816-00 |  | RES,FXD,FILM: 5 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033RD5K000F |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
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| A11R366 | 321-0816-0 |  | RES,FXD,FILM:5K OHM,1\%,0.125W,TC=T0 | 19701 | 5033RD5K000F |
| A11R376 | 311-2234-0 |  | RES,VAR,TRMR:CERMET;5K OHM,20\%,0.5W | TK2073 | GF06UT2 502 ML |
| A11R380 | 321-0001-0 |  | RES,FXD,FILM:10 OHM, 1\%,0.125W,TC=TO | 91637 | CMF55116G10R00F |
| A11R381 | 321-0001-0 |  | RES,FXD,FILM: 10 OHM, 1\%,0.125W,TC=T0 | 91637 | CMF55116G10R00F |
| A11R382 | 321-0926-07 |  | RES,FXD,FILM:4K OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T9 | TK1727 | MPR24-2322-141 |
| A11R383 | 321-0816-0 |  | RES,FXD,FILM:5K OHM, 1\%,0.125W,TC= T0 | 19701 | 5033RD5K000F |
| A11R384 | 321-0816-00 |  | RES,FXD,FILM:5K OHM, 1\%,0.125W,TC=T0 | 19701 | 5033RD5K000F |
| A11R385 | 321-0276-00 |  | RES,FXD,FILM:7.32K OHM, 1\%,0.125W,TC=TO | TK1727 | MR25-2322-151-7 |
| A11R400 | 315-0101-0 |  | RES,FXD,FILM:100 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R421 | 307-0446-00 |  | RES NTWK,FXD,FI:10K OHM, $20 \%$,(9)RES | 11236 | 750-101-R10K |
| A11R441 | 315-0103-00 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A11R450 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R470 | 321-0230-00 |  | RES,FXD,FILM:2.43K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ To | TK1727 | 2322-151-2K43 |
| A11R471 | 321-0273-00 |  | RES,FXD,FILM:6.81K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED6K810F |
| A11R472 | 321-0300-00 |  | RES,FXD,FILM:13.0K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED13K00F |
| A11R473 | 321-0377-00 |  | RES,FXD,FILM:82.5K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED82K50F |
| A11R474 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ To | 19701 | 5043ED10K00F |
| A11R475 | 321-0289-0 |  | RES,FXD,FILM: 10.0 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED10K00F |
| A11R480 | 321-0243-00 |  | RES,FXD,FILM:3.32K OHM,1\%,0.125W,TC=T0 | 19701 | 5033ED3K32F |
| A11R481 | 321-0251-0 |  | RES,FXD,FILM:4.02K OHM,1\%,0.125W,TC=TO | 19701 | 5043ED4K020F |
| A11R482 | 321-0275-m |  | RES,FXD,FILM:7.15K OHM, 1\%,0.125W,TC= $=$ T0 | 19701 | 5043ED7K150F |
| A11R483 | 321-0272-0 |  | RES,FXD,FILM:6.65K OHM, 1\%,0.125W,TC=T0 | TK1727 | MR25-2322-151-6 |
| A11R484 | 321-0326-0 |  | RES,FXD,FILM:24.3K OHM, 1\%,0.125W,TC=T0 | TK1727 | 2322-151-24K3 |
| A11R485 | 321-0300-00 |  | RES,FXD,FILM:13.0K OHM, 1\%,0.125W,TC=TO | 19701 | 5043ED13K00F |
| A11R490 | 321-0222-00 |  | RES,FXD,FILM:2.00K OHM, 1\%,0.125W,TC=T0 | 19701 | 5033ED2K00F |
| A11R492 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM,1\%,0.125W,TC= $=$ T0 | 19701 | 5043ED10K00F |
| A11R493 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED10K00F |
| A11R494 | 321-0414-00 |  | RES,FXD,FILM:200K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ To | 19701 | 5043ED200KOF |
| Al1R501 | 315-0101-00 |  | RES,FXD,FILM:100 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R522 | 315-0560-00 |  | RES,FXD,FILM:56 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R530 | 315-0560-00 |  | RES,FXD,FILM: 56 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R542 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R555 | 315-0560-00 |  | RES,FXD,FLLM: 56 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R570 | 321-0385-00 |  | RES,FXD,FILM:100K OHM,1\%,0.125W,TC=TO | 19701 | 5043ED100KOF |
| A11R580 | 311-2234-00 |  | RES,VAR,TRMR:CERMET;5K OHM,20\%,0.5W | TK2073 | GF06UT2 502 M L |
| A11R581 | 321-0193-00 |  | RES,FXD,FILM:1K OHM,1\%,0.125W,TC=TO | TK1727 | MR25 2322-151-1 |
| A11R583 | 311-2236-00 |  | RES,VAR,TRMP:CERMET;20K OHM,20\%,0.5W | TK2073 | GF06UT2 203 ML |
| A11R584 | 311-2236-00 |  | RES,VAR,TRMR:CERMET;20K OHM,20\%,0.5W | TK2073 | GF06UT2 203 ML |
| A11R585 | 311-2236-00 |  | RES,VAR,TRMR:CERMET;20K OHM, $20 \%, 0.5 \mathrm{~W}$ | TK2073 | GF06UT2 203 M L |
| A11R586 | 311-2234-00 |  | RES,VAR,TRMR:CERMET;5K OHM, $20 \%, 0.5 \mathrm{~W}$ | TK2073 | GF06UT2 502 ML |


| Component Number | Tektronlx <br> Part No. | Serial Effective | 1 No. Dscont | Name \& Description | Mts. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A11R587 | 311-2236-00 |  |  | RES,VAR,TRMR:CERMET;20K OHM,20\%,0.5W | TK2073 | GF06UT2 203 ML |
| A11R591 | 321-0816-0 |  |  | RES,FXD,FILM:5K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033RD5K000F |
| A11R592 | 321-0816-0 |  |  | RES,FXD,FILM:5K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033RD5K000F |
| A11R593 | 315-0202-02 |  |  | RES,FXD,CMPSN:2K OHM, 5\%,0.25W | 50139 | CB2025 |
| A11R594 | 315-0202-02 |  |  | RES,FXD,CMPSN:2K OHM, 5\%,0.25W | 50139 | CB2025 |
| A11R595 | 315-0202-02 |  |  | RES,FXD,CMPSN:2K OHM, $5 \%, 0.25 \mathrm{~W}$ | 50139 | CB2025 |
| A11R596 | 315-0202-02 |  |  | RES,FXD,CMPSN:2K OHM, $5 \%, 0.25 \mathrm{~W}$ | 50139 | CB2025 |
| A11R601 | 321-0118-0 |  |  | RES,FXD,FILM: 165 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED165Rof |
| A11R603 | 321-0129-00 |  |  | RES,FXD,FILM: 215 OHM, 1\%,0.125W.TC = T0 | TK1727 | MR25 2322-151-2 |
| A11R605 | 321-0097-00 |  |  | RES,FXD,FILM: 100 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | TK1727 | MR25 2322-151-9 |
| A11R607 | 321-0193-00 |  |  | RES,FXD,FILM:1K OHM,1\%,0.125W,TC=T0 | TK1727 | MR25 2322-151-1 |
| A11R610 | 315-0103-00 |  |  | RES,FXD,FILM:10K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A11R612 | 315-0750-00 |  |  | RES,FXD,FILM:75 OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R620 | 311-2231-00 |  |  | RES,VAR,TRMR:CERMET; 1 K OHM, $20 \%, 0.5 \mathrm{~W}$ | TK2073 | GFO6UT2 102 ML |
| A11R650 | 307-0446-00 |  |  | RES NTWK,FXD,Fl: 10 K OHM, $20 \%$,(9)RES | 11236 | 750-101-R10K |
| A11R670 | 315-0270-00 | B010170 | B010504 | RES,FXD,FILM:27 OHM,5\%,0.25W (STANDARD) | TK1727 | SFR25 2322-181 |
| A11R690 | 321-0097-0 |  |  | RES,FXD,FILM: 100 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO (NOMINAL VALUE) | TK1727 | MR25 2322-151-9 |
| A11R600 | 321-0100-0 | B010284 |  | RES,FXD,FILM: 107 OHM, 1\%,0.125W,TC = TO | 07716 | CEAD107ROF |
| A11R690 | 321-0101-00 | B010284 |  | RES,FXD,FILM:110 OHM,1\%,0.125W,TC=TO (TEST SELECTABLE) | TK1727 | MR25 2322-151-1 |
| A11R713 | 315-0560-0 |  |  | RES,FXD,FILM:56 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R715 | 315-0560-0 |  |  | RES,FXD,FILM: 56 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A11R716 | 315-0560-00 |  |  | RES,FXD,FILM: 56 OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A11R720 | 307-0446-00 |  |  | RES NTWK,FXD,FI: 10 K OHM, $20 \%$,(9)RES | 11236 | 750-101-R10K |
| A11R721 | 307-0446-00 |  |  | RES NTWK,FXD,Fl: 10 K OHM,20\%,(9)RES | 11236 | 750-101-R10K |
| A11R722 | 315-0101-0 |  |  | RES,FXD,FILM: $100 \mathrm{OHM}, 5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A11R723 | 315-0560-0 |  |  | RES,FXD,FULM:56 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R732 | 315-0103-0 |  |  | RES,FXD,FILM:10K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A11R780 | 321-0085-0 |  |  | RES,FXD,FILM: 75 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | TK1727 | MR25 2322-151-9 |
| A11R781 | 321-0143-00 |  |  | RES,FXD,FILM:301 OHM, $1 \%, 0.125 \mathrm{~W}$,TC = T0 | TK1727 | MR25 2322-151-3 |
| A11R832 | 315-0560-0 |  |  | RES,FXD,FILM: 56 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R833 | 315-0560-00 |  |  | RES,FXD,FILM: 56 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R835 | 307-0677-00 |  |  | RES NTWK,FXD,FI:4,56 OHM,2\%,0.2W | 11236 | 750-83-R56 OR 7 |
| A11R841 | 315-0560-0 |  |  | RES,FXD,FILM: 56 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R842 | 315-0560-0 |  |  | RES,FXD,FILM: 56 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| Al1R843 | 315-0560-0 |  |  | RES,FXD,FILM: 56 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A11R845 | 307-0677-0 |  |  | RES NTWK,FXD,FI:4,56 OHM,2\%,0.2W | 11236 | 750-83-R56 OR 7 |
| A11R880 | 321-0068-0 |  |  | RES,FXD,FILM:49.9 OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-9 |
| A11R881 | 321-0143-00 |  |  | RES,FXD,FILM:301 OHM,1\%,0.125W,TC=TO (NOMINAL VALUE) | TK1727 | MR25 2322-151-3 |


| Component Number | Tektronix Part No. | Serial Effective | No. Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A11R881 | 321-0149-00 | B010284 |  | RES,FXD,FILM:348 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | TK1727 | MR25 2322-151-3 |
| A11R881 | 321-0152-00 | B010284 |  | RES,FXD,FILM:374 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO (TEST SELECTABLE) | TK1727 | MR25 2322-151-3 |
| A11R884 | 321-0239-00 |  |  | RES,FXD,FILM:3.01K OHM, 1\%,0.125W, ${ }^{\text {TC }}=$ TO | TK1727 | 2322-151-3K01 |
| A11R891 | 321-0068-00 | B010100 | B010329 | RES,FXD,FILM:49.9 OHM, $0.1 \%, 0.125 W, T C=$ T0 | TK1727 | MR25 2322-151-9 |
| A11R891 | 322-3068-0 | B010330 |  | RES,FXD:METAL FILM;49.9 OHM,1\%,0.2W (STANDARD ONLY) | 91637 | CCF501G49R90F |
| A11R891 | 322-3068-0 |  |  | RES,FXD:METAL FILM;49.9 OHM,1\%,0.2W (2440M ONLY) | 91637 | CCF501G49R90F |
| A11TP130 | 131-0566-- |  |  | BUS,CONDUCTOR:DUMMY RES, 0.094 OD X 0.225L | 24546 | OMA0207 |
| A11TP133 | 131-0566-0 |  |  | BUS,CONDUCTOR:DUMMY RES, 0.094 OD X 0.225L | 24546 | OMA0207 |
| A11TP200 | 131-0566-0 |  |  | BUS,CONDUCTOR:DUMMY RES, 0.094 OD $\times 0.225 \mathrm{~L}$ | 24546 | OMA0207 |
| Al1TP250 | 131-0566-0 |  |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD $\times 0.225 \mathrm{~L}$ | 24546 | OMA0207 |
| A11TP341 | 131-0566-0 |  |  | BUS,CONDUCTOR:DUMMY RES, 0.094 OD $\times 0.225 \mathrm{~L}$ | 24546 | OMA0207 |
| A11TP400 | 131-0566-0 |  |  | BUS,CONDUCTOR:DUMMY RES, 0.094 OD X 0.225L | 24546 | OMA0207 |
| A11TP490 | 131-0566-00 |  |  | BUS,CONDUCTOR:DUMMY RES, 0.094 OD X 0.225L | 24546 | OMA0207 |
| A11TP530 | 131-0566-00 |  |  | BUS,CONDUCTOR:DUMMY RES, 0.094 OD $\times 0.225 \mathrm{~L}$ | 24546 | OMA0207 |
| A11TP600 | 131-0566-00 |  |  | BUS,CONDUCTOR:DUMMY RES, 0.094 OD $\times 0.225 \mathrm{~L}$ | 24546 | OMA0207 |
| A11TP601 | 131-0566-00 |  |  | BUS,CONDUCTOR:DUMMY RES, 0.094 OD X 0.225 L | 24546 | OMA0207 |
| A11TP602 | 131-0566-0 |  |  | BUS,CONDUCTOR:DUMMY RES, 0.094 OD $\times 0.225 \mathrm{~L}$ | 24546 | OMA0207 |
| A11TP680 | 131-0566-00 |  |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A11TP700 | 131-0566-00 |  |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD $\times 0.225 \mathrm{~L}$ | 24546 | OMA0207 |
| A11TP710 | 131-0566-00 |  |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A11U130 | 156-0852-0 |  |  | IC,DIGITAL:LSTTL,GATES;NONINV, HEX BUS | 01295 | SN74LS367N |
| A11U140 | 156-0956-0 |  |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV | 01295 | SN74LS244N3 |
| A1tU141 | 156-0956-00 |  |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV | 01295 | SN74LS244N3 |
| A11U142 | 156-1638-0 |  |  | IC,CONVERTER:BIPOLAR,D/A;10 BIT, 150 NS | 24355 | DAC10-041P |
| A11U170 | 156-1156-00 |  |  | IC,LINEAR:BIFET,OP-AMP | 27014 | LF356N |
| A11 210 | 156-0530-00 |  |  | IC,DIGITAL:LSTTL,MUX;QUAD 2-TO-1 | 01295 | SN74LS157N |
| A11U211 | 156-0422-00 |  |  | IC,DIGITAL:LSTTL,COUNTER;SYNCH 4-BIT | 01295 | SN74LS191N |
| A11U212 | 156-0530-00 |  |  | IC,DIGITAL:LSTTL,MUX;QUAD 2-TO-1 | 01295 | SN74LS157N |
| A11U220 | 156-0422-0 |  |  | IC,DIGITAL:LSTTL,COUNTER;SYNCH 4-BIT | 01295 | SN74LS191N |
| A11U221 | 156-0530-00 |  |  | IC,DIGITAL:LSTTL,MUX;QUAD 2-TO-1 | 01295 | SN74LS157N |
| A11U222 | 156-0422-00 |  |  | IC,DIGITAL:LSTTL,COUNTER;SYNCH 4-BIT | 01295 | SN74LS191N |
| A11U223 | 156-0481-00 |  |  | IC,DIGITAL:LSTTL,GATES;TRIPLE 3-INPUT | 01295 | SN74LS11N |
| A11U230 | 156-0994-02 |  |  | IC,DIGITAL:LSTTL,MUX/ENCODER | 01295 | SN74LS151N |
| A11U231 | 156-0844-0 |  |  | IC,DIGITAL:LSTTL,COUNTER;SYNCH 4-BIT | 01295 | SN74LS161AN |
| A11U232 | 160-2559-- |  |  | MICROCKT,DGTL:32 $\times 8$ PROM,PRGM | 80009 | 160-2559-00 |
| A11U240 | 156-0852- -0 |  |  | IC,DIGITAL:LSTTL,GATES;NONINV, HEX BUS | 01295 | SN74LS367N |
| A11U241 | 156-0982-03 |  |  | IC,DIGITAL:LSTTL,FLIP FLOP | 01295 | SN74LS374N |
| A11U243 | 156-0956-00 |  |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV | 01295 | SN74LS244N3 |


| Component Number | Toktronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A11U250 | 156-1638-00 |  | IC,CONVERTER:BIPOLAR,D/A;10 BIT,150NS | 24355 | DAC10-041P |
| A11U270 | 156-0515-00 |  | IC,MISC:CMOS,ANALOG MUX;TRIPLE SPDT | 04713 | MC14053BCP |
| A11U280 | 156-2485-00 |  | IC,LINEAR:BIFET,OP-AMP:WIDEBAND,HIGH SLEW | 34371 | HA2-5162-5 |
| A11U281 | 156-0742-00 |  | IC,LINEAR:BIPOLAR,OP-AMP;HIGH SLEW RATE | 01295 | LM318P |
| A11U282 | 156-2485-00 |  | IC,LINEAR:BIFET,OP-AMP;WIDEBAND,HIGH SLEW | 34371 | HA2-5162-5 |
| A11U290 | 156-0514-00 |  | IC,MISC:CMOS,ANALOG MUX:DUAL 4 CHANNEL | 04713 | MC14052BCP |
| A11U300 | 156-1714- $-\infty$ |  | IC,DIGITAL:FTTL,COUNTER;SYNCH 4-BIT | 1 CH 66 | N74F191N |
| AliU312 | 156-0386-0 |  | IC,DIGITAL:LSTTL,GATES;TRIPLE 3-INPUT | 01295 | SN74LS10N |
| A11U313 | 156-0452-0 |  | IC,DIGITAL:LSTTL,GATES;4-WIDE 2-INPUT | 01295 | SN74LS54N |
| A11U314 | 156-1111-02 |  | IC,DIGITAL:LSTTL,TRANSCEIVER | 01295 | SN74LS245N |
| A11U320 | 156-0956-0 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 01295 | SN74LS244N3 |
| A11U321 | 156-0956-0 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 01295 | SN74LS244N3 |
| A11U322 | 156-1111-02 |  | IC,DIGITAL:LSTTL,TRANSCEIVER | 01295 | SN74LS245N |
| A11U323 | 156-0479-0 |  | IC,DIGITAL:LSTTL,GATES;QUAD 2-INPUT | 01295 | SN74LS32N |
| A11U330 | 160-2560-0 |  | MICROCKT,DGTL:32 $\times 8$ PROM,PRGM | 80009 | 160-2560-00 |
| A11U340 | 156-0382-00 |  | IC,DIGITAL:LSTTL,GATE;QUAD 2-INPUT | 01295 | SN74LSOON |
| A11U350 | 156-0381-00 |  | IC,DIGITAL:LSTTL,GATES;QUAD 2-INPUT | 01295 | SN74LS86AN |
| A11U370 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TLO74CN |
| A11U392 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL074CN |
| A11U400 | 156-1714-00 |  | IC,DIGITAL:FTTL,COUNTER;SYNCH 4-BIT | 1 CH 66 | N74F191N |
| Al1U401 | 156-1714-0 |  | IC,DIGITAL:FTTL,COUNTER;SYNCH 4-BIT | 1 CH 66 | N74F191N |
| A11U410 | 156-0910-00 |  | IC,DIGITAL:LSTTL,COUNTER;DUAL 4-BIT DECADE | 01295 | SN74LS390N |
| A11U411 | 156-0386-00 |  | IC,DIGITAL:LSTTL,GATES;TRIPLE 3-INPUT | 01295 | SN74LS10N |
| At1U412 | 156-0382-00 |  | IC,DIGITAL:LSTTL,GATE;QUAD 2-INPUT | 01295 | SN74LS00N |
| A11U413 | 156-0385-00 |  | IC,DIGITAL:LSTTL,GATES;HEX INV | 01295 | SN74LS04N |
| A11U414 | 156-0388-0 |  | IC,DIGITAL:LSTTL,FLIP FLOP;DUAL D | 01295 | SN74LS74AN |
| A11U415 | 156-0388-0 |  | IC,DIGITAL:LSTTL,FLIP FLOP;DUAL D | 01295 | SN74LS74AN |
| A11U416 | 156-1172-0 |  | IC,DIGITAL:LSTTL,COUNTER;DUAL 4-BIT BINARY | 01295 | SN74LS393N |
| A11U420 | 160-2558-00 |  | MICROCKT,DGTL:4096 X 8 EPROM,PRGM | 80009 | 160-2558-0 |
| A1tU421 | 156-0480-0 |  | IG,DIGITAL:LSTTL,GATES; QUAD 2-INPUT | 01295 | SN74LS08N |
| A11U422 | 156-0479-0 |  | IC,DIGITAL:LSTTL,GATES;QUAD 2-INPUT | 01295 | SN74LS32N |
| A11U423 | 156-1373-00 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 01295 | SN74LS125AN |
| A11U430 | 156-1228-00 |  | IC,MEMORY:NMOS, SRAM; $4 \mathrm{~K} \times 1,70 \mathrm{NS}$ | 80009 | 156122800 |
| A11U431 | 156-2016-00 |  | IC,MEMORY:NMOS,SRAM;2K X 8,100NS | 65786 | CY6116A-55PC |
| A11U440 | 156-1594-00 |  | IC,MEMORY:NMOS,SRAM;2K X 8,150NS | OBOA9 | DS2016 |
| Al1U441 | 156-0982-03 |  | IC,DIGITAL:LSTTL,FLIP FLOP | 01295 | SN74LS374N |
| A11U442 | 156-0382-00 |  | IC,DIGITAL:LSTTL,GATE;QUAD 2-INPUT | 01295 | SN74LSOON |
| Al1U450 | 156-0480-00 |  | IC,DIGITAL:LSTTL,GATES;QUAD 2-INPUT | 01295 | SN74LS08N |
| A11U460 | 156-1200-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TL074CN |
| A11U500 | 156-0382-00 |  | IC,DIGITAL:LSTTL,GATE;QUAD 2-INPUT | 01295 | SN74LSOON |


| Component Number | Tektronlx Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mtr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A11U501 | 156-1909-00 |  | IC,DIGITAL:FTTL,MUX;QUAD 2-TO-1 DATA | 04713 | MC74F157N |
| A11U502 | 156-0982-03 |  | IC,DIGITAL:LSTTLL,FLIP FLOP | 01295 | SN74LS374N |
| A11U510 | 156-1611-00 |  | IC,DIGITAL:FTTL,FLIP FLOP;DUAL D-TYPE | 04713 | MC74F74N |
| A11U511 | 156-1611-0 |  | IC,DIGITAL:FTTL,FLIP FLOP;DUAL D-TYPE | 04713 | MC74F74N |
| A11U512 | 156-1724-0 |  | IC,DIGITAL:FTTL,GATES;QUAD 2-INPUT | 04713 | MC74F32N |
| A11U513 | 156-1722-00 |  | IC,DIGITAL:FTTL,GATE;HEXINV | 04713 | MC74F04N |
| A11U520 | 156-1611-00 |  | IC,DIGITAL:FTTL,FLIP FLOP;DUAL D-TYPE | 04713 | MC74F74N |
| Al1U521 | 156-1611-00 |  | IC,DIGITAL:FTTL,FLIP FLOP;DUAL D-TYPE | 04713 | MC74F74N |
| A11U522 | 156-1724-00 |  | IC,DIGITAL:FTTL,GATES;QUAD 2-INPUT | 04713 | MC74F32N |
| A11U523 | 156-0118-00 |  | IC,DIGITAL:STTL,FLIP FLOP;DUAL J-K | 01295 | SN74S112AN |
| A11U530 | 156-0913-02 |  | IC,DIGITAL:LSTTL,FLIP FLOP | 01295 | SN74LS377N |
| A11U531 | 156-1277-00 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 27014 | DM81LS95AN |
| Al1U532 | 156-1277-00 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 27014 | DM81LS95AN |
| A11U540 | 156-0913-02 |  | IC,DIGITAL:LSTTL,FLIP FLOP | 01295 | SN74LS377N |
| A11U541 | 156-0865-00 |  | IC,DIGITAL:LSTTL,FLIP FLOP;OCTAL D-TYPE | 01295 | SN74LS273N |
| A11U542 | 156-1277-00 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 27014 | DM81LS95AN |
| A11U550 | 156-0469-00 |  | IC,DIGITAL:LSTTL,DEMUXIDECODER | 01295 | SN74LS138 |
| A11U560 | 156-2800-00 |  | IC,CONVERTER:BIPOLAR,AD | 04713 | MC10319 |
| A11U600 | 156-2000-00 |  | IC,MEMORY:NMOS,SRAM:2K X 8,45NS | OJR04 | TMM2018D-45 |
| A11U601 | 156-0982-03 |  | IC,DIGITAL:LSTTL,FLIP FLOP | 01295 | SN74LS374N |
| A11U610 | 156-1111-02 |  | IC,DIGITAL:LSTTL, TRANSCEIVER | 01295 | SN74LS245N |
| A11U612 | 156-0118-0 |  | IC,DIGITAL:STTL,FLIP FLOP;DUAL J-K | 01295 | SN74S112AN |
| A11U613 | 156-1962- ${ }^{\text {- }}$ |  | IC,DIGITAL:FTTL,BUFFER | 04713 | MC74F244N |
| A11U615 | 156-0118-00 |  | IC,DIGITAL:STTL,FLIP FLOP;DUAL J-K | 01295 | SN74S112AN |
| A11U620 | 156-1707-00 |  | IC,DIGITAL:FTTL,GATE;QUAD 2-INPUT | 04713 | MC74F00 |
| A11U621 | 156-1935-00 |  | IC,DIGITAL:FTTL,COUNTER;SYNCH 4-BIT BINARY | 04713 | MC74F163AN/J |
| A11U622 | 156-1935-00 |  | IC,DIGITAL:FTTL,COUNTER;SYNCH 4-BIT BINARY | 04713 | MC74F163AN/J |
| A11U623 | 156-1663-00 |  | IC,DIGITAL:FTTL,GATE;TRIPLE 3-INPUT | 04713 | MC74F11N |
| A11U624 | 156-1909-00 |  | IC,DIGITAL:FTTL,MUX;QUAD 2-TO-1 DATA | 04713 | MC74F157N |
| A11U630 | 156-1704-00 |  | IC,DIGITAL:FTTL,FLIP FLOP;OCTAL D-TYPE | 01295 | SN74F374N |
| A11U631 | 156-1704-0 |  | IC,DIGITAL:FTTL,FLIP FLOP;OCTAL D-TYPE | 01295 | SN74F374N |
| A11U632 | 156-1704-00 |  | IC,DIGITAL:FTTL,FLIP FLOP;OCTAL D-TYPE | 01295 | SN74F374N |
| A11U640 | 156-1704-00 |  | IC,DIGITAL:FTTL,FLIP FLOP;OCTAL D-TYPE | 01295 | SN74F374N |
| A11U641 | 156-1111-02 |  | IC,DIGITAL:LSTTL, TRANSCEIVER | 01295 | SN74LS245N |
| A11U642 | 156-1961-00 |  | IC,DIGITAL.FTTL,SHIFT REGISTER | 04713 | MC74F194N |
| A11U650 | 156-1752-00 |  | IC,DIGITAL:FTTL,GATE;TRIPLE 3-INPUT | 04713 | MC 74F10N |
| A11U651 | 156-0388-00 |  | IC,DIGITAL:LSTTL,FLIP FLOP;DUAL D | 01295 | SN74LS74AN |
| A11U670 | 156-3353-00 | B010100 B010504 | MICROCKT,DGTL:CMOS,SEMI CUSTOM | 66302 | ADG016 (VF4565) |
| A11U670 | 156-3353-01 | B010505 | MICROCKT,DGTL:CMOS,SEMI CUSTOM | 66302 | VF4581PC CC0001 |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A11U670 | 156-3353-01 |  | MICROCKT,DGTL:CMOS,SEMI CUSTOM (2440M) | 66302 | VF4581PC CC0001 |
| A11U680 | 156-0956-00 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV | 01295 | SN74LS244N3 |
| A11U710 | 156-1973-00 |  | IC,DIGITAL:FTTL,FLIP FLOP;QUAD D-TYPE | 01295 | SN74F175N |
| A11U711 | 156-1800-0 |  | IC,DIGITAL:FTTL,GATES;QUAD 2-INPUT | 04713 | MC74F86N |
| A11U712 | 156-1723-00 |  | IC,DIGITAL:FTTL,GATE;QUAD 2-INPUT | 04713 | MC74F08N |
| A11U720 | 156-1611-0 |  | IC,DIGITAL:FTTL,FLIP FLOP:DUAL D-TYPE | 04713 | MC74F74N |
| A11U721 | 156-1935-0 |  | IC,DIGITAL:FTTL,COUNTER;SYNCH 4-BIT BINARY | 04713 | MC74F163AN/J |
| A11U722 | 156-1662-0 |  | IC,DIGITAL:FTTL,MUX;DUAL 4-TO-1 DATA | 04713 | MC74F153N |
| A11U730 | 156-1961-0 |  | IC,DIGITAL:FTTL,SHIFT REGISTER | 04713 | MC74F194N |
| A11U731 | 156-1723-00 |  | IC,DIGITAL:FTTL,GATE;QUAD 2-INPUT | 04713 | MC74F08N |
| A11U732 | 156-1041-02 |  | IC,DIGITAL:STTL,COMPARATOR;4-BIT | 01295 | SN74S85N |
| A11U740 | 156-1041-02 |  | IC,DIGITAL:STTL,COMPARATOR;4-BIT | 01295 | SN74S85N |
| A11U750 | 156-0651-00 |  | IC,DIGITAL:LSTTL,SHIFT REGISTER;8-BIT SIPO | 01295 | SN74LS164N |
| A11U780 | 156-2804-0 |  | IC.LINEAR:BIPOLAR,OP-AMP;600V/US SLEW | 34371 | HA1-2539-5 |
| A11U830 | 156-1961-00 |  | IC,DIGITAL:FTTL,SHIFT REGISTER;4-BIT | 04713 | MC74F194N |
| A11U831 | 156-1961-00 |  | IC,DIGITAL:FTTL,SHIFT REGISTER;4-BIT | 04713 | MC74F194N |
| A11U832 | 156-1722-0 |  | IC,DIGITAL:FTTL,GATE;HEXINV | 04713 | MC74F04N |
| A11U833 | 156-1961-0 |  | IC,DIGITAL:FTTL,SHIFT REGISTER;4-BIT | 04713 | MC74F194N |
| A11U834 | 156-1724-00 |  | IC,DIGITAL:FTTL,GATES;QUAD 2-INPUT | 04713 | MC74F32N |
| A11U835 | 156-1722-00 |  | IC,DIGITAL:FTTL,GATE;HEXINV | 04713 | MC74F04N |
| A11U880 | 156-1149-0 |  | IC,LINEAR:BIFET,OP-AMP; | 27014 | LF351N |
| A11W140 | 175-9026-0 |  | CA ASSY,SP:RIBBON,;IDC,50,28 AWG,6.5 L | 53387 | ORDER BY DESC |
| A11W780 | 131-0566-0 |  | BUS.CONDUCTOR:DUMMY RES, 0.094 OD X 0.225L | 24546 | OMA0207 |
| A11Y611 | 119-2430-0 |  | OSCILLATOR,RF:CRYSTAL CONTROLLER,40MHZ | 01537 | K1144 AM-40MHZ |


| Component Number | Tektronix Part No. | Seri <br> Effective | No. Dscont | Name \& Description | Mir. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A12 | 670-9746-17 |  |  | CIRCUIT BD ASSY:PROCESSOR (STANDARD ONLY) | 80009 | 670974617 |
| A12 | 670-9746-25 |  |  | CIRCUIT BD ASSY:PROCESSOR (OPTION 05 ONLY) | 80009 | 670974625 |
| A12BT800 | 146-0062-01 | B010100 | B013314 | BATTERY,PRIMARY:3.5V,1.6AH,LITHIUM | 81855 | LTC-16P-CO-F-S |
| A12C104 | 281-0763-00 |  |  | CAP,FXD,CERAMIC:MLC;47PF,10\%,100V | 04222 | SA102A470KAA |
| A12C105 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C107 | 281-0763-0 |  |  | CAP,FXD,CERAMIC:MLC;47PF,10\%,100V | 04222 | SA102A470KAA |
| A12C120 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C130 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C132 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C150 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C202 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C204 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C206 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V (OPTION 05 ONLY) | 04222 | SA105C223MAA |
| A12C217 | 281-0773-00 |  |  | CAP,FXD,CERAMIC:MLC; 0.01 UF,10\%,100V | TK1743 | CGB103KEX |
| A12C218 | 281-0775-00 |  |  | CAP,FXD,CER DI:0.1UF,20\%,50V (OPTION 05 ONLY) | 04222 | SA105E104MAA |
| A12C238 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C276 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C308 | 281-0785-00 |  |  | CAP,FXD,CERAMIC:MLC;68PF,10\%,100V (OPTION 05 ONLY) | 04222 | SA102A680KAA |
| A12C322 | 290-0183-00 |  |  | CAP,FXD,TANT:DRY;1UF,10\%,35V (OPTION O5 ONLY) | 12954 | AT513A105K035N |
| A12C324 | 28t-086t-0 |  |  | CAP,FXD,CER DI:270PF,5\%,50V (OPTION 05 ONLY) | 04222 | SA101A271JAA |
| A12C325 | 281-0820-00 |  |  | CAP,FXD,CERAMIC:MLC;680 PF,10\%,50V (OPTION 05 ONLY) | 04222 | SA101C681KAA |
| A12C328 | 281-0813-00 |  |  | CAP,FXD,CERAMIC:MLC;0.047UF,20\%,50V (OPTION 05 ONLY) | 04222 | SA105E473MAA |
| A12C330 | 281-0812-00 |  |  | CAP,FXD,CERAMIC:MLC; 1000 PF, $10 \%, 100 \mathrm{~V}$ (OPTION 05 ONLY) | 04222 | SA101C102KAA |
| A12C332 | 281-0814-00 |  |  | CAP,FXD,CERAMIC:MLC; $100 \mathrm{PF}, 10 \%, 100 \mathrm{~V}$ (OPTION 05 ONLY) | TK1743 | CGB101KEN |
| A12C336 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C342 | 281-0757-00 |  |  | CAP,FXD,CER Dl:10PF,20\%,100V | 04222 | SA102A100MAA |
| A12C344 | 283-0107-00 |  |  | CAP,FXD,CER DI:51PF,5\%,200V | 04222 | SR292A510JAA |
| A12C348 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C358 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C360 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C366 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C370 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mif. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A12C372 | 283-0051-00 |  | CAP,FXD,CER DI:0.0033UF,5\%,100V | 04222 | SR211A332JAA |
| A12C374 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C386 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C402 | 281-0775-0 |  | CAP,FXD,CER DI:0.1UF,20\%,50V (OPTION 05 ONLY) | 04222 | SA105E104MAA |
| A12C414 | 281-0863-00 |  | CAP,FXD,CERAMIC:MLC;240PF,5\%,100V (OPTION 05 ONLY) | 04222 | SA101A241JAA |
| A12C416 | 281-0792-00 |  | CAP,FXD,CER DI:82PF,10\%,100V (OPTION 05 ONLY | 04222 | SA102A820KAA |
| A12C418 | 281-0775-00 |  | CAP.FXD.CER DI: 0.1 UF,20\%,50V (OPTION 05 ONLY | 04222 | SA105E104MAA |
| A12C424 | 281-0775-00 |  | CAP,FXD,CER DI:0.1UF,20\%,50V (OPTION 05 ONLY) | 04222 | SA105E104MAA |
| A12C426 | 290-0183-00 |  | CAP,FXD,TANT:DRY;1UF,10\%,35V (OPTION 05 ONLY) | 12954 | AT513A105K035N |
| A12C452 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C462 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C464 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C466 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C472 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C474 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C484 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C510 | 281-0814-0 |  | CAP,FXD,CERAMIC:MLC; $100 \mathrm{PF}, 10 \%, 100 \mathrm{~V}$ (OPTION 05 ONLY) | TK1743 | CGB101KEN |
| A12C512 | 281-0775-0 |  | CAP,FXD,CER DI:0.1UF,20\%,50V (OPTION 05 ONLY) | 04222 | SA105E104MAA |
| A12C514 | 281-0786-0 |  | CAP,FXD,CERAMIC:MLC;150PF,10\%,100V (OPTION 05 ONLY) | 04222 | SA101A151KAA |
| A12C520 | 281-0773-00 |  | CAP,FXD,CERAMIC:MLC;0.01UF,10\%,100V | TK1743 | CGB103KEX |
| A12C522 | 281-0826-0 |  | CAP,FXD,CERAMIC:MLC;2200PF,10\%,100V (OPTION 05 ONLY) | TK1743 | CGB222KEX |
| A12C526 | 281-0775-0 |  | CAP,FXD,CER DI:0.1UF,20\%,50V (OPTION 05 ONLY) | 04222 | SA105E104MAA |
| A12C528 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V (OPTION 05 ONLY) | 04222 | SA105C223MAA |
| A12C532 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C542 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C550 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C572 | 281-0909-00 |  | CAP,FXD.CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C580 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C582 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A12C586 | 281-0814-00 |  | CAP,FXD,CERAMIC:MLC;100 PF,10\%,100V | TK1743 | CGB101KEN |
| A12C590 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A12C592 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |


| Component Number | Tektronix Part No. | Serial No. Effective Dscont | Name \& Description | Mfr. Code | Mtr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A12C606 | 281-0788-00 |  | CAP,FXD,CERAMIC:MLC;470PF, $10 \%, 100 \mathrm{~V}$ (OPTION 05 ONLY) | 04222 | SA102C471KAA |
| A12C608 | 281-0814-00 |  | CAP,FXD,CERAMIC:MLC; $100 \mathrm{PF}, 10 \%, 100 \mathrm{~V}$ (OPTION 05 ONLY) | TK1743 | CGB101KEN |
| A12C609 | 281-0863-00 |  | CAP,FXD,CERAMIC:MLC;240PF,5\%,100V (OPTION 05 ONLY) | 04222 | SA101A241JAA |
| A12C612 | 281-0775-00 |  | CAP,FXD,CER DI:0.1UF,20\%.50V (OPTION 05 ONLY | 04222 | SA105E104MAA |
| A12C620 | 281-0775-00 |  | CAP,FXD,CER DI:0.1UF,20\%,50V (OPTION 05 ONLY | 04222 | SA105E104MAA |
| A12C622 | 290-0246-00 |  | CAP,FXD,TANT:DRY;3.3UF,10\%,15V (OPTION 05 ONLY | 12954 | D3R3EA15K1 |
| A12C624 | 281-0775-00 |  | CAP,FXD,CER DI: $0.1 \mathrm{UF}, 20 \%, 50 \mathrm{~V}$ (OPTION 05 ONLY | 04222 | SA105E104MAA |
| A12C626 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C646 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C670 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C712 | 281-0775-00 |  | CAP,FXD,CER DI:0.1UF,20\%,50V (OPTION 05 ONLY) | 04222 | SA105E104MAA |
| A12C713 | 281-0775-00 |  | CAP,FXD,CER DI:0.1UF,20\%,50V (OPTION 05 ONLY) | 04222 | SA105E104MAA |
| A12C714 | 281-0775-00 |  | CAP,FXD,CER DI:0.1UF,20\%,50V (OPTION 05 ONLY) | 04222 | SA105E104MAA |
| A12C716 | 290-0808-00 |  | CAP,FXD,TANT:DRY;2.7UF,10\%,20V (OPTION 05 ONLY) | 24165 | 173D275X9020V |
| A12C719 | 281-0775-00 |  | CAP,FXD,CER DI:0.1UF,20\%,50V (OPTION 05 ONLY) | 04222 | SA105E104MAA |
| A12C720 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C748 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C764 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C766 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C774 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C780 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C790 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C850 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C862 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C882 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A12C884 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A12C886 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A12C894 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C904 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A12C936 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12C938 | 290-0748-0 |  | CAP,FXD,ELCTLT:10UF, $+50-20 \%, 25 \mathrm{~W}$ | OHIN5 | CEUST1E100 |
| A12C944 | 281-0775-00 |  | CAP,FXD,CER DI:0.1UF,20\%,50V | 04222 | SA105E104MAA |


| Component Number | Tektronix Part No. | Serial No. Effective Dscent | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A12C948 | 281-0757-00 |  | CAP,FXD,CER DI:10PF,20\%,100V | 04222 | SA102A100MAA |
| A12C950 | 283-0107-00 |  | CAP,FXD,CER DI:51PF,5\%,200V | 04222 | SR292A510JAA |
| A12C964 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A12C980 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A12CR104 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A12CR107 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA ,4NS,2PF | 27014 | FDH9427 |
| A12CR120 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A12CR122 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A12CR224 | 152-0951-00 |  | DIODE,SIG:SCHTKY;60V,2.25PF (OPTION 05 ONLY) | 66958 | IN6263 |
| A12CR244 | 152-0951-00 |  | DIODE,SIG:SCHTKY;;60V,2.25PF | 66958 | 1N6263 |
| A12CR324 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (OPTION 05 ONLY) | 27014 | FDH9427 |
| A12CR325 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (OPTION 05 ONLY) | 27014 | FDH9427 |
| A12CR326 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (OPTION 05 ONLY) | 27014 | FDH9427 |
| A12CR328 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (OPTION 05 ONLY) | 27014 | FDH9427 |
| A12CR329 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (OPTION 05 ONLY) | 27014 | FDH9427 |
| A12CR332 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (OPTION 05 ONLY) | 27014 | FDH9427 |
| A12CR334 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (OPTION 05 ONLY) | 27014 | FDH9427 |
| A12CR336 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V.150MA,4NS,2PF (OPTION 05 ONLY) | 27014 | FDH9427 |
| A12CR422 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (OPTION 05 ONLY) | 27014 | FDH9427 |
| A12CR502 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (OPTION 05 ONLY) | 27014 | FDH9427 |
| A12CR510 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (OPTION 05 ONLY) | 27014 | FDH9427 |
| A12CR512 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (OPTION 05 ONLY) | 27014 | FDH9427 |
| A12CR526 | 152-0460-00 |  | DIODE,SIG:,REGLTR;100V,1.20MA IP,1.45V (OPTION 05 ONLY) | 04713 | 1N5299 |
| A12CR594 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A12CR596 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A12CR606 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (OPTION 05 ONLY) | 27014 | FDH9427 |
| A12CR612 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (OPTION O5 ONLY) | 27014 | FDH9427 |
| A12CR620 | 152-0460-00 |  | DIODE,SIG:,REGLTR;100V,1.20MA IP,1.45V (OPTION 05 ONLY) | 04713 | 1N5299 |
| A12CR701 | 152-0141-02 | B010100 B013314 | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |


| Component Number | Tektronix Part No. | Effective | No. Dscont | Name \& Description | Mfr. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A12CR702 | 152-0141-02 | B010100 | B013314 | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A12CR715 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (OPTION 05 ONLY) | 27014 | FDH9427 |
| A12CR722 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V, 150MA,4NS,2PF | 27014 | FDH9427 |
| A12CR802 | 152-0951-00 |  |  | DIODE,SIG:SCHTKY;;0V,2.25PF | 66958 | 1N6263 |
| A12CR806 | 152-0951-00 | B010100 | B013314 | DIODE,SIG:SCHTKY;;6V,2.25PF | 66958 | 1N6263 |
| A12CR900 | 152-0951-00 | B010100 | B013314 | DIODE,SIG:SCHTKY;;0V,2.25PF | 66958 | 1N6263 |
| A12CR902 | 152-0951-00 | B010100 | 8013314 | DIODE,SIG:SCHTKY;;0V,2.25PF | 66958 | 1N6263 |
| A12CR944 | 152-0951-00 |  |  | DIODE,SIG:SCHTKY; 60V,2.25PF | 66958 | 1N6263 |
| A12CR992 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A12DL580 | 119-1804-00 |  |  | DELAY LINE,ELEC:10NS +/-0.5NS, 100 OHM | 24165 | 62Z03A010H |
| A12J103 | 131-3182-0 |  |  | CONN,HDR:PCB,;MALE,RTANG, $2 \times 25,0.1$ CTR | 53387 | 2550-5002UB |
| A12J120 | 131-3181-00 |  |  | CONN,HDR:PCB,;MALE,RTANG, $2 \times 20,0.1$ CTR | 22526 | 69155-440R |
| A12J123 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 8) <br> (OPTION 05 ONLY) | 22526 | 48283-018 |
| A12J124 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 4) | 22526 | 48283-018 |
| A12J125 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB;,MALE,STR (QUANTITY OF 15) | 22526 | 48283-018 |
| A12J126 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 3) | 22526 | 48283-018 |
| A12J127 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB;;MALE,STR (QUANTITY OF 4) | 22526 | 48283-018 |
| A12J128 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR (QUANTITY OF 2) | 22526 | 48283-018 |
| A12J129 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 2) | 22526 | 48283-018 |
| A12J181 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR (QUANTITY OF 24) | 22526 | 48283-018 |
| A12J184 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 2) | 22526 | 48283-018 |
| A12J207 | 131-0608- -0 |  |  | TERMINAL,PIN:PRESSFIT/PCB;;MALE,STR (QUANTITY OF 4) | 22526 | 48283-018 |
| A12J790 | 131-0608-0 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 5) | 22526 | 48283-018 |
| A12L976 | 108-0538-0 |  |  | COIL,RF:FIXED,2.7UH | O.JR03 | 108-0538-0 |
| A12L984 | 108-0538-00 |  |  | COIL,RF:FIXED,2.7UH | OJR03 | 108-0538-00 |
| A12L990 | 108-0538-00 |  |  | COIL,RF:FIXED,2.7UH | OJR03 | 108-0538-0 |
| A12L992 | 108-0538-00 |  |  | COIL,RF:FIXED,2.7UH | OJR03 | 108-0538-00 |
| A12LS498 | 119-1427-01 |  |  | XDCR,AUDIO:1-4.2KHZ,30MA,6V | TK6051 | CB-168P06B |
| A12P126 | 131-0993-00 |  |  | CONN,BOX:SHUNT/SHORTING,;FEMALE,STR | 22526 | 65474-006 |
| A12P127 | 131-0993-00 |  |  | CONN,BOX:SHUNT/SHORTING,;FEMALE,STR | 22526 | 65474-006 |
| A12P128 | 131-0993-00 |  |  | CONN,BOX:SHUNT/SHORTING,;FEMALE,STR | 22526 | 65474-006 |


| Component Number | Tektronix Part No. | Serial Effective | No. Dscont | Name \& Description | Mir. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A12P184 | 131-0993-00 |  |  | CONN,BOX:SHUNT/SHORTING;;FEMALE,STR | 22526 | 65474-006 |
| A12Q104 | 151-0223-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;15V,500MA | 04713 | MPS2369A |
| A12Q107 | 151-0223-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;15V,500MA | 04713 | MPS2369A |
| A12Q244 | 151-0223-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN; 15V,500MA | 04713 | MPS2369A |
| A12Q330 | 151-0188-0 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA (OPTION 05 ONLY) | 04713 | 2N3906 |
| A12Q332 | 151-0223-0 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN; 15V,500MA | 04713 | MPS2369A |
| A12Q419 | 151-1059- 0 |  |  | TRANSISTOR,SIG:JFET,N-CH;10V,30MA(MIN) (OPTION 05 ONLY) | 04713 | MPF4391 |
| A12Q420 | 151-1059-0 |  |  | TRANSISTOR,SIG:JFET,N-CH;10V,3OMA(MIN) (OPTION 05 ONLY) | 04713 | MPF4391 |
| A12Q422 | 151-0188-00 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA (OPTION 05 ONLY) | 04713 | 2N3906 |
| A12Q502 | 151-0188-00 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP;4OV,200MA (OPTION 05 ONLY) | 04713 | 2N3906 |
| A12Q504 | 151-0188-00 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA (OPTION 05 ONLY) | 04713 | 2N3906 |
| A12Q510 | 151-0188-00 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP:40V,200MA (OPTION 05 ONLY) | 04713 | 2N3906 |
| A12Q512 | 151-0188-00 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA (OPTION 05 ONLY) | 04713 | 2N3906 |
| A12Q514 | 151-1059-00 |  |  | TRANSISTOR,SIG:JFET,N-CH;10V,3OMA(MIN) (OPTION 05 ONLY) | 04713 | MPF4391 |
| A12Q588 | 151-0188-00 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A12Q592 | 151-0254-03 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN:30V,500MA | OJR04 | MPSA14, TPE2 |
| A12Q594 | 151-0190-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN:40V,200MA | 04713 | 2N3904 |
| A12Q596 | 151-0190-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA | 04713 | 2N3904 |
| A12Q612 | 151-0188-0 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP:40V,200MA (OPTION 05 ONLY) | 04713 | 2N3906 |
| A12Q710 | 151-1059-00 |  |  | TRANSISTOR,SIG:JFET,N-CH;10V,3OMA(MIN) (OPTION 05 ONLY) | 04713 | MPF4391 |
| A12Q720 | 151-0223-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN:15V,500MA | 04713 | MPS2369A |
| A12Q804 | 151-0622-00 | B010100 | B013314 | TRANSISTOR,SIG:BIPOLAR,PNP:40V, 1.0A,50MHZ | 04713 | MPS6727 |
| A120806 | 151-0192-05 | B010100 | B013314 | TRANSISTOR,SIG:BIPOLAR,NPN:25V.100MA | 04713 | SPS8801RLRP |
| A120842 | 151-0223-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN: $15 \mathrm{~V}, 500 \mathrm{MA}$ | 04713 | MPS2369A |
| A12Q960 | 151-0223-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN:15V.500MA | 04713 | MPS2369A |
| A12R102 | 315-0621-00 |  |  | RES,FXD,FILM: 620 OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R103 | 313-1181-00 |  |  | RES,FXD,FILM: 180 OHM, $5 \% 0.2 \mathrm{~W}$ | 91637 | CCF50-2-180ROS |
| A12R104 | 313-1470-00 |  |  | RES,FXD,FILM:47 OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-47ROOJ |
| A12R105 | 313-1390-00 |  |  | RES,FXD,FILM: 39 OHM, 5\%,0.2W | 91637 | CCF50-2-39R00J |
| A12R106 | 313-1181-00 |  |  | RES,FXD,FILM: 180 OHM, $5 \% 0.2 \mathrm{~W}$ | 91637 | CCF50-2-180ROJ |
| A12R107 | 313-1470-00 |  |  | RES,FXD,FILM:47 OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-47R00J |
| A12R108 | 313-1102-0 |  |  | RES,FXD,FILM:1K OHM,5\%,0.2W | 91637 | CCF50-2-10000J |


| Component Number | Tektronix Part No. | Serial No. Effective Dscont | Name \& Description | Mfr. <br> Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A12R120 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A12R122 | 313-1470-00 |  | RES,FXD,FILM:47 OHM,5\%,0.2W | 91637 | CCF50-2-47R00J |
| A12R208 | 315-0102-0 |  | RES,FXD,FILM:1K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R210 | 315-0123-0 |  | RES,FXD,FILM:12K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R212 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R214 | 315-0683-00 |  | RES,FXD,FILM:68K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R218 | 315-0101-0 |  | RES,FXD,FILM: 100 OHM. $5 \%, 0.25 \mathrm{~W}$ (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R224 | 315-0393-00 |  | RES,FXD,FILM:39K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R226 | 315-0104-00 |  | RES,FXD.FILM:100K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R228 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R234 | 315-0751-00 |  | RES,FXD,FILM:750 OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R244 | 315-0473-00 |  | RES,FXD,FILM:47K OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A12R246 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A12R274 | 313-1153-00 |  | RES,FXD,FILM:15K,5\%,0.2W | 91637 | CCF50-2-15001J |
| A12R276 | 315-0104-0 |  | RES,FXD,FILM: 100 K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A12R300 | 313-1102-00 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000 |
| A12R308 | 315-0162-0 |  | RES,FXD,FILM:1.6K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R314 | 315-0474- |  | RES,FXD,FILM:470K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R320 | 315-0202-0 |  | RES,FXD,FILM:2K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R321 | 315-0222-0 |  | RES,FXD,FILM:2.2K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R322 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R323 | 315-0514-00 |  | RES,FXD,FILM:510K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R324 | 315-0123-00 |  | RES,FXD,FILM:12K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R325 | 315-0154-00 |  | RES,FXD,FILM:150K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R326 | 315-0563-00 |  | RES,FXD,FILM:56K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R327 | 315-0472-00 |  | RES,FXD,FILM:4.7K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R328 | 315-0203-00 |  | RES,FXD.FILM:20K OHM,5\%,0.25W (OPTION 05 ONLY | TK1727 | SFR25 2322-181 |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mir. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A12R329 | 315-0824-00 |  | RES,FXD,FILM:820K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R330 | 315-0683-00 |  | RES,FXD,FILM:68K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R332 | 313-1102-00 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000 J |
| A12R334 | 315-0272-0 |  | RES,FXD,FILM:2.7K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R336 | 315-0333-0 |  | RES,FXD,FILM:33K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R338 | 315-0103-0 |  | RES,FXD,FILM:10K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R342 | 313-1103-00 |  | RES,FXD,FILM: 10 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10001J |
| A12R344 | 321-0222-00 |  | RES,FXD,FILM:2.00K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033ED2K00F |
| A12R346 | 321-0193-00 |  | RES,FXD,FILM: 1 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ To | TK1727 | MR25 2322-151-1 |
| A12R348 | 321-0222-00 |  | RES,FXD,FILM:2.00K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033ED2K00F |
| A12R349 | 315-0102-0 |  | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A12R370 | 313-1201-0 |  | RES,FXD,FILM:200 OHM,5\%,0.2W | 91637 | CCF50-2-200ROJ |
| A12R374 | 315-0102-0 |  | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A12R376 | 315-0201-00 |  | RES,FXD,FILM:200 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A12R378 | 313-1103-00 |  | RES,FXD,FLLM: 10 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10001J |
| A12R401 | 307-0104-00 |  | RES,FXD,CMPSN:3.3 OHM,5\%,0.25W (OPTION 05 ONLY) | 19701 | 5043CX3R300. |
| A12R402 | 315-0223-00 |  | RES,FXD,FILM:22K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R403 | 315-0332-00 |  | RES,FXD,FILM:3.3K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R404 | 315-0471-0 |  | RES,FXD,FILM:470 OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R405 | 315-0182- |  | RES,FXD,FILM:1.8K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R406 | 315-0911-00 |  | RES,FXD,FILM:910 OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R407 | 315-0123-00 |  | RES,FXD,FILM:12K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R408 | 315-0512-00 |  | RES,FXD,FILM:5.1K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R409 | 315-0112-00 |  | RES,FXD,FILM:1.1K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R410 | 315-0243-00 |  | RES,FXD,FILM:24K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R411 | 315-0243-00 |  | RES,FXD,FILM:24K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R412 | 315-0104-00 |  | RES,FXD,FILM:100K OHM, $5 \%, 0.25 \mathrm{~W}$ (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R413 | 315-0104-00 |  | RES,FXD,FILM:100K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mrt. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A12R414 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R415 | 315-0273-00 |  | RES,FXD,FILM:27K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R416 | 315-0104-0 |  | RES,FXD,FILM:100K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R417 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R418 | 315-0391-00 |  | RES,FXD,FILM:390 OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R419 | 311-2100-00 |  | RES,VAR,NONWW:TRMR,1K OHM,10\%,0.5W (OPTION 05 ONLY) | 32997 | 3386M-1-102 |
| A12R420 | 315-0104-00 |  | RES,FXD,FILM:100K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R421 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R422 | 315-0392-00 |  | RES,FXD,FILM:3.9K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R423 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R424 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R425 | 315-0103-0 |  | RES,FXD,FILM:10K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R426 | 315-0203-00 |  | RES,FXD,FILM:20K OHM,5\%,0.25W (OPTION 05 ONLY | TK1727 | SFR25 2322-181 |
| A12R427 | 315-0163-00 |  | RES,FXD,FILM:16K OHM,5\%,0.25W (OPTION 05 ONLY | TK1727 | SFR25 2322-181 |
| A12R428 | 315-0334-00 |  | RES,FXD,FILM:330K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R429 | 315-0204-00 |  | RES,FXD,FILM:200K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R474 | 307-0446-00 |  | RES NTWK,FXD,FI:10K OHM,20\%,(9)RES | 11236 | 750-101-R10K |
| A12R479 | 315-0103-00 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A12R502 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R506 | 315-0432-00 |  | RES,FXD,FILM:4.3K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R512 | 315-0333-00 |  | RES,FXD,FILM:33K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R524 | 315-0511-0 |  | RES,FXD,FILM:510 OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R529 | 315-0101-0 |  | RES,FXD,FILM: 100 OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R572 | 313-1103-00 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10001J |
| A12R580 | 313-1241-00 |  | RES,FXD,FILM:240 OHM,5\%,0.2W | 91637 | CCF50-2-240ROJ |
| A12R582 | 315-0241-00 |  | RES,FXD,FILM:240 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A12R584 | 315-0101-00 |  | RES,FXD,FILM:100 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A12R590 | 307-0446-00 |  | RES NTWK,FXD,FI:10K OHM,20\%,(9)RES | 11236 | 750-101-R10K |
| A12R592 | 313-1102-0 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000J |
| A12R594 | 313-1472-0 |  | RES,FXD,FILM:4.7K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-47000J |
| A12R596 | 313-1103-0 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A12R597 | 313-1102-0 |  | RES,FXD,FILM:1K OHM,5\%,0.2W | 91637 | CCF50-2-10000J |
| A12R598 | 313-1512-00 |  | RES,FXD,FILM:5.1K OHM,5\%,0.2W | 91637 | CCF50-2-51000J |
| A12R602 | 315-0122-00 |  | RES,FXD,FILM:1,2K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R603 | 315-0392-00 |  | RES,FXD,FILM:3.9K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R604 | 315-0472-00 |  | RES,FXD,FILM:4.7K OHM,5\%,0.25W (OPTION 05 ONLY | TK1727 | SFR25 2322-181 |
| A12R606 | 315-0303-00 |  | RES,FXD,FILM:3OK OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R607 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R608 | 315-0102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R609 | 315-0102-0 |  | RES,FXD,FILM:1K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R610 | 315-0475-00 |  | RES,FXD,FILM:4.7M OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R611 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R612 | 315-0103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R613 | 315-0201-00 |  | RES,FXD,FILM:200 OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R614 | 315-0471-00 |  | RES,FXD,FILM:470 OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R616 | 315-0470-0 |  | RES,FXD,FILM:47 OHM,5\%,0.25W (OPTION 05 ONLY | TK1727 | SFR25 2322-181 |
| A12R617 | 315-0222-00 |  | RES,FXD,FILM:2.2K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R622 | 321-0226-00 |  | RES,FXD,FILM:2.21K OHM, 1\%,0.125W,TC=TO (OPTION 05 ONLY) | 19701 | 5043ED2K210F |
| A12R624 | 315-0100-00 |  | RES,FXD,FILM:10 OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-182 |
| A12R626 | 315-0101-0 |  | RES,FXD,FILM:100 OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R628 | 313-1102-00 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000J |
| A12R646 | 313-1102-00 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000 J |
| A12R648 | 313-1102-00 |  | RES,FXD,FILM:1K OHM, 5\%,0.2W | 91637 | CCF50-2-10000J |
| A12R700 | 321-0251-00 |  | RES,FXD,FILM:4.02K OHM, $1 \%, 0.125 W, T C=$ TO (OPTION 05 ONLY) | 19701 | 5043ED4K020F |


| Component Number | Tektronix Part No. | Seria Effective | No. Dscont | Name \& Description : | Mtr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A12R701 | 313-1102-00 | B010100 | B013314 | RES,FXD,FILM:1K OHM,5\%,0.2W | 91637 | CCF50-2-10000J |
| A12R711 | 315-0475-00 |  |  | RES,FXD.FILM:4.7M OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R712 | 315-0102-00 |  |  | RES,FXD,FILM:1K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R713 | 315-0564-00 |  |  | RES,FXD,FILM:560K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R714 | 315-0394-00 |  |  | RES,FXD,FILM:390K OHM,5\%,0.25W (OPTION 05 ONLY | TK1727 | SFR25 2322-181 |
| A12R715 | 315-0392-00 |  |  | RES,FXD,FILM:3.9K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R716 | 315-0620-00 |  |  | RES,FXD,FILM:62 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A12R717 | 313-1181-00 |  |  | RES,FXD,FILM:180 OHM,5\%0.2W | 91637 | CCF50-2-180R0J |
| A12R718 | 313-1470-00 |  |  | RES,FXD,FILM: 47 OHM,5\%,0.2W | 91637 | CCF50-2-47ROOJ |
| A12R719 | 315-0100-00 |  |  | RES,FXD,FILM:10 OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-182 |
| A12R722 | 313-1102-00 |  |  | RES,FXD,FILM:1K OHM,5\%,0.2W | 91637 | CCF50-2-10000 |
| A12R742 | 307-0446-00 |  |  | RES NTWK,FXD,FI:10K OHM,20\%,(9)RES | 11236 | 750-101-R10K |
| A12R744 | 315-0103-00 |  |  | RES,FXD,FILM:10K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A12R746 | 315-0103-00 |  |  | RES,FXD,FILM: 10 K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A12R748 | 313-1102-00 |  |  | RES,FXD,FILM:1K OHM,5\%,0.2W | 91637 | CCF50-2-10000 J |
| A12R764 | 313-1102-00 |  |  | RES,FXD,FILM:1K OHM, $5 \%, 0.2 W$ | 91637 | CCF50-2-10000J |
| A12R792 | 313-1151-00 |  |  | RES,FXD,FILM:150 OHM,5\%,0.2W | 91637 | CCF50-2-150ROJ |
| A12R794 | 313-1151-00 |  |  | RES,FXD,FILM:150 OHM,5\%,0.2W | 91637 | CCF50-2-150ROJ |
| A12R796 | 313-1151-0 |  |  | RES,FXD,FILM: 150 OHM,5\%,0.2W | 91637 | CCF50-2-150ROJ |
| A12R800 | 313-1561-0 | B010100 | B013314 | RES,FXD,FILM:560 OHM,5\%,0.2W | 91637 | CCF50-2-560ROJ |
| A12R801 | 313-1392-00 | B013315 |  | RES,FXD,FILM:3.9K OHM,5\%,0.2W | 91637 | CCF50-2-39000J |
| A12R802 | 315-0106-00 | B010100 | B013314 | RES,FXD,FILM:10M OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A12R810 | 315-0121-0 |  |  | RES,FXD,FILM:120 OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R812 | 322-3235-00 | B010100 | B013314 | RES,FXD:METAL FILM;2.74K OHM,1\%,0.2W,TC=100 | 91637 | CCF501G27400F |
| A12R814 | 313-1512-00 | B010100 | B013314 | RES,FXD,FILM:5.1K OHM,5\%,0.2W | 91637 | CCF50-2-51000J |
| A12R816 | 315-0102-0 |  |  | RES,FXD,FILM: 1 K OHM,5\%,0.25W (OPTION 05 ONLY) | TK1727 | SFR25 2322-181 |
| A12R820 | 313-1560-00 |  |  | RES,FXD,FILM:56 OHM,5\%,0.2W | 91637 | CCF50-2-56R00J |
| A12R822 | 313-1560-00 |  |  | RES,FXD,FILM:56 OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-56R00J |
| A12R830 | 307-0675-00 |  |  | RES NTWK,FXD,FI:(9),1K OHM,2\%,1.25W | 11236 | 750-101-R1K OHM |
| A12R894 | 313-1102-00 |  |  | RES,FXD,FILM: 1 K OHM,5\%,0.2W | 91637 | CCF50-2-10000J |
| A12R896 | 313-1102-00 |  |  | RES,FXD,FILM: 1 K OHM,5\%,0.2W | 91637 | CCF50-2-10000J |
| A12R900 | 313-1103-00 |  |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A12R936 | 313-1204-00 |  |  | RES,FXD,FILM:200K,5\%,0.2W | 91637 | CCF50-2-20002J |
| A12R940 | 313-1103-00 |  |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A12R941 | 313-1102-0 |  |  | RES,FXD,FILM:1K OHM,5\%,0.2W | 91637 | CCF50-2-10000 J |


| Component Number | Tektronix Part No. | Serial No. Effective Dscont | Name \& Description | Mir. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A12R945 | 313-1472-00 |  | RES,FXD,FILM:4.7K OHM, 5\%,0.2W | 91637 | CCF50-2-47000J |
| A12R946 | 313-1103-00 |  | RES,FXD,FILM: 10 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10001J |
| A12R948 | 313-1183-0 |  | RES,FXD,FILM:18K OHM,5\%,0.2W | 91637 | CCF50-2-18001J |
| A12R952 | 322-3222- |  | RES,FXD:METAL FILM; 2 K OHM,1\%,0.2W | 91637 | CCF501G20000F |
| A12R954 | 322-3193-00 |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A12R956 | 322-3222-0 |  | RES,FXD:METAL FILM;2K OHM, 1\%,0.2W | 91637 | CCF501G20000F |
| A12R957 | 313-1102-00 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000 |
| A12TP332 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB; MALE,STR | 22526 | 48283-018 |
| A12TP370 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A12TP371 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB;,MALE,STR | 22526 | 48283-018 |
| A12TP372 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A12TP373 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A12TP374 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A12TP375 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A12TP378 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A12TP562 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A12TP574 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A12TP576 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A12TP578 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A12TP580 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A12TP664 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A12TP774 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A12TP820 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A12TP840 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A12TP842 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A12TP902 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A12U120 | 156-1962-00 |  | IC,DIGITAL:FTTL,BUFFER | 04713 | MC74F244N |
| A12U130 | 156-1800-0 |  | IC,DIGITAL:FTTL,GATES;QUAD 2-INPUT | 04713 | MC74F86N |
| A12U132 | 156-1724-00 |  | IC,DIGITAL:FTTL,GATES;QUAD 2-INPUT | 04713 | MC74F32N |
| A12U220 | 156-0366-00 | B010100 B011178 | IC,DIGITAL:CMOS,FLIP FLOP;DUAL D-TYPE | 04713 | MC14013BCP |
| A12U220 | 156-0366-04 | B011179 | IC,DIGITAL:CMOS,FLIP FLOP:DUAL D-TYPE (OPTION 05 ONLY) | 34371 | CD4013BE |
| A12U250 | 156-0739-00 |  | IC,DIGITAL:STTL,GATES;QUAD 2-INPUT | 01295 | SN74S32N |
| A12U254 | 156-0323-00 |  | IC,DIGITAL:STTL,GATES; HEX INV | 01295 | SN74SO4N |
| A12U260 | 156-1220-01 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 01295 | SN74LS365AN |
| A12U262 | 156-1220-01 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 01295 | SN74LS365AN |
| A12U264 | 156-0739-0 |  | IC,DIGITAL:STTL,GATES;QUAD 2-INPUT | 01295 | SN74S32N |
| A12U270 | 156-0323- |  | IC,DIGITAL:STTL,GATES;HEXINV | 01295 | SN74S04N |
| A12U274 | 156-0402-00 |  | IC,MISC:BIPOLAR,TIMER | 27014 | LM555CN |
| A12U276 | 156-1663-00 |  | IC,DIGITAL:FTTL,GATE;TRIPLE 3-INPUT | 04713 | MC74F11N |


| Component Number | Tektronix <br> Part No. | Serial Effective | No. Dscont | Name \& Description | Mir. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A12U308 | 156-0575-00 |  |  | IC,DIGITAL:CMOS,GATE;TRIPLE 3-INPUT (OPTION 05 ONLY) | 04713 | MC14025BCP |
| A12U310 | 156-0366-0 | B010100 | B011178 | IC,DIGITAL:CMOS,FLIP FLOP;DUAL D-TYPE | 04713 | MC14013BCP |
| A12U310 | 156-0366-04 | B011179 |  | IC,DIGITAL:CMOS,FLIP FLOP;DUAL D-TYPE (OPTION 05 ONLY) | 34371 | CD4013BE |
| A12U314 | 156-0704-0 |  |  | IC,MISC:CMOS,PLL:LOW SPEED (OPTION 05 ONLY | 04713 | MC14046BCP |
| A12U332 | 156-0479-00 |  |  | IC,DIGITAL:LSTTL,GATES;QUAD 2-iNPUT | 01295 | SN74LS32N |
| A12U350 | 156-3103-00 | B010100 | B013314 | IC,MEMORY:CMOS,SRAM; $32 \mathrm{~K} \times 8.120 \mathrm{NS}$ | TK2540 | CXK58257P-12L |
| A12U350 | 156-3870-00 | B013315 |  | IC,MEMORY:CMOS,NVRAM;32K X 8,120NS | OBOA9 | DS1230AB-120 |
| A12U352 | 156-1725-00 |  |  | IC,DIGITAL:FTTL,BUS TRANSCEIVER | 04713 | MC74F245 N OR J |
| A12U360 | 156-1725-00 |  |  | IC,DIGITAL:FTTL,BUS TRANSCEIVER | 04713 | MC74F245 N OR J |
| A12U364 | 156-1721-00 |  |  | IC,DIGITAL:FTTL,LATCH;OCTAL D-TYPE | 04713 | MC74F373N |
| A12U366 | 156-1662-0 |  |  | IC,DIGITAL:FTTL,MUX;DUAL 4-TO-1 DATA | 04713 | MC74F153N |
| A12U410 | 156-1381-0 |  |  | IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY (OPTION 05 ONLY) | 34371 | CA3096AE-17 |
| A12U420 | 156-1381-00 |  |  | IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY (OPTION 05 ONLY) | 34371 | CA3096AE-17 |
| A12U424 | 156-0385-00 |  |  | IC,DIGITAL:LSTTL,GATES;HEX INV | 01295 | SN74LS04N |
| A12U430 | 156-0366-00 | B010100 | B011178 | IC,DIGITAL:CMOS,FLIP FLOP;DUAL D-TYPE | 04713 | MC14013BCP |
| A12U430 | 156-0366-04 | B011179 |  | IC,DIGITAL:CMOS,FLIP FLOP;DUAL D-TYPE (OPTION 05 ONLY | 34371 | CD4013BE |
| A12U432 | 156-0459-0 |  |  | IC,DIGITAL:STTL,GATES;QUAD 2-INPUT | 01295 | SN74S08N |
| A12U440 | 156-2274-0 |  |  | IC,MEMORY:CMOS,SRAM;8K X 8,120NS | 62786 | HM6264LP-12 |
| A12U470 | 156-2380-0 |  |  | IC,ASIC:HMOS,CUSTOM WAVEFORM PROCESSOR | 66302 | VF4101RC CC0001 |
| A12U480 | 160-4946-00 | 8010100 | B010662 | MICROCKT,DGTL:8192 $\times 8$ PROM.PRGM | 80009 | 160494600 |
| A12U480 | 160-4946-01 | B010663 | B011820 | MICROCKT,DGTL:8192 $\times 8$ EPROM,PRGM | 80009 | 160494601 |
| A12U480 | 160-4946-03 | B011821 |  | MICROCKT,DGTL:8192 X 8 EPROM,PRGM (STANDARD) | 80009 | 160494603 |
| A12U480 | 160-4946-01 | B010100 | B010105 | MICROCKT,DGTL:8192 X 8 EPROM,PRGM | 80009 | 160494601 |
| A12U480 | 160-6496-03 | B010106 |  | MICROCKT,DGTL:8192 X 8 EPROM,PRGM (2440M) | 80009 | 160649603 |
| A12U490 | 160-4947-00 | B010100 | B010662 | MICROCKT,DGTL:8192 X 8 PROM,PRGM | 80009 | 160494700 |
| A12U490 | 160-4947-01 | B010663 | B011820 | MICROCKT,DGTL: $8192 \times 8$ EPROM,PRGM | 80009 | 160494701 |
| A12U490 | 160-4947-03 | B011821 |  | MICROCKT,DGTL:8192 X 8 EPROM,PRGM (STANDARD) | 80009 | 160494703 |
| A12U490 | 160-4947-01 | B010100 | B010105 | MICROCKT,DGTL:8192 X 8 EPROM,PRGM | 80009 | 160494701 |
| A12U490 | 160-6497-03 | B010106 |  | MICROCKT,DGTL:8192 X 8 EPROM,PRGM (2440M) | 80009 | 160649703 |
| A12U504 | 156-0912-01 |  |  | IC,LINEAR:BIPOLAR,OP-AMP (OPTION 05 ONLY) | 27014 | LM3080N/A |
| A12U510 | 156-0912-01 |  |  | IC,LINEAR:BIPOLAR,OP-AMP (OPTION 05 ONLY) | 27014 | LM3080N/A |
| A12U514 | 156-0912-01 |  |  | IC,LINEAR:BIPOLAR,OP-AMP (OPTION 05 ONLY) | 27014 | LM3080N/A+ |


| Component Number | Tektronlx <br> Part No. | Seria Effective | No. Dscont | Name \& Description | Mir. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A12U520 | 156-0912-01 |  |  | IC,LINEAR:BIPOLAR,OP-AMP (OPTION 05 ONLY) | 27014 | LM3080N/A |
| A12U524 | 156-0388-0 |  |  | IC,DIGITAL:LSTTL,FLIP FLOP (OPTION 05 ONLY) | 01295 | SN74LS74AN |
| A12U530 | 156-1426-00 |  |  | IC.PROCESSOR:NMOS,PERIPHERAL (OPTION 05 ONLY) | 04713 | MC68B40 |
| A12U532 | 156-1111-02 |  |  | IC,DIGITAL:LSTTL,TRANSCEIVER | 01295 | SN74LS245N |
| A12U540 | 156-0469-00 |  |  | IC,DIGITAL:LSTTL,DEMUXJDECODER | 01295 | SN74LS138 |
| A12U541 | 156-0382-00 |  |  | IC,DIGITAL:LSTTL,GATE;QUAD 2-INPUT NAND (OPTION 05 ONLY) | 01295 | SN74LSOON |
| A12U542 | 156-1962-00 |  |  | IC,DIGITAL:FTTL,BUFFER;OCTAL | 04713 | MC74F244N |
| A12U550 | 156-1326-00 |  |  | IC,DIGITAL:LSTTL,FLIP FLOP;QUAD D-TYPE,COMP | 01295 | SN74LS379N |
| A12U552 | 156-1111-02 |  |  | IC,DIGITAL:LSTTL.TRANSCEIVER | 01295 | SN74LS245N |
| A12U560 | 156-1962-00 |  |  | IC,DIGITAL:FTTL,BUFFER;OCTAL | 04713 | MC74F244N |
| A12U562 | 156-1721-00 |  |  | IC,DIGITAL:FTTL,LATCH:OCTAL D-TYPE | 04713 | MC74F373N |
| A12U564 | 156-0956-00 |  |  | IC.DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV | 01295 | SN74LS244N3 |
| A12U570 | 156-0694-00 |  |  | IC,DIGITAL:STTL,DEMUX/DECODER;3-TO-8 | 01295 | SN74S138AN |
| A12U572 | 156-1722-0 |  |  | IC,DIGITAL:FTTL,GATE;HEX INV | 04713 | MC74F04N |
| A12U580 | 156-0459-0 |  |  | IC,DIGITAL:STTL,GATES;QUAD 2-INPUT | 01295 | SN74S08N |
| A12U610 | 156-0048-0 |  |  | IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY (OPTION 05 ONLY) | 04713 | MC3346P |
| A12U612 | 156-1349-0 |  |  | IC,LINEAR:BIPOLAR,AMPLIFIER;DUAL (OPTION 05 ONLY) | 34371 | CA3054-98 |
| A12U624 | 156-1414-0 |  |  | IC,DIGITAL:LSTTL,TRANSCEIVER | 01295 | SN75160BN |
| A12U630 | 156-1444-01 |  |  | IC,PROCESSOR:NMOS,CONTROLLER:GPIB ADAPTER | 01295 | TMS9914A |
| A12U632 | 156-0956-00 |  |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 01295 | SN74LS244N3 |
| A12U640 | 156-1494-01 |  |  | IC,PROCESSOR:NMOS,MICROPROCESSOR | 04713 | MC68B09P |
| A12U650 | 156-1111-02 |  |  | IC,DIGITAL:LSTTL,TRANSCEIVER | 01295 | SN74LS245N |
| A12U654 | 156-0956-00 |  |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 01295 | SN74LS244N3 |
| A12U660 | 156-1111-02 |  |  | IC,DIGITAL:LSTTL,TRANSCEIVER | 01295 | SN74LS245N |
| A12U664 | 156-3103-00 | B010100 | B013314 | IC,MEMORY:CMOS,SRAM;32K X 8,12ONS | TK2540 | CXK58257P-12L |
| A12U664 | 156-3870-0 | B013315 |  | IC,MEMORY:CMOS,NVRAM;32K X 8,120NS | OBOA9 | DS1230AB-120 |
| A12U668 | 156-1727-00 |  |  | IC,DIGITAL:FTTL,DEMUXJDECODER | 04713 | MC74F138 N |
| A12U670 | 160-4941-00 | B010100 | B010197 | MICROCKT,DGTL:16384 X 8 EPROM,PRGM | 80009 | 160494100 |
| A12U670 | 160-4941-01 | B010198 | B010662 | MICROCKT,DGTL:16384 X 8 EPROM,PRGM | 80009 | 160494101 |
| A12U670 | 160-4941-03 | B010663 | B010779 | MICROCKT,DGTL:16384 X 8 EPROM,PRGM | 80009 | 160494103 |
| A12U670 | 160-4941-04 | B010780 | B011820 | MICROCKT,DGTL:16384 X 8 EPROM,PRGM | 80009 | 160494104 |
| A12U670 | 160-4941-05 | B011821 | B011872 | MICROCKT,DGTL:16384 X 8 EPROM,PRGM | 80009 | 160494105 |
| A12U670 | 160-4941-06 | B011873 | B012859 | MICROCKT,DGTL:16384 X 8 EPROM PRGM | 80009 | 160494106 |
| A12U670 | 160-4941-07 | B012860 |  | MICROCKT,DGTL: 16384 X 8 EPROM,PRGM (STANDARD) | 80009 | 160494107 |


| Component Number | Tektronix Part No. | Seria Effective | INo. Dscont | Name \& Description | Mrr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A12U670 | 160-4941-03 |  |  | MICROCKT,DGTL:16384 X 8 EPROM,PRGM (2440M) | 80009 | 160494103 |
| A12U680 | 160-4942-0 | B010100 | B010197 | MICROCKT,DGTL:65536 $\times 8$ EPROM,PRGM | 80009 | 160494200 |
| A12U680 | 160-4942-01 | B010198 | B010662 | MICROCKT,DGTL:65536 $\times 8$ EPROM,PRGM | 80009 | 160494201 |
| A12U680 | 160-4942-03 | B010663 | B010779 | MICROCKT,DGTL:65536 $\times 8$ EPROM,PRGM | 80009 | 160494203 |
| A12U680 | 160-4942-04 | B010780 | B011820 | MICROCKT,DGTL:65536 $\times 8$ EPROM,PRGM | 80009 | 160494204 |
| A12U680 | 160-4942-05 | B011821 | B011872 | MICROCKT,DGTL: $65536 \times 8$ EPROM,PRGM | 80009 | 160494205 |
| A12U680 | 160-4942-06 | B011873 | B012859 | MICROCKT,DGTL:65536 $\times 8$ EPROM PRGM | 80009 | 160494206 |
| A12U680 | 160-4942-07 | B012860 |  | MICROCKT,DGTL:65536 X 8 EPROM,PRGM (STANDARD) | 80009 | 160494207 |
| A12U680 | 160-4942-03 |  |  | MICROCKT,DGTL:65536 X 8 EPROM,PRGM (2440M) | 80009 | 160494203 |
| A12U682 | 160-4943-00 | B010100 | B010197 | MICROCKT,DGTL:65536 $\times 8$ EPROM,PRGM | 80009 | 160494300 |
| A12U682 | 160-4943-01 | B010198 | B010662 | MICROCKT,DGTL:65536 $\times 8$ EPROM,PRGM | 80009 | 160494301 |
| A12U682 | 160-4943-03 | B010663 | B010779 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160494303 |
| A12U682 | 160-4943-04 | B010780 | B011820 | MICROCKT;DGTL:65536 $\times 8$ EPROM,PRGM | 80009 | 160494304 |
| A12U682 | 160-4943-05 | B011821 | B011872 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160494305 |
| A12U682 | 160-4943-06 | B011873 | B012859 | MICROCKT,DGTL:65536 $\times 8$ EPROM PRGM | 80009 | 160494306 |
| A12U682 | 160-4943-07 | B012860 |  | MICROCKT,DGTL:65536 X 8 EPROM,PRGM (STANDARD) | 80009 | 160494307 |
| A12U682 | 160-4943-03 |  |  | MICROCKT,DGTL:65536 X 8 EPROM,PRGM (2440M) | 80009 | 160494303 |
| A12U690 | 160-4944-00 | B010100 | B010197 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160494400 |
| A12U690 | 160-4944-01 | 8010198 | B010662 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160494401 |
| A12U690 | 160-4944-03 | B010663 | B010779 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160494403 |
| A12U690 | 160-4944-04 | B010780 | B011820 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160494404 |
| A12U690 | 160-4944-05 | B011821 | B011872 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160494405 |
| A12U690 | 160-4944-06 | B011873 | B012859 | MICROCKT,DGTL:65536 $\times 8$ EPROM PRGM | 80009 | 160494406 |
| A12U690 | 160-4944-07 | B012860 |  | MICROCKT,DGTL:65536 X 8 EPROM,PRGM (STANDARD) | 80009 | 160494407 |
| A12U690 | 160-4944-03 |  |  | MICROCKT,DGTL:65536 X 8 EPROM,PRGM (2440M) | 80009 | 160494403 |
| A12U692 | 160-4945-00 | B010100 | B010197 | MICROCKT,DGTL:65536 X 8 EPROM.PRGM | 80009 | 160494500 |
| A12U692 | 160-4945-01 | B010198 | B010662 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160494501 |
| A12U692 | 160-4945-03 | B010663 | B010779 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160494503 |
| A12U692 | 160-4945-04 | B010780 | B011820 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160494504 |
| A12U692 | 160-4945-05 | B011821 | B011872 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160494505 |
| A12U692 | 160-4945-06 | B011873 | B012859 | MICROCKT,DGTL:65536 X 8 EPROM PRGM | 80009 | 160494506 |
| A12U692 | 160-4945-07 | B012860 |  | MICROCKT,DGTL:65536 X 8 EPROM,PRGM (STANDARD) | 80009 | 160494507 |
| A12U692 | 160-5841-00 | B010100 | B010197 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584100 |
| A12U692 | 160-5841-01 | B010198 | B010662 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584101 |
| A12U692 | 160-5841-02 | B010663 | B010779 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584102 |


| Component Number | Tektronix Part No. | Serial Effective | No. Dscont | Name \& Description | Mtr. <br> Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A12U692 | 160-5841-04 | B010780 | B011820 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584104 |
| A12U692 | 160-5841-05 | B011821 | B012859 | MICROCKT,DGTL: $65536 \times 8$ EPROM | 80009 | 160584105 |
| A12U692 | 160-5841-07 | B012860 |  | MICROCKT,DGTL:65536 X 8 EPROM,PRGM (FRENCH HELP TEXT) | 80009 | 160584107 |
| A12U692 | 160-5842-0 | B010100 | B010197 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584200 |
| A12U692 | 160-5842-01 | B010198 | B010662 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584201 |
| A12U692 | 160-5842-02 | B010663 | B010779 | MICROCKT,DGTL:65536 $\times 8$ EPROM,PRGM | 80009 | 160584202 |
| A12U692 | 160-5842-04 | B010780 | B011820 | MICROCKT,DGTL:65536 $\times 8$ EPROM,PRGM | 80009 | 160584204 |
| A12U692 | 160-5842-05 | B011821 | B012859 | MICROCKT,DGTL:65536 X 8 EPROM | 80009 | 160584205 |
| A12U692 | 160-5842-07 | B012860 |  | MICROCKT,DGTL:65536 $\times 8$ EPROM,PRGM (GERMAN HELP TEXT) | 80009 | 160584207 |
| A12U692 | 160-5843-00 | B010100 | B010197 | MICROCKT,DGTL:65536 $\times 8$ EPROM,PRGM | 80009 | 160584300 |
| A12U692 | 160-5843-01 | B010198 | B010662 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584301 |
| A12U692 | 160-5843-02 | B010663 | B010779 | MICROCKT,DGTL:65536 $\times 8$ EPROM,PRGM | 80009 | 160584302 |
| A12U692 | 160-5843-04 | B010780 | B011820 | MICROCKT,DGTL:65536 $\times 8$ EPROM,PRGM | 80009 | 160584304 |
| A12U692 | 160-5843-05 | B011821 | B012859 | MICROCKT,DGTL:65536 X 8 EPROM | 80009 | 160584305 |
| A12U692 | 160-5843-07 | B012860 |  | MICROCKT,DGTL:65536 X 8 EPROM,PRGM (ITALIAN HELP TEXT) | 80009 | 160584307 |
| A12U692 | 160-5844-00 | B010100 | B010197 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584400 |
| A12U692 | 160-5844-01 | B010198 | B010662 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584401 |
| A12U692 | 160-5844-02 | B010663 | B010779 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584402 |
| A12U692 | 160-5844-04 | B010780 | B011820 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584404 |
| A12U692 | 160-5844-05 | B011821 | B012859 | MICROCKT,DGTL:65536 X 8 EPROM | 80009 | 160584405 |
| A12U692 | 160-5844-06 | B012860 |  | MICROCKT,DGTL:65536 X 8 EPROM (SPANISH HELP TEXT) | 80009 | 160584406 |
| A12U692 | 160-5845-00 | B010100 | B010197 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584500 |
| A12U692 | 160-5845-01 | B010198 | B010662 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584501 |
| A12U692 | 160-5845-02 | B010663 | B010779 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584502 |
| A12U692 | 160-5845-04 | B010780 | B011820 | MICROCKT,DGTL:65536 X 8 EPROM,PRGM | 80009 | 160584504 |
| A12U692 | 160-5845-05 | B011821 | B012859 | MICROCKT,DGTL:65536 X 8 EPROM | 80009 | 160584505 |
| A12U692 | 160-5845-07 | B012860 |  | MICROCKT,DGTL:65536 X 8 EPROM,PRGM (DUTCH HELP TEXT) | 80009 | 160584507 |
| A12U692 | 160-4945-03 |  |  | MICROCKT,DGTL:65536 X 8 EPROM,PRGM (2440M) | 80009 | 160494503 |
| A12U710 | 156-1200-01 |  |  | IC,LINEAR:BIFET,OP-AMP (OPTION 05 ONLY) | 01295 | TL074CN |
| A12U720 | 156-2013-00 |  |  | IC,DIGITAL:STTL,TRANSCEIVER | 01295 | SN75162BN |
| A12U730 | 156-0956-00 |  |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 01295 | SN74LS244N3 |
| A12U750 | 156-0865-0 |  |  | IC,DIGITAL:LSTTL,FLIP FLOP;OCTAL D-TYPE | 01295 | SN74LS273N |
| A12U754 | 156-0865-00 |  |  | IC,DIGITAL:LSTTL,FLIP FLOP;OCTAL D-TYPE | 01295 | SN74LS273N |
| A12U760 | 156-0865-00 |  |  | IC,DIGITAL:LSTTL,FLIP FLOP;OCTAL D-TYPE | 01295 | SN74LS273N |
| A12U830 | 156-0914-00 |  |  | IC.DIGITAL:LSTTL,BUFFER/DRIVER:OCTAL INV | 01295 | SN74LS240N |
| A12U840 | 156-1724-00 |  |  | IC.DIGITAL:FTTL,GATES;QUAD 2-INPUT | 04713 | MC74F32N |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mifr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A12U844 | 156-1216-01 |  | IC,DIGITAL:STTL,GATES | 01295 | SN74S37N |
| A12U850 | 156-0985-00 |  | IC,DIGITAL:LSTTL,GATES;DUAL 5-INPUT | 04713 | SN74LS260N |
| A12U854 | 156-0956-00 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER;OCTAL NONINV | 01295 | SN74LS244N3 |
| A12U860 | 156-0865-00 |  | IC,DIGITAL:LSTTL,FUP FLOP;OCTAL D-TYPE | 01295 | SN74LS273N |
| A12U862 | 156-0478-00 |  | IC,DIGITAL:LSTTL,GATE;DUAL 4-INPUT | 01295 | SN74LS21AN |
| A12U866 | 156-0323-00 |  | IC,DIGITAL:STTL,GATES;HEXINV | 01295 | SN74S04N |
| A12U870 | 156-0180-00 |  | IC,DIGITAL:STTL,GATES;QUAD 2-INPUT | 01295 | SN74S00N |
| A12U874 | 156-0382-0 |  | IC,DIGITAL:LSTTL,GATE;QUAD 2-INPUT | 01295 | SN74LSOON |
| A12U880 | 156-0480-00 |  | IC,DIGITAL:LSTTL,GATES;QUAD 2-INPUT | 01295 | SN74LS08N |
| A12U884 | 156-0469-00 |  | IC,DIGITAL:LSTTL,DEMUXJDECODER | 01295 | SN74LS138 |
| A12U890 | 156-0693-00 |  | IC,DIGITAL:STTL,DEMUXIDECODER | 01295 | SN74S139AN |
| A12U894 | 156-0388-00 |  | IC,DIGITAL:LSTTL,FLIP FLOP;DUAL. D | 01295 | SN74LS74AN |
| A12U940 | 156-1191-01 |  | IC,LINEAR:BIFET,OP-AMP | 01295 | TLO72ACP |
| A12U942 | 156-2396-00 |  | IC,MISC:BIPOLAR,PWR SUPPLY SUPERVISOR | 01295 | TL7705 ACP |
| A12VR105 | 152-0278-00 |  | DIODE,ZENER:,;3V,5\%,0.4W | 04713 | 1N4372ARL |
| A12VR234 | 152-0166-00 |  | DIODE,ZENER:;;6.2V,5\%,0.4W (OPTION 05 ONLY) | 04713 | SZ11738RL |
| A12VR717 | 152-0278-00 |  | DIODE,ZENER:,33V,5\%,0.4W | 04713 | 1N4372ARL |
| A12VR816 | 152-0175- |  | DIODE,ZENER:;;5.6V.5\%,0.4W (OPTION 05 ONLY) | 04713 | SZG35008 |
| A12W123 | 175-9353-01 |  | CA ASSY,SP:COAXIAL,;RFP,2,50 OHM COAX,15.0L (OPTION 05 ONLY) | 0.37N9 | ORDER BY DESC |
| A12W130 | 175-9025-0 |  | CA ASSY,SP:RIBBON,;IDC,50,28 AWG,1.7 L | 53387 | ORDER BY DESC |
| A12W800 | 176-0121-0 | B013315 | WIRE,ELECTRICAL:20 AWG,BARE,12.0 L | TK1326 | ORDER BY DESC |
| A12W802 | 131-0566-0 | B013315 | BUS,CONDUCTOR:DUMMY RES, 0.094 OD X 0.225L | 24546 | OMA0207 |
| A12W900 | 131-0566- 0 | B013315 | BUS,CONDUCTOR:DUMMY RES, 0.094 OD X 0.225L | 24546 | OMA0207 |
| A12W902 | 131-0566-0 | B013315 | BUS,CONDUCTOR:DUMMY RES, 0.094 OD X 0.225L | 24546 | OMA0207 |
| A12XU470 | 136-0813-00 |  | SKT,PL-IN ELEK:CHIP CARRIER,68 CONTACTS | 53387 | 2-0068-05400-00 |
| A12XU480 | 136-0751-0 |  | SOCKET DIP:PCB,;STR, $2 \times 12,24$ POS | 09922 | DILB24P108 |
| A12XU490 | 136-0751-00 |  | SOCKET DIP:PCB,;STR, $2 \times 12,24$ POS | 09922 | DILB24P108 |
| A12XU640 | 136-0757-00 |  | SOCKET,DIP:PCB,;FEMALE,STR, $2 \times 20,40$ POS | 09922 | DILB40P-108 |
| A12XU670 | 136-0755-00 |  | SOCKET,DIP:PCB,;FEMALE,STR, $2 \times 14,28$ POS | 09922 | DILB28P-108 |
| A12XU680 | 136-0755-00 |  | SOCKET,DIP:PCB,;FEMALE,STR, $2 \times 14,28$ POS | 09922 | DILB28P-108 |
| A12XU682 | 136-0755-00 |  | SOCKET,DIP:PCB,;FEMALE,STR,2 $\times 14,28$ POS | 09922 | DiLB28P-108 |
| A12XU690 | 136-0755-00 |  | SOCKET,DIP:PCB,;FEMALE,STR,2 $\times 14,28$ POS | 09922 | DILB28P-108 |
| A12XU692 | 136-0755-00 |  | SOCKET,DIP:PCB,;FEMALE,STR, $2 \times 14,28$ POS | 09922 | DILB28P-108 |


| Component Number | Tektronix <br> Part No. | Serial No. Effective Dscont | Name \& Description | Mr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A13 | 671-0125-00 |  | CIRCUIT BD ASSY:SIDE | 80009 | 671012500 |
| A13C700 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C701 | 283-0177-05 |  | CAP,FXD,CER DI:1UF, $+80-20 \%, 25 \mathrm{~V}$ | 04222 | SR303E105ZAAAP1 |
| A13C702 | 290-0967-0 |  | CAP,FXD,ELCTLT:22UF,+50-10\%,25V | OHiN5 | CE02W1E220C |
| A13C731 | 290-0967-00 |  | CAP,FXD,ELCTLT:22UF,+50-10\%,25V | OHIN5 | CE02W1E220C |
| A13C750 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C751 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C752 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C753 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C754 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C755 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C756 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C757 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C758 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C800 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C801 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C811 | 281-0814-00 |  | CAP,FXD,CERAMIC:MLC;100 PF,10\%,100V | TK1743 | CGB101KEN |
| A13C812 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C813 | 281-0814-0 |  | CAP,FXD,CERAMIC:MLC; 100 PF,10\%,100V | TK1743 | CGB101KEN |
| A13C831 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C832 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C833 | 281-0757-00 |  | CAP,FXD,CER DI:10PF,20\%,100V | 04222 | SA102A100MAA |
| A13C841 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C842 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C843 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C850 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C851 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C852 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C853 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C854 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C861 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C864 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C871 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C872 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C873 | 281-0909-0 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A13C881 | 290-0183-0 |  | CAP,FXD,TANT:DRY; 1 UF,10\%,35V | 12954 | AT513A105K035N |
| A13C882 | 281-0865-0 |  | CAP,FXD,CER DI: $1000 \mathrm{PF}, 5 \%, 100 \mathrm{~V}$ | 04222 | SA201A102JAA |
| A13C883 | 281-0814-m |  | CAP,FXD,CERAMIC:MLC; 100 PF, $10 \%, 100 \mathrm{~V}$ | TK1743 | CGB101KEN |
| A13C884 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC; $0.022 \mathrm{UF}, 20 \%, 50 \mathrm{~V}$ | 04222 | SA105C223MAA |
| A13C885 | 281-0775-00 |  | CAP,FXD,CER DI:0.1UF,20\%,50V | 04222 | SA105E104MAA |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mr. Code | Mir. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A13CR761 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A13CR771 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A13CR772 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A13CR773 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A13J150 | 131-0608-00 |  | TERMINAL.PIN:PRESSFIT/PCB.:MALE.STR (QUANTITY OF 26) | 22526 | 48283-018 |
| A13J155 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 3) | 22526 | 48283-018 |
| A13J156 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A135731 | 174-0677- |  | CABLE ASSY,RF:50 OHM COAX,6.0L | O.J7N9 | ORDER BY DESC |
| A13J843 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 3) | 22526 | 48283-018 |
| A13J844 | 131-0608-00 |  | TERMINAL.PIN:PRESSFIT/PCB.:MALE.STR (QUANTITY OF 3) | 22526 | 48283-018 |
| A13L731 | 108-0538-00 |  | COIL,RF:FIXED,2.7UH | 0.JR03 | 108-0538-00 |
| A13P156 | 131-0993-00 |  | CONN,BOX:SHUNT/SHORTING;FEMALE,STR | 22526 | 65474-006 |
| A13P843 | 131-0993-00 |  | CONN,BOX:SHUNT/SHORTING;;FEMALE,STR | 22526 | 65474-006 |
| A13P844 | 131-0993-00 |  | CONN,BOX:SHUNT/SHORTING;;FEMALE,STR | 22526 | 65474-006 |
| A13Q761 | 151-0188-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A13Q771 | 151-0188-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A13Q772 | 151-0188-0 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A13Q773 | 151-0188-0 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A13Q781 | 151-0190-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA | 04713 | 2N3904 |
| A13Q782 | 151-1121-00 |  | TRANSISTOR,PWR:MOS,N-CH;60V,0.5A,3.0 OHM | 17856 | VN0606L |
| A130783 | 151-0188-0 |  | TRANSISTOR,SIG:BIPOLAR,PNP;40V,200MA | 04713 | 2N3906 |
| A13Q831 | 151-0190- |  | TRANSISTOR,SIG:BIPOLAR,NPN;40V,200MA | 04713 | 2N3904 |
| A13R711 | 313-1103-0 |  | RES,FXD,FLLM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A13R731 | 321-1682-07 |  | RES,FXD,FILM:5.7K OHM,0.1\%,0.125W,TC = T9 | 19701 | 5033RE5K700B |
| A13R732 | 321-0641-07 |  | RES,FXD,FILM:1.8K OHM, $0.1,0.125 \mathrm{~W}, \mathrm{TC}=$ T9 | 19701 | 5033RE1 K800B |
| A13R741 | 315-0162-00 |  | RES,FXD,FILM:1,6K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A13R750 | 313-1101-00 |  | RES,FXD,FILM: 100 OHM,5\%,0.2W | 91637 | CCF50-2-100ROJ |
| A13R751 | 313-1101-00 |  | RES,FXD,FILM:100 OHM,5\%,0.2W | 91637 | CCF50-2-100ROJ |
| A13R752 | 313-1101-00 |  | RES,FXD,FILM:100 OHM,5\%,0.2W | 91637 | CCF50-2-100ROJ |
| A13R753 | 313-1101-00 |  | RES,FXD,FILM:100 OHM,5\%,0.2W | 91637 | CCF50-2-100ROJ |
| A13R755 | 313-1201-00 |  | RES,FXD,FILM:200 OHM,5\%,0.2W | 91637 | CCF50-2-200ROJ |
| A13R761 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A13R762 | 321-1489-00 |  | RES,FXD,FILM:1.23M,1\%,0.125W,TC=TO | 19701 | 5033RD1M230F |
| A13R771 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A13R772 | 322-3293-00 |  | RES,FXD:METAL FILM; 11 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50G11001F |
| A13R773 | 313-1103-00 |  | RES,FXD.FILM:10K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10001J |
| A13R774 | 3-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 1637 | CCF50-2-10001J |


| Component Number | Toktronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A13R775 | 321-0393-00 |  | RES,FXD,FILM:121K OHM,1\%,0.125W,TC=T0 | TK1727 | 2322-151-121K |
| A13R780 | 321-1720-00 |  | RES,FXD,FILM:3.24M OHM, $1 \%, 0.125 W, T C=$ T0 | 64537 | PME55 3.24 MEGO |
| A13R781 | 321-0556-00 |  | RES,FXD,FILM:6.04M OHM, 1.0\%,0.125W,TC=TO | 64537 | PME60 6.04MOHM |
| A13R782 | 321-0556-00 |  | RES,FXD,FILM: 6.04 M OHM, $1.0 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 64537 | PME60 6.04MOHM |
| A13R783 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A13R784 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A13R800 | 307-0648-00 |  | RES NTWK, FXD, Fl: 8,100 OHM, $2 \%, 0.125 \mathrm{~W}$ | 11236 | 761-3-R100 |
| A13R801 | 313-1103-00 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10001J |
| A13R802 | 313-1103-00 |  | RES,FXD,FILM: 10 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10001J |
| A13R803 | 313-1103-00 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10001J |
| A13R804 | 313-1512-0 |  | RES,FXD,FILM:5.1K OHM,5\%,0.2W | 91637 | CCF50-2-51000 |
| A13R805 | 313-1512-0 |  | RES,FXD,FILM:5.1K OHM,5\%,0.2W | 91637 | CCF50-2-51000 J |
| A13R806 | 313-1103-0 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A13R807 | 313-1512-00 |  | RES,FXD,FILM:5.1K OHM,5\%,0.2W | 91637 | CCF50-2-51000J |
| A13R808 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A13R809 | 313-1101-00 |  | RES,FXD,FILM: 100 OHM,5\%,0.2W | 91637 | CCF50-2-100ROJ |
| A13R810 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A13R811 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A13R812 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A13R813 | 313-1103-00 |  | RES,FXD,FILM: 10 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10001J |
| A13R814 | 313-1103-00 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10001J |
| A13R815 | 313-1101-00 |  | RES,FXD,FILM: $100 \mathrm{OHM}, 5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-100ROJ |
| A13R832 | 321-0808-03 |  | RES, FXD,FILM: 300 OHM, $0.25 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T2 | TK1727 | MPR24-2322-141 |
| A13R833 | 321-0282-00 |  | RES,FXD,FILM: 8.45 K OHM, $4 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED8K450F |
| A13R834 | 322-3293-00 |  | RES,FXD:METAL FILM; 11 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50G11001F |
| A13R835 | 313-1101-0 |  | RES,FXD,FILM: 100 OHM,5\%,0.2W | 91637 | CCF50-2-100ROJ |
| A13R841 | 313-1621-00 |  | RES,FXD,FILM: 620 OHM,5\%,0.2W | 91637 | CCF50-2-620ROJ |
| A13R842 | 315-0162-0 |  | RES,FXD,FILM:1.6K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A13R843 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A13R844 | 313-1103-00 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10001 J |
| A13R845 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A13R846 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001 J |
| A13R861 | 313-1103-00 |  | RES,FXD,FILM: 10 K OHM,5\%,0.2W | 91637 | CCF50-2-10001 |
| A13R862 | 313-1103-00 |  | RES,FXD,FILM: 10 K OHM,5\%,0.2W | 91637 | CCF50-2-10001 |
| A13R863 | 313-1102-00 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000 J |
| A13R871 | 313-1102-00 |  | RES,FXD,FILM:1K OHM,5\%,0.2W | 91637 | CCF50-2-10000 J |
| A13R881 | 313-1103-00 |  | RES,FXD,FILM:10K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10001J |
| A13R882 | 321-0271-00 |  | RES,FXD,FILM:6.49K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED6K490F |
| A13R883 | 321-0245-00 |  | RES.FXD.FILM:3.48K OHM, 1\%,0.125W.TC= $=$ To | 19701 | 5033ED3K48F |
| A13R884 | 313-1102-0 |  | RES,FXD,FILM:1K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000J |


| Component Number | Tektronlx <br> Part No. | Sorial No. Effective Dscont | Name a Description | Mir. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A13R885 | 313-1101-00 |  | RES,FXD,FILM: 100 OHM,5\%,0.2W | 91637 | CCF50-2-100ROJ |
| A13R886 | 313-1183-00 |  | RES,FXD,FILM:18K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-18001J |
| A13R887 | 313-1183-00 |  | RES,FXD,FILM: 18 K OHM,5\%,0.2W | 91637 | CCF50-2-18001J |
| A13R888 | 315-0162-00 |  | RES,FXD,FILM:1.6K OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A13R889 | 313-1102-00 |  | RES,FXD,FILM: 1 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10000 |
| A13TP701 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB;;MALE,STR | 22526 | 48283-018 |
| A13TP702 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A13TP811 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A13TP812 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB;;MALE,STR | 22526 | 48283-018 |
| A13TP813 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB; MALE,STR | 22526 | 48283-018 |
| A13TP814 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A13TP815 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB;;MALE,STR | 22526 | 48283-018 |
| A13TP821 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A13TP822 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A13TP823 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A13TP824 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB;MALE,STR | 22526 | 48283-018 |
| A13TP825 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB,MALE,STR | 22526 | 48283-018 |
| A13TP826 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A13TP827 | 131-0608-00 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A13TP871 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB,MALE,STR | 22526 | 48283-018 |
| A13TP881 | 131-0608-0 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
| A13U700 | 160-2405-0 |  | MICROCKT,DGTL:8 BIT MICROCOMPUTER | 04713 | MC6805R3P |
| A13U731 | 156-1149-01 |  | IC,LINEAR:BIFET,OP-AMP | 27014 | LF351N |
| A13U732 | 156-1722-00 |  | IC,DIGITAL:FTTL,GATE;HEXINV | 04713 | MC74F04N |
| A13U741 | 156-1221-0 |  | IC,DIGITAL:LSTTL,FLIP FLOP;HEX D | 01295 | SN74LS378N |
| A13U742 | 156-1065-01 |  | IC,DIGITAL:LSTTL,LATCH | 01295 | SN74LS373N |
| A13U750 | 156-1277-00 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 27014 | DM81LS95AN |
| A13U751 | 156-0956-00 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 01295 | SN74LS244N3 |
| A13U752 | 156-1277-00 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 27014 | DM81LS95AN |
| A13U753 | 156-1277-00 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 27014 | DM81LS95AN |
| A13U761 | 156-1277-00 |  | IC,DIGITAL:LSTTL,BUFFER/DRIVER | 27014 | DM81LS95AN |
| A13U762 | 156-1221-00 |  | IC,DIGITAL:LSTTL,FLIP FLOP;HEXD | 01295 | SN74LS378N |
| A13U781 | 156-0469-00 |  | IC.DIGITAL:LSTTL,DEMUX/DECODER | 01295 | SN74LS138 |
| A13U831 | 156-0048-0 |  | IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY | 04713 | MC3346P |
| A13U841 | 156-1611-0 |  | IC,DIGITAL:FTTL.FLIP FLOP;DUAL D-TYPE | 04713 | MC74F74N |
| A13U842 | 156-1611-0 |  | IC,DIGITAL:FTTL,FLIP FLOP;DUAL D-TYPE | 04713 | MC74F74N |
| A13U843 | 156-2251-0 |  | IC,DIGITAL:FTTL,COUNTER:SYNCH 4-BIT BINARY | 04713 | MC74F161AN |
| A13U844 | 156-2251-0 |  | IC,DIGITAL:FTTL,COUNTER;SYNCH 4-BIT BINARY | 04713 | MC74F161AN |
| A13U851 | 156-1743-00 |  | IC,DIGITAL:FTTL,GATE;QUAD 2-INPUT | 04713 | MC74F02N |
| A13U852 | 156-1172-00 |  | IC,DIGITAL:LSTTL,COUNTER;DUAL 4-BIT BINARY | 01295 | SN74LS393N |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mitr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A13U853 | 156-1172-00 |  | IC,DIGITAL:LSTTL,COUNTER;DUAL 4-BIT BINARY | 01295 | SN74LS393N |
| A13U861 | 156-0388-00 |  | IC,DIGITAL:LSTTL,FLIP FLOP;DUAL D | 01295 | SN74LS74AN |
| A13U862 | 156-0383-00 |  | IC,DIGITAL:LSTTL,GATES; QUAD 2-INPUT | 01295 | SN74LSO2N |
| A13U871 | 156-1126-01 |  | IC,LINEAR:BIPOLAR,COMPARATOR | 01295 | LM311P |
| A13U872 | 156-0388-00 |  | IC,DIGITAL:LSTTL,FLIP FLOP;DUAL D | 01295 | SN74LS74AN |
| A13U881 | 156-1126-01 |  | IC,LINEAR:BIPOLAR,COMPARATOR | 01295 | LM311P |
| A13VR841 | 152-0195-00 |  | DIODE,ZENER:,5.1V,5\%,0.4W | 04713 | SZ11755RL |
| A13W101 | 175-9023-00 |  | CA ASSY,SP,ELEC:50,28 AWG,8.675 L | 53387 | ORDER BY DESC |
| A13W110 | 175-9027-00 |  | CA ASSY,SP,ELEC:40,28 AWG,1.4 L | 53387 | ORDER BY DESC |
| A13W122 | 175-9024-00 |  | CA ASSY,SP:RIBBON,;IDC,40,28 AWG,3.5 L | 53387 | ORDER BY DESC |
| A13W800 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A14 | 614-0752-00 |  | FRONT PNL ASSY:STANDARD (STANDARD) | 80009 | 614075200 |
| A14 | 614-0753-0 |  | FRONT PNL ASSY:TV OPT 05 (OPTION 05) | 80009 | 614075300 |
| A14C902 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A14C903 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A14C904 | 290-0943-02 |  | CAP,FXD,ELCTLT:47UF,20\%,25V | 1W344 | SME25VB47RM5X11 |
| A14C905 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A14C906 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A14CR901 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR902 | 152-0141-02 |  | DIODE,SIG; ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR903 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR904 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST:40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR906 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR907 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR908 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST:40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR909 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST:40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR911 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST:40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR912 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST; $40 \mathrm{~V}, 150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A14CR913 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR914 | 152-0141-02 |  | DIODE,SIG: ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR916 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR917 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR918 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR919 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR921 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST; $40 \mathrm{~V}, 150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A14CR922 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR923 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST:40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR924 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR927 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST; $40 \mathrm{~V}, 150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A14CR928 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, $150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A14CR929 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR932 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST:40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR933 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR934 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST; $40 \mathrm{~V}, 150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A14CR937 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, $150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A14CR938 | 152-0141-02 |  | DIODE,SIG; ULTRA FAST;40V, $150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A14CR939 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST; $40 \mathrm{~V}, 150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A14CR942 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR943 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR944 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |


| Component Number | Tektronlx <br> Part No. | Serial No. Effective Dscont | Name \& Description | Mir. Code | Mir. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A14CR947 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR948 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, 150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR949 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, 150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR952 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR953 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, $150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A14CR954 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, $150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A14CR957 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR958 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR959 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR962 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR963 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR964 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR967 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR968 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, 150MA,4NS,2PF | 27014 | FDH9427 |
| A14CR969 | 152-0141-02 |  | DIODE,SIG:,ULTRA FAST;40V, $150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A14DS901 | 150-1109-0 |  | DIODE,OPTO:,LED;GRN,565NM,1.5MCD AT 20MA | 50434 | HLMP-0503 OPT S |
| A14DS902 | 150-1109-0 |  | DIODE,OPTO:,LED;GRN,565NM,1.5MCD AT 20MA | 50434 | HLMP-0503 OPT S |
| A14DS903 | 150-1109-00 |  | DIODE,OPTO:,LED;GRN,565NM, 1.5MCD AT 20MA | 50434 | HLMP-0503 OPT S |
| A14DS904 | 150-1109-00 |  | DIODE,OPTO:,LED;GRN,565NM, 1.5MCD AT 20MA | 50434 | HLMP-0503 OPT S |
| A14DS906 | 150-1109-0 |  | DIODE,OPTO:LED;GRN,565NM,1.5MCD AT 20MA | 50434 | HLMP-0503 OPT S |
| A14R901 | 311-2181-0 |  | RES,VAR,NONWW:LINEAR,5K OHM,30\%,0.25W | 32997 | 91Z2D-Z45-EA002 |
| A14R902 | 311-2181-0 |  | RES,VAR,NONWW:LINEAR,5K OHM,30\%,0.25W | 32997 | 91Z2D-Z45-EA002 |
| A14R903 | 313-1103-00 |  | RES,FXD,FILM: 10 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10001J |
| A14R904 | 313-1103-00 |  | RES,FXD,FILM:10K OHM, 5\%,0.2W | 91637 | CCF50-2-10001J |
| A14R813 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A14R914 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A14R916 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A14R917 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A14R918 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A14R919 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A14R922 | 313-1101-00 |  | RES,FXD,FILM: 100 OHM,5\%,0.2W | 91637 | CCF50-2-100ROJ |
| A14R923 | 313-1101-00 |  | RES,FXD.FILM: $100 \mathrm{OHM}, 5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-100ROJ |
| A14R924 | 313-1101-00 |  | RES,FXD,FILM:100 OHM,5\%,0.2W | 91637 | CCF50-2-100R0J |
| A14R927 | 313-1101-00 |  | RES,FXD,FILM:100 OHM, 5\%,0.2W | 91637 | CCF50-2-100ROJ |
| A14R928 | 313-1101-00 |  | RES,FXD,FILM: 100 OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-100ROJ |
| A14R930 | 313-1101-00 |  | RES,FXD,FILM: $100 \mathrm{OHM}, 5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-100ROJ |
| A14R933 | 313-1101-00 |  | RES,FXD,FILM: $100 \mathrm{OHM}, 5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-100ROJ |
| A14R934 | 313-1103-00 |  | RES,FXD,FLLM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A14R935 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A14R936 | 313-1103-00 |  | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |


| Component Number | Toktronix Part No. | Serial No. Effective Dscont | Name \& Description | Mr. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A14R937 | 313-1101-00 |  | RES,FXD,FILM: 100 OHM,5\%,0.2W | 91637 | CCF50-2-100ROJ |
| A14S901 | 263-0099-00 |  | SW-VAR RES ASSY:2430 | 80009 | 263009900 |
| A14S902 | 263-0099-00 |  | SW-VAR RES ASSY:2430 | 80009 | 263009900 |
| A14S903 | 263-0099-0 |  | SW-VAR RES ASSY:2430 | 80009 | 263009900 |
| A14S904 | 263-0099-00 |  | SW-VAR RES ASSY:2430 | 80009 | 263009900 |
| A14S906 | 260-2088-00 |  | SWITCH,PUSH:1 BTN,1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S907 | 260-2088-00 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A145908 | 260-2088-00 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A145909 | 260-2088-0 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S911 | 260-2088-¢ |  | SWITCH,PUSH:1 BTN,1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S912 | 260-2088-00 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S913 | 260-2088-00 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S914 | 260-2088-00 |  | SWITCH,PUSH:1 BTN,1 POLE,TRIGGER | 71590 | 2LLI99NB021068 |
| A14S916 | 260-2088-00 |  | SWITCH,PUSH:1 BTN,1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S917 | 260-2088-00 |  | SWITCH,PUSH: 1 BTN,1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A145918 | 260-2088-00 |  | SWITCH,PUSH:1 BTN,1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S919 | 260-2088-00 |  | SWITCH,PUSH:1 BTN,1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S921 | 260-2088-00 |  | SWITCH,PUSH:1 BTN,1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S922 | 260-2088-00 |  | SWITCH,PUSH:1 BTN,1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S923 | 260-2088-00 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A145924 | 260-2088-00 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S927 | 260-2088-00 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A145928 | 260-2088-00 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A145929 | 260-2088-0 |  | SWITCH,PUSH: 1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A145932 | 260-2088-0 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A145933 | 260-2088-0 |  | SWITCH,PUSH:1 BTN,1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A145934 | 260-2224-0 |  | SWITCH,ROTARY:GRAY CODE,OUTPUT | 76854 | 2090 MMP-REL-16 |
| A145942 | 260-2088-0 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S943 | 260-2088- 0 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A145944 | 260-2224-0 |  | SWITCH,ROTARY:GRAY CODE,OUTPUT | 76854 | 2090 MMP-REL-16 |
| A145952 | 260-2088-0 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A145953 | 260-2088-00 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S954 | 260-2224-00 |  | SWITCH,ROTARY:GRAY CODE,OUTPUT | 76854 | 2090 MMP-REL-16 |
| A14S962 | 260-2088-00 |  | SWITCH,PUSH:1 BTN,1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S963 | 260-2088-00 |  | SWITCH,PUSH:1 BTN,1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S964 | 260-2088-00 |  | SWITCH,PUSH:1 BTN,1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S967 | 260-2088-00 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S968 | 260-2088-00 |  | SWITCH,PUSH:1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14S969 | 260-2088-00 |  | SWITCH,PUSH: 1 BTN, 1 POLE,TRIGGER | 71590 | 2LL199NB021068 |
| A14U902 | 156-0513-03 |  | IC,MISC:CMOS,ANALOG MUX;8 CHANNEL | 04713 | MC14051BCP |


| Component <br> Number | Tektronix <br> Part No. | Serial No. <br> Effective <br> Dscont | Name \& Description | Mr. <br> Code | Mfr. Part No. |
| :--- | :--- | :--- | :--- | :--- | :--- |
| A14U903 | $156-0469-00$ |  | IC,DIGITAL:LSTTL,DEMUX/DECODER | 01295 | SN74LS138 |
| A14U904 | $156-0625-00$ |  | IC,DIGITAL:CMOS,SHIFT REGISTER;8-BIT PISO | 27014 | MM74C165N |
| A14W151 | $175-9022-00$ |  | CA ASSY,SP,ELEC:26,28 AWG,18.95L | 53387 | ORDER BY DESC |


| Component <br> Number | Tektronix <br> Part No. | Serial No. <br> Effective <br> Dscont | Name \& Description | Mfr. <br> Code | Mfr. Part No. |
| :--- | :--- | :--- | :--- | :--- | :--- |
| A15 | $175-9270-01$ |  | FLEX CKT ASSY:GPIB,POLYMIDE | $\mathbf{8 0 0 0 9}$ | 175927001 |
|  |  |  | LT EMITTING DIO:YELLOW | 50434 | QLMP-1487 |
| A15DS920 | $150-1161-00$ | LT EMITTING DIO:YELLOW | 50434 | QLMP-1487 |  |
| A15DS921 | $150-1161-00$ | LT EMITTING DIO:YELLOW | 50434 | QLMP-1487 |  |
| A15DS922 | $150-1161-00$ |  |  |  |  |


| Component Number | Toktronix Part No. | Serial Effective | No. Dscont | Name \& Description | Mtr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A16 | 670-9902-01 | B010100 | B012402 | CIRCUIT BD ASSY:LV PWR SPLY | 80009 | 670990201 |
| A16 | 670-9902-04 | B012403 | B012656 | CIRCUIT BD ASSY:LV POWER SUPPLY | 80009 | 670990204 |
| A16 | 670-9902-05 | B012657 | B013269 | CIRCUIT BD ASSY:LV POWER SUPPLY | 80009 | 670990205 |
| A16 | 670-9902-06 | B013270 | B013320 | CIRCUIT BD ASSY:LV POWER SUPPLY | 80009 | 670990206 |
| A16 | 670-9902-07 | B013321 |  | CIRCUIT BD ASSY:LV POWER SUPPLY (STANDARD ONLY) | 80009 | 670990207 |
| A16 | 670-9902-01 | B010100 | B010107 | CIRCUIT BD ASSY:LV PWR SPLY | 80009 | 670990201 |
| A16 | 670-9902-04 | B010108 | B010110 | CIRCUIT BD ASSY:LV POWER SUPPLY | 80009 | 670990204 |
| A16 | 670-9902-05 | B010111 | B010118 | CIRCUIT BD ASSY:LV POWER SUPPLY | 80009 | 670990205 |
| A16 | 670-9902-06 | B010118 | B010118 | CIRCUIT BD ASSY:LV POWER SUPPLY | 80009 | 670990206 |
| A16 | 670-9902-07 | B010119 |  | CIRCUIT BD ASSY:LV POWER SUPPLY (2440M ONLY) | 80009 | 670990207 |
| A16C105 | 290-1022-00 |  |  | CAP,FXD,ELCTLT:680UF,+50-10\%,200V | 00853 | DCM681T200AL2PC |
| A16C128 | 290-0183-00 |  |  | CAP,FXD,TANT:DRY; $1 \mathrm{~F}, 10 \%, 35 \mathrm{~V}$ | 12954 | AT513A105K035N |
| A16C137 | 281-0775-00 |  |  | CAP,FXD,CER DI:0.1UF,20\%,50V | 04222 | SA105E104MAA |
| A16C138 | 290-0183-00 |  |  | CAP,FXD,TANT:DRY; 1 UF,10\%,35V | 12954 | AT513A105K035N |
| A16C144 | 281-0812-00 |  |  | CAP,FXD,CERAMIC:MLC; $1000 \mathrm{PF}, 10 \%, 100 \mathrm{~V}$ | 04222 | SA101C102KAA |
| A16C145 | 281-0775-00 |  |  | CAP,FXD,CER DI: 0.1 UF,20\%,50V | 04222 | SA105E104MAA |
| A16C175 | 281-0775-0 |  |  | CAP,FXD,CER DI:0.1UF,20\%,50V | 04222 | SA105E104MAA |
| A16C184 | 290-0183-0 |  |  | CAP,FXD,TANT:DRY; 1 UF, $10 \%, 35 \mathrm{~V}$ | 12954 | AT513A105K035N |
| A16C185 | 281-0812-00 |  |  | CAP,FXD,CERAMIC:MLC;1000PF,10\%,100V | 04222 | SA101C102KAA |
| A16C195 | 281-0812-00 |  |  | CAP,FXD,CERAMIC:MLC; $1000 \mathrm{PF}, 10 \%, 100 \mathrm{~V}$ | 04222 | SA101C102KAA |
| A16C197 | 281-0812-00 |  |  | CAP,FXD,CERAMIC:MLC;1000PF,10\%,100V | 04222 | SA101C102KAA |
| A16C219 | 285-1192-0 |  |  | CAP,FXD,PPR DI:0.0022 UF,20\%,250VAC | TK0515 | PME271Y422 |
| A16C223 | 283-0078-0 |  |  | CAP,FXD,CER DI:0.001UF,20\%,500V | 59660 | 0801547 X5FO 1 |
| A16C225 | 285-1192-0 |  |  | CAP,FXD,PPR Di:0.0022 UF,20\%,250VAC | TK0515 | PME271Y422 |
| A16C227 | 281-0812-0 | B010100 | B013320 | CAP,FXD,CERAMIC:MLC; $1000 \mathrm{PF}, 10 \%, 100 \mathrm{~V}$ | 04222 | SA101C102KAA |
| A16C227 | 285-1344-0 | B013321 |  | CAP,FXD,PLASTIC:1000PF,100V,5\% (STANDARD ONLY) | TK1913 | FKP2 1000 PF 5 |
| A16C227 | 281-0812-00 | B010100 | B010118 | CAP,FXD,CERAMIC:MLC; $1000 \mathrm{PF}, 10 \%, 100 \mathrm{~V}$ | 04222 | SA101C102KAA |
| A16C227 | 285-1344-00 | B010119 |  | CAP,FXD,PLASTIC:1000PF,100V,5\% (2440M ONLY) | TK1913 | FKP2 1000 PF 5 |
| A16C238 | 281-0775-00 |  |  | CAP,FXD,CER DI:0.1UF,20\%,50V | 04222 | SA105E104MAA |
| A16C244 | 290-0798-00 |  |  | CAP,FXD,ELCTLT:180UF, $+100-10 \%, 40 \mathrm{~V}$ | 24165 | 672D187H040DM5C |
| A16C262 | 290-0945-00 |  |  | CAP,FXD,ELCTLT:840UF $10+100 \%, 12 \mathrm{~V}$ | 00853 | 301 EN841 U012B2 |
| A16C305 | 290-1022-00 |  |  | CAP,FXD,ELCTLT:680UF, $+50-10 \%, 200 \mathrm{~V}$ | 00853 | DCM681T200AL2PC |
| A16C328 | 285-1384-00 |  |  | CAP,FXD,PLASTIC:0.27UF,10\%,440V | 84411 | TEK265 27104 |
| A16C329 | 283-0665-00 | B012403 |  | CAP,FXD,MICA DI:190PF,1\%,100V (STANDARD ONLY) | TK0891 | RDM15FD191F03 |
| A16C329 | 283-0665-00 | 8010100 | B010107 | CAP,FXD,MICA DI:190PF, $1 \%, 100 \mathrm{~V}$ (2440M ONLY) | TK0891 | RDM15FD191F03 |
| A16C368 | 281-0775-00 |  |  | CAP,FXD,CER DI:0.1UF,20\%,50V | 04222 | SA105E104MAA |
| A16C384 | 281-0812-00 |  |  | CAP,FXD,CERAMIC:MLC;1000PF,10\%,100V | 04222 | SA101C102KAA |


| Component Number | Toktronix <br> Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A16C405 | 285-1383-00 |  | CAP,FXD,PLASTIC:0.1UF,10\%,100V | 84411 | TEK291. 11010 |
| A16C455 | 290-0877-00 |  | CAP,FXD,ELCTLT:1200UF,+100-10\%,6.3V | 24165 | 672D128H6R3DS2A |
| A16C460 | 290-0800-0 |  | CAP,FXD,ELCTLT:250UF, $+100-10 \%, 20 \mathrm{~V}$ | 1 W344 | RXC25B251W12X24 |
| A16C461 | 290-0942-00 |  | CAP,FXD,ELCTLT: 100 UF, $+100-10 \%, 25 \mathrm{~V}$ | OH1N5 | CEUFM1E101 |
| A16C483 | 281-0775-0 |  | CAP,FXD,CER DI:0.1UF,20\%,50V | 04222 | SA105E104MAA |
| A16C485 | 281-0812-0 |  | CAP,FXD,CERAMIC:MLC;1000PF,10\%,100V | 04222 | SA101C102KAA |
| A16C487 | 290-0942-0 |  | CAP,FXD,ELCTLT:100UF,+100-10\%,25V | OH1N5 | CEUFM1E101 |
| A16C494 | 290-0942-0 |  | CAP,FXD,ELCTLT: $100 \mathrm{UF},+100-10 \%, 25 \mathrm{~V}$ | OH1N5 | CEUFM1E101 |
| A16C525 | 285-1187-00 |  | CAP,FXD,MTLZD:0.47 UF,10\%,100 V | 05292 | PMT 3R . 47 K 100 |
| A16C528 | 281-0773-00 |  | CAP.FXD,CERAMIC:MLC;0.01UF,10\%,100V | TK1743 | CGB103KEX |
| A16C550 | 290-0942-00 |  | CAP,FXD,ELCTLT: $100 \mathrm{UF},+100-10 \%, 25 \mathrm{~V}$ | OH1N5 | CEUFM1E101 |
| A16C553 | 290-0945-00 |  | CAP,FXD,ELCTLT:840UF $10+100 \%, 12 \mathrm{~V}$ | 00853 | 301 EN841U012B2 |
| A16C575 | 281-0773-00 |  | CAP,FXD,CERAMIC:MLC;0.01UF,10\%,100V | TK1743 | CGB103KEX |
| A16C584 | 281-0812-00 |  | CAP,FXD,CERAMIC:MLC; $1000 \mathrm{PF}, 10 \%, 100 \mathrm{~V}$ | 04222 | SA101C102KAA |
| A16C585 | 290-0942-00 |  | CAP,FXD,ELCTLT:100UF, $+100-10 \%, 25 \mathrm{~V}$ | OHIN5 | CEUFM1E101 |
| A16C594 | 290-0942-00 |  | CAP,FXD,ELCTLT:100UF, $+100-10 \%, 25 \mathrm{~V}$ | OH1N5 | CEUFM1E101 |
| A16C595 | 290-0942-00 |  | CAP,FXD,ELCTLT: 100 UF, $+100-10 \%, 25 \mathrm{~V}$ | OH1N5 | CEUFM1E101 |
| A16C625 | 285-1245-00 |  | CAP,FXD,PLASTIC:0.01UF,10\%,400V | TK1913 | MKP 100.01/400 |
| A16C650 | 290-0942-00 |  | CAP,FXD,ELCTLT:100UF, +100-10\%,25V | OH1N5 | CEUFM1E101 |
| A16C664 | 290-1045-00 |  | CAP,FXD,ELCTLT:4.7UF,10\%,35V | 24165 | 173D475X9035W |
| A16C675 | 281-0812-0 |  | CAP,FXD,CERAMIC:MLC; 1000 PF,10\%,100V | 04222 | SA101C102KAA |
| A16C683 | 281-0812-0 |  | CAP,FXD,CERAMIC:MLC;1000PF,10\%,100V | 04222 | SA101C102KAA |
| A16C695 | 290-0942-00 |  | CAP,FXD,ELCTLT: $100 \mathrm{UF},+100-10 \%, 25 \mathrm{~V}$ | OH1N5 | CEUFM1E101 |
| A16C706 | 285-1222-0 |  | CAP,FXD,PLASTIC:0.068UF,20\%,250V | TK0515 | PME 271 M 568 |
| A16C728 | 281-0775-00 |  | CAP,FXD,CER DI:0.1 1 F,20\%,50V | 04222 | SA105E104MAA |
| A16C750 | 290-0798-0 |  | CAP,FXD,ELCTLT: $180 \mathrm{UF},+100-10 \%, 40 \mathrm{~V}$ | 24165 | 672D187H040DM5C |
| A16C756 | 290-0798-00 |  | CAP,FXD,ELCTLT: $180 \mathrm{UF},+100-10 \%, 40 \mathrm{~V}$ | 24165 | 672D187H040DM5C |
| A16C764 | 290-1045-00 |  | CAP,FXD,ELCTLT:4.7UF,10\%,35V | 24165 | 173D475X9035W |
| A16C816 | 285-1222-00 |  | CAP,FXD,PLASTIC:0.068UF,20\%,250V | TK0515 | PME 271 M 568 |
| A16C823 | 281-0812-00 |  | CAP,FXD,CERAMIC:MLC; $1000 \mathrm{PF}, 10 \%, 100 \mathrm{~V}$ | 04222 | SA101C102KAA |
| A16C829 | 290-0183-0 |  | CAP,FXD,TANT:DRY; 1 UF,10\%,35V | 12954 | AT513At05K035N |
| A16C835 | 281-0773-00 |  | CAP,FXD,CERAMIC:MLC;0.01UF,10\%,100V | TK1743 | CGB103KEX |
| A16C856 | 290-0800-00 |  | CAP,FXD,ELCTLT:250UF,+100-10\%,20V | 1W344 | RXC25B251W12X24 |
| A16C873 | 281-0775-00 |  | CAP,FXD,CER DI:0.1UF,20\%,50V | 04222 | SA105E104MAA |
| A16C890 | 281-0775-00 |  | CAP,FXD,CER DI:0.1UF,20\%,50V | 04222 | SA105E104MAA |
| A16C900 | 290-0183-00 |  | CAP,FXD,TANT:DRY; 1 UF,10\%,35V | 12954 | AT513A105K035N |
| A16C901 | 281-0775-0 |  | CAP,FXD,CER DI:0.1UF,20\%,50V | 04222 | SA105E104MAA |
| A16C929 | 281-0775-0 |  | CAP,FXD,CER DI:0.1UF,20\%,50V | 04222 | SA105E104MAA |
| A16C944 | 281-0773-0 |  | CAP,FXD,CERAMIC:MLC;0.01UF,10\%,100V | TK1743 | CGB103KEX |
| A16C947 | 290-0942- |  | CAP,FXD,ELCTLT: $100 \mathrm{UF},+100-10 \%, 25 \mathrm{~V}$ | OH1N5 | CEUFM1E101 |


| Component Number | Tektronix Part No. | Effective | No. Dscont | Name \& Description | Mfr. Code | Mtr, Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A16C956 | 290-0800-00 |  |  | CAP,FXD,ELCTLT:250UF,+100-10\%,20V | 1W344 | RXC25B251W12X24 |
| A16CR239 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V, $150 \mathrm{MA}, 4 \mathrm{NS}$,2PF | 27014 | FDH9427 |
| A16CR245 | 152-0333-00 |  |  | DIODE,SIG:,ULTRA FAST;80V,4NS,1VF AT 200MA | 27014 | FDH-6012 |
| A16CR265 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V, 150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR266 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR354 | 152-0794-00 |  |  | SEMICOND DVC,DI:RECT,SI,10A,30V,TO-220 | 81483 | 95-4269 |
| A16CR426 | 152-0808-00 |  |  | DIODE,RECT:,ULTRA FAST;400V,1.5A,50NS | 25403 | BYD73G |
| A16CR450 | 152-0398-00 | B010100 | B011312 | DIODE,RECT:,FAST RCVRY;200V,1A,200NS | 14936 | 1N4935GP |
| A16CR465 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR466 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST:40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR483 | 152-0066-0 |  |  | DIODE,RECT:; $400 \mathrm{~V}, 1 \mathrm{~A}, \mathrm{IFSM}=30 \mathrm{~A}, 1.2 \mathrm{VF}, 2 \mathrm{US}$ | 05828 | GP10G-020 |
| A16CR484 | 152-0066-- |  |  | DIODE,RECT:; $400 \mathrm{~V}, 1 \mathrm{~A}, \mathrm{IFSM}=30 \mathrm{~A}, 1.2 \mathrm{VF}, 2 \mathrm{US}$ | 05828 | GP10G-020 |
| A16CR485 | 152-0066-- |  |  | DIODE,RECT:; $400 \mathrm{~V}, 1 \mathrm{~A}, 1 \mathrm{FSM}=30 \mathrm{~A}, 1.2 \mathrm{FF}, 2 \mathrm{US}$ | 05828 | GP10G-020 |
| A16CR510 | 152-0750- | B010100 | B012402 | DIODE,RECT:FAST RCVRY;BRIDGE,600V,3A (STANDARD ONLY) | TK2319 | RKBPC606 |
| A16CR510 | 152-0750-0 | $B 010100$ | B010107 | DIODE,RECT;,FAST RCVRY;BRIDGE,600V,3A (2440M ONLY) | TK2319 | RKBPC606 |
| A16CR511 | 152-0661-0 | B012403 |  | DIODE,RECT;,FAST RCVRY;600V,3A,200NS (STANDARD ONLY) | 12954 | DR850701B |
| A16CR511 | 152-0661-00 | B010108 |  | DIODE,RECT:,FAST RCVRY;600V,3A,200NS (2440M ONLY) | 12954 | DR850701B |
| A16CR512 | 152-0661-00 | B012403 |  | DIODE,RECT:,FAST RCVRY;600V,3A,200NS (STANDARD ONLY) | 12954 | DR850701B |
| A16CR512 | 152-0661-0 | B010108 |  | DIODE,RECT:,FAST RCVRY;600V,3A,200NS (2440M ONLY) | 12954 | DR850701B |
| A16CR513 | 152-0661-00 | B012403 |  | DIODE,RECT:,FAST RCVRY;600V,3A,200NS (STANDARD ONLY) | 12954 | DR850701B |
| A16CR513 | 152-0661-00 | B010108 |  | DIODE,RECT:,FAST RCVRY;600V,3A,200NS (2440M ONLY) | 12954 | DR850701B |
| A16CR514 | 152-0661-00 | B012403 |  | DIODE,RECT:,FAST RCVRY;600V,3A,200NS (STANDARD ONLY <br> (2440M ONLY) | 12954 | DR850701B |
| A16CR550 | 152-0398-00 | B010100 | B011312 | DIODE,RECT,FAST RCVRY;200V,1A,200NS | 14936 | 1N4935GP |
| A16CR550 | 152-0836-0 | 8011313 |  | DIODE,RECT:SCHTKY; $40 \mathrm{~V}, 1 \mathrm{~A}, 1 \mathrm{IFSM}=25 \mathrm{~A}$ | 04713 | 1N5819 |
| A16CR551 | 152-0867-00 |  |  | SEMICOND DVC,DI:DUAL RECT,SCHOTTKY,SI,30V | 6 L 334 | SR1603A |
| A16CR575 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR576 | 152-0066-00 |  |  | DIODE,RECT: ;400V, $1 \mathrm{~A}, 1 \mathrm{FSM}=30 \mathrm{~A}, 1.2 \mathrm{VF}, 2 \mathrm{US}$ | 05828 | GP10G-020 |
| A16CR583 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR586 | 152-0066-00 |  |  | DIODE,RECT:;400V,1A,IFSM=30A,1.2VF,2US | 05828 | GP10G-020 |
| A16CR588 | 152-0066-00 |  |  | DIODE,RECT:;;400V, 1 A,IFSM $=30 \mathrm{~A}, 1.2 \mathrm{FF}, 2 \mathrm{~S}$ | 05828 | GP10G-020 |
| A16CR630 | 152-0400-00 |  |  | DIODE,RECT:,FAST RCVRY; $400 \mathrm{~V}, 1 \mathrm{~A}, 200 \mathrm{NS}$ | 14552 | MB2501 |
| A16CR631 | 152-0400-00 |  |  | DIODE,RECT:,FAST RCVRY;400V, 1A,200NS | 14552 | MB2501 |
| A16CR650 | 152-0398-00 | B010100 | B013269 | DIODE,RECT;,FAST RCVRY;200V,1A,200NS | 14936 | 1N4935GP |


| Component Number | Tektronlx Part No. | Effective | No. Dscont | Name \& Description | Mfr. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A16CR650 | 152-0601-01 | B013270 |  | SEMICOND DVC,DI:RECTIFIER,SI,150V,1A,35NS (STANDARD ONLY) | 04713 | MUR115RL |
| A16CR650 | 152-0398-00 | 8010100 | B010118 | DIODE,RECT:,FAST RCVRY;200V, 1A,200NS | 14936 | 1N4935GP |
| A16CR650 | 152-0601-01 | B010119 |  | SEMICOND DVC,DI:RECTIFIER,SI,150V,1A,35NS (2440M ONLY) | 04713 | MUR115RL |
| A16CR651 | 152-0398-00 | B010100 | 8013269 | DIODE,RECT:,FAST RCVRY:200V,1A,200NS | 14936 | 1N4935GP |
| A16CR651 | 152-0601-01 | B013270 |  | SEMICOND DVC,D: RECTIFIER,SI,150V,1A,35NS (STANDARD ONLY) | 04713 | MUR115RL |
| A16CR651 | 152-0398-00 | B010100 | B010118 | DIODE,RECT:,FAST RCVRY;200V,1A,200NS | 14936 | 1N4935GP |
| A16CR651 | 152-0601-01 | B010119 |  | SEMICOND DVC,DI:RECTIFIER,SI,150V,1A,35NS (2440M ONLY) | 04713 | MUR115RL |
| A16CR683 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR684 | 152-0066-0 |  |  | DIODE,RECT:; $400 \mathrm{~V}, 1 \mathrm{~A}, \mathrm{IFSM}=30 \mathrm{~A}, 1.2 \mathrm{VF}, 2 \mathrm{~S}$ | 05828 | GP10G-020 |
| A16CR685 | 152-0066-0 |  |  | DIODE,RECT:;400V, 1 A,IFSM $=30 \mathrm{~A}, 1.2 \mathrm{VF}, 2 \mathrm{US}$ | 05828 | GP10G-020 |
| A16CR723 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST:40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR724 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR730 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST:40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR750 | 152-0398-00 | 8010100 | B013269 | DIODE,RECT:,FAST RCVRY;200V, 1A,200NS | 14936 | 1N4935GP |
| A16CR750 | 152-0601-01 | B013270 |  | SEMICOND DVC,DI:RECTIFIER,SI, 150V,1A,35NS (STANDARD ONLY) | 04713 | MUR115RL |
| A16CR750 | 152-0398-00 | B010100 | B010118 | DIODE,RECT:,FAST RCVRY;200V,1A,200NS | 14936 | 1N4935GP |
| A16CR750 | 152-0601-01 | 8010119 |  | SEMICOND DVC,DI:RECTIFIER,SI, 150V,1A,35NS (2440M ONLY) | 04713 | MUR115RL |
| A16CR751 | 152-0398-00 | B010100 | B013269 | DIODE,RECT:,FAST RCVRY;200V,1A,200NS | 14936 | 1N4935GP |
| A16CR751 | 152-0601-01 | B013270 |  | SEMICOND DVC,DI:RECTIFIER,SI,150V,1A,35NS (STANDARD ONLY) | 04713 | MUR115RL |
| A16CR751 | 152-0398-00 | B010100 | B010118 | DIODE,RECT:,FAST RCVRY;200V,1A,200NS | 14936 | 1N4935GP |
| A16CR751 | 152-0601-01 | B010119 |  | SEMICOND DVC,DI:RECTIFIER,SI, 150V,1A,35NS (2440M ONLY) | 04713 | MUR115RL |
| A16CR765 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR766 | 152-0141-02 |  |  | DIODE,SIG:ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR796 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR823 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR824 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR845 | 152-0867-00 |  |  | SEMICOND DVC,DI:DUAL RECT,SCHOTTKY,SI,30V | 6L334 | SR1603A |
| A16CR846 | 152-0794-00 |  |  | SEMICOND DVC,DI:RECT,SI,10A,30V,TO-220 | 81483 | 95-4269 |
| A16CR865 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR866 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V, 150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR896 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V, 150MA,4NS,2PF | 27014 | FDH9427 |
| A16CR930 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V, $150 \mathrm{MA}, 4 \mathrm{NS}, 2 \mathrm{PF}$ | 27014 | FDH9427 |
| A16CR4450 | 152-0836-00 | B011313 |  | DIODE,RECT:SCHTKY; 40V, 1 A,IFSM $=25 \mathrm{~A}$ | 04713 | 1N5819 |
| A16CT750 |  |  |  | (2440M ONLY) |  |  |
| A16E609 | 119-0181-00 |  |  | ARSR,ELEC SURGE:230,GAS FILLED, + /-15\% | 25088 | B1-A230T |


| Component Number | Toktronix Part No. | Seria Effective | INo. Dscont | Name \& Description | Mfr. Code | Mtr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A16E616 | 119-0181-00 |  |  | ARSR,ELEC SURGE:230,GAS FILLED, +/-15\% | 25088 | B1-A230T |
| A16F269 | 159-0236-00 |  |  | FUSE,WIRE LEAD:10A, 125V,FAST,T\&R | 61857 | SP5-10A(T\&R) |
| A16F961 | 159-0235-0 |  |  | FUSE,WIRE LEAD:0.75A,125V,FAST | 71400 | TR/MCR 3/4 |
| A16J102 | 131-3147-00 |  |  | CONN,HDR:PCB,;MALE,STR, $2 \times 25,0.1$ CTR | 53387 | 2550-6002UB |
| A16,166 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 9) | 22526 | 48283-018 |
| A16L256 | 108-1234-00 |  |  | COIL,RF:FIXED,5UH | 0.1 RO 0 | 108-1234-00 |
| A16L556 | 108-1234-0 |  |  | COIL,RF:FIXED,5UH | 0.JRO3 | 108-1234-00 |
| A16L557 | 108-1233-0 |  |  | COIL,RF:FIXED,27UH,10\% | O.JRO3 | ORDER BY DESC |
| A16L656 | 108-1233-0 |  |  | COIL,RF:FIXED,27UH,10\% | 0.1203 | ORDER BY DESC |
| A16L709 | 108-1209-0 |  |  | COIL,RF:FXD TOROIDAL,8OUH MIN,3A DC | O.JR03 | ORDER BYDESC |
| A16L715 | 108-1209-0 |  |  | COIL,RF:FXD TOROIDAL,80UH MIN,3A DC | O.JR03 | ORDER BYDESC |
| A16L756 | 108-1233-00 |  |  | COIL,RF:FIXED,27UH,10\% | OJR03 | ORDER BY DESC |
| A16L945 | 108-1233-0 |  |  | COIL,RF:FIXED,27UH,10\% | O.JR03 | ORDER BY DESC |
| A16L950 | 108-1233-0 |  |  | COIL,RF:FIXED,27UH,10\% | O.JR03 | ORDER BY DESC |
| A16P30 | 131-2427-0 |  |  | TERM, QIK DISC.:PCB; MALE TAB, $0.250 \times 0.032$ | 00779 | 62409-1 |
| A16P60 | 131-2427-0 |  |  | TERM, QIK DISC.:PCB,;MALE TAB, $0.250 \times 0.032$ | 00779 | 62409-1 |
| A16P70 | 131-2427-00 |  |  | TERM,QIK DISC.:PCB,;MALE TAB, $0.250 \times 0.032$ | 00779 | 62409-1 |
| A16P80 | 131-2427-00 |  |  | TERM, QIK DISC.:PCB,;MALE TAB,0.250 X 0.032 | 00779 | 62409-1 |
| A16Q148 | 151-0432-0 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;80V,500MA | 04713 | MPS8099 |
| A16Q240 | 151-0301-00 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP:60V,600MA | 04713 | 2N2907A |
| A16Q279 | 151-0798-00 |  |  | TRANSISTOR,PWR:BIPOLAR,PNP;50V, 12A | S4091 | 2SB826 Q OR R |
| A16Q295 | 151-0341-0 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN:45V,50MA,40MHZ | 04713 | MPS6520 |
| A16Q365 | 151-0134-0 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP;60V,600MA | 04713 | 2N2905A |
| A16Q421 | 151-1214-0 | B010100 | B010903 | TRANSISTOR,PWR:MOS,N-CH:500V,4.5A.1.5 OHM | 04713 | STP4063 |
| A16Q421 | 151-1214-01 | B010904 | B012656 | TRANSISTOR,PWR:MOS,N-CH:500V,4.5A,1.5 OHM | 04713 | IRF830 |
| A16Q421 | 151-1195-00 | B012657 | B012656 | TRANSISTOR,PWR:MOS, $\mathrm{N}-\mathrm{CH} ; 500 \mathrm{~V}, 8.0 \mathrm{~A}$ | 04713 | MTP8N50E |
| A16Q421 | 151-1195-01 | B012657 |  | TRANSISTOR,PWR:MOS,N-CH;500V,8.0A (STANDARD) | 34371 | IRF840R |
| A16Q421 | 151-1214-01 | B010100 | B010t10 | TRANSISTOR,PWR:MOS,N-CH:500V,4.5A,1.5 OHM | 04713 | IRF830 |
| A16Q421 | 151-1195-00 | B010111 |  | TRANSISTOR,PWR:MOS,N-CH;500V,8.OA (2440M) | 04713 | MTP8N50E |
| A16Q423 | 151-1214-00 | B010100 | B010903 | TRANSISTOR,PWR:MOS,N-CH;500V,4.5A,1.5 OHM | 04713 | STP4063 |
| A16Q423 | 151-1214-01 | B010904 | B012656 | TRANSISTOR,PWR:MOS,N-CH;500V,4.5A,1.5 OHM | 04713 | IRF830 |
| A16Q423 | 151-1195-00 | B012657 |  | TRANSISTOR,PWR:MOS,N-CH;500V,8.OA (STANDARD) | 04713 | MTP8N50E |
| A16Q423 | 151-1214-01 | B010100 | B010110 | TRANSISTOR,PWR:MOS,N-CH;500V,4.5A,1.5 OHM | 04713 | IRF830 |
| A16Q423 | 151-1195-00 | B010111 |  | TRANSISTOR,PWR:MOS,N-CH;500V,8.0A (2440M) | 04713 | MTP8N50E |
| A16Q465 | 151-0103-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN; $40 \mathrm{~V}, 800 \mathrm{MA}$ | 04713 | 2N2219A |
| A16Q479 | 151-0797-0 |  |  | TRANSISTOR,PWR:BIPOLAR,NPN;50V,12A | S4091 | 2SD1062 Q OR R |


| Component Number | Tektronix Part No. | Serlal No. <br> Effective Dscont | Name \& Description | Mfr. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A16Q521 | 151-1141-00 |  | TRANSISTOR,PWR:MOS,N-CH;400V,5.5A,1.0 OHM | 04713 | MTP5N40E |
| A16Q665 | 151-0134-00 |  | TRANSISTOR,SIG:BIPOLAR,PNP;60V,600MA | 04713 | 2N2905A |
| A16Q721 | 151-1141-0 |  | TRANSISTOR,PWR:MOS,N-CH;400V,5.5A,1.0 OHM | 04713 | MTP5N40E |
| A16Q779 | 151-0798-0 |  | TRANSISTOR,PWR:BIPOLAR,PNP;50V,12A | S4091 | 2SB826 Q OR R |
| A16Q836 | 151-0103-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;40V,800MA | 04713 | 2N2219A |
| A16Q870 | 151-0103-00 |  | TRANSISTOR,SIG:BIPOLAR,NPN;40V,800MA | 04713 | 2N2219A |
| A16Q879 | 151-0797-00 |  | TRANSISTOR,PWR:BIPOLAR,NPN:50V,12A | S4091 | 2SD1062 Q OR R |
| A16R117 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED10K00F |
| A16R128 | 321-0289-00 |  | RES,FXD,FILM: 10.0 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED10K00F |
| A16R129 | 321-0430-0 |  | RES,FXD,FILM:294K OHM,1\%,0.125W,TC=T0 | 19701 | 5043ED294KOF |
| A16R136 | 321-0932-0 |  | RES,FXD,FILM:2.5K OHM, 1\%,0.125W,TC=T0 | 19701 | 5033RD2K500F |
| A16R143 | 321-0356-0 |  | RES,FXD,FILM:49.9K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033ED49K90F |
| A16R144 | 321-0289-0 |  | RES,FXD,FILM:10.0K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED10K00F |
| A16R146 | 321-0420-0 |  | RES,FXD,FILM:232K OHM,1\%,0.125W,TC=T0 | 19701 | 5043ED232KOF |
| A16R164 | 321-0289-07 |  | RES,FXD,FILM:10.0K OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T9 | 19701 | 5033RE10K00B |
| A16R165 | 321-0816-07 |  | RES,FXD,FILM:5K OHM,0.1\%,0.125W,TC=T9 | TK1727 | MPR24-2322-141 |
| A16R166 | 321-0242-00 |  | RES,FXD,FILM:3.24K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | 2322-151-3K24 |
| A16R167 | 315-0474-0 |  | RES,FXD,FILM:470K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R185 | 315-0753-00 |  | RES,FXD,FILM:75K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R186 | 321-0335-00 |  | RES,FXD,FILM:30.1K OHM, 1\%,0.125W,TC = T0 | 19701 | 5033RD30K12FB29 |
| A16R187 | 321-0337-00 |  | RES,FXD,FILM:31.6K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED31K60F |
| A16R195 | 315-0474-00 |  | RES,FXD,FILM:470K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R217 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED10KOOF |
| A16R223 | 305-0104-00 |  | RES,FXD,CMPSN:100K OHM,5\%,2W | 11502 | GF-3 OR GS-3 10 |
| A16R226 | 321-0289-0 |  | RES,FXD,FILM: 10.0 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED10K00F |
| A16R227 | 321-0193-00 |  | RES,FXD,FILM:1K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-1 |
| A16R228 | 321-0335-0 |  | RES,FXD,FILM:30.1K OHM, 1\%,0.125W,TC=T0 | 19701 | 5033RD30K12FB29 |
| A16R238 | 315-0470-m |  | RES,FXD,FILM:47 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R240 | 321-0932-0 |  | RES,FXD,FILM:2.5K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033RD2K500F |
| A16R244 | 315-0753-00 |  | RES,FXD,FILM:75K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R265 | 321-0932-00 |  | RES,FXD,FILM:2.5K OHM, 1\%,0.125W,TC=T0 | 19701 | 5033RD2K500F |
| A16R274 | 321-0420-00 |  | RES,FXD,FILM:232K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ To | 19701 | 5043ED232KOF |
| A16R275 | 321-0286-00 |  | RES,FXD,FILM:9.31K OHM,1\%,0.125W,TC=T0 | 19701 | 5043ED9K310F |
| A16R276 | 321-0143-00 |  | RES,FXD,FILM:301 OHM,1\%,0.125W,TC=TO | TK1727 | MR25 2322-151-3 |
| A16R281 | 315-0100-00 |  | RES,FXD,FILM: 10 OHM, $5 \%, 0.25 \mathrm{~W}$, | TK1727 | SFR25 2322-182 |
| A16R285 | 321-0356-00 |  | RES,FXD,FILM:49.9K OHM, 1\%,0.125W,TC=T0 | 19701 | 5033ED49K90F |
| A16R293 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED10K00F |
| A16R295 | 321-0932-00 |  | RES,FXD,FILM:2.5K OHM, 1\%,0.125W,TC = T0 | 19701 | 5033RD2K500F |
| A16R296 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED10K00F |
| A16R323 | 321-0932-00 |  | RES,FXD,FILM:2.5K OHM, 1\%,0.125W,TC=T0 | 19701 | 5033RD2K500F |


| Component Number | Tektronix Part No. | Serial Effective | No. Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A16R324 | 321-0114-00 | B010100 | B012656 | RES,FXD,FILM:150 OHM, 1\%,0.125 W,TC=T0 | TK1727 | MR25 2322-151-1 |
| A16R324 | 315-0750-00 | B012657 |  | RES,FXD,FILM: 75 OHM,5\%,0.25W (STANDARD ONLY) | TK1727 | SFR25 2322-181 |
| A16R324 | 321-0114-00 | B010100 | B010110 | RES,FXD,FILM:150 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ To | TK1727 | MR25 2322-151-1 |
| A16R324 | 315-0750-0 | B010111 |  | RES,FXD,FILM:75 OHM,5\%,0.25W (2440M ONLY) | TK1727 | SFR25 2322-181 |
| A16R325 | 323-0436-00 |  |  | RES,FXD,FILM:340K OHM, $1 \%, 0.5 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CMF65116G34002F |
| A16R368 | 321-0210-00 |  |  | RES,FXD,FILM:1.50K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033ED1K50F |
| A16R369 | 321-0184-00 |  |  | RES,FXD,FILM:806 OHM, 1\%,0.125W,TC=T0 | TK1727 | MR25 2322-151-8 |
| A16R374 | 315-0100-00 |  |  | RES,FXD,FILM: 10 OHM,5\%,0.25W, | TK1727 | SFR25 2322-182 |
| A16R376 | 308-0839-0 |  |  | RES,FXD:0.1 OHM,5\%,1.0W | 75042 | SP-20-R1000J |
| A16R388 | 315-0101-0 |  |  | RES,FXD,FILM: 100 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R394 | 321-0337-0 |  |  | RES,FXD,FILM:31.6K OHM,1\%,0.125W,TC= T0 | 19701 | 5043ED31K60F |
| A16R396 | 321-0337-00 |  |  | RES,FXD,FILM:31.6K OHM,1\%,0.125W,TC= T0 | 19701 | 5043ED31K60F |
| A16R397 | 321-0932-00 |  |  | RES,FXD,FILM:2.5K OHM, 1\%,0.125W,TC=T0 | 19701 | 5033RD2K500F |
| A16R401 | 315-0474-00 |  |  | RES,FXD,FILM:470K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R405 | 308-0703-0 |  |  | RES,FXD,WW:1.8 OHM,5\%,2W | 75042 | SPH 1.8 OHM 5 P |
| A16R410 | 315-0474-00 |  |  | RES,FXD,FILM:470K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R428 | 305-0221-00 |  |  | RES,FXD,CMPSN:220 OHM,5\%,2W | 50139 | HB2215 |
| A16R429 | 321-0289-00 |  |  | RES,FXD,FILM:10.0K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED10K00F |
| A16R434 | 321-0242-00 |  |  | RES,FXD,FILM:3.24K OHM, 1\%,0.125W,TC=T0 | TK1727 | 2322-151-3K24 |
| A16R435 | 321-0242-00 |  |  | RES,FXD,FILM:3.24K OHM, 1\%,0.125W,TC=TO | TK1727 | 2322-151-3K24 |
| A16R436 | 321-0385-00 |  |  | RES,FXD,FILM:100K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED100K0F |
| A16R465 | 321-0184-00 |  |  | RES,FXD,FLM:806 OHM, 1\%,0.125W,TC=T0 | TK1727 | MR25 2322-151-8 |
| A16R466 | 321-0242-0 |  |  | RES,FXD,FILM:3.24K OHM, 1\%,0.125W,TC=T0 | TK1727 | 2322-151-3K24 |
| A16R473 | 308-0839-00 |  |  | RES,FXD:0.1 OHM,5\%,1.OW | 75042 | SP-20-R1000J |
| A16R474 | 321-0143-00 |  |  | RES,FXD,FILM:301 OHM,1\%,0.125W,TC= $=$ T0 | TK1727 | MR25 2322-151-3 |
| A16R475 | 321-0335-00 | B010100 | B011312 | RES,FXD,FILM:30.1K OHM,1\%,0.125W,TC=T0 | 19701 | 5033RD30K12FB29 |
| A16R475 | 321-0322-00 | B011313 |  | RES,FXD,FILM:22.1K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033ED22K10F |
| A16R476 | 321-0193-00 |  |  | RES,FXD,FILM:1K OHM,1\%,0.125W,TC=T0 | TK1727 | MR25 2322-151-1 |
| A16R477 | 321-0385-00 |  |  | RES,FXD,FILM:100K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED100K0F |
| A16R478 | 315-0100-00 |  |  | RES,FXD,FILM:10 OHM,5\%,0.25W | TK1727 | SFR25 2322-182 |
| A16R483 | 321-0106-00 |  |  | RES,FXD,FILM:124 OHM 1\%,0.125W,TC=TO | TK1727 | MR25 2322-151-1 |
| A16R505 | 321-0385-00 |  |  | RES,FXD,FILM: 100 K OHM,1\%,0.125W,TC= 0 | 19701 | 5043ED100KOF |
| A16R516 | 321-0356-00 |  |  | RES,FXD,FILM:49.9K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033ED49K90F |
| A16R518 | 321-0356-00 |  |  | RES,FXD,FILM:49.9K OHM, 1\%,0.125W,TC = T0 | 19701 | 5033ED49K90F |
| A16R565 | 321-0816-00 |  |  | RES,FXD,FILM:5K OHM,1\%,0.125W,TC=T0 | 19701 | 5033RD5K000F |
| A16R566 | 315-0100-00 |  |  | RES,FXD,FILM:10 OHM,5\%,0.25W | TK1727 | SFR25 2322-182 |
| A16R575 | 321-0289-00 |  |  | RES,FXD,FILM:10.0K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED10K00F |
| A16R576 | 321-0816-00 |  |  | RES,FXD,FILM:5K OHM,1\%,0.125W,TC=T0 | 19701 | 5033RD5K000F |
| A16R578 | 315-0100-00 |  |  | RES,FXD,FILM:10 OHM,5\%,0.25W | TK1727 | SFR25 2322-182 |
| A16R624 | 321-0114-0 | B010100 | B012656 | RES,FXD,FILM: 150 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-1 |


| Component Number | Tektronix Part No. | Seria Eftective | No. Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A16R624 | 315-0750-0 | B012657 |  | RES,FXD,FILM: 75 OHM,5\%,0.25W (STANDARD ONLY) | TK1727 | SFR25 2322-181 |
| A16R624 | 321-0114-00 | B010100 | B010110 | RES,FXD,FILM: 150 OHM, $1 \%, 0.125$ W,TC $=$ TO | TK1727 | MR25 2322-151-1 |
| A16R624 | 315-0750-0 | B010111 |  | RES,FXD,FILM:75 OHM,5\%,0.25W (2440M ONLY) | TK1727 | SFR25 2322-181 |
| A16R627 | 306-0154-00 |  |  | RES,FXD,CMPSN:150K OHM,10\%,2W | 24546 | FP42 OR FP2 150 |
| A16R640 | 315-0101-00 |  |  | RES,FXD,FILM:100 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R675 | 321-0289-00 |  |  | RES,FXD,FILM:10.0K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED10K00F |
| A16R676 | 321-0816-0 |  |  | RES,FXD,FILM:5K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033RD5K000F |
| A16R684 | 321-0193-00 |  |  | RES,FXD,FILM:1K OHM, 1\%,0.125W,TC= 0 | TK1727 | MR25 2322-151-1 |
| A16R686 | 321-0306-00 |  |  | RES,FXD,FILM:15.0K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED15K00F |
| A16R688 | 321-0280-00 |  |  | RES,FXD,FILM:8,06K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033ED8K060F |
| A16R713 | 301-0680-0 |  |  | RES,FXD,FILM:68 OHM,5\%,0.5W | 19701 | $5053 \mathrm{CX68R00J}$ |
| A16R723 | 315-0470-0 |  |  | RES,FXD,FILM:47 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R724 | 315-0470-0 |  |  | RES,FXD,FILM:47 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R727 | 308-0843-0 |  |  | RES,FXD:WIREWOUND;0.2 OHM,5\%,1W | 91637 | CW-1-R20JT |
| A16R728 | 321-0184-- |  |  | RES,FXD,FILM:806 OHM, 1\%,0.125W,TC= 0 | TK1727 | MR25 2322-151-8 |
| A16R758 | 308-0223-00 |  |  | RES,FXD,WW:35 OHM,5\%,3W | 91637 | CW2B-35ROOJ |
| A16R760 | 308-0555-00 |  |  | RES,FXD,WW:5 OHM,5\%,3W | 91637 | CW2B-5R000J |
| A16R765 | 315-0100-00 |  |  | RES,FXD,FILM:10 OHM,5\%,0.25W | TK1727 | SFR25 2322-182 |
| A16R769 | 321-0932-00 |  |  | RES,FXD,FILM:2.5K OHM, 1\%,0.125W,TC=T0 | 19701 | 5033RD2K500F |
| A16R773 | 308-0839-00 |  |  | RES,FXD:0.1 OHM, $5 \%, 1.0 \mathrm{~W}$ | 75042 | SP-20-R1000J |
| A16R774 | 315-0101-00 |  |  | RES,FXD,FILM:100 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R775 | 321-0264-00 | 3010100 | B010670 | RES,FXD,FILM:5.49K OHM,1\%,0.125W,TC=T0 | 19701 | 5043ED5K490F |
| A16R775 | 321-0816-00 | B010671 |  | RES,FXD,FILM:5K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ = 0 (STANDARD ONLY) | 19701 | 5033RD5K000F |
| A16R775 | 321-0816-00 |  |  | RES,FXD,FILM:5K OHM,1\%,0.125W,TC=TO (2440M ONLY) | 19701 | 5033RD5K000F |
| A16R776 | 321-0143-00 |  |  | RES,FXD,FILM:301 OHM, 1\%,0.125W,TC=T0 | TK1727 | MR25 2322-151-3 |
| A16R777 | 321-0385-00 |  |  | RES,FXD,FILM:100K OHM, 1\%,0.125W,TC=TO | 19701 | 5043ED100K0F |
| A16R794 | 321-0306-00 |  |  | RES,FXD,FILM:15.0K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED15K00F |
| A16R795 | 321-0280-m |  |  | RES,FXD,FILM:8.06K OHM, 1\%,0.125W,TC=T0 | 19701 | 5033ED8K060F |
| A16R796 | 321-0816-0 |  |  | RES,FXD,FILM:5K OHM,1\%,0.125W,TC=T0 | 19701 | 5033RD5K000F |
| A16R797 | 321-0816-0 |  |  | RES,FXD,FILM:5K OHM,1\%,0.125W,TC=T0 | 19701 | 5033RD5K000F |
| A16R808 | 315-0470-00 |  |  | RES,FXD,FILM:47 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R809 | 301-0300-0 |  |  | RES,FXD,FILM: 30 OHM,5\%,0.5W | 19701 | 5053CX30R00J |
| A16R815 | 315-0470-00 |  |  | RES,FXD,FILM:47 OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R822 | 321-0289-00 |  |  | RES,FXD,FILM:10.0K OHM,1\%,0.125W,TC=T0 | 19701 | 5043ED10K00F |
| A16R823 | 321-0816-00 |  |  | RES,FXD,FILM:5K OHM,1\%,0.125W,TC=T0 | 19701 | 5033RD5K000F |
| A16R824 | 321-0193-00 |  |  | RES,FXD,FILM:1K OHM,1\%,0.125W,TC=T0 | TK1727 | MR25 2322-151-1 |
| A16R834 | 321-0143-00 |  |  | RES,FXD,FILM:301 OHM, 1\%,0.125W,TC=T0 | TK1727 | MR25 2322-151-3 |


| Component Number | Tektronix Part No. | Serial No. <br> Effective Dscont | Name \& Description | Mr. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A16R835 | 321-0289-00 |  | RES,FXD,FILM:10.0 $\mathrm{OHM}, 1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED10K00F |
| A16R836 | 321-0184-00 |  | RES,FXD,FILM: 806 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | TK1727 | MR25 2322-151-8 |
| A16R845 | 321-0242-0 |  | RES,FXD,FILM:3.24K OHM, 1\%,0.125W,TC=TO | TK1727 | 2322-151-3K24 |
| A16R847 | 321-0210-00 |  | RES,FXD,FILM:1.50K OHM, 1\%,0.125W,TC=T0 | 19701 | 5033EDIK50F |
| A16R864 | 321-0932-00 |  | RES,FXD,FILM:2.5K ОНM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5033RD2K500F |
| A16R865 | 321-0816-m |  | RES,FXD,FILM:5K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033RD5K000F |
| A16R866 | 321-0816-0 |  | RES,FXD,FILM:5K OHM,1\%,0.125W,TC=T0 | 19701 | 5033RD5K000F |
| A16R872 | 321-0289-00 |  | RES,FXD,FILM: 10.0 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED10K00F |
| A16R873 | 308-0839-00 |  | RES,FXD:0.1 OHM,5\%,1.0W | 75042 | SP-20-R1000J |
| A16R874 | 315-0101-00 |  | RES,FXD,FILM:100 OHM, 5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R875 | 321-0269-00 |  | RES,FXD,FILM:6.19K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED6K190F |
| A16R876 | 321-0143-00 |  | RES,FXD,FILM:301 OHM, 1\%,0.125W,TC = T0 | TK1727 | MR25 2322-151-3 |
| A16R877 | 321-0356-00 |  | RES,FXD,FILM:49.9K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033ED49K90F |
| A16R900 | 321-0356-00 |  | RES,FXD,FILM:49.9K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033ED49K90F |
| A16R905 | 321-0184-00 |  | RES,FXD,FILM: 806 OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | TK1727 | MR25 2322-151-8 |
| A16R906 | 321-0193-00 |  | RES,FXD,FILM:1K OHM, 1\%,0.125W,TC=T0 | TK1727 | MR25 2322-151-1 |
| A16R925 | 321-0816-0 |  | RES,FXD,FILM:5K OHM,1\%,0.125W,TC=T0 | 19701 | 5033RD5K000F |
| A16R926 | 321-0289-00 |  | RES,FXD,FILM:10.0K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED10K00F |
| A16R931 | 321-0193- |  | RES,FXD,FILM:1K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | TK1727 | MR25 2322-151-1 |
| A16R932 | 315-0474-0 |  | RES,FXD,FILM:470K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A16R938 | 321-0242-00 |  | RES,FXD,FILM:3.24K OHM,1\%,0.125W,TC= To | TK1727 | 2322-151-3K24 |
| A16R939 | 321-0289-0 |  | RES,FXD,FILM:10.0K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED10K00F |
| A16R975 | 321-0932-00 |  | RES,FXD,FILM:2.5K OHM,1\%,0.125W,TC= TO | 19701 | 5033RD2K500F |
| A16RT717 | 307-0157-00 |  | RES,THERMAL: 5 OHM, 10\%,DISC | 15454 | 5DA5ROK-270-SIL |
| A16RT805 | 307-0157-00 |  | RES,THERMAL:5 OHM,10\%,DISC | 15454 | 5DA5R0K-270-SIL |
| A16S1020 | 260-0724-00 |  | SWITCH,THRMSTC:NC,OPEN 83.3,CL 66.7,10A240V | TK2292 | 430-367 |
| A16T117 | 120-1560-00 |  | TRANSFORMER,RF:HIGH FREQUENCY COMM | 02113 | ORDER BY DESC |
| A16T335 | 120-1561-00 |  | TRANSFORMER,RF:POT CORE | 02113 | ORDER BY DESC |
| A16T415 | 120-1401-00 |  | XFMR,TRIGGER:LINE, 1:1 TURNS RATIO | 54937 | DMI 500-2044 |
| A16T620 | 120-1555-00 |  | TRANSFORMER,RF:DRIVER HIGH FREQ,GATE D | 54937 | ORDER BY DESC |
| A16T639 | 120-1550-00 |  | XFMR,PWR,STPDN:HIGH FREQUENCY | TK2425 | ORDER BY DESC |
| A16U155 | 156-0885-00 |  | CPLR,OPTOELECTR:LED,5KV ISOLATION | OMS63 | H11AX861 |
| A16U170 | 156-0853-00 |  | IC,LINEAR:BIPOLAR,OP-AMP;DUAL | 01295 | LM358P |
| A16Ut80 | 156-2186-00 |  | IC,LINEAR:BIPOLAR,VOLTAGE REFERENCE | 27014 | LM368H-10 |
| A16U189 | 156-0853-00 |  | IC,LINEAR:BIPOLAR,OP-AMP;DUAL | 01295 | LM358P |
| A16U233 | 156-2024-0 |  | IC,UNEAR:BIPOLAR,SW - REGULATOR CONT | 34333 | SG3525AN |
| A16U265 | 156-0885-00 |  | CPLR,OPTOELECTR:LED,5KV ISOLATION | OMS63 | H11AX861 |
| A16U270 | 156-0853-00 |  | IC,LINEAR:BIPOLAR,OP-AMP;DUAL | 01295 | LM358P |
| A16U395 | 156-1225-00 |  | IC,LINEAR:BIPOLAR,COMPARATOR;DUAL | 01295 | LM393P |
| A16U470 | 156-0853-00 |  | IC,LINEAR:BIPOLAR,OP-AMP;DUAL. | 01295 | LM358P |


| Component Number | Tektronix Part No. | Serial No. Effective Dscont | Name \& Description | Mfr. Code | Mtr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A16U570 | 156-0853-00 |  | IC,LNEAR:BIPOLAR,OP-AMP:DUAL | 01295 | LM358P |
| A16U579 | 156-1161-00 |  | IC,LINEAR:BIPOLAR,VOLTAGE REGULATOR | 04713 | LM317T |
| A16U679 | 156-1451-00 |  | IC,LINEAR:BIPOLAR,VOLTAGE REGULATOR | 04713 | LM337T |
| A16U770 | 156-0853-00 |  | IC,LINEAR:BIPOLAR,OP-AMP;DUAL. | 01295 | LM358P |
| A16U829 | 156-0366-00 |  | IC,DIGITAL:CMOS,FLIP FLOP;DUAL D-TYPE | 04713 | MC14013BCP |
| A16U834 | 156-1225-00 |  | IC,LINEAR:BIPOLAR,COMPARATOR;DUAL | 01295 | LM393P |
| A16U840 | 156-0411-00 |  | IC,LINEAR:BIPOLAR,COMPARATOR;QUAD | 01295 | LM339 |
| A16U870 | 156-0853-00 |  | IC,LINEAR:BIPOLAR,OP-AMP;DUAL | 01295 | LM358P |
| A16U900 | 156-0854-00 |  | IC,LINEAR:BIPOLAR,OP -AMP;LOW INPUT BIAS | 27014 | LM308AN |
| A16VR144 | 152-0168-00 |  | DIODE,ZENER:,;12V,5\%,0.4W | 04713 | 1N963BRL |
| A16VR380 | 152-0195-00 |  | DIODE,ZENER:,55.1V.5\%,0.4W | 04713 | SZ11755RL |
| A16VR870 | 152-0168-00 |  | DIODE,ZENER:,;12V,5\%,0.4W | 04713 | 1N963BRL |
| A16VR929 | 152-0168-0 |  | DIODE,ZENER:,;12V,5\%,0.4W | 04713 | 1N963BRL |
| A16W270 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A16W280 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD $\times 0.225 \mathrm{~L}$ | 24546 | OMA0207 |
| A16W310 | 196-2827-00 |  | LEAD,ELECTRICAL:18 AWG,2.75 L,3-4 | O.J7N9 | ORDER BY DESC |
| A16W315 | 196-2827-00 |  | LEAD,ELECTRICAL:18 AWG,2.75 L, 3-4 | 0.17 N 9 | ORDER BY DESC |
| A16W360 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A16W368 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES, 0.094 OD X 0.225L | 24546 | OMA0207 |
| A16W460 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A16W462 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A16W467 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A1.6W566 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A16W627 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A16W662 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A16W664 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A16W762 | 131-0566-0 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A16W860 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A16W862 | 131-0566-0 |  | BUS,CONDUCTOR:DUMMY RES.0.094 OD $\times 0.225 \mathrm{~L}$ | 24546 | OMA0207 |
| A16W865 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |
| A16W868 | 131-0566-00 |  | BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225L | 24546 | OMA0207 |


| Component Number | Tektronix Part No. | Seria Effective | INo. Dscont | Name \& Description | Mfr. <br> Code | Mir. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A17 | 670-9748-00 | B010100 | B012402 | CIRCUIT BD ASSY:HV POWER SPLY | 80009 | 670974800 |
| A17 | 670-9748-01 | B012403 | B012656 | CIRCUIT BD ASSY:HV POWER SUPPLY | 80009 | 670974801 |
| A17 | 670-9748-02 | B012657 | B013269 | CIRCUIT BD ASSY:HV POWER SUPPLY | 80009 | 670974802 |
| A17 | 670-9748-03 | B013269 | B013320 | CIRCUIT BD ASSY:HV POWER SUPPLY | 80009 | 670974803 |
| A17 | 670-9748-04 | B013321 |  | CIRCUIT BD ASSY:HV POWER SUPPLY (STANDARD ONLY) | 80009 | 670974804 |
| A17 | 670-9748-00 | B010100 | B010107 | CIRCUIT BD ASSY:HV POWER SPLY | 80009 | 670974800 |
| A17 | 670-9748-01 | B010108 | B010110 | CIRCUIT BD ASSY:HV POWER SUPPLY | 80009 | 670974801 |
| A17 | 670-9748-02 | B010111 | B010118 | CIRCUIT BD ASSY:HV POWEA SUPPLY | 80009 | 670974802 |
| A17 | 670-9748-03 | B010118 | B010118 | CIRCUIT BD ASSY:HV POWER SUPPLY | 80009 | 670974803 |
| A17 | 670-9748-04 | B010119 |  | CIRCUIT BD ASSY:HV POWER SUPPLY (2440M ONLY) | 80009 | 670974804 |
| A17C109 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A17C133 | 281-0772-0 |  |  | CAP,FXD,CERAMIC:MLC;4700PF,10\%,100V | 04222 | SA101C472KAA |
| A17C139 | 283-0167-02 |  |  | CAP,FXD,CER DI:0.1UF,10\%,100V | 04222 | SR591C104KAAAP1 |
| A17C150 | 281-0909-0 | B012403 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V (STANDARD ONLY) | 04222 | SA105C223MAA |
| A17C150 | 281-0909-00 | B010108 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V (2440M ONLY) | 04222 | SA105C223MAA |
| A17C160 | 281-0865-00 |  |  | CAP,FXD,CER DI:1000PF,5\%,100V | 04222 | SA201A102JAA |
| A17C165 | 281-0909-00 | B0t2403 |  | CAP,FXD,CERAMIC:MLC;0,022UF,20\%,50V (STANDARD ONLY) | 04222 | SA105C223MAA |
| A17C165 | 281-0909-00 | B010108 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V (2440M ONLY) | 04222 | SA105C223MAA |
| A17C179 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A17C189 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A17C215 | 281-0865-00 | B012403 |  | CAP,FXD,CER DI:1000PF,5\%,100V (STANDARD ONLY) | 04222 | SA201A102JAA |
| A17C215 | 281-0865-00 | B010108 |  | CAP,FXD,CER DI:1000PF,5\%,100V (2440M ONLY) | 04222 | SA201A102JAA |
| A17C216 | 285-1187-00 | B012403 |  | CAP,FXD,MTLZD:0.47 UF,10\%,100 V (STANDARD ONLY) | 05292 | PMT 3R .47K 100 |
| A17C216 | 285-1187-00 | B010108 |  | CAP,FXD,MTLZD:0.47 UF,10\%,100 V (2440M ONLY) | 05292 | PMT 3R .47K 100 |
| A17C217 | 283-0167-02 | B012403 |  | CAP,FXD,CER DI:0.1UF,10\%,100V (STANDARD ONLY) | 04222 | SR591C104KAAAP1 |
| A17C217 | 283-0167-02 | 8010108 |  | CAP,FXD,CER DI:0.1UF,10\%,100V (2440M ONLY) | 04222 | SR591C104KAAAP1 |
| A17C218 | 290-0766-00 | B010100 | B012402 | CAP,FXD,ALUM:2.2UF, $+50-20 \%, 160 \mathrm{~V}$ | 1W344 | SME250VB2R2M8X1 |
| A17C218 | 290-1144-00 | B012403 |  | CAP,FXD,ALUM:;4.7UF,20\%,100V (STANDARD ONLY) | OHiN5 | CEUSM2A4R7T12 |
| A17C218 | 290-0766-00 | B010100 | B010107 | CAP,FXD,ALUM:2.2UF,+50-20\%,160V | 1W344 | SME250VB2R2M8X1 |
| A17C218 | 290-1144-00 | B010108 |  | CAP,FXD,ALUM:;4.7UF,20\%,100V (2440M ONLY) | OH1N5 | CEUSM2A4R7T12 |
| A17C222 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A17C234 | 281-0762-00 |  |  | CAP,FXD,CER DI:27PF,20\%,100V | 04222 | SA102A270MAA |


| Component Number | Toktronlx Part No. | Effective | No. Dscont | Name \& Description | Mr. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A17C239 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A17C260 | 283-0167-02 |  |  | CAP,FXD,CER DI:0.1UF,10\%,100V | 04222 | SR591C104KAAAP1 |
| A17C269 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A17C288 | 283-0167-02 |  |  | CAP,FXD,CER DI:0.1UF,10\%,100V | 04222 | SR591C104KAAAP1 |
| A17C289 | 283-0187-05 |  |  | CAP,FXD,CER DI:0.047UF,10\%,500V | 04222 | SR307C473KAAAP1 |
| A17C295 | 281-0798-00 |  |  | CAP,FXD,CER DI:51PF, $1 \%, 100 \mathrm{~V}$ | TK1743 | CGB510GEN |
| A17C317 | 290-0939-00 | B010100 | 3012402 | CAP,FXD,ELCTLT:10UF, $+100-10 \%, 100 \mathrm{~V}$ (STANDARD ONLY) | 1W344 | LX100VB10RM10X2 |
| A17C317 | 290-0939-0 | B010100 | B010107 | CAP,FXD,ELCTLT: $10 \mathrm{UF},+100-10 \%, 100 \mathrm{~V}$ (2440M ONLY) | 1W344 | LX100VB10RM10X2 |
| A17C327 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A17C409 | 281-0814-00 |  |  | CAP,FXD,CERAMIC:MLC; 100 PF,10\%,100V | TK1743 | CGB101KEN |
| A17C613 | 290-0973-00 | B010100 | B012402 | CAP,FXD,ELCTLT:100UF,20\%,25VDC | OH1N5 | CEUSM1E101 |
| A17C613 | 290-0973-01 | B012403 |  | CAP,FXD,ALUM:;100UF,20\%,25VDC (STANDARD ONLY) | 1W344 | SME35VB101M8X11 |
| A17C613 | 290-0973-00 | B010100 | B010107 | CAP,FXD,ELCTLT:100UF,20\%,25VDC | OH1N5 | CEUSM1E101 |
| A17C613 | 290-0973-01 | B010108 |  | CAP,FXD,ALUM:;100UF,20\%,25VDC (2440M ONLY) | 1W344 | SME35VB101M8X11 |
| A17C617 | 283-0339-00 |  |  | CAP,FXD,CER DI:0.22UF,10\%,50V | 04222 | SR305C224KAA |
| A17C618 | 283-0187-05 |  |  | CAP,FXD,CER D: $0.047 \mathrm{UF}, 10 \%, 500 \mathrm{~V}$ | 04222 | SR307C473KAAAP1 |
| A17C628 | 281-0865-00 |  |  | CAP,FXD,CER DI:1000PF,5\%,100V | 04222 | SA201A102JAA |
| A17C629 | 283-0187-05 |  |  | CAP,FXD,CER DI:0.047UF,10\%,500V | 04222 | SR307C473KAAAP1 |
| A17C638 | 283-0187-05 |  |  | CAP,FXD,CER DI:0.047UF,10\%,500V | 04222 | SR307C473KAAAP1 |
| A17C639 | 281-0865-00 | B012403 |  | CAP,FXD,CER DI: $1000 \mathrm{PF}, 5 \%, 100 \mathrm{~V}$ | 04222 | SA201A102JAA |
| A17C640 | 281-0766-00 |  |  | CAP,FXD,CER DI:100PF,20\%,200V | 04222 | SA102A101KAA |
| A17C643 | 283-0187-05 | B010100 | B012402 | CAP,FXD,CER D: $0.047 \mathrm{UF}, 10 \%, 500 \mathrm{~V}$ (STANDARD ONLY) | 04222 | SR307C473KAAAP1 |
| A17C643 | 283-0187-05 | B010100 | 8010107 | CAP,FXD,CER DI:0.047UF,10\%,500V (2440M ONLY) | 04222 | SR307C473KAAAP1 |
| A17C688 | 283-0429-00 |  |  | CAP,FXD,CER DI:270PF,20\%,2000V | 18796 | DHR12-Z5U271M |
| A17C689 | 283-0187-05 |  |  | CAP,FXD,CER DI:0.047UF,10\%,500V | 04222 | SR307C473KAAAP1 |
| A17C690 | 283-0167-02 |  |  | CAP,FXD,CER DI:0.1UF,10\%,100V | 04222 | SR591C104KAAAP1 |
| A17C692 | 283-0187-05 |  |  | CAP,FXD,CER DI:0.047UF,10\%,500V | 04222 | SR307C473KAAAP1 |
| A17C694 | 283-0167-02 |  |  | CAP,FXD,CER DI:0.1UF,10\%,100V | 04222 | SR591C104KAAAP1 |
| A17C957 | 283-0167-02 | B012403 |  | CAP,FXD,CER D: $0.1 \mathrm{UF}, 10 \%, 100 \mathrm{~V}$ (STANDARD ONLY) | 04222 | SR591C104KAAAP1 |
| A17C957 | 283-0167-02 | B010108 |  | CAP,FXD,CER DI:0.1UF,10\%,100V (2440M ONLY) | 04222 | SR591C104KAAAP1 |
| A17CR134 | 152-0574-0 |  |  | DIODE,SIG:,ULTRA FAST;120V,150MA,4NS | 27014 | FDH9876 |
| A17CR162 | 152-0141-02 | B012403 |  | DIODE,SIG:ULTRA FAST;40V,150MA,4NS,2PF (STANDARD ONLY) | 27014 | FDH9427 |
| A17CR162 | 152-0141-02 | B010108 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (2440M ONLY) | 27014 | FDH9427 |


| Component Number | Tektronix Part No. | Effecthe | No. Dscont | Name \& Description | Mfr. Code | Mr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A17CR217 | 152-0141-02 | B012403 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (STANDARD ONLY | 27014 | FDH9427 |
| A17CR217 | 152-0141-02 | B010108 |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF (2440M ONLY) | 27014 | FDH9427 |
| A17CR315 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST:40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A17CR411 | 152-0400-00 |  |  | DIODE,RECT:,FAST RCVRY; $400 \mathrm{~V}, 1 \mathrm{~A}, 200 \mathrm{NS}$ | 14552 | MB2501 |
| A17CR442 | 152-0061-0 |  |  | DIODE,SIG:;200V,0.1A,700NS,4.0PF | 27014 | FDH2161 |
| A17CR500 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A17CR541 | 152-0061-00 |  |  | DIODE,SIG:;200V,0.1A,700NS,4.0PF | 27014 | FDH2161 |
| A17CR565 | 152-0805-03 |  |  | MODULE,HV:;4.67KVAC IN,14KVDC OUT | 51406 | MSR8506B |
| A17CR610 | 152-0400-00 |  |  | DIODE,RECT;,FAST RCVRY; $400 \mathrm{~V}, 1 \mathrm{~A}, 200 \mathrm{NS}$ | 14552 | MB2501 |
| A17CR611 | 152-0400-00 |  |  | DIODE,RECT:,FAST RCVRY; $400 \mathrm{~V}, 1 \mathrm{~A}, 200 \mathrm{NS}$ | 14552 | MB2501 |
| A17CR643 | 152-0141-02 |  |  | DIODE,SIG:,ULTRA FAST;40V,150MA,4NS,2PF | 27014 | FDH9427 |
| A17CR644 | 152-0061-00 |  |  | DIODE,SIG:;200V,0.1A,700NS,4.0PF | 27014 | FDH2161 |
| A17DS490 | 150-0030-00 |  |  | LAMP,GLOW:60-90V MAX, 0.6 MA, A28-T,WIRE | OJ9R2 | NE-2B(AC/DC)R-T |
| A17DS491 | 150-0030-00 |  |  | LAMP,GLOW:60-90V MAX,0.6MA,A28-T,WIRE | OJ9R2 | NE-2B(AC/DC)R-T |
| A17J162 | 131-0608-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 2) | 22526 | 48283-018 |
| A17J172 | 131-0589-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 2) | 22526 | 48283-087 |
| A17J173 | 131-0589-00 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 2) | 22526 | 48283-087 |
| A17J174 | 131-0608-0 |  |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 9) | 22526 | 48283-018 |
| A17J176 | 131-0608-0 |  |  | TERMINAL,PIN:PRESSFIT/PCB;;MALE,STR (QUANTITY OF 9) | 22526 | 48283-018 |
| A17L605 | 108-0318-0 |  |  | COIL,RF:FIXED,100UH | OJRO3 | ORDER BY DESC |
| A17Q145 | 151-0443-00 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP;300V,500MA | 04713 | MPSA92 |
| A17Q152 | 151-0443-00 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP;300V,500MA | 04713 | MPSA92 |
| A17Q215 | 151-0444-0 | B010100 | B012402 | TRANSISTOR,SIG:BIPOLAR,NPN;350V,500MA | 04713 | 2N6517 |
| A17Q215 | 151-0443-03 | B012403 |  | TRANSISTOR,SIG:BIPOLAR,PNP;300V,500MA (STANDARD ONLY) | 04713 | MPSA92RLRP |
| A17Q215 | 151-0444-00 | B010100 | B010107 | TRANSISTOR,SIG:BIPOLAR,NPN;350V,500MA | 04713 | 2N6517 |
| A17Q215 | 151-0443-03 | B010108 |  | TRANSISTOR,SIG:BIPOLAR,PNP;300V,500MA (2440M ONLY) | 04713 | MPSA92RLRP |
| A170216 | 151-0444-0 | B012403 |  | TRANSISTOR,SIG:BIPOLAR,NPN;350V,500MA (STANDARD ONLY) | 04713 | 2N6517 |
| A17Q216 | 151-0444-00 | B010108 |  | TRANSISTOR,SIG:BIPOLAR,NPN;350V,500MA (2440M ONLY) | 04713 | 2N6517 |
| A17Q217 | 151-0192-05 | B012403 |  | TRANSISTOR,SIG:BIPOLAR,NPN;25V,100MA (STANDARD ONLY) | 04713 | SPS8801RLRP |
| A17Q217 | 151-0192-05 | B010108 |  | TRANSISTOR,SIG:BIPOLAR,NPN;25V,100MA (2440M ONLY) | 04713 | SPS8801RLRP |
| A170269 | 151-0443-00 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP;300V,500MA | 04713 | MPSA92 |
| A170500 | 151-0443- 0 |  |  | TRANSISTOR,SIG:BIPOLAR,PNP;300V,500MA | 04713 | MPSA92 |


| Component Number | Tektronix <br> Part No. | Seria Effective | No. Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A170628 | 151-0816-00 |  |  | TRANSISTOR,PWR:BIPOLAR,PNP;120V,8.0A,20MHZ | O.R04 | 2SA1264N-R |
| A170640 | 151-0444-0 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;350V,500MA | 04713 | 2N6517 |
| A170641 | 151-0276-01 | B012403 |  | TRANSISTOR,SIG:BIPOLAR,PNP;5OV,50MA,40MHZ (STANDARD ONLY | 04713 | 2N5087RLRP |
| A17Q641 | 151-0276-01 | B010108 |  | TRANSISTOR,SIG:BIPOLAR,PNP;50V,50MA,40MHZ (2440M ONLY) | 04713 | 2N5087RLRP |
| A17R100 | 311-2234-00 |  |  | RES,VAR,TRMR:CERMET; 5 K OHM, $20 \%, 0.5 \mathrm{~W}$ | TK2073 | GF06UT2 502 M L |
| A17R119 | 315-0102-00 | B010100 | B012402 | RES,FXD,FILM:1K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A17R119 | 315-0102-03 | B012403 |  | RES,FXD,CMPSN: 1 K OHM,5\%,0.25W (STANDARD ONLY) | 50139 | CB1025 |
| A17R119 | 315-0102-00 | B010100 | 8010107 | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A17R119 | 315-0102-03 | B010108 |  | RES,FXD,CMPSN:1K OHM,5\%,0.25W (2440M ONLY | 50139 | CB1025 |
| A17R122 | 321-0267-00 | B010100 | B012402 | RES,FXD,FILM:5.90K OHM, 1\%,0.125W,TC=TO | 19701 | 5033ED5K900F |
| A17R122 | 322-3267-00 | B012403 |  | RES,FXD,FILM:5.9K OHM,1\%,0.2W,TC=TO (STANDARD ONLY) | 56845 | CCF50-2-G5901FT |
| A17R122 | 321-0267-00 | B010100 | $B 010107$ | RES,FXD,FILM:5.90K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033ED5K900F |
| A17R122 | 322-3267-00 | B010108 |  | RES,FXD,FILM:5.9K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO (2440M ONLY) | 56845 | CCF50-2-G5901FT |
| A17R137 | 301-0752-00 |  |  | RES,FXD,FILM:7.5K OHM,5\%,0.5W | TK1727 | SFR30 2322-182 |
| A17R145 | 321-0368-00 |  |  | RES,FXD,FILM: 66.5 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5043ED66K50F |
| A17R160 | 315-0202-00 | B010100 | B012402 | RES,FXD,FILM:2K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A17R160 | 322-3222-0 | B012403 |  | RES,FXD:METAL FILM;2K OHM,1\%,0.2W (STANDARD ONLY | 91637 | CCF501G20000F |
| A17R160 | 315-0202-m | B010100 | B010107 | RES,FXD,FILM:2K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A17R160 | 322-3222-00 | B010108 |  | RES,FXD:METAL FILM;2K OHM, $1 \%, 0.2 W$ (2440M ONLY) | 91637 | CCF501G20000F |
| A17R161 | 313-1224-00 |  |  | RES, FXD,FILM:220K,5\%,0.2W | 91637 | CCF50-2-22002J |
| A17R162 | 313-1272-0 | B010100 | B012402 | RES,FXD,FILM:2.7K OHM,5\%,0.2W | 91637 | CCF50-2-27000J |
| A17R162 | 313-1103-00 | B012403 | B012656 | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A17R162 | 313-1272-00 | B012657 |  | RES,FXD,FILM:2.7K OHM,5\%,0.2W (STANDARD ONLY) | 91637 | CCF50-2-27000 J |
| A17R162 | 313-1272-00 | B010100 | B010107 | RES,FXD,FILM:2.7K OHM,5\%,0.2W | 91637 | CCF50-2-27000. |
| A17R162 | 313-1103-00 | B010108 | B010110 | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A17R162 | 313-1272-00 | B010111 |  | RES,FXD,FILM:2.7K OHM,5\%,0.2W (2440M ONLY) | 91637 | CCF50-2-27000J |
| A17R170 | 313-1272-00 | B010100 | 8012402 | RES,FXD,FILM: 2.7 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-27000 |
| A17R170 | 322-3231-00 | B012403 | B013320 | RES,FXD,FILM:2.49K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF50-1G24900F |
| A17R170 | 322-3239-00 | B013321 |  | RES,FXD,FILM:3.01K OHM, $1 \%, 0.2 W, T C=$ TO (STANDARD ONLY) | 91637 | CCF501G30100F |
| A17R170 | 313-1272-00 | B010100 | B010107 | RES,FXD,FILM:2.7K OHM,5\%,0.2W | 91637 | CCF50-2-27000J |
| A17Ri70 | 322-3231-00 | B010108 | B010118 | RES,FXD,FILM: 2.49 K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF50-1G24900F |
| A17R170 | 322-3239-0 | B010119 |  | RES,FXD,FILM: 3.01 K OHM, $1 \%, 0.2 W, T C=$ TO (2440M ONLY) | 91637 | CCF501G30100F |


| Component Number | Tektronix <br> Part No. | Serial Effective | No. Dscont | Name \& Description | Mitr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A17R178 | 313-1393-00 | B010100 | B012402 | RES,FXD,FILM:39K OHM,5\%,0.2W | 91637 | CCF50-2-39001J |
| A17R178 | 322-3346-0 | B012403 |  | RES,FXD:METAL FILM;39.2K OHM,1\%,0.2W (STANDARD ONLY) | 91637 | CCF50-2-G39201F |
| A17R178 | 313-1393- ${ }^{\text {a }}$ | B010100 | B010107 | RES,FXD,FILM:39K OHM,5\%,0.2W | 91637 | CCF50-2-39001J |
| A17R178 | 322-3346-00 | B010108 |  | RES,FXD:METAL FILM;39.2K OHM,1\%,0.2W (2440M ONLY) | 91637 | CCF50-2-G39201F |
| A17R179 | 321-0693-00 |  |  | RES,FXD,FILM: 68.1 K OHM, $0.5 \%, 0.125 W, T C=$ TO | 19701 | 5033RD6812DB298 |
| A17R180 | 313-1103-00 | B012403 |  | RES,FXD,FILM: 10 K OHM, $5 \%, 0.2 \mathrm{~W}$ (STANDARD ONLY) | 91637 | CCF50-2-10001J |
| A17R180 | 313-1103-00 | B010108 |  | RES,FXD,FILM:1OK OHM,5\%,0.2W (2440M ONLY) | 91637 | CCF50-2-10001J |
| A17R200 | 311-2239-0 |  |  | RES,VAR, TRMR:CERMET; 100 K OHM, $20 \%, 0.5 \mathrm{~W}$ | TK2073 | GF06UT2 104 ML |
| A17R209 | 321-0245-0 | B010100 | $B 012402$ | RES,FXD,FILM:3.48K OHM,1\%,0.125W,TC=TO (STANDARD ONLY) | 19701 | 5033ED3K48F |
| A17R209 | 321-0245-0 | B010100 | B010107 | RES,FXD,FILM:3.48K OHM,1\%,0.125W,TC=TO (2440M ONLY) | 19701 | 5033ED3K48F |
| A17R216 | 322-3322-0 | B012403 |  | RES,FXD:METAL FILM;22.1K OHM,1\%,0.2W (STANDARD ONLY) | 91637 | CCF501G22101F |
| A17R216 | 322-3322-00 | B010108 |  | RES,FXD:METAL FILM; 22.1 K OHM,1\%,0.2W (2440M ONLY) | 91637 | CCF501G22101F |
| A17R218 | 322-3373-00 | B012403 |  | RES,FXD,FILM:75K OHM,1\%,0.2W,TC=TO (STANDARD ONLY) | 91637 | CCF501G75001F |
| A17R218 | 322-3373-00 | B010108 |  | RES,FXD,FILM:75K OHM,1\%,0.2W,TC=T0 (2440M ONLY) | 91637 | CCF501G75001F |
| A17R219 | 322-3327-00 | B012403 |  | RES,FXD,FLLM:24.9K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO (STANDARD ONLY) | 91637 | CCF50-2-G24901F |
| A17R219 | 322-3327-00 | B010108 |  | RES,FXD,FILM: $24.9 \mathrm{KOHM}, 1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ To (2440M ONLY) | 91637 | CCF50-2-G24901F |
| A17R220 | 322-3193-00 | B012403 |  | RES,FXD:METAL FILM;1K OHM,1\%,0.2W (STANDARD ONLY | 91637 | CCF501G10000F |
| A17R220 | 322-3193-00 | B010108 |  | RES,FXD:METAL FILM;1K OHM,1\%,0.2W (2440M ONLY) | 91637 | CCF501G10000F |
| A17R221 | 315-0620-02 | B012403 |  | RES,FXD,CMPSN:62 OHM,5\%,0.25W (STANDARD ONLY) | 50139 | CB6205 |
| A17R221 | 315-0620-02 | $B 010108$ |  | RES,FXD,CMPSN:62 OHM,5\%,0.25W (2440M ONLY) | 50139 | CB6205 |
| A17R233 | 313-1560-00 | B010100 | B012402 | RES,FXD,FILM: 56 OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-56R00J |
| A17R233 | 315-0620-02 | B012403 |  | RES,FXD,CMPSN:62 OHM,5\%,0.25W (STANDARD ONLY) | 50139 | CB6205 |
| A17R233 | 313-1560-00 | B010100 | B010107 | RES,FXD,FILM: 56 OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-56R00J |
| A17R233 | 315-0620-02 | B010108 |  | RES,FXD,CMPSN: 62 OHM,5\%,0.25W (2440M ONLY) | 50139 | CB6205 |
| A17R245 | 322-3438-00 | B010100 | B012402 | RES,FXD,FILM:357K OHM, 1\%,0.2W,TC=T0 | 91637 | CCF501G35702F |
| A17R245 | 321-0438-00 | B012403 |  | RES,FXD,FILM:357K OHM,1\%,0.125W,TC=TO (STANDARD ONLY) | 19701 | 5043ED357KOF |
| A17R245 | 322-3438-00 | B010100 | B010107 | RES,FXD,FILM:357K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF501G35702F |


| Component Number | Tektronix <br> Part No. | Effective | No. Dscont | Name \& Description | Mir. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A17R245 | 321-0438-00 | B010108 |  | RES,FXD,FILM:357K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 (2440M ONLY) | 19701 | 5043ED357KOF |
| A17R246 | 321-0447-00 |  |  | RES,FXD,FILM:442K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED442KOF |
| A17R247 | 321-0393-00 |  |  | RES,FXD,FILM:121K OHM, 1\%,0.125W,TC=T0 | TK1727 | 2322-151-121K |
| A17R248 | 321-0407-00 |  |  | RES,FXD,FILM:169K OHM, 1\%,0.125W,TC=T0 | 19701 | 5043ED169KOF |
| A17R260 | 321-0393-00 | B010100 | B012402 | RES,FXD,FILM: 121 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ To | TK1727 | 2322-151-121K |
| A17R260 | 313-1124-00 | B012403 |  | RES,FXD,FILM:120K OHM, $5 \%, 0.2 \mathrm{~W}$ (STANDARD ONLY) | 91637 | CCF50-2-12002J |
| A17R260 | 321-0393-00 | B010100 | B010107 | RES,FXD,FILM:121K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ To | TK1727 | 2322-151-121K |
| A17R260 | 313-1124-00 | B010108 |  | RES,FXD,FILM:120K OHM,5\%,0.2W (2440M ONLY) | 91637 | CCF50-2-12002.J |
| A17R261 | 321-0367-00 |  |  | RES,FXD,FILM:64.9K OHM, 1\%,0.125W, TC = To | 19701 | 5043ED64K90F |
| A17R262 | 321-0413-00 |  |  | RES,FXD,FILM:196K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ To | 19701 | 5043ED196KOF |
| A17R263 | 321-0693-07 | B010100 | B013320 | RES,FXD,FILM:196K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ To | 80009 | 321069307 |
| A17R263 | 321-0385-07 | B013321 |  | RES,FXD,FILM: 100 K OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T9 | TK1727 | MPR24-2322-141 |
| A17R263 | 321-0693-07 | B013321 |  | RES,FXD,FILM:100K OHM,0.1\%,0.125W,TC=T9 (SELECTABLE VALUE) (STANDARD ONLY) | 80009 | 321069307 |
| A17R263 | 321-0693-07 | B010100 | B010118 | RES,FXD,FILM:100K OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T9 | 80009 | 321069307 |
| A17R263 | 321-0385-07 | B010119 |  | RES,FXD,FILM: 100 K OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=\mathrm{T} 9$ | TK1727 | MPR24-2322-141 |
| A17R263 | 321-0693-07 | B010119 |  | RES,FXD,FILM:100K OHM,0.1\%,0.125W,TC=T9 (SELECTALBE VALUE) (2440M ONLY) | 80009 | 321069307 |
| A17R278 | 321-0481-07 | B010100 | B012402 | RES,FXD,FILM:1M OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T9 | 19701 | 5033RE1M000B |
| A17R278 | 321-0481-04 | B012403 |  | RES,FXD,FILM:1M OHM,0.1\%,0.125W,TC $=$ T2 (STANDARD ONLY) | 19701 | 5033RC1M000B |
| A17R278 | 321-0481-07 | B010100 | B010107 | RES,FXD,FILM:1M OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T9 | 19701 | 5033RE1M000B |
| A17R278 | 321-0481-04 | B010108 |  | RES,FXD,FILM:1M OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=\mathrm{T} 2$ (2440M ONLY) | 19701 | 5033RC1M000B |
| A17R279 | 321-0481-07 | B010100 | B012402 | RES,FXD,FILM: 1 M OHM $, 0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T9 | 19701 | 5033RE1M000B |
| A17R279 | 321-0481-04 | B012403 |  | RES,FXD,FILM:1M OHM,0.1\%,0.125W,TC=T2 (STANDARD ONLY) | 19701 | 5033RC1M000B |
| A17R279 | 321-0481-07 | B010100 | B010107 | RES,FXD,FILM: 1 M OHM, $0.1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=\mathrm{T} 9$ | 19701 | 5033RE1M000B |
| A17R279 | 321-0481-04 | B010108 |  | RES,FXD,FILM:1M OHM,0.1\%,0.125W,TC $=$ T2 (2440M ONLY) | 19701 | 5033RC1MOOOB |
| A17R297 | 321-0245-00 |  |  | RES,FXD,FILM:3.48K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ T0 | 19701 | 5033ED3K48F |
| A17R298 | 315-0101-03 | B012403 |  | RES,FXD,CMPSN: 100 OHM,5\%,0.25W (STANDARD ONLY) | 50139 | CB1015 |
| A17R298 | 315-0101-03 | B010108 |  | RES,FXD,CMPSN:100 OHM,5\%,0.25W (2440M ONLY) | 50139 | CB1015 |
| A17R300 | 311-2236-0 |  |  | RES,VAR,TRMR:CERMET;20K OHM,20\%,0.5W | TK2073 | GF06UT2 203 M L |
| A17R305 | 311-2234-00 |  |  | RES,VAR,TRMR:CERMET;5K OHM, $20 \%, 0.5 \mathrm{~W}$ | TK2073 | GFO6UT2 502 ML |
| A17R315 | 313-1512-0 | B010100 | B012402 | RES,FXD,FILM:5.1K OHM,5\%,0.2W | 91637 | CCF50-2-51000J |
| A17R315 | 322-3235-0 | B012403 |  | RES,FXD:METAL FILM;2.74K OHM, $1 \%, 0.2 \mathrm{~W}$ (STANDARD ONLY) | 91637 | CCF501G27400F |


| Component Number | Tektronix <br> Part No. | Serial Effective | No. Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A17R315 | 313-1512-00 | B010100 | B010107 | RES,FXD,FILM:5.1 K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-51000J |
| A17R315 | 322-3235-00 | B010108 |  | RES,FXD:METAL FILM;2.74K OHM,1\%,0.2W (2440M ONLY) | 91637 | CCF501G27400F |
| A17R316 | 313-1180-00 | 8012403 |  | RES,FXD,FILM: 18 OHM,5\%,0.2W (STANDARD ONLY) | 91637 | CCF50-2-18R00J |
| A17R316 | 313-1180-0 | B010108 |  | RES,FXD,FILM: 18 OHM,5\%,0.2W (2440M ONLY) | 91637 | CCF50-2-18R00J |
| A17R393 | 315-0102-0 | 8010100 | B010696 | RES,FXD,FILM: 1 K OHM, $5 \%, 0.25 \mathrm{~W}$ | TK1727 | SFR25 2322-181 |
| A17R393 | 315-0102-03 | B010697 |  | RES,FXD,CMPSN:1K OHM,5\%,0.25W (STANDARD ONLY) | 50139 | CB1025 |
| A17R393 | 315-0102-03 |  |  | RES,FXD,CMPSN:1K OHM,5\%,0.25W (2440M ONLY) | 50139 | CB1025 |
| A17R395 | 321-0271-00 |  |  | RES,FXD,FILM: 6.49 K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED6K490F |
| A17R400 | 311-2236-00 |  |  | RES,VAR,TRMR:CERMET; 20 K OHM, $20 \%, 0.5 \mathrm{~W}$ | TK2073 | GF06UT2 203 ML |
| A17R442 | 313-1331-0 | B010100 | B012402 | RES,FXD,FILM:330 OHM,5\%,0.2W | 91637 | CCF50-2-330ROJ |
| A17R442 | 315-0331-03 | B012403 |  | RES,FXD,CMPSN:330 OHM 5\%,0.25W (STANDARD ONLY) | 50139 | CB3315 ALLEN BR |
| A17R442 | 313-1331-00 | B010100 | B010107 | RES,FXD,FILM:330 OHM, 5\%,0.2W | 91637 | CCF50-2-330ROJ |
| A17R442 | 315-0331-03 | B010108 |  | RES,FXD,CMPSN:330 OHM 5\%,0.25W (2440M ONLY) | 50139 | CB3315 ALLEN BR |
| A17R443 | 315-0162-00 |  |  | RES,FXD,FILM:1.6K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A17R500 | 313-1512-0 | B010100 | B012402 | RES,FXD,FILM:5.1K OHM,5\%,0.2W | 91637 | CCF50-2-51000J |
| A17R500 | 315-0512-0 | B012403 |  | RES,FXD,FILM:5.1K OHM,5\%,0.25W (STANDARD ONLY) | TK1727 | SFR25 2322-181 |
| A17R500 | 313-1512-0 | B010100 | B010107 | RES.FXD,FILM:5.1K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-51000J |
| A17R500 | 315-0512-0 | B010108 |  | RES,FXD,FILM:5.1K OHM,5\%,0.25W (2440M ONLY) | TK1727 | SFR25 2322-181 |
| A17R543 | 313-1393-00 | B010100 | B012402 | RES,FXD,FILM:39K OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-39001J |
| A17R543 | 315-0393-00 | B012403 |  | RES,FXD,FILM:39K OHM,5\%,0.25W (STANDARD ONLY) | TK1727 | SFR25 2322-181 |
| A17R543 | 313-1393-00 | B010100 | B010107 | RES,FXD,FILM:39K OHM,5\%,0.2W | 91637 | CCF50-2-39001J |
| A17R543 | 315-0393-00 | B010108 |  | RES,FXD,FILM:39K OHM,5\%,0.25W (2440M ONLY) | TK1727 | SFR25 2322-181 |
| A17R546 | 313-1201-00 | B010100 | B012402 | RES,FXD,FILM:200 OHM, 5\%,0.2W | 91637 | CCF50-2-200ROJ |
| A17R546 | 315-0201-02 | B012403 |  | RES,FXD,CMPSN:200 OHM,5\%,0.25W (STANDARD ONLY) | 50139 | CB2015 |
| A17R546 | 313-1201-00 | B010100 | B010107 | RES,FXD,FILM:200 OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-200ROJ |
| A17R546 | 315-0201-02 | B010108 |  | RES,FXD,CMPSN:200 OHM,5\%,0.25W (2440M ONLY | 50139 | CB2015 |
| A17R620 | 313-1220-00 |  |  | RES,FXD,FILM:22 OHM,5\%,0.2W | 91637 | CCF50-2-22R00J |
| A17R639 | 322-3385-00 | 8012403 |  | RES,FXD:METAL FILM; 100 K OHM, $1 \%, 0.2 W$ (STANDARD ONLY) | 91637 | CCF501G10002F |
| A17R639 | 322-3385-0 | B010108 |  | RES,FXD:METAL FILM;100K OHM,1\%,0.2W (2440M ONLY) | 91637 | CCF501G10002F |


| Component Number | Tektronlx Part No. | Serial Eftective | No. Dscont | Name \& Description | Mfr. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A17R641 | 322-3385-00 | B012403 |  | RES,FXD:METAL FILM;100K OHM,1\%,0.2W (STANDARD ONLY) | 91637 | CCF501G10002F |
| A17R641 | 322-3385-00 | B010108 |  | RES,FXD:METAL. FILM; 100 K OHM, $1 \%, 0.2 W$ (2440M ONLY) | 91637 | CCF501G10002F |
| A17R642 | 321-0407-0 | B010100 | B012402 | RES,FXD,FILM:169K OHM, 1\%,0.125W,TC=TO | 19701 | 5043ED169KOF |
| A17R642 | 322-3426-0 | B012403 |  | RES,FXD,FILM:267K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO (STANDARD ONLY) | 91637 | CCF50-2F26702F |
| A17R642 | 321-0407-0 | 8010100 | B010107 | RES,FXD,FILM:169K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO | 19701 | 5043ED169KOF |
| A17R642 | 322-3426-0 | B010108 |  | RES,FXD,FILM:267K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO (2440M ONLY)LY) | 91637 | CCF50-2F26702F |
| A17R643 | 313-1103-00 | 8010100 | B012402 | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A17R643 | 315-0103-03 | B012403 |  | RES,FXD,CMPSN:10K OHM,5\%,0.25W | 50139 | CB1035 |
| A17R643 | 313-1103-00 | B010100 | B010107 | RES,FXD,FILM:10K OHM,5\%,0.2W | 91637 | CCF50-2-10001J |
| A17R643 | 315-0103-03 | 8012403 |  | RES,FXD,CMPSN:10K OHM,5\%,0.25W (STANDARD ONLY) | 50139 | CB1035 |
| A17R644 | 313-1224-00 | B010100 | 8012402 | RES,FXD,FILM:220K,5\%,0.2W | 91637 | CCF50-2-22002J |
| A17R644 | 322-3421-0 | B012403 |  | RES,FXD,FILM:237K OHM,1\%,0.2W.TC=TO (STANDARD ONLY) | 91637 | CCF50-2F23702F |
| A17R644 | 313-1224-00 | B010100 | $B 010107$ | RES,FXD,FLLM:220K,5\%,0.2W | 91637 | CCF50-2-22002J |
| A17R644 | 322-3421-00 | B010108 |  | RES,FXD,FILM:237K OHM, $1 \%, 0.2 \mathrm{~W}$, TC $=$ TO (2440M ONLY) | 91637 | CCF50-2F23702F |
| A17R645 | 321-0463-00 | B010100 | B012402 | RES,FXD,FILM:649K OHM, 1\%,0.125W | 19701 | 5033YD649KOF |
| A17R645 | 321-0481-04 | B012403 |  | RES,FXD,FILM:1M ОНM, $0.1 \%, 0.125 W, T C=T 2$ (STANDARD ONLY | 19701 | 5033RC1M000B |
| A17R645 | 321-0463-00 | B010100 | B010107 | RES.FXD.FILM:649K OHM, 1\%,0.125W | 19701 | 5033YD649KOF |
| A17R645 | 321-0481-04 | B010108 |  | RES,FXD,FILM:1M OHM,0.1\%,0.125W,TC=T2 (2440M ONLY) | 19701 | 5033RC1M000B |
| A17R689 | 322-3438-00 | B010100 | B012402 | RES,FXD,FILM:357K OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CCF501G35702F |
| A17R689 | 321-0438-00 | B012403 |  | RES,FXD,FILM:357K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO (STANDARD ONLY) | 19701 | 5043ED357K0F |
| A17R689 | 322-3438-00 | B010100 | B010107 | RES,FXD,FILM:357K OHM, 1\%,0.2W,TC=T0 | 91637 | CCF501G35702F |
| A17R689 | 321-0438-00 | B010108 |  | RES,FXD,FILM:357K OHM, $1 \%, 0.125 \mathrm{~W}, \mathrm{TC}=$ TO (2440M ONLY) | 19701 | 5043ED357KOF |
| A17R690 | 315-0102-00 | B010100 | B012402 | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A17R690 | 315-0102-03 | B012403 |  | RES,FXD,CMPSN: 1 K OHM,5\%,0.25W (STANDARD ONLY) | 50139 | CB1025 |
| A17R690 | 315-0102-00 | B010100 | B010107 | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A17R690 | 315-0102-03 | B010108 |  | RES,FXD,CMPSN: 1 K OHM,5\%,0.25W (2440M ONLY) | 50139 | CB1025 |
| A17R691 | 315-0102-00 | B010100 | B010696 | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A17R691 | 315-0102-03 | B010697 |  | RES,FXD,CMPSN:1K OHM,5\%,0.25W (STANDARD ONLY) | 50139 | CB1025 |
| A17R691 | 315-0102-03 |  |  | RES,FXD,CMPSN: 1 K OHM, $5 \%, 0.25 \mathrm{~W}$ (2440M ONLY) | 50139 | CB1025 |
| A17R693 | 315-0102-00 | B010100 | B010696 | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |


| Component Number | Tektronix Part No. | Serla <br> Effective | No. Dscont | Name \& Description | Mtr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A17R693 | 315-0102-03 | B010697 |  | RES,FXD,CMPSN:1K OHM,5\%,0.25W (STANDARD ONLY) | 50139 | CB1025 |
| A17R693 | 315-0102-03 |  |  | RES,FXD,CMPSN:1K OHM,5\%,0.25W (2440M ONLY) | 50139 | CB1025 |
| A17R694 | 315-0102-00 | B010100 | B010696 | RES,FXD,FILM:1K OHM,5\%,0.25W | TK1727 | SFR25 2322-181 |
| A17R694 | 315-0102-03 | B010697 |  | RES,FXD,CMPSN:1K OHM,5\%,0.25W (STANDARD ONLY) | 50139 | CB1025 |
| A17R694 | 315-0102-03 |  |  | RES,FXD,CMPSN:1K OHM,5\%,0.25W (244OM ONLY) | 50139 | CB1025 |
| A17R976 | 315-0102-03 | B012403 |  | RES,FXD,CMPSN:1K OHM,5\%,0.25W (STANDARD ONLY) | 50139 | CB1025 |
| A17R976 | 315-0102-03 | B010108 |  | RES,FXD,CMPSN:1K OHM,5\%,0.25W (2440M ONLY) | 50139 | CB1025 |
| A17T525 | 120-1548-00 |  |  | TRANSFORMER,RF:HIGH VOLTAGE | 75498 | 120-1548-00 |
| A17U168 | 156-0158-07 |  |  | IC,LINEAR:BIPOLAR,OP-AMP | 01295 | MC1458P |
| A17U227 | 155-0294-00 | B010100 | 8013860 | MICROCKT,LINEAR:Z-AXIS AMPLIFIER | 80009 | 155029400 |
| A17U227 | 155-0294-01 | B013861 |  | IC,ASIC:BIPOLAR,Z-AXIS TRIGGER | 80009 | 155029401 |
| A17NR209 | 152-0217-00 | B012403 |  | DIODE,ZENER:;8.2V,5\%,0.4W (STANDARD ONLY) | 04713 | SZG20RL |
| A17VR209 | 152-0217-00 | B010108 |  | DIODE,ZENER:;;8.2V,5\%,0.4W (2440M ONLY) | 04713 | SZG20RL |
| A17VR210 | 152-0285-00 | B010100 | B012402 | DIODE,ZENER:,;62V,5\%,0.4W (STANDARD ONLY) | 04713 | 1N980BRL |
| A17VR210 | 152-0285-0 | B010100 | B010107 | DIODE,ZENER:;62V,5\%,0.4W (2440M ONLY) | 04713 | 1N980BRL |
| A17VR316 | 152-0243-0 |  |  | DIODE,ZENER:,;15V,5\%,0.4W | 04713 | SZ13203 |
| A17W175 | 175-9231-01 |  |  | CA ASSY,SP:RIBBON; CPR,7,26 AWG,2.75 L | 0.J7N9 | ORDER BY DESC |


| Component <br> Number | Tektronix <br> Part No. | Serial No. <br> Effective <br> Dscont | Name \& Description | Mfr. <br> Code | Mfr. Part No. |
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| A18 | $670-7280-0$ |  | CIRCUIT BD ASSY:SCALE ILLUM | 80009 | 670728000 |
|  |  |  |  |  |  |
| A18DS100 | 150-0057-01 |  | LAMP,INCAND:5V,0.115A,WIRE LD,AGED \& SEL | S3774 | OL7153AS15TPL |
| A18DS101 | $150-0057-01$ |  | LAMP,INCAND:5V,0.115A,WIRE LD,AGED \& SEL | S3774 | OL7153AS15TPL |
| A18DS102 | 150-0057-01 |  | LAMP,INCAND:5V,0.115A,WIRE LD,AGED \& SEL | S3774 | OL7153AS15TPL |


| Component Number | Tektronix Part No. | Seria Effective | No. Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A30 | 671-0367-00 |  |  | CIRCUIT BD ASSY:CCD OUT | 80009 | 671036700 |
| A30C114 | 281-0798-00 |  |  | CAP,FXD,CER DI:51PF,1\%,100V | TK1743 | CGB510GEN |
| A30C115 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A30C116 | 281-0909-0 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A30C121 | 281-0798-00 |  |  | CAP,FXD,CER DI:51PF,1\%,100V | TK1743 | CGB510GEN |
| A30.115 | 131-4553-0 | B010100 | B012361 | CONN,HDR::PCB,:MALE,RTANG, $1 \times 5,0.1$ CTR (QUANTITY OF 4) | 53387 | 2405-5112TB |
| A30.J115 | 131-4554-0 | $B 010100$ | B012361 | CONN,HDR:PCB,;MALE,RTANG, $1 \times 8,0.1$ CTR (QUANTITY OF 4) | 53387 | 2408-5112TB |
| A30.J115 | 131-0608-00 | B012362 |  | TERMINAL,PIN:PRESSFIT/PCB,MALE,STR (QUANTITY OF ${ }^{13)}$ <br> (STANDARD ONLY | 22526 | 48283-018 |
| A30,115 | 131-4553-00 | B010100 | B010106 | CONN,HDR::PCB,;MALE,RTANG, $1 \times 5,0.1$ CTR (QUANTITY OF 4) | 53387 | 2405-5112TB |
| A30,115 | 131-4554-00 | B010100 | B010106 | CONN,HDR:PCB,;MALE,RTANG, $1 \times 8,0.1$ CTR (QUANTITY OF 4) | 53387 | 2408-51 12TB |
| A30J115 | 131-0608-00 | B010107 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 13) (2440M ONLY | 22526 | 48283-018 |
| A30Q111 | 151-0341-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;45V,50MA,40MHZ | 04713 | MPS6520 |
| A30Q112 | 151-0341-0 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;45V,50MA,40MHZ | 04713 | MPS6520 |
| A30Q428 | 151-0341-0 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN:45V,50MA,40MHZ | 04713 | MPS6520 |
| A30Q129 | 151-0341-0 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;45V,50MA,40MHZ | 04713 | MPS6520 |
| A30R111 | 322-3193- |  |  | RES,FXD:METAL FILM; 1 K OHM,1\%,0.2W | 91637 | CCF501G10000F |
| A30R112 | 322-3175-00 |  |  | RES,FXD,FILM:649 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CCF50G649ROF |
| A30R113 | 322-3145-00 |  |  | RES,FXD,FILM:316 OHM, $1 \%, 0.2 W, T C=$ TO | 91637 | CCF50G316ROF |
| A30R114 | 322-3145-00 |  |  | RES,FXD,FILM:316 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ To | 91637 | CCF50G316R0F |
| A30R115 | 322-3193-00 |  |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A30R116 | 322-3193-00 |  |  | RES,FXD:METAL FILM; 1 K OHM, 1\%,0.2W | 91637 | CCF501G10000F |
| A30R117 | 313-1821-00 |  |  | RES,FXD,FILM:820 OHM,5\%,0.2W | 91637 | CCF50-2-820ROJ |
| A30R118 | 313-1100-00 |  |  | RES,FXD,FILM: 10 OHM,5\%,0.2W | 91637 | CCF50-2-10ROOJ |
| A30R120 | 322-3193-0 |  |  | RES,FXD:METAL FILM; 1 K OHM,1\%,0.2W | 91637 | CCF501G10000F |
| A30R121 | 313-1821-00 |  |  | RES,FXD,FILM:820 OHM,5\%,0.2W | 91637 | CCF50-2-820ROJ |
| A30R122 | 313-1100-00 |  |  | RES,FXD,FILM:10 OHM,5\%,0.2W | 91637 | CCF50-2-10R00J |
| A30R123 | 313-1751-00 |  |  | RES,FXD,FILM:750 OHM,5\%,0.2W | 91637 | CCF50-2-750ROS |
| A30R124 | 313-1751-0 |  |  | RES,FXD,FILM: 750 OHM,5\%,0.2W | 91637 | CCF50-2-750ROS |
| A30R125 | 322-3145-00 |  |  | RES,FXD,FILM: 316 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ To | 91637 | CCF50G316ROF |
| A30R126 | 322-3193-00 |  |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A30R127 | 322-3145-00 |  |  | RES,FXD,FILM:316 OHM, 1\%,0.2W,TC=T0 | 91637 | CCF50G316ROF |
| A30R128 | 322-3193-00 |  |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A30R129 | 322-3175-00 |  |  | RES,FXD,FILM: 649 OHM,1\%,0.2W,TC=TO | 91637 | CCF50G649ROF |
| A30U111 | 156-3293-00 |  |  | IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY | 24355 | MAT04-006P |
| A30U118 | 156-1272-00 |  |  | IC,LINEAR:BIPOLAR,OP-AMP;DUAL,HIGH OUTPUT | 01295 | NE5532P |
| A30U125 | 156-3293-00 |  |  | IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY | 24355 | MAT04-006P |


| Component Number | Tektronix Part No. | Seria Effective | No. Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A31 | 671-0367-00 |  |  | CIRCUIT BD ASSY:CCD OUT | 80009 | 671036700 |
| A31C114 | 281-0798-00 |  |  | CAP,FXD,CER DI:51PF,1\%,100V | TK1743 | CGB510GEN |
| A31C115 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A31C116 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A31C121 | 281-0798-0 |  |  | CAP,FXD,CER DI:51PF,1\%,100V | TK1743 | CGB510GEN |
| A30.J115 | 131-4553-00 | B010100 | B012361 | CONN,HDR::PCB,;MALE,RTANG, $1 \times 5,0.1$ CTR (QUANTITY OF 4) | 53387 | 2405-5112TB |
| A30.115 | 131-4554-0 | B010100 | B012361 | CONN,HDR:PCB;,MALE,RTANG,1 $\times 8,0.1$ CTR (QUANTITY OF 4) | 53387 | 2408-5112TB |
| A30.115 | 131-0608-0 | B012362 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 13) <br> (STANDARD ONLY) | 22526 | 48283-018 |
| A30.1115 | 131-4553-00 | B010100 | B010106 | CONN,HDR::PCB;,MALE,RTANG, $1 \times 5,0.1$ CTR (QUANTITY OF 4) | 53387 | 2405-5112TB |
| A30.J115 | 131-4554-00 | 3010100 | B010106 | CONN,HDR:PCB,;MALE,RTANG, $1 \times 8,0.1$ CTR (QUANTITY OF 4) | 53387 | 2408-5112TB |
| A30.J115 | 131-0608-0 | B010107 |  | TERMINAL,PIN:PRESSFIT/PCB,MALE,STR (QUANTITY OF ${ }^{13)}$ (2440M ONLY) | 22526 | 48283-018 |
| A31Q111 | 151-0341-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;45V,50MA,40MHZ | 04713 | MPS6520 |
| A31Q112 | 151-0341-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN; $45 \mathrm{~V}, 50 \mathrm{MA}, 40 \mathrm{MHZ}$ | 04713 | MPS6520 |
| A31Q128 | 151-0341-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;45V,50MA,40MHZ | 04713 | MPS6520 |
| A31Q129 | 151-0341-0 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;45V,50MA,40MHZ | 04713 | MPS6520 |
| A31R111 | 322-3193-00 |  |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 W$ | 91637 | CCF501G10000F |
| A31R112 | 322-3175-00 |  |  | RES,FXD,FILM:649 OHM, $1 \%, 0.2 W, T C=$ T0 | 91637 | CCF50G649ROF |
| A31R113 | 322-3145- |  |  | RES,FXD,FILM:316 OHM, $1 \%, 0.2 W, T C=$ T0 | 91637 | CCF50G316ROF |
| A31R114 | 322-3145- 0 |  |  | RES,FXD,FILM: 316 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CCF50G316ROF |
| A31R115 | 322-3193-0 |  |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A31R116 | 322-3193-00 |  |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A31R117 | 313-1821-0 |  |  | RES,FXD,FILM:820 OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-820ROJ |
| A31R118 | 313-1100-0 |  |  | RES,FXD,FILM:10 OHM, 5\%,0.2W | 91637 | CCF50-2-10ROOS |
| A31R120 | 322-3193-00 |  |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A31R121 | 313-1821-00 |  |  | RES,FXD,FILM:820 OHM,5\%,0.2W | 91637 | CCF50-2-820ROJ |
| A31R122 | 313-1100-00 |  |  | RES,FXD,FILM:10 OHM,5\%,0.2W | 91637 | CCF50-2-10ROOJ |
| A31R123 | 313-1751-00 |  |  | RES,FXD,FILM:750 OHM,5\%,0.2W | 91637 | CCF50-2-750ROJ |
| A31R124 | 313-1751-00 |  |  | RES,FXD,FILM: 750 OHM,5\%,0.2W | 91637 | CCF50-2-750ROJ |
| A31R125 | 322-3145-00 |  |  | RES,FXD,FILM:316 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CCF50G316ROF |
| A31R126 | 322-3193-00 |  |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A31R127 | 322-3145-00 |  |  | RES,FXD,FILM:316 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CCF50G316ROF |
| A31R128 | 322-3193-00 |  |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A31R129 | 322-3175-0 |  |  | RES,FXD,FILM: 649 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF50G649ROF |
| A31U111 | 156-3293-0 |  |  | IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY | 24355 | MAT04-006P |
| A31U118 | 156-1272- |  |  | IC,LINEAR:BIPOLAR,OP-AMP:DUAL,HIGH OUTPUT | 01295 | NE5532P |
| A31U125 | 156-3293-00 |  |  | IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY | 24355 | MAT04-006P |


| Component Number | Toktronix Part No. | Serial <br> Effective | No. Dscont | Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A32 | 671-0367-00 |  |  | CIRCUIT BD ASSY:CCD OUT | 80009 | 671036700 |
| A32C114 | 281-0798-00 |  |  | CAP,FXD.CER DI:51PF,1\%,100V | TK1743 | CGB510GEN |
| A32C115 | 281-0909-00 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A32C116 | 281-0909-0 |  |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A32C121 | 281-0798-00 |  |  | CAP,FXD,CER DI:51PF,1\%,100V | TK1743 | CGB510GEN |
| A30,115 | 131-4553-0 | B010100 | B012361 | CONN,HDR::PCB;;MALE,RTANG, $1 \times 5,0.1$ CTR (QUANTITY OF 4) | 53387 | 2405-5112TB |
| A30,315 | 131-4554-0 | B010100 | B012361 | CONN,HDR:PCB,;MALE,RTANG,1 X8,0.1 CTR (QUANTITY OF 4) | 53387 | 2408-5112TB |
| A30,115 | 131-0608-00 | B012362 |  | TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR (QUANTITY OF 13) <br> (STANDARD ONLY) | 22526 | 48283-018 |
| A30,115 | 131-4553-0 | $B 010100$ | B010106 | CONN,HDR::PCB;;MALE,RTANG,1 X 5,0.1 CTR (QUANTITY OF 4) | 53387 | 2405-5112TB |
| A30J115 | 131-4554-00 | B010100 | B010106 | CONN,HDR:PCB,;MALE,RTANG, $1 \times 8,0.1$ CTR (QUANTITY OF 4) | 53387 | 2408-5112TB |
| A30,115 | 131-0608-00 | B010107 |  | TERMINAL,PIN:PRESSFIT/PCB;;MALE,STR (QUANTITY OF 13) (2440M ONLY) | 22526 | 48283-018 |
| A32Q111 | 151-0341-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;45V,50MA,40MHZ | 04713 | MPS6520 |
| A32Q112 | 151-0341-0 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN:45V,50MA,40MHZ | 04713 | MPS6520 |
| A32Q128 | 151-0341-0 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;45V,50MA,40MHZ | 04713 | MPS6520 |
| A32Q129 | 151-0341-00 |  |  | TRANSISTOR,SIG:BIPOLAR,NPN;45V,50MA,40MHZ | 04713 | MPS6520 |
| A32R111 | 322-3193-00 |  |  | RES,FXD:METAL FILM;1K OHM,1\%,0.2W | 91637 | CCF501G10000F |
| A32R112 | 322-3175-00 |  |  | RES,FXD,FILM: 649 OHM,1\%,0.2W,TC=T0 | 91637 | CCF50G649ROF |
| A32R113 | 322-3145-00 |  |  | RES,FXD,FILM:316 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CCF50G316R0F |
| A32R114 | 322-3145-00 |  |  | RES,FXD,FILM:316 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ T0 | 91637 | CCF50G316ROF |
| A32R115 | 322-3193-00 |  |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A32R116 | 322-3193-00 |  |  | RES,FXD:METAL FILM; 1 K OHM,1\%,0.2W | 91637 | CCF501G10000F |
| A32R117 | 313-1821-00 |  |  | RES,FXD,FILM:820 OHM,5\%,0.2W | 91637 | CCF50-2-820ROS |
| A32R118 | 313-1100-00 |  |  | RES,FXD,FILM:10 OHM, 5\%,0.2W | 91637 | CCF50-2-10ROO |
| A32R120 | 322-3193-00 |  |  | RES,FXD:METAL FILM;1K OHM,1\%,0.2W | 91637 | CCF501G10000F |
| A32R121 | 313-1821-00 |  |  | RES,FXD,FILM:820 OHM,5\%,0.2W | 91637 | CCF50-2-820ROJ |
| A32R122 | 313-1100-00 |  |  | RES,FXD,FILM:10 OHM,5\%,0.2W | 91637 | CCF50-2-10ROOJ |
| A32R123 | 313-1751-00 |  |  | RES,FXD,FLLM:750 OHM,5\%,0.2W | 91637 | CCF50-2-750ROJ |
| A32R124 | 313-1751-00 |  |  | RES,FXD,FILM: 750 OHM,5\%,0.2W | 91637 | CCF50-2-750ROJ |
| A32R125 | 322-3145-0 |  |  | RES,FXD,FILM:316 OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50G316ROF |
| A32R126 | 322-3193-00 |  |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A32R127 | 322-3145-00 |  |  | RES,FXD,FILM:316 OHM, $1 \%, 0.2$ W,TC=To | 91637 | CCF50G316ROF |
| A32R128 | 322-3193-00 |  |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A32R129 | 322-3175-00 |  |  | RES,FXD,FILM: 649 OHM,1\%,0.2W,TC = T | 91637 | CCF50G649ROF |
| A32U111 | 156-3293-00 |  |  | IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY | 24355 | MAT04-006P |
| A32U118 | 156-1272-00 |  |  | IC,LINEAR:BIPOLAR,OP-AMP | 01295 | NE5532P |
| A32U125 | 156-3293-00 |  |  | IC.LINEAR:BIPOLAR,TRANSISTOR ARRAY | 24355 | MAT04-006P |


| Component Number | Toktronix <br> Part No. | Serial No. Effective Dscont | Name \& Description | Mr. Code | Mr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A33 | 671-0367-0 |  | CIRCUIT BD ASSY:CCD OUT | 80009 | 671036700 |
| A33C114 | 281-0798-00 |  | CAP,FXD,CER DI:51PF,1\%,100V | TK1743 | CGB510GEN |
| A33C115 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A33C116 | 281-0909-00 |  | CAP,FXD,CERAMIC:MLC;0.022UF,20\%,50V | 04222 | SA105C223MAA |
| A33C121 | 281-0798-00 |  | CAP,FXD,CER DI:51PF,1\%,100V | TK1743 | CGB510GEN |
| A33/115 | 131-4553-00 |  | CONN,HDR::PCB,;MALE,RTANG,1 X 5,0,1 CTR (QUANTITY OF 4) | 53387 | 2405-5112TB |
| A33/115 | 131-4554-0 |  | CONN,HDR:PCB; $;$ MALE,RTANG, $1 \times 8,0.1$ CTR (QUANTITY OF 4) | 53387 | 2408-5112TB |
| A33Q111 | 151-0341-0 |  | TRANSISTOR,SIG:BIPOLAR,NPN:45V,50MA,40MHZ | 04713 | MPS6520 |
| A33Q112 | 151-0341-0 |  | TRANSISTOR,SIG:BIPOLAR,NPN;45V,50MA,40MHZ | 04713 | MPS6520 |
| A33Q128 | 151-0341-0 |  | TRANSISTOR,SIG:BIPOLAR,NPN;45V,50MA,40MHZ | 04713 | MPS6520 |
| A33Q129 | 151-0341-0 |  | TRANSISTOR,SIG:BIPOLAR,NPN;45V,50MA,40MHZ | 04713 | MPS6520 |
| A33R111 | 322-3193-0 |  | RES,FXD:METAL FILM:1K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A33R112 | 322-3175-0 |  | RES,FXD,FILM: 649 OHM, $1 \%, 0.2 W, T C=$ T0 | 91637 | CCF50G649ROF |
| A33R113 | 322-3145-0 |  | RES,FXD,FILM: 316 OHM, $1 \%, 0.2$ W,TC=TO | 91637 | CCF50G316ROF |
| A33R114 | 322-3145-0 |  | RES,FXD,FILM:316 OHM, 1\%,0.2W,TC=TO | 91637 | CCF50G316ROF |
| A33R115 | 322-3193-00 |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A33R116 | 322-3193-00 |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A33R117 | 313-1821-00 |  | RES,FXD,FILM:820 OHM,5\%,0.2W | 91637 | CCF50-2-820ROJ |
| АЗ3R118 | 313-1100-00 |  | RES,FXD,FILM: 10 OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10ROOJ |
| A33R120 | 322-3193-00 |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| A33R121 | 313-1821-00 |  | RES,FXD,FILM:820 OHM,5\%,0.2W | 91637 | CCF50-2-820ROJ |
| A33R122 | 313-1100-00 |  | RES,FXD,FILM:10 OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-10ROOJ |
| A33R123 | 313-1751-00 |  | RES,FXD,FILM: 750 OHM,5\%,0.2W | 91637 | CCF50-2-750ROJ |
| A33R124 | 313-1751-- |  | RES,FXD,FILM:750 OHM, $5 \%, 0.2 \mathrm{~W}$ | 91637 | CCF50-2-750ROS |
| A33R125 | 322-3145-0 |  | RES,FXD,FILM:316 OHM, $1 \%, 0.2 \mathrm{~W}, \mathrm{TC}=$ TO | 91637 | CCF50G316ROF |
| A33R126 | 322-3193- 0 |  | RES,FXD:METAL FILM; 1 K OHM, $1 \%, 0.2 \mathrm{~W}$ | 91637 | CCF501G10000F |
| А33R127 | 322-3145-0 |  | RES,FXD,FILM:316 OHM, $1 \%, 0.2 W, T C=$ TO | 91637 | CCF50G316ROF |
| A33R128 | 322-3193-0 |  | RES,FXD:METAL FILM:1K OHM, 1\%,0.2W | 91637 | CCF501G10000F |
| A33R129 | 322-3175- |  | RES,FXD,FILM: 649 OHM, $1 \%, 0.2 W, T C=$ TO | 91637 | CCF50G649ROF |
| A33U111 | 156-3293-00 |  | IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY | 24355 | MAT04-006P |
| Аз3U118 | 156-1272-0 |  | IC,LINEAR:BIPOLAR,OP-AMP;DUAL,HIGH OUTPUT | 01295 | NE5532P |
| АЗ3U125 | 156-3293-00 |  | IC,LINEAR:BIPOLAR,TRANSISTOR ARRAY | 24355 | MAT04-006P |


| Component Number | Tektronix <br> Part No. | Serial No. Effective Dscont | Name \& Description | Mtr. Code | Mrt. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| B1000 | 119-1770-01 |  | FAN,TUBEAXIAL:12V, 1.72 W,42 CFM W/CONN | S4246 | CUDC12D4 |
| F1000 | 159-0014-00 |  | FUSE,CARTRIDGE:3AG,5A,250V,0.8SEC | 61857 | SS2-5A |
| FL1000 | 119-1306-00 |  | FILTER,RFI:6A,250V,50-400HZ | TK2515 | 619-569-6577 |
| J1900 | 131-0955-00 |  | CONN,RF JACK:BNC,;50 OHM, FEMALE,STR | TK1725 | G35152BN |
| J1901 | 131-0955-0 |  | CONN,RF JACK:BNC,;50 OHM,FEMALE,STR | TK1725 | G35152BN |
| J1902 | 131-0955-0 |  | CONN,RF JACK:BNC,;50 OHM,FEMALE,STR | TK1725 | G35152BN |
| J1903 | 131-0955-0 |  | CONN,RF JACK:BNC,;50 OHM,FEMALE,STR | TK1725 | G35152BN |
| J1904 | 131-0955-0 |  | CONN,RF JACK:BNC,;50 OHM,FEMALE,STR | TK1725 | G35152BN |
| J1905 | 131-0955-00 |  | CONN,RF JACK:BNC,;50 OHM,FEMALE,STR | TK1725 | G35152BN |
| J1906 | 131-0955-00 |  | CONN,RF JACK:BNC,;50 OHM,FEMALE,STR | TK1725 | G35152BN |
| J1907 | 175-9229-00 |  | CA ASSY,SP:RIBBON,GPIB;24,28 AWG,7.0 L | OJ7N9 | ORDER BY DESC |
| J1908 | 131-1471-00 |  | CONN,CIRC:SLDR CUP,:3 MALE, 3 FEMALE,6 POS | TK1312 | ERA.1S.306.CLL |
| J1909 | 131-0771-0 |  | CONN,CIRC::PNL,LEMO; 4 POS, 2 MALE, 2 FEMALE (OPTION 11 ONLY) | TK1312 | ERA.OS.304.CLL |
| J2000 | 131-0771-00 |  | CONN,CIRC::PNL,LEMO;4 POS,2 MALE,2 FEMALE (OPTION 11 ONLY) | TK1312 | ERA.OS.304.CLL |
| L1000 | 119-1478-01 |  | COIL,TUBE DEFL:FXD,TRACE ROTATION | TK1177 | 06244 |
| P174 | 175-9356-00 |  | CA ASSY,SP:RIBBON,;SDI,5,26 AWG,22.75 L | OJ7N9 | ORDER BY DESC |
| R1000 | 301-0474-00 |  | RES,FXD,FILM:470K OHM, $5 \%, 0.5 \mathrm{~W}$ | TK1727 | SFR30 2322-182 |
| R1077 | 311-1845-0 |  | RES,VAR,NONWW:PNL,5K OHM,0.5W | 12697 | W8355 |
| R1088 | 311-1845-0 |  | RES,VAR,NONWW:PNL,5K OHM,0.5W | 12697 | W8355 |
| R1099 | 311-1845-0 |  | RES,VAR,NONWW:PNL,5K OHM,0.5W | 12697 | W8355 |
| R1121 | 311-2248-0 |  | RES,VAR,NONWW:PNL,(2)10K OHM,20\%,0.5WLINEAR | 12697 | CM43462 |
| S1000 | 260-1967-00 |  | SWITCH,SLIDE:DPDT 5A/250V 10A/125V | 7W718 | 4021.0512 |
| St350 | 260-2202-00 |  | SWITCH,PUSH:DPDT,5A,250VAC | 31918 | 51870 |
| S1666 | 260-2173-0 |  | SW,PUSH BUTTON:MOMENTARY,5 BUTTON | 61545 | CP85-41313 |
| V1000 | 154-0850-01 |  | CRT ASSEMBLY:FINISHED | 80009 | 154085001 |

Section 9 - 2440 Service

## DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols
Graphic symbols and class design
based on ANSI Standard Y32.2-1975. Logic symbology is based on ANSI Y32. 14-1973 in
terms of positive logic. Logic symbols depict the tunction performed and may differ from the manutac-
turer's data.
The overine on a signal name indicates that the signal
performs it intitended function when it is in the low state.
Abbreviations are based on ANSI Y1.1-1972.
Other ANSI standards that are used in the preparation
of diagrams by Tektronix, Inc. are:

—— The information and special symbols below may appear in this manual. -

## Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an
assembly number (e.9, A20). The assembly number
 titie for the circuit board component location ill sustration,
and in the lookup table for the schematic diagram and
corressond

 in numerical sequence: the components ares isted by
comonent nember isee following illostration to
constructing a compenent number).

## COLOR CODE


(1)(2) and (3) -15 t, 2nd, and 3 rd significant figures
(1) -multipier © -tilerance








## TEST WAVEFORMS

Test waveforms for schematic diagrams (if applicable) precede the schematic. They are intended to aid in troubleshooting the instrument. Special conditions required of the test oscilloscope are given above the waveform; special conditions for the $\mathbf{2 4 4 0}$ under test are given beneath the waveform. Unless otherwise stated, the test conditions for the first waveform listed pertain to all the waveforms for a given schematic diagram. Normal control settings for the test oscilloscope are given in the readouts shown in each waveform illustration.

RECOMMENDED TEST EQUIPMENT

| Item | Specification | Example |
| :---: | :---: | :---: |
| Test oscilloscope with 10X probe and 1 X probe ( 1 X probe is optional accessory.) | Digital Storage; frequency response: dc to 40 MHz single event bandwidth to 150 MHz equivalent-time sampling. | TEKTRONIX 2440 Digital Oscilloscope with two 10X probes. |
| Calibration Generator | Standard-amplitude signal levels: 5 mV to 50 V . Accuracy $\pm 3 \%$. | TEKTRONIX PG 506 Calibration Generator. ${ }^{\text {a }}$ |
| Digital Voltmeter (DMM) | Range 0 to 140 V . Dc voltage accuracy: $\pm 0.15 \% .41 / 2$ digit display. | TEKTRONIX DM 501A Digital Multimeter. ${ }^{\text {a }}$ |
| High Voltage Probe for DMM | Maximum voltage $\mathbf{2 0} \mathrm{kV}$. | Fluke Model 80K-40 High Voltage Probe. |
| Precision Coaxial Cable | Impedance: 50 ohm. Length: 36 in . Connectors: BNC. | Tektronix Part Number 012-0482-00. |
| Dual-Input Coupler | Connectors: BNC female-to-dual-BNC male. | Tektronix Part Number 103-0090-00. |
| Sync and Linearity Test Generator | Conforms to TV System requirements. | TEKTRONIX R147A NTSC Test Signal Generator. <br> TEKTRONIX R148 Insertion Test Signal Generator. |
| Coaxial Cable (2 required) | Impedance: 75 ohm. Length: 42 in. Connectors: BNC. | Tektronix Part Number 012-0074-00. |

${ }^{\text {a }}$ TM 500-Series Power-Module Maintrame required.

## DC VOLTAGE MEASUREMENTS

Dc voltages indicated on the schematic diagrams are typical of a normally operating instrument. Voltages are with respect to chassis ground except in the isolated portion of the Low Voltage Power Supply, where they are with respect to the REF NODE indicated by the darker line in the Control Power Supply circuitry.

OTHER PARTS

| CIRCUIT nUMBER | SCHEM nUMBER | SCHEM LOCATION | CIACUIT NUMBER | SCHEM NUMBER | SCHEM LOCATION | CIRCUIT NUMBER | SCHEM NUMBER | SCHEM LOCATION | CIRCUIT NUMBER | SCHEM NUMBER | SCHEM LOCATION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| C1005 | 8 | 16 | P105 | 19 | 1 C | P124 | 2 | 7M | P148 | 18 | 4 M |
| F1000 | 22 | 2 A | P105 | 19 | 8 C | P125 | 20 | 1 L | P148 | 18 | 6M |
| FL1000 | 22 | 1 A | P105 | 6 | 4 N | P125 | 20 | 4 H | P150 | 3 | 1 N |
| J30 | 22 | 2 A | P106 | 8 | 3 G | ${ }^{\text {P128 }}$ | 1 | 5 D | P150 | 3 | ${ }^{2}$ |
| J60 | 22 | 2 A | P107 | 14 | 5 N | $\mathrm{P}^{127}$ | 2 | ${ }^{2 A}$ | P150 | 3 | 8A |
| J70 | 22 | 4 A | P108 | 19 | 18 | ${ }^{\text {P128 }}$ | 2 | 6A | P150 | 3 | 8N |
| J80 | 22 | 5A | P108 | 6 | ${ }^{31}$ | P131 | 16 | ${ }^{1 /}$ | P150 | 3 | 7A |
| $J 1900$ | 11 | 7 K | P111 | 10 | 7 F | P131 | 16 | 7A | P152 | ${ }^{6}$ | 1 J |
| 31901 | 11 | 6K | P111 | 10 | 8 D | P131 | 17 | 1 J | P152 | 8 | 2 |
| $J 1902$ | 9 | 6 N | P111 | 11 | 6A | P131 | 17 | 4K | P152 | 6 | 2 M |
| $J 1803$ | 20 | 1M | P111 | 11 | 7 J | P131 | 18 | 3 M | P162 | 19 | 7A |
| J1904 | 20 | 2M | P111 | 12 | ${ }^{2 \mathrm{M}}$ | P131 | 18 | 5A | P168 | 23 | 1 M |
| $J 1805$ | 20 | ${ }^{2 M}$ | P111 | 13 | 7E | P131 | 18 | 8 M | $\mathrm{P}^{186}$ | 23 | 2 M |
| J1906 | 20 | 3 N | P111 | 14 | 8 G | P131 | 8 | 1E | P166 | 23 | 4M |
| J1907 | 20 | 2 C | P111 | 6 | 8 M | P131 | 8 | 1 M | P186 | 23 | 5M |
| J1808 | 20 | 4 G | P111 | 9 | 5 F | P131 | 8 | 6M | P166 | 23 | BM |
| $J 1909$ | 20 | 4 M | P113 | 11 | 7E | P131 | 8 | 7 F | P172 | 19 | 2M |
| J2000 | 20 | 5M | P113 | 11 | 8 A | P131 | ${ }^{8}$ | 7 | P173 | 19 | 2 C |
| J2004 | 9 | 7A | P113 | 9 | 3 H | P141 | 10 | 2 F | P174 | 19 | 19 |
| J2002 | 9 | 7 A | P113 | ${ }^{9}$ | ${ }^{3 N}$ | P141 | 11 | 1A | P174 | 19 | 29 |
| J2004 | 9 | 1 c | P114 | 11 | 8 | P141 | 11 | 5K | P174 | 19 | 2 M |
| J2005 | 9 | 6 C | P114 | $\theta$ | 6N | P141 | 11 | 6E | P174 | 19 | 4M |
| L1000 | 19 | 1K | P117 | 15 | 3A | P141 | 11 | 6, | P178 | 19 | 8A |
| P100 | 17 | 4A | P120 | 1 | 1K | P141 | 11 | 6M | P181 | 20 | 2 F |
| P100 | 18 | 3A | P120 | 1 | 2 M | P141 | 11 | 7A | P207 | 20 | 8L |
| P100 | 7 | 2 N | P120 | 1 | 4 E | P141 | 14 | 20 | P513 | 7 | 1 B |
| P100 | 7 | 7E | P120 | 1 | 6K | P141 | 14 | 2 H | P1121 | 8 | 6F |
| P100 | 8 | 6F | P120 | 1 | 8A | P141 | 14 | 3 B | R1000 | 22 | 2 A |
| P102 | 22 | 1 D | P120 | 1 | 8M | P141 | 14 | 4 G | R1005 | - | 1 G |
| P102 | 23 | 1 M | P120 | 20 | 45 | P141 | 14 | ${ }^{6 C}$ | R1077 | 19 | 1A |
| P102 | 23 | 3M | P120 | 20 | 5A | P141 | 14 | 8 H | R1088 | 19 | 3A |
| P102 | ${ }^{23}$ | 4 E | P120 | 21 | 8 B | P141 | 14 | 78 | R1089 | 19 | 2 A |
| P102 | 23 | 4M | P121 | 17 | 1A | P141 | 14 | 8 B | R1121A | 6 | 4 |
| P102 | 23 | 5M | P121 | 18 | 2 A | P141 | 19 | 8 B | R1121B | 6 | 3 |
| P103 | 1 | 4A | P121 | 8 | 10 | P141 | 5 | 1 A | 51000 | 22 | 4A |
| P103 | 1 | 5A | P121 | 8 | 3A | P141 | 5 | 3M | 51020 | 22 | 3 c |
| P103 | 1 | 9A | P121 | 8 | BA | P141 | 6 | 5A | S1350 | 22 | 1 A |
| P103 | 20 | 2A | P123 | 21 | 3A | P141 | 6 | 6G | 51666 | 6 | 2 H |
| P103 | 2 | 1A | ${ }^{\text {P123 }}$ | 21 | 6 G | P146 | 9 | 1 F | V1000 | 19 | 1K |
| P103 | 2 | 2 A | P123 | 21 | 7 N | P147 | 9 | 6 F |  |  |  |
| P104 | 6 | 1 J | P124 | 2 | 6 F | P148 | 18 | 2M |  |  |  |

WAVEFORMS FOR DIAGRAM 1
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AT POWER ON

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SYSTEM PROCESSOR 〈 $\downarrow$


| ASSEMBLY A12 |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Breo |  | ${ }^{84}$ |  |  |  |  |  |  |  |  |  |
|  | ${ }_{6}^{2}$ | ${ }^{\text {®i }}$ | （osem |  |  |  | coic | ${ }_{\substack{\text { ge } \\ \text { gr }}}^{\text {ef }}$ | Unem | $\underset{\substack{n \\ 0}}{\substack{n}}$ |  |
|  | ${ }_{8}^{56}$ | ${ }_{\text {of }}$ | 0 | ${ }_{24}^{206}$ |  | $\underbrace{}_{\substack{\text { nase } \\ \text { neas }}}$ | $\substack{\begin{subarray}{c}{20 \\ x,} }} \\ {x,} \end{subarray}$ | ${ }^{6}$ | Usama | $\begin{aligned} & \substack{80 \\ 40 \\ 4 \\ \hline 0} \end{aligned}$ | \％ |
|  | $\underset{\substack{20 \\ 24}}{\substack{20}}$ | ${ }_{\substack{8 \%}}^{80}$ |  |  | ${ }_{0}^{\circ}$ | nes8 | ${ }_{24}^{24}$ | ${ }_{\infty}^{\infty}$ | Usatic | $\underset{\substack{\begin{subarray}{c}{c \\ r} }} \\ {\hline}\end{subarray}}{ }$ | （er |
| caror | ${ }^{\text {m }}$ | ${ }^{\text {Ta }}$ |  | $\underset{\infty}{\text { cos}}$ |  | meao |  | ${ }^{8 \%}$ | Uues |  | ${ }_{\substack{80 \\ 80}}^{\text {ef }}$ |
|  |  | \％an |  | $\substack{\begin{subarray}{c}{s i c \\ \text { sen }} }} \\ {\hline} \end{subarray}$ | come | Unem |  | $\underbrace{\substack{\text { cic }}}_{\substack{36 \\ 36}}$ | Uesers | $\begin{gathered} { }_{\substack{46 \\ b 5}} \end{gathered}$ | 运 |
|  | ${ }_{\text {if }}^{\text {if }}$ | ¢ |  | ¢ | $\underset{\substack { \text { \％} \\ \begin{subarray}{c}{\text { \％}{ \text { \％} \\ \begin{subarray} { c } { \text { \％} } }\end{subarray}}{\substack{\text { a }}}$ |  | $\begin{gathered} \substack{\text { ack } \\ \text { son }} \end{gathered}$ |  | Usese | $\begin{gathered} { }_{\substack{40 \\ 341}} \end{gathered}$ | 䢔 |
| crase | ${ }_{24}$ | ${ }_{0}^{6}$ |  | $\underset{\substack{i n \\ 20}}{\substack{0}}$ | $\underset{\substack{\pi \ldots \\ \pi}}{\substack{1}}$ | Usisea |  | ¢ | Useso | $\begin{gathered} 30 \\ \substack{s \\ b y} \end{gathered}$ |  |
| ${ }_{\text {jos }}$ | ${ }_{\text {a }}^{4}$ | ${ }^{2}$ |  | $\stackrel{\substack{2 H \\ i H}}{4 .}$ | ${ }^{7 A}$ | Sose | $\begin{gathered} { }_{c}^{78} \\ 80 \\ 80 \end{gathered}$ | ${ }_{\substack{\text { SE }}}^{\substack{8, 88}}$ | Cumo | $\substack{\begin{subarray}{c}{\text { s.0. } \\ \text { ge }} }} \end{subarray}$ |  |
| （jas | 就 | 发 |  | ${ }_{\substack{19 \\ 10 \\ 10}}$ | ${ }_{\substack{88 \\ 88}}^{88}$ | Uose | coic | 8 | Cusee | $\begin{gathered} \text { gin } \\ \substack{80} \end{gathered}$ |  |
| （1200 | ${ }_{\substack{2 m \\ \hline ⿷ 匚 ⿳ 亠 丷 厂 犬}}^{2 m}$ | ${ }_{\text {\％}}$ |  | $\begin{aligned} & \text { aid } \\ & \text { an } \end{aligned}$ | 80 | U0080 | $\begin{gathered} \text { and } \\ 20 \\ 20 \end{gathered}$ |  | cise |  | ${ }_{\text {ax }}$ |
| ， | ${ }^{\text {ax }}$ | ${ }^{\circ 8}$ |  | $\begin{aligned} & { }_{80}^{a} \\ & { }_{80} \end{aligned}$ |  | Usero |  |  | Useas |  |  |
|  |  |  |  | ${ }_{\text {oin }}^{\text {eig }}$ | ${ }_{\text {com }}^{\substack{0 \\ 80}}$ | $\begin{gathered} \text { ueice } \\ \text { Uuse } \\ \text { Uose } \end{gathered}$ |  | ${ }_{\text {ox }}$ |  | ${ }^{\text {®08 }}$ |  |
| Jjas | ${ }_{\substack{\text { ser } \\ \text { en }}}$ | ${ }_{\pi}^{8 F}$ |  | ${ }_{5 A}^{5 A}$ |  | Uneon | ， | ${ }^{\circ}$ | Uasab | ${ }_{\text {cis }}^{68}$ | ${ }_{\substack{\text { ef } \\ \text { ef } \\ \text { ef }}}$ |
|  |  |  |  |  |  |  |  |  |  |  |  |
| OTHER Parts |  |  |  |  |  |  |  |  |  |  |  |
|  |  | $\begin{gathered} \substack{\text { chassessess } \\ \text { OhAlsssis }} \end{gathered}$ | $\begin{gathered} \substack{\text { Pr } 1200 \\ P 120} \\ \hline \end{gathered}$ | $\begin{aligned} & \frac{1 k}{2 k} \\ & 2 \mu \end{aligned}$ | $\begin{array}{\|c\|c\|c\|c\|c\|c\|cccl} \substack{\text { chassiss } \\ \text { ChHssis }} \end{array}$ | $\begin{gathered} \text { prep } \\ p_{p 120}(1200 \end{gathered}$ | $\substack{\begin{subarray}{c}{\text { ond } \\ \text { en }} }} \\ {\hline} \end{subarray}$ | $\begin{array}{\|c} \substack{\text { chassess } \\ \text { chassis } \\ \text { CHAssis }} \end{array}$ | ${ }^{\text {P12a }}$ | ${ }^{50}$ | crusss |




WAVEFORMS FOR DIAGRAM 2


WAVEFORM 34 IS NOT USED

| cincema | schem | ${ }^{\text {Loasaion }}$ | cincur | Sconkow | Locaton | cincur | ${ }^{\text {coshem }}$ | boano | cincur | sochew | Learaion |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Assembly al2 |  |  |  |  |  |  |  |  |  |  |  |
|  |  | ${ }_{\substack{3 F \\ 3 F}}^{\substack{\text { and }}}$ |  | ${ }_{\substack{60}}^{80}$ | ${ }^{3 \mathrm{aK}}$ | ${ }^{\text {I23act }}$ | ${ }_{3}^{3 \times}$ | ${ }^{36}$ | ${ }^{\text {U5652}}$ |  | ${ }^{56}$ |
| ciccicicis |  | ${ }_{6}^{66}$ |  | ${ }_{\substack { 76 \\ \begin{subarray}{c}{80{ 7 6 \\ \begin{subarray} { c } { 8 0 } } \\{36}\end{subarray}}$ | $\underbrace{}_{\substack { 4 \times \\ \begin{subarray}{c}{4 \times \\ \hline 8{ 4 \times \\ \begin{subarray} { c } { 4 \times \\ \hline 8 } }\end{subarray}}$ |  | ${ }^{3 \times}$ | ${ }_{\substack{36 \\ 36}}$ |  | ${ }_{\substack{26 \\ 36}}^{\substack{\text { a }}}$ |  |
| coso | ${ }^{34}$ | ${ }^{\circ \times}$ |  |  |  | , | ${ }_{\text {10, }}^{16}$ | ${ }_{\substack{3 \% \\ 34}}^{\substack{34 \\ \hline}}$ | \% | ${ }_{\text {cosm }}^{10}$ | \% |
| ${ }^{0} 5$ | ${ }_{2 a}$ | ${ }_{\text {sk }}$ |  | ${ }_{\substack { \text { si } \\ \begin{subarray}{c}{\text { sin }{ \text { si } \\ \begin{subarray} { c } { \text { sin } } }\end{subarray}}$ |  |  | cocco | - |  | ¢ | ¢ |
| л193 | ${ }^{\text {a }}$ | a |  |  | ${ }_{4}^{4 \times 1}$ |  | $\underbrace{88}_{\substack{38 \\ 88}}$ | 3 |  |  |  |
| ${ }_{\substack{\text { Ju2 } \\ \hline 124}}$ | ${ }_{\substack{28 \\ 88}}^{29}$ | ${ }^{\text {ar }}$ |  | ${ }_{\substack{\text { n }}}^{\substack{\text { a }}}$ |  |  | ${ }_{\text {gex }}^{\substack{\text { ge }}}$ | ${ }_{3}^{3}$ | $\xrightarrow{\text { U5sec }}$ |  | ${ }_{\substack{\text { st } \\ \text { st } \\ \hline}}$ |
| , 122 |  |  | ${ }_{\text {traro }}$ | $50$ | ${ }^{3}$ |  | ${ }_{\substack{28 \\ 18}}^{4}$ | ¢ | Usean | $\underset{\substack{3 \mathrm{sk} \\ \text { 3k }}}{ }$ |  |
| Jus | ${ }_{\text {ct }}^{68}$ |  |  | ${ }_{\substack{s c \\ 96}}$ | 3 3 | $\pm$ | $\underbrace{\substack{\text { gi }}}_{\text {sig }}$ | ${ }_{\substack{36 \\ 36}}$ |  | ${ }_{3}^{18}$ | ${ }_{8}^{86}$ |
| ${ }^{2} 24$ | ${ }_{56}$ | ${ }^{35}$ | $\underbrace{}_{\substack{\text { crear } \\ \text { Tr37 }}}$ | ${ }_{\substack{\mathrm{sc} \\ \mathrm{cc} \\ 0}}$ | ${ }_{\substack{3 \\ 3 \\ 3}}$ | (1328 | ${ }_{30}^{4 \times}$ | ${ }_{\substack{40 \\ 4 \\ 4 \\ 0}}$ | Usese | ${ }_{\substack{18 \\ 20}}$ | \% |
| ${ }^{032}$ | ${ }^{66}$ | ${ }^{35}$ |  | $\underbrace{2 H}_{4}$ |  | U3068 | ${ }_{10}^{16}$ | $\stackrel{4}{4}$ | Usaran | $\substack{2 \mathrm{c} \\ 4 \times}_{\substack{\text { ck }}}$ | ${ }_{\substack{\text { ake } \\ \text { ok }}}$ |
|  |  |  |  | ${ }_{\substack{40 \\ 10}}$ | $\underset{\substack{\text { sk } \\ \text { sk }}}{\text { ck }}$ | Uas3a | ${ }_{\text {sid }}^{50}$ |  | Usara | ${ }_{3}^{3 \times}$ | ${ }_{\text {ox }}^{\text {ok }}$ |
|  |  | $\underbrace{\substack{3}}_{\substack{3 F \\ 35}}$ | 20 |  | ${ }^{\text {8f }}$ |  |  | cick | ${ }_{\substack{\text { wise } \\ \text { wiso }}}^{\text {a }}$ | ${ }_{\substack{20 \\ 80}}^{20}$ | * |
|  | ${ }_{\substack{\text { be } \\ 86 \\ 86}}$ | ${ }_{\substack{3 F \\ 35}}$ | cill |  | ${ }_{\substack{\text { k } \\ \text { k } \\ \text { \% }}}$ | Unem |  |  | $\underbrace{\text { N10 }}_{\substack{\text { wise } \\ \text { wiso }}}$ |  | $\underset{\text { \% }}{\substack{\text { \% } \\ 1 \\ 1}}$ |
|  | ¢ |  |  | ¢ |  |  |  | ${ }_{\substack{86 \\ 88}}^{8}$ |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| OTHER | RTS |  |  |  |  |  |  |  |  |  |  |
| ${ }_{\substack{\text { P.103 } \\ \text { pros }}}$ | ${ }_{24}^{14}$ | $\substack{\text { chasss } \\ \text { chasss }}_{\text {ctas }}$ | ${ }_{\substack{\text { prid } \\ \text { prid }}}$ | $\stackrel{\text { ¢f }}{\text { ¢ }}$ |  | ${ }_{\substack{\text { Prize } \\ \text { P127 }}}$ | ${ }_{8}^{24}$ | ${ }_{\substack{\text { chansss } \\ \text { Chasss }}}^{\text {che }}$ |  |  |  |




| A13-SIDE Board |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\underbrace{}_{\substack{\text { cimeur } \\ \text { Wuser }}}$ | sictem | cincur | Scemen | $\underbrace{}_{\substack{\text { cincur } \\ \text { Numer }}}$ | Stemem |  | Schem |
|  |  |  |  |  |  |  |  |


front panel processor <3


| ASSEMBLY A 13 |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\underbrace{\text { a }}_{\substack{\text { crove } \\ \text { crov }}}$ | ${ }_{28}^{48}$ |  | $\underset{\substack{\text { femo } \\ \text { neme }}}{ }$ | ${ }_{7}^{7 \mathrm{~m}}$ |  |  | ${ }^{48}$ |  | ${ }_{\text {U }}^{5}$ |  |  |
|  | $\stackrel{\text { ab }}{\text { a }}$ | ${ }_{3}^{39}$ |  | ${ }_{\substack{\text { am } \\ \text { gr } \\ \hline 8 \\ \hline 1}}$ | ${ }_{3}^{3 A}$ | ${ }_{\substack{\text { pron } \\ \text { Troo }}}$ | $\begin{gathered} 28 \\ 28 \\ 28 \end{gathered}$ | ${ }_{3}^{38}$ | ${ }_{\substack{\text { und }}}^{\text {Urse }}$ |  | ${ }_{2}^{24}$ |
|  | $\stackrel{\pi}{\pi}$ | $\begin{aligned} & 36 \\ & 36 \\ & 30 \end{aligned}$ |  | $\begin{gathered} i k \\ \substack{i k\\ } \end{gathered}$ | $\begin{aligned} & 3 A \\ & 2 A \\ & 2 A \\ & 2 A \end{aligned}$ |  | $\frac{18}{18}$ | $\begin{aligned} & 20 \\ & x \\ & x \end{aligned}$ |  |  | a3 |
|  | $\begin{gathered} \stackrel{\otimes}{8} \\ \text { im } \end{gathered}$ | $\begin{aligned} & 36 \\ & 2 n \\ & 2 n \end{aligned}$ |  | $\begin{gathered} \pi \\ n \\ n \end{gathered}$ | $\begin{aligned} & \text { en } \\ & 2 \pi \\ & 2 \pi \end{aligned}$ |  | $\begin{gathered} 36 \\ \substack{36 \\ 38} \\ \hline \end{gathered}$ | $\begin{aligned} & x_{2}^{2} \\ & \substack{c \\ x} \end{aligned}$ |  | $\begin{gathered} \substack{\text { Bek } \\ \text { ge }} \\ \hline \end{gathered}$ | $3_{3}^{2}$ |
| cinco | $\substack{\begin{subarray}{c}{\text { mox } \\ \text { ex }} }} \end{subarray}$ | $\begin{gathered} 2 a \\ \substack{2 a \\ 2 A} \end{gathered}$ | cincoin | $\begin{gathered} n \\ \substack{n \\ 0} \end{gathered}$ | $\begin{gathered} 2 \pi \\ 30 \\ 30 \end{gathered}$ |  | $\begin{gathered} 36 \\ 28 \\ 28 \end{gathered}$ | $\begin{aligned} & 20 \\ & 20 \\ & 20 \end{aligned}$ | woor | ${ }^{1 A}$ | ${ }^{26}$ |
| (juso | $\begin{gathered} \substack{\text { sum } \\ 4 \\ 4} \\ \hline \end{gathered}$ | $\begin{gathered} 2 R \\ \substack{2 a \\ 28} \\ 28 \end{gathered}$ |  |  | $\begin{gathered} 30 \\ \substack{30 \\ 3 \\ \hline} \end{gathered}$ |  | $\begin{gathered} 28 \\ \substack{28 \\ 28} \\ \hline 10 \end{gathered}$ |  |  | $\begin{gathered} \text { eac } \\ \substack{00 \\ x,} \end{gathered}$ | (en $\begin{gathered}20 \\ 30 \\ 30\end{gathered}$ |
|  | $\begin{aligned} & 4 \\ & 5 \end{aligned}$ | ${ }^{28}$ |  | $\begin{aligned} & \text { iH } \\ & i \\ & a \\ & i \end{aligned}$ | $\begin{gathered} \substack{38 \\ 28 \\ 28} \\ \hline \end{gathered}$ |  | $\begin{gathered} 28 \\ \substack{28 \\ 28 \\ 28} \end{gathered}$ |  |  | $\begin{gathered} x \\ \substack{x a \\ i A} \\ \hline \end{gathered}$ | , |
|  |  | $\begin{aligned} & 2 a \\ & 2 a \\ & 2 a \end{aligned}$ |  | $\begin{aligned} & \text { ab } \\ & \text { at } \end{aligned}$ | $\begin{gathered} 28 \\ 28 \\ 28 \end{gathered}$ | $\begin{gathered} \text { P} \\ \hline \\ \hline \end{gathered}$ | $\begin{gathered} \substack{80 \\ x \\ x} \\ \hline 0.0 \end{gathered}$ | $\begin{aligned} & \text { cot } \\ & \substack{\text { co }} \end{aligned}$ |  | $\substack{\begin{subarray}{c}{\text { sit } \\ \text { sit }} }} \\ {\hline} \end{subarray}$ | , |
| $\underbrace{\text { end }}_{\substack{\text { Rapes } \\ \text { neox }}}$ | $\underset{\substack{7 \times \\ 7}}{\substack{\text { m }}}$ | ${ }_{3}^{3 A}$ |  | ${ }_{\text {明 }}^{\sim}$ | 30 | Unoe | ${ }_{\text {sk }}$ | ${ }_{28}$ |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |


Waverorms for diagram 3



| A14-Front panel board |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Cincur | Scilem | cincer | Scemem |  | Sctem | $\underbrace{\substack{\text { creur } \\ \text { Numer }}}_{\text {cher }}$ | Seltem | $\underbrace{}_{\substack{\text { cifeur } \\ \text { memed }}}$ | Sctem | cincur | Sctem |
|  | 4 | ${ }^{\text {capar }}$ | 4 |  |  |  |  |  |  |  |  |
| coss | $\stackrel{4}{4}$ | $\underbrace{}_{\substack{\text { caras } \\ \text { cama }}}$ | $\stackrel{4}{4}$ | $\underset{\substack{\text { chass } \\ \text { Cons } \\ \hline}}{ }$ | ${ }_{4}^{4}$ |  |  | $\underset{\substack{\text { sixat } \\ \text { sex }}}{\substack{0 \\ \hline}}$ |  |  |  |
| ${ }_{\text {cose }}$ | 4 |  | ${ }_{4}^{4}$ |  | 4 |  | 4 | coss |  |  | 4 |
| $\underbrace{}_{\substack{\text { craon } \\ \text { canaz }}}$ | ${ }_{4}^{4}$ |  | ${ }_{4}^{4}$ | $\underbrace{}_{\substack{\text { crasis } \\ \text { crase } \\ \text { case }}}$ | 4 | cin | ${ }_{4}^{4}$ | (inctit | 4 |  | 4 |
| ctiche | 4 |  | ${ }_{4}^{4}$ | $\underbrace{}_{\substack{\text { crabi } \\ \text { crabe } \\ \text { chase }}}$ | ${ }_{4}^{4}$ |  | 4 | cis | 4 |  | ${ }_{4}^{4}$ |
|  | 4 | cincien | $\stackrel{4}{4}$ | crase | 4 |  | ${ }_{4}^{4}$ | ¢ | 4 | ciss | ${ }_{4}^{4}$ |
|  | 4 | coicce | $\stackrel{4}{4}$ |  | ${ }_{4}^{4}$ |  | ${ }_{4}^{4}$ | cis | ${ }_{4}^{4}$ |  | ${ }_{4}^{4}$ |
|  | ${ }_{4}^{4}$ |  | ${ }_{4}^{4}$ |  | ${ }_{4}^{4}$ |  | ${ }_{4}^{4}$ |  | 4 | sisg | , |
|  | ${ }_{4}^{4}$ |  | ${ }_{4}^{4}$ | 㐋 | 4 | nesp | ${ }_{4}^{4}$ |  | 4 |  | 4 |
|  | ${ }_{4}^{4}$ | $\underset{\substack{\text { crass } \\ \text { Crsas }}}{\substack{\text { and }}}$ | ${ }_{4}^{4}$ |  | ${ }_{4}^{4}$ |  | 4 |  | $\stackrel{4}{4}$ | w51 |  |

front panel 〈4




## A10-MAIN BOARD (cont)

| CIRCUIT <br> NUMBER | SCHEM NUMBER | CIRCUIT <br> NUMBER | SCHEM NUMBER | CIRCUIT NUMBER | SCHEM NUMBER | CIRCUIT <br> NUMBER | SCHEM <br> NUMBER | CIRCUIT NUMBER | SCHEM NUMBER | CIRCUTT NUMBER | SCHEM NUMBER |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| C263 | 10 | C581 | 10 | C826 | 6 | CR784 | 14 | Q110 | 9 | R135 | 9 |
| C264 | 10 | C581 | 14 | C830 | 6 | CR810 | 6 | Q140 | 11 | R136 | 9 |
| C265 | 10 | C582 | 14 | C832 | 6 | CR870 | 14 | Q150 | 11 | R140 | 9 |
| C272 | 11 | C590 | 12 | C834 | 6 | CR874 | 14 | Q151 | 11 | R141 | 9 |
| C280 | 11 | C591 | 12 | C835 | 6 | CR880 | 14 | Q170 | 10 | R142 | 5 |
| C281 | 11 | C600 | 9 | C840 | 6 | CR884 | 14 | Q240 | 9 | R143 | 9 |
| C282 | 12 | C601 | 6 | C843 | 6 |  |  | Q250 | 11 | R144 | 9 |
| C283 | 5 | C602 | 6 | C844 | 6 | J104 | 6 | Q251 | 11 | R145 | 11 |
| C287 | 11 | C630 | 6 | C850 | 6 | J105 | 6 | Q270 | 11 | R146 | 11 |
| C288 | 11 | C631 | 6 | C851 | 14 | J105 | 19 | Q271 | 11 | R150 | 11 |
| C290 | 12 | C632 | 6 | C870 | 14 | J106 | 6 | Q287 | 11 | R151 | 11 |
| C311 | 9 | C633 | 6 | C872 | 14 | J107 | 14 | Q288 | 11 | R160 | 11 |
| C316 | 9 | C640 | 10 | C880 | 14 | J108 | 6 | Q290 | 12 | R161 | 11 |
| C319 | 9 | C641 | 10 | C882 | 14 | J108 | 19 | Q291 | 12 | R162 | 11 |
| C320 | 9 | C642 | 6 | C950 | 5 | $J 111$ | 6 | Q356 | 10 | R163 | 11 |
| C321 | 9 | C643 | 6 | C951 | 5 | J111 | 9 | Q372 | 10 | R165 | 11 |
| C322 | 9 | C644 | 6 | C955 | 5 | 1111 | 10 | Q375 | 10 | R170 | 10 |
| C330 C340 | 10 10 | C645 C646 | 6 | C956 C 957 | 5 | 5111 <br>  <br>  <br>  <br> 111 | 11 | Q380 | 12 | R171 | 10 |
| C340 C341 | 10 10 | C646 | 6 | C957 | 5 | d111 <br>  <br>  <br> 111 | 12 | Q390 | 12 | R182 | 5 |
| C341 C350 | 10 10 | C647 | 5 | C958 C 960 | 5 | J111 | 13 | Q381 | 12 | R183 | 11 |
| C361 | 11 | C649 | 5 | C961 | 5 | J113 | 9 | Q393 | 12 | R184 | 11 |
| C367 | 10 | C650 | 5 | C965 | 5 | J113 | 11 | 0446 | 10 | R186 | 11 |
| C370 | 10 | C651 | 5 | C966 | 5 | J114 | 9 | Q450 | 10 | R188 | 11 |
| C370 | 11 | C652 | 10 |  |  | J114 | 11 | Q460 | 10 | R201 | 9 |
| C371 | 11 | C653 | 5 | CR140 | 9 | J141 | 5 | 0490 | 12 | R202 | 9 |
| C372 | 10 | C654 | 5 | CR141 | 9 | J141 | 6 | Q491 | 12 | R210 | 9 |
| C375 | 10 | C655 | 5 | CR220 | 9 | J141 | 10 | Q492 | 12 | R211 | 9 |
| C380 | 11 | C656 | 5 | CR221 | 9 | J141 | 11 | Q493 | 12 | R215 | 9 |
| C390 C391 | 12 | C660 | 5 | CR222 | 9 | J141 | 14 | 0494 | 12 | R216 | 9 |
| C391 C410 | 12 9 | C661 | 5 | CR223 | 9 | J141 | 19 | 0495 | 12 | R220 | 9 |
| C410 | 9 | C662 | 5 | CR224 | 9 | J146 | 9 | Q530 | 10 | R222 | 9 |
| $\mathrm{C412}$ | 9 | C663 | 14 | CR225 | 9 | $J 147$ | 9 | 0540 | 10 | R225 | 11 |
| C414 | 9 | C664 | 14 | CR226 | 9 | $J 152$ | 6 | Q551 | 10 | R230 | 9 |
| C420 | 9 | C685 | 14 | CR227 | 5 | $J 157$ | 11 | 0580 | 10 | R231 | 9 |
| C421 | 9 | C686 C690 | 14 | CR228 | 5 | J190 | 14 | Q620 | 9 | R232 | 10 |
| C 422 | 9 | C690 | 6 | CR270 | 11 | J191 | 14 | Q621 | 9 | R233 | 10 |
| C423 | 9 | C701 | 6 | CR285 | 11 | J192 | 14 | Q630 | 10 | R234 | 9 |
| C430 C432 | 10 9 | C711 C730 | 6 | CR286 | 11 | J2006 | 13 | 0640 | 10 | R235 | 9 |
| $C 432$ $C 440$ | 9 10 | C730 c731 | 6 | CR290 CR291 | 12 | L120 |  | 0660 | 14 | R236 | 9 |
| C441 | 10 | C732 | 6 | CR292 | 12 | L150 | 11 | 0770 | 14 | R238 | 10 |
| C456 | 9 | C733 | 6 | CR310 | 9 | 1200 | 9 | Q771 | 14 | R240 | 9 |
| C462 | 10 | C734 | 6 | CR311 | 9 | $\underline{L 210}$ | 9 | Q772 | 14 | R241 | 9 |
| C463 | 10 | C735 | 6 | CR392 | 12 | $\underline{L 20}$ | 9 | Q773 | 14 | R242 | 10 |
| C464 | 10 | C740 | 6 | CR410 | 9 | $\underline{L} 50$ | 9 | 0774 | 14 | R243 | 9 |
| C465 | 10 | C741 | 6 | CR411 | 9 | 1260 | 11 | 0775 | 14 | R244 | 10 |
| C467 | 10 | C742 | 6 | CR420 | 5 | $\underline{L 261}$ | 10 | 0780 | 14 | R245 | 10 |
| C468 | 10 | C743 | 6 | CR421 | 9 | L270 | 11 | Q781 | 14 | R250 | 11 |
| C 471 | 12 | C744 | 6 | CR490 | 12 | L332 | 10 | 0782 | 14 | R251 | 10 |
| C472 | 11 | 6745 | 6 | CR491 | 12 | L340 | 10 | Q783 | 14 | R252 | 11 |
| C473 | 11 | C746 | 6 | CR500 | 9 | L431 | 10 | 0784 | 14 | R253 | 11 |
| C474 | 10 | C747 | 6 | CR501 | 9 | 1460 | 9 | Q785 | 14 | R255 | 11 |
| C480 | 10 | C748 | 6 | CR502 | 9 | 1480 | 12 - | 0810 | 6 | R260 | 11 |
| C481 | 12 | C751 | 5 | CR503 | 9 | 5510 | 9 | Q870 | 14 | R261 | 11 |
| C483 | 12 | 6752 | 5 | CRS21 | 9 | 1520 | 9 | Q871 | 14 | R262 | 11 |
| C484 | 11 | C753 | 5 | CR530 | 5 | L521 | 9 | 0872 | 14 | R263 | 9 |
| C488 | 11 | C760 | 5 | CR551 | 10 | $L 530$ | 10 | Q873 | 14 | R265 | 10 |
| C490 | 12 | C761 | 6 | CR552 | 10 | 1531 | 10 | Q874 | 14 | R267 | 11 |
| C491 | 12 | C762 | 14 | CR553 | 10 |  |  | Q875 | 14 | R268 | 11 |
| C492 | 12 | C763 | 14 | CR5B0 | 11 | LR215 | 9 | Q880 | 14 | R269 | 5 |
| C493 | 10 | C765 | 14 | CR581 | 11 | LR220 | 9 | Q881 | 14 | R270 | 11 |
| C 500 | 9 | C768 | 14 | CR582 | 11 | LR341 | 10 | Q882 | 14 | R271 | 11 |
| C 509 | 9 | C770 | 14 | CR590 | 12 | LR342 | 10 | Q883 | 14 | R272 | 11 |
| C510 | 9 | C771 | 14 | CR591 | 12 | LR344 | 10 | Q884 | 14 | R273 | 5 |
| C511 | 9 | C774 | 14 | CR600 | 9 | LR345 | 10 | Q885 | 14 | R274 | 11 |
| C512 | 9 | C780 | 14 | CR60t | 9 | LR410 | 9 | Q970 | 14 | R275 | 11 |
| C522 | 9 | C781 | 14 | CR602 | 9 | LR421 | 9 | 0980 | 14 | R276 | 11 |
| C523 | 9 | C784 | 14 | CR610 | 9 | LR422 | 9 |  |  | R278 | 11 |
| C 524 | 9 | C809 | 6 | CR612 | 6 | LR450 | 11 | R102 | 13 | R279 | 11 |
| C530 | 9 | C810 | 6 | CR613 | 6 | LR451 | 11 | R110 | 9 | R280 | 5 |
| C 532 | 10 | C812 | 6 | CR614 | 6 | LR452 | 11 | R111 | 9 | R281 | 11 |
| C535 | 10 | $\mathrm{C813}$ | 6 | CR620 | 9 | LR453 | 11 | R112 | 9 | R282 | 11 |
| C540 | 10 | C817 | 6 | CR621 | 9 | LR454 | 11 | R120 | 9 | R283 | 12 |
| C 541 | 10 | C820 | 14 | CR622 | 9 | LR455 | 11 | R121 | 9 | R284 | 12 |
| C542 | 10 | C821 | 6 | CR701 | 5 | LR456 | 11 | R130 | 9 | R285 | 5 |
| C 550 | 10 | C822 | 6 | CR702 | 5 | LR457 | 11 | R131 | 9 | R285 | 10 |
| C561 | 14 | C823 | 6 | CR771 | 14 | LR510 | 9 | R132 | 9 | R286 | 11 |
| C562 | 10 | C824 | 6 | CR774 | 14 | LR520 | 9 | R133 | 9 | R287 | 11 |
| C563 | 14 | C825 | 6 | CR780 | 14 |  |  | R134 | 11 | R288 | 11 |


| A10-MAIN BOARD (cont) |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CIRCUIT <br> NUMBER | SCHEM NUMBER | CIRCUIT NUMBER | SCHEM NUMBER | CIRCUIT <br> NUMBER | SCHEM NUMBER | CIRCUIT NUMBER | SCHEM NUMBER | CIRCUIT <br> NUMBER | SCHEM NUMBER | CIRCUIT NUMBER | SCHEM <br> NUMBER |
| R289 | 12 | R444 | 10 | R564 | 14 | R675 | 14 | R840 | 6 | U340 | 10 |
| R290 | 5 | R445 | 10 | R565 | 6 | R676 | 14 | R841 | 6 | U350 | 10 |
| R291 | 5 | R446 | 10 | R566 | 6 | R677 | 14 | R850 | 5 | U360 | 10 |
| R292 | 12 | R447 | 10 | R570 | 11 | R678 | 14 | R851 | 5 | U370 | 11 |
| R293 | 12 | R448 | 10 | R571 | 11 | R680 | 14 | R852 | 5 | U380 | 11 |
| R294 | 5 | R449 | 10 | R572 | 11 | R681 | 14 | R853 | 5 | U381 | 11 |
| R295 | 12 | R452 | 10 | R573 | 11 | R682 | 14 | R855 | 5 | U390 | 12 |
| R296 | 12 | R453 | 10 | R574 | 11 | R683 | 14 | R856 | 5 | U420 | 9 |
| R297 | 12 | R454 | 10 | R575 | 11 | R684 | 14 | R857 | 5 | U440 | 10 |
| R298 | 12 | R455 | 10 | R580 | 11 | R685 | 14 | R860 | 5 | U450 | 10 |
| R299 | 12 | R456 | 10 | R581 | 11 | R686 | 14 | R861 | 14 | U460 | 10 |
| R320 | 9 | R461 | 10 | R584 | 11 | R687 | 14 | R863 | 14 | U470 | 11 |
| R340 | 10 | R463 | 10 | R585 | 10 | R690 | 12 | R868 | 14 | U490 | 12 |
| R341 | 10 | R464 | 9 | R586 | 10 | R700 | 6 | R871 | 14 | U510 | 9 |
| R342 | 10 | R464 | 10 | R587 | 10 | R710 | 6 | R872 | 14 | U511 | 9 |
| R343 | 10 | R466 | 10 | R588 | 10 | R726 | 6 | R873 | 14 | U520 | 6 |
| R344 | 10 | R467 | 10 | R591 | 12 | R730 | 6 | R875 | 14 | U520 | 9 |
| R345 | 10 | R468 | 10 | R592 | 12 | R731 | 6 | R879 | 14 | U530 | 5 |
| R346 | 10 | R469 | 10 | R593 | 12 | R732 | 6 | R881 | 14 | U540 | 10 |
| R347 | 10 | R470 | 10 | R594 | 12 | R734 | 6 | R882 | 14 | U560 | 14 |
| R348 | 10 | R471 | 12 | R595 | 12 | R735 | 6 | R883 | 14 | U570 | 14 |
| R349 | 10 | R477 | 12 | R596 | 12 | R736 | 6 | R884 | 14 | U580 | 10 |
| R353 | 10 | R478 | 12 | R598 | 12 | R740 | 6 | R885 | 14 | U580 | 11 |
| R354 | 10 | R479 | 11 | R599 | 12 | R741 | 6 | R891 | 14 | U590 | 12 |
| R355 | 10 | R480 | 11 | R600 | 6 | R742 | 10 | R950 | 5 | U600 | 6 |
| R356 | 10 | R481 | 11 | R601 | 6 | R743 | 10 | R951 | 5 | U610 | 6 |
| R357 | 10 | R482 | 12 | R612 | 9 | R750 | 5 | R952 | 5 | U630 | 6 |
| R358 | 10 | R483 | 12 | R613 | 9 | R751 | 5 | R953 | 5 | U631 | 6 |
| R359 | 10 | R484 | 12 | R614 | 9 | R752 | 5 | R954 | 5 | U640 | 6 |
| R361 | 11 | R485 | 12 | R615 | 6 | R753 | 5 | R955 | 5 | U641 | 5 |
| R368 | 11 | R486 | 10 | R622 | 9 | R760 | 5 | R956 | 5 | $\cup 650$ | 5 |
| R370 | 10 | R487 | 10 | R623 | 9 | R761 | 5 | R957 | 5 | U651 | 5 |
| R371 | 11 | R488 | 10 | R624 | 9 | R763 | 14 | R1001 | 9 | U660 | 5 |
| R372 | 10 | R489 | 12 | R625 | 9 | R764 | 14 | R1002 | 9 | U661 | 5 |
| R373 | 10 | R490 | 12 | R626 | 6 | R766 | 14 | R1003 | 9 | U661 | 6 |
| R374 | 10 | R491 | 12 | R627 | 6 | R771 | 14 | R1004 | 9 | U700 | 6 |
| R375 | 10 | R492 | 12 | R628 | 6 | R772 | 14 |  |  | U770 | 14 |
| R376 | 10 | R493 | 12 | R631 | 10 | R773 | 14 | \$600 | 6 | U780 | 14 |
| R377 | 10 | R494 | 12 | R632 | 10 | R774 | 14 | S800 | 6 | U810 | 6 |
| R378 | 10 | R495 | 12 | R633 | 10 | R775 | 14 | S801 | 6 | U811 | 6 |
| R379 | 10 | R496 | 12 | R634 | 6 | R777 | 14 |  |  | U812 | 6 |
| R380 | 11 | R497 | 12 | R635 | 10 | R778 | 14 | T370 | 11 | 4820 | 6 |
| R381 | 11 | R498 | 12 | R636 | 10 | R779 | 14 | T371 | 11 | U821 | 6 |
| R382 | 11 | R499 | 11 | R637 | 10 | R781 | 14 |  |  | 4830 | 6 |
| R383 | 11 | R500 | 9 | R639 | 6 | R782 | 14 | TP163 | 11 | U831 | 6 |
| R384 | 11 | R501 | 9 | R640 | 10 | R783 | 14 | TP173 | 11 | U840 | 6 |
| R385 | 11 | R502 | 9 | R641 | 10 | R784 | 14 | TP174 | 11 | U841 | 6 |
| R386 | 12 | R510 | 9 | R642 | 10 | R785 | 14 | TP231 | 11 | U850 | 5 |
| R387 | 12 | R512 | 9 | R643 | 10 | R786 | 14 | TP281 | 10 | U851 | 5 |
| R388 | 12 | R515 | 9 | R646 | 10 | R788 | 14 | TP284 | 11 | U860 | 5 |
| R389 | 12 | R516 | 9 | R647 | 10 | R789 | 14 | TP288 | 11 | U861 | 14 |
| R390 | 12 | R520 | 9 | R648 | 5 | R790 | 14 | TP291 | 11 | 4870 | 14 |
| R391 | 12 | R522 | 9 | R649 | 5 | R800 | 6 | TP370 | 11 | 4880 | 14 |
| R392 | 12 | R523 | 9 | R651 | 10 | R809 | 6 | TP568 | 11 | U950 | 5 |
| R393 | 12 | R525 | 9 | R652 | 5 | R810 | 6 | TP581 | 11 | U951 | 5 |
| R394 | 12 | R530 | 9 | R653 | 5 | R811 | 6 | TP585 | 11 | 4960 | 5 |
| R395 | 12 | R531 | 5 | R654 | 5 | R812 | 6 | TP612 | 11 |  |  |
| R396 | 12 | R532 | 10 | R655 | 5 | R813 | 6 | TP650 | 5 | VR200 | 9 |
| R397 | 12 | R533 | 10 | R656 | 5 | R814 | 6 | TP660 | 5 | VR298 | 11 |
| R398 | 12 | R534 | 10 | R660 | 5 | R815 | 6 | TP832 | 11 | VR390 | 12 |
| R399 | 12 | R535 | 10 | R661 | 5 | R816 | 6 |  |  | VR391 | 12 |
| R410 | 9 | R536 | 10 | R662 | 5 | R817 | 6 | U100 | 9 | VR420 | 9 |
| R420 | 9 | R541 | 10 | R663 | 5 | R818 | 6 | U120 | 9 | VR492 | 12 |
| R425 | 9 | R543 | 10 | R664 | 5 | R820 | 6 | U140 | 5 | VR493 | 12 |
| R430 | 10 | R544 | 10 | R665 | 5 | R821 | 6 | U150 | 11 |  |  |
| R431 | 10 | R545 | 10 | R666 | 5 | R822 | 6 | U190 | 5 | W110 | 9 |
| R435 | 10 | R546 | 10 | R667 | 14 | R823 | 6 | U220 | 9 | W221 | 9 |
| R436 | 9 | R547 | 10 | R668 | 14 | R824 | 6 | U221 | 9 | W470 | 11 |
| R437 | 10 | R550 | 14 | R669 | 14 | R825 | 6 | U230 | 9 | W511 | 9 |
| R438 | 10 | R551 | 10 | R670 | 14 | R828 | 6 | U270 | 5 | W762 | 14 |
| R440 | 10 | R555 | 5 | R671 | 14 | R830 | 6 | U271 | 5 |  |  |
| R441 | 10 | R556 | 10 | R672 | 14 | R831 | 6 | U272 | 5 |  |  |
| R442 | 10 | R557 | 10 | R673 | 14 | R832 | 6 | U280 | 5 |  |  |
| R443 | 10 | R558 | 10 | R674 | 14 | R833 | 6 | U320 | 9 |  |  |



SVSTEM DAC \& ACQUIIITION CONTROL REGISTERS <




## waveforms for diagram 5



SYSTEM DAC (CONT) \& AUXILLARY FRONT PANEL $\langle 6$


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WAVEFORMS FOR DIAGRAM 7


## WAVEFORMS FOR DIAGRAM 7 (con't)


*WAVEFORM 53 IS Shown twice



|  |  |  |  | A11－TIM | E base | displa | boar |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
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| cose | ${ }^{18}$ |  | ${ }_{\substack { 15 \\ \begin{subarray}{c}{15{ 1 5 \\ \begin{subarray} { c } { 1 5 } }\end{subarray}}^{1 / 2}$ |  | ${ }^{18}$ |  |  |  | ${ }_{\text {coid }}^{18}$ | （intis |  |
| $\underset{\substack{\text { cisisf } \\ \text { cise }}}{\substack{\text { cis }}}$ | ， |  |  |  |  |  |  |  | ${ }_{\substack{18 \\ 18 \\ 18}}^{18}$ | （ise | 7 |
| cial | ${ }^{18}$ | coicicis | ${ }_{8}^{15}$ | ${ }^{2008}$ | ${ }_{18}$ |  | ${ }_{\substack{18 \\ 18}}^{18}$ | U130 | ${ }_{16}$ | （ism | 8 |
| cicle | ${ }^{18}$ |  | ${ }_{15}$ | ${ }_{\substack{0181 \\ 0182}}^{108}$ | ${ }^{18}$ |  | ${ }^{18}$ | （utai | ${ }^{16}$ | cisso | \％ |
| coict | ${ }^{16}$ | cose | ${ }^{15}$ | ${ }_{\substack{\text { aras } \\ \text { ara }}}$ | ${ }^{18}$ |  | ${ }_{8}^{18}$ | ${ }^{4}$ | ${ }^{18}$ | ciseme | 品 |
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| coict | ${ }^{18}$ | $\substack{\text { corle } \\ \text { craz }}$ | ${ }^{15}$ |  | ${ }^{\frac{18}{18}}$ |  |  | （1022 | 品 | （ixio |  |
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| cos | ${ }_{\text {保 }}^{18}$ |  | ${ }^{15}$ | ${ }_{\substack{\text { R155 } \\ \text { R15 }}}$ | ${ }_{18}^{16}$ |  | 8 | ${ }^{12320}$ | ${ }^{17}$ |  |  |
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|  | ${ }^{15}$ |  | ${ }^{18}$ | ${ }_{\substack{\text { a }}}^{\substack{223 \\ 2024}}$ | ${ }^{18}$ | ${ }^{\text {asa }}$ | $\stackrel{15}{7}$ | U3at | ${ }^{16}$ |  | ， |
| coick | ， 15 | cose | ${ }^{18}$ |  | ${ }_{\text {coidi }}^{\substack{18 \\ 18}}$ |  | $\frac{3}{7}$ | （usion |  | cirun | $\stackrel{8}{7}$ |
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|  | ${ }^{15}$ | cintins | ${ }^{18}$ |  |  | ${ }_{\substack{\text { arase } \\ \text { ara }}}^{\text {a }}$ | ${ }_{15}^{17}$ |  | ${ }_{10}^{10}$ | ${ }_{\substack{4392}}^{\substack{402}}$ | ${ }_{15}^{15}$ |
| cick | ${ }^{15}$ |  | ${ }^{18}$ |  | ${ }^{8}$ |  | ${ }^{15}$ |  | 品 |  | ${ }^{18}$ |
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|  | ${ }_{\substack{15 \\ 15}}^{15}$ | cincore | ${ }_{8}^{8}$ | $\underbrace{}_{\substack { \text { cien } \\ \begin{subarray}{c}{\text { Rase } \\ \text { Ras }{ \text { cien } \\ \begin{subarray} { c } { \text { Rase } \\ \text { Ras } } }\end{subarray}}$ | ${ }_{\substack{18 \\ 18 \\ 18}}^{18}$ |  | $\frac{7}{7}$ | （uasi | ${ }_{18}^{70}$ | （uas |  |
| ${ }_{\substack{\text { cisil } \\ \text { cisis }}}^{\substack{\text { cis }}}$ | ${ }^{15}$ | ，yino | 8 |  | ${ }^{18}$ |  | ${ }_{15}$ | U423 | 16 | Uu35 | 8 |
|  | ${ }^{15}$ | cinco | ${ }^{18}$ | ${ }_{\substack{\text { and } \\ \text { arat } \\ \text { arat }}}$ | ？ |  | ${ }^{15}$ | cise | ${ }^{16}$ |  |  |
|  | 年15 | ， | \％ |  | ${ }_{15}$ |  | ${ }^{18}$ |  | ${ }^{16}$ |  | ${ }^{8} 8$ |
|  |  |  |  |  |  |  |  |  | ${ }_{18}^{10}$ | （wita | \％ |
|  | ${ }^{16}$ | ${ }^{\text {disa }}$ | ${ }^{18}$ |  | ${ }^{18}$ |  | ${ }^{18}$ | cismo | 8 | ${ }^{\text {wr }} 80$ | ${ }^{5}$ |
|  | ¢ | $\underbrace{\text { jus }}_{\substack{\text { jus } \\ \text { jus }}}$ |  |  |  |  |  |  | ${ }^{6}$ |  |  |

system clocks $\rangle$


| ASSEMBLY A11 |  |  |  |  |  |  |  |  |  |  |  |
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| （cas | ${ }_{4}^{45}$ | ${ }_{\text {\％}}^{\text {\％}}$ | $\underbrace{}_{\substack{\text { Rr21］} \\ \text { R21F }}}$ | ${ }_{\substack{36 \\ 4 \\ 4 \\ \hline}}$ | $\underset{\substack{\text { TF }}}{\text { T }}$ | ${ }_{\text {L }}^{\text {U5288 }}$ |  |  |  |  |  |
| ${ }_{\text {cass }}$ | ${ }_{4}$ |  |  | $\stackrel{4}{4}$ | $\underset{\substack{\text { TF } \\ \sim}}{\substack{\text { a }}}$ |  |  | ${ }_{70}^{70}$ | Us80 | $\begin{gathered} { }_{\Omega}^{8} \\ { }_{3}^{6} \end{gathered}$ | ${ }_{\infty}$ |
| cine |  | ${ }_{\circ}^{\circ}$ | ${ }_{\substack{\text { arral } \\ \text { Rras }}}^{\text {and }}$ |  |  |  | － | $\begin{gathered} 70 \\ { }_{8 E} 0 \\ \hline \end{gathered}$ |  |  |  |
| ${ }^{5613}$ | ${ }^{18}$ | ${ }^{\circ}$ | ${ }_{\substack{\text { Reas } \\ \text { Reas }}}^{\text {and }}$ | $\underset{\substack{2 M \\ 3 M}}{\substack{\text { a }}}$ | ${ }_{\substack{\text { g\％}}}$ |  | $\underset{\substack{\text { ax } \\ \text { ef }}}{\substack{\text { a }}}$ | 辰 |  |  | ${ }_{\text {orn }}^{\text {ert }}$ |
|  | ${ }_{\substack{\text { sf } \\ 18}}^{\text {cid }}$ | ${ }_{\substack{\text { dem }}}^{\text {dem }}$ | $\underbrace{}_{\substack{\text { Reass } \\ \text { Resbe }}}$ | ${ }_{\substack{\text { Sn } \\ \text { Sn }}}$ |  |  | $\underbrace{}_{\substack { 2 \in \\ \begin{subarray}{c}{\text { EH }{ 2 \in \\ \begin{subarray} { c } { \text { EH } } }\end{subarray}}$ | 辰长 |  | $\begin{aligned} & { }_{3}^{30} \\ & 20 \\ & 20 \end{aligned}$ | ， |
|  | ${ }_{28}{ }_{28}$ | ${ }_{\text {\％}}^{0}$ |  | ${ }_{\text {en }}^{\text {en }}$ | ${ }_{\text {at }}^{\text {g\％}}$ | Ue2za | ${ }_{\substack{16 \\ 40}}^{0}$ | $\underset{\sim}{\text { \％}}$ | Ueas | $\hat{o n}_{\mathrm{gn}}^{6}$ | ${ }_{\sim}^{\infty}$ |
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|  |  | 80 |  | ${ }_{\text {cos }}^{\substack{0}}$ | ＊ |  | ¢ |  | Unemo | $\substack{\begin{subarray}{c}{\begin{subarray}{c} { c \\ \begin{subarray}{c}{0{ c \\ \begin{subarray} { c } { 0 } } \end{subarray}} \end{subarray}} \\ {\hline} \end{subarray}$ | 迷 |
|  | ， |  |  | ${ }_{4 N}^{4 \times}$ | 䇣 | cin | ${ }_{\substack{88 \\ 88 \\ 8 \\ 8}}$ | ¢ | （ Uasse |  |  |
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|  | $\underset{\substack{\text { ofe }}}{16}$ | $\underset{\substack{\text { \％}}}{\text { F }}$ |  | $\underset{\substack{10 \\ 3 \\ 3}}{\substack{1}}$ |  | 隹 | $\stackrel{\substack{1 / 4 \\ i j}}{ }$ |  | ve11 | ${ }^{24}$ |  |
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| OTHER PAATS |  |  |  |  |  |  |  |  |  |  |  |
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TIME BASE CONTROLLER \& ACQUISITION MEMORY $\langle 8$



"See Parts List ior
serial number ranges.


ATTENUATORS \＆PREAMPS $\langle\stackrel{9}{9}\rangle$

| circur | Scomem | bocaro | cricur | ${ }^{\text {cockum }}$ | －coano | circur | ${ }_{\text {scoatiom }}$ | Locarom | cincur | scomb | bocarom |
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| coill |  | ${ }_{\substack{20 \\ 20}}^{\substack{20}}$ |  | \％00 | ${ }^{30}$ | 110 | ${ }^{\text {ax }}$ | ${ }^{10}$ |  | ${ }_{\substack{24 \\ 24}}^{28}$ | 80 |
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| coicle | ¢ |  | ${ }^{\text {coind }}$ | ${ }_{45}$ | ${ }^{20}$ | ${ }_{0} 081$ | ${ }_{8}^{68}$ | ${ }_{80}$ |  | $\underset{\substack{3 \\ 3 \times \\ 23}}{ }$ | coic |
| coin | $\underbrace{}_{\substack{\text { ox } \\ \text { ga }}}$ | ${ }^{3}$ | coick | $\infty$ | coc | $\substack{\text { R．10 } \\ \text { R．11 }}_{\substack{\text { Ren }}}$ | ${ }_{\text {a }}^{\text {en }}$ | ${ }^{18}$ |  | ， |  |
|  | ${ }_{\substack{\text { sut } \\ \hline 1}}$ | ${ }_{\substack{30 \\{ }_{3} \\ \\ \\ \hline}}$ | ${ }^{\text {Ca3 }}$ | ${ }_{\substack{80 \\ 10}}$ | ${ }_{\substack{40 \\ 80}}$ |  | \％ | coc |  | $\substack { \text { sad } \\ \begin{subarray}{c}{\text { Sa }{ \text { sad } \\ \begin{subarray} { c } { \text { Sa } } } \\{\hline} \end{subarray}$ | ${ }_{\substack{80 \\ 88 \\ 80}}^{80}$ |
|  |  | 哏30 | cinil | ${ }_{4}^{10}$ | $\underset{\substack { \text { sc } \\ \begin{subarray}{c}{\text { ction }{ \text { sc } \\ \begin{subarray} { c } { \text { ction } } }\end{subarray}}{ }$ | $\underbrace{}_{\substack { \text { R} \\ \begin{subarray}{c}{12121 \\ \text { R130 }{ \text { R} \\ \begin{subarray} { c } { 1 2 1 2 1 \\ \text { R130 } } }\end{subarray}}$ |  |  |  | $\underset{\substack{\text { sin }}}{\substack{\text { an }}}$ | ¢ |
|  | ¢ |  | Cims | ${ }_{\substack{30 \\ 30}}$ | ${ }_{\substack{\text { rc } \\ 0}}^{\substack{\text { c }}}$ | ${ }_{\substack{\text { R，312 } \\ \text { R，32 }}}$ | ${ }^{1 \times}$ |  |  | ${ }_{68}^{48}$ | 年 |
| cier |  | $\substack{30 \\ 30}_{\substack{30}}$ |  | $\underbrace{}_{\substack{36 \\ \\ 85}}$ |  |  | $\underset{\substack{2 \mathrm{an} \\ 20}}{2}$ | $\underbrace{\substack{\text { F }}}_{\substack{\text { zF }}}$ |  | ${ }_{78}^{48}$ | ¢ |
| ${ }_{\text {cose }}^{\substack{\text { c2a } \\ \text { c2a }}}$ | ${ }_{\text {am }}^{4}$ |  |  | ${ }_{\substack{2 \\ 35}}^{2}$ |  | ${ }_{\substack{\text { R．138 } \\ \text { R140 }}}^{\text {dic }}$ | ${ }_{6}^{4 M}$ |  | $\underbrace{}_{\substack{\text { R．1002 } \\ \text { Riose }}}$ | ${ }_{78}^{78}$ | ${ }^{3,}$ |
| coick | ${ }_{\substack{40 \times \\ 2 m}}^{\text {m }}$ |  |  | ${ }_{\substack{35 \\ 30}}^{35}$ | ${ }_{\substack{78 \\ 78}}^{70}$ | ${ }_{\substack{\text { R．14，} \\ \text { Ris }}}^{\text {and }}$ | $\underset{\substack{\text { em } \\ \text { emm }}}{\text { en }}$ | ${ }_{\substack{26 \\ 26}}^{26}$ | ${ }^{\text {n } 1004}$ | ${ }^{8}$ | ${ }^{14}$ |
| ${ }_{\substack{\text { cose } \\ \text { cist } \\ \text { c2a }}}$ | $\underbrace{\substack{50 \\ 30}}_{3}$ | ${ }_{\substack{20 \\ 50}}^{\substack{\text { so }}}$ |  | ${ }_{80} 8$ | ${ }_{\substack{80 \\ 70}}^{\text {go }}$ | ${ }_{\substack{\text { Relat } \\ \text { Reat } \\ \hline 102}}$ | ${ }_{80}$ | $\underbrace{2 a^{2}}_{\substack{2 x \\ 38}}$ | U1120 | $\underbrace{}_{\substack{\text { ck } \\ \text { ¢H }}}$ | ${ }_{20}{ }^{18}$ |
| cosis |  |  | cincen | ${ }_{\substack{30 \\ 88}}$ | 品品 | （ixal | $\begin{gathered} \text { en } \\ \substack{10} \\ \hline \end{gathered}$ | $\begin{gathered} 38 \\ 38 \\ 38 \end{gathered}$ | Su20 |  | cick |
| cose | $\stackrel{3}{6}$ | ${ }_{\substack{4 c \\ 40}}^{\substack{0}}$ | \％1112 | $\underbrace{}_{\substack{56 \\ 34 \\ 34}}$ | ${ }^{20}$ |  | sim | ${ }_{\substack{30 \\ 30}}^{30}$ | 旡 | 2， | ${ }_{\substack{2 E \\ 26}}^{\substack{26}}$ |
|  | ${ }_{4}^{4}$ | ${ }_{\substack{\circ \\ 80}}$ | ¢ |  | ${ }_{\substack{16 \\ \\ 20}}^{10}$ | ¢ | ${ }_{3}$ | ¢ | （tat |  |  |
|  | ${ }_{3}^{30}$ | ${ }_{\substack{4 c \\ s c}}^{\substack{\text { c }}}$ |  | $\underbrace{\text { cr }}_{\substack{\text { cf } \\ \text { ef }}}$ | ${ }_{\text {cia }}^{\text {en }}$ |  |  |  |  | 込 | $\underset{\substack{70 \\ 70}}{\text { col }}$ |
|  | ${ }^{\text {a }}$ | ¢0 | ， 12 | ${ }_{\text {or }}^{\text {of }}$ |  | ${ }_{\substack{\text { R231 } \\ \text { R23，} \\ \text { R2a }}}$ | ${ }^{4}$ |  |  | ${ }_{\substack{\text { 3n }}}^{\substack{\text { and }}}$ |  |
| can | ${ }_{21}^{110}$ | St |  | $\underbrace{\text { ck }}_{\substack{\text { ox } \\ \text { st }}}$ |  |  | $\ldots$ |  |  | ${ }_{\substack{3 \\ 3 \\ 3 \\ 3 \\ 4}}$ | 隹 |
| $\underset{\substack{\text { cass } \\ \text { ciso }}}{\substack{\text { ase }}}$ |  | ${ }_{8}^{80}$ | ${ }_{\text {cose }}^{1250}$ | ${ }^{\text {a }}$ | 50 |  | ${ }^{6}$ | ${ }^{2}$ | vera | ${ }_{5}^{54}$ | ${ }^{30}$ |
|  |  |  | （isto |  | ， |  | com |  | vareo | ${ }^{24}$ | 10 |
| ccis | $\underbrace{24}_{3}$ |  | L2275 |  | ${ }_{25}$ |  |  |  |  | $\underset{\substack{56 \\ \text { at } \\ \text { at }}}{ }$ | （30 |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Other parts |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  | （cherssems | ${ }_{\text {P147 }}^{\text {P14e }}$ | ${ }_{\text {gf }}^{\text {gF }}$ | chats |
|  | ${ }_{\text {and }}^{\text {an }}$ |  |  |  |  |  | ${ }_{\text {and }}^{\text {an }}$ |  | яroms | A |  |

－See Parss List tor
serial number ranges．




BzECL in SHORTPIPE MODE (20us/DV)


$\stackrel{\text { *See Parts List for }}{\text { serfal number ranges }}$



TRIGGERS \＆PHASE CLocks（1）

| circur |  | Locanom | circur | ${ }^{\text {Locatiow }}$ | Loomion | cincur | ${ }_{\text {coctem }}$ | bocarom | cincur | Scoctiow | Loantow |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ASSEMBLY A10 |  |  |  |  |  |  |  |  |  |  |  |
|  |  | ${ }_{1 \times}^{10}$ | ${ }^{1157}$ | ${ }^{3 N}$ | $\stackrel{ }{ }$ |  |  | ${ }_{3}^{3 \times}$ |  |  |  |
|  | ${ }_{\substack{\mathrm{sc} \\ \mathrm{cc} \\ 0}}$ | ${ }_{2}^{2 \times}$ | $\stackrel{\substack{1250 \\ 12200}}{ }$ | ${ }^{80}$ | ${ }_{\substack{20 \\ 3 H \\ 36}}$ |  |  | ${ }_{\substack{3 \times \\ 4 \times}}$ |  | $\underbrace{\substack{ \\3}}_{\substack{3 \times \\ 3 \times}}$ | ${ }^{\text {em }}$ |
| ¢ | $\overbrace{\substack{i 8 \\ \hline 18}}^{\substack{18}}$ | ${ }^{3 N}$ |  | 10 | ${ }_{\text {3K }}^{\text {3\％}}$ | cien | ${ }_{8}^{40}$ | ¢ |  | $\underbrace{24}_{2}$ |  |
| cois | ${ }_{\substack{80 \\ 40 \\ 40}}$ | $\substack{2 H \\ 3 H \\ 3 H}_{\substack{\text { r }}}$ | $\xrightarrow[\substack{\text { Lasso } \\ \text { Last }}]{ }$ | $\underset{\substack{\text { am } \\ 4 \\ 4}}{ }$ | $\underbrace{}_{\substack { 6 \mathrm{sk} \\ \begin{subarray}{c}{6{ 6 \mathrm { sk } \\ \begin{subarray} { c } { 6 } }\end{subarray}}$ | $\substack{\text { Rese } \\ \text { Reage } \\ \text { Reade }}$ |  |  | ${ }_{\substack{\text { Resas } \\ \text { R594 }}}$ | ${ }_{2}^{24}$ | ${ }_{\text {a }}$ |
|  | ${ }_{\substack{76 \\ \\ 80}}$ |  | cise | ${ }_{4}^{4 \times}$ |  |  | T0 | ${ }_{\substack{3 \times \\ 4}}$ |  | ${ }_{4}^{38}$ | ${ }_{\substack{3 \times \\ 4 \times}}$ |
|  | 碳 | ${ }_{\substack{3 \times 1 \\ 3 \times \\ 2 \times}}$ |  | ${ }_{4}^{4 M}$ |  |  |  | ${ }_{\substack{\text { sm } \\ \text { mim }}}$ | тре3 | $48$ | ${ }_{2 m}^{2 k}$ |
|  | \％ | ${ }_{\substack{2 \times \\ 20}}^{2 \times}$ |  | ${ }_{4 \times}$ | ${ }_{5}$ |  | ${ }_{\text {a }}^{20}$ | ${ }_{3}^{3 m}$ |  | ${ }_{\substack{\text { sk }}}^{\text {ck }}$ | $\begin{aligned} & { }_{21}^{20} \\ & { }_{21} \end{aligned}$ |
|  | ${ }_{\substack{10 \\ 3,5}}^{10}$ | ${ }_{\substack{4 \times \\ 3 \times}}$ |  |  | ${ }_{\text {lik }}^{16}$ | $\substack{\text { Rer } \\ \text { R278 }}_{2}$ | $\underset{\substack{4 \\ 4 \sim}}{\substack{\text { d }}}$ | ${ }_{4}^{4}$ | ${ }_{\substack{\text { Treas }}}^{\text {Treas }}$ | ${ }_{\substack{28 \\ 28}}^{28}$ | $\underbrace{\substack{3}}_{\substack{3 E \\ 2 \times 1}}$ |
| coick | ${ }_{\substack{2, 16}}$ |  |  |  | ${ }_{\substack{1 \times \\ 3 \times}}$ | ${ }_{\text {Rex }}^{\text {Reas }}$ | ${ }_{\sim}^{21}$ | ${ }_{2 \times}^{2 \times}$ | ${ }_{\substack{\text { Trpaid }}}^{\text {Tras }}$ | ${ }_{\text {am }}^{\text {am }}$ | ${ }_{\text {in }}^{\text {2N }}$ |
| $\substack{\text { cars } \\ \text { casa }}$ | $\underbrace{}_{\substack{\text { gat } \\ 24}}$ | ${ }_{\substack{\text { si }}}^{\text {n }}$ | 0270 | ${ }^{\text {з }}$ | ${ }_{3}^{3 \times}$ | ${ }_{\text {Reas }}^{\text {Reas }}$ | $\stackrel{\substack{\text { gm } \\ \text { gm }}}{\text { cos }}$ | ${ }_{\substack{2 N \\ 2 N}}$ |  | $\underbrace{}_{\substack{\text { st } \\ 28}}$ | ${ }_{6}^{40}$ |
| ${ }^{\text {casb }}$ | ${ }^{24}$ | $\pi$ |  | ${ }_{3}^{3}$ | ${ }_{2 \times}^{4 N}$ | ${ }_{\text {coser }}^{\text {Reag }}$ | ${ }_{\substack{\text { om } \\ \text { \％m }}}$ | ${ }_{\substack{2 N \\ 2 N}}^{2 N}$ |  | ${ }_{28}^{23}$ | $\begin{aligned} & \text { en } \\ & \end{aligned}$ |
|  | ＊ | ${ }_{3 \times}^{4 \times}$ | ${ }^{0288}$ | ${ }^{\text {a }}$ | ${ }^{2 P}$ |  |  | ¢ | ${ }_{\text {Trase }}^{\text {Trais }}$ | ${ }_{\substack{28 \\ 28}}^{28}$ | ${ }_{\text {\％}}^{108}$ |
|  | ${ }^{\text {N }}$ | ${ }_{\substack{3 N \\ 80 \\ 8 .}}$ |  | 780 | ${ }^{16}$ |  | ¢ | ${ }_{3}^{3 \times 2}$ | U1180 | ${ }^{20}$ | \#1 |
| cinco | ${ }_{2}^{24}$ | ${ }_{\text {n }}^{\text {n }}$ |  | 70 |  |  | cick | ¢ |  | $\stackrel{\substack{40 \\{ }_{x}^{m} \\ m}}{ }$ | ${ }_{3}^{4}$ |
| mint | ${ }_{\text {\％8 }}{ }^{\text {® }}$ | ${ }_{20}^{20}$ |  | ${ }_{\substack{4.0 \\ 40}}^{\substack{4}}$ |  | ${ }^{2308}$ |  | ${ }_{4 \times}^{4 \times}$ | 边 | ${ }_{\text {gem }}^{\text {gm }}$ | $\substack{\begin{subarray}{c}{3 m \\ 3 m} }} \\{3 m} \end{subarray}$ |
| ¢， | ${ }_{\substack{7, 8, \\ \hline 8 .}}$ | ${ }^{16}$ |  | ${ }_{88}^{88}$ | $\begin{gathered} \text { ik } \\ 2.2 \end{gathered}$ | ${ }_{\text {a }}^{\text {ama }}$ | $\underset{\substack{20 \\ 28}}{\substack{2}}$ | ${ }_{\substack{\text { sm } \\ 4 M}}$ | 込 | ${ }^{20}$ | $\underset{\substack{4 \mathrm{~m} \\ \mathrm{~m} \\ \hline \\ \hline}}{ }$ |
| cin | ${ }_{\substack{1 / \\ b_{k} \\ \hline}}$ | ${ }_{\substack{2 \times \\{ }_{2}^{2 K}}}$ |  | ${ }^{6+4}$ | ${ }_{3}$ | ${ }_{\substack{\text { Rass } \\ \text { Rase }}}^{\text {ase }}$ | ${ }_{20}^{20}$ | ${ }_{4 \times}^{4 \times}$ | ve238 | ＋ |  |
|  |  | $c22K$ |  | ¢ |  | $\begin{gathered} \substack{\text { Rase } \\ \text { Rese }} \end{gathered}$ |  |  | w70 | ${ }^{*}$ | 4 |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| OTHER PARTS |  |  |  |  |  |  |  |  |  |  |  |
| ${ }_{\substack{12000}}^{\text {Numo }}$ | ${ }_{\substack{\text { ¢K } \\ \text { OK}}}$ | ${ }_{\text {chasems }}^{\text {chasss }}$ |  | ${ }_{\text {TH}}^{\text {T，}}$ |  |  |  |  |  | ${ }_{78}^{80}$ | $\underset{\substack{\text { chassss } \\ \text { chasss }}}{ }$ |
| P111 | ${ }^{\text {an }}$ | cruss |  | ${ }_{\text {en }}^{\text {en }}$ |  | ${ }^{\text {P1414 }}$ |  |  |  |  |  |



WAVEFORMS FOR DIAGRAM 12


## 

JITTER CORRECTION RAMPS

| crincur | Sochem | Locano | circur |  | Looano | cincur |  | Locono | cincur | ${ }_{\text {semen }}^{\text {sochem }}$ | ${ }^{\text {Boanao }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ASSEMBLY A10 |  |  |  |  |  |  |  |  |  |  |  |
| ${ }^{\text {casa }}$ | ${ }^{6}$ | ${ }^{3 N}$ | ${ }^{020}$ | ${ }^{8,}$ | ${ }^{3 N}$ | ${ }^{\text {R3a }}$ | ${ }^{\text {gr }}$ | ${ }^{4 P}$ | ${ }^{\text {Rese }}$ | ${ }^{2 F}$ | ${ }^{6 N}$ |
|  | ผ | ${ }_{\text {ap }}$ |  | ${ }_{\text {\％}}^{8,}$ | ${ }_{\text {amm }}$ |  | ${ }_{8}^{80}$ | $\underbrace{}_{\substack{\text { gn } \\ 3 \mathrm{~N}}}$ |  | ${ }_{\text {c }}^{\text {a }}$ | ${ }^{1}$ |
| cial | cic | ${ }_{4}^{4 N}$ |  |  | ${ }_{\substack{\text { an }}}^{\text {N }}$ |  | 边 | ${ }_{3}^{30}$ | cincin | ${ }_{\substack { \text { cic } \\ \begin{subarray}{c}{16{ \text { cic } \\ \begin{subarray} { c } { 1 6 } } \\{\hline 0}\end{subarray}}$ | ${ }_{\text {sin }}$ |
|  | ¢ | 巡 |  |  | ${ }_{\substack{0}}^{\substack{N}}$ |  | $\underbrace{88}_{\substack{38 \\ 88}}$ | ${ }_{\substack{\text { sm } \\ \text { sm }}}^{\text {cm }}$ |  |  | ${ }_{4}^{48}$ |
|  |  | ®N | ois | $\underbrace{}_{\substack { \text { RE，} \\ \begin{subarray}{c}{E{ \text { RE，} \\ \begin{subarray} { c } { E } }\end{subarray}}$ | ${ }_{\text {on }}^{\text {on }}$ |  |  | ${ }_{\substack{\text { gp }}}^{\text {gp }}$ |  | ${ }_{\substack{\text { co } \\ 70}}$ |  |
| ${ }_{\substack{\text { cisen } \\ \text { cose }}}^{\text {cos }}$ | \％${ }_{\text {en }}$ | ${ }_{\substack{\text { an }}}^{\substack{N}}$ |  |  | ${ }^{4 N}$ | $\underbrace{}_{\substack { \text { Rase } \\ \begin{subarray}{c}{\text { mage }{ \text { Rase } \\ \begin{subarray} { c } { \text { mage } } }\end{subarray}}$ | ${ }_{21}^{23}$ | ${ }_{\substack{\text { sp }}}^{50}$ | $\underbrace{\text { Rex }}_{\substack{\text { Rese } \\ \text { Rex }}}$ |  | ${ }_{\text {ap }}^{\text {ap }}$ |
| Cr2as | ${ }_{\text {TE }}$ | $\underset{\substack{3 N \\ 2 N}}{ }$ |  |  |  |  | 近 | $\underbrace{\text { en }}_{\substack{\text { an } \\ \text { gn }}}$ | \％390 | ${ }_{31}^{70}$ | ${ }^{38}$ |
| cos | coic | ${ }_{\substack{3 N \\ 3 N}}$ |  | $\begin{gathered} 8 \mathrm{~g} \\ \substack{80\\ } \end{gathered}$ |  |  |  |  | Usisma | $\begin{aligned} & 30 \\ & 10 \\ & 00 \end{aligned}$ | ¢ |
|  |  | ¢ | $\underbrace{\text { ase }}_{\substack{\text { Reas } \\ \text { R2as }}}$ | ${ }_{\substack{80 \\ 80 \\ 80}}^{8}$ | ${ }_{\substack{3 N \\ 3 N}}$ |  | 数 | ${ }_{\text {gm }}^{\text {gm }}$ |  | ¢00 | $\underbrace{}_{\substack{\text { SN } \\ \text { SN }}}$ |
|  |  | ¢ ${ }_{\substack{\text { sN }}}^{\text {N }}$ |  | ${ }_{\substack{\text { \％} \\ \sim}}$ | ${ }_{\substack{3 P \\ 3}}^{3}$ |  | ${ }_{40}^{3 H}$ |  | vaso | \％ |  |
| ง11 | ${ }^{24}$ | ${ }^{20}$ | ${ }_{\substack{\text { Rexal } \\ \text { R298 }}}$ | \％ | ${ }_{\substack{3 P \\ 3 p^{3}}}$ | $\substack{\text { Real } \\ \text { Ras2 }}_{\text {Ras }}$ |  | ¢0\％ | Vmas |  |  |
| Ls80 |  |  |  |  |  |  | ${ }_{40}^{4}$ | ${ }_{\substack{\text { gn } \\ \text { gn }}}$ |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| OTHER PAATS |  |  |  |  |  |  |  |  |  |  |  |
| Pl11 | ${ }^{24}$ | cmassis |  |  |  |  |  |  |  |  |  |



2440 Service
WAVEFORMS FOR DIAGRAM 13


| cincur | sochtion | Locarom | cimeur | socatiow | Looantow | cincur | scontiom | Locanion | cincur | socheum | bocarom |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ASSEmbly aio |  |  |  |  |  |  |  |  |  |  |  |
| 0102 | ${ }^{1} \mathrm{E}$ | ${ }^{24}$ | ${ }_{\text {din }}$ |  | ${ }_{24}^{20}$ | ${ }^{\text {R102 }}$ | ${ }^{7}$ | ${ }^{24}$ |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| ASSEMELY 13 |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  | U841B U842A U842B U851A U851B U851C U852A U852B U853A U853B U871 U872A U872B U881 VR841 W101 W110 W110 W110 W110 W110 W110 $W 110$ $W 122$ $W 122$ $W 122$ |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| OTHER PAATS |  |  |  |  |  |  |  |  |  |  |  |
| P11 | ${ }^{76}$ | ${ }^{\text {chassss }}$ |  |  |  |  |  |  |  |  |  |



## WAVEFORMS FOR DIAGRAM 14

TEST SCOPE A TRIGGERED RISING EDGE OF SO \& B TRIGGERED ON RISING EDGE OF TTLB1


VOLTS/DIV AT 100 mV
SEC/DIV AT 5 5 s;
CALIBRATOR SIGNAL APPLIED
TO CH 1 INPUT; AC COUPLED.
VERT MODE CH 1 (CH 2 FOR


| cincur | socter | Locarion | cincur | scontiow | ${ }_{\text {Locano }}^{\text {boan }}$ | crincur | ，ocham | （10ation |  | Scoction | Locaram |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Assembly aio |  |  |  |  |  |  |  |  |  |  |  |
|  | ${ }_{\substack{2 H \\ 8 H}}$ | ${ }^{\text {en }}$ | ${ }^{\text {Juat }}$ | ${ }^{\text {c／}}$ | ${ }_{2 \times}^{2 \times}$ | ${ }_{\text {ascos }}^{\text {Reso }}$ | ${ }^{50}$ |  | ${ }^{\text {Rreme }}$ | ${ }^{40}$ | ${ }^{\text {aK }}$ |
|  | \％ |  |  |  | $\underbrace{\substack{2 \times}}_{\substack{2 \times \\ 2 \times}}$ | cinctin | ${ }_{\substack{30 \\ 30}}^{20}$ | ${ }_{\text {en }}^{\text {en }}$ |  | ${ }_{\substack{\text { em } \\ 40}}$ |  |
| ${ }_{\text {cosas }}$ | ${ }_{4}$ | ${ }_{\text {ak }}$ | N100 | ${ }^{1,}$ | 近 | nemos | ${ }_{\substack{36 \\ \\ \\ 0}}$ | ${ }^{2}$ |  | ${ }^{7 \times 1}$ | ${ }_{\text {ak }}^{0}$ |
|  | ${ }_{80}^{81}$ | $\underset{\substack{\text { im } \\ \hline \multirow{2}{*}{\hline}\\ \hline}}{ }$ | j100 | ${ }_{2}^{2 M}$ | ${ }^{\text {a }}$ |  | ${ }^{80}$ | ${ }^{8 N}$ |  | $\begin{gathered} 30 \\ 3.30 \\ 3.31 \end{gathered}$ | \％ |
|  | ${ }_{\substack{\text { ci } \\ \text { cu } \\ \text { en }}}$ | ${ }^{2}$ | cise | $\underset{\substack{2 m \\ s f}}{\substack{\text { che }}}$ | ${ }_{\text {gim }}^{\text {gim }}$ |  | ， | ${ }_{\text {sin }}^{\text {sin }}$ | ners | ${ }_{\substack{80 \\ 80 \\ 80}}$ |  |
|  | ${ }_{\substack{\text { Ren } \\ 80}}$ | \％ | $0 \times 8$ | ${ }^{6}$ | ev |  | ${ }^{20}$ | ${ }_{\text {at }}^{\text {git }}$ | Rear |  | ¢ |
| cion | ${ }_{20}^{10}$ | ${ }_{\text {¢m }}^{\text {om }}$ | （ormo | coick | ${ }_{\substack{\text { en } \\ \text { en }}}$ |  | ${ }_{2}^{23}$ | ${ }_{9}^{8 \mathrm{em}}$ |  | 紮 | ${ }_{\text {on }}^{\text {on }}$ |
| circia |  | ${ }_{\text {en }}$ |  | $\underset{\substack { 1 / \\ \begin{subarray}{c}{2{ 1 / \\ \begin{subarray} { c } { 2 } }\end{subarray}}{ }$ | ${ }_{\text {am }}^{\text {gm }}$ |  | $\underbrace{2 J}_{\substack{2 J \\ s E}}$ | ${ }_{\text {sim }}$ |  | ${ }_{\substack{6 \\ 60}}$ | ${ }_{\substack{\text { ow } \\ \text { \％K }}}$ |
| citas | ${ }_{\substack{\circ 0 \\ \infty}}^{\text {ec }}$ |  |  | ${ }_{\substack { 2 \\ \begin{subarray}{c}{20{ 2 \\ \begin{subarray} { c } { 2 0 } } \\{i,}\end{subarray}}$ | ${ }_{\substack{\text { em } \\ \text { em }}}$ |  | ¢00 | ${ }_{\text {a }}$ | Useon | ${ }^{10}$ |  |
|  | com | cot |  | ¢ | $\underbrace{\text { m }}_{\substack{\text { gm } \\ \text { m }}}$ |  | \％ |  | （viseos | $\underset{\substack{36 \\ \hline 14}}{ }$ | \％ |
| coicce | cos | \％ | coirco | ¢ | ${ }_{\text {n }}$ |  | ， | $\stackrel{\text { ma }}{\substack{\text { m }}}$ | cistion | ${ }_{5}$ | 既 |
| ${ }_{\text {cosaz }}$ | ${ }_{80}$ | ${ }_{80}$ | cos |  | $\underset{\substack { \text { TK } \\ \begin{subarray}{c}{\text { TK }{ \text { TK } \\ \begin{subarray} { c } { \text { TK } } }\end{subarray}}{ }$ | $\substack{\text { Ritase } \\ \text { Rree }}$ | ${ }_{\substack{8 \\ 80}}^{20}$ |  |  |  | $\underbrace{80}_{\substack{80 \\ 80}}$ |
|  |  | ${ }_{\text {8\％}}^{\text {8\％}}$ | coic |  |  |  |  |  | cos | ${ }^{2}$ | ${ }_{\substack{\text { gm } \\ \text { gm }}}$ |
|  |  | ${ }_{80}^{\text {m }}$ |  | ${ }_{\substack{3 \% \\ 40}}$ | ${ }_{\substack{0 \\ 0 \times}}$ | ${ }_{\text {R }}^{\text {R773 }}$ |  | ¢ |  | ${ }_{\text {®0 }}^{00}$ | ${ }_{n}^{\pi}$ |
|  | $\underbrace{\substack{\text { k }}}_{\substack{3 \times \\ 3 \times}}$ | ${ }_{\text {at }}$ | $\underbrace{\text { ari }}_{\substack{\text { ara } \\ \text { ara }}}$ | $\underbrace{\substack{\text { cen }}}_{\substack{3 E \\ 4.5}}$ | ${ }_{\substack{8 \% \\ 88}}$ |  | ¢ | ${ }_{\substack{8 \times \\ \%}}^{\text {\％}}$ |  | $\stackrel{\substack{\text { a } \\ 7 \mathrm{~m} \\ \hline}}{ }$ | ＊＊ |
|  |  | ${ }_{\substack{\text { sm }}}^{\text {sm }}$ |  | ${ }_{\substack{\text { 8K } \\ \text { 8K }}}$ | ${ }_{\text {80 }}^{\text {80 }}$ | ${ }_{\text {corm }}^{\text {R7\％}}$ | ${ }_{\sim}^{4}$ | ¢ |  | ${ }_{\substack{\text { mim } \\ 7 m}}$ | \％ |
| Ju7 | ${ }^{40}$ | ${ }^{\text {sm }}$ | coicle | ${ }_{\substack{10 \\ 80}}^{\substack{0}}$ | ¢ |  | ${ }_{\substack{\text { so } \\ 50}}$ | ${ }_{3}$ |  | ${ }_{4}^{40}$ | ${ }_{\text {a }}$ |
| Sill | ¢ | $\underbrace{\substack{\text { 2K }}}_{\substack{20 \\ 2 \times}}$ |  |  |  |  |  |  | Usemen | ${ }_{\text {\％}}^{\text {\％}}$ | ¢ |
| Stai | ${ }_{\substack{38 \\ 46 \\ 46}}^{26}$ | ${ }_{\substack{2 \times \\ 2 \times}}^{2 \times}$ |  |  |  |  | \％ | $\cdots$ | w82 | a | ＊ |
|  |  |  |  |  |  |  |  |  |  |  |  |
| OTHER | Aats |  |  |  |  |  |  |  |  |  |  |
| $\substack { \text { che } \\ \begin{subarray}{c}{\text { plof } \\ \text { plat }{ \text { che } \\ \begin{subarray} { c } { \text { plof } \\ \text { plat } } } \end{subarray}^{\text {pri }}$ | ${ }_{\substack { 50 \\ \begin{subarray}{c}{50{ 5 0 \\ \begin{subarray} { c } { 5 0 } } \\{\text { con }}\end{subarray}}$ |  |  | ${ }_{38}^{24}$ |  | $\begin{gathered} \text { p,441 } \\ \text { Pp } 1,141 \end{gathered}$ |  | $\underbrace{\substack{\text { and }}}_{\substack{\text { chassss } \\ \text { Chabssis }}}$ | P141 | ${ }^{80}$ | ${ }^{\text {crasssis }}$ |

＊See Parts List for
serial number ranges




DISPLAY \& ATTRIBUTES MEMORY $\langle 16$



Waveforms for diagram 17


DISPLAY CONTROL 17


|  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |  |  |
| OTHER PARTS |  |  |  |  |  |  |  |  |  |  |  |
| P100 | ${ }^{\text {A }}$ | Crasss | ${ }^{\text {P121 }}$ | A | crusss | ${ }^{131}$ | ${ }^{1}$ | crasss | ${ }^{\text {P13 }}$ | « |  |



## WAVEFORMS FOR DIAGRAM 18


(137)

(138)


display output＜${ }^{\text {® }}$ 〉

| ciear | sexim | ，omatiou | ¢emur | scation | ${ }_{\text {coman }}^{\text {Leanom }}$ | ${ }_{\text {chemema }}^{\text {cimem }}$ | saction | coso | comer | sockem | beamo |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Assembivail |  |  |  |  |  |  |  |  |  |  |  |
|  | ${ }^{\text {a }}$ | ${ }^{16}$ | ， |  |  | ${ }_{\substack{\text { axem } \\ \text { cex }}}$ |  |  |  |  |  |
|  |  |  | cis |  | \％ |  | $\substack{\begin{subarray}{c} { x 0 \\ \begin{subarray}{c}{c{ x 0 \\ \begin{subarray} { c } { c } } \\ {\hline} \end{subarray}} \\ {\hline} \end{subarray}$ |  | $\substack{\text { max } \\ \text { nem } \\ \text { nem }}$ |  |  |
|  | ${ }_{20}^{201}$ |  | Noe | gim | ${ }^{*}$ |  | $\begin{aligned} & \infty \\ & \substack{\infty\\ \\ } \end{aligned}$ | m | poso | $x_{0}^{\infty}$ |  |
| coin | cos |  | coick |  | ${ }_{\text {®a }}^{\text {® }}$ |  | coic | 告起 | come | $\begin{gathered} \text { em } \\ \text { en } \\ \hline \end{gathered}$ |  |
|  |  | ${ }^{2}$ |  |  | ${ }^{\circ}$ |  | \％ | d | mem |  | \％ |
|  |  | ${ }^{3 \times}$ | com | ¢ | $\cdots$ | coin | ， | a | $\begin{aligned} & \text { com } \\ & \substack{\text { con } \\ 0} \\ & \hline \end{aligned}$ |  |  |
| comm | ${ }^{\text {a }}$ | ＊ |  |  |  |  | ${ }_{\text {a }}$ | ${ }^{\text {a }}$ |  |  | ${ }_{\substack{18}}^{\text {m }}$ |
|  |  |  | cind | $\begin{aligned} & 80 \\ & 20 \\ & 20 \end{aligned}$ |  |  | ${ }^{2}$ | 起 | \％ro | $\underset{\substack{x \\ x}}{\substack{x}}$ | ${ }_{\text {n }}^{\sim}$ |
|  |  |  |  |  | $\underset{\substack{i k \\ n}}{i k}$ |  |  | an | 这 |  |  |
|  | 约 |  | ${ }_{\text {coile }}^{\text {fied }}$ | coic | ${ }^{\prime \prime \prime}$ |  | ${ }_{\sim}^{\text {\％}}$ |  | $\begin{aligned} & \text { Ueas } \\ & \text { Useat } \end{aligned}$ | $\underset{\substack{20 \\ 20}}{\substack{2 \\ 4}}$ | \％ |
|  |  |  | cin | 䢕 | \％ |  | ck |  |  | $\begin{aligned} & \text { én } \\ & \text { ex } \end{aligned}$ |  |
|  |  | wis | $\underbrace{}_{\substack{\text { min } \\ n m m a}}$ |  |  |  |  | $\begin{gathered} a \\ 4 \\ 4 \\ 4 \end{gathered}$ |  | $\begin{aligned} & \infty \\ & \substack { \infty \\ \begin{subarray}{c}{\infty\\ { \infty \\ \begin{subarray} { c } { \infty \\ } } \\ {\hline} \\ & \hline \end{aligned}$ |  |
|  | ${ }^{24}$ |  | ${ }_{\text {cosem }}$ |  | ${ }_{\frac{a}{a}}^{a}$ | cos |  | ${ }_{\substack{a \\ \hline}}$ | den |  | m |
| $\begin{gathered} \text { cond } \\ \text { che } \\ \text { chex } \\ \hline \end{gathered}$ | （ |  |  | ${ }^{m}$ |  | cos |  |  |  |  | \％ |
|  | 永㠰品 | \％ |  | ${ }^{x}$ | \％ | cosm |  | cim |  |  |  |
| ${ }_{\text {cores }}$ | ${ }_{\text {m }}{ }^{\text {H／}}$ | ${ }^{3}$ | cien | \％ |  | ase |  | \％ |  |  | a |
|  | ${ }_{24}^{24}$ | － |  |  |  | \％ | ¢ | \％ | cix |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  | $\stackrel{34}{24}$ | coms | fan | ${ }_{\text {am }}$ | comss | ） | ${ }^{24}$ | ${ }_{\text {comemsem }}$ | fite | ${ }^{\text {am }}$ | comse |




Figure 9－11．A17－High Voltage board．

| ait－high voltage board |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| cincer | sumber | Crmuer | Sumber | muner | Sumber | ${ }_{\text {cher }}^{\text {cinuer }}$ | sumber | Crimur | sumber | cimeur | Selter |
|  | 19 |  | ${ }^{18}$ | ${ }_{\text {chas }}^{\text {chas }}$ | ${ }^{18}$ | ${ }^{\circ} 9$ | ${ }^{1}$ |  |  |  |  |
| coile | 砣 |  | ${ }^{10}$ | ${ }_{\text {coser }}^{\text {cheat }}$ | ${ }^{18}$ | Riom | \％ |  |  |  |  |
| cise | 18 | cosic |  |  | ${ }_{18}^{18}$ |  | ${ }^{10}$ |  | \％ |  | 㫛 |
| coicter | 㫛 |  |  |  | ${ }^{18}$ |  |  |  |  |  | 翌 |
| coic | 㫛 | come | 㫛 | ， | 浆品 |  | 隹星 |  |  |  |  |
| coic | ${ }^{18}$ | ${ }_{\text {cosem }}$ | ${ }^{18}$ | 376 | ${ }_{18}$ |  | ${ }_{18}^{19}$ |  | 込 |  |  |
|  |  | cos chat | ${ }^{18}$ | ${ }^{208}$ | ${ }^{18}$ |  | ${ }_{\text {仿 }}^{18}$ |  |  |  | ${ }_{18}$ |
| coiso |  |  | 号 |  | ${ }^{18}$ |  | ${ }_{18}^{19}$ |  | ${ }^{18}$ | ${ }_{7235}$ | ${ }^{18}$ |
|  |  |  |  |  | 腮 |  | ${ }^{18}$ |  | ${ }^{18}$ |  | 㫛 |
| coick | 䎌 |  | ${ }^{18}$ | ${ }_{\substack{\text { a }}}^{\substack{2027}}$ | 㘶 |  |  |  | \％ | ${ }_{\text {vaxas }}$ | ${ }^{10}$ |
| coicle | 19 |  | ${ }^{18}$ |  |  |  |  |  |  |  |  |

waverorms for diagram 19





HIGH VOLTAGE SUPPLY \＆CRT DIAGRAM 19




| 7 HIGH VOLTAGE Boa |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {cioge }}$ | 隹 | ${ }^{18}$ | cmat | ${ }^{\text {PE }}$ | ${ }^{18}$ | osal |  | ${ }^{10}$ | ${ }^{2915}$ |  |  |
| cila | 茞 | 碗 | come | 80 | ${ }^{\text {ia }}$ | ${ }^{\text {R100 }}$ | ${ }^{\circ}$ | ${ }^{10}$ | cinc exis | ${ }^{50}$ |  |
| citer |  | ${ }_{8}^{8}$ |  |  | ${ }_{\substack{28 \\ 10 \\ 10}}$ |  | 退 | ${ }_{18}^{18}$ | cismo | cim | 唇 |
| cita | $\begin{aligned} & 30 \\ & \substack{300 \\ c i n} \end{aligned}$ | ${ }_{4}^{4 E}$ | ${ }_{\text {cosma }}^{\text {casmi }}$ | ${ }_{8}^{\text {\％}}$ | 品 | $\underset{\substack{\text { andes } \\ \text { alm }}}{\substack{\text { and }}}$ | ${ }_{\substack{3 E \\ 88}}$ |  |  |  |  |
| coic |  | ${ }^{12}$ |  | ${ }_{8}$ | coic |  | ${ }_{\sim}^{\circ}$ |  |  |  | ${ }^{\text {c }}$ |
|  |  | ${ }_{2}^{24}$ | cos |  | coic | ${ }_{\substack { \text { anfo } \\ \begin{subarray}{c}{1780{ \text { anfo } \\ \begin{subarray} { c } { 1 7 8 0 } }\end{subarray}}$ | ${ }_{\text {e }}$ |  | cime |  | cic |
|  |  | ${ }_{8}^{18}$ | csaso | 5 | ${ }_{2}$ |  |  | ${ }_{\substack{40 \\ i c}}^{\substack{c \\ i c}}$ |  | ¢ |  |
| coicle | ${ }_{6}$ | ${ }^{\text {a }}$ |  | ${ }^{*}$ | ${ }^{2}$ |  | 込 | ${ }_{\text {1a }}$ |  | ${ }_{\text {cof }}^{\text {ef }}$ | cos |
| coicce | ， |  |  | $\underset{\substack{78 \\ 20}}{\substack{0}}$ |  |  | ${ }_{\text {80 }}^{80}$ | ${ }_{1}^{1 a}$ | $\substack{\text { caise } \\ \text { nemo }}$ |  | $\underset{\substack { 3 \\ \begin{subarray}{c}{\text { cki }{ 3 \\ \begin{subarray} { c } { \text { cki } } }\end{subarray}}{ }$ |
|  | － | E | ， | － | $\begin{gathered} \text { 楽 } \end{gathered}$ |  |  | ${ }^{20}$ | （100） |  | 既 |
| cis | ${ }^{\text {成 }}$ | 3，${ }_{3}$ | ， | ${ }_{2}^{2 M}$ | ${ }_{\text {桭 }}$ |  |  | cick | cosic | $\underset{\substack{36 \\ i n \\ \text { in }}}{\substack{\text { and }}}$ |  |
| ciem | A | ${ }_{3}{ }^{20}$ | \％ | ${ }_{88}$ |  |  | ${ }_{3}$ | ${ }_{\text {at }}$ | ${ }^{25}$ | ${ }_{a c}^{a c}$ | ${ }_{3}$ |
|  | \％ | ${ }_{10}^{10}$ | ${ }^{10465}$ | 20 | $\underset{\substack{35 \\ 35}}{ }$ |  | ${ }_{\substack{20 \\ 30}}^{\substack{\text { che }}}$ | 近 | U16ea | 4 | 8 |
| cos | 込 | ， |  | coic | $\begin{aligned} & 3 \mathrm{E} \\ & \mathrm{BA}_{1} \end{aligned}$ |  | ， | ${ }_{\text {a }}$ | ${ }_{\text {unt }}$ | ${ }^{5}$ | ${ }_{8}$ |
|  |  |  |  | ${ }_{\text {cie }}^{\text {cie }}$ |  |  |  | 退 |  | ${ }_{70}^{10}$ | 10 |
| ${ }_{\text {cosi }}$ | ${ }_{2 E}^{24}$ | ${ }_{48}{ }_{4}$ |  |  |  |  | $\underset{\substack { 2 \times \\ \begin{subarray}{c}{\text { ck }{ 2 \times \\ \begin{subarray} { c } { \text { ck } } }\end{subarray}}{ }$ | 硈 |  | ${ }_{10}^{10}$ | ${ }_{4}^{4}$ |




## WAVEFORMS FOR DIAGRAM 20



PRESS GPIB TRANSMIT TO RING BELL


153 IS FIRST BYTE IN
svstem 10 ( 2 )


| ASSEmBLY A12 |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |  |  |
| (inco |  | $\begin{aligned} & 18 \\ & \substack{18 \\ 10} \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 30 \\ & \substack{3 c \\ 3 c \\ 30} \end{aligned}$ | $\begin{aligned} & 80 \\ & \substack{80 \\ 80 \\ 0} \end{aligned}$ |  |  | $\begin{gathered} \text { ge } \\ \text { or } \\ 0 \end{gathered}$ | $\begin{gathered} \text { Rras } \\ \hline 1820 \end{gathered}$ |  |  |
|  |  | , 10 | (crer | 30 |  | ${ }^{1082}$ | ${ }_{4 B}^{28}$ | ${ }^{\circ}$ | ${ }_{\text {ma32 }}$ |  | ${ }_{3}$ |
|  |  |  | ${ }_{\substack{\text { crea } \\ \text { crese }}}$ | ${ }_{3}^{30}$ | $\xrightarrow{7}$ | ${ }^{\text {Ls998 }}$ | ${ }^{10}$ | 4 M |  | $\begin{aligned} & 48 \\ & \hline 8 \\ & 48 \end{aligned}$ |  |
| (tas |  |  | citay | $\begin{aligned} & \substack{a c \\ 30 \\ 30 \\ 30} \end{aligned}$ | $\begin{gathered} \substack{7_{n}^{K} \\ n \\ n} \end{gathered}$ |  | $\underset{\substack{20 \\ 18}}{\substack{20}}$ | $\begin{gathered} 2 a \\ \substack{28} \\ \theta_{0} \end{gathered}$ |  |  | $\begin{gathered} \substack{\text { sick } \\ { }_{k}} \end{gathered}$ |
|  | cock |  |  | ${ }_{\substack{30 \\ 40}}^{\substack{6}}$ |  |  | $\begin{aligned} & 10 \\ & i c \\ & i c \end{aligned}$ | $\underset{\substack{\text { sin } \\ 6 \times 4 \\ \hline}}{ }$ | Tranz | ${ }_{\substack{80}}^{6}$ | ${ }_{\sim}$ |
|  | 2a |  |  | ¢ | ${ }_{\text {a }}^{\text {a }}$ | ${ }_{\text {a }}^{0}$ | $\stackrel{18}{4}$ | ${ }^{50}$ |  | $\underset{\substack{16 \\ i c \mid}}{\substack{2}}$ | , |
| $\substack{\text { cise } \\ \text { cise } \\ \text { case }}$ | $\begin{gathered} \substack{30 \\ 30 \\ 30} \end{gathered}$ | ${ }_{\substack{36 \\ 36}}^{\substack{36}}$ |  | $\begin{gathered} \begin{array}{l} 36 \\ 20 \\ 20 \end{array} \\ \hline \end{gathered}$ | ${ }_{8}^{8,}$ |  | ij | ${ }^{12}$ |  |  | ${ }_{3}^{30}$ |
|  | ${ }_{\substack{36 \\ 46}}$ | ${ }_{\substack{3 \% \\ 3 \\ \hline}}$ | ${ }_{\text {cose }}^{\text {cose }}$ | ${ }_{\substack{3 a \\ 30}}$ | $\underbrace{\text { gx }}_{\text {ck }}$ | $\substack{\text { Rincos } \\ \text { R10e }}$ | $\begin{aligned} & \text { N } \\ & \text { N } \end{aligned}$ | ${ }_{\substack{28 \\ 28}}$ | Cizat |  | $\substack{2 \\ 2 k}_{\substack{2}}$ |
|  | - | ¢ | crios | $i_{x}^{i v}$ | ${ }^{28}$ |  | $\begin{gathered} 2_{2 \times}^{2 \times} \\ 2 \times \end{gathered}$ | $\begin{gathered} 28 \\ 280 \\ 180 \end{gathered}$ |  | $\bar{\circ}$ |  |
|  | ${ }_{\substack{30 \\ 30}}^{\substack{20 \\ \\ \hline}}$ | ${ }_{\substack{3 \\ 4 \\ 4 \\ 0}}$ | (ention | $\begin{gathered} \text { 2K2 } \\ 2 \times \\ 2 \times \end{gathered}$ | 20 <br> 10 <br> 10 <br> 10 |  | $\begin{aligned} & 20 \\ & \substack{2 \times \\ 1 A} \end{aligned}$ | $\begin{aligned} & 10 \\ & \text { nk } \\ & 3 k \end{aligned}$ |  |  | $\underbrace{50}_{\substack{85 \\ 80}}$ |
|  | 30 36 30 | $\stackrel{4}{4}$ |  | $\begin{gathered} \text { 2K } \\ \substack{208 \\ 18} \end{gathered}$ | ¢ | $\substack{\begin{subarray}{c}{\text { arat } \\ \text { Rex }} }} \end{subarray}$ | $\underset{\substack{12 A \\ i A \\ i n}}{ }$ |  | cosk |  | $\begin{aligned} & \text { on } \\ & \\ & 0 \end{aligned}$ |
|  | $\underbrace{\substack{48 \\ 4}}_{\substack{38 \\ 48}}$ | $\underset{\substack{4 \\ 3 \\ 3}}{\substack{\text { d }}}$ |  | ${ }_{38}^{28}$ | $\underset{\substack{\text { on }}}{\substack{\text { on }}}$ |  | $\begin{gathered} 80 \\ 20 \\ 10 \end{gathered}$ | $\underset{\substack { 3 \mathrm{E} \\ \mathrm{sm} \\ \begin{subarray}{c}{3 \\ \hline{ 3 \mathrm { E } \\ \mathrm { sm } \\ \begin{subarray} { c } { 3 \\ \hline } } \\{\hline}\end{subarray}}{ }$ | cis | ${\underset{\Omega}{n}}_{\substack{0}}$ |  |
| 为cas | coc | $\underbrace{}_{\substack { \text { den } \\ \begin{subarray}{c}{\text { dec }{ \text { den } \\ \begin{subarray} { c } { \text { dec } } }\end{subarray}}$ |  | ${ }_{4}^{2 a}$ | ${ }_{8}^{8}$ |  | $\begin{aligned} & 10 \\ & 18 \\ & 18 \end{aligned}$ | ¢ |  | ${ }_{20}^{20}$ |  |
|  |  | ¢ | (1320 |  | ¢ |  | $\begin{gathered} 10 \\ \substack{10 \\ 30 \\ 3 k} \end{gathered}$ | ¢00 | vaios | ${ }_{3}{ }_{\text {3k }}$ | ${ }^{18}$ |
|  | ${ }_{\substack{4 c \\ i c}}^{\substack{c \\ i c}}$ |  | (inctiol |  |  |  | $\underset{\substack{\text { 3k } \\ 4 \times}}{\substack{\text { 3k }}}$ | ¢ |  | ${ }_{\substack{5 A \\ \text { ci }}}$ | $\underset{\text { \% }}{\substack{1+1 \\ \hline}}$ |
|  |  |  |  |  |  |  |  |  |  |  |  |
| OTHER PARTS |  |  |  |  |  |  |  |  |  |  |  |
|  | $\underset{\substack{2 m \\ 2 m}}{2 m}$ |  |  | ¢ | $\underset{\substack{\text { chasssis } \\ \text { chassis } \\ \text { chass }}}{ }$ |  | ${ }_{4}^{24}$ | $\substack{\text { chanssis } \\ \text { Ohassis }}$ |  | ${ }_{\text {u }}^{\text {u }}$ |  |
| Numb | ${ }_{3}^{20}$ | ctamss | jucem | ${ }_{s m}$ | conco | ${ }_{\substack{\text { prao } \\ \text { P120 }}}$ | ${ }_{54}$ | $\underset{\substack{\text { chassss } \\ \text { chmosis }}}{\text { chem }}$ |  | ${ }_{\substack{28 \\ 8.2}}^{2}$ |  |



## WAVEFORMS FOR DIAGRAM 21

BW LIMIT;
20 MHz ON TEST SCOPE


COMPOSITE FLAT-FIELD NEG-SYNC YIDEO SIGNAL AP PLIED TO CH 2 INPUT. TRIG SOURCE, CH 2; TRIG CPLG, TV: A TV COUPLING, ALT

(161)



MORE


TV CLAMP ON; CH 2 INVERT ON


6285-46
vioe ootion $1 人)$





COMPONENT NUMBER EXAMPLE

|  | $\overbrace{\text { A23 A2 R1234 }}^{\text {Component Number }}$ |
| :---: | :---: |
| Assembly | $-]_{\substack{\text { Subzssembiy } \\ \text { Number (fit sect) }}}^{\substack{\text { Schematcic } \\ \text { Cucrubuit } \\ \text { Numer }}}$ |

Static Sensitiva Devices
See Mantenance Section


WAVEFORMS FOR DIAGRAM 22 (cont)




LOW Voltage power supply 22

| circur | schan | Locaron | cipaur | sochem | Loochion | cincour | ${ }_{\text {L }}^{\text {cochem }}$ | bocaro | cincur | s．actem | ${ }^{\text {Loamapon }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ASSEMBLY A16 |  |  |  |  |  |  |  |  |  |  |  |
| ${ }^{\text {ciob }}$ | ${ }_{80}^{80}$ | ${ }^{4 B}$ | ${ }^{\text {cabss }}$ | ${ }^{\text {sm }}$ | ${ }_{20}^{2 F}$ | ${ }^{\text {R12 }}$ | ${ }^{60}$ | ${ }^{6 E}$ | ${ }^{\text {nam }}$ |  | ${ }^{\text {ef }}$ |
|  | ${ }_{\substack{\text { de } \\ 40}}^{\text {de }}$ |  | ${ }_{\text {chases }}^{\text {chase }}$ | $\stackrel{4}{4}$ | ${ }_{20}^{20}$ |  | ${ }_{\substack{56 \\ 20}}$ | ${ }^{20}$ |  | ${ }^{80}$ |  |
| coict |  | ¢¢ |  | $\underbrace{}_{\substack{\text { sk } \\ \text { ek }}}$ | ${ }_{\text {3H }}^{3}$ |  | ${ }_{2}^{2}$ | ${ }_{\substack{\text { ef } \\ \text { en }}}^{\text {en }}$ | $\underbrace{\text { nex }}_{\substack{\text { aner } \\ \text { nean }}}$ |  |  |
| coile | ${ }_{\substack{80 \\ 88}}$ |  |  | ¢ | ${ }_{\substack{56 \\ 80}}^{80}$ |  | $\substack{2 H \\ 3 H}_{2 H}$ | ${ }_{\substack{30 \\ 80}}$ |  |  |  |
| ${ }_{\text {coic }}$ | ${ }^{40}$ | ${ }^{20}$ | ${ }_{\text {charso }}$ | ${ }_{5}^{5 k}$ | ${ }^{36}$ | ${ }_{\text {r23 }}$ | ${ }^{20}$ | ${ }_{4 E}^{4 E}$ |  |  |  |
|  |  |  | carsi | ${ }_{8}$ | ${ }_{\substack{36 \\ s_{5} \\ \hline}}$ |  | ${ }_{\substack{20 \\ 30}}$ | ${ }_{\text {80 }}^{\text {80 }}$ |  | ${ }_{\substack{28 \\ 38}}$ | ${ }_{\substack{50 \\ s c}}$ |
| $cciad cata$ | ${ }_{\text {80 }}^{80}$ |  |  | ${ }_{\substack{s, 80}}^{8}$ |  |  | ${ }_{\substack{30 \\ 30}}$ | ${ }_{\text {¢ }}^{\text {em }}$ | T117 | ${ }_{3}$ | ${ }^{28}$ |
|  | ${ }_{\substack{4 c \\ 40}}^{\substack{c}}$ | ${ }_{\substack{3 A \\ 80}}$ | $\substack{\text { crases } \\ \text { craso }}$ | $\underbrace{\substack{\text { gen }}}_{\substack{s 6 \\ 36}}$ | ${ }_{\substack{3 \\{ }_{65} \\ \hline}}$ |  |  |  | ${ }_{\substack{\text { cisas } \\ \text { T145 }}}$ | ${ }_{\substack{20 \\ 10}}^{\substack{6\\}}$ | ${ }_{\substack{30 \\ 30 \\ 28}}$ |
|  | $\underbrace{}_{\substack{\text { ck } \\ \text { em }}}$ | ${ }_{\substack{16 \\ 16}}^{16}$ | EEOP | ${ }^{48}$ | ${ }_{8} 8$ | ${ }_{\substack{\text { R232 } \\ \text { R23 }}}^{\text {R2，}}$ | ${ }_{\substack{20 \\ 15}}^{20}$ | so | $\underset{\substack{1720 \\ \text { Tres }}}{ }$ | ${ }_{\substack{1 / 8}}^{\text {k }}$ | 碞10 |
|  | ${ }_{\text {¢0 }}$ | ${ }_{3}^{24}$ | ${ }^{6018}$ | ${ }_{4}$ | ${ }^{\circ}$ |  | ${ }_{\substack{36 \\ 48}}^{36}$ |  | U155 | ${ }^{2 \times}$ | ${ }^{6}$ |
| cick |  | 䞨 | ${ }_{\text {F289 }}$ | ${ }^{*}$ | $\cdots$ |  |  | ${ }_{\substack{10}}^{10}$ | citu |  | ${ }_{\substack{20 \\ 80}}^{20}$ |
| cos |  | ${ }^{\text {cis }}$ | ง102 | 10 | $\cdots$ |  |  | $\underbrace{\substack{0}}_{\substack{\text { cen }}}$ | cisme |  | cos |
| $\underbrace{}_{\substack { \text { cose } \\ \begin{subarray}{c}{\text { cass } \\ \text { casa }{ \text { cose } \\ \begin{subarray} { c } { \text { cass } \\ \text { casa } } }\end{subarray}}$ | ${ }_{\text {arn }}^{\text {arn }}$ | ， | ${ }_{\text {cosem }}$ | ， | ， |  | 兂 |  | Uneaid |  |  |
| ${ }_{\substack{\text { cros } \\ \text { cras }}}^{\substack{\text { cas }}}$ | ${ }_{\substack{28 \\ 88}}^{28}$ | ${ }_{\substack{86 \\ 68}}$ | （1288 | $\underbrace{}_{\substack{\text { sum } \\ \text { 3n }}}$ | ${ }_{\text {cex }}^{68}$ | $\substack{\text { Reas } \\ \text { Rass }}$ | ${ }_{\substack{16 \\ 48}}^{16}$ | ${ }_{\substack{2 \\ 88}}^{2}$ | Unema | $\underbrace{85}_{\substack{85 \\ 88}}$ | ${ }_{\substack{\text { ef } \\ \text { ef }}}^{\text {che }}$ |
|  |  | ${ }_{\substack{46 \\ 36}}$ |  |  | ${ }_{\substack{50}}^{\substack{50}}$ |  | ${ }^{18}$ | ${ }_{\substack{2 a \\ 2 a}}$ | Ueam |  | ${ }_{\substack{\text { ef } \\ \text { ef }}}^{\text {cos }}$ |
| coict | ¢ | $\underbrace{\text { cis }}_{\substack{\text { sf } \\ \text { sf }}}$ | Ls80 | ${ }_{50}$ | ${ }_{3 F}$ |  |  | ¢ | vitas |  | ${ }_{4 \times}^{4 E}$ |
| ciss | ${ }_{\substack{40 \\ 0}}^{40}$ | ${ }_{4}^{4 F}$ | ¢po | $\underbrace{88}_{\substack{28 \\ 88}}$ | ${ }_{8}^{8{ }_{8}^{8 A}}$ |  | ${ }_{\substack{\text { as } \\ \text { en }}}$ | $\underbrace{}_{\substack { \text { sem } \\ \begin{subarray}{c}{\text { Sex }{ \text { sem } \\ \begin{subarray} { c } { \text { Sex } } }\end{subarray}}$ | 270 | 10 |  |
| cosce | $\substack{\begin{subarray}{c} { e f \\ \begin{subarray}{c}{e f \\ \text { em }{ e f \\ \begin{subarray} { c } { e f \\ \text { em } } } \end{subarray}} \\{\hline} \end{subarray}$ | ¢ | P80 | ${ }_{5}{ }_{5}^{2 A}$ | ${ }^{4 A}$ |  | ¢ |  | cick |  | ${ }_{3}^{36}$ |
| ${ }_{\text {cass }}$ | ${ }^{\text {8N }}$ | ${ }^{3+}$ |  |  |  |  | ${ }_{\substack{38 \\ 88 \\ 88}}$ | ${ }_{\substack{\text { sig } \\ \text { sab }}}$ |  | ， | ${ }_{\substack{24 \\ 24 \\ 3}}$ |
| coick | ${ }_{\substack{18 \\ 80}}^{\text {cos }}$ | ${ }_{\substack{4 E \\ 4 E}}^{\substack{\text { cke }}}$ |  | ${ }^{15}$ | ${ }_{\substack{s c \\ 40}}^{\substack{\text { co }}}$ |  | ${ }_{\substack{28 \\ 56}}^{28}$ |  | cis |  | $\stackrel{4}{45}_{4}^{45}$ |
|  | ¢ | ${ }^{15}$ |  |  |  |  |  |  | Weer | ${ }^{3+14}$ | ${ }_{30}^{30}$ |
|  | ${ }_{\substack{\text { sin } \\ 80 \\ 80}}$ | coiz ${ }_{20}^{20}$ | 817 | ${ }_{3}$ | ${ }_{18}$ |  |  | $\underset{\substack { 4 . \\ \begin{subarray}{c}{\text { cic }{ 4 . \\ \begin{subarray} { c } { \text { cic } } }\end{subarray}}{ }$ |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |
| OTHER Parts |  |  |  |  |  |  |  |  |  |  |  |
| ${ }^{\text {F1000 }}$ | ${ }^{24}$ | asss | ${ }_{\substack{\text { ase } \\ 500}}$ | ${ }_{\substack{24 \\ 24}}^{4}$ |  | P102 |  | ${ }^{\text {crassss }}$ |  |  |  |
|  |  |  |  | ${ }_{\substack{4 \\ \text { ba }}}^{2 A}$ | cotas | ，1000 | ${ }^{24}$ | crusss | sites | ${ }_{\substack{36 \\ 14}}$ |  |



Low voltage regulators（23）

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|  | ${ }^{2}$ | 2 |  |  | \％ |  | $\begin{aligned} & \text { \% } \\ & \hline \end{aligned}$ |  |  |  |  |
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|  | ${ }_{6}$ | ces |  | ※im | \％ | ［ | ${ }^{2}$ | ${ }^{\text {anem }}$ |  |  |  |



POWER SUPPLY OVERCURRENT FAULT
IN THE EVENT OF A SHORTED LOAD ON AN UNREGLATED VOLTAGE SUPPLY, THE
POWER SUPPLY WIL GO INTO THE "CHIPP" MOEE IT CONTNUALLY STARTS UP AND



 IOENTFIED BY A MUCH SMALLER VOLTAGE WAVEFORM THAN
SECONDARY (SEE ACCOMPANYING WAVEFORM ILUSTRATON).

A SHORT ON THE +5 VD SUPPLY WILL BLOW FUSE F269.


| H | , J |
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|  |  |



## warning

turn off all power before attempting to SOLDER OR REPLACE COMPONENTS OR TO MAKE RESISTANCE MEASUREMENTS.

## EXERCISE E/A (ERROR AMPLIFIER)

TO VERIFY THE FUNCTIONAL OPERATION OF THE PWM (PULSE-WIDTH MODULATOR) COMPARATOR, EXERCISE THE ERROR AMPLIFIER OUTPUT AND THE SLOW START INPUT. USE THE NODE BETWEEN R845 AND R847 AS A SOURCE OF +1.6 V TO DRIVE THE COMP (PIN 9 ) AND SOFT START (PIN 8) INPUTS OF U233 IN THE FOLLOW. ING MANNER:

1. monitor the drive waveforms to the gates OF PWM FETS Q424 AND Q421 TO OBSERVE THE CHANGES THAT OCCUR.
2. CONNECT THE +1.6V LEVEL TO PIN 8 OF U233. CHECK THAT THE DRIVE WAVEFORM DUTY CYCLE DECREASES FROM APPROXIMATELY 45\% TO APPROXIMATELY $15 \%$. MEASURE THAT THE DC VOLTAGE ON PIN 9 OF U233 IS APPROXIMATELY 0.7 V MORE POSITIVE THAN PIN 8 OF U233.
3. MOVE THE +1.6 V LEVEL TO PIN 9 OF U233. CHECK THAT THE DRIVE WAVEFORM DUTY CYCLE AGAIN DECREASES FROM APPROXIMATELY 45\% TO APPROXIMATELY $15 \%$.





## REPLACEABLE MECHANICAL PARTS

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

When ordering parts, include the following information in your order: part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you conceming any change in part number.

Change information, if any, is located at the rear of this manual.

## ITEM NAME

In the parts list, an item name is separated from the description by a colon(i). Because of space limitations, an item name may sometimes appear as incomplete. For further Item name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

## FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

## INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentations system used in the description column.

## $\begin{array}{llllll}1 & 2 & 3 & 4 & 5 & \text { Name \& Description }\end{array}$

Assembly and/or component Attaching parts for assembly and/or component

END ATTACHING PARTS
Detail part of assembly and/or component Attaching parts for detall part

END ATTACHING PARTS
Parts of detail part
Attaching parts for parts or detail part
END ATTACHING PARTS
Attaching parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation.

Attaching parts must be purchased separately, unless otherwise specified.

## ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

## CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

| Mfr. Code | Manufacturer | Address | City, State, Zip Code |
| :---: | :---: | :---: | :---: |
| S3109 | FELLER | 72 VERONICA AVE UNIT 4 | SUMMERSET NJ 08873 |
| S3629 | SCHURTER AG H C/O PANEL COMPONENTS CORP | 2015 SECOND STREET | BERKELEY CA 94170 |
| TK0011 | OREGON FOUR-SLIDE PROD | RT 1 BOX 83G | YONCOLLA OR 97499 |
| TK0032 | POWELL ELECTRONICS | 411 FAIRCHILD DR | MT VIEW CA 94040 |
| TK0433 | PORTLAND SCREW CO |  |  |
| TK0435 | LEWIS SCREW CO | 4300 S RACINE AVE | CHICAGO IL 60609-3320 |
| TK0588 | UNIVERSAL PRECISION PRODUCTS | 1775 NW 216TH | HILLSBORO OR 97123 |
| TK0657 | CALORIC COLOR CO | 176 SADDLE RIVER AVE | GARFIELD NJ 07026-1914 |
| TK0860 | LABEL GRAPHICS | 6700 SW BRADBURY CT | PORTLAND OR 97224 |
| TK1159 | IMPROVED PRODUCTS | 3400 OLYMPIC STREET | SPRINGFIELD OR 97477 |
| TK1163 | POLYCAST INC | 9898 SW TIGARD ST | TIGARD OR 97223 |
| TK1165 | STEN MFG INC | 9702 85TH AVENUE N | MINNEAPOLIS MN 55369 |
| TK1167 | COLUMBINE PLASTICS CORP | 3195 BLUFF | BOULDER CO 80301-2103 |
| TK1169 | DIEMAKERS INC | $\begin{aligned} & 801 \text { 2ND ST } \\ & \text { PO BOX } 278 \end{aligned}$ | MONROE CITY MO 63456-1441 |
| TK1287 | ENOCH MFG CO | 14242 SE 82ND DR PO BOX 98 | CLACKAMAS OR 97015 |
| TK1302 | MOUNTAIN MOLDING | 606 SECOND STREET | BERTHOUD CO 80513 |
| TK1312 | LEMO USA INC | 335 TESCONI CIR PO BOX 11006 | SANTA ROSA CA 95406 |
| TK1359 | BLAIR HIRSCH CO | 9645 SW BEAVERTON HWY | BEAVERTON OR 97005 |
| TK1386 | PYRAMID ELECTRONICS SUPPLY INC | 9757 JUANITA DRIVE NE | KIRKLAND WA 98034 |
| TK1465 | BEAVERTON PARTS MFG CO | 1800 NW 216TH AVE | HILLSBORO OR 97124-6629 |
| TK1499 | AMLAN INC | 97 THORNWOOD RD | STAMFORD CT 06903-2617 |
| TK1585 | POFCO INC | 12805 SE CAPPS RD PO BOX 307 | CLACKAMAS OR 97015-8903 |
| TK1591 | EASTMAN PLASTICS INC | 4605 SW 180TH | ALOHA OR 97007 |
| TK1614 | STUCKEL R JCO | 1385 HOWARD ST | ELK GROVE VILLAGE IL 60007-2213 |
| TK1622 | TRIPLEL PRECISION | P OBOX 85 | TIMBER OR 97144 |
| TK1623 | STARKOR MFG | 3454 NE HWY 101 | LINCOLN CITY OR 97367 |
| TK1725 | GREENPAR CONNECTORS LTD | PO BOX 15 HARLOW | ESSEX CM20 2ER ENGLAND |
| TK1905 | PUGET CORP OF OREGON | 7440 S W BONITA | TIGARD OR 97223 |
| TK2394 | HARTZELL MANUFACTURING INC | 2516 WABASH AVENUE | ST PAUL MN 55114 |
| OB445 | ELECTRI-CORD MFG CO INC | 312 EAST MAIN ST | WESTFIELD PA 16950 |
| O.JRZ2 | BADGLEY MFG CO | 1620 NE ARGYLE | PORTLAND OR 97211 |
| OJR05 | TRIQUEST CORP | 3000 LEWIS AND CLARK HWY | VANCOUVER WA 98661-2999 |
| OJ260 | COMTEK MANUFACTURING OF OREGON (METALS) | POBOX 4200 | BEAVERTON OR 97076-4200 |
| OJ7N9 | MCXINC | 30608 SAN ANTONIO ST | HAYWARD CA 94544 |
| O.J9P9 | GEROME MFG CO INC | PO BOX 737 | NEWBERG OR 97132 |

## CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

| Mfr. Code | Manufacturer | Address | City, State, Zip Code |
| :---: | :---: | :---: | :---: |
| OKB00 | SCHRAMM PLASTIC FABRICATIORS | 7885 SW HUNZIKER | TIGARD OR 97223 |
| OKB01 | STAUFFER SUPPLY | 810 SE SHERMAN | PORTLAND OR 97214 |
| 04811 | PRECISION COIL SPRING CO | 10107 ROSE ST PO BOX 5450 | EL MONTE CA 91734 |
| 05006 | 20TH CENTURY PLASTICS INC | 3628 CRENSHAW BLVD PO BOX 30231 | LOS ANGELES CA 90030 |
| 06090 | RAYCHEM CORP | 300 CONSTITUTION DRIVE | MENLO PARK CA 94025-1111 |
| 07416 | NELSON NAME PLATE CO | 3191 CASITAS | LOS ANGELES CA 90039-2410 |
| 18565 | CHOMERICS INC | 77 DRAGON COURT | WOBURN MA 01801-1039 |
| 2K262 | BOYD CORP | $\begin{aligned} & 6136 \text { NE } 87 \text { th AVE } \\ & \text { PO BOX } 20038 \end{aligned}$ | PORTLAND OR 97220 |
| 22526 | DU PONT EI DE NEMOURS AND CO INC DU PONT ELECTRONICS DEPT | 515 FISHING CREEK RD | NEW CUMBERLAND PA 17070-3007 |
| 22670 | G M NAMEPLATE INC | 2040 15TH AVE WEST | SEATTLE WA 98119-2728 |
| 31918 | ITT SCHADOW INC | 8081 WALLACE RD | EDEN PRAIRIE MN 55344-2224 |
| 5Y400 | TRIAX METAL PRODUCTS INC DIV OF BEAVERTON PARTS MFG CO | 1800 216TH AVE NW | HILLSBORO OR 97124-6629 |
| 58050 | TEKA PRODUCTS INC | 45 SALEM ST | PROVIDENCE RI 02907 |
| 61857 | SAN-O INDUSTRIAL CORP | 85 ORVILLE DR PO BOX 511 | BOHEMIA LONG ISLAND NY 11716-2501 |
| 7X318 | KASO PLASTICS INC | 11015 A NE 39th | VANCOUVER WA 98662 |
| 70903 | COOPER BELDEN ELECTRONICS WIRE <br> AND CABLE <br> SUB OF COOPER INDUSTRIES INC |  |  |
| 73743 | FISCHER SPECIAL MFG CO | 111 INDUSTRIAL RD | COLD SPRING KY 41076-9749 |
| 76814 | NORTHERN ENGRAVING CORP | 803 S BLACK RIVER ST | SPARTA WI 54656-2221 |
| 78189 | ILLINOIS TOOL WORKS INC SHAKEPROOF DIV | ST CHARLES ROAD | ELGIN IL 60120 |
| 78488 | STACKPOLE CORP THE | 201 STACKPOLE ST | ST MARYS PA 15857-1401 |
| 80009 | TEKTRONIX INC | 14150 SW KARL BRAUN DR PO BOX 500 | BEAVERTON OR 97077-0001 |
| 83014 | HARTWELL CORP LOCKWELL DIVISION | 950 S RICHFIELD RD | PLACENTIA CA 92670-6732 |
| 85480 | BRADY W H CO <br> CORP HQ <br> INDUSTRIAL PRODUCTS DIV | 2221 W CAMDEN RD PO BOX 2131 | MILWAUKEE WI 53209 |
| 92101 | SCHULZE MFG | 50 INGOLD RD | BURLINGAME CA 94010-2206 |


| Fig. 8 Index No. | Tektronix Part No. | Seria Effective | No. Dscont | Oty | 12345 Name \& Description | M\&r. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1-1 | $\begin{aligned} & 334-7093-00 \\ & 378-0896-01 \end{aligned}$ |  |  | $\begin{aligned} & 1 \\ & 3 \end{aligned}$ | MARKER,IDENT:MARKED 2440 LENS,LIGHT:CLEAR LED | $\begin{aligned} & 22670 \\ & \text { TK1591 } \end{aligned}$ | ORDER BY DESC ORDER BY DESC |
| -2 | $\begin{aligned} & 366-1833-01 \\ & 377-0512-01 \\ & 377-0512-03 \end{aligned}$ | $\begin{aligned} & B 010100 \\ & \text { B011144 } \end{aligned}$ | B011143 | $\begin{aligned} & 1 \\ & 1 \\ & 1 \end{aligned}$ | KNOB:DOVE GRAY,0.25 ID X 0.392 OD X 0.466 H INSERT,KNOB: 0.172 ID X 0.28 OD $\times 0.64$, NYL INSERT,KNOB:0.128 ID X 0.37 OD $\times 0.67 \mathrm{~L}, \mathrm{XL}$ | OJR05 <br> OJR05 <br> TK1163 | ORDER BY DESC ORDER BY DESC ORDER BY DESC |
| -3 | 366-2036-00 |  |  | 3 | PUSH BUTTON:GY,0.206 SQ,1.445 H | OJR05 | ORDER BY DESC |
| -4 | 334-6726-00 |  |  | 1 | MARKER,IDENT:MKD CRT CONTROLS | 76814 | ORDER BY DESC |
| -5 | 105-0608-00 |  |  | 5 | ACTUATOR,SWITCH:MENU,ABS,SMOKE TAN | TK1163 | ORDER BY DESC |
| -6 | 200-2779-00 |  |  | 1 | COVER,TOP:TRIM | O.JR05 | ORDER BY DESC |
| -7 | 348-0740-00 |  |  | 2 | FOOT,CABINET:BOTTOM FRONT,PLASTIC ATTACHING PARTS | OJR05 | ORDER BY DESC |
| -8 | 211-0718-00 |  |  | 2 | SCREW,MACHINE:6-32 X 0.312,FLH,STL END ATTACHING PARTS | OKBO1 | ORDER BY DESC |
| -9 | 101-0006-00 |  |  | 1 | TRIM,DECORATIVE:FRONT ATTACHING PARTS | TK1163 | ORDER BY DESC |
| -10 | $211-0718-\infty$ |  |  | 6 | SCREW,MACHINE:6-32 X 0.312,FLH,STL END ATTACHING PARTS | OKB01 | ORDER BY DESC |
|  | 214-3374-01 |  |  | 1 | SPRING,FILTER: 1.32 L,CU-BE | TK0011 | ORDER BY DESC |
| -11 | 337-2926-03 |  |  | 1 | SHLD,IMPLOSION: $4.44 \times 3.67 \times 0.06$, CLEAR | TK1159 | ORDER BY DESC |
| -12 | 334-5581-03 |  |  | 1 | MARKER,IDENT:MKD , | 76814 | ORDER BY DESC |
| -13 | $\begin{aligned} & 334-6758-00 \\ & 334-6759-00 \end{aligned}$ |  |  | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | MARKER,IDENT:MKD STD CONNECTOR MARKER,IDENT:MKD PROBE POWER (OPTION 11 ONLY) | $\begin{aligned} & 76814 \\ & 76814 \end{aligned}$ | ORDER BY DESC <br> ORDER BY DESC |
| -14 | 334-5696-02 |  |  | 1 | MARKER,IDENT:MKD OPTION | 07416 | ORDER BY DESC |
| -15 | 348-0729-01 |  |  | 2 | FOOT,CABINET:W/CORD WRAP,REAR ATTACHING PARTS | OJR05 | ORDER BY DESC |
| -16 | 212-0154-00 |  |  | 4 | SCREW,MACHINE:8-32 X 1.125,PNH,STL END ATTACHING PARTS | OKB01 | ORDER BY DESC |
| -17 | 200-2961-00 |  |  | 1 | COVER,REAR:POLYCARBONATE,SMOKE TAN | TK1163 | ORDER BY DESC |
| -18 | 334-8202-00 |  |  | 1 | MARKER,IDENT:MKD HANDLE | 80009 | 334820200 |
| -19 | 367-0303-04 |  |  | 1 | HANDLE,CARRYNG:12.86 L,GRIP \& INDEX ATTACHING PARTS | OJR05 | ORDER BY DESC |
| -20 | 212-0144-00 |  |  | 2 | SCREW,TPG,TF:8-16 X 0.562 L,PLASTITE END ATTACHING PARTS | OKB01 | ORDER BY DESC |
| -21 | 337-2395-00 |  |  | 2 | SHIELD,ELEC:HANDLE ATTACHING PARTS | TK1614 | ORDER BY DESC |
| -22 | 213-0138-00 |  |  | 4 | SCREW,TPG,TF:4-24 X 0.188,TYPE B,PNH,STL END ATTACHING PARTS | TK0435 | TAPPING SCREW |
| -23 | 437-0139-00 |  |  | 1 | CABINET,SCOPE: | 0.99P9 | ORDER BY DESC |
| -24 | 348-0792-01 |  |  | 1 | GASKET:ELECTRICAL SHIELD,34.0 | 18565 | ORDER BY DESC |
| -25 | 211-0730-00 |  |  | 2 | SCR,ASSEM WSHR:6-32 X 0.375,PNH,STL,T15 | OKB01 | ORDER BY DESC |

Fig. \& Tektronix Serial No. Oty 12345 Name \& Description Mfr.
Index Part No. Effective Dscont





| Fig. $\&$ Index No. | Tektronix Part No. | Seria Effective | No. Dscont | Oty | 12345 Name \& Description | Mfr. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 2-1 | 441-1563-01 |  |  | 1 | CHASSIS,SCOPE:TOP | TK1163 | ORDER BY DESC |
| -2 | 426-1864-01 |  |  | 1 | FRAME,CRT: ATTACHING PARTS | TK1169 | ORDER BY DESC |
| -3 | 213-0914-00 |  |  | 4 | SCREW,TPG,TR:6-32 X 0.75,FLH,STL | OKBO1 | ORDER BY DESC |
| -4 | 211-0713-00 |  |  | 4 | SCREW,MACHINE:6-32 X 1.25,FLH,STL END ATTACHING PARTS | OKBO1 | ORDER BY DESC |
| -5 | 343-0992-00 |  |  | 2 | RETAINER,CRT:CLEAR,PLASTIC | TK1163 | ORDER BY DESC |
| -6 | 343-0993-00 |  |  | 2 | RETAINER,CRT:BLACK,PLASTIC | TK1163 | ORDER BY DESC |
| -7 | 348-0731-01 |  |  | 1 | GASKET:CRT,POLYETHYLENE | TK1159 | ORDER BY DESC |
| -8 | 378-0204-00 |  |  | 1 | REFLECTOR,LIGHT:INT SCALE ILLUMINATION | $7 \times 318$ | ORDER BY DESC |
| -9 |  |  |  | 1 | CKT BD ASSY:SGALE ILLUM (SEE A18 REPL) |  |  |
| -10 | 366-1833-01 |  |  | 6 | KNOB:DOVE GRAY,0.25 ID X 0.392 OD X 0.466 H | OJR05 | ORDER BY DESC |
| -11 | 366-0555-00 |  |  | 3 | KNOB: | TK1163 | ORDER BY DESC |
| -12 | 366-2017-00 |  |  | 31 | PUSH BUTTON:0.18 SQ X 0.644 H,IVORY GY | 0.1R05 | ORDER BY DESC |
| -13 |  |  |  | 1 | CKT BD ASSY:FRONT PANEL (SEE A14 REPL) ATTACHING PARTS |  |  |
| -14 | 211-0304-00 | B010100 | 8013221 | 4 | SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,T9 | OKBO1 | ORDER BY DESC |
|  | 211-0337-00 | B013222 |  | 4 | SCREW,MACHINE:4-40 X 0.25,PNH,SST (STANDARD ONLY) | TK0435 | ORDER BY DESC |
|  | 211-0304-0 | B010100 | B010116 | 4 | SCR,ASSEM WSHR:4-40 $\times 0.312$, PNH,STL, T9 | OKBO1 | ORDER BY DESC |
|  | 211-0337-0 | B010117 |  | 4 | SCREW,MACHINE:4-40 X 0.25,PNH,SST (2440M ONLY) <br> END ATTACHING PARTS | TK0435 | ORDER BY DESC |
|  | 352-0641-0 |  |  | 1 | HOLDER,LED:FIVE,POLYURETHANE,BLACK | TK1905 | ORDER BYDESC |
| -15 | 377-0550-01 |  |  | 2 | INSERT,KNOB:0.178 ID $\times 0.37$ OD $\times 0.64$ | TK1167 | ORDER BY DESC |
| -16 | 210-0590-00 |  |  | 3 | NUT,PLAIN,HEX:0.375-32 X 0.438 BRS | 73743 | 28269-402 |
| -17 | 210-0012-00 |  |  | 3 | WASHER,LOCK:0.384 ID,INTL,0.022 THK,STL | 78189 | 1220-02-00-0541 |
| -18 | 214-3373-00 |  |  | 3 | SPRING,GROUND:PHOSPHOR-BRONZE | 92101 | ORDER BY DESC |
| -19 | 377-0383-0 |  |  | 4 | INSERT,KNOB:0.178 ID 0.78 OD X 1.0,PLSTC | TK1163 | ORDER BY DESC |
| -20 | 129-0938-00 |  |  | 4 | SPACER,POST:1.102 L,4-40 EA END,AL | TK1622 | ORDER BYDESC |
| -21 | 354-0465-01 |  |  | 1 | RING,MOUNTING:6.065 X 4.16,BRASS | OJ260 | ORDER BY DESC |
| -22 | з33-3378-00 |  |  | 1 | PANEL,FRONT:STANDARD (STANDARD ONLY | 07416 | ORDER BY DESC |
|  | 333-3379-00 |  |  | 1 | PANEL,FRONT:TV TRIGGER (OPTION 05 ONLY) | 07416 | ORDER BY DESC |
| -23 | 386-4728-01 |  |  | 1 | SUBPANEL,FRONT: <br> ATTACHING PARTS | TK2394 | ORDER BY DESC |
|  | 210-0046-0 |  |  | 4 | WASHER,LOCK:0.261 ID,INTL,0.018 THK,STL | 78189 | 1214-05-00-0541 |
|  | 210-0583-00 |  |  | 4 | NUT,PLAIN,HEX: $0.25-32 \times 0.312$, BRS END ATTACHING PARTS | 73743 | 2X-20319-402 |
|  | 131-3772-00 |  |  | 2 | CONN,BOX:PCB; FEMALE,STR, $1 \times 4,0.1$ CTR | 22526 | 76308-004 |
| -24 | 348-0792-01 |  |  | 1 | GASKET:ELECTRICAL SHIELD, 34.0 L | 18565 | ORDER BY DESC |
| -25 | 175-4593-01 |  |  | 1 | CA ASSY,SP,ELEC:2,22 AWG,3.5 L,RIBBON | OJ7N9 | ORDER BY DESC |
| -26 | 384-0837-00 |  |  | 1 | EXTENSION SHAFT:13.470 L X $0.250 \times 0.300$ | TK1163 | ORDER BY DESC |
| -27 | 366-1767-00 |  |  | 1 | PUSH BUTTON:BLACK,YELLOW INDICATOR | 31918 | 160597 |
| -28 | 407-2904-02 |  |  | 1 | BRACKET,EXT SFT:POWER,POLYCARBONATE ATTACHING PARTS | TK1163 | 407-2904-02 |


| Fig． 8 Index No． | Tektronix Part No． | Serial No． Effective Dscont | 12345 Name \＆Description | Mfr． Code | Mfr．Part No． |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 2－29 | 211－0718－00 | 1 | SCREW，MACHINE： $6-32 \times 0.312$, FLH，STL END ATTACHING PARTS | OKBO1 | ORDER BY DESC |
|  | 626－0009－00 | 1 | SHIELD，CRT ASSY： | 0J9P9 | ORDER BY DESC |
| －30 | 337－2931－01 | 1 | ．SHIELD，CRT： | 0．J9P9 | 337－2931－01 |
| －31 | 214－0291－0 | 2 | ．CONTACT，ELEC：CRT CONNECTOR，CU BE ATTACHING PARTS | 04811 | ORDER BY DESC |
| －32 | 211－0324－00 | 2 | ．SCR，ASSEM WSHR： $4-40 \times 0.188, \mathrm{PNH}, \mathrm{T} 9$ | OKB01 | ORDER BY DESC |
| －33 | 210－0586－00 | 2 | ．NUT，PL，ASSEM WA：4－40 X 0．25，STL END ATTACHING PARTS | TK0435 | ORDER BY DESC |
| －34 | 334－1379－00 | 1 | ．MARKER，IDENT：MKD HI VACUUM | 07416 | ORDER BY DESC |
| －35 | 334－1951－00 | 1 | ．MARKER，IDENT：MKD WARNING，CRT VOLTAGES | TK0860 | ORDER BY DESC |
| －36 | $\begin{aligned} & 195-6851-01 \\ & 195-8410-00 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | ．LEAD，ELECTRICAL：BRAIDED，1．65 L ．LEAD，ELECTRICAL：22 AWG， 1.65 L <br> ATTACHING PARTS | TK1386 <br> TK1386 | ORDER BY DESC ORDER BY DESC |
| －37 | 211－0324－00 | 1 | ．SCR，ASSEM WSHR：4－40 $\times 0.188, \mathrm{PNH}, \mathrm{T9}$ | OKB01 | ORDER BY DESC |
| －38 | 210－0586－00 | 1 | ．NUT，PL，ASSEM WA：4－40 X 0．25，STL END ATTACHING PARTS | TK0435 | ORDER BY DESC |
| －39 | －－ー－ー－－ | 1 | FLEX CKT ASSY：GPIB，POLYMIDE （SEE A15 REPL） |  |  |
| －40 | 175－9359－01 | 1 | FLEX CKT ASSY：CRT CONTROLS，POLYMIDE | 80009 | 175935901 |
| －41 | 386－0867－00 | 1 | PLATE，MOUNTING：LED ATTACHING PARTS | TK1302 | ORDER BY DESC |
| －42 | 211－0304－00 | 4 | SCR，ASSEM WSHR：4－40 $\times 0.312$, PNH，STL，T9 END ATTACHING PARTS | OKB01 | ORDER BY DESC |
| $-43$ | －－ー－－－－－ | 1 | COIL，TUBE DEFL：（SEE L1000 REPL） |  |  |
|  | 348－0762－00 | 1 | GROMMET，PLASTIC：NATURAL，ROUND，0．54 ID | 0．JR05 | ORDER BY DESC |
| －44 | 175－9271－00 | 1 | CA ASSY，HV：DESCRETE，；SDI，14，24 AWG，9．5 L | 0.77 N 9 | ORDER BY DESC |
| －45 | 200－0917－01 | 1 | COVER，CRT SKT：2．052 OD $\times 0.291$ H，PLASTIC | O．JR05 | ORDEA BY DESC |
| －46 | 441－1562－00 | 1 | CHASSIS，SCOPE：REAR ATTACHING PARTS | 0．J9P9 | ORDER BY DESC |
| －47 | 213－0942－00 | 4 | SCREW，TPG，TR：6－32 X 0．75，TYPE TT，PNH，STL END ATTACHING PARTS | OKB01 | ORDEA BY DESC |
| －48 | －－ーーー－－－ | 1 | FILTER，RFI：（SEE FL1000 REPL） ATTACHING PARTS |  |  |
| －49 | 211－0304－00 | 2 | SCR，ASSEM WSHR：4－40 $\times 0.312$, PNH，STL，T9 END ATTACHING PARTS | OKB01 | ORDER BY DESC |
| －50 | 200－2264－00 | 1 | CAP，FUSEHOLDER：3AG FUSES， | S3629 | FEK 0311666 |
| －51 | 204－0832－00 | 1 | BODY，FUSEHOLDER：3AG \＆ $5 \times 20 \mathrm{MM}$ FUSES | S3629 | 0311673 （FEU M |
|  | 195－5569－00 | 1 | LEAD，ELECTRICAL：18 AWG，3．0 L，8－0 | OJ7N9 | ORDER BY DESC |
|  | 196－2828－01 | 1 | LEAD，ELECTRICAL：DESCRETE，；CUT， 1,18 AWG | OJ7N9 | ORDER BY DESC |
|  | 196－2830－00 | 1 | LEAD，ELECTRICAL：18 AWG，4．5 L，8－01 | OJ7N9 | ORDER BY DESC |
|  | $196-2831-00$ | 1 | LEAD，ELECTRICAL： 18 AWG， $4.75 \mathrm{~L}, 8-02$ | 0J7N9 | ORDER BY DESC |
|  | $196-2832-00$ | $1$ | LEAD，ELECTRICAL：18 AWG，5．25 L，8－19 | OJ7N9 | ORDER BY DESC |
|  | $196-2833-00$ | $1$ | CA ASSY，SP：DESCRETE；；PSC，1，18 AWG，4．75 L | 0．J7N9 | ORDER BY DESC |
|  | 276－0573－00 | 2 | CORE，EM：TOROID，FERRITE <br> （ADDED TO 195－5569－00 \＆196－2828－01） | 78488 | $57-0972$ |
| －52 | －－－－－－＊－ | 1 | CA ASSY，SP：RIBBON，GP｜B；24，28 AWG，7．0 L （SEE J1907 REPL） <br> ATTACHING PARTS |  |  |
| －53 | 129－1107－00 | 2 | SPACER，POST：0．98 L，6－32 EXT \＆M3．5 INT THD | TK1287 | 129－1107－00 |


|  <br> Index <br> No. | Tektronix <br> Part No. | Serial No. <br> Effective <br> Dscont | Qty | 12345 Name \& Description | Mfr. | Mifr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Code |  |  |  |  |  |  |


| Fig．${ }^{\text {a }}$ <br> Index No． | Tektronix Part No． | Serial No． Effective Dscont | Qty | 12345 Name \＆Description | Mrr． Code | Mfr．Part No． |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 3－1 | －ーーーーーーー |  | 1 | CKT BD ASSY：TIME BASE DSPLY（SEE A11 REPL） ATTACHING PARTS |  |  |
| －2 | 213－0927－0 |  | 3 | SCREW，TPG，TR： $6-32 \times 0,875$ ，TYPE TT，PNH，STL END ATTACHING PARTS | OKB01 | ORDER BY DESC |
| －3 | －－－－－－－－ |  | 1 | CKT BD ASSY：PROCESSOR（SEE A12 REPL） |  |  |
| －4 | 175－9353－01 |  | 1 | CA ASSY，SP：COAXIAL；；RFP，2，50 OHM COAX，15．0L （OPTION 05 ONLY） | O．J7N9 | ORDER BY DESC |
| －5 | 343－0150－00 |  | 1 | CLAMPTIEDOWN：PLASTIC （OPTION 05 ONLY） | 85480 | TYPE A－30 |
| －6 | 343－0549－00 |  | 2 | STRAP，TIEDOWN，E：0．098 W X 4.0 L，ZYTEL （OPTION 05 ONLY） | TK1499 | HW－047 |
| －7 | －－－－－－－－ |  | 1 | SKT，PL－IN ELEK：（SEE A12XU470 REPL） |  |  |
| －8 | －－－－－－ |  | 1 | MICROCKT，DGTL：（SEE A12U470 REPL） |  |  |
| －9 | 214－3637－01 |  | 1 | HT SK，MICROCKT：ALUMINUM，BLACK ANODIZE | TK1359 | MCHS－68－1．2 |
| －10 | －－－－ー－ー－ |  | 1 | CKT BD ASSY：SIDE（SEE A13 REPL） ATTACHING PARTS |  |  |
| －11 | 213－0927－00 |  | 1 | SCREW，TPG，TR： $6-32 \times 0.875$, TYPE TT，PNH，STL END ATTACHING PARTS | OKB01 | ORDER BY DESC |
| －12 | －－－－－－－－ |  | 1 | CKT BD ASSY：MAIN（SEE A10 REPL） ATTACHING PARTS |  |  |
| －13 | 211－0730－00 |  | 1 | SCR，ASSEM WSHR：6－32 $\times 0.375, \mathrm{PNH}, \mathrm{STL}, \mathrm{T} 15$ | OKB01 | ORDER BY DESC |
| －14 | 210－0586－00 |  | 2 | NUT，PL，ASSEM WA：4－40 $\times 0.25, S T L$ END ATTACHING PARTS MAIN BOARD INCLUDES： | TK0435 | ORDER BY DESC |
| －15 | －－－－－－－－ |  | 2 | SKT，PL－IN ELEK：（SEE A10XU370，XU470 REPL） |  |  |
| －16 | －－ーーー－－－ |  | 2 | INTEGRATED CKT：（SEE A10U370，U470 REPL） |  |  |
| －17 | 214－3637－01 |  | 2 | ．HT SK，MICROCKT：ALUMINUM，BLACK ANODIZE | TK1359 | MCHS－68－1．2 |
| －18 | －－－－－－－ |  | 2 | SKT，PL－IN ELEK：（SEE A10XU340，XU440 REPL） |  |  |
| －19 | －－－－－－－－ |  | 2 | MICROCKT，HYBRID：（SEE A10U340，440 REPL） ATTACHING PARTS |  |  |
| －20 |  |  |  |  |  |  |
|  | $211-0324-00$ |  | $2$ | ．SCR，ASSEM WSHR： $4-40 \times 0.188$, PNH，T9 | OKB01 | ORDER BY DESC |
|  | 129－0985－0 |  | 2 | ．SPACER，POST：0．350 L，4－40 THRU，STL，0．25HEX | TK1287 | ORDER BY DESC |
|  | 214－2270－00 |  | 2 | ．CONTACT，ELEC：CRT TO SHLD，CU－BE END ATTACHING PARTS | 5 Y 400 | ORDER BY DESC |
| －21 | －－－－－－－－ |  | 2 | SKT，PL－IN ELEK：（SEE A10XU350，XU450 REPL） |  |  |
| －22 | －－－－－－－－ |  | 2 | MICROCKT，HYBRID：（SEE A10U350，U450 REPL） ATTACHING PARTS |  |  |
| －23 | 210－0586－00 |  | 8 | ．NUT，PL，ASSEM WA：4－40 X 0．25，STL END ATTACHING PARTS | TK0435 | ORDER BY DESC |
| －24 | －－ー－ー－－－ |  | 2 | SKT，PL－IN ELEK：（SEE A10XU100，XU150 REPL） |  |  |
| －25 | －－－－－－－－ |  | 2 | MICROCKT，LINEAR：（SEE A10U100，U150 REPL） ATTACHING PARTS |  |  |
| －26 | 210－0586－00 |  | 8 | ．NUT，PL，ASSEM WA：4－40 X 0．25，STL END ATTACHING PARTS | TK0435 | ORDER BY DESC |
| －27 | 337－3031－00 |  | 2 | ．SHIELD，ELEC：PRE－AMP ATTACHING PARTS | TK1585 | ORDER BY DESC |
| －28 | 211－0324－00 |  | 4 | ．SCR，ASSEM WSHR： $4-40 \times 0.188$, PNH，T9 END ATTACHING PARTS | OKB01 | ORDER BY DESC |


| Fig．\＆ Index No． | Tektronix Part No． | Serial <br> Effective | No． Dscont | Qty | 12345 Name \＆Description | Mfr． Code | Mrr．Part No． |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 3－29 | 129－0985－00 |  |  | 4 | ．SPACER，POST：0，350 L，4－40 THRU，STL，0．25HEX | TK1287 | ORDER BY DESC |
| －30 | －ーーーーー－－ |  |  | 1 | SKT，PL－IN ELEK：（SEE A10XU420 REPL） |  |  |
| －31 | $386-4699-00$ |  |  | $\begin{aligned} & 2 \\ & 1 \end{aligned}$ | MICROCKT，HYBRID：（SEE A10U320，U420 REPL） ．BAR，SUPPORT：ATTENUATOR，AL ATTACHING PARTS | TK1169 | ORDER BY DESC |
| －32 | $\begin{aligned} & 136-0252-07 \\ & 210-0586-00 \end{aligned}$ |  |  | $\begin{aligned} & 32 \\ & 4 \end{aligned}$ | ．SOCKET，PIN TERM：SINGLE，PCB，T／G， 0.030 H ．NUT，PL，ASSEM WA：4－40 $\times 0.25$, STL END ATTACHING PARTS | $\begin{aligned} & 22526 \\ & \text { TKO435 } \end{aligned}$ | $\begin{aligned} & \text { 75060-012 } \\ & \text { ORDER BY DESC } \end{aligned}$ |
| －33 | －－ーー－－－－ |  |  | 2 | ATTENUATOR，VAR：（SEE A10AT300，AT400 REPL） ATTACHING PARTS |  |  |
| －34 | 211－0304－00 |  |  | 4 | ．SCR，ASSEM WSHR：4－40×0．312，PNH，STL，T9 END ATTACHING PARTS | OKB01 | ORDER BY DESC |
| －35 | 351－0677－01 |  |  | 2 | ．GUIDE，MAG CATCH：BLACK，PLOYCARBONATE | TK1905 | 351－0677－01 |
| －37 | 361－0382－00 |  |  | 6 | ．SPACER，PB SW：0．275 L，BROWN POLYCARB | OJR05 | ORDER BY DESC |
| －38 | $\begin{aligned} & 214-0973-00 \\ & 162-0533-\infty \end{aligned}$ | $\begin{aligned} & B 010100 \\ & B 012568 \end{aligned}$ | B012567 | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | ．HEAT SINK，XSTR：TO－92，CU BE ．INSUL SLVG，ELEC：HT SHRINK， 0.25 ID | 80009 <br> 06090 | $\begin{aligned} & 214097300 \\ & \text { VERSAFIT } \end{aligned}$ |
| －39 | 386－4735－01 |  |  | 1 | ．PLATE，CMPNT MTG：ALUMINUM ATTACHING PARTS | TK1169 | ORDER BY DESC |
| －40 | 213－0006－00 |  |  | 2 | ．SETSCREW：8－32 X 0．188，STL END ATTACHING PARTS | TK0433 | ORDER BY DESC |
| －41 | －－ー－ー－－－ |  |  | 2 | ．CONN，RF JACK：：BNC，；50 OHM，FEMALE，STR （SEE A10J2001，A10J2002 REPL） |  |  |
| －42 | －－－－－－－－ |  |  | 1 | ．TERMINAL，CAL： <br> （SEE A10J2006 REPL） |  |  |
| －43 | －－－－－－－－ |  |  | 1 | CKT BD ASSY：GAIN CELL（SEE A30，A31，A32，A33） |  |  |


| Fig. \& | Tektronix | Serlal No. | Qty | 12345 | Name \& Description |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Index | Part No. | Effective Dscont |  | Mfr. <br> No. |  |





| Fig. 8 Index No. | Tektronix Part No. | Serial Effective | INo. Dscont | Oty | 12345 Name \& Description | Mr. Code | Mrr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 4-1 | 337-3163-01 |  |  | 1 | SHIELD,ELEC:LV,UPPER ATTACHING PARTS | 0.J9P9 | OORDER BY DESCT |
| -2 | 211-0730-00 |  |  | 7 | SCR,ASSEM WSHR:6-32 $\times 0.375$, PNH,STL,T15 | OKB01 | ORDER BY DESC |
| -3 | 211-0730-00 |  |  | 2 | SCR,ASSEM WSHR:6-32 $\times$ 0.375,PNH,STL,T15 | OKB01 | ORDER BY DESC |
| -4 | 129-0474-0 |  |  | 2 | SPACER,POST:0.92 L,0.24 DIA STEEL, 0.250 HEX END ATTACHING PARTS | TK0588 | ORDER BY DESC |
| -5 | 334-4759-00 |  |  | 1 | MARKER,IDENT:MKD SHIELDS INVERTER | 07416 | ORDER BY DESC |
| -6 | ----- |  |  | 1 | SWITCH,THRMSTC: (SEE A16S1020 REPL) ATTACHING PARTS |  |  |
| -7 | 211-0730-0 |  |  | 2 | SCR,ASSEM WSHR:6-32 X 0.375,PNH,STL,T15 END ATTACHING PARTS | OKB01 | ORDER BY DESC |
| -8 | 343-0527-00 |  |  | 7 | RETAINER,XSTR:POLYCARBONATE ATTACHING PARTS | TK1163 | ORDER BY DESC |
| -9 | 211-0730-00 |  |  | 7 | SCR,ASSEM WSHR:6-32 X 0.375,PNH,STL,T15 END ATTACHING PARTS | OKB01 | ORDER BY DESC |
| -10 | 342-0676-0 |  |  | 7 | INSULATOR,XSTR:SILICON RUBBER,0.006 THK | 2K262 | ORDER BY DESC |
| -11 | 337-3196-00 |  |  | 1 | SHIELD,ELEC:FARADAY,POLYMIDE | 80009 | 337319600 |
| -12 | 407-2843-01 |  |  | 1 | BRACKET,XSTR:ALUMINUM ATTACHING PARTS | 0J9P9 | ORDER BY DESC |
| -13 | 210-0586-00 |  |  | 7 | NUT,PL,ASSEM WA:4-40 X 0.25,STL END ATTACHING PARTS | TK0435 | ORDER BY DESC |
| -14 |  |  |  | 1 | CKT BD ASSY:LVPS (SEE A16 REPL) |  |  |
| -15 | 131-0608-00 |  |  | 1 | .TERMINAL,PIN:PRESSFIT/PCB,;MALE,STR | 22526 | 48283-018 |
|  | 166-0165-00 |  |  | 2 | .SPACER,SLEEVE:0.35 L X 0.055 ID,CERAMIC | 80009 | 166016500 |
|  | 175-9230-01 |  |  | 1 | .CA ASSY,SP:RIBBON,;CPR,10,26 AWG,0.1 CTR (LVPS TO HV BOARDS) | O.J7N9 | ORDER BY DESC |
| -16 | 441-1573-01 |  |  | 1 | CHASSIS,SCOPE:CENTER | OJ9P9 | ORDER BY DESC |
| -17 | 348-0897-00 |  |  | 1 | GROMMET,PLASTIC:1.534 ID,BLACK,RECT | TK1163 | ORDER BYDESC |
| -18 | 337-1925-00 | B010100 | B012402 | 1 | SHIELD,ELEC:CIRCUIT BOARD | 0J9P9 | ORDER BY DESC |
|  | 337-3682-00 | B012403 |  | 1 | SHIELD,ELEC:HIGH VOLTAGE POWER SUPPLY (STANDARD ONLY) | 0J9P9 | ORDER BY DESC |
|  | $337-1925-00$ | B010100 | B010107 | $1$ | SHIELD,ELEC:CIRCUIT BOARD | OJ9P9 | ORDER BY DESC |
|  | $337-3682-00$ | B010108 |  | $1$ | SHIELD,ELEC:HIGH VOLTAGE POWER SUPPLY (2440M ONLY) | OJ9P9 | ORDER BY DESC |
| -19 | 334-5583-00 | B010100 | B012402 | 1 | .MARKER,IDENT:MKD CAUTION HIGH VOLTAGE (STANDARD ONLY) | 07416 | ORDER BY DESC |
|  | 334-5583-00 | B010100 | B010107 | 1 | .MARKER,IDENT:MKD CAUTION HIGH VOLTAGE (2440M ONLY) <br> ATTACHING PARTS FOR SHIELD | 07416 | ORDER BY DESC |
| -20 | 211-0730-00 |  |  | 1 | SCR,ASSEM WSHR:6-32 X 0.375,PNH,STL,T15 END ATTACHING PARTS | OKB01 | ORDER BY DESC |
| -21 | 129-0474-00 |  |  | 1 | SPACER,POST:0.92 L,0.24 DIA STEEL, 0.250 HEX | TK0588 | ORDER BY DESC |
| -22 |  |  |  | 1 | CKT BD ASSY:HIGH VOLTAGE (SEE A17 REPL) |  |  |
| -23 | -------- |  |  | 1 | FAN,TUBEAXIAL: (SEE B1000 REPL) |  |  |
| -24 | 131-0707-00 |  |  | 2 | CONTACT,ELEC:22-26 AWG,BRS \& CU BE | 22526 | 47439-000 |
| -25 | 204-0805-00 |  |  | 1 | CONN BODY,PLUG:HOLDE:,MINI PV | 22526 | 65039-035 |
| -26 | 129-1044-0 |  |  | 1 | SPACER,POST:0.575 L,6-32 INT THRU,STL | TK0588 | ORDER BY DESC |


| Fig. 8 Index No. | Tektronlx Part No. | Serial Effective | No. Dscont | Oty | 12345 Name \& Description | Mfr. Code | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | STANDARD ACCESSORIES |  |  |  |  |  |  |
| 5-1 | 016-0692-00 |  |  | 1 | POUCH,ACCESSORY:2465/2445 | 0.JRZ2 | ORDER BY DESC |
| -2 | 386-4849-0 |  |  | 1 | PLATE,MOUNTING:ACCESSORY POUCH,AL | TK1165 | ORDER BY DESC |
| -3 | 378-0199-03 |  |  | 1 | FILTER,LT,CRT:BLUE,3.415 X 4.105 X 0.030THK (STANDARD) | OKB00 | 378019903 |
|  | 378-0199-05 |  |  | 1 | FILTER,LT,CRT:BLUE,4.105 X 3.415 X 0.03 THK (OPTION 05) | OKBOO | 378-01999-05 |
|  | 378-0208-00 |  |  | 1 | FILTER,LT,CRT:CLEAR,4.105 X 3.415,POLYCARB (STANDARD) | TK0657 | 101-7 LEXAN |
| -4 | 159-0014-00 |  |  | 1 | FUSE,CARTRIDGE:3AG,5A,250V,0.8SEC | 61857 | SS2-5A |
| -5 | 200-3199-01 |  |  | 1 | COVER,FRONT:ABS | O.JR05 | ORDER BY DESC |
| -6 | 161-0104-00 |  |  | 1 | CABLE ASSY,PWR,:3,18 AWG,98 L,SVT,GREY/BLK | 0B445 | MC6-3 CG86 |
| -7 | 343-1213-00 |  |  | 1 | CLAMP,PWR CORD:POLYMIDE | TK1163 | ORDER BY DESC |
| -8 | 161-0104-06 |  |  | 1 | CABLE ASSY,PWR,:3 X 0.75MM SQ,220V,98.0 L (OPTION A1 - EUROPEAN) | S3109 | VIGSOPO-HO5WF |
| -9 | 161-0104-08 |  |  | 1 | CABLE ASSY,PWR,:3,18 AWG,98 L (OPTION A4 - NORTH AMERICAN) | 70903 | ORDER BY DESC |
| -10 | 161-0104-07 |  |  | 1 | CABLE ASSY,PWR,:3,1.OMM SQ,240 VOLT,2.5M (OPTION A2 - UNITED KINGDOM) | S3109 | ORDER BY DESC |
| $-11$ | 161-0104-05 |  |  | 1 | CABLE ASSY,PWR,:3,18 AWG,240V,98.0 L (OPTION A3 - AUSTRALIAN) | S3109 | SAA/3-OD3CCFC3X |
| $-12$ | 161-0167-0 |  |  | 1 | CABLE ASSY,PWR,:3.0 X 0.75,6A,240V,2.5M (OPTION A5 - SWISS) | S3109 | ORDER BY DESC |
|  | ---- |  |  | 1 | ACCESSORY KIT:TWO PROBES,COMPACT TIP |  |  |
|  | 016-0537-00 |  |  | 1 | POUCH,ACCESSORY:6 IN X 9 IN W/ZIPPER | 05006 | ZIP-6X9ID |
|  | 070-6599-00 |  |  | 1 | MANUAL,TECH:OPERATORS,2440 | 80009 | 070659900 |
|  | 070-6600-00 |  |  | 1 | MANUAL, TECH:USERS,2440 | 80009 | 070660000 |
|  | 070-6601-00 |  |  | 1 | MANUAL,TECH:PROGRAMMERS,2440 | 80009 | 070660100 |
|  | 070-6602-0 |  |  | 1 | MANUAL,TECH:POCKET PROGRAMMERS,2440P2G | 80009 | 070660200 |
|  | 134-0016-01 |  |  | 1 | ADAPTER.CONN:BANANA W/BINDING POST OPTIONAL ACCESSORIES | OJ260 | ORDER BY DESC |
|  | 016-0096-00 |  |  | 1 | HDW KIT,ELEK EQ:RACKMOUNTING | TK1465 | ORDER BY DESC |
|  | 016-0825-01 |  |  | 1 | RACK MOUNT KIT:2430/2445A/2465A/2467 | 80009 | 016082501 |
|  | 061-3516-06 |  |  | 1 | DATA SHEET:INSTL,2430/30A/32/32A/40/24L/31L | 80009 | 061351606 |
|  | 070-6603-00 |  |  | 1 | MANUAL,TECH:SERVICE,2440 | 80009 | 070660300 |
|  | 202-0302-00 |  |  | 1 | CASE,CARRYNG:23.75 $\times 15.75 \times 7$,TEK BLUE | 80009 | 202030200 |
|  | 346-0199-00 |  |  | 1 | STRAP,CARRYING:MKD TEKTRONIX | TK1623 | ORDER BY DESC |
|  | 020-1699-00 | $\mathrm{B} 010100$ | B012859 | $1$ |  | $80009$ | 020169900 |
|  | 020-1699-02 | B012860 |  | 1 | COMPONENT KIT:FRENCH HELP TEXT (OPTION 4F ONLY) | 80009 | 020169902 |
|  | 020-1700-00 | B010100 | B012859 | 1 | UPGRADE KIT:GERMAN | 80009 | 020170000 |
|  | 020-1700-02 | B012860 |  | 1 | COMPONENT KIT:GERMAN HELP TEXT (OPTION 4G ONLY) | 80009 | 020170002 |
|  | 020-1701-00 | B010100 | B012859 | 1 | UPGRADE KIT:ITALIAN | 80009 | 020170100 |
|  | 020-1701-02 | B012860 |  | 1 | COMPONENT KIT:ITALIAN HELP TEXT (OPTION 4H ONLY) | 80009 | 020170102 |


|  <br> Index <br> No. | Tektronix <br> Part No. | Serial No. <br> Effective <br> Dscont | Oty | 12345 Name si Description | Mfr. Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | Code |



$\qquad$

## Manual Insert Status

| DATE | CHANGE REFERENCE | STATUS |
| :---: | :---: | :---: |
| 1 July 1993 | C7/0793 | Effective |

## EFFECTIVE SERIAL NUMBERS: B011739 and above

## DIAGRAM CHANGES

## Diagram 5 SYSTEM DAC \& ACQ. CONTROL REG.

Change the value of resistors R951 (location 6L), R952 (location 8L), R955 (location 7L), and R957 (location 6L) to $15 \mathrm{~K} \Omega$.

Diagram 6 SYSTEM DAC (CONT) \& AUX. FRONT PANEL
Change the value of resistors R740 (location 3E), R832 (location 1E), R833 (location 2E), and R840 (location 3E) to $15 \mathrm{~K} \Omega$.

Diagram 10 PEAK DETECTORS \& CCD/CLOCK DRIVERS
Remove test point TP281 (location 8C).

Diagram

Change the value of resistors R683 (location 5J), R771 (location 1D), R775 (location 1J), R781 (location 5D), R871 (location 3D), R873 (location 3J), R881 (location 7D), and R883 (location 7J) to 1.5K $\Omega$.

EFFECTIVE SERIAL NUMBERS: 2440 B013321 and above EFFECTIVE SERIAL NUMBERS: 2440M B010119 and above

DIAGRAM CHANGES
Dlagram 19> HV SUPPLY \& CRT
Change the value of resistor R170 (location 4B) to $3.01 \mathrm{~K} \Omega$.
Change the value of resistor R263 (location 4D) to $100 \mathrm{~K} \Omega$.
EFFECTIVE SERIAL NUMBERS: 2440 B012657 and above
EFFECTIVE SERIAL NUMBERS: 2440M B010111 and above
Diagram 19〉 HV SUPPLY \& CRT
Change the value of resistor R162 (location 4D) to $2.7 \mathrm{~K} \Omega$.
Diagram LV POWER SUPPLY

Change the value of resistors R324 and R624 (location 1F) to $75 \Omega$.

## EFFECTIVE SERIAL NUMBERS: 2440 B013315 and above

 EFFECTIVE SERIAL NUMBERS: 2440M B010119 and above
## BOARD CHANGES

## A12 PROCESSOR BOARD

The following partial A12 Processor Board shows the changes listed in the Replaceable Parts List Changes. The change removes the battery circuitry.


DIAGRAM
CHANGES


The following partial schematic shows the changes to Diagram 1 listed in the Replaceable Parts List Changes. The change removes the battery circulity.


Page 2 of 5

Product: $\qquad$ 2440 Service

EFFECTIVE SERIAL NUMBERS: B010826 and above

## DIAGRAM CHANGES

Diagram 10 PEAK DETECTORS \& CCD/CLOCK DRIVERS

Change cest (location 4M) to a 0.022 mf capacitor. add R8so. a se a resistor.


## BOARD CHANGES

## A10 MAIN BOARD

On the A10 Main Board, R650 is teepee'd to C652 (location 7H).

## EFFECTIVE SERIAL NUMBERS: 2440 B012403 and above

 EFFECTIVE SERIAL NUMBERS: 2440M B010108 and above
## DIAGRAM CHANGES

Replace the A17 HV Power Supply Circult board layout and reference table with the new layout and table attached.
Replace Dlagram 19 HV SUPPLY \& CRT schematic and reference table with the new schematic and table attached.

Remove CR510 on the A16 LV Power Supply Circuit board layout and replace with CR511, CR512, CR513, and CR514 as shown.

Product: _2440 Service_Date:_1 July 1993_Change Reference: C7/0793

## EFFECTIVE SERIAL NUMBERS: 2440 B012403 and above EFFECTIVE SERIAL NUMBERS: 2440M B010108 and above <br> DIAGRAM CHANGES

Replace CR510 on Diagram 22 LV POWER SUPPLY with diodes CR511, CR512, CR513, and CR514 as shown.


EFFECTIVE SERIAL NUMBERS: B011739 and above

Add the procedure on the following page after Procedure 1. Cabinet Removal, on page 6-17.

## 1.a.Cabinet Installation

a. Grasp the handle hubs (at right and left sides of the instrument) and pull outward. While holding the hubs outward, carefully lower the cabinet onto the instrument.
b. Align the front edges of the cabinet with the EMI rope gasket (see Fig. 6-2a).

## WARNING

To obtain maximum EMI susceptibility protection, the front edges of the cabinet must be seated on the EMI rope gasket. No portion of the cabinet should be touching the front casting. In addition, the gaskets, front and rear, should be in good condition, showing no signs of corrosion, wear, or loss of resilience. If the EMI rope gaskets are not in good condition they should be replaced.
c. Replace the back panel and install the four screws in an $X$ pattern (install top left screw then bottom right screw followed by bottom left screw then top right screw) to 16 inch-pounds of torque.
d. Attach the power cord to the Rear panel by inserting the retainer clip into mounting hole and rotating the clip $1 / 4$ turn to lock.


Figure 6-2a: Placement of cabinet on EMI rope gasket.


[^0]:    Warning
    The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

[^1]:    ${ }^{a}$ A stable trigger is one that results in a uniform, regular display triggered on the selected slope ( $\pm$ ). A stably-triggered display should NOT have the trigger point switch between opposite slopes on the waveform, nor should it "roll" across the screen, as successive acquisitions occur. At TIME/DIV settings of $2 \mathrm{~ms} /$ DIV and faster, the TRIG'D LED is constantly lit if the display is stably triggered (the LED can flash for SEC/DIV settings of $10 \mathrm{~ms} /$ DIV and slower).

[^2]:    aPerformance Requirement not checked in the manual.

[^3]:    aPerformance Requirement not checked in the manual.

[^4]:    ${ }^{\text {a }}$ Performance Requirements not checked in the manual.

[^5]:    aPerformance Requirement not checked in the manual.

[^6]:    DO-R/O (readout) goes HI when a readout display should start.

[^7]:    ${ }^{\text {a Requires a TM }} \mathbf{5 0 0 - S e r i e s ~ p o w e r - m o d u l e ~ m a i n f r a m e . ~}$

[^8]:    The isolation transformer (item 13) is an important SAFETY item. The switching power supply of the scope has areas that float at the ac-source potential, and a serious shock hazard exists when the power supply safety shield is removed to permit troubleshooting if power is applied directly from the ac-source.

[^9]:    TEST NUMBER 1100: Test number 1100 tests U670, a $16 \mathrm{~K} \times 8$ ROM that contains the scope operating system. There are no sublevel tests for test number 1100.

    TEST NUMBER 1200-1500: Test numbers $1200-1500$ test the remaining four $64 \mathrm{~K} \times 8$ ROMs comprising the remainder of the System ROM memory, with numbers $1200,1300,1400$, and 1500 testing U680 (ROM0.0), U682 (ROM0.1), U690 (ROM0.2), and U692 (ROM0.3), respectively. There are four sublevels to each test $1200-1500$. This is because each ROM device is divided into four pages ( 16 Kbytes each) with each pages selectable by 2 address-page bits. Each sublevel test (1210-1240, 1310-1340, etc.) tests one of the four pages for a device.

[^10]:    SYSTEM $\mu$ P System $\mu$ P Aborts on Start-Up or While Operating:
    There is some internal consistency checking that can result in an "abort" of the operating routines. The abort routine loops endlessly, blinking the Trigger LEDs on and off in an abort code. On an abort, the Trigger LEDs are flashed three times, then an abort code is displayed in binary with the TRIG'D LED being the LSB of the code (see Figure 6-5), and the cycle is then repeated continually.

