TEKTRONIX®

CP1100/CP BUS INTERFACE (670-2383-02)

SERVICE

INSTRUCTION MANUAL

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Serial Number _____

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SECTION 1

OPERATING INSTRUCTIONS

Introduction

The CP1100/CP Bus Interface Card is located inside a CP1100 Series Controller[1]. It provides interfacing between the CP1100 and a common bus called the CP Bus. This card allows the Controller to communicate with one of eight external devices (Waveform Digitizing Instruments) on the other end of the CP Bus (see Fig. 1-1).

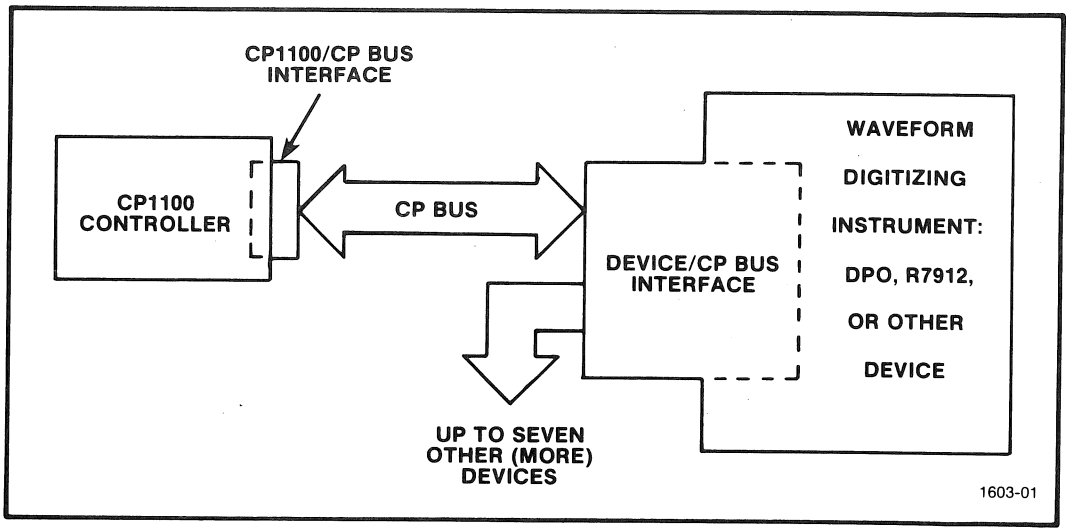

Fig. 1-1. CP Bus.

Waveform Digitizing Instruments, such as the DPO or the R7912 each with its appropriate interface to the CP Bus may be used. The CP1100 can accomodate up to four CP1100/CP Bus Interface Cards provided peripheral slots are available. This allows a total of up to 32 devices to be controlled by one CP1100 Controller.

[1]*The CP1100 Series Controller is fully compatible with DEC® (Digital Equipment Corporation) PDP-11 Series Minicomputers.*

Cabling and Strapping Information

The only means of communication between a device (DPO or R7912) and a Controller is through the two interfaces, one in the device and one in the Controller. Since a configuration may have as few as one or as many as 32 instruments, it is difficult to describe a complete system interface for every possible case. In general, however, the system interface may contain a combination of some or all of the following interfaces and cables:

1) CP1100/CP Bus Interface.

2) DPO/CP Bus Interface.

3) R7912/CP Bus Interface.

4) Interconnecting Cables (standard six foot lengths):
   (a) R7912/Controller Interconnecting Cable.
   (b) DPO/Controller Interconnecting Cable.

Additional information on these interfaces is given in the appropriate instruction manual.

CP1100/CP Bus Interface. CP1100 Series Controllers may contain up to four CP1100/CP Bus Interface Cards, depending upon the number of peripheral slots available; i.e., those not in use by other peripheral interface cards. Empty peripheral slots must contain a Grant Continuity Jumper Card (Fig. 1-2). The four cards differ only in the setting of the Interrupt Vector Address and the Controller Address Straps (see Fig. 1-3). The strap settings are a factor in determining an instrument's Hardware Unit Number (HUN). This will

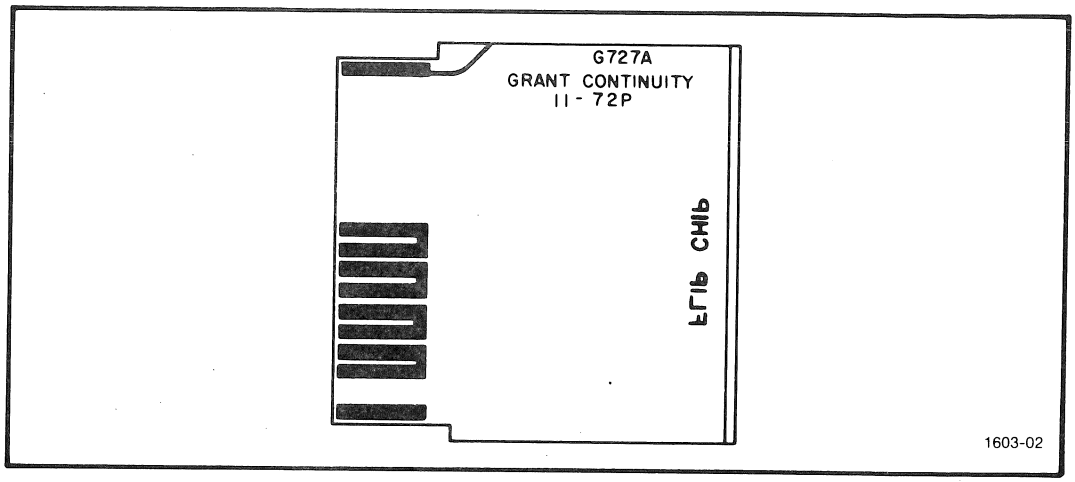

Fig. 1-2. Grant Continuity Jumper Card.

be discussed later.

Each CP1100/CP Bus Interface Card has a single 37-pin jack (Fig. 1-3). This jack accepts the cable which serves as a CP Bus branch connecting each of the eight possible instruments on that line. The exact method of cabling will be discussed later.

DPO/CP Bus Interface. The DPO/CP Bus Interface inserted in the rear panel of the DPO's P7001 Processor Unit, contains a 37-pin plug (male) on the left side and a 37-pin Jack (female) on the right side. The plug accepts the cable coming from the Controller or other instrument on the Controller side of the CP Bus. The jack accepts the cable going to instruments on the terminating side of the CP Bus.

When the DPO is the last instrument on its branch of the CP Bus (the farthest from the Controller), no cable will be connected to the jack of the DPO/CP Bus Interface. However, terminating resistors must be installed in this instrument (see Fig. 1-4). The terminating

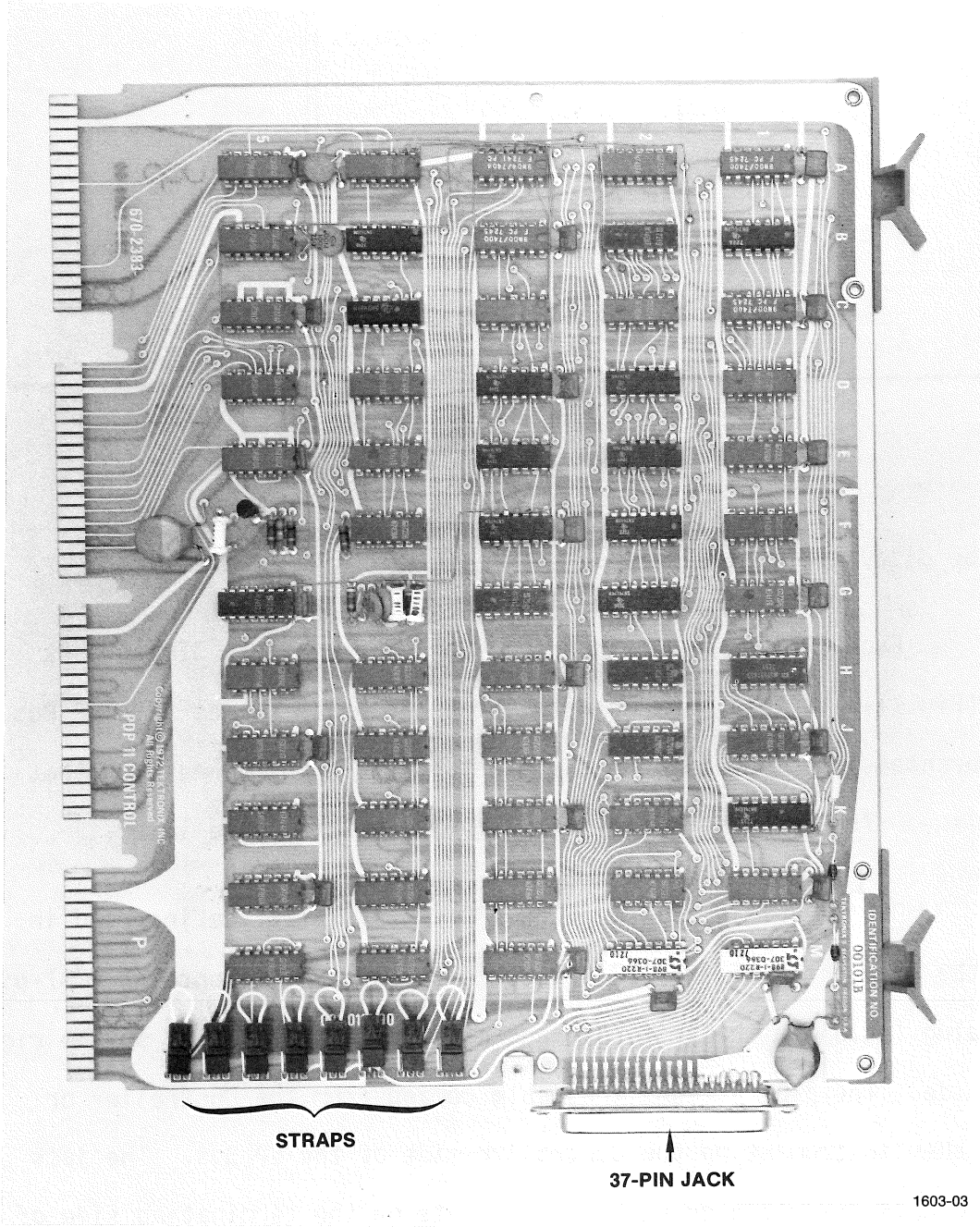

Fig. 1-3. Side view of CP1100/CP Bus Interface.

resistors must be removed from all other instruments on that branch of the CP Bus, as will be explained later in this section.

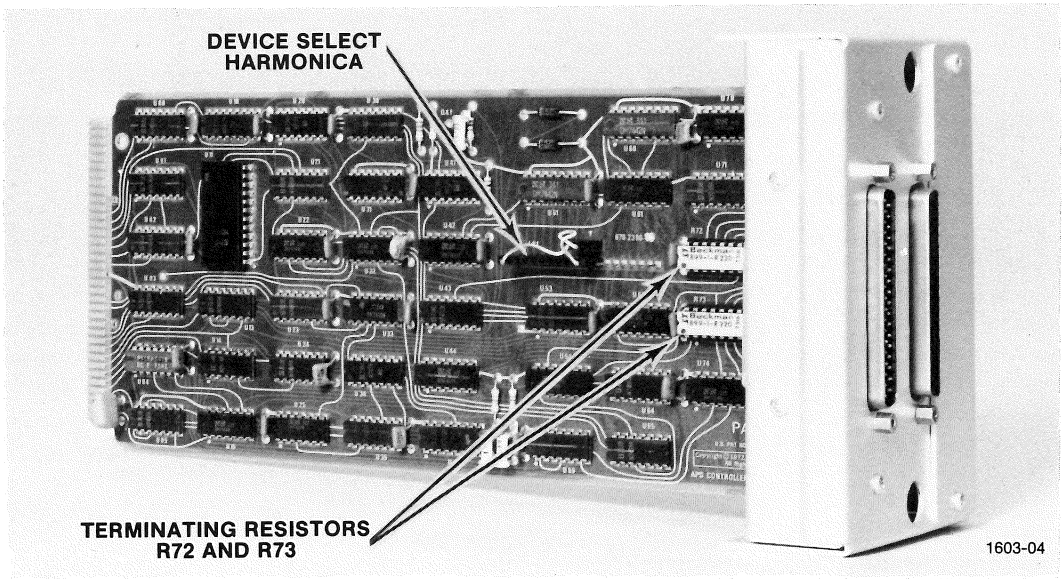

Fig. 1-4. DPO/CP Bus Interface.

R7912/CP Bus Interface. The R7912/CP Bus Interface is a circuit card located in the INT (interface) slot behind the swing-out front panel of the R7912. Connections to this interface card are made via the 104-pin DIGITAL OUT jack located on the rear panel of the R7912 (see Fig. 1-8). Since the R7912 has just one of these jacks, an "R7912 INTERCONNECT CABLE" must be used. One end of this cable terminates in a junction box (or T connection) so that a second cable for the next instrument on this CP Bus can be connected to this junction box.

When an R7912 is the terminating instrument on its branch of the CP Bus, no other cables are connected to the terminating cable's junction box. Instead, insert terminating resistors U1 and U6 in their respective sockets in the R7912/CP Bus Interface (see Fig. 1-5).

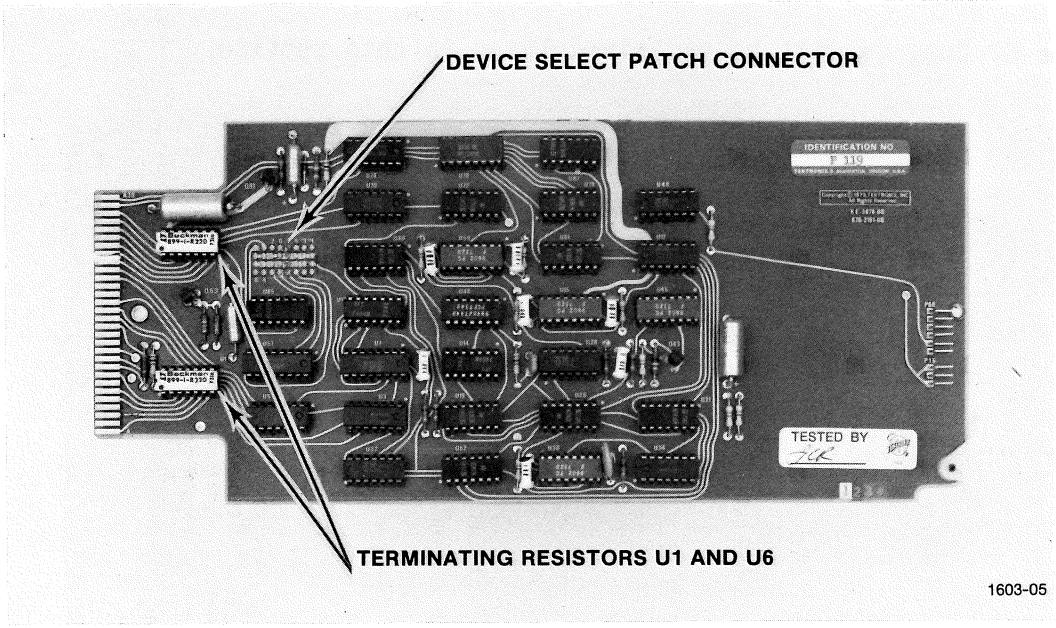

Fig. 1-5. R7912/CP Bus Interface Card.

Terminating resistors must be removed from all other instruments on this branch of the CP Bus, as will be explained later.

Instrument Cabling Instructions

Two types of cables are needed to cable the instruments in a system configuration. The first is a "DPO INTERCONNECT CABLE". It has a 37-pin, screw-type jack on one end and a 37-pin, screw-type plug on the other end (Fig. 1-6). The second cable is the "R7912 INTERCONNECT CABLE". One end of this cable terminates in a junction box containing a 37-pin jack on one side of the box and a 104-pin plug on the adjacent side. The other end of this cable contains a 37-pin plug (see Fig. 1-7). The 104-pin plug inserts directly into the DIGITAL OUT jack of the R7912, while the 37-pin jack accepts the cable going to instruments on the terminating side of the CP Bus.

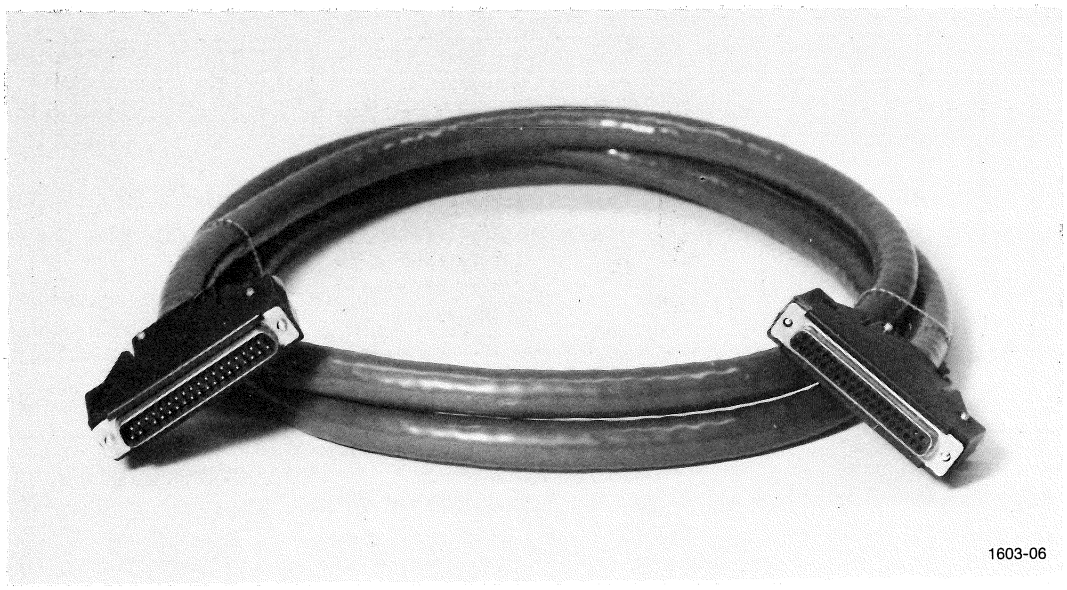

Fig. 1-6. DPO Interconnect Cable.

The 37-pin jack on the CP1100/CP Bus Interface will accept the 37-pin plug from either the DPO INTERCONNECT CABLE or the R7912 INTERCONNECT CABLE.

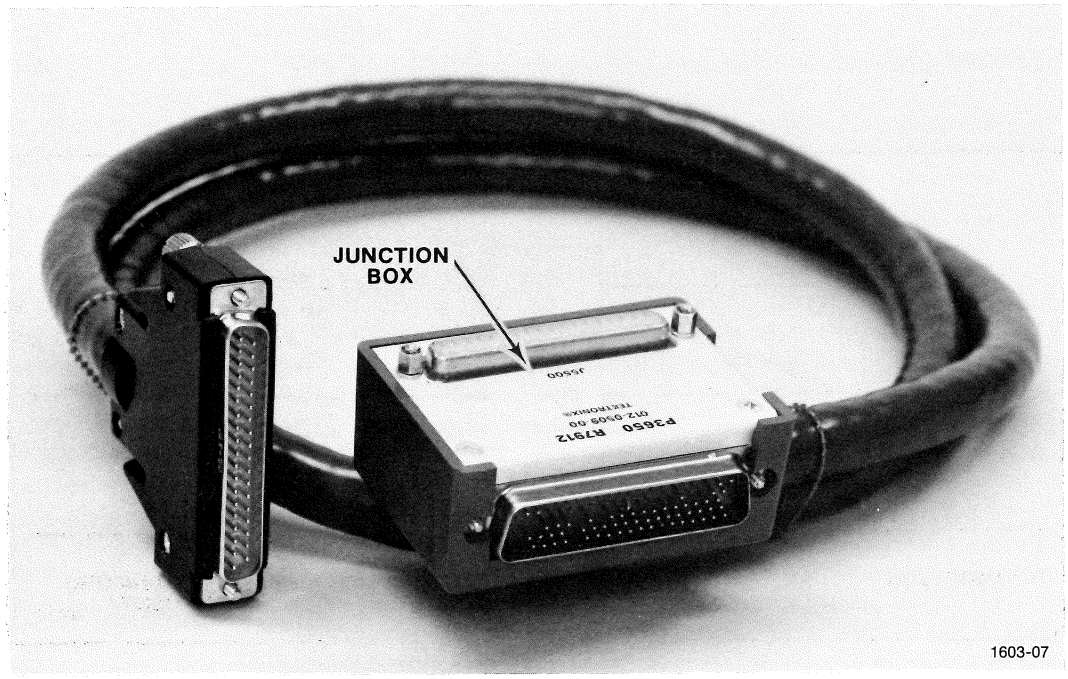

Fig. 1-7. R7912 Interconnect Cable.

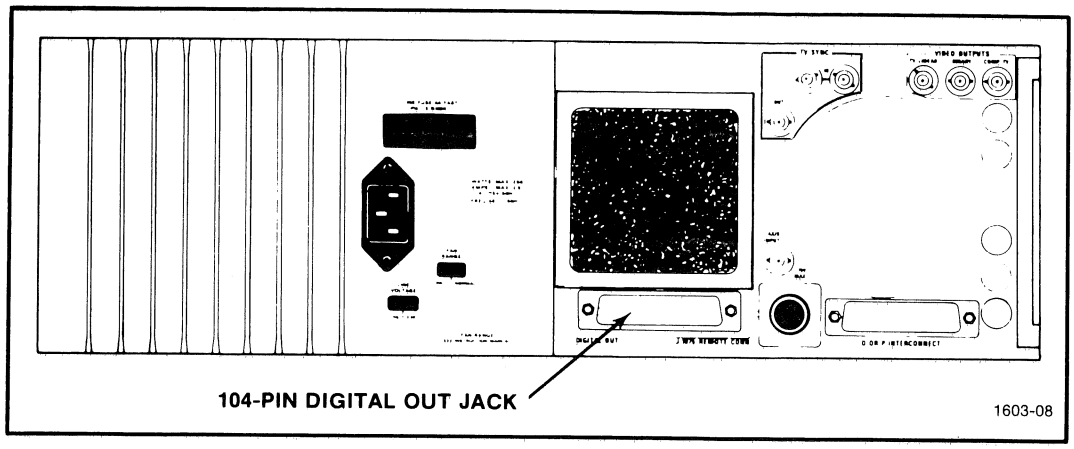

Fig. 1-8. Location of Digital Out Jack on Rear Panel of R7912.

DPO and R7912 INTERCONNECT CABLES are available in different lengths to allow convenience and flexibility in cabling a system. In general, the length of any particular cable is unimportant. However, the total cable length of any one branch of the CP Bus should not exceed 50 feet -- including 18" of internal cable for each R7912 on the line.

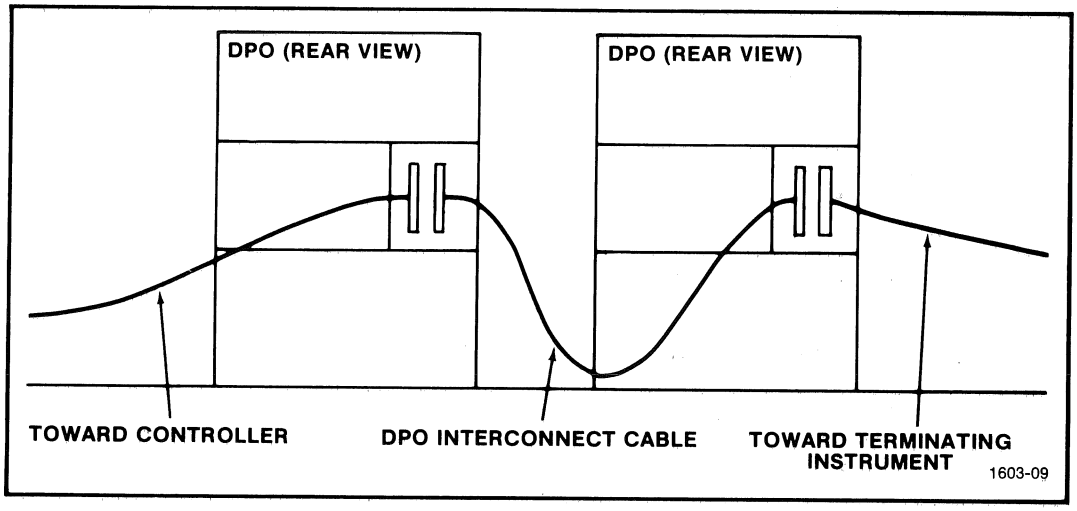

Fig. 1-9. Connecting DPO to DPO.

When connecting one DPO to another, use a DPO INTERCONNECT CABLE, connect the male end to the jack on the DPO/CP Bus Interface that is "electrically closer" to the CP1100. Connect the female end to the plug on the next DPO/CP Bus Interface (Fig. 1-9).

When connecting one R7912 to another R7912, use an R7912 INTERCONNECT CABLE (Fig. 1-10). Insert the 104 pin plug into the DIGITAL OUT jack of the R7912 that is "electrically farther" from the Controller. Insert the other end of the cable into the 37-pin jack located on the junction box of the preceding R7912 INTERCONNECT CABLE. (It is assumed that this preceding cable has already been connected to the DIGITAL OUT jack of the R7912 that is closer to the Controller.)

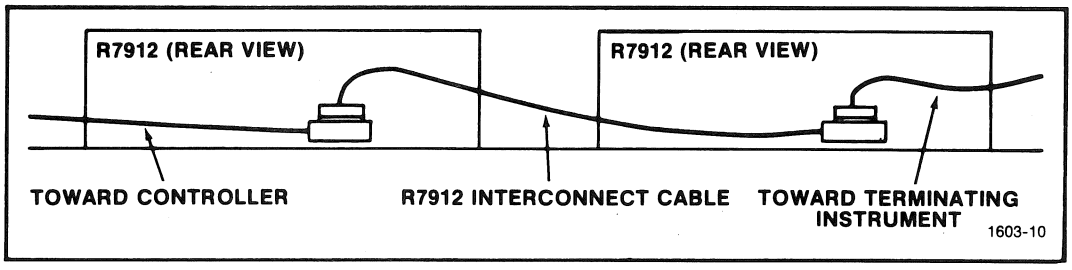

Fig. 1-10. Connecting R7912 to R7912.

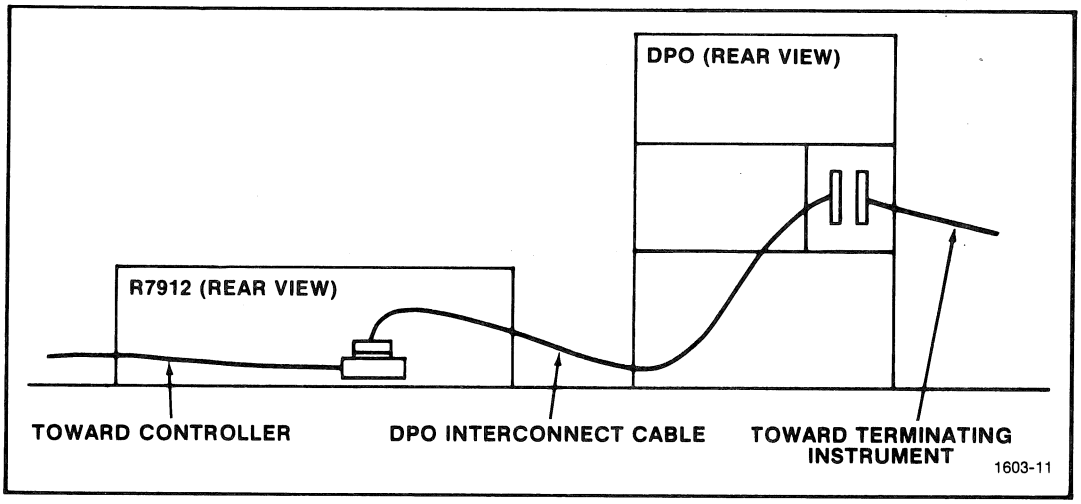

Fig. 1-11. Connecting an R7912 to a DPO.

When connecting an R7912 to a DPO that is "electrically farther" from the Controller, use a DPO INTERCONNECT CABLE (see Fig. 1-11). Connect the female end to the 37-pin plug on the left side of the DPO/CP Bus Interface. Connect the male end to the 37-pin jack located on the junction box of the preceding R7912 INTERCONNECT CABLE. (Again, it is assumed that this preceding cable has already been connected to the DIGITAL OUT jack of the R7912.)

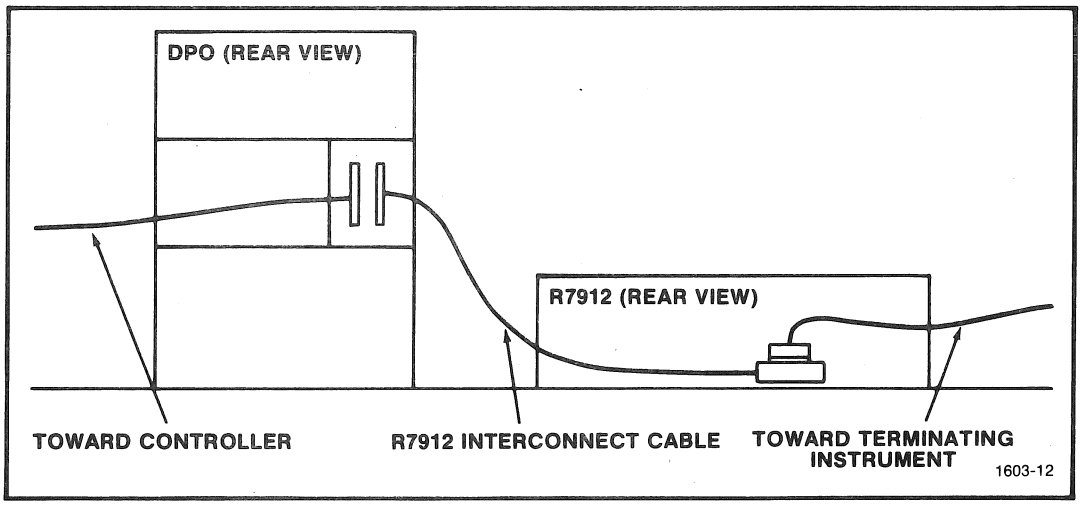

Fig. 1-12. Connecting a DPO to an R7912.

When connecting a DPO to an R7912 that is "electrically farther" from the Controller, use an R7912 INTERCONNECT CABLE (see Fig. 1-12). Insert the 104-pin plug of the cable into the DIGITAL OUT jack of the R7912. Connect the other end of the cable to the 37-pin jack of the preceding DPO/CP Bus Interface.

Terminating a Branch of the CP Bus

Each of the four possible branches of the CP Bus must be properly terminated. This is done by inserting terminating resistors in the interface card of the instrument that terminates a particular CP Bus branch. Terminating resistors are interchangeable between the R7912 and the DPO.

When a DPO is the terminating instrument on a CP Bus branch (the instrument that is "electrically farthest" from the Controller),

terminating resistors R72 and R73 must be inserted in the proper sockets of the DPO/CP Bus Interface (see Fig. 1-4). However, the terminating resistors must be removed from all other instruments on that branch of the CP Bus. R72 and R73 are actually a group of resistors enclosed in a DIP case. These resistors must be in place even when there is just one instrument on the line.

To access resistors R72 and R73, loosen the screws through the holes in the back panel of the DPO/CP Bus Interface. With the power off, remove the interface from the back of the DPO. Once the resistors have been removed or replaced, as required, again insert the DPO/CP Bus Interface into the back of the DPO and tighten the screws.

When an R7912 is the terminating instrument on a CP Bus branch, terminating resistors U1 and U6 must be inserted in their respective sockets on the R7912/CP Bus Interface (see Fig. 1-5). As with the DPO, terminating resistors must be removed from all interface cards except the last instrument on that particular branch of the CP Bus. (Resistors U1 and U6 are enclosed in the two DIP cases.) These resistors must be in place even if only one R7912 is on the line.

To access resistors U1 and U6, loosen the retaining screws and swing out the hinged front panel of the R7912. With the power off, pull out the interface card from the INT slot and remove or replace the terminating resistors as required. Then replace the R7912/CP Bus Interface and again tighten the retaining screws on the R7912 front panel.

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Strapping Options

Strapping options are normally set at the factory or when the system is first installed. However, you may wish to add several more DPO's or R7912's to the system at some later time. Also, you may want to change the configuration of those on a particular system. This section will explain how such changes are made.

Since there is a possibility of 32 instruments in any configuration, some means must be used to determine or select which instrument the Controller wants to communicate with. In terms of hardware, this selection is facilitated by Hardware Unit Numbers (HUNs). These are unique integers in the range of 0 to 31. Since a configuration may contain up to 32 instruments, there may be as many as 32 HUNs for the system and each instrument of the system will have a unique HUN associated with it. Thus an HUN may be thought of as the "name" by which the Controller identifies a particular instrument. An existing instrument may be "renamed" or a new instrument may be given a "new name" by assigning a unique HUN according to the procedures outlined in this section.

The HUN of a particular instrument is a function of two factors. The first factor is the setting of the Group Select straps on the CP1100/CP Bus Interface. The second factor is either the setting of the Device Select harmonica (in the case of a DPO/CP Bus Interface), or the setting of the Device Select straps (in the case of an R7912/CP Bus Interface).

CP1100/CP Bus Interface Straps. The Group Select straps on the CP1100/CP Bus Interface determine the range of values that a HUN can assume for any instrument cabled to that particular interface card. For example, one setting of the straps causes the HUN of any instrument connected to the interface to range from 0 to 7. A second setting causes the HUNs to range from 8 to 15. A third setting causes the HUNs to range from 16 to 23, and a fourth and final setting causes the HUNs to range from 24 to 31. The Device Select settings on the DPO and R7912 interface cards will then determine the specific value of the instrument's HUN within one of the four ranges. This concept is illustrated in the following table:

Table 2

Table for Determining Hardware Unit Numbers (HUNs)

Group Select Strap Settings	0	1	2	3	4	5	6	7
0	0	1	2	3	4	5	6	7
1	8	9	10	11	12	13	14	15
2	16	17	18	19	20	21	22	23
3	24	25	26	27	28	29	30	31
	0	1	2	3	4	5	6	7

Device Select Strap Settings

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In order for each of the 32 possible HUNs to be unique, each of the four possible CP1100/CP Interface cards must have different Group Select strap settings. Also, each of the eight possible R7912 or DPO interface cards on a particular CP Bus branch must have unique Device Select strap settings. With respect to the entire system, there may be as many as four DPO or R7912 interface cards that have the same

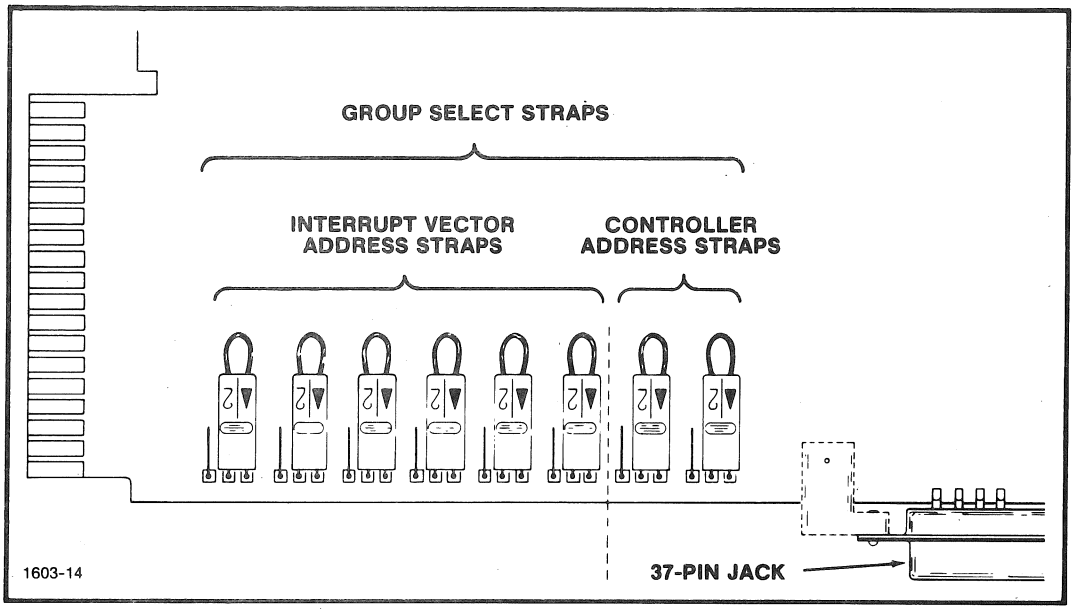

Fig. 1-13. CP1100/CP Bus Interface strapped for instruments in group Ø (HUNs Ø through 7).

Device Select number. Yet each of these four must be on a different branch of the common bus.

As shown in Fig. 1-13, there are eight Group Select straps on the CP1100/CP Bus Interface card. The two nearest the 37-pin jack are the Controller Address straps. The other six are the Interrupt Vector Address straps. Although identical in appearance, these two sets of straps perform different (but related) functions. These functions correspond to the two types of communication that occur between the Controller and the DPO or R7912. The position of the straps determine the logic state of the bit. Fig. 1-14 indicates the strapping necessary for the four Groups and their decimal and octal equivalent.

The first type of communication occurs when the interrupting instrument is trying to gain attention from the Controller. In this mode, the purpose of the Interrupt Vector Address straps is to select the interrupt processing routine according to which group of eight devices the interrupt came from. The Interrupt Vector Addresses are 374_8, 370_8, 364_8, and 360_8, depending upon whether the interrupting instrument is in group 0, 1, 2, or 3, respectively (see Fig. 1-14). Each of these Interrupt Vector Addresses contains the address of a different interrupt processing routine and each of these four routines corresponds to one of the four groups of eight instruments. Once the interrupt has been processed, then the second type of communication with the Controller can occur.

The second type of communication occurs when a group of instruments has already established an interrupt and is "talking" to the Controller. In this mode, the purpose of the two Controller Address straps is to select which group of eight instruments the Controller will accept inputs from or direct outputs to. The Interrupt Vector Address straps and the Controller Address straps must both be set to the same group number in order for the Controller to recognize the interrupt from a particular instrument and subsequently communicate with it. Thus, whenever the Controller Address straps are changed on a particular interface board, the Interrupt Vector Address straps must be set to the same group number.

By convention, the four possible groups of eight instruments have been designated 0, 1, 2, and 3, as indicated in Table 2. Fig. 1-14 shows the proper settings of each of the Controller Address

GROUP NUMBER	INTERRUPT VECTOR ADDRESS STRAPS	CONTROLLER ADDRESS STRAPS = X IN 16XØDR
(HUNs Ø TO 7)	MSB … LSB: LOWER TWO BITS WIRED TO "Ø"	LSB … MSB: MSB WIRED TO "1"
DECIMAL NO.	1 1 1 1 1 1 Ø Ø	Ø Ø 1
OCTAL EQUIV.	3 7 4	4
(HUNs 8 TO 15)	LOWER TWO BITS WIRED TO "Ø"	MSB WIRED TO "1"
DECIMAL NO.	1 1 1 1 1 Ø Ø Ø	1 Ø 1
OCTAL EQUIV.	3 7 Ø	5
(HUNs 16 TO 23)	LOWER TWO BITS WIRED TO "Ø"	MSB WIRED TO "1"
DECIMAL NO.	1 1 1 1 Ø 1 Ø Ø	Ø 1 1
OCTAL EQUIV.	3 6 4	6
(HUNs 24 TO 31)	LOWER TWO BITS WIRED TO "Ø"	MSB WIRED TO "1"
DECIMAL NO.	1 1 1 1 Ø Ø Ø Ø	1 1 1
OCTAL EQUIV.	3 6 Ø	7

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Fig. 1-14. Positions of Group Select Straps for controlling groups 0, 1, 2, or 3.

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straps and Interrupt Vector straps for the group of instruments being addressed. For example, to control instruments whose HUNs range from 0 to 7, you would need to strap the CP1100 CP Bus Interface board for group 0. This occurs when all of the straps are set to the right hand position. To restrap this interface card to group 1 (for HUNs 8 to 15), you would need to change the setting of the Interrupt Vector Address strap that is on the extreme right as well as the setting of the Controller Address strap that is next to it. This is shown in Fig. 1-14.

DPO/CP Bus Interface Straps. Once a range of values has been determined by the Group Select Straps on the CP1100/CP Bus Interface, the value of a DPO's HUN depends solely upon the setting of the Device Select harmonica in the DPO/CP Bus Interface. Fig. 1-15 shows the location of this harmonica on the DPO/CP Bus Interface.

The Device Select harmonica may be placed in any one of eight positions. When the harmonica is in the extreme left position (as shown in Fig. 1-15), the DPO has a HUN of either 0, 8, 16, or 24 -- depending upon the strapping of the CP1100/CP Bus Interface to which it is cabled. When the harmonica is in the extreme right position, the DPO has a HUN of either 7, 15, 23, or 31 -- again depending upon the strap settings of the CP1100/CP Bus Interface. The other positions on the harmonica are numbered one through seven consecutively and determine the HUN of the DPO in a similar manner. Be sure each DPO or R7912 on the same brance of the common bus is set to a unique Device Select number.

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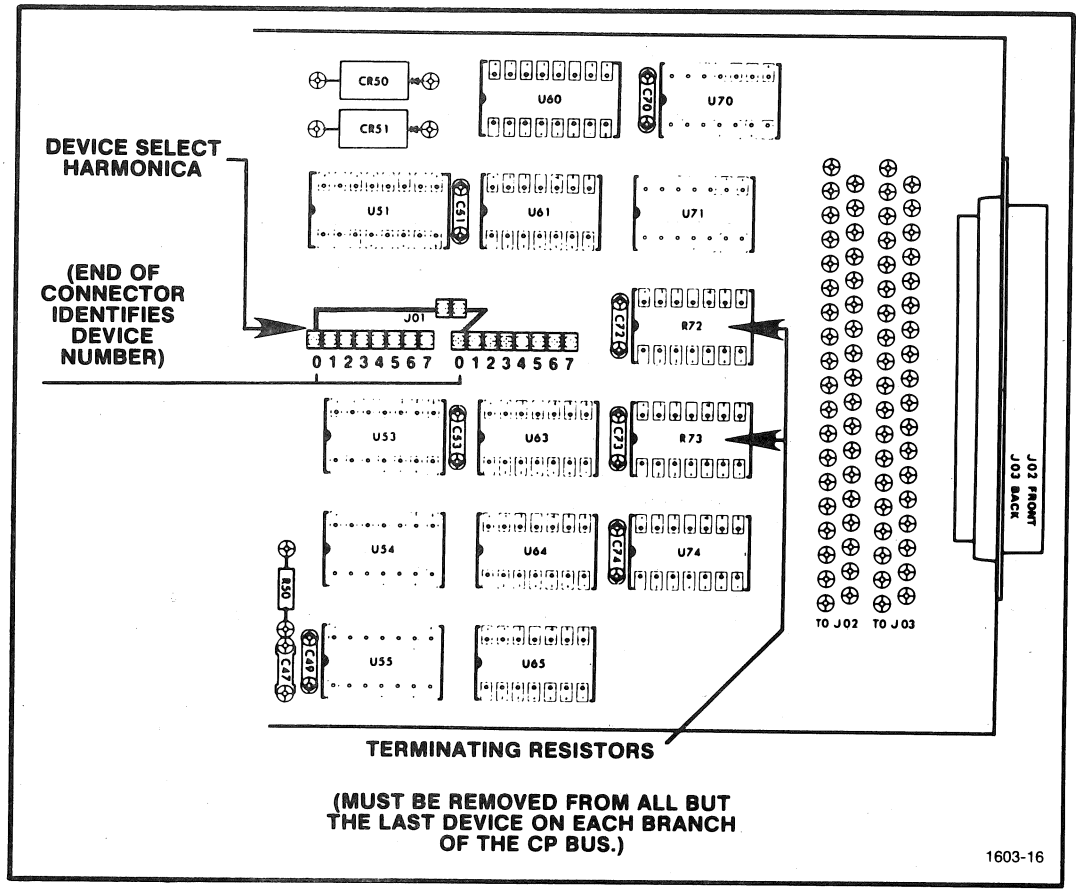

Fig. 1-15. Location of Device Select Harmonica and terminating resistors on DPO/CP Bus Interface.

R7912/CP Bus Interface Straps. Once a range of HUNs has been determined by the CP1100/CP Bus Interface, the value of an R7912's HUN depends solely upon the setting of the Device Select patch connector on the R7912/CP Bus Interface. Fig. 1-16 shows the location of this connector on the interface.

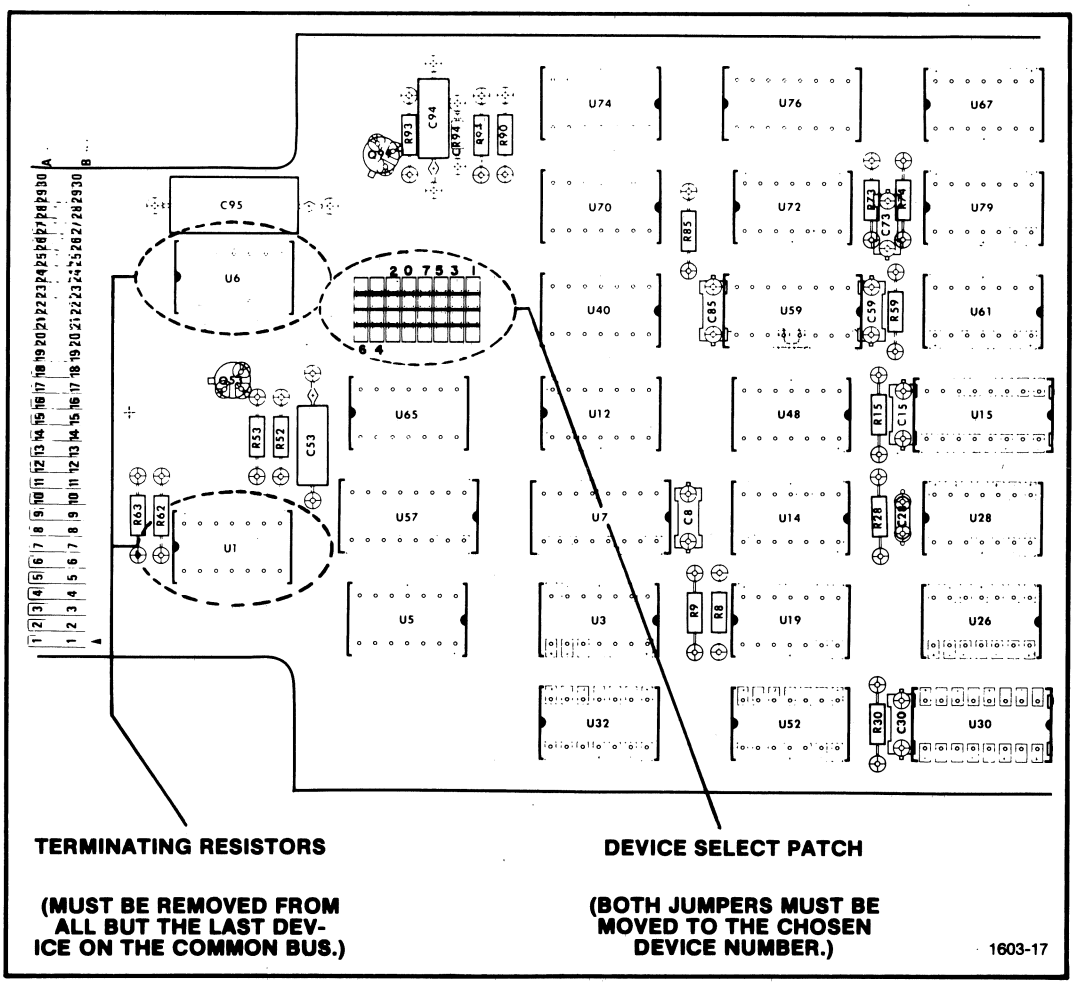

Fig. 1-16. Location of Device Select Straps and Terminating Resistors on R7912/CP Bus Interface.

The Device Select patch connector of the R7912/CP Bus Interface card contains two movable jumpers that are inserted in a line in any one of eight positions. Notice that the connector's patch positions are not numbered consecutively. When the interface is oriented as in Fig. 1-16, the numbers on the patch connector read from left to right as follows: 6, 4, 2, 0, 7, 5, 3, 1. Therefore, when both jumpers are in the extreme left position, the R7912 has a HUN of either 6, 14, 22, or 30 -- depending upon the Group Select strap settings of the CP1100/CP Bus Interface to which the R7912 is cabled. When both jumpers are in the extreme right position (as shown in Fig. 1-10), the R7912 has a HUN of either 1, 9, 17, or 25 -- again depending upon how the CP1100/CP Bus Interface is strapped. The other six positions on the Device Select patch connector determine Hardware Unit Numbers in a similar manner. Be sure that each R7912 or DPO on the same brance of the common bus is set to a unique Device Select number.

Summary

A partial block diagram of a typical configuration is given in Fig. 1-17 to illustrate the information in this section. While this example may not be ideal, it illustrates the flexibility that is allowed when cabling a system.

Several changes can be made in cabling the system shown in Fig. 1-17. For example, since there are only six instruments on the system, all six can be cabled to one CP1100/CP Bus Interface. This is done by removing the terminating resistors from the R7912 whose

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SECTION 2

CIRCUIT DESCRIPTION

The CP1100/CP Bus Interface Card serves as an interface between a CP1100 Series Controller and the CP Bus to transfer address and data information from and to devices on the other end of the CP Bus. Using the proper software in the Controller, the Controller can collect data from the device, manipulate, store, or transfer it. It can also direct the operation of the device, i.e., change its status. All operations depend upon the abilities of the device. Presently only two are available: the DPO and R7912. A table of Mnemonics is located on page 2-20 to provide a definition of line and signal labels.

General Description

There are four functional states which the Controller can command to the device through the CP1100/CP Bus Interface.

1) Data Read ---- The Controller reads data from the device.

2) Status Read -- The Controller reads the status of the device.

3) Data Write --- The Controller transfers data to the device.

4) Address Write -The Controller transfers an address or command to the device.

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Interrupts

The interrupt structure of the CP1100 Series Controllers is designed to enable the Controller's processor to run at all times and perform specific operations when interrupted. Each interrupting device has a unique interrupt vector which causes the Controller to change program control to the appropriate interrupt handling routine. Each interrupt vector has a priority assigned which causes the Controller to interrupt the current routine only if the interrupting device has a higher priority than the current operating routine.

The Controller returns to the interrupted routine after the higher priority routine is completed.

Interrupt Vectors. The interrupt handling capability of the CP1100 Controller may be enabled by setting the Interrupt Arm FF (U45A-Diag. 14B) to "one" or disabled by setting it to "zero" under program control. If enabled, the CP1100 Controller may be able to receive an interrupt from any external device.

The CP1100 Interrupt trap address (vector) may be patched to any address within the range 0-374 (in octal) (Diag. 14A). It is recommended, however, that one of the user definable vector addresses (270, 274, 360, 364, 370, 374) be used to eliminate any conflict with other peripherals (see Section 1).

Each request by an external device causes the device code of the requesting device to be stored in the CP1100 Controller Status Register (Diag. 14B). This information is then available for software to determine which device caused the interrupt.

During the power up sequence, a large number of interrupts can occur. Therefore, the Processor Status Word that is assumed upon an interrupt (Vector +2) should contain an interrupt priority level of at least 5 so that further interrupts will not occur until such a time as the software can cope with them.

Interrupt Pending (Bit 0) and device number (bits 3, 4, 5) can only be set by the device when it sends an interrupt to the CP1100. These bits are cleared whenever data is moved into the Status Register. Interrupt Pending (IPEND) will be set whenever the device requests an interrupt. If ARM is set, the CP1100 will be interrupted. If ARM is not set, the interrupt will not be acknowledged by the CP1100 (see Fig. 2-1).

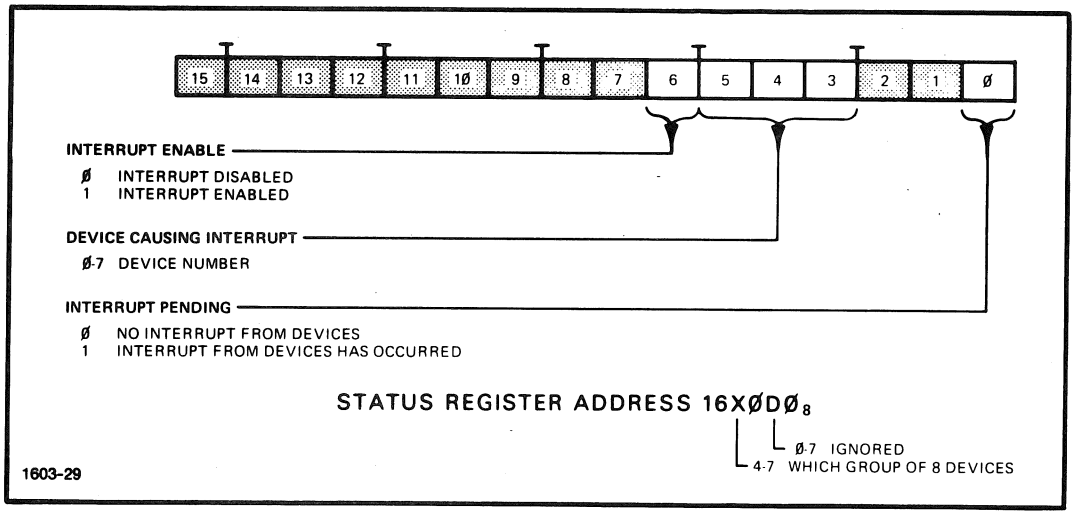

Fig. 2-1. CP1100 Controller Status Word format.

DPO Interrupts. When the DPO addresses the CP1100, it sends an Interrupt Request. It comes in on one of the lines $\overline{CB0}$ through $\overline{CB7}$ (Diag. 14C). These eight lines represent one of the eight possible DPOs connected to the CP Bus.

Assuming only one device, such as device #Ø, sends an interrupt in on $\overline{CB0}$ it will be inverted in U27D and go out this diagram as T0 to diagram 14A. All eight interrupt lines come into diagram 14A near the center of the page. They are inverted again and sent to U07, an Interrupt Priority Encoder. If we receive an interrupt from Device Ø, T0 is inverted by U27C and goes to pin 10 of U07. The output of U07 appears in binary code on pins 6, 7, and 9. Pin 6 has a value of 1, pin 7 is 2, and pin 9 is 4. This gives us a binary count from 0 thru 7, or eight possible counts. Since our interrupt-ind device is #Ø, then the output will be Ø (all lines HIGH). If the interrupting device is device #3, then pin 6 and 7 are LOW and pin 9 is HIGH.

If any input at all is received then a LOW appears on pin 14 of U07. This LOW is inverted by U08F and when it passes through the Interrupt Latch U09, it becomes IPEND (Interrupt Pending).

Each time a reset is programmed or when the START switch on the CP1100 front panel is pressed, interrupts are disarmed and the Status Register is cleared by "INIT" (Initialize) from the CP1100 Controller arriving on pin 5 of U83A (Diag. 14B).

If two Interrupts arrive from two different devices at the same time, then the Interrupt Priority Encoder will pick out the one with

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the largest number (i.e., 5 over 2, etc.). The largest number would appear at the output of the Interrupt Priority Encoder. If device #5 was selected, then pin 6 and 9 would be "ones" designating binary 5. The second device's interrupt will have to wait until the common bus is free again. However, its interrupt will be held in the Interrupt Shift Register (U26, Diag. 10A).

R7912 Interrupts. Only one condition causes the R7912 to request a CP1100 interrupt; the completion of an R7912 memory load cycle (end of a digitizing operation). This occurs in single sweep mode with every sweep. In repetitive sweep mode, it occurs after every sweep that was preceded by a load memory command. Once such a condition has occurred, the R7912 will request an interrupt and continue doing so until its request is set into the status word (or until a CP1100 hardware reset is performed). When more than one R7912 requests an interrupt at one time, the unit with the highest device number is serviced first. A CP1100 INIT or RESET command will clear any R7912 interrupts and the busy flag.

Timing

When the Controller receives an interrupt, it will acknowledge by setting $\overline{S1}$, $\overline{S2}$, $\overline{S3}$, $\overline{CBBZY}$, $\overline{BQ1}$, and $\overline{BQ2}$. Signals $\overline{S1}$, $\overline{S2}$, and $\overline{S3}$ determine which device will be addressed. These three lines carry the BCD representation of the selected device number.

$\overline{BQ1}$ and $\overline{BQ2}$ are control lines which tell the external device which function to perform. There are four states for these lines: Both low, Both high, $\overline{BQ1}$ high and $\overline{BQ2}$ low, and $\overline{BQ1}$ low and $\overline{BQ2}$ high.

Figure 2-2 shows the states and lists the function the device will perform for that state.

SEE FIG:	$\overline{BQ1}$	$\overline{BQ2}$	FUNCTION
2-3	LOW	HIGH	XFR ADDRESS TO DEVICE
2-4	LOW	LOW	START READ CYCLE
2-4	HIGH	HIGH	CONTINUE READ CYCLE (TRANSFER DATA FROM DEVICE)
2-5	HIGH	LOW	SEND DATA TO DEVICE

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Fig. 2-2. $\overline{BQ1}$ and $\overline{BQ2}$ Function Commands.

Timing diagrams for each of the four states are shown in figures 2-3, 2-4 and 2-5. Each setting of $\overline{BQ1}$ and $\overline{BQ2}$ listed in Fig. 2-2 refer to the figure containing its timing diagram. For example: $\overline{BQ1}$ LOW and $\overline{BQ2}$ HIGH indicates the function of transferring an address to the device and refers to Fig. 2-3 for its timing diagram. These timing diagrams are for the CP1100 Controller and the CP1100/CP Bus Interface. They may differ slightly from the ideal timing diagrams shown in the DPO/CP Bus Interface and the R7912/CP Bus Interface.

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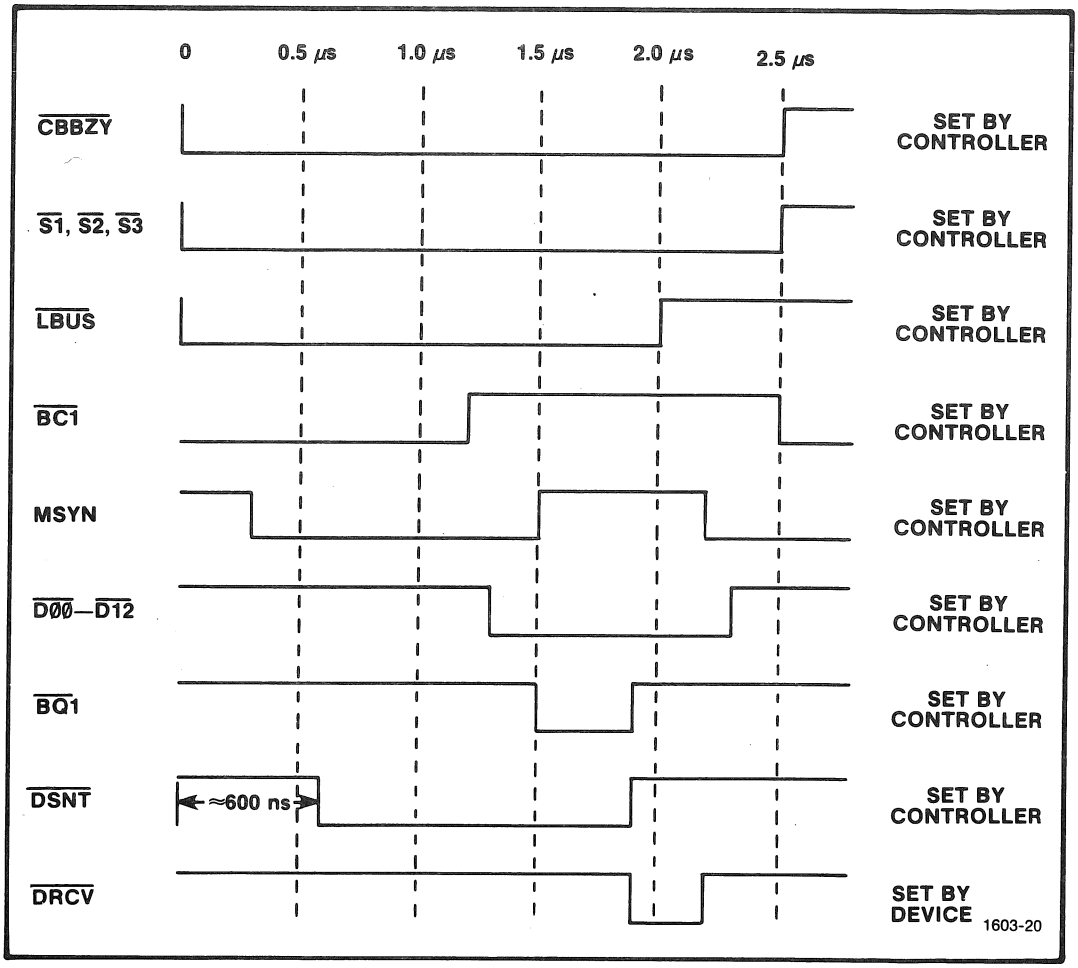

Fig. 2-3. ADDRESS/COMMAND WORD Transfer From CP1100 Controller.

Address/Command Cycle. When the Controller answers an interrupt or wants to contact a device, it asserts the device select code ($\overline{S1}$, $\overline{S2}$, $\overline{S3}$) and sets $\overline{CBBZY}$, and $\overline{BQ1}$ (Fig. 2-3). The Controller then sets the Address or Command Word on bus lines $\overline{CB0}$-$\overline{CB12}$ (Diag. 14C). After approximately 300 nanoseconds, to allow the data to settle, the Controller issues $\overline{DSNT}$. If everything is right, the device will answer with $\overline{DRCV}$.

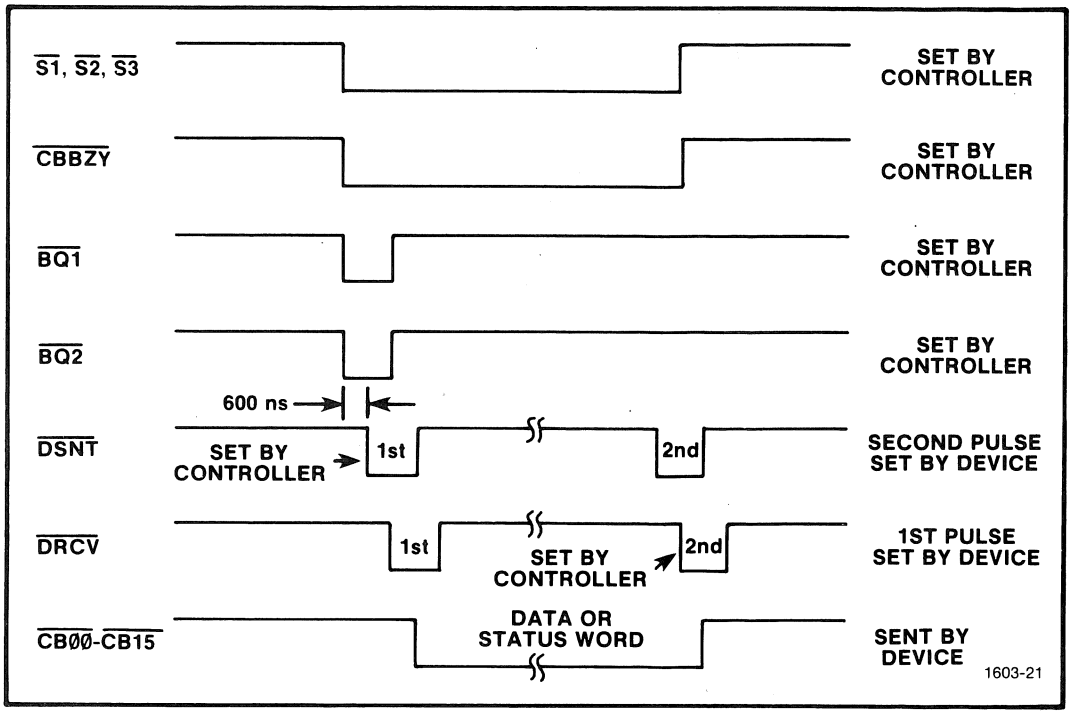

Fig. 2-4. READ CYCLE Timing Diagram.

Read Start. For the Controller to read data from the device, it must send the proper address or command and then start the read cycle by asserting the device select code ($\overline{S1}$, $\overline{S2}$, $\overline{S3}$), $\overline{CBBZY}$, $\overline{BQ1}$ and $\overline{BQ2}$ (Fig. 2-4). This tells the device that it wants to read data at the address previously sent.

Read Cycle. After the Read Start command has been sent, the Controller starts the Read Cycle. $\overline{BQ1}$ and $\overline{BQ2}$ are set low, $\overline{DSNT}$ is set by the Controller, and $\overline{DRCV}$ is then received from the device. $\overline{BQ1}$ and $\overline{BQ2}$ are brought back high by the Controller and the data or status word is placed on the CP Bus by the device. When complete, the device sends $\overline{DSNT}$. The Controller answers with $\overline{DRCV}$.

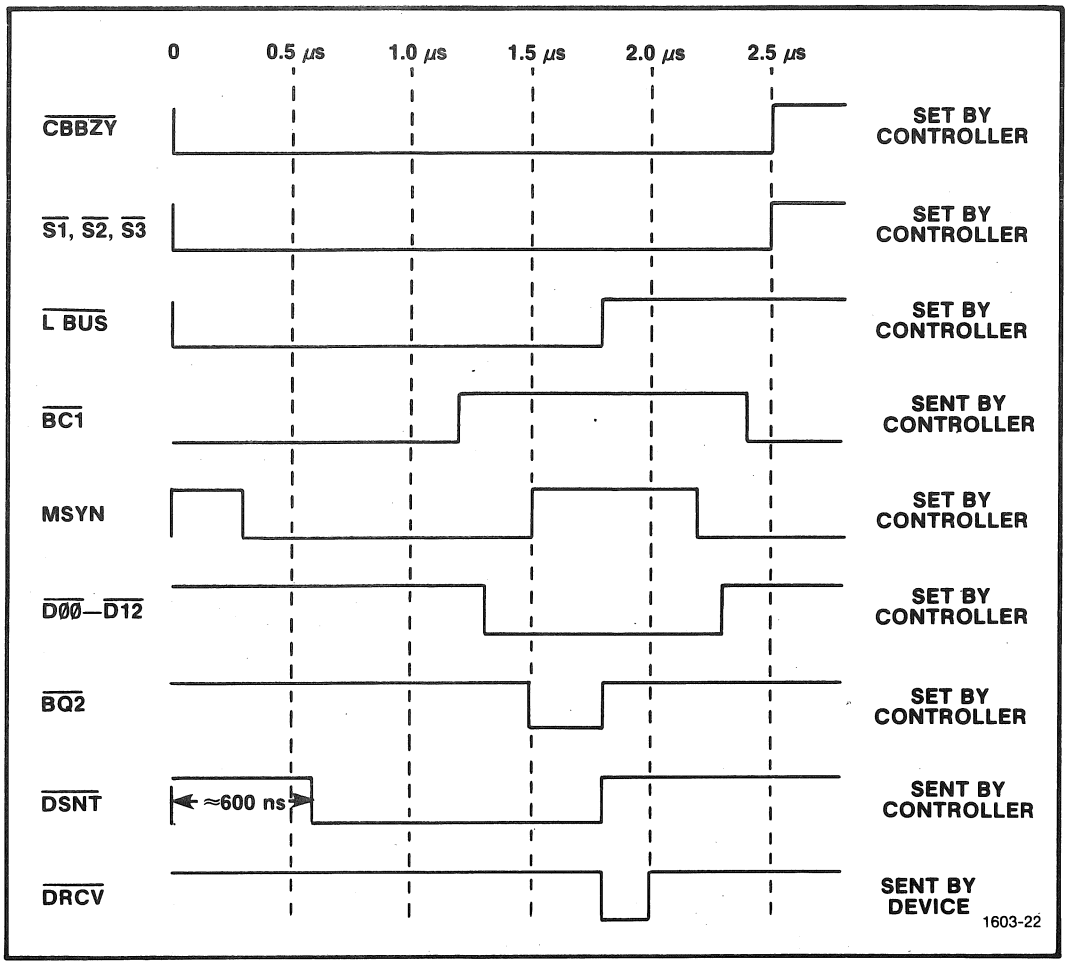

Fig. 2-5. Write Data in DPO Memory.

Write Cycle. No data is written in the R7912 Memory by the Controller. However, the DPO Memory can receive data from the Controller. Fig. 2-5 shows the timing flow for this function.

Again, the Controller must address the DPO in the same manner as for a Read Cycle, setting $\overline{S1}$, $\overline{S2}$, $\overline{S3}$, $\overline{CBBZY}$, and $\overline{BQ1}$ (see Fig. 2-3). After addressing is completed, $\overline{S1}$, $\overline{S2}$, $\overline{S3}$, $\overline{CBBZY}$, and $\overline{BQ2}$ are asserted. The data is then placed on the Bus, ($\overline{CB0}$-$\overline{CB15}$). 300 nanoseconds later, $\overline{DSNT}$ is sent by the Controller and held during the time that data is on the bus. When $\overline{DRCV}$ is sent by the DPO, $\overline{DSNT}$ is lifted. The R7912 will answer immediately with $\overline{DRCV}$ when addressed with a Write command.

Registers

There are four registers used by the CP1100/CP Bus Interface during transfer of information. They are the Address/Register (DPO), Command Register (R7912), Data Register, and Status Register. Fig. 2-6 shows the location of each of these registers. The Status Register is in the CP1100/CP Bus Interface only. The Address Register is located in the DPO/CP Bus Interface and is called the DPO Address Register (DAR). The Command Register for theR7912 is located on the R7912/CP Bus Interface Card. Each DPO and R7912/CP Bus Interface has a Data Register.

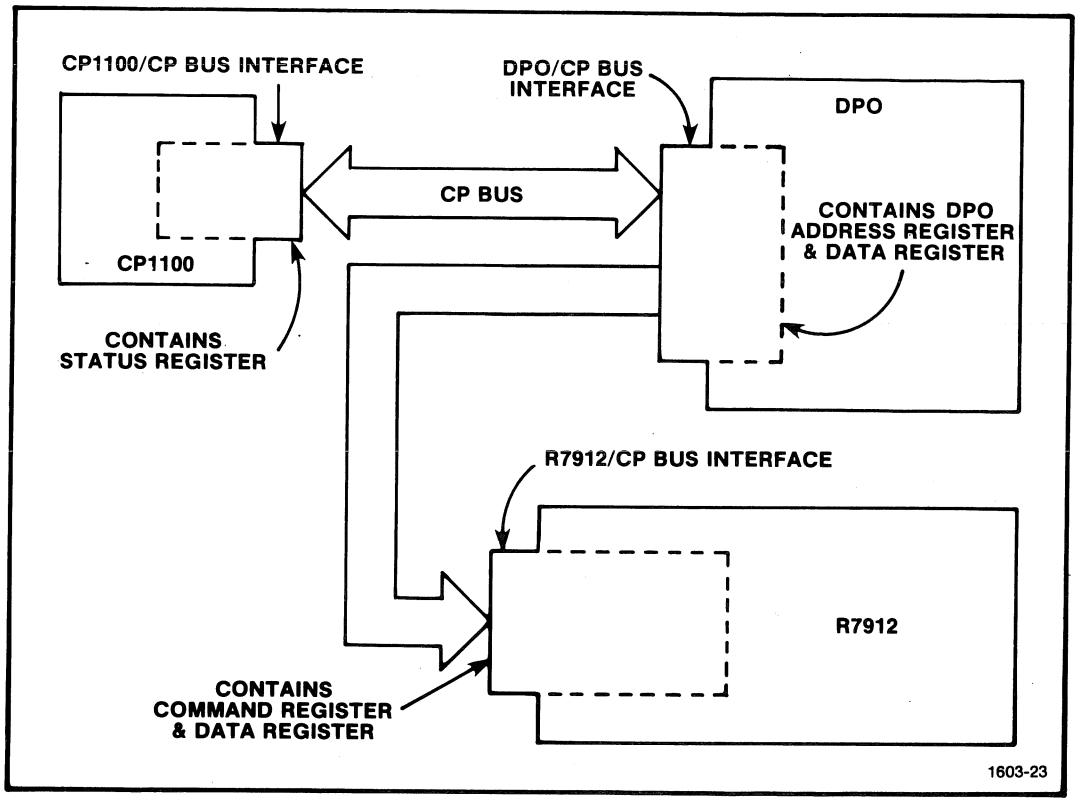

Fig. 2-6. Location of Registers.

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Address Registers. Before any transfer between the CP1100 and a device (DPO or R7912) can occur, the two interface cards must establish an address from which or to which the data is coming or going. The CP1100 establishes the device or command address by setting up the DAR or Command Register with the device or command address. This causes no action or transfer of data. It only alerts the interface for the forthcoming data by first sending the desired address.

1) DAR-DPO ADDRESS REGISTER. The DAR is a 13-bit register located on the DPO/CP Bus Interface card. When data is written into the DAR, the 13 low order bits of the CP1100 Controller will be placed into the DAR. If a READ operation is attempted from the DAR, a value of zero will be returned and the contents of the DAR will remain unchanged. Addresses normally sent to the DAR are sent in the format shown in Fig. 2-7.

2) COMMAND REGISTER. The R7912/CP Bus Interface has a register similar to the DAR. It performs the same function of receiving the Command word from the CP1100 (see Fig. 2-8).

DATA Registers. After an address has been set in the DAR or Command Register, data is transferred to or from the CP1100 through the Data Register. Each interface on the other end of the CP Bus will have a Data Register. Data is transferred as a full 16-bit word in a parallel fashion which is an immediate (non-byte) operation.

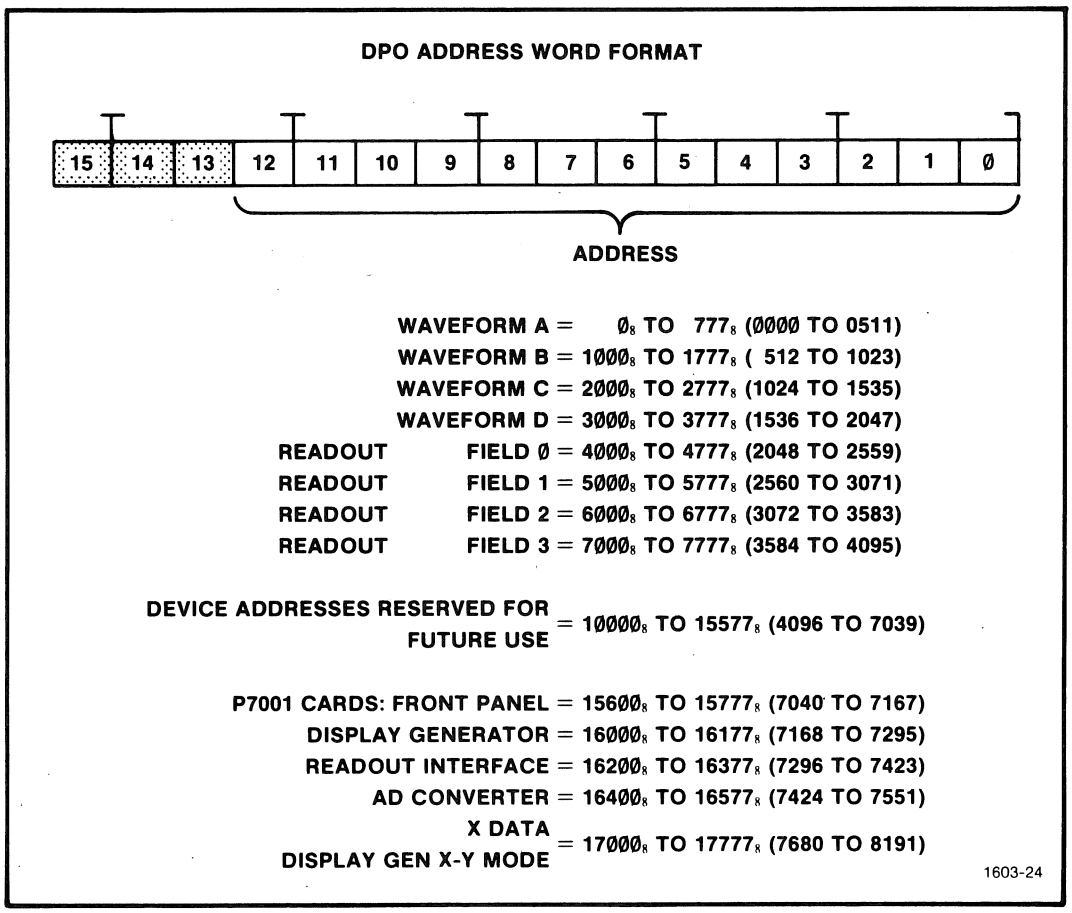

Fig. 2-7. DPO Address Word Format.

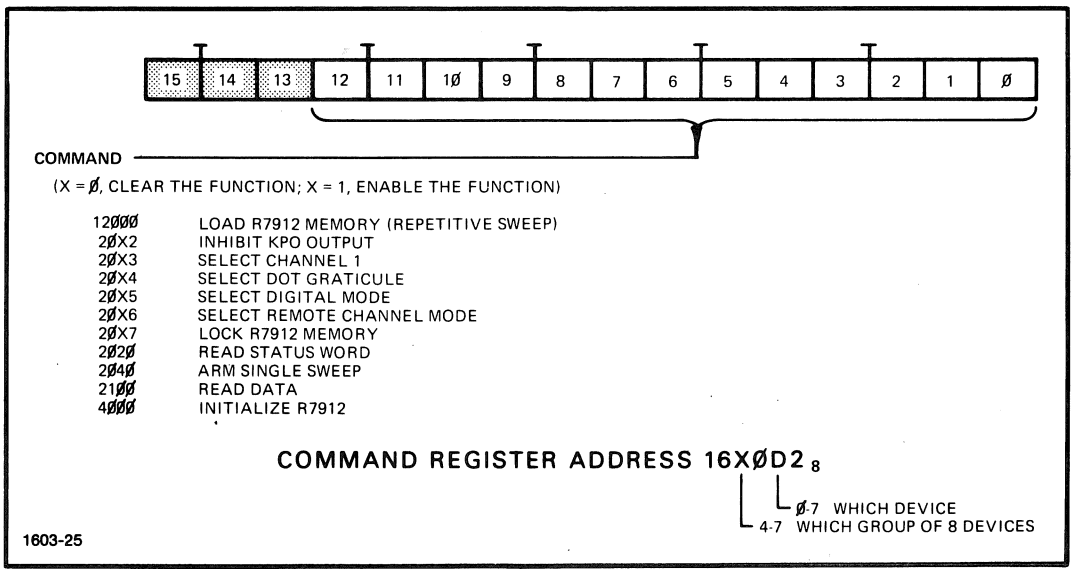

Fig. 2-8. R7912 Command Word Format.

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1) DPO DATA REGISTER (DDR). There are basically two types of information sent to and received from the DDR. They are Status Words and Data. Status Words are instructions to the cards in the P7001 (processor part of the DPO) which tell them what actions to take, i.e., STORE, HOLD, etc. Data is the converted vertical data from the A-D Converter, ASCII data or vertical data to or from the P7001 Memory, or vertical data to the Display Generator. Formats are shown in Fig. 2-9 and 2-10.

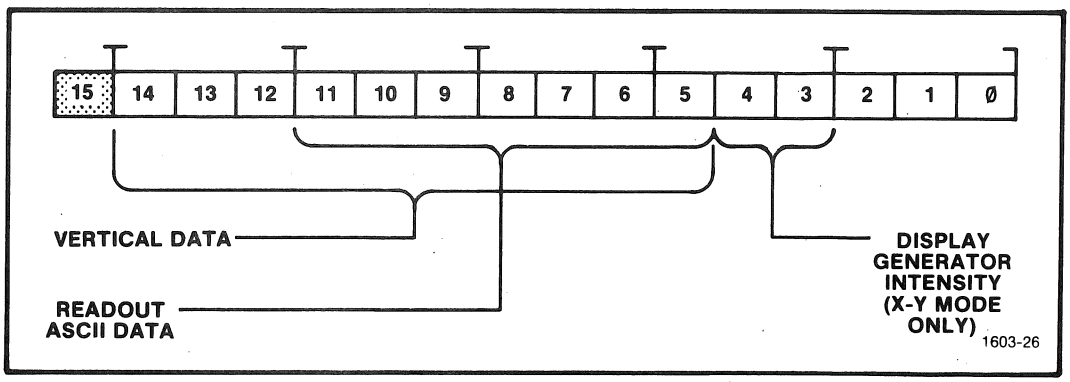
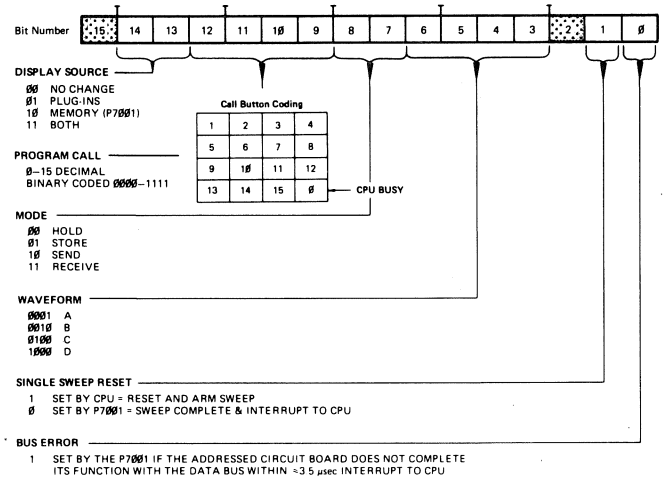
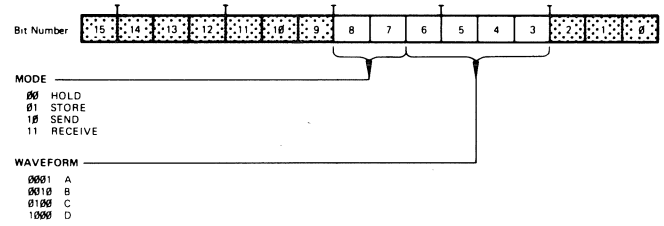


Fig. 2-9. DPO Data Word Format.

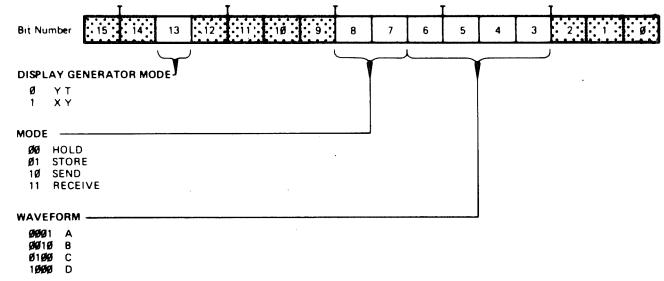
2) R7912 - DATA REGISTER. All information supplied to the CP1100 Controller by the R7912 is sent via its Data Register. After a Command Address has been sent, and a Read Data command is issued, the R7912 sends all the data values of the waveform currently stored in its memory to the Data Register. Each time the register is read, the next data value is placed in it. Fig. 2-11 shows the R7912 Data Word Format.



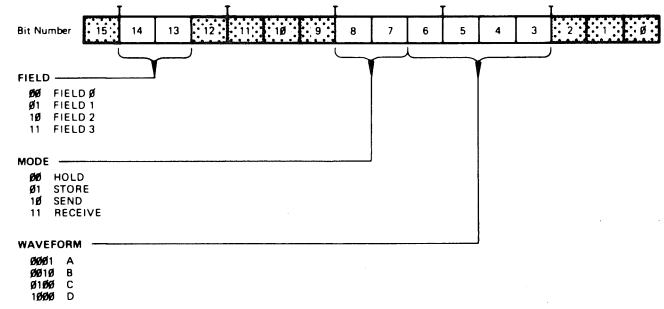
(a). FRONT PANEL STATUS WORD FORMAT.



(b). A/D CONVERTER STATUS WORD FORMAT.



(c). DISPLAY GENERATOR STATUS WORD FORMAT.



(d). READOUT INTERFACE STATUS WORD FORMAT.

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Fig. 2-10. DPO Status Word Formats.

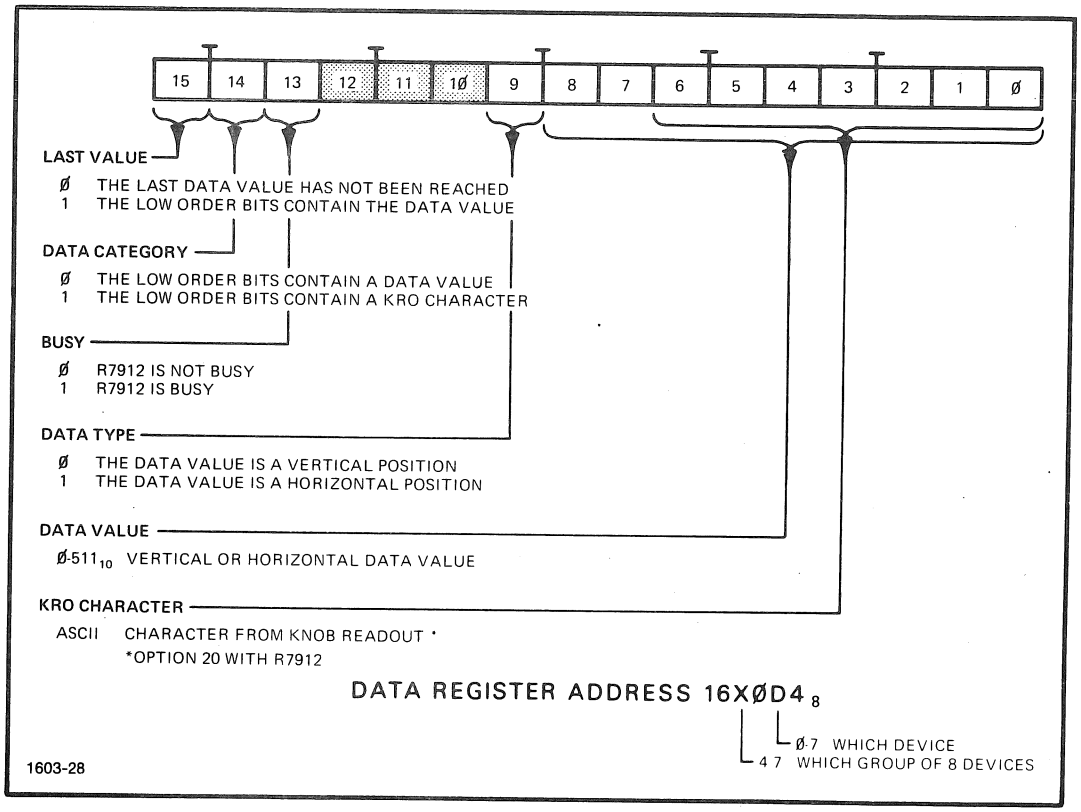

Fig. 2-11. R7912 Data Word Format.

Status Register. This register is different from the Address and Data Registers in that this is located on the CP1100/CP Bus Interface Card (Diag. 14A). When the Status Register is addressed by the CP1100, the device number (bits 3, 4, and 5) is ignored (Fig. 2-12). The Status Register controls the interrupt processing of the devices on the other end of the CP Bus (up to eight DPOs and/or R7912s). When the device wishes to cause an interrupt in the CP1100, its device number is set into bits 3, 4, and 5. Interrupt pending (IPEND) is set only if the interrupt enable (bit 6) is set. When an interrupt from a device occurs, the CP1100 reads the status register and determines the device number of the interrupting device.

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No further device interrupts will be recognized until both a CP1100 interrupt has occurred and the status register is written into. If the interrupt enable bit is not set, device interrupt requests are not set in the Status Register. They cannot be detected until after the interrupt enable bit is set. The format of the CP1100 Controller Status Word is shown in Fig. 2-12.

Attempting to write into the Status Register will reset the status word to all zeros. (Except bit 6, which when the Status Register is addressed arms the interrupt circuitry.)

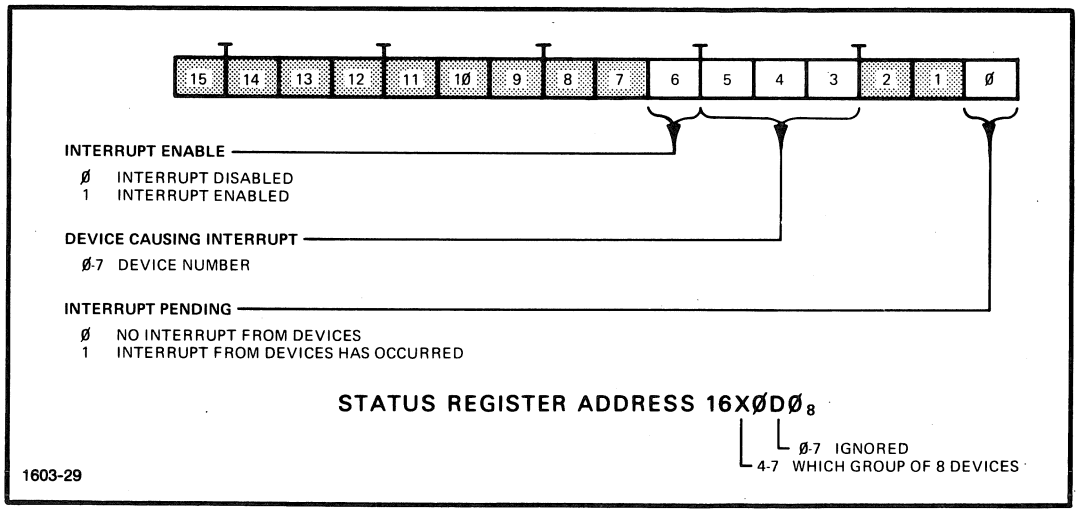

Fig. 2-12. CP1100 Controller Status Word Format.

Addressing

The CP1100 must perform two addressing steps to set up the device so it can perform a particular function. The CP1100 sends an address to one of the CP1100/CP Bus Interface cards telling it which one of its eight devices it wants to contact. Then the Controller sends another address to one of the device addresses. Once

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the second address is established, the Status word or data may be sent to or received from the device.

CP1100/CP Bus Address Decoder

Addresses from the CP1100 Controller come in on lines $\overline{A0}$ thru $\overline{A17}$ shown on the left side of diagram 14A. The address format for the three registers (Address, Data, and Status) is $16X\emptyset DR_8$, where X is the card number of the CP1100/CP Bus Interface (up to four cards), see Fig. 1-14. The numbers can be either 4, 5, 6, or 7. "D" is the device number, Ø through 7 (for the eight devices on each of the Interface cards).

R can be Ø, 2 or 4 representing the register:

R=Ø Status Register

R=2 DPO Address Register or R7912 Command Register

R=4 Data Register

Example:

If we have CP1100/CP Bus Interface #4, device #Ø, and we want to address the DPO Address Reigster, then the address coming from the CP1100 would be 164002_8. Fig. 2-13 shows the address word for address 164002_8.

ADD BITS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø
BINARY	1	1	1	Ø	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	Ø
OCTAL	1	6			4			Ø			Ø			2		

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Fig. 2-13. ADDRESS WORD.

If Data is coming from the device to the CP1100, the signal $\overline{\text{UNLOAD BUS}}$ will gate it through from left to right. To transfer data in the opposite direction, CP1100 to the device, $\overline{\text{L BUS}}$ gates the data through.

At the lower right of diagram 14A, lines $\overline{\text{D00}}$ thru $\overline{\text{D07}}$ are duplicates of the $\overline{\text{D00}}$ thru $\overline{\text{D07}}$ lines going to the CP1100 in diagram 14C.

For the address shown in Fig. 2-13, starting in the upper left side of diagram 14A, the lines will have the following condition: $\overline{\text{A0}}$ is LOW, $\overline{\text{A2}}$ thru $\overline{\text{A10}}$ are LOW, A11 is HIGH, $\overline{\text{A12}}$ is LOW, and $\overline{\text{A13}}$, $\overline{\text{14,15}}$ are LOW. $\overline{\text{A16 and 17}}$ are hard wired in the CP1100 to HIGHs, with the exception of the CP1160, bits $\overline{\text{A16}}$ and $\overline{\text{A17}}$ are set HIGH by software when addressing this Interface. This address will be decoded by the several sets of AND gates so that one of the three registers will be selected by U22B (DAR Gate), U21B, (DDR Gate), or U22A (Status Gate).

With the address set in this manner we have address 164002_8. This address tells the device to get ready to load another address to follow. After this address (164002_8) is set the CP1100 sends MYSN to the CP1100/CP Bus Interface which in turn generates LBUS and $\overline{\text{LBUS}}$. $\overline{\text{LBUS}}$ goes over to diagram 14C and turns on all the NAND gates on the left-hand side, passing whatever information is on the CP1100 Bus to the Common Bus lines (CP Bus).

The Q output from U24B (Diag. 14A), Load Bus FF, turns on NAND Gates U04C and U04D to load $\overline{\text{BQ1}}$ and $\overline{\text{BQ2}}$ on to the CP Bus. It also

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starts the Data Sent Generator (diag. 14B). When L BUS is received, it sets one shot U46A to its unstable state where it remains for about 275 nanoseconds. After it has timed out, the $\overline{Q}$ output goes high, clocking U45B's D input (L BUS) to its Q output. This goes over to U05. It also goes through a delay network, U40C and U62B, and then to the other input of U05C. The output from U05C is delayed from L BUS by about 300 nanoseconds. This delay is necessary to prevent a $\overline{DSNT}$ (data sent) from being interpreted as a $\overline{DRCV}$ (data received). This is sent on the Common Bus (CP Bus) as $\overline{DSNT}$. $\overline{DSNT}$ lets a device on the other end of the CP Bus know that the data has been sent by the CP1100.

When the device receives the data it will send back $\overline{DRCV}$. This goes to U25C, diagram 14B, pin 10. Pin 9 of this NAND Gate is low (set by L BUS), so U25C will pass $\overline{DRCV}$. This fires one shot U46B (150 nanoseconds). Its output goes through U02C and U03B and switches the DONE Flip-Flop U02B. C1 input (pin 9) to U02C is set by the Bus Control line (BC1-write mode) on diagram 14A.

Notice that MSYN will also switch the BUS BUSY Flip-Flop, U24A (diag. 14A). This pulls $\overline{CBBZY}$ low, holding the Common Bus. It gates CS1, CS2, and CS3 (the device select information) onto the Common Bus lines where they become $\overline{S1}$, $\overline{S2}$, and $\overline{S3}$. The $\overline{Q}$ output from U24A will also inhibit U10D, U10C, and U10B, preventing the S1, S2, and S3 outputs from the Interrupt Latch from going onto the CP Bus.

Mnemonics Table

The following Mnemonics table is included to aid in following through the circuit diagrams and the circuit description:

ARM = Enable Interrupt

BG = Bus Grant

BQ1, BQ2 = Bus Q1 and Bus Q2. Central lines which indicate action to be taken on a bus.

Q1	Q2	Function
Ø	Ø	DATA from DDR
Ø	1	DATA to DDR
1	Ø	DATA to DAR
1	1	Start Read

$\overline{BS1}$, $\overline{BS2}$, $\overline{BS3}$ = Bus Select 1, 2, and 3. Device code for addressed instrument.

BZY = Bus Busy

BZYF = Bus Busy Flip-Flop

C1 = Write Cycle

$\overline{C1}$ = Read Cycle

$\overline{CBØ}$-$\overline{CB15}$ = Common Bus Ø to 15 Data Lines

$\overline{CBBZY}$ = Common Bus Busy

$\overline{CLI}$ = Clear Interrupt. Indicates receipt of an interrupt request.

$\overline{CLR}$ = Clear. A master clear signal applied by the computer.

CMPR = Compare

$\overline{CQ}$ = Clear Q's

CS1, CS2, CS3 = Call Select #1, #2, or #3

DØØ-D15 = CP1100 Data Lines

DAR = DPO Address Register

DDR = DPO Data Register

DDRCV = Delayed Data Received

Disarm = Disenable Interrupt

Done = End of cycle designator (to PDP-11)

$\overline{DRCV}$ = Data Received

$\overline{DSNT}$ = Data Sent. Indicates presence of valid data on lines CBØ-CB15.

EOBC = End of Bus Cycle

$\overline{EOC}$ = End of Cycle (to I/O Bus Controller)

GIV = Grant Interrupt Vector

IDLE = Idle status of DPO

INT = Interrupt

IPEND = Interrupt Pending

LAD = Load Address

LBUS = Load Bus

LDW = Load Data on Write Cycle

NSYN = No Sync

OMIT = Device Selected

$\overline{RF}$ = Read Flop

S1, S2, S3 = Select #1, #2, and #3

SRD = Start Read

STAT = Status Register

$\overline{SSYN}$ = Start Sync

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SECTION 3

MAINTENANCE

Preventive Maintenance

The CP1100/CP Bus Interface Card requires no calibration. However, the card should be removed and cleaned during normal service of the CP1100 Series Controller.

Troubleshooting

If problems should develop in the Interface, the circuit description will prove helpful in locating the fault. The failure symptoms should be carefully noted. Loss of a circuit function will will isolate the problem area to those components providing that function.

The circuit card is a multilayer type and requires careful soldering techniques. Avoid heating the card excessively. Remove component leads from the card with care. The integrated circuits on the interface card may be socket-mounted. If so, component replacement is straightforward. Should the IC's be soldered in, a solder removal tool is required. Carefully remove the solder from each lead of the suspect IC. Apply as little heat and pressure as possible during removal.

Obtaining Replacement Parts

All parts for the CP1100/CP Bus Interface Card can be obtained from a local Tektronix Field Office or representative.

Many of the standard components can be obtained more quickly through local distributors, however.

When obtaining replacement parts, it is important to remember that component size and electrical characteristics are often critical, and exact replacements should be used wherever possible. Substitutions should be made only when it is known that a different component will not adversely affect instrument performance.

When ordering parts from Tektronix, Inc., include the following information:

1) Instrument type

2) Instrument Serial number

3) Circuit Card number

4) A description of the part

5) Tektronix Part number

If the circuit card is damaged beyond repair, the entire assembly, including all soldered-in components, can be replaced. Part numbers for the complete card can be found in the Parts Lists.

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REPLACEABLE PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

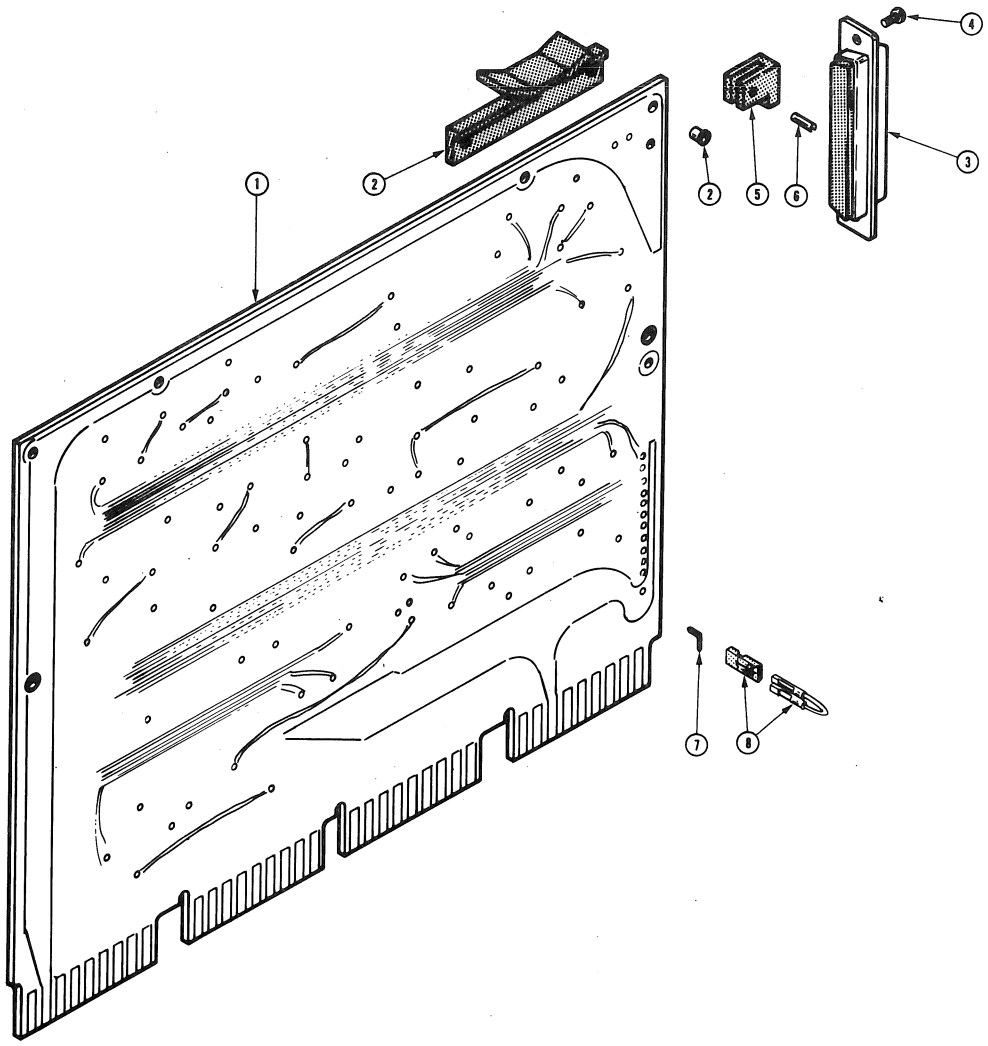
CROSS INDEX MFR. CODE NUMBER TO MANUFACTURER

MFR.CODE	MANUFACTURER	ADDRESS	CITY,STATE,ZIP
00779	AMP, INC.	P. O. BOX 3608	HARRISBURG, PA 17105
01121	ALLEN-BRADLEY CO.	1201 2ND ST. SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P. O. BOX 5012	DALLAS, TX 75222
04713	MOTOROLA, INC., SEMICONDUCTOR PRODUCTS DIV.	5005 E. MCDOWELL RD.	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS ST.	MOUNTAIN VIEW, CA 94042
14099	SEMTECH CORP.	652 MITCHELL ROAD	NEWBURY PARK, CA 91320
15476	DIGITAL EQUIPMENT CORP.	146 MAIN ST.	MAYNARD, MA 01754
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SAN YSIDRO WAY	SANTA CLARA, CA 95051
56289	SPRAGUE ELECTRIC CO.		NORTH ADAMS, MA 01247
71468	ITT CANNON ELECTRIC	666 E. DYER RD.	SANTA ANA, CA 92702
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BlVD.	FULLERTON, CA 92634
80009	TEKTRONIX, INC.	P. O. BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
	670-2383-02			CKT CARD ASSY:PDP-11 CONTROLLER	80009	670-2383-02
C01	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C03	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C05	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C07	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C09	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C11	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C12	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C13	290-0533-00			CAP.,FXD,ELCTLT:330UF,20%,,6V	56289	196D337X006MA3
C25	283-0065-00			CAP.,FXD,CER DI:0.001UF,5%,100V	72982	805-505B102J
C32	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C41	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C43	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C46	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C48	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C50	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C52	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C60	283-0065-00			CAP.,FXD,CER DI:0.001UF,5%,100V	72982	805-505B102J
C70	281-0589-00			CAP.,FXD,CER DI:170PF,5%,500V	72982	301-057Z5D0171J
C72	281-0637-00			CAP.,FXD,CER DI:91PF,5%,500V	72982	301-000Z5D0910J
C74	283-0065-00			CAP.,FXD,CER DI:0.001UF,5%,100V	72982	805-505B102J
C76	283-0065-00			CAP.,FXD,CER DI:0.001UF,5%,100V	72982	805-505B102J
C80	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C81	283-0065-00			CAP.,FXD,CER DI:0.001UF,5%,100V	72982	805-505B102J
C82	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C84	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C85	281-0623-00			CAP.,FXD,CER DI:650PF,5%,500V	72982	301-000Y5D0651J
C86	290-0533-00			CAP.,FXD,ELCTLT:330UF,20%,,6V	56289	196D337X006MA3
C88	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C89	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C91	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
CR10	152-0066-01			SEMICOND DEVICE:SILICON,400V,750MA	14099	SM4
CR11	152-0066-01			SEMICOND DEVICE:SILICON,400V,750MA	14099	SM4
Q85	151-0190-00			TRANSISTOR:SILICON,NPN	80009	151-0190-00
R11	307-0347-00			RES.,FXD,FILM:220 OHM,2%,1.5W	73138	899-1-R220
R31	307-0347-00			RES.,FXD,FILM:220 OHM,2%,1.5W	73138	899-1-R220
R66	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R70	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R72	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R74	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R76	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R80	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
R81	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
R85	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R86	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
R87	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R89	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
U00	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U01	156-0043-00			MICROCIRCUIT,DI:2-INPUT NOR GATE	01295	SN7402N
U02	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U03	156-0129-00			MICROCIRCUIT,DI:QUAD 2-INPUT GATE	01295	SN7408N

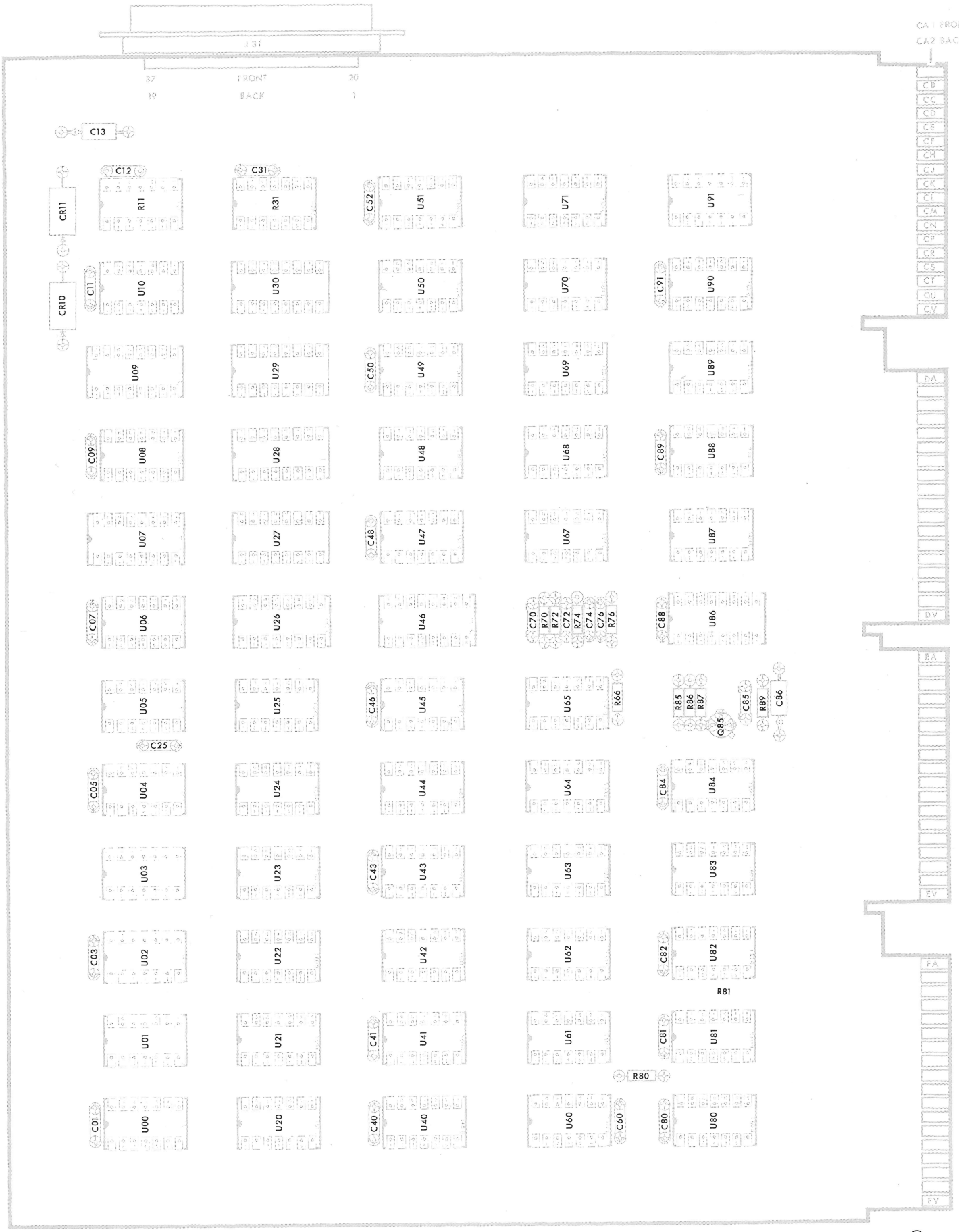
Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U04	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U05	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U06	156-0163-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT POS AND GATE	18324	N7411A
U07	156-0219-00			MICROCIRCUIT,DI:8-INPUT PRIORITY DCDR	07263	9318DC
U08	156-0058-00			MICROCIRCUIT,DI:HEX INVERTER	04713	MC7404P
U09	156-0221-00			MICROCIRCUIT,DI:QUAD LATCH	01295	SN74175N
U10	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U20	156-0150-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7437N
U21	156-0129-00			MICROCIRCUIT,DI:QUAD 2-INPUT GATE	01295	SN7408N
U22	156-0129-00			MICROCIRCUIT,DI:QUAD 2-INPUT GATE	01295	SN7408N
U23	156-0041-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U24	156-0041-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U25	156-0456-00			MICROCIRCUIT DI:QUAD 2-INPUT NOR BUS REC	27014	DM8836N
U26	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	01295	SN74174N
U27	156-0455-00			MICROCIRCUIT,DI:HEX.BUS VEC	27014	DM8837N
U28	156-0455-00			MICROCIRCUIT,DI:HEX.BUS VEC	27014	DM8837N
U29	156-0455-00			MICROCIRCUIT,DI:HEX.BUS VEC	27014	DM8837N
U30	156-0455-00			MICROCIRCUIT,DI:HEX.BUS VEC	27014	DM8837N
U40	156-0058-00			MICROCIRCUIT,DI:HEX INVERTER	04713	MC7404P
U41	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U42	156-0058-00			MICROCIRCUIT,DI:HEX INVERTER	04713	MC7404P
U43	156-0047-00			MICROCIRCUIT,DI:3-INPUT NAND GATE	01295	SN7410N
U44	156-0041-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U45	156-0041-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U46	156-0172-00			MICROCIRCUIT,DI:DUAL MONOSTABLE MV	01295	SN74123N
U47	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U48	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U49	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U50	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U51	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U60	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U61	156-0047-00			MICROCIRCUIT,DI:3-INPUT NAND GATE	01295	SN7410N
U62	156-0178-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NOR GATE	01295	SN7427N
U63	156-0255-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	18324	SP380A
U64	156-0163-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT POS AND GATE	18324	N7411A
U65	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U67	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U68	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U69	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U70	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U71	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U80	156-0255-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	18324	SP380A
U81	156-0255-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	18324	SP380A
U82	156-0255-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	18324	SP380A
U83	156-0255-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	18324	SP380A
U84	156-0255-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	18324	SP380A
U86	156-0172-00			MICROCIRCUIT,DI:DUAL MONOSTABLE MV	01295	SN74123N
U87	156-0255-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	18324	SP380A
U88	156-0255-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	18324	SP380A
U89	156-0255-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	18324	SP380A
U90	156-0255-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	18324	SP380A
U91	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N

EXPLODED



Mechanical Parts List

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
1-1	----- -----			-	CKT BOARD ASSY:PDP-11 CONTROLLER		
-2	367-0183-00			2	. PULL,CKT CARD:GRAY PLASTIC	15476	0937
-3	131-0972-00			1	. CONN,RCPT,ELEC:37 PIN,FEMALE	71468	DC37S-14
					(ATTACHING PARTS)		
-4	211-0022-00			2	. SCREW,MACHINE:2-56 X 0.188,PNH,STL	83385	OBD
					- - - * - - -		
-5	386-2642-00			2	. SUPPORT,CONN:PLASTIC	80009	386-2642-00
					(ATTACHING PARTS FOR EACH)		
-6	214-1337-00			1	. PIN,SPRING:0.10 OD X 0.25 INCH LONG	80009	214-1337-00
					- - - * - - -		
-7	131-0589-00			24	. TERMINAL,PIN:0.46 INCH LONG	22526	47350
-8	131-0993-00			8	. LINK,TERM CONNE:JUMPER	00779	530153-2



CP1100/CP BUS INTERFACE

@

TO CP1100

EH2 $\overline{A0}$ U82B 380
EH1 $\overline{A1}$ U63A 380
EF1 $\overline{A2}$ U63B 380
EV2 $\overline{A3}$ U80B 380
EU2 $\overline{A4}$ U80C 380
EV1 $\overline{A5}$ U80D 380
EU1 $\overline{A6}$ U81D 380
EP2 $\overline{A7}$ U82A 380
EN2 $\overline{A8}$ U82C 380
ER1 $\overline{A9}$ U81C 380
EP1 $\overline{A10}$ U81B 380
EL1 $\overline{A11}$ U84B 380
EC1 $\overline{A12}$ U84B 380
EK2 $\overline{A13}$ U83D 380
EK1 $\overline{A14}$ U83C 380
ED2 $\overline{A15}$ U83C 380
EE2 $\overline{A16}$ U63D 380
ED1 $\overline{A17}$ U63D 380
EF2 $\overline{BC1}$ U83B 380

U40E 7404
U40F 7404
U41A 7400
U62A 7427
U62C 7427
U64C 7411
U64B 7411

ADDRESS DECODER
ADDRESSED

REGISTER DECODER
U42B 7404
U42A 7404
U21C 7408
U21A 7408
U21D 7408
U22B 7408
U21B 7408
U22A 7408

MSYN
DAR
CMPR
$\overline{CMPR}$
DDR
U01A 7402
U00D 7400
U43A 7410
STATUS
CS1
CS2
CS3

U44B 7474 Q1 F.F.
U44A 7474 Q2 F.F.
U64A 7411
U24B 7474 LOAD BUS F.F.
U24A 7474 BUS BUSY F.F.
U04A 7438
$\overline{UL\ BUS}$
$\overline{END}$
L BUS
$\overline{CLR\ Q}$
Q1
Q2
$\overline{BQ1}$
$\overline{BQ2}$
U04C 7438
U04D 7438
$\overline{CBBZY}$

+5.1V
C01 .05 C03 .05 C05 .05 C07 .05 C09 .05 C11 .05 C41 .05 C43 .05 C46 .05 C48 .05 C50 .05
C52 .05 C80 .05 C82 .05 C84 .05 C88 .05 C89 .05 C91 .05 C86 330µF
R87 1k
CR10
CR11
C12 .05 C32 .05 C13 330µF
+3V
GND
CT1 CC2 DT1 DC2 ET1 EC2 FT1 FC2
CA2 DA2 EA2 FA2

INTERRUPT PRIORITY ENCODER
U07 9318
U27C 8837
U27F 8837
U28A 8837
U28F 8837
U08D 7404
U08E 7404
U29A 8837
U29F 8837
T0 T1 T2 T3 T4 T5 T6 T7
U08B 7404
U08C 7404
U08A 7404
U08F 7404
U00C 7400
STAT
$\overline{C1}$
C1
U06C 7411
WST
U01B 7402
U42F 7404
U06A 7411

INTERRUPT CLOCK
R74 4.7k C74 .001
R76 4.7k C76 .001
U86B 74123
U86A 74123
ARM

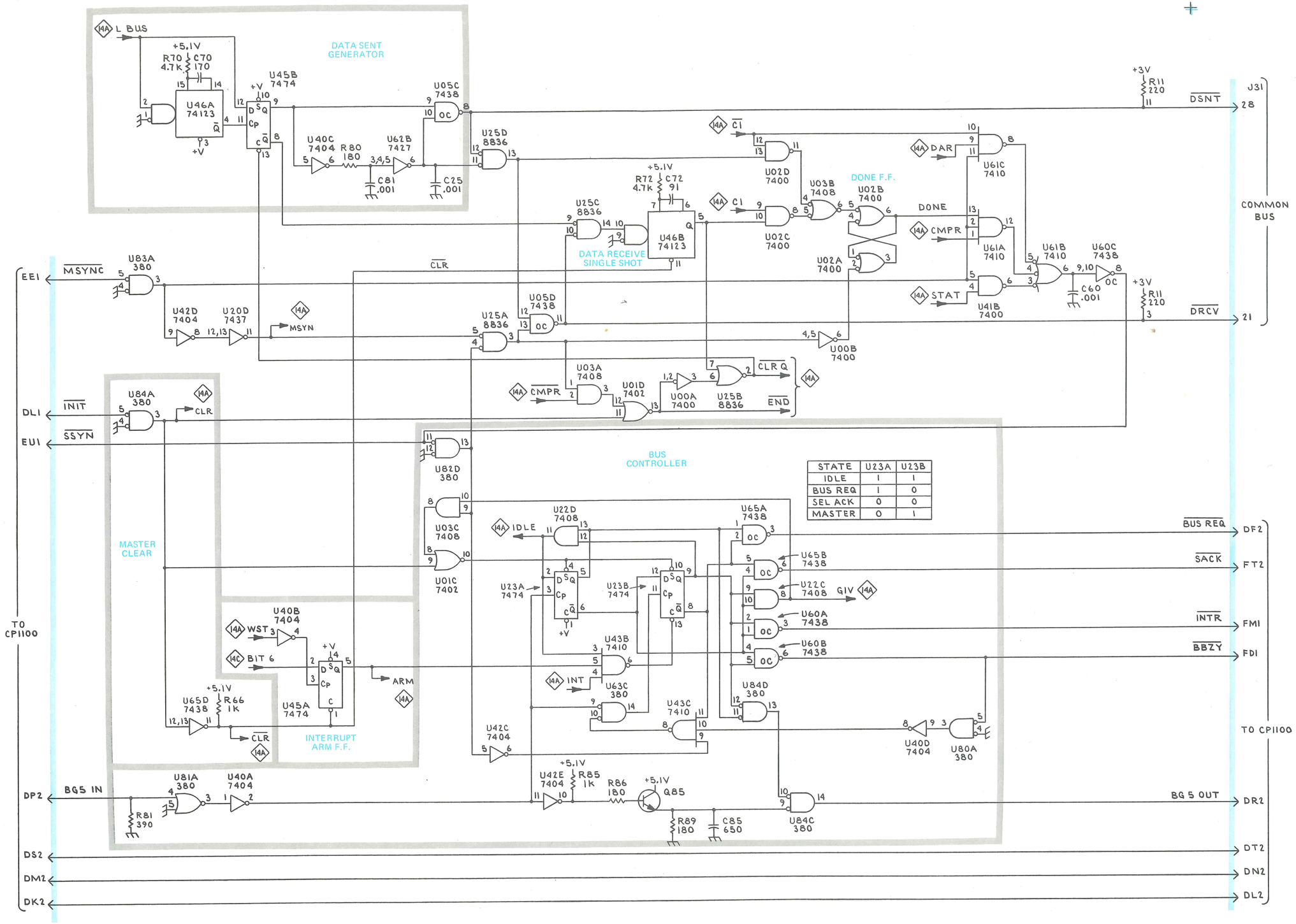
INTERRUPT LATCH
U09 74175
S3 S2 S1 IPEND

INTERRUPT SHIFT REGISTER
U03D 7408
U27A 8837
U27B 8837
U26 74174
U06B 7411
U05A 7438
GIV
INT
IDLE
$\overline{CLR}$
CLR
U04B 7438

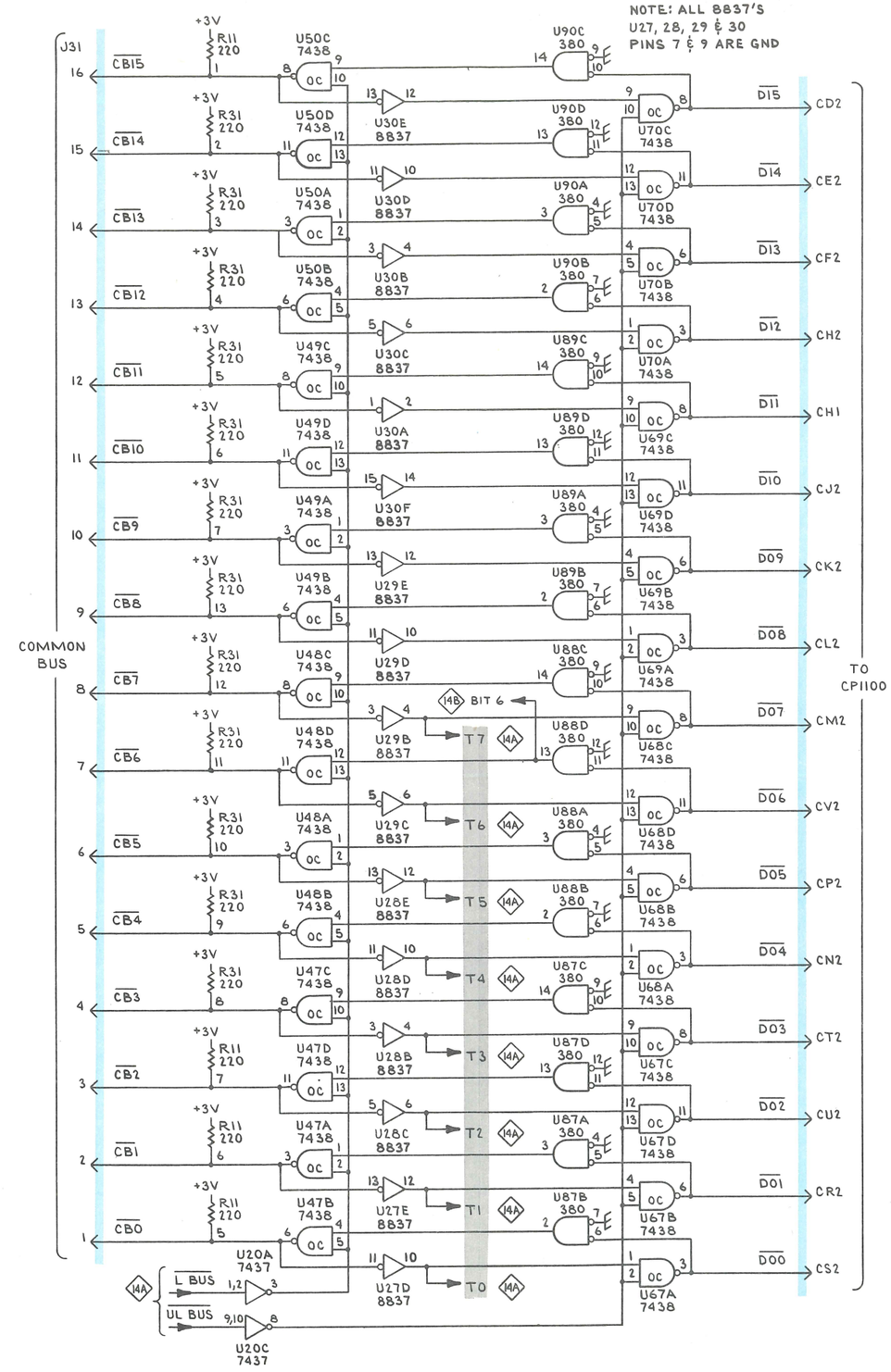
ARM
U10A 7438
U51B 7438
U51A 7438
U10D 7438
U10C 7438
U10B 7438
U71A 7438
U71C 7438
U71D 7438
U71B 7438
U05B 7438
U51D 7438
U51C 7438
U91D 7438
U91C 7438
U91A 7438
U91B 7438
$\overline{S1}$ $\overline{S2}$ $\overline{S3}$

COMMON BUS
J31
$\overline{BQ1}$ 22
$\overline{BQ2}$ 23
$\overline{CBBZY}$ 24
$\overline{S1}$ 25
$\overline{S2}$ 26
$\overline{S3}$ 27
GND 18 29 30 31 32 33 34 35 36 37
$\overline{D00}$ CS2
$\overline{D02}$ CU2
$\overline{D03}$ CT2
$\overline{D04}$ CN2
$\overline{D05}$ CP2
$\overline{D06}$ CV2
$\overline{D07}$ CM2
TO CP1100
J31
$\overline{CL1}$ 20
COMMON BUS
$\overline{BCLR}$ 19

NOTE: ALL 8837'S U27, 28, 29 & 30 PINS 7 & 9 ARE GND



STATE	U23A	U23B
IDLE	1	1
BUS REQ	1	0
SEL ACK	0	0
MASTER	0	1


NOTE: ALL 8837'S
U27, 28, 29 & 30
PINS 7 & 9 ARE GND
J31
COMMON BUS
+3V
R11 220
R31 220
CB15
CB14
CB13
CB12
CB11
CB10
CB9
CB8
CB7
CB6
CB5
CB4
CB3
CB2
CB1
CB0
U50C 7438
U50D 7438
U50A 7438
U50B 7438
U49C 7438
U49D 7438
U49A 7438
U49B 7438
U48C 7438
U48D 7438
U48A 7438
U48B 7438
U47C 7438
U47D 7438
U47A 7438
U47B 7438
U20A 7437
U20C 7437
L BUS
UL BUS
U30E 8837
U30D 8837
U30B 8837
U30C 8837
U30A 8837
U30F 8837
U29E 8837
U29D 8837
U29B 8837
U29C 8837
U28E 8837
U28D 8837
U28B 8837
U28C 8837
U27E 8837
U27D 8837
BIT 6
T7
T6
T5
T4
T3
T2
T1
T0
U90C 380
U90D 380
U90A 380
U90B 380
U89C 380
U89D 380
U89A 380
U89B 380
U88C 380
U88D 380
U88A 380
U88B 380
U87C 380
U87D 380
U87A 380
U87B 380
U70C 7438
U70D 7438
U70B 7438
U70A 7438
U69C 7438
U69D 7438
U69B 7438
U69A 7438
U68C 7438
U68D 7438
U68B 7438
U68A 7438
U67C 7438
U67D 7438
U67B 7438
U67A 7438
D15
D14
D13
D12
D11
D10
D09
D08
D07
D06
D05
D04
D03
D02
D01
D00
CD2
CE2
CF2
CH2
CH1
CJ2
CK2
CL2
CM2
CV2
CP2
CN2
CT2
CU2
CR2
CS2
TO CPI100