TEKTRONIX®

LA 501 LOGIC ANALYZER

WITH OPTIONS

OPERATORS

INSTRUCTION MANUAL

Tektronix, Inc.
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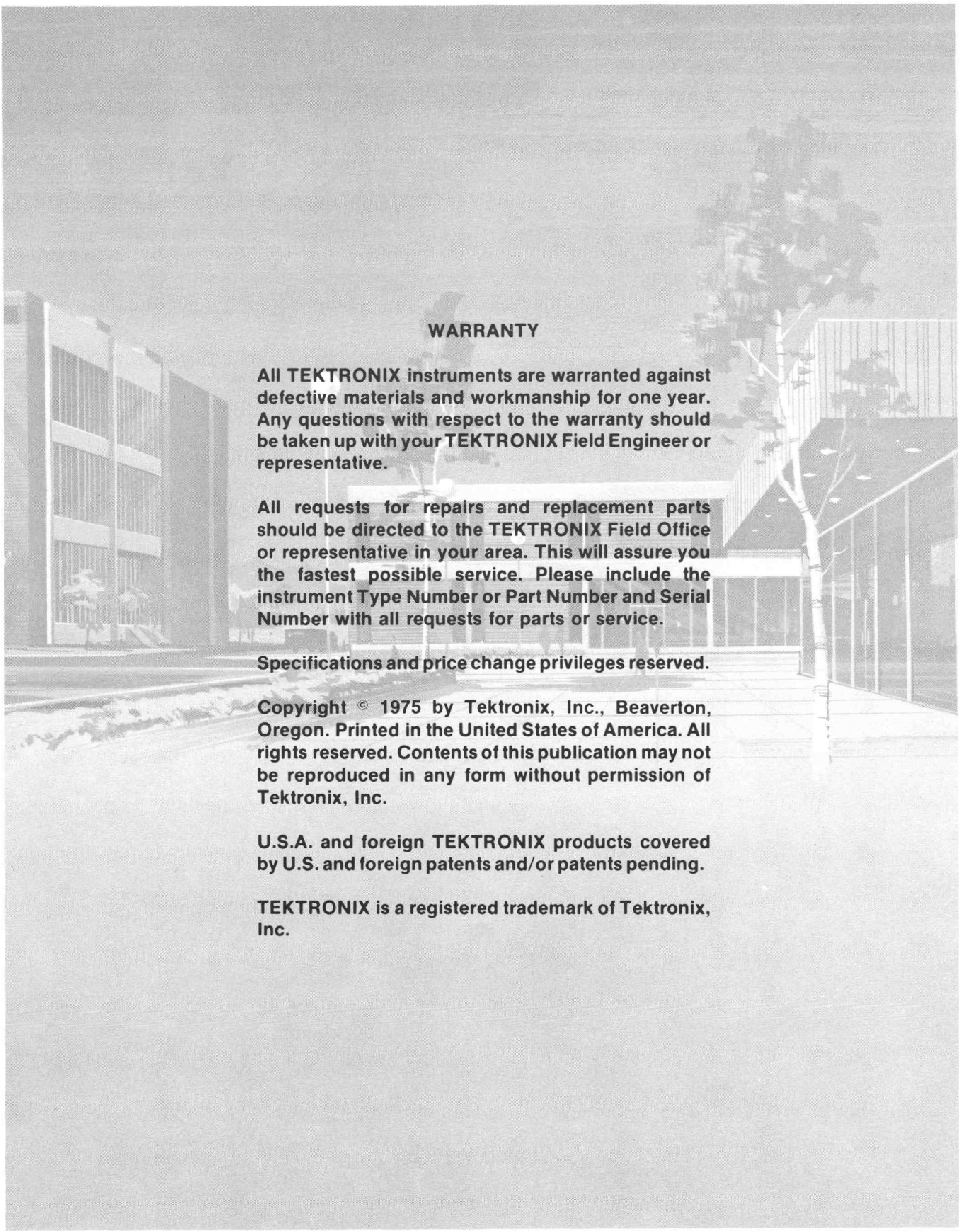

WARRANTY

All TEKTRONIX instruments are warranted against defective materials and workmanship for one year. Any questions with respect to the warranty should be taken up with your TEKTRONIX Field Engineer or representative.

All requests for repairs and replacement parts should be directed to the TEKTRONIX Field Office or representative in your area. This will assure you the fastest possible service. Please include the instrument Type Number or Part Number and Serial Number with all requests for parts or service.

Specifications and price change privileges reserved.

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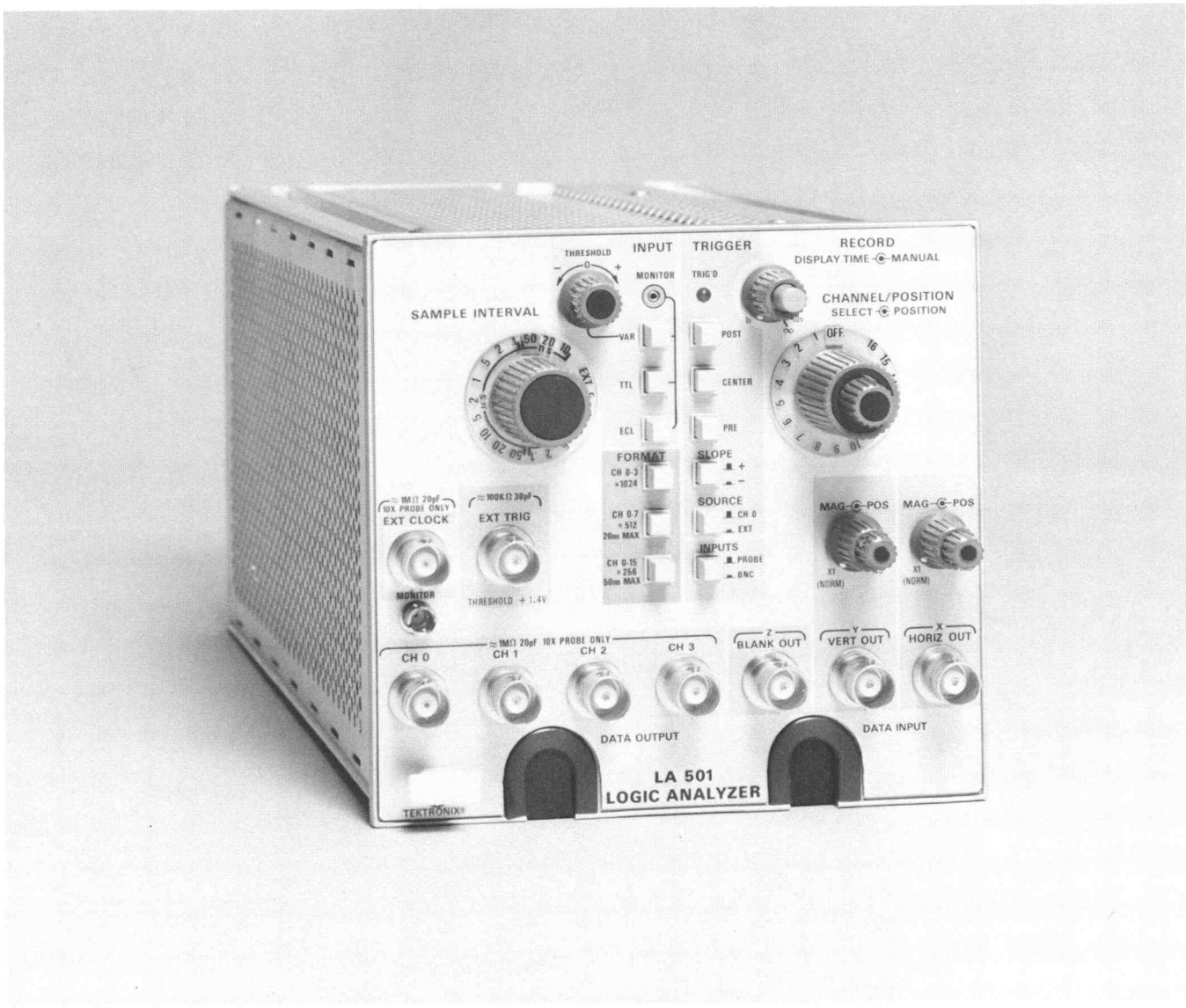

LA 501 Features

The LA 501 Logic Analyzer is designed for rapid troubleshooting of digital equipment. The simultaneous multi-channel raster can be displayed on almost any low-frequency X-Y monitor or oscilloscope.

The 4096-bit memory can be formatted into 4 channels of 1024 data bits, 8 channels of 512 data bits, or 16 channels of 256 data bits, for a wide range of bit serial, byte serial, or word serial data.

The flexible external (synchronous) or internal (asynchronous) sample rate clock capability will accomodate nearly all of the logic family speeds in use.

Three trigger delay modes (PRE, CENTER, and POST) allows selection of the best mode for the application. Negative trigger delay (PRE) allows analysis of the sequence of events that precede a fault trigger.

Digital data outputs provide a serial or parallel format to "loop back" stored data to a computer for quick error checks. This feature allows analysis or logging of data while viewing it, or it can be used without a display device.

Horizontal and vertical magnification, with positioning, provide high resolution. A unique vertical positioning system allows the selection and positioning of any one trace for timing comparisons with other traces in the raster.

The LA 501 can be powered by any TM-500-series power module which has three-unit, or greater, capability.

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OPERATING INSTRUCTIONS

TM 500-SERIES INSTRUMENTS

The LA 501 Logic Analyzer is a member of Tektronix' growing TM 500 line of Test and Measurement Instruments. This product line consists of both general- and special-purpose instruments such as digital multimeters, counter-timers, variable dc power supplies, pulse generators, function generators, calibration sources, oscilloscopes, signal processors, and others. Each instrument is a plug-in module. Power-module mainframes with 1, 3, 4, 5, and 6 compartments are available. The power module provides power and an overall housing for the plug-in modules, and permits internal signal interconnections between plug-in instruments to reduce clutter or to allow two or more instruments to perform a function which neither could perform alone. Each user can thus select from a broad choice of instrumentation to assemble a multi-function test set to fit his needs. This test set is compact and portable; yet it can be quickly reconfigured by exchanging plug-in instruments when test needs change. TM 500 systems can be configured for benchtop, rackmount, roll-about, and portable applications. For more information on the TM 500 line, please contact your Tektronix Field Office or representative.

SAFETY INFORMATION

The following warnings must be observed during maintenance and adjustment of the LA 501.

Component Replacement

To avoid electrical shock, disconnect the LA 501 from the power source before replacing components.

Soldering

To avoid electrical shock, disconnect the LA 501 from the power source before soldering.

Semiconductor Replacement

Semiconductors that have heat radiators use silicone grease to increase heat transfer. When one of these semiconductors is replaced, the silicone grease must also be replaced. Handle silicone grease with care. Avoid getting silicone grease in eyes. Wash hands thoroughly after use.

FRONT-PANEL CONTROLS, CONNECTORS, AND INDICATORS

The major controls and connectors for operation of the LA 501 are located on the front panel. Figure 1-1 shows and briefly describes the front-panel controls, connectors, and indicators. More information is given under Detailed Operating Information in this section.

Several connectors and switches are located inside the LA 501. These are described under Internal Connectors and Switches in this section.

INTERNAL CONNECTORS AND SWITCHES

Figure 1-2 shows the location of the internal connectors and switches. A brief description of these internal functions is given here. More information is given under Detailed Operating Information in this section.

(A) Data Input Connector

Multi-pin connector for use with the Data Acquisition Probe to provide the following functions:

DATA INPUTS. Provides input for each of the 16 channels (selected when the front-panel INPUTS switch is in the PROBE position).

CLOCK OUT. Provides signal output from the internal clock.

INVALID MODE. Provides an input to indicate an external-source sample interval that is too fast for the selected memory format (selected by jumper-connector P300).

(B) Data Output Connector

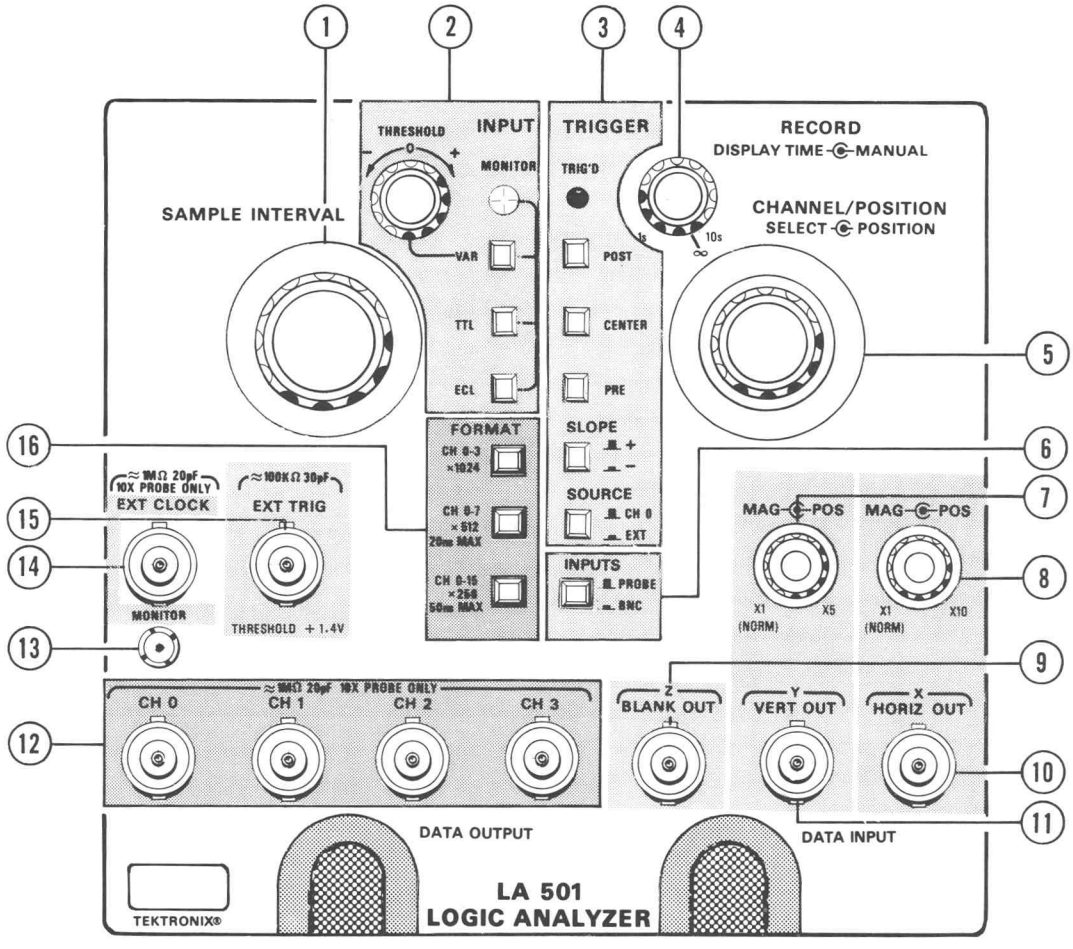
Multi-pin connector with the following functions:

PARALLEL DATA OUTPUT. Provides outputs for each of the 16 memory channels.

SERIAL DATA OUTPUT. Provides an output for serial data from the memory.

FLAG OUTPUT. Provides an output that indicates the start of each channel of data.

FORMAT OUTPUT. Provides an output that indicates memory format (selected by jumper-connector P300).



(1) SAMPLE INTERVAL Switch—Selects data input sample interval. The EXT position selects input from the EXT CLOCK connector. The knob skirt lamp blinks when the sample interval is too fast when in 8 or 16 channel record format.

(2) INPUT—

THRESHOLD Control: Provides a variable threshold voltage level for data input channels (selected by VAR switch).

MONITOR Pin Jack: Provides an output to monitor the dc threshold voltage level of the data input channels.

VAR Switch: Selects the variable THRESHOLD control.

TTL Switch: Selects a preset data input threshold voltage level for TTL logic.

ECL Switch: Selects a preset data input threshold voltage level for negative voltage ECL logic.

Fig. 1-1. Front-panel controls, connectors, and indicators.

(3) TRIGGER—

TRIG'D Indicator: Lights when record circuit has received a trigger signal.

POST Switch: Selects data to be stored after the trigger.

CENTER Switch: Selects data to be stored before and after the trigger.

PRE Switch: Selects data to be stored before the trigger.

SLOPE Switch: Selects the positive or negative-going edge of the record trigger signal.

SOURCE Switch: Selects Channel 0 or EXT TRIG connector for record trigger source.

(4) RECORD—

DISPLAY TIME Control: A variable control sets the time which memory stored data will be held for display before a new record cycle begins.

MANUAL Switch: A push button switch which resets the trigger circuit to start a new record cycle.

(5) CHANNEL/POSITION—

SELECT Switch: Selects any channel for positioning within the raster.

POSITION Control: Vertically positions channel selected by SELECT switch.

(6) INPUTS Switch—Selects data input signals from CH 0 through CH 3 front-panel BNC high impedance connectors or the internal low impedance DATA INPUT connector.

(7) MAG/POS Controls—Provides variable vertical magnification (X1 to X5) and vertical positioning of the displayed raster.

(8) MAG/POS Controls—Provides variable horizontal magnification (X1 to X10) and horizontal positioning of the displayed raster.

(9) Z BLANK OUT Connector—BNC connector for output of crt retrace blanking pulses.

(10) X HORIZ OUT Connector—BNC connector for output of horizontal (X-axis) display signal.

(11) Y VERT OUT Connector—BNC connector for output of Y-axis display signal.

(12) CH 0 Through CH 3 Connectors—BNC connectors for data inputs with 10X probes (selected by INPUTS switch in the BNC position).

(13) MONITOR Probe-Tip Connector—Provides output to monitor the EXT CLOCK connector when compensating high impedance 10X probes.

(14) EXT CLOCK Connector—BNC connector for input of external sampling clock signal (selected by SAMPLE INTERVAL switch in the EXT position).

(15) EXT TRIG Connector—BNC connector for external input to record trigger circuit (selected by SOURCE switch in the EXT position).

(16) FORMAT—

CH 0-3 X 1024 Switch: Selects channel 0 through channel 3 for data recording with 1024 bits of memory per channel.

CH 0-7 X 512 Switch: Selects channel 0 through channel 7 for data recording with 512 bits of memory per channel. Maximum sample interval is 50 nanoseconds.

CH 0-15 X 256 Switch: Selects channel 0 through channel 15 for data recording with 256 bits of memory per channel. Maximum sample interval is 20 nanoseconds.

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Fig. 1-1. Front-panel controls, connectors, and indicators. (Continued)

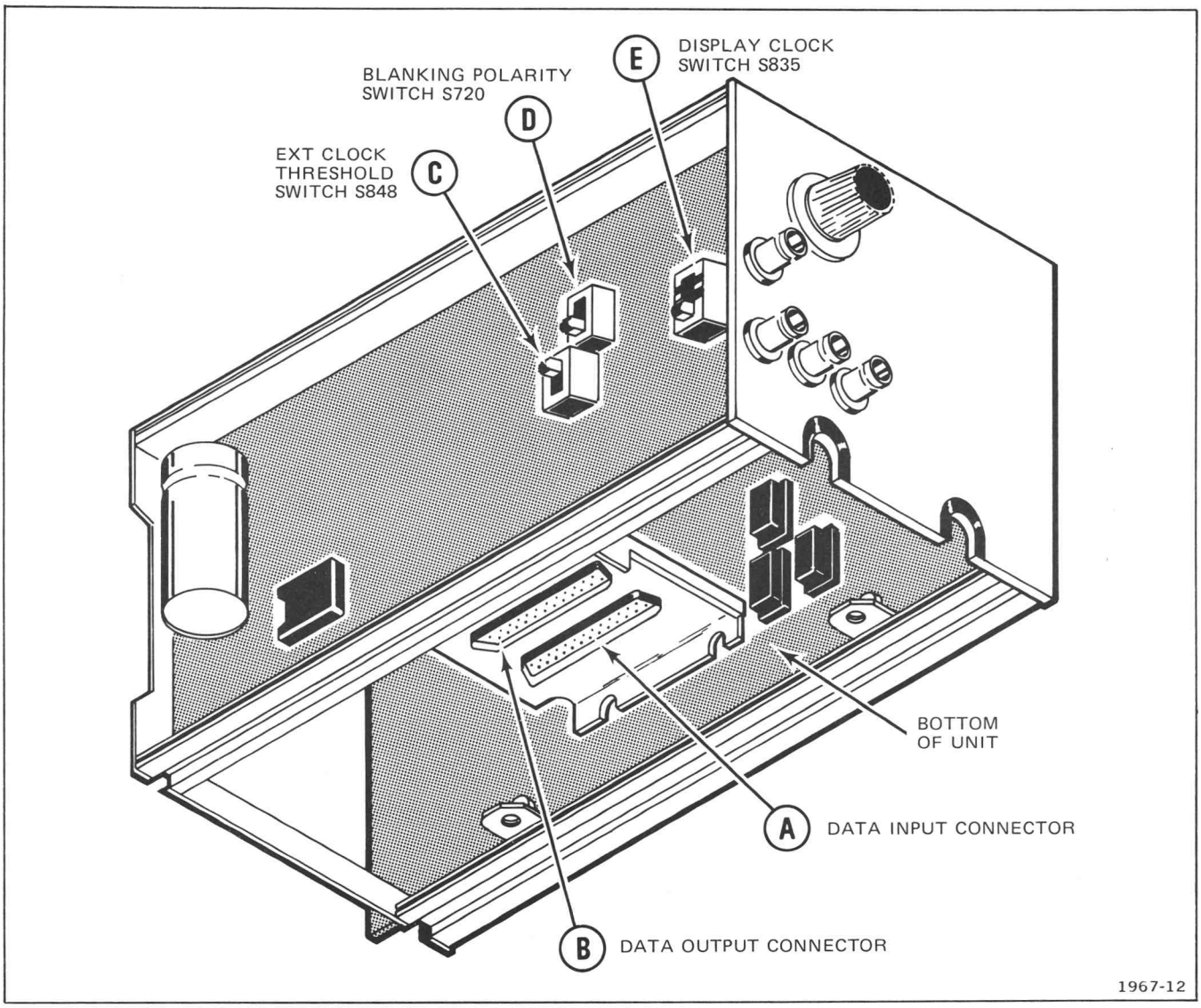

Fig. 1-2. Location of internal connectors and switches.

DISPLAY-STORE MODE OUTPUT. Provides an output to indicate whether the memory is in a Display or Store Mode (selected by jumper-connector P300).

FRAME OUTPUT. Provides an output to show a complete memory scan when reading the memory serially (selected by jumper-connector P300).

DISPLAY-CLOCK OUTPUT. Provides an ECL-level clock output during the Display Mode (selected by jumper-connector P300).

Z-AXIS INPUT. Provides an input to intensify a crt display via the front-panel Z BLANK OUT connector.

RECORD ENABLE. Provides an input to set the memory into a Store Mode.

EXT DISPLAY CLOCK INPUT. Provides an input to read the memory with an external clock signal (ECL level).

(C) External Clock Threshold Switch (S848)

Selects the external clock threshold level source. In the up position, threshold levels are selected by front-panel INPUT switches VAR, TTL, or ECL. In the down position, a fixed ECL threshold level is selected.

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(D) Blanking Polarity Switch (S720)

Selects the polarity of the blanking pulses at the Z BLANK OUT connector. In the up position, the blanking pulses are +5 volts (positive blanking signal). In the down position, the blanking pulses are −5 volts (negative blanking signal).

(E) Display Clock Switch (S835)

A three position switch that selects the source of the display clock signal applied to the clock gate. In the up position, an ECL input clock signal from the DATA OUTPUT connector is selected. In the center position, the front-panel EXT CLOCK connector is selected. In the down position, the 500 kHz internal display clock signal is selected.

CAUTION

Turn the power module off before inserting or removing the LA 501; otherwise, damage may occur to the LA 501 circuitry.

INSTALLATION

The LA 501 is calibrated and ready for use when received. It is designed to operate in a TM 500-series power module only. Before proceeding with installation, check that the internal switches and jumpers are set as necessary to operate the LA 501 with the associated equipment. For more information, refer to Internal Connectors and Switches in this section.

To install (refer to Figure 1-3), align the upper and lower rails of the LA 501 with the power module tracks and fully insert it. The front will be flush with the front of the power module when the LA 501 is fully inserted.

To remove the LA 501, pull on the release latch at the bottom of the front panel and the LA 501 will unlatch. Continue pulling on the release latch to slide the LA 501 out of the power module.

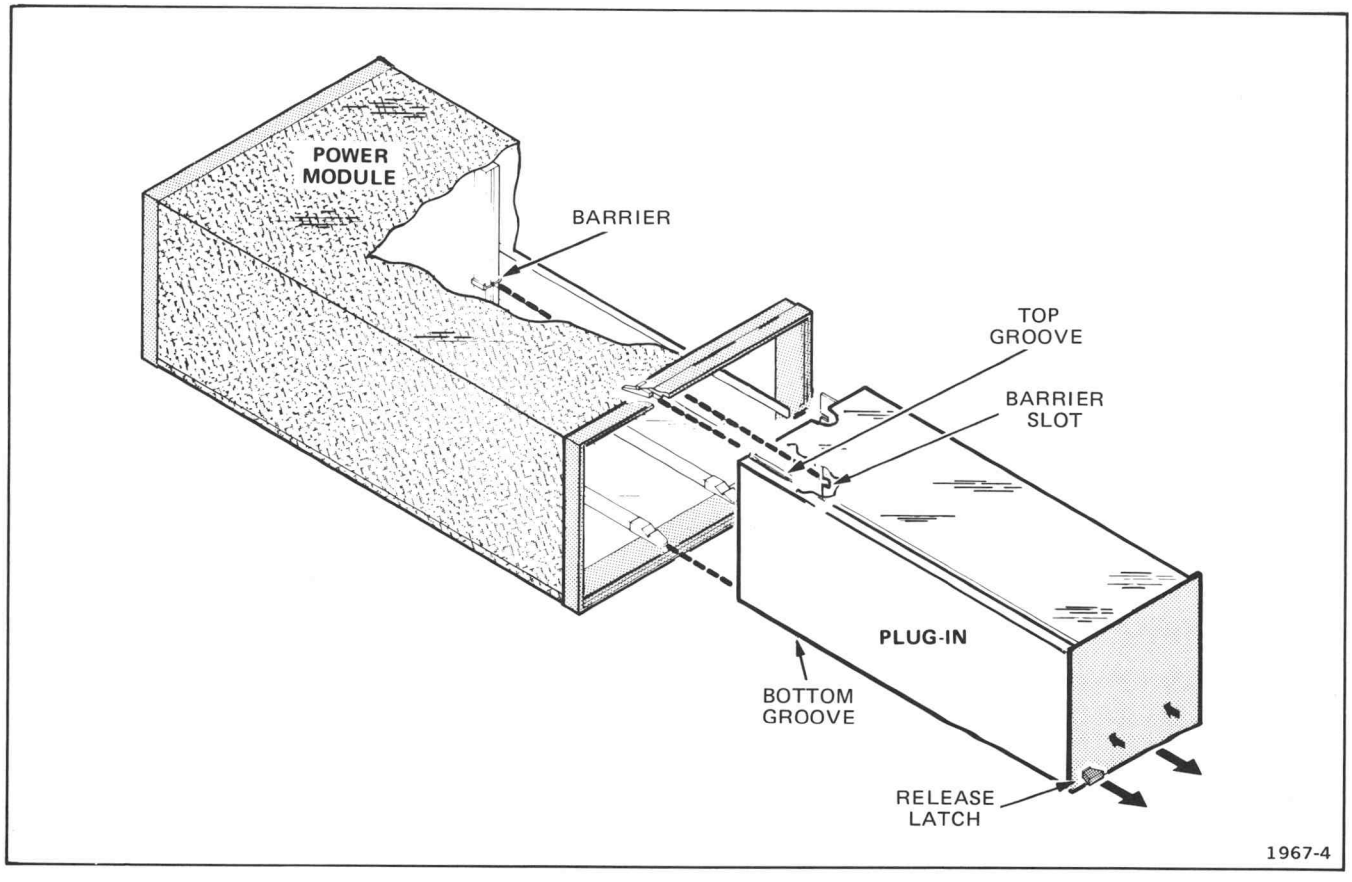


Fig. 1-3. LA 501 installation and removal.

FUNCTIONAL CHECK

The following procedure provides a method to check the basic operation of this instrument. The procedure can be used for incoming inspection to verify proper operation. The procedure can also be used by the operator for instrument familiarization or system troubleshooting.

Functions only are checked in this procedure. Measurement quantities and tolerances are not checked. Therefore, a minimum amount of test equipment is required.

Test Equipment Required

The following test equipment was used as a basis to write the Functional Check procedure. Other test equipment, which meets the requirements, may be substituted. When other equipment is substituted, the control settings or set up might need to be altered.

1. Test Oscilloscope

Description: Frequency response, dc to 500 kilohertz minimum; deflection factor, 50 millivolts to 2 volts/division. Test oscilloscope must have an external Z-axis input. Time base should have an external horizontal amplifier input with deflection factor of 50 millivolts/division.

Type Used: Tektronix 5403/D40 Oscilloscope system with 5A45 Amplifier, and 5B40 Time Base.

2. Power Module

Description: Tektronix TM 500-series power module with 3 or more plug-in compartments.

Type Used: Tektronix TM 503 Power Module (used with the LA 501 and pulse generator).

3. Pulse Generator

Description: Frequency range, 10 kilohertz to 10 megahertz minimum; output amplitude, minus 2 volts to plus 2 volts with 50-ohm output impedance.

Type Used: Tektronix PG 502 Pulse Generator (used with TM 503 Power Module).

4. Cables (5 Required)

Description: Impedance, 50 ohms; length, 18 inches (2 needed), 42 inches (3 needed); connectors, BNC.

Type Used: Type RG-58/U, 50 ohm coaxial, Tektronix Part 012-0076-00 (18 inch), Tektronix Part 012-0057-01 (42 inch).

5. Termination

Description: Impedance, 50 ohms; connectors, BNC.

Type Used: 50-ohm termination with BNC connectors, Tektronix Part 011-0049-01.

6. T Connector

Description: Connectors, BNC-to-BNC.

Type Used: BNC-to-BNC T connector, Tektronix Part 103-0030-00.

Preliminary Set Up

1. Within the LA 501, set the slide switches as follows (see Figure 1-2 for switch locations):

a. Display Clock switch (S835), set to down position for internal Display Clock.

b. External Clock Threshold switch (S848), set to up position for front-panel selection of threshold level.

c. Blanking Polarity switch (S720), set to down position for negative Z-axis blanking.

NOTE

If the Tektronix 5403/D40 test oscilloscope is not used, check the oscilloscope or monitor instruction manual for the required Z-axis blanking polarity.

2. Install the LA 501 in the 2 right side compartments and the pulse generator in the left compartment of power module (see Figure 1-4).

3. Turn on power module and test oscilloscope system.

4. Set pulse generator for 10 kilohertz square wave. Using a 0-volt base-line reference, set output amplitude to +0.25 volts.

5. Connect cables from LA 501 to test oscilloscope as shown in Figure 1-5.

6. Set LA 501 controls as follows:

SAMPLE INTERVAL	1 μs
INPUT	TTL
FORMAT	CH 0-3 X1024
TRIGGER	POST
SLOPE	(+)
SOURCE	CH 0
INPUTS	BNC
DISPLAY TIME	1 s
CHANNEL SELECT	OFF
Vertical MAG	X1 (NORM)
Vertical POS	Midrange
Horizontal MAG	X1 (NORM)
Horizontal POS	Midrange

7. With test oscilloscope inputs grounded, set the display to graticule center, and adjust oscilloscope for well-defined display. If necessary, refer to oscilloscope instruction manual for operating instructions.

8. Set test oscilloscope for vertical deflection factor of 100 millivolts/division with dc input coupling.

9. Set test oscilloscope for external horizontal amplifier operation (horizontal deflection factor of 50 millivolts/division with dc input coupling).

Raster Display

If necessary, perform the Preliminary Set Up procedure. To obtain a raster display, proceed as follows:

1. Connect the +0.25 volt, 10 kilohertz square-wave signal from pulse generator (as set in Preliminary Set Up procedure) to LA 501 CH 0 input connector.

2. Check that TRIG'D indicator is lit.

3. Set the LA 501 vertical and horizontal POS controls for centered display.

4. Set test oscilloscope intensity control at desired viewing level.

5. Check display for one square wave (top trace, channel 0) and 3 trace lines.

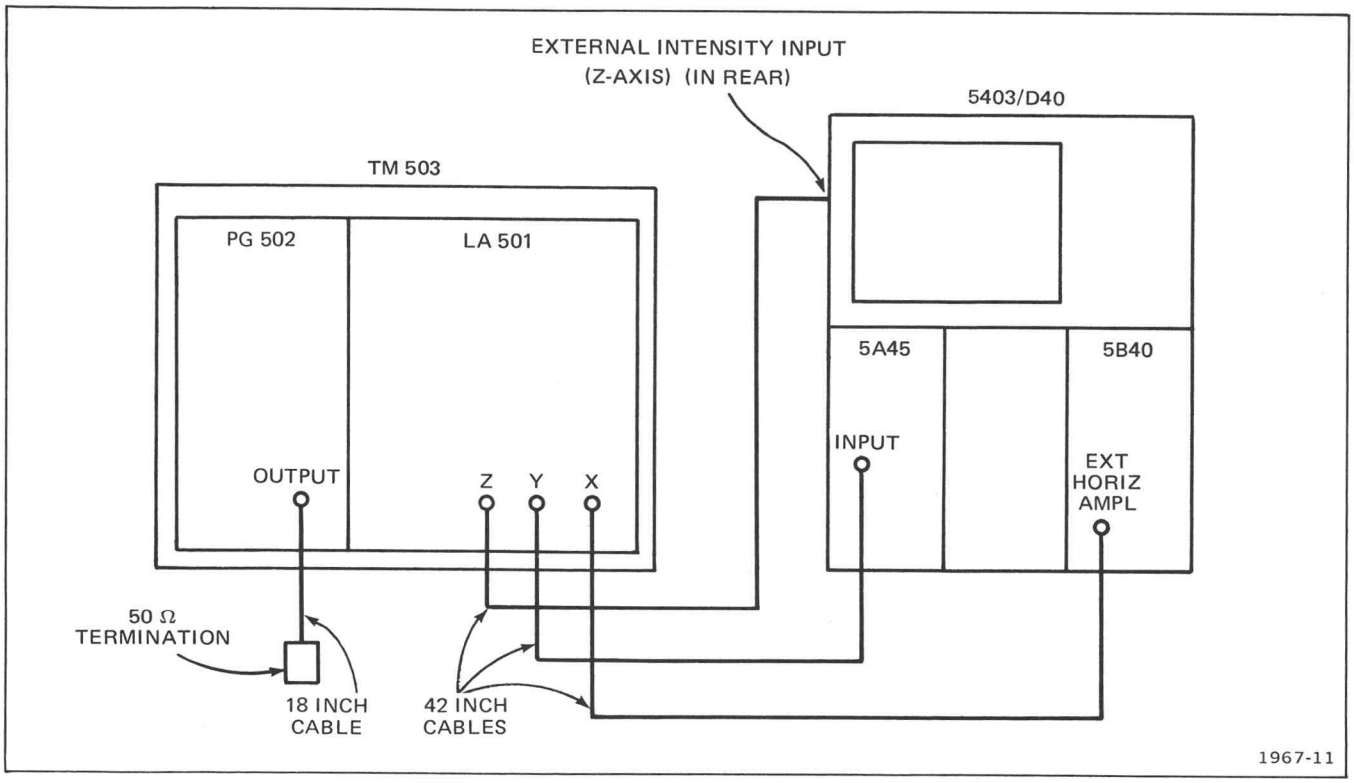


Fig. 1-4. Equipment set up for Functional Check.

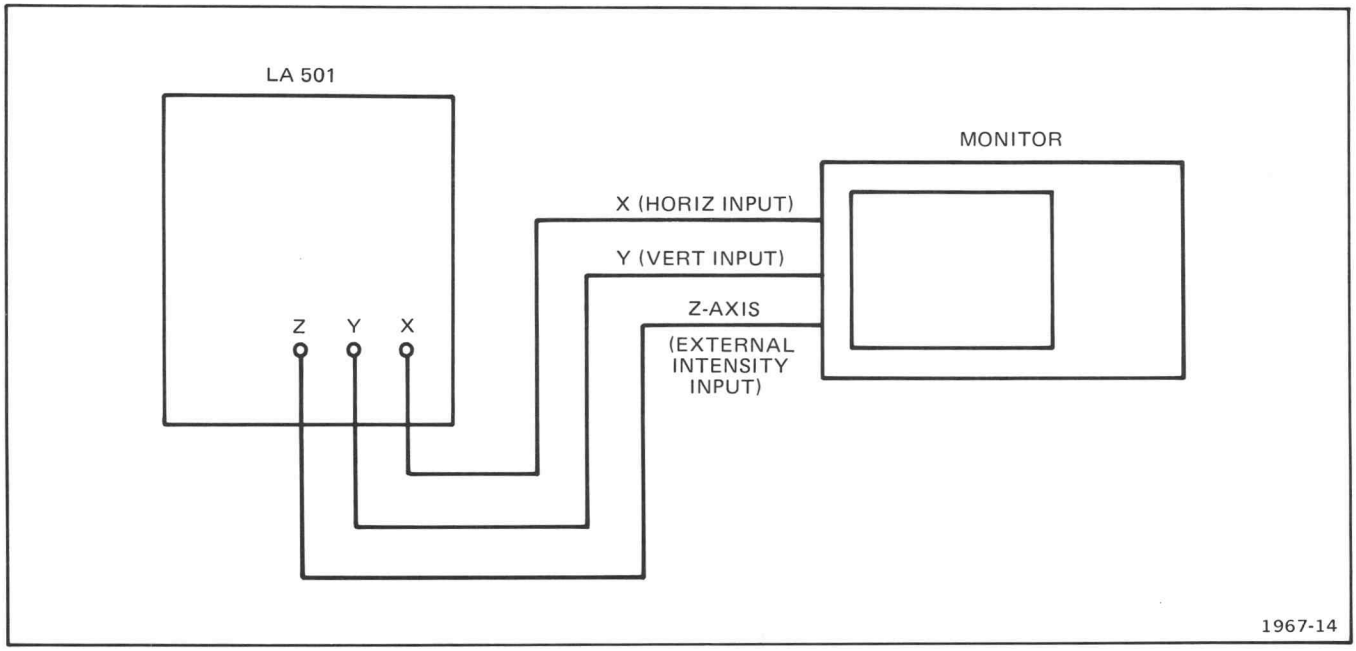


Fig. 1-5. LA 501 and monitor X, Y, and Z signal connections for Functional Check.

Display Functions

If necessary, perform the Preliminary Set Up procedure. Use the following procedure to check the Display Functions:

1. Connect the +0.25 volt, 10 kilohertz square-wave signal from pulse generator (as set in Preliminary Set Up procedure) to CH 0 and CH 1 input connectors with BNC T connector.

2. Check test oscilloscope for a square-wave display on channels 0 and 1.

3. Disconnect pulse generator signal from CH 1, and connect to CH 2 (retain connection to CH 0).

4. Check for square-wave display on channels 0 and 2.

5. Disconnect pulse generator signal from CH 2, and connect to CH 3.

6. Check for square-wave display on channels 0 and 3.

7. Check that display expands vertically as vertical MAG control is rotated to X5.

8. Return vertical MAG control to X1 position.

9. Check that display expands horizontally as horizontal MAG control is rotated to X10.

10. Return MAG control to X1 position.

11. Press in CH 0-7 X512 FORMAT switch.

12. Set the LA 501 Vertical and Horizontal POS controls for centered display.

13. Check display for 8 traces.

14. Press in CH 0-15 X256 FORMAT switch.

15. Set the LA 501 Vertical and Horizontal POS controls for centered display.

16. Check display for 16 traces.

17. Set CHANNEL:SELECT switch to 0.

18. Check that channel 0 trace can be positioned anywhere within raster as POSITION control (CHANNEL/POSITION) is rotated.

19. If desired, repeat step 18 for remainder of channel selections.

20. Return CHANNEL:SELECT switch to OFF.

21. Set RECORD DISPLAY TIME control to ∞ detent position.

22. Disconnect pulse generator from CH 3 connector.

23. Press in RECORD MANUAL switch and release it.

24. Check display for square wave on channel 0 only.

25. Return RECORD DISPLAY TIME control to 1 s.

26. Check that SAMPLE INTERVAL knob skirt lamp blinks as SAMPLE INTERVAL switch is set to 20 ns and 10 ns.

27. Set SAMPLE INTERVAL switch to EXT.

28. Disconnect the pulse generator from CH 0 connector.

29. Press in INPUT:ECL switch.

30. Press in CH 0-3 X1024 FORMAT switch.

31. Set pulse generator for 0-volt base-line reference, and set output amplitude to −0.2 volts.

32. Connect −0.2 volt, 10 kilohertz square-wave signal from pulse generator (as set in step 31) to EXT CLOCK and CH 0 connectors.

33. Check display for 4 traces.

34. Disconnect pulse generator from EXT CLOCK and CH 0 connectors.

Trigger Functions

If necessary, perform the Preliminary Set Up procedure. Use the following procedure to check the Trigger Functions:

1. Set SAMPLE INTERVAL switch to 50 ns.

2. Connect a +0.25 volt, 10 kilohertz square-wave signal from pulse generator (as set in Preliminary Set Up procedure) to CH 0 connector.

3. Check that channel 0 (top trace) has positive-going transition at left side of trace.

4. Press in TRIGGER:CENTER switch.

5. Check that positive-going transition is now near center of trace.

6. Press in TRIGGER:PRE switch.

7. Check that positive-going transition is at right side of trace.

8. Set SLOPE switch to −.

9. Check for negative-going transition at right side of trace.

10. Disconnect pulse generator signal from CH 0 connector.

11. Press in TRIGGER:POST switch.

12. Set SLOPE switch to +.

13. Set SOURCE switch to EXT.

14. Using a 0-volt base-line reference, set pulse generator output amplitude to +2 volts.

15. Connect the +2 volt, 10 kilohertz signal (as set in previous step) to LA 501 EXT TRIG connector.

16. Check that TRIG'D indicator is lit.

17. Check display for 4 traces.

18. Disconnect signal from EXT TRIG connector.

This completes the Functional Check procedure.

DETAILED OPERATING INFORMATION

Signal Connection

Probes offer the most convenient means of connecting signals to the LA 501 inputs. Tektronix probes are shielded to prevent pickup of electrostatic interference, and are designed to monitor the signal source with minimum circuit loading.

10X PROBES. The P6108 (optional accessory), a 10X attenuation probe, offers a high input impedance and allows the circuit under test to perform very close to the normal operating conditions.

When using 10X probes, select a probe with a rise time of less than 2.25 nanoseconds, and which is capable of compensating 20 picofarads of input capacitance.

10X PROBE COMPENSATION. When using 10X probes on the EXT CLOCK and CH 0 to CH 3 front-panel BNC input connectors, the probe capacitance must be compensated to match instrument input capacitance to obtain the best rise-time response. See Figure 1-6 for probe compensation set up and procedure.

DATA ACQUISITION PROBE. The P6450 (standard accessory) is a passive, 5X attenuation probe, which is designed for use with the LA 501. When plugged into the DATA INPUT connector, it offers input connections to all 16 channels.

DATA OUTPUT CABLE. In order to use DATA OUTPUT connector, J120, it is necessary to assemble a special cable. One end of the cable must be terminated with a connector to meet the test requirements. The other end of the cable is terminated with a connector to mate with the DATA OUTPUT connector. Use a type DB-25P, 25-pin, male connector; order Tektronix part 131-0570-00. For further information, contact your Tektronix Field Office or representative.

COAXIAL CABLE. The front-panel output signals, Z BLANK OUT, Y VERT OUT, and X HORIZ OUT, should be connected to other equipment with 50-ohm coaxial cables. Use high-quality, low-loss cables.

Display Monitor

The display monitor may be any oscilloscope or display monitor with X, Y, and Z-axis capabilities with the following characteristics:

Frequency response	dc to 500 kilohertz
Deflection factor	
Horizontal	50 millivolts/division
Vertical	100 millivolts/division
External Z-Axis sensitivity (external intensity input)	plus or minus 5 volts

Connections from the LA 501 X, Y, and Z outputs to the oscilloscope or monitor inputs should be made with coaxial cables. Figure 1-5 shows the proper set up for operation. Check the oscilloscope or monitor instruction manual for the required Z-axis blanking polarity. Set the Blanking Polarity switch (S720) down for negative blanking, or up for positive blanking. See Figure 1-2 for the location of S720. For more information on blanking polarity selection, see Internal Switches in this section.

Sample Interval

The SAMPLE INTERVAL switch selects calibrated sample-interval times from the internal clock. The number of times that the input channels are sampled is determined by the format selected. A 4-channel format is sampled 1024 times; 8-channel format, 512 times; and a 16-channel format, 256 times.

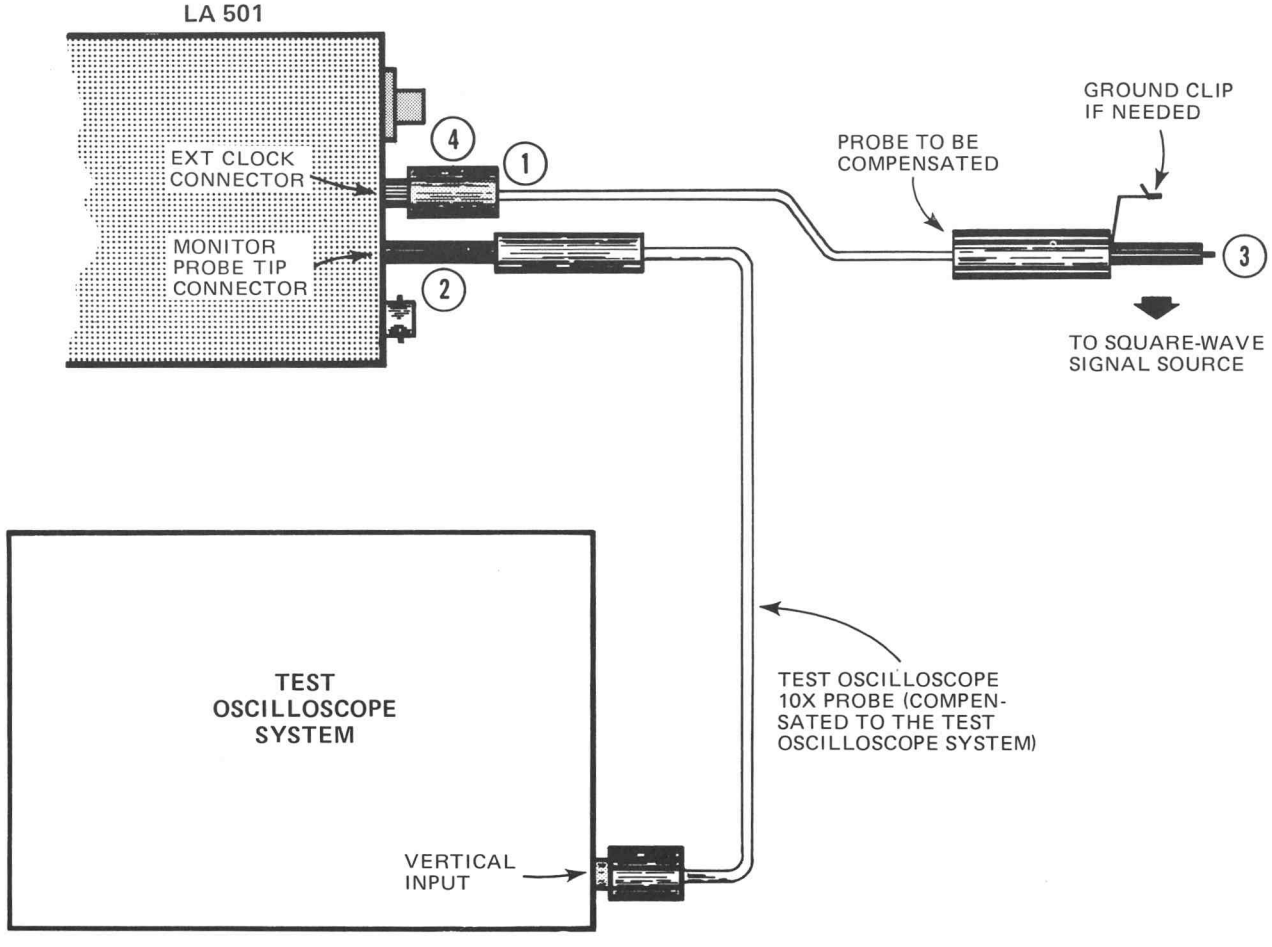
To capture and store the state of a pulse, one or more sample intervals must occur during the pulse. Resolution is determined by the number of samples taken during the pulse.

The lamp that illuminates the SAMPLE INTERVAL knob skirt blinks when the sample interval is too fast for 8 channel (10 nanosecond) or 16 channel (10 or 20 nanosecond) storage. When using an external clock signal, the EXT position of the SAMPLE INTERVAL switch selects the front-panel EXT CLOCK connector.

External Clock Input

The EXT CLOCK input provides a means of using a clock signal from the equipment under test, or any other clock signal that the operator may desire.

EXT CLOCK. This connector allows the connection of external clock signals. The external clock threshold level is selected by an internal switch (S848) that selects a preset



(1) Connect the 10X probe to be compensated to the LA 501 EXT CLOCK connector.

(2) Insert the test oscilloscope 10X probe tip into the EXT CLOCK MONITOR probe-tip jack.

(3) Connect the 10X probe to be compensated to a 600 mV, fast-rise, 1 KHz square-wave signal source (e.g., oscilloscope calibrator) for low-frequency compensation. For high-frequency compensation (if applicable), use a 600 mV square wave with a rise time of 3 ns or less. The test oscilloscope bandwidth should be at least 100 MHz.

(4) Adjust the probe compensation adjustment(s) (see probe instruction manual for adjustment locations) for an optimum square front corner and flat top on the test oscilloscope display.

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Fig. 1-6. 10X probe compensation set up and procedure.

ECL threshold voltage level or the front-panel INPUT THRESHOLD controls. When in the EXT CLOCK mode, either the positive or negative slope may be used for the clock edge. When the negative edge is selected, data sample intervals are stored into memory on the negative edge of the external clock signal. When the positive edge is selected, data sample intervals are stored into memory on the positive edge of the external clock signal. An internal jumper-connector, P831, provides polarity selection. Figure 1-7 shows the location of P831 and the selection positions.

MONITOR. This probe-tip jack allows the operator to view the external clock signal, and is also used for compensating 10X probes. Refer to 10X Probe Compensation in this section for more information.

Input Threshold Controls

The INPUT THRESHOLD controls allow the selection of two fixed threshold levels, or the variable THRESHOLD level control. Fixed threshold levels are for TTL and ECL logic.

TTL. This switch selects a preset TTL input threshold level for each of the data input channels, and for the EXT CLOCK input. When the recommended probes are used, the input threshold level is +1.4 volts.

ECL. This switch selects a preset ECL input threshold level for each of the data input channels and for the EXT CLOCK input. When the recommended probes are used, the input threshold level is −1.25 volts.

VAR. This switch selects the variable THRESHOLD level control.

THRESHOLD. The variable THRESHOLD control allows the selection of a wide range of threshold levels for the data input channels and for the EXT CLOCK input. When the recommended probes are used, the threshold level is adjustable from −10 volts to +10 volts.

MONITOR. The MONITOR pin jack provides an output to monitor the dc threshold voltage level.

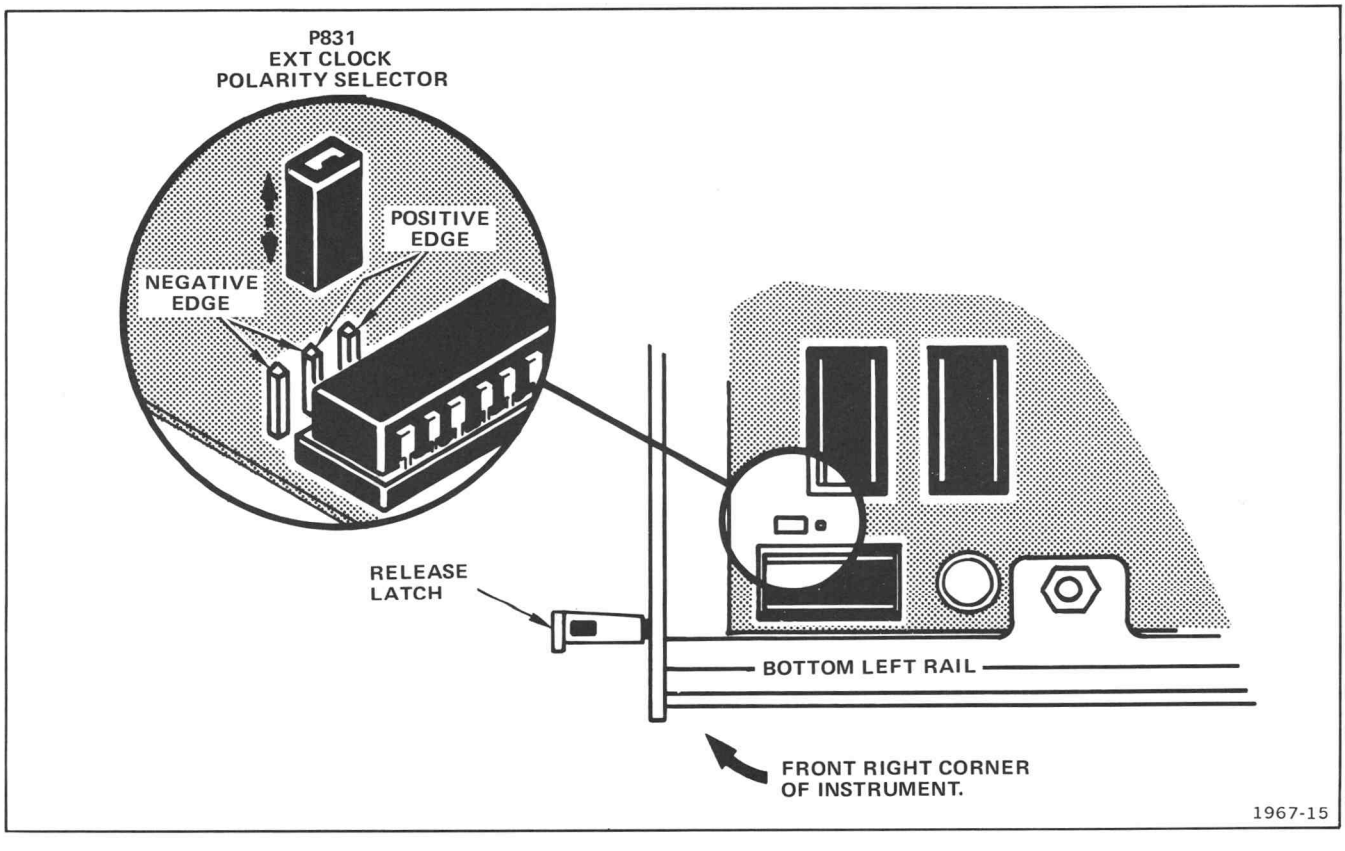


Fig. 1-7. Location of EXT CLOCK polarity selector.

Trigger Controls

The TRIGGER controls provide a means to select the signal source, select the slope on the waveform to stop the storage cycle, and select the point in the storage cycle at which the trigger will occur.

TRIG'D INDICATOR. This light provides a convenient indication of the Trigger circuit condition. If the INPUT THRESHOLD controls are correctly set for the input logic level used and the Trigger circuit has received a trigger, the TRIG'D light is on. If the TRIG'D light is off, the LA 501 is in the storage cycle, but has not yet received a trigger.

POST. This switch selects data for memory storage after the trigger has occurred. The stored data consists of 6 per cent before-trigger data and 94 per cent after-trigger data.

CENTER. This switch selects data for memory storage before and after the trigger has occurred. Half of the stored data is before the trigger, and the other half is data after the trigger.

PRE. This switch selects data for memory storage before the trigger has occurred. The stored data consists of 94 per cent before-trigger data and 6 per cent after-trigger data.

SLOPE. This switch determines whether the Trigger circuit responds to a positive- or a negative-going transition of the trigger signal. When the SLOPE switch is set to −, the Trigger circuit responds to negative-going transitions. When the SLOPE switch is set to +, the Trigger circuit responds to positive-going transitions.

SOURCE. This switch selects the source of the signal for the Trigger circuit. When the switch is set to CH 0, the input signal connected to the channel 0 input is used for the trigger source. When the switch is set to EXT, an external signal connected to the EXT TRIG connector is selected for the trigger source.

EXTERNAL TRIGGER. Trigger signals from the equipment under test, or other equipment the operator may prefer to use, can be connected to the EXT TRIG connector.

Ext Trig. This connector allows the connection of an external TTL logic level trigger signal. The input threshold level is fixed at +1.4 volts. This connector is selected when the SOURCE switch is in the EXT position.

Format Switches

The FORMAT switches select the number of data channels to be used. Three switches allow the operator to select 4, 8, or 16 data channels.

CH 0-3 (X1024). This switch selects the first 4 data channels. In this mode, each channel has a memory storage capacity of 1024 bits. The 4-channel mode has a maximum sample rate of 10 nanoseconds.

CH 0-7 (X512). This switch selects the first 8 data channels. In this mode, each channel has a memory storage capacity of 512 bits. The 8-channel mode has a maximum sample rate of 20 nanoseconds.

CH 0-15 (X256). This switch selects all 16 data channels. In this mode, each channel has a memory storage capacity of 256 bits. The 16-channel mode has a maximum sample rate of 50 nanoseconds.

Record Controls

The RECORD controls allow the operator to select the display time to view stored information, and also allows manual or automatic resetting of the Trigger circuit.

DISPLAY TIME. This variable control sets the time during which stored data will be held for display before a new storage cycle begins. The display time is variable from 1 to 10 seconds, or is held indefinitely when turned to the fully clockwise detent position (∞).

MANUAL. This switch resets the Trigger circuit to start a new storage cycle.

Monitor Output Signals and Controls

Vertical, horizontal, and Z-axis output signals are provided to produce a raster display on the display monitor. The vertical and horizontal outputs each have magnification and positioning controls.

Z BLANK OUT. When connected to a display monitor external Z-axis input, the Z-axis blanking signal performs two functions.

The first function is to blank the crt retrace lines. The second function is, if the new storage cycle fails to go through

a full memory storage cycle before a trigger is received, old data (bad data) is blanked out on the crt display. Positive or negative blanking pulses are selected by Blanking Polarity switch, S720.

Y VERT OUT. When connected to a display monitor Y-axis (vertical) input, this output signal provides an on-screen display of serial data from the memory. Channel separation is accomplished by stepping each channel down with a dc offset voltage. Channel 0 is at the top of the display.

Mag (Y-Axis). This control provides a variable X1 to X5 amplification of the Y VERT OUT signal to permit greater display resolution.

Pos (Y-Axis). This control vertically positions the raster within the display area of the monitor. To obtain maximum use of the Vertical POS control, the display monitor must first be adjusted for a centered spot with the X- and Y-axis inputs grounded. All vertical position adjustments are then made with the LA 501 Vertical POS control.

X HORIZ OUT. When connected to a display monitor X-axis (horizontal) input, this output signal provides the display with an X-axis sweep. The sweep rate is determined by the FORMAT switch setting. If desired, an external clock source may be used to scan the memory; however, any clock rate other than that of the internal clock will affect the sweep length. The external clock signal may be from the front-panel EXT CLOCK connector, or from the Ext Display Clock input at the DATA OUTPUT connector. The display clock source is selected by the internal Display Clock switch (S835).

Mag (X-Axis). This control provides a variable X1 to X10 amplification of the X HORIZ OUT signal to permit greater display resolution.

Pos (X-Axis). This control horizontally positions the data channels within the display area of the monitor. To obtain maximum use of the horizontal control, the display monitor must first be adjusted for a centered spot with the X- and Y-axis inputs grounded. All horizontal position adjustments are then made with the LA 501 Horizontal POS control.

CHANNEL/POSITION. The SELECT and POSITION controls under this title are used for comparison of any one channel with any other channel.

Select. This switch selects any channel (0 through 15) for positioning within the display raster.

Position. This control vertically positions the selected comparison channel within the display.

Data Input Signals

Both low impedance and high impedance inputs are provided for the data channels. Front-panel BNC connectors, CH 0 through CH 3, provide high impedance inputs, and multi-pin DATA INPUT connector, J100, provides low impedance inputs to all 16 channels. The INPUTS switch selects the desired input connector(s). 10X probes are used for connecting signals to the front-panel data input connectors.

INPUTS. This switch selects the desired data input probe connector(s). When in the BNC position, the four front-panel CH 0 through CH 3 connectors are selected. When in the PROBE position, the multi-pin DATA INPUT connector is selected.

CH 0 THROUGH CH 3. The four front-panel BNC connectors provide a means of connecting data signals through 10X probes to the channel 0, 1, 2, and 3 input preamplifiers. The 10X probes must be compensated for use with ECL logic, due to the low signal levels.

DATA INPUT. The internal, multi-pin connector, J100, provides a means of connecting data signals through the Data Acquisition Probe to the inputs of all 16 channels. Figure 1-8 identifies the pin assignments for the DATA INPUT connector. The Clock Out at pin 22 is an unterminated ECL-level output of the internal clock signal. Pin 23 of J100 (probe line A) is connected to Signal Selector jumper, P300. At the factory, P300 is wired to connect pin 23 of J100 to the Invalid Mode Input line. However, this connection can be changed to a different signal line if desired. For further information, see P300 Signal Selector in this section.

Data Output Connector

Internal multi-pin connector, J120, provides several functions. Figure 1-9 identifies the DATA OUTPUT connector pin assignments. As shown in Figure 1-9, three of the pins of J120 are connected to Signal Selector jumper, P300. At the factory, P300 is wired to make signal-line connections to these pins as shown in Figure 1-10. The connections can be changed to different signal lines if desired. For further information, see P300 Signal Selector in this section. The functions provided by the Data Output connector are described as follows:

PARALLEL DATA OUTPUT. Output connections are provided from each of the 16 memory channels to read the memory in parallel data form. The parallel data outputs are ECL-logic level signals.

SERIAL DATA OUTPUT. This connection is provided to read the memory in serial data form. The serial data output is an ECL-logic level signal.

FLAG OUTPUT. This connection provides for the output of an ECL-level pulse. The negative-going edge of the Flag Output pulse indicates the beginning of each channel.

Z-AXIS INPUT. This connection is provided to intensify the display by application of an external signal. A positive 5-volt input will fully intensify the display. As the input voltage is lowered towards zero volts, the display will be intensified less.

RECORD ENABLE. This connection is provided to set the memory into the Store Mode by application of an external

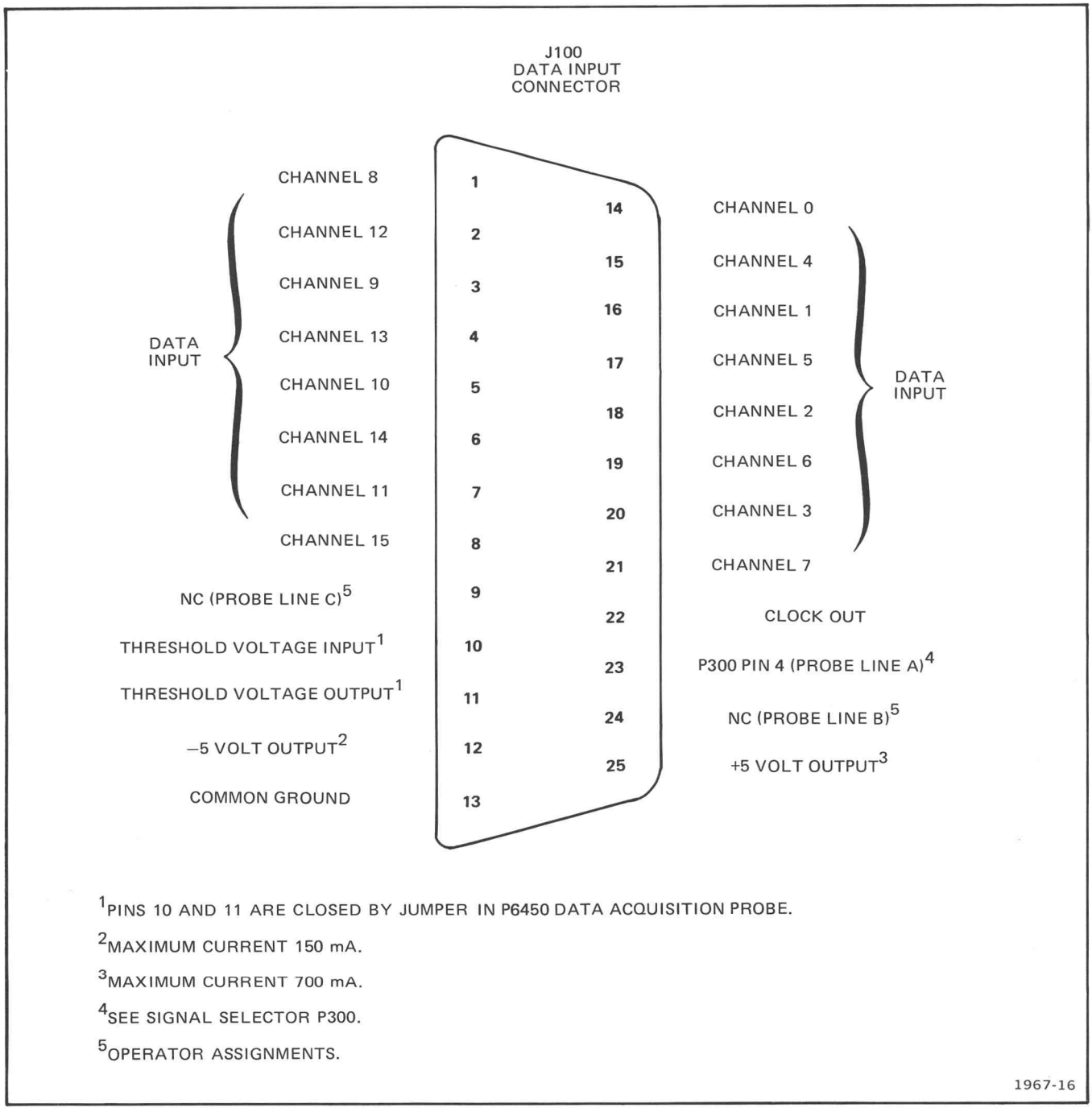


Fig. 1-8. Pin assignments for the DATA INPUT connector, J100.

signal. The Record Enable input is ac coupled, and requires only the negative-going edge of a 1.5-volt pulse to enable the Store Mode.

EXT DISPLAY CLOCK INPUT. This connection is provided for the application of an external, ECL-level, display clock signal. The input is terminated by 100 ohms to −2 volts. The External Display Clock Input signal requirements are: The HI level must be more positive than −1 volt, and the LO level must be more negative than −1.5 volts. The usable frequency range is from less than one hertz to two megahertz.

P300 Signal Selector

Internal multi-pin jumper-connector, P300, provides selection of several input and output signal lines to the DATA INPUT, J100, and DATA OUTPUT, J120, connectors. Figure 1-10 shows the location of P300 and identifies the pin assignments. Figure 1-10 shows the jumpers as they are installed at the factory. To change the connections for different requirements, see Signal Selection with P300 in this section.

DISPLAY CLOCK OUTPUT. This connection provides a display-clock output from the memory. An ECL-level clock output is provided during the Display Mode. During the Store Mode, the output assumes an ECL LO state.

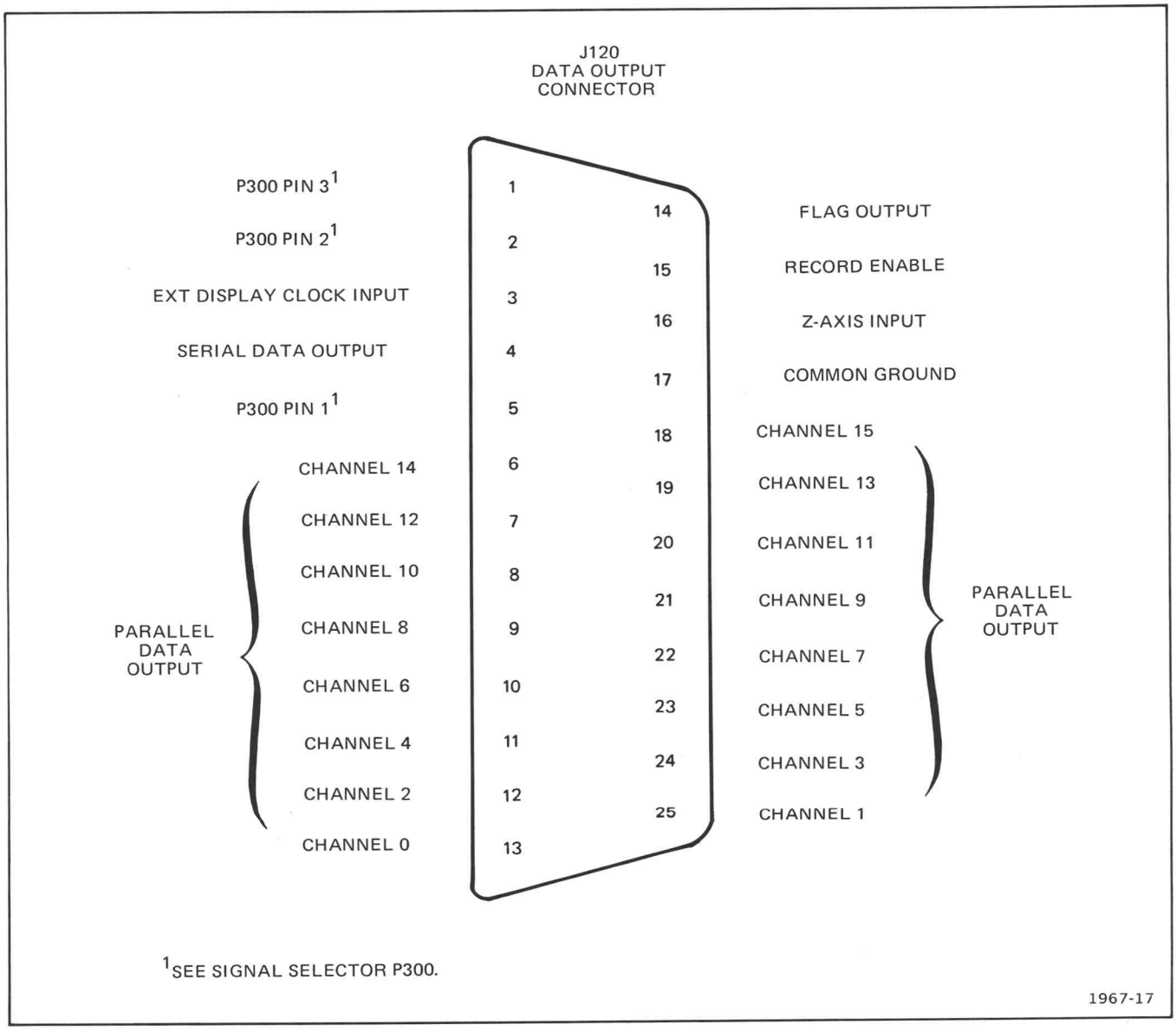


Fig. 1-9. Pin assignments for the DATA OUTPUT connector, J120.

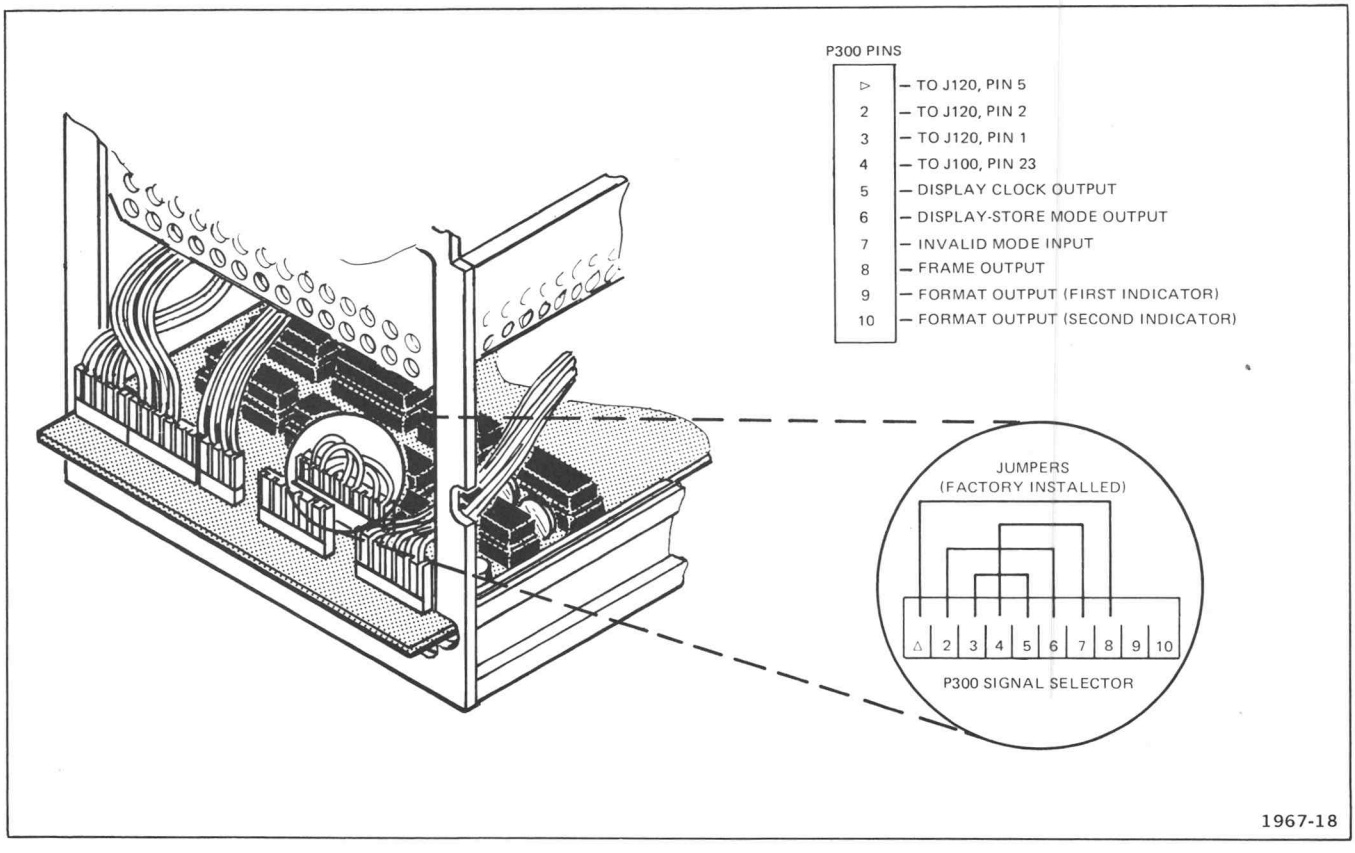


Fig. 1-10. Location of Signal Selector P300, and P300 pin assignments.

DISPLAY-STORE MODE OUTPUT. This output indicates whether the memory is in a Display or a Store Mode. An ECL LO level indicates that the memory is in the Display Mode. An ECL HI level indicates that the memory is in the Store Mode.

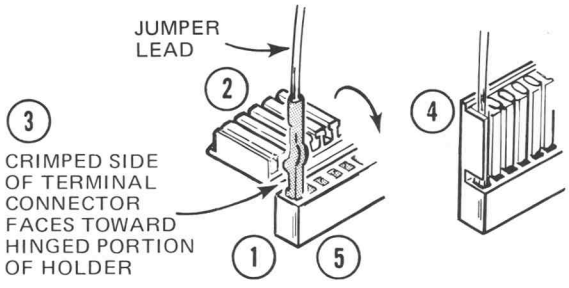
INVALID MODE INPUT. The Invalid Mode Input is used in conjunction with an external clock source. When an external ground is applied to this input, the SAMPLE INTERVAL light blinks to indicate that the sample interval is too fast for the selected memory format.

FRAME OUTPUT. This connection provides for the output of an ECL-level pulse. One complete pulse cycle represents at least one complete serial scan of the data in the memory.

FORMAT OUTPUT. Two connections provide ECL-level outputs which indicate the memory format selected by the front-panel FORMAT switches. Table 1-1 shows the ECL-level output states at pins 9 and 10 of P300 for each of the FORMAT switch positions.

TABLE 1-1
Format Output Levels at P300

FORMAT Switch	P300	
	Pin 9	Pin 10
CH 0-3 X1024	HI	HI
CH 0-7 X512	LO	HI
CH 0-15 X256	LO	LO



1. Remove P300 from instrument (refer to Figure 1-10).
2. Bend grooved portion of holder (part nearest jumper) away from the jumper in direction of its hinged side.
3. Insert the jumper lead connector into the selected hole in the holder. (Refer to Figure 1-10).
4. Bend the grooved part of holder back to its vertical position so connector is inserted into groove.
5. Observe the connector polarity (refer to Figure 1-10), and install P300 back into the instrument.

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Fig. 1-11. P300 jumper placement procedure.

SIGNAL SELECTION WITH P300. To change the signal selections to the DATA INPUT (J100) and DATA OUTPUT (J120) connectors shown in Figure 1-10, perform the procedure shown in Figure 1-11.

Internal Switches

Three switches within the LA 501 provide selection of display Blanking Polarity, EXT CLOCK threshold source, and the Display Clock source. Figure 1-12 shows the location and describes the use of these switches.

LA 501 GLOSSARY

The terms listed in this glossary are used throughout this manual.

Asynchronous—Multiple digital information transferred at non-common clock rates.

Bit—The smallest increment of digital information.

CPU—Central Processing Unit.

ECL—Emitter-Coupled Logic.

Jitter—A form of distortion in asynchronous systems that is due to timing variations of the received data.

Multiplexing—The combining of multiple inputs into a single output.

Parallel Data—Data transferred on multiple lines. Parallel data logic is derived from the multiple lines.

Parallel-to-Serial Conversion—The technique of storing a digital pattern from a parallel bus, then transferring that pattern out to a serial bus.

Parity Bits—Bits added to the data stream which enable the receiver to verify whether the data is correctly or incorrectly received.

PROM—Programmable Read Only Memory.

RAM—Random Access Memory.

Serial Data—Data transferred on a single line. Serial data logic is derived in a sequential mode.

Store Clock—The clock used to store information into the LA 501 memory.

Synchronous—Digital information transferred with the same clock reference.

Threshold Voltage—The comparator input voltage on the inverting input, which is used as a reference. Thus, if the signal on the non-inverting input is more positive than the threshold voltage, the output is HI; if the signal is more negative, the output is LO.

TTL—Transistor-Transistor Logic.

"wired OR"—ECL gate outputs that are connected together to yield the equivalent output of an OR gate.

Blanking Polarity

Switch S720 selects the polarity of the voltage at the Z BLANK OUT connector.

(1) In the up position, the display blanking pulses are +5 volts (positive blanking).

(2) In the down position, the display blanking pulses are −5 volts (negative blanking).

Ext Clock Threshold S848

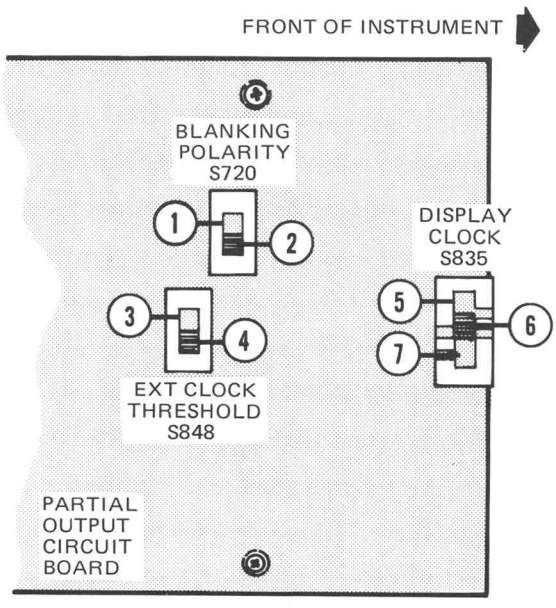
Switch S848 selects the external clock threshold level source.

(3) In the up position, threshold levels are selected by the front-panel INPUT switches VAR, TTL, or ECL.

(4) In the down position, a fixed ECL threshold level is selected.

Display Clock S835

Switch S835, a three-position switch, selects the source of the display clock signal applied to the display clock gate.



LEFT SIDE, WITH SIDE PANEL REMOVED.

(5) In the up position, an ECL input clock signal from the DATA OUTPUT connector is selected.

(6) In the center position, the front-panel EXT CLOCK connector is selected.

(7) In the down position, the internal 500 kilohertz display clock signal is selected.

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Fig. 1-12. Internal switch locations, and switch selection positions.

APPLICATIONS

Malfunctions in digital equipment systems are difficult to isolate with conventional test equipment, such as oscilloscopes or counters. The following applications describe some typical situations in which the LA 501 Logic Analyzer can be used to make digital equipment troubleshooting relatively easy.

MICROPROCESSORS

A malfunctioning microprocessor system is shown in Figure 1-13. Software had previously worked properly, but was still not free of suspicion. Data was stored in the RAM (random-access read/write memory). The system program was resident in the PROM (programmable read only memory). Restart vectors pointed to the address of the first instruction in the restart routine.

When the restart hardware was exercised, the CPU (central processing unit) should have performed certain initialization routines and then gone to the Wait for Interrupt mode. The terminal would then call up other operating software in the PROM, or provide access to a binary loader. The failure consisted of very erratic operation after restart.

The LA 501 was connected to the system as shown in Figure 1-13 to store and display a large data block from the eight data lines. The display was obtained by triggering the LA 501 on the beginning of the restart cycle and using the system clock as an external data sampling strobe.

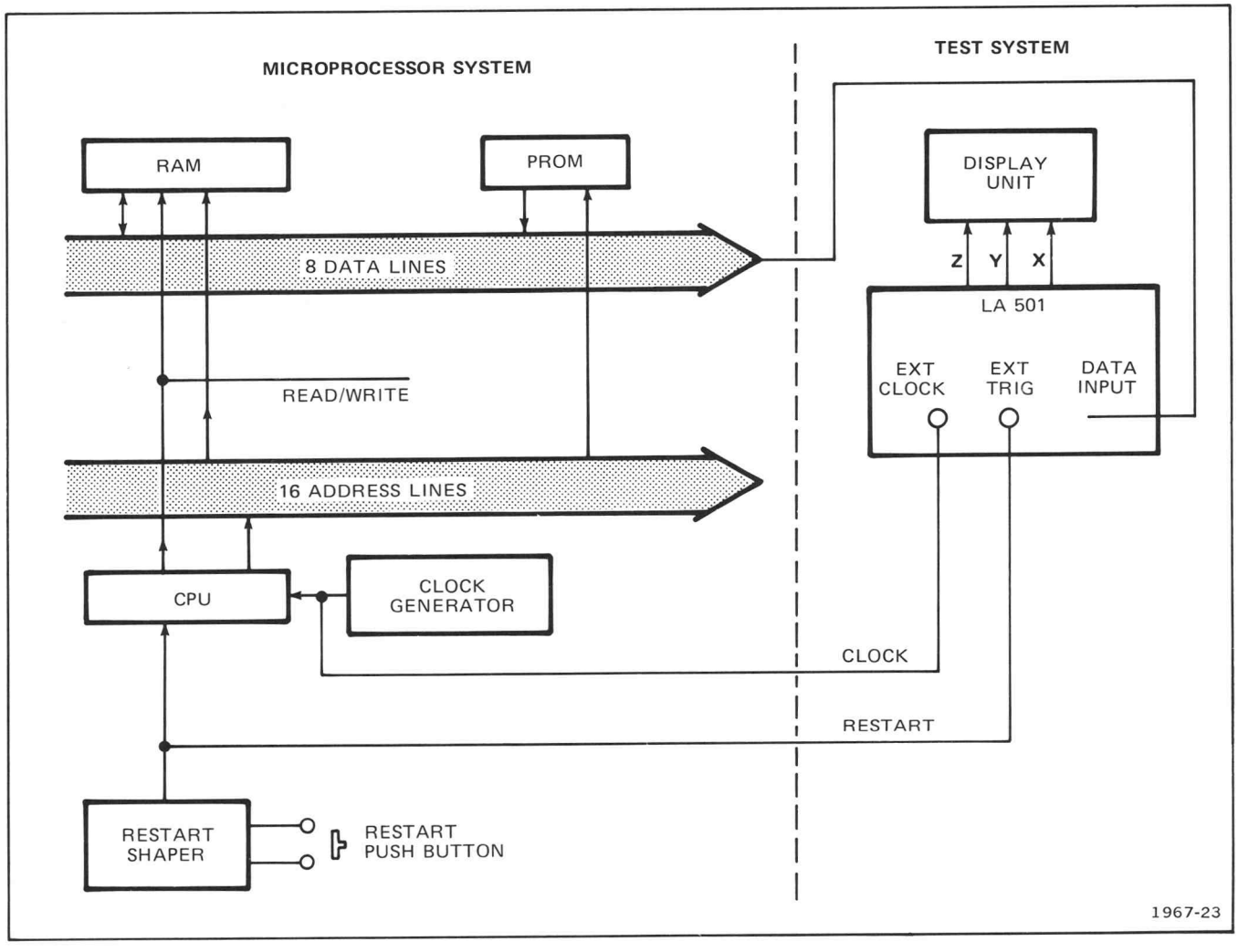


Fig. 1-13. Typical set up for troubleshooting a microprocessor system with the LA 501 Logic Analyzer.

Analysis of the data display showed the problem to be a dropped bit in the portion of the PROM providing the re-start routine. The CPU fetched an invalid restart vector, causing data from the RAM to be executed as instructions.

STORAGE BUFFERS

A multi-input logic analyzer will provide a quick and easy method for checking the performance of a storage buffer. The following application shows how the inputs and outputs of a buffer can be monitored simultaneously and observed for verification of performance or for a malfunction, if it is suspected.

The non-synchronous buffer is a commonly used type, in which data flows continuously from input to output. A quick snapshot of this data flow will show at a glance if all the memory cells are functioning properly.

The LA 501 can take this single shot snapshot of 8 input and 8 output lines simultaneously and display all sixteen data lines on a single display for a quick comparison. A typical set up and display are shown in Figure 1-14. When the LA 501 is clocked asynchronously from the internal clock, a high-resolution timing diagram display will provide timing information as well as reveal malfunctions that would otherwise be difficult to detect with any other type of test equipment such as an oscilloscope or DVM.

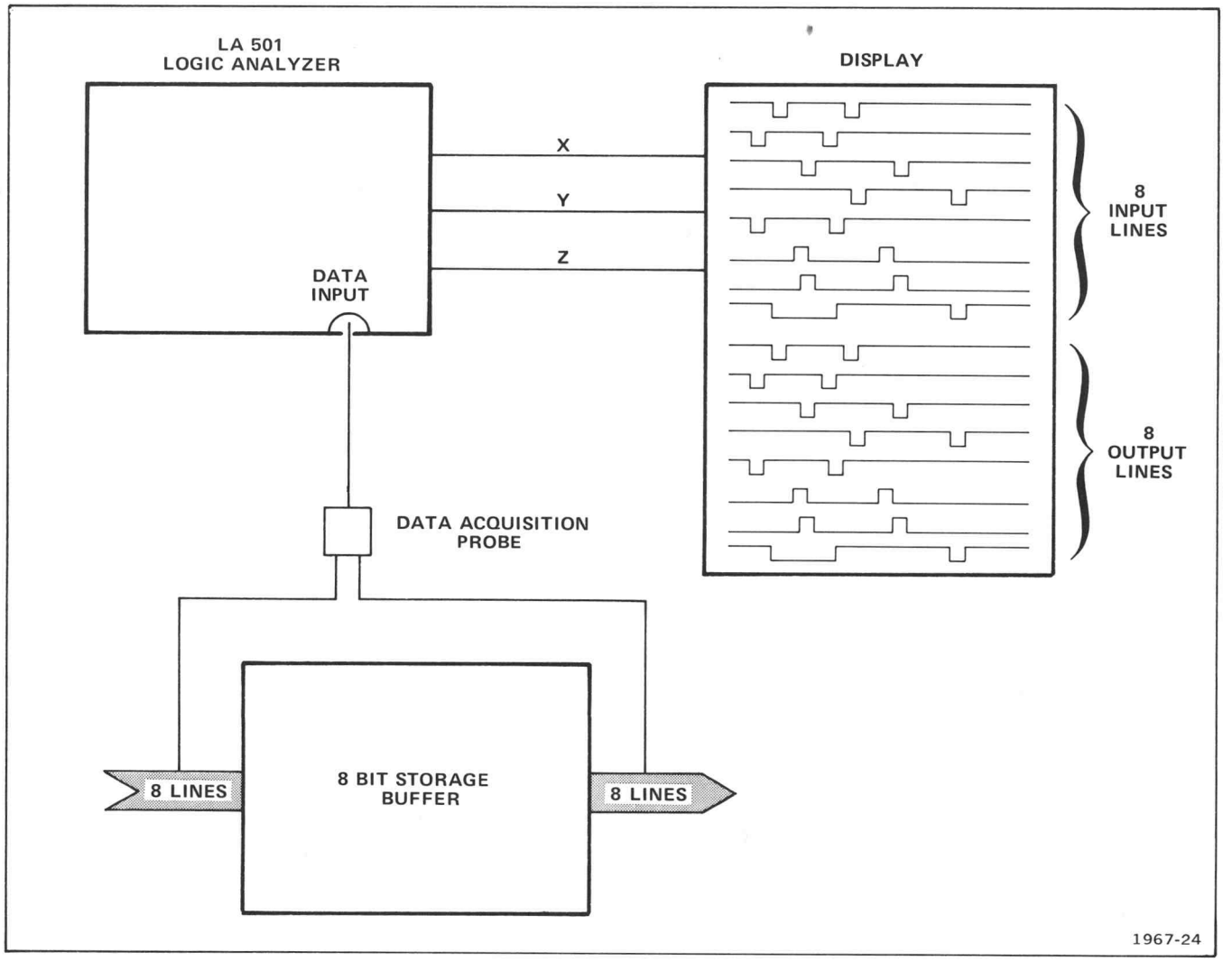


Fig. 1-14. Typical set up and display for troubleshooting a storage buffer with the LA 501 Logic Analyzer.

SPECIFICATION

The electrical specifications listed in Table 2-1 apply when the following conditions are met: (1) The instrument must have been adjusted at an ambient temperature between +20° and +30°C, (2) the instrument must be operating at an ambient temperature between 0° and +50°C, and (3) the instrument must be operating for at least 15 minutes.

TABLE 2-1
Electrical

Characteristic	Performance Requirement		
DATA INPUTS			
Impedance			
Channel 0-3 (High-Impedance Data Input connectors)	1 MΩ within 1% paralleled by approximately 20 pF.		
Channel 0-15 (Low-Impedance Data Input connector)	20 kΩ within 1% paralleled by approximately 20 pF.		
Threshold Level	At Data Input Connectors		At Probe Tip
	P6450 Probe[1]	10X Probe[1]	
VAR (Variable)	At least −2 V to +2 V	At least −1 V to +1 V	At least −10 V to +10 V
TTL	+0.280 V within .05 V	+0.140 V within .025 V	+1.4 V within 0.25 V
ECL	−0.250 V within .010 V	−0.125 V within .006 V	−1.25 V within .06 V
MONITOR Output	Within 3% of threshold level at Data Input connectors.		
Sensitivity (without probes)			
High-Impedance Data Input	At least 60 mV p-p.		
Low-Impedance Data Input	At least 120 mV p-p.		
Minimum Pulse Width	1 sample interval + 5 ns HI or LO to ensure pulse recording.		
Input Delay Between Channels			
High-Impedance Data Input	6 ns or less.		
Low-Impedance Data Input			
Channel 0-7	7 ns or less.		
Channel 0-15	12 ns or less.		
Input Delay Between High-Impedance Data Input Connectors and P6450 Probe Tip	22 ns or less.		

[1] **Probe rise time for high-impedance data and external clock inputs should be 2.25 ns or less with aberrations not to exceed 10% p-p.**

TABLE 2-1 (CONT.)
Electrical

Characteristic	Performance Requirement
DATA INPUTS (CONT.)	
Maximum Input Voltage	
At High-Impedance Data Input Connectors	Clamped at ±2.5 V, protected to ±150 V.
At Low-Impedance Data Input Connector	Clamped at ±2.5 V (no protection).
With P6450 Probe	Clamped at ±12.5 V, protected to ±50 V.
TRIGGER	
Source	
Input Level	
Internal (CH 0)	Set by INPUT controls.
External	Threshold Level: +1.4 V, within 0.2 V, clamped at +2.7 V and −0.6 V, protected to ±15 V.
Input R and C	Approximately 100 kΩ paralleled by approximately 20 pF.
Minimum Pulse Width	10 ns.
Record Display Time Range	Approximately 1 s to 10 s.
TIME BASE	
Internal	
Frequency	100 MHz within 50 parts per million.
Sample Rate	10 ns to 5 ms/sample in 1-2-5 sequence. Maximum sample rate: 4X = 10 ns, 8X = 20 ns, 16X = 50 ns.
External (EXT CLOCK Input)	
Input R and C	1 MΩ within 1% paralleled by approximately 20 pF. Clamped at ±2.5 V, protected to ±150 V.
Sensitivity	At least 60 mV p-p.
Pulse Width	
CH 0-3 X1024	HI for at least 10 ns and LO for at least 10 ns.
CH 0-7 X512	HI for at least 10 ns and LO for at least 10 ns.
CH 0-15 X256	HI for at least 25 ns and LO for at least 25 ns.

TABLE 2-1 (CONT.)
Electrical

Characteristic	Performance Requirement
TIME BASE (CONT.)	
Threshold Level	Same as data inputs, or −0.125 V within .006 V (internal switch).
Slope	Data strobed in on positive or negative edge of external clock.
Data Change With Respect to Clock Edge at EXT CLOCK Connector (internally selectable + or − edge)	
At High-Impedance Data Input Connectors	
Set-Up	2 ns.
Hold	15 ns.
At P6450 Probe Tip	
Channel 0-7	
Set-Up	14 ns.
Hold	3 ns.
Channel 8-15	
Set-Up	20 ns.
Hold	2 ns.
DISPLAY SIGNALS (FRONT PANEL)	
Blanking Output	0 V to +5 V or 0 V to −5 V within 1 V (internal switch)
CRT Retrace Blanking Time	
CH 0-3 X1024	4.2 μs within 20% (4 bits).
CH 0-7 X512	2.2 μs within 20% (2 bits).
CH 0-15 X256	1.2 μs within 20% (1 bit).
Vertical Output	0.1 V/div within 10%.
Magnify	X1 to X5 within 10%.
Horizontal Output	.05 V/div within 10%.
Linearity	Pulse width within 10% from 10% to 100% of sweep.
Magnify	X1 to X10 within 10%.

TABLE 2-1 (CONT.)
Electrical

Characteristic	Performance Requirement
DISPLAY SIGNALS (FRONT PANEL) (CONT.)	
Display Format	
CH 0-3 X1024	1 group of 4 lines.
CH 0-7 X512	2 groups of 4 lines each.
CH 0-15 X256	4 groups of 4 lines each.
Raster Shift With Format Change	1 div or less at X1 magnification.

LOW-IMPEDANCE DATA INPUT

Data Input

Pin	Channel	Pin	Channel
1	8	14	0
2	12	15	4
3	9	16	1
4	13	17	5
5	10	18	2
6	14	19	6
7	11	20	3
8	15	21	7

Clock Out	Pin 22. Unterminated ECL level. The output, when terminated, is a standard negative voltage ECL level.
Invalid Mode	Jumper, P300 pin 7. Ground closure causes blinking of SAMPLE INTERVAL switch light.
Threshold DC	Pin 10.
Comparator Input	Pin 11.
+5 Volts	Pin 25. 700 mA or less.
−5 Volts	Pin 12. 150 mA or less.
Ground	Pin 13.

DATA OUTPUT

Parallel Data Output — Parallel data from memory (ECL level).

Pin	Channel	Pin	Channel
6	14	18	15
7	12	19	13
8	10	20	11
9	8	21	9
10	6	22	7
11	4	23	5
12	2	24	3
13	0	25	1

TABLE 2-1 (CONT.)
Electrical

Characteristic	Performance Requirement
DATA OUTPUT (CONT.)	
Serial Data Output	Pin 4. Serial data from memory (ECL level).
Flag Output	Pin 14. Negative-going edge indicates beginning of each channel (ECL level).
Format Output	Jumper, P300. Indicates memory format.
	Pin 9 / Pin 10
CH 0-3 X1024	1 / 1
CH 0-7 X512	0 / 1
CH 0-15 X256	0 / 0
Z-Axis Input	Pin 16. A positive signal (+5 V or less) intensifies the display.
Record Enable	Pin 15. Negative-going pulse of at least 1.5 V sets memory into Record mode.
Ext Display Clock Input	Pin 3. Terminated by 100 Ω to −2 V.
	Signal Levels: HI = more positive than −1 V. LO= more negative than −1.5 V.
Frequency	From less than 1 Hz to 2 MHz.
Display—Store Mode Output	Jumper, P300 pin 6. A HI indicates memory is in Store mode. A LO indicates memory is in Display mode.
Frame Output	Jumper, P300 pin 8. A positive-going edge indicates the start of channel 0.
Display Clock Output	Jumper, P300 pin 5. LO when memory is in Store mode.
Ground	Pin 17.
POWER SOURCE	
Line Voltage Ranges	Refer to TM 500 power module performance requirements.
Power Consumption	32 W at nominal line voltage.

TABLE 2-2
Environmental

Characteristic	Performance Requirement
Temperature	
Operating	0° to +50°C.
Storage	−40° to +75°C.
Altitude	
Operating	To 15,000 feet.
Storage	To 50,000 feet.
Transportation	Qualified under National Safe Transit Committee Test Procedure 1A, Category II.

TABLE 2-3
Physical

Characteristic	Description
Weight (without accessories)	Approximately 4 lbs (1.8 kg).
Dimensions	See Fig. 2-1.

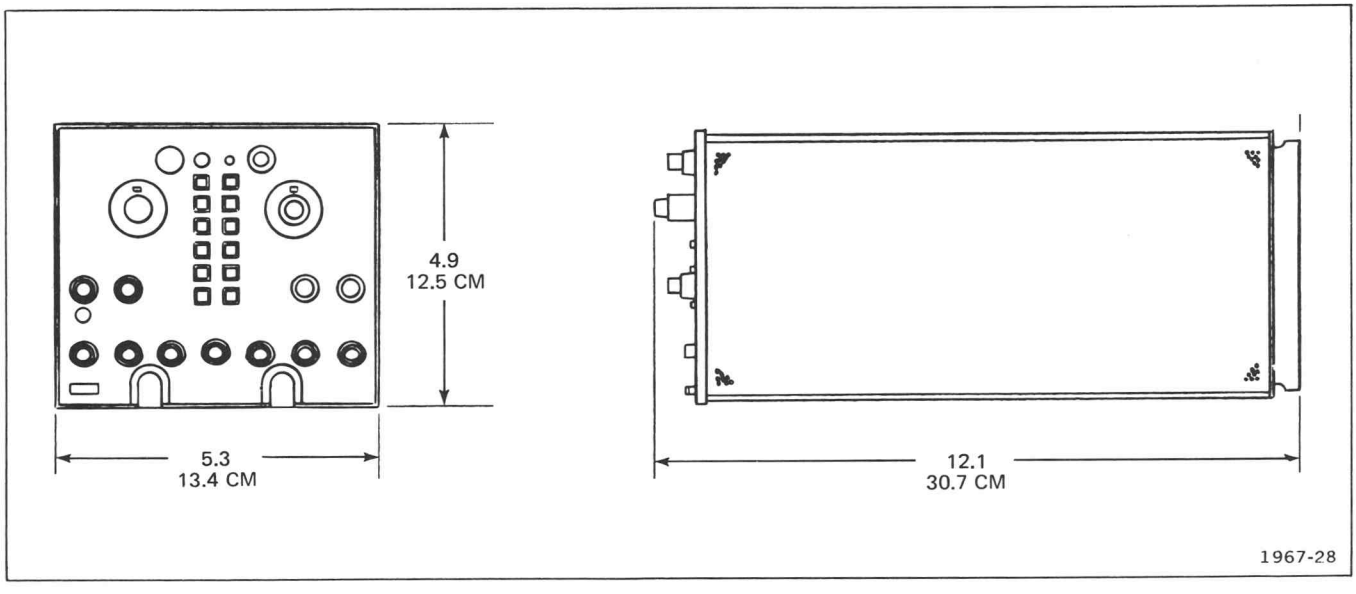


Fig. 2-1. LA 501 dimensional drawing.

STANDARD ACCESSORIES

1 ea	Instruction Manual	070-1967-00
1 ea	Operators Manual	070-2047-00
3 ea	Cables, Coaxial BNC, 50 Ohm, 42 Inch	012-0057-01
1 ea	Probe Package Includes:	010-6450-01

1 ea P6450 Probe
2 ea Lead Sets, Probe to Hook Tip (10 Leads/Set Color Coded)
2 ea Lead Sets, Probe to :025 Inch, Square Pin (10 Leads/Set Color Coded)
1 ea Data Sheet
1 ea Accessory Pouch

For more detailed information, refer to the tabbed Accessories page in the back of this manual.

RECOMMENDED ACCESSORIES

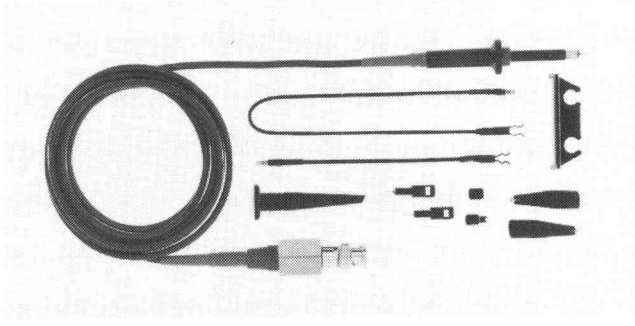
The following accessories have been selected from our catalog specifically for your instrument. They are listed as a convenience to help you meet your measurement needs. For detailed information and prices, refer to a Tektronix Products Catalog or contact your local Tektronix Field Representative.

PROBE

P6108: Miniature passive modular probe. Attenuation, 10X, within 1%. Bandwidth, at least 100 MHz. Input R and C, 10 MΩ with capacitance adjustable from 15 to 47 pF. Maximum input voltage, 500 V (dc + peak ac), derated with frequency.

Cable length:

1 meter (input C, approx. 10.5 pF) Order...010-6108-01
2 meter (input C, approx. 13.0 pF) Order...010-6108-03
3 meter (input C, approx. 15.0 pF) Order...010-6108-05



CARTS

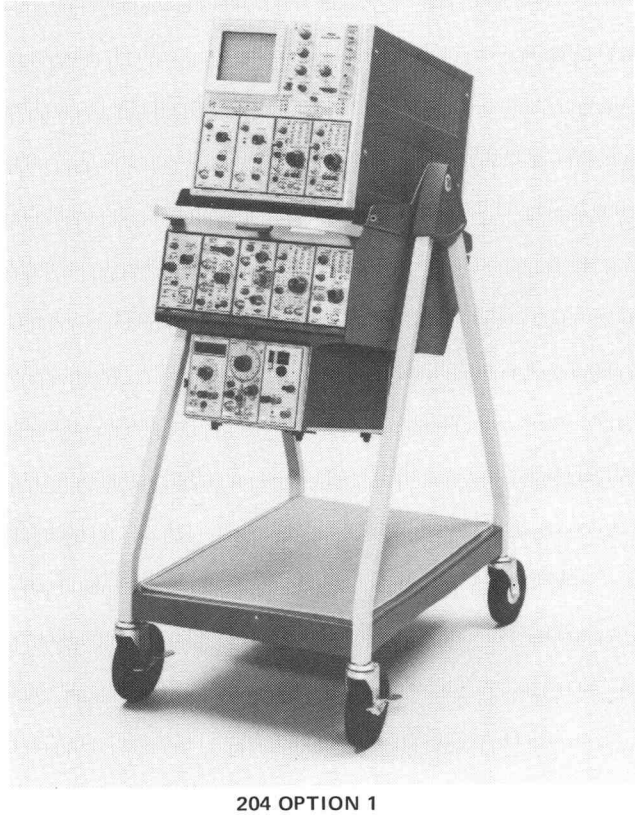
203 Opt. 1: Designed to accommodate a 5000-series or 3-plug-in compartment 7000-series oscilloscope and one TM 503 in a roll-around test-station configuration.

Order . . . . . 203 OPT. 1

204 Opt. 1: Designed to accommodate a 4-plug-in compartment 7000-series oscilloscope and one TM 503 in a roll-around test-station configuration.

Order . . . . . 204 OPT. 1

203 MOD 901R: Designed to accommodate a 400-series (except 455) oscilloscope and two TM 503's in a roll-around test-station configuration. This is a modified item; consult your local Tektronix representative for ordering information.

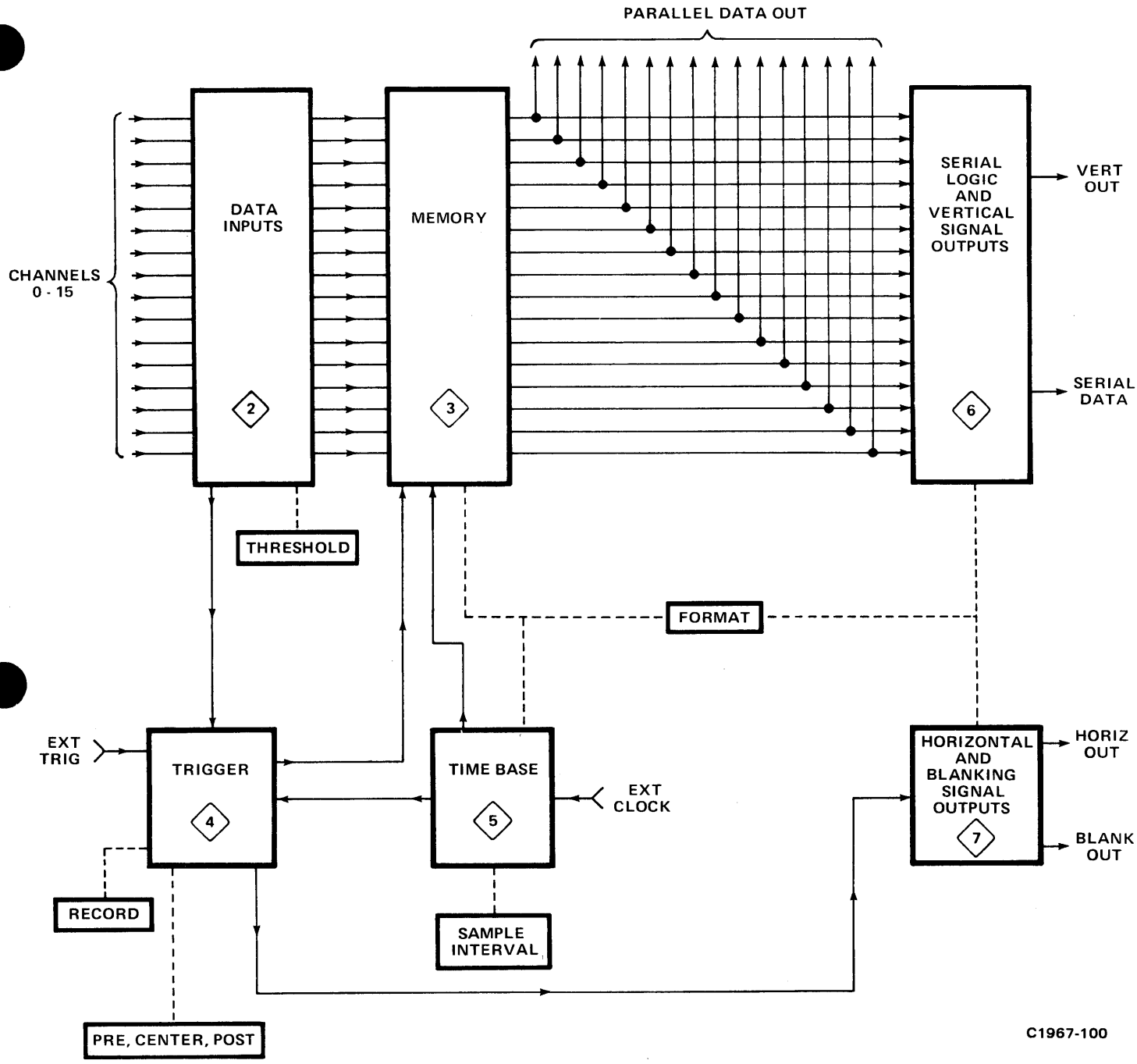


204 OPTION 1
SCOPE-MOBILE CART

INSTRUMENT OPTIONS

No options were available for this instrument at the time of this printing.

Information on any supsequent options may be found in the CHANGE INFORMATION section in the back of this manual.



Block Diagram.

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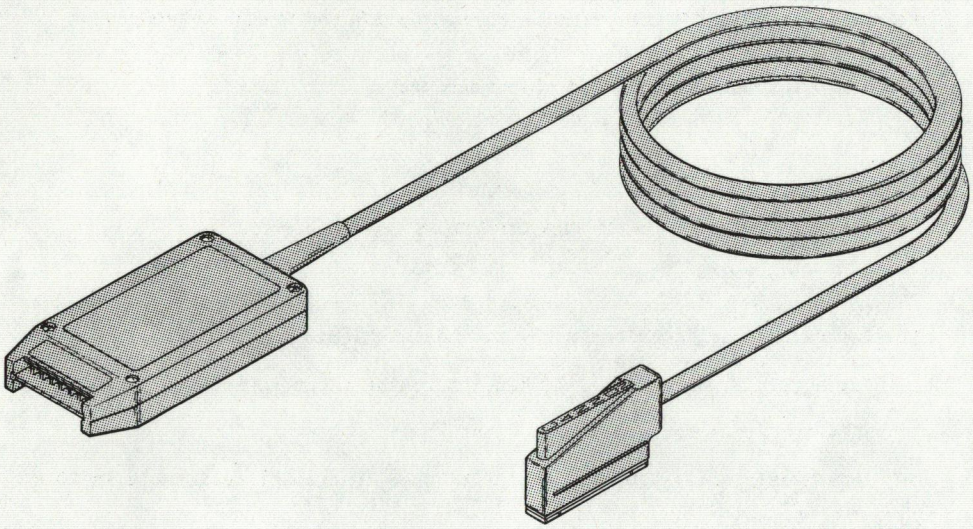
data sheet

PARTS PUBLICATION

P6450

PROBE ASSY, DATA ACQUISITION



The P6450 is a multiple input, 5X, passive probe for use with digital circuit analysis instruments, such as the LA501. The probe has 16 independent 5X attenuation inputs, 3 straight through connectors (A, B, and C) for customer assignment, and one ground. The 5X attenuation is compatible with instruments having an input resistance of 20KΩ and an input capacitance of approximately 20 pf.

The probe leads lock into the probe head. They will not pull out if the probe lead is accidently pulled. To remove a probe lead, place your fingernail on the connector and pull. To insert a probe lead, push the connector into the probe head as shown in Figure 1, page 4. Be sure the correct side of the connector is facing upward.

The probe leads come in 4 sets of 10 leads. There are 10 different colored leads in each set. Two sets of leads are terminated with retractable hook. The other two sets of leads are terminated in square-pin connectors.

NO. 062-1799-00
DATE MAR. 1976 (R)

WARRANTY

All TEKTRONIX instruments are warranted against defective materials and workmanship for one year. Any questions with respect to the warranty should be taken up with your TEKTRONIX Field Engineer or representative.

All requests for repairs and replacement parts should be directed to the TEKTRONIX Field Office or representative in your area. This will assure you the fastest possible service. Please include the instrument Type Number or Part Number and Serial Number with all requests for parts or service.

Specifications and price change privileges reserved.

U.S.A. and foreign TEKTRONIX products covered by U.S. and foreign patents and/or patents pending.

TEKTRONIX is a registered trademark of Tektronix, Inc.

SPECIFICATIONS

ELECTRICAL

All electrical specifications apply to channels 0 through 15 only.

Attenuation: 5X within 3% (when instrument input resistance is 20 kΩ within 1%). Series resistor 81 kΩ within 1.1%

Input Resistance: 100 kΩ within 3% (when instrument resistance is 20 kΩ within 1%).

Input Capacitance: (without test leads) approximately 45 pF (with probe connected to instrument).

Risetime (Probe Only): 9 ns (channels, 0, 1, 2, 3,); 15 ns (channels 4-15).

Maximum Input Voltage: 50 V (dc + peak ac).

Probe delay time (from end of signal input lead to multi-pin connector): Approximately, 15 nsec.

ENVIRONMENTAL

Probe operates within specifications over the following ranges:

Temperature; 0 C to +75 C (32 F to 167 F).

Altitude: To 15,000 ft.

PHYSICAL

Net Weight: 377 gms (13.3 oz).

Length: Probe; 1.5 m (4.9 ft).

Input Leads; 40 cm (15.7 in).

MAINTENANCE

The P6450 contains only passive components. These components are located on 2 circuit boards, one in the probe head and one in the multipin cable connector body.

PROBE HEAD COMPONENT ACCESS

1. Remove 4 screws from the probe head.
2. While pulling apart the 2 halves of the probe head body, make note of which half of the body covers which side of the circuit board.
3. Replace the defective components.
4. When reinstalling the circuit board be sure the correct half of the body covers the correct side of the circuit board. Verify by tracing ground braid connection to the ground input.

MULTIPIN CONNECTOR COMPONENT ACCESS

1. Set the connector locking flange to gain access to the 3 screws (see Figure 2).
2. Remove 2 screws and loosen 1 screw.

CAUTION

The leads from the cable to the circuit board are fragile. Be careful not to damage them.

3. Carefully push the cable into the plastic body while pulling out the connector.
4. Replace the defective component.
5. To reassemble, carefully pull on the cable while guiding the connector and circuit board back into the plastic body.
6. Replace the 3 screws.

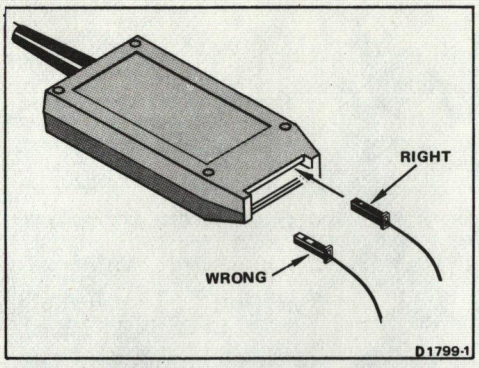


FIGURE 1

TABLE 1

PROBE INPUTS	CONNECTOR PINS
1	16
2	18
3	20
4	15
5	17
6	19
7	21
8	1
9	3
10	5
11	7
12	2
13	4
14	6
15	8
	12 N.C.
	22 N.C.
	25 N.C.

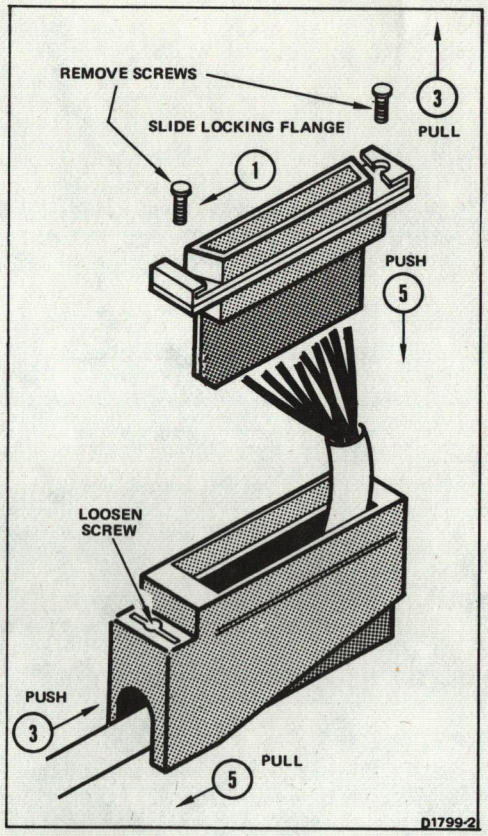
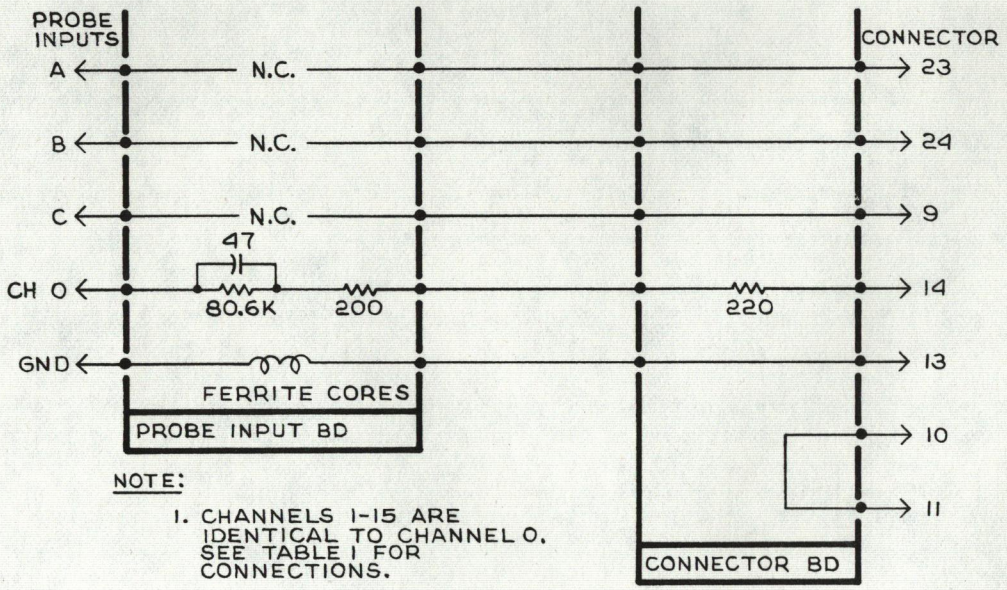


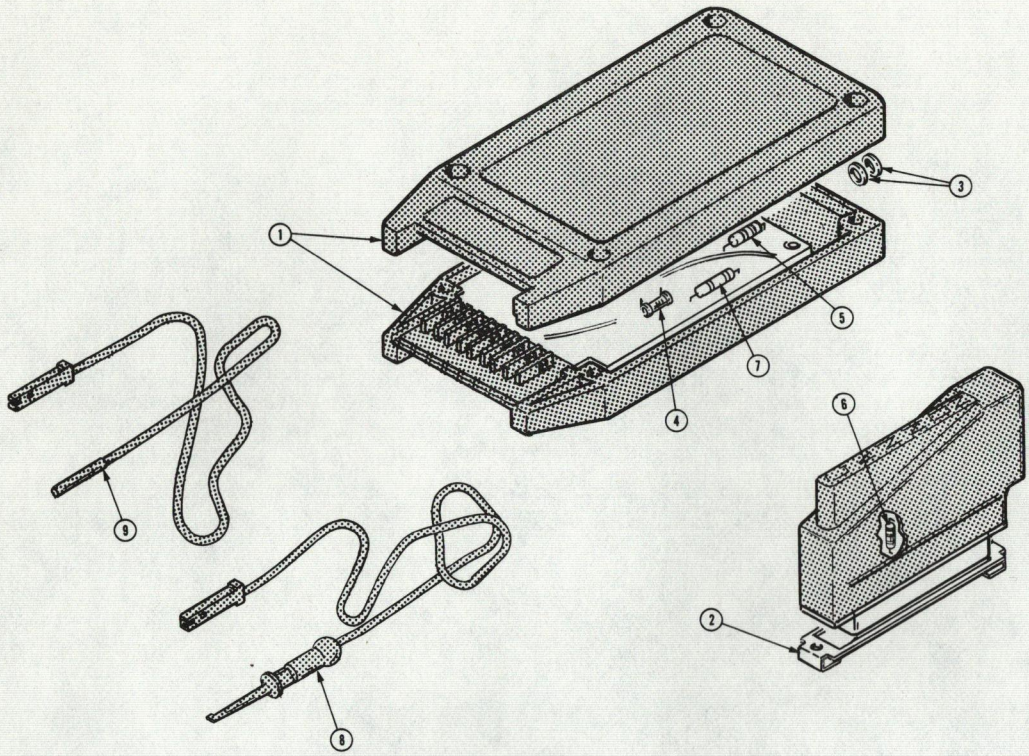
FIGURE 2

SCHEMATIC



NOTE:

1. CHANNELS 1-15 ARE IDENTICAL TO CHANNEL 0. SEE TABLE 1 FOR CONNECTIONS.



Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						MECHANICAL PARTS LIST		
	010-6450-01			1		PROBE,DATA ACQ:MULTI LEAD,W/ACCESSORIES	80009	010-6450-01
	010-6450-00			1		. PROBE,DATA ACQ:MULTILEAD,20	80009	010-6450-00
-1	380-0463-01			1		. . HOUSING,PROBE:W/IDENTIFICATION MARKERS	80009	380-0463-01
-2	343-0323-00			1		. . RETAINER,CONN:25 PIN D CONN,SLIDE LOCK	09133	DB51221-1
						ELECTRICAL PART LIST		
-3	276-0596-00			2		. . CORE,TOROID,FER:0.09 ID X 0.19 OD X 0.08"H	78488	56-1657
-4	281-0651-00			16		. . CAP.,FXD,CER DI:47PF,5%,200V	72982	374-001T2H0470J
-5	315-0201-00			16		. . RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
-6	317-0221-00			16		. . RES.,FXD,CMPSN:220 OHM,5%,0.125W	01121	CB2215
-7	321-0376-00			16		. . RES.,FXD,FILM:80.6K OHM,1%,0.125W	75042	CEATO-8062F
						ACCESSORIES		
-8	012-0670-00			2		. LEAD SET,TEST:W/10 15.748L WIRES W/CONNECTORS	80009	012-0670-00
-9	012-0655-01			2		. LEAD SET,TEST:INPUT,W/10 15.748L WIRES	80009	012-0655-01
	016-0537-00			1		. POUCH,ACCESSORY:6" X 9" W/ZIPPER	80009	016-0537-00
	062-1799-00			1		. DATA SHEET:P6450(not shown)	80009	062-1799-00

CROSS INDEX MFR. CODE NUMBER TO MANUFACTURER

MFR.CODE	MANUFACTURER	ADDRESS	CITY,STATE,ZIP
01121	ALLEN-BRADLEY CO.	1201 2ND ST. SOUTH	MILWAUKEE, WI 53204
09133	KIERULFF ELECTRONICS, INC.	2585 COMMERCE WAY	LOS ANGELES, CA 90015
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
78488	STACKPOLE CARBON CO.		ST. MARYS, PA 15857
80009	TEKTRONIX, INC.	P. O. BOX 500	BEAVERTON, OR 97077

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

SERVICE NOTE

Because of the universal parts procurement problem, some electrical parts in your instrument may be different from those described in the Replaceable Electrical Parts List. The parts used will in no way alter or compromise the performance or reliability of this instrument. They are installed when necessary to ensure prompt delivery to the customer. Order replacement parts from the Replaceable Electrical Parts List.

CALIBRATION TEST EQUIPMENT REPLACEMENT

Calibration Test Equipment Chart

This chart compares TM 500 product performance to that of older Tektronix equipment. Only those characteristics where significant specification differences occur, are listed. In some cases the new instrument may not be a total functional replacement. Additional support instrumentation may be needed or a change in calibration procedure may be necessary.

Comparison of Main Characteristics

DM 501 replaces 7D13		
PG 501 replaces 107	PG 501 - Risetime less than 3.5 ns into 50 Ω.	107 - Risetime less than 3.0 ns into 50 Ω.
108	PG 501 - 5 V output pulse; 3.5 ns Risetime.	108 - 10 V output pulse; 1 ns Risetime.
111	PG 501 - Risetime less than 3.5 ns; 8 ns Pretrigger pulse delay.	111 - Risetime 0.5 ns; 30 to 250 ns Pretrigger Pulse delay.
114	PG 501 - ±5 V output.	114 - ±10 V output. Short proof output.
115	PG 501 - Does not have Paired, Burst, Gated, or Delayed pulse mode; ±5 V dc Offset. Has ±5 V output.	115 - Paired, Burst, Gated, and Delayed pulse mode; ±10 V output. Short-proof output.
PG 502 replaces 107		
108	PG 502 - 5 V output	108 - 10 V output.
111	PG 502 - Risetime less than 1 ns; 10 ns Pretrigger pulse delay.	111 - Risetime 0.5 ns; 30 to 250 ns Pretrigger pulse delay.
114	PG 502 - ±5 V output	114 - ±10 V output. Short proof output.
115	PG 502 - Does not have Paired, Burst, Gated, Delayed & Undelayed pulse mode; Has ±5 V output.	115 - Paired, Burst, Gated, Delayed & Undelayed pulse mode; ±10 V output. Short-proof output.
2101	PG 502 - Does not have Paired or Delayed pulse. Has ±5 V output.	2101 - Paired and Delayed pulse; 10 V output.
PG 506 replaces 106	PG 506 - Positive-going trigger output signal at least 1 V; High Amplitude output, 60 V.	106 - Positive and Negative-going trigger output signal, 50 ns and 1 V; High Amplitude output, 100 V.
067-0502-01	PG 506 - Does not have chopped feature.	0502-01 - Comparator output can be alternately chopped to a reference voltage.
SG 503 replaces 190, 190A, 190B	SG 503 - Amplitude range 5 mV to 5.5 V p-p.	190B - Amplitude range 40 mV to 10 V p-p.
191	SG 503 - Frequency range 250 kHz to 250 MHz.	191 - Frequency range 350 kHz to 100 MHz.
067-0532-01	SG 503 - Frequency range 250 kHz to 250 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
TG 501 replaces 180, 180A	TG 501 - Marker outputs, 5 sec to 1 ns. Sinewave available at 5, 2, and 1 ns. Trigger output - slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	180A - Marker outputs, 5 sec to 1 μs. Sinewave available at 20, 10, and 2 ns. Trigger pulses 1, 10, 100 Hz; 1, 10, and 100 kHz. Multiple time-marks can be generated simultaneously.
181	TG 501 - Marker outputs, 5 sec to 1 ns. Sinewave available at 5, 2, and 1 ns.	181 - Marker outputs, 1, 10, 100, 1000, and 10,000 μs, plus 10 ns sinewave.
184	TG 501 - Marker outputs, 5 sec to 1 ns. Sinewave available at 5, 2, and 1 ns. Trigger output - slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	184 - Marker outputs, 5 sec to 2 ns. Sinewave available at 50, 20, 10, 5, and 2 ns. Separate trigger pulses of 1 and .1 sec; 10, 1, and .1 ms; 10 and 1 μs. Marker amplifier provides positive or negative time marks of 25 V min. Marker intervals of 1 and .1 sec; 10, 1, and .1 ms; 10 and 1 μs.
2901	TG 501 - Marker outputs, 5 sec to 1 ns. Sinewave available at 5, 2, and 1 ns. Trigger output - slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	2901 - Marker outputs, 5 sec to 0.1 μs. Sinewave available to 50, 10, and 5 ns. Separate trigger pulses, from 5 sec to 0.1 μs. Multiple time-marks can be generated simultaneously.

NOTE: All TM 500 generator outputs are short-proof. All TM 500 plug-in instruments require TM 500-Series Power Module.

TEKTRONIX®
committed to technical excellence

MANUAL CHANGE INFORMATION

PRODUCT LA 501 Operators
070-2047-00

CHANGE REFERENCE C1/1176
DATE 11-10-76

CHANGE:	DESCRIPTION

TEXT CORRECTIONS

Page 1-1, right column

CHANGE: Delete the CLOCK OUT heading and accompanying text. Insert the following:

1 MHz CLOCK OUT: Provides an unterminated (negative voltage ECL level) 1 MHz clock from an internal time base.

CHANGE: Delete the INVALID MODE heading and accompanying text. Replace it with the following:

AUX CLOCK INPUT. Provides for an external ECL level Store/Display Clock signal input.

AUX CLOCK INPUT. Provides an input for ECL level trigger signal.

Page 1-3, item 16, FORMAT

CHANGE: The third line should read "Maximum sample interval is 20 nanoseconds."

The fifth line should read "Maximum sample interval is 50 nanoseconds."

Page 1-6, right column, just ahead of the "Preliminary Set Up" heading

CHANGE: Insert the following text.

Setting The Internal Jumpers

The internal jumpers should be set to the positions that will give the desired operation. The jumpers and their functions are as follows:

P831-Clock Polarity (positive - pin 1 to pin 2*; negative - pin 2 to pin 3) and Variable Threshold Trigger (pin 3 to pin 4).

P629-Trigger Lockout (pin 1 to pin 2)* and Bad Data Blanking (pin 2 to pin 3).

P608-CH 0 Trigger (pin 2 to pin 3)*, Auxiliary Trigger (pin 3 to pin 4).

P136-Clock Ticks (pin 1 to pin 2)* and No Clock Ticks (pin 2 to pin 3).

P120-Trigger Sync Output (pin 1 to pin 2)* and Trigger Sync Input (pin 2 to pin 3).

P101-Auxiliary Clock (pin 2 to pin 3)* and Ext Store/Display Clock (pin 1 to pin 2).

P100-Display Clock (pin 1 to pin 2)* and Ext Store/Display Clock (pin 2 to pin 3).

Note: *indicates jumper position when shipped from the factory.

CHANGE:	DESCRIPTION

Page 1-7, left column, step 7.

CHANGE: Re-word Step 7 as follows:

7. Set the oscilloscope for X-Y mode and ground the inputs. Postion the resulting dot display to center screen and adjust the oscilloscope for a well-defined display. If necessary, refer to the oscilloscope instruction manual for operating instructions.

Page 1-10, left column, between the paragraphs title DATA OUTPUT CABLE and COAXIAL CABLE.

CHANGE: Insert the following note.

NOTE

When inputting ECL data on a P6450 probe and outputting parallel data on J120, complete shielding between connectors and cables is needed. Therefore, shielded cables and connectors should be used on J120.

Page 1-11, Steps 3 and 4.

CHANGE: Delete the last two sentences of Step 3. In Step 4, delete the words "Square front corner and".

Page 1-12, left column, top paragraph

CHANGE: Delete the last two sentences in the paragraph and insert the following headings and text before the paragraph titled "MONITOR".

INTERNAL JUMPERS:

P831-External Clock Polarity Selector.

In the first two positions, P831 selects external clock polarity. In the third position, it provides a means to use the EXT CLOCK connector on the front panel as a Variable Threshold Trigger source.

P629-Bad Data Blanking Selector.

This jumper is used to select either Trigger Lockout or Bad Data Blanking triggering mode.

P608-Internal Trigger Selector.

This jumper permits selection of CH 0 or Auxiliary Trigger Input as the trigger source when the front panel SOURCE pushbutton is in CH 0 position.

CHANGE:	DESCRIPTION

P136-Clock Tick Selector.

Allows positive or negative Clock Ticks to be added to each channel of displayed data. Each Clock Tick represents the active edge of the Store Clock signal; moving the jumper disables the Clock Ticks.

P100-Display Clock Selector.

In a master/slave configuration (cascaded LA 501's), P100 provides the means to connect the Ext/Store/Display Clock from the master unit to the display clock circuitry in the slave unit.

P101-Ext Store/Display Clock Selector.

This jumper selects the Auxiliary Clock for the Store Clock. In a master/slave configuration, P101 connects the Ext Store/Display Clock to both the Store Clock and P100.

P120-Trigger Sync Selector.

Selects master or slave mode of operation. In master/slave configuration, synchronizes the memory multiplexers in the slave unit to the master unit.

Page 1-12. Fig. 1-7

Figure 1-7 is in error. The callout that reads negative edge should read positive edge and vice versa.

Page 1-13, under "Z BLANK OUT" at the bottom of the right hand column, add the following:

For Serial No.s B010245 and below, the only function of the Z-axis blanking signal is to blank the crt retrace lines.

Page 1-14, right column, under the"DATA INPUT" heading, fifth line. CHANGE: Delete all text under the foregoing head following the word "connector". in the fifth line.

Page 1-15, top of the right column, under "Z-AXIS INPUT", change to read as follows:

Z-AXIS INPUT. This connection permits control of display intensity with an externally generated signal. As the external signal goes positive (5 volts maximum) the display intensifies.

CHANGE:	DESCRIPTION

Page 1-15, right column, under "RECORD ENABLE", change to read as follows:

RECORD ENABLE. This connection is provided to set the memory into the Store Mode by application of an external signal. A HI pulse at ECL level is required.

Page 1-15, Fig. 1-8.

CHANGE: Delete superscripts 3, 4, and 5. Change the nomenclature describing functions of J100 as follows:

9. AUX TRIGGER INPUT
22. AUX CLOCK INPUT
23. CLOCK STATUS
24. CLOCK STATUS
25. 1 MHz CLOCK OUTPUT

Page 1-16, Fig. 1-9.

CHANGE: Change the nomenclature describing pin functions of J120 as follows:

2. P300 PIN 1^1
5. P300 PIN 2^1

Page 1-17, left column.

CHANGE: Delete the paragraph entitled "INVALID MODE INPUT".

Page 1-17, Fig. 1-10

CHANGE: Change the nomenclature describing the pin functions of P300 as follows:

1 -TO J120, PIN 2
2 -TO J120, PIN 5
4 -TRIGGER SYNC
7 -MASTER RECORD ENABLE
11 -EXT STORE/DISPLAY CLOCK OUTPUT
12 -EXT STORE/DISPLAY CLOCK INPUT

Pins not listed retain their original nomenclature. Pins 11 and 12 are additions. In the detail circle showing the jumper positions, remove the jumper between 4 and 7, and add pins 11 and 12.

Page 1-17, left column, change the text under the FRAME OUTPUT heading as follows:

CHANGE: This connection provides for the output of an unterminated ECL level pulse. The negative edge of the frame output pulse indicates the start of channel 3 data. One complete pulse cycle represents one complete serial scan of data in the memory in 16-channel operation, two scans in 8-channel operation, and four scans in 4-channel operation.

CHANGE:	DESCRIPTION

Page 2-3, in the lower part of Table 2-1, the CRT Retrace Blanking Time Performance Requirement should read as follows:

4.2 µs within 20% (2 bits)

2.2 µs within 20%, (1 bit)

1.2 µs within 20%, (1/2 bit)

Page 2p3, in the lower part of Table 2-1, the Horizontal Output-Linearity Performance Requirement should read:

Pulse width within 10% from 1% ot 100% of sweep.

Page 2-4 Following the title "Low-Impedance Data Input",

INSERT: (J100)

Page 2-4, under Low-Impedance Data Input

CHANGE: Clock Out, and its Performance Requirement to:

1 MHz Clock Output — Pin 25, Unterminated ECL level. When terminated, the output is a standard, negative voltage ECL 1 MHz signal.

DELETE: Invalid Mode and its Performance Requirement.

DELETE: + 5 Volts and its Performance Requirement.

Page 2-4, following the last characteristic under Low-Impedance Data Input:

ADD: Aux Clock Input — Pin 22. Input to Store/Display clock gate. (Negative level ECL.) Selected by P101.

ADD: Clock Status Output — Pins 23, 24. Both pins are HI (gnd.) when SAMPLE INTERVAL switch is in EXT position.

ADD: Aux Trigger Input — Pin 9. Provides trigger signal input from J100. (Negative level ECL.)

Pages 2-4 & 2-5, following the title "DATA OUTPUT",

INSERT: J(120)

Pages 2-4 & 2-5, under Data Output

CHANGE: The Performance Requirement of Record Enable to read as follows:

Positive going pulse at ECL levels sets memory into record mode.

CHANGE: The Performance Requirement of Frame Output

Jumper, P300 pin 8. A negative going edge indicates the start of Channel 3.

CHANGE:	DESCRIPTION

Page 2-5, following the last characteristic under Data Output:

ADD: Trigger Sync Output	Jumper, P300 pin 4. Permits synchronous displayed data from two or more units (master-slave operation).
ADD: Master Store Enable Output	Jumper, P300 pin 7. Sets slave unit (s) to Store mode (master-slave operation).
ADD: Ext Store/Display Clock Output	Jumper, P300 pin 11. Master unit clock signal output for use by slave units (s).
ADD: Ext Store/Display Clock Input	Jumper, P300 pin 12. Clock signal input for slave unit (s) from master unit.

Page 2-5, following the last newly added characteristics under Data Output add a new major title 'REAR INTERFACE CONNECTOR'.

ADD: Display Clock Input	B21 (same as J120-3)
ADD: Serial Data Output	B19 (same as J120-4)
ADD: Display-Store Mode Output	B20 (same as P300-6)
ADD: Frame Output	B12 (same as P300-8)
ADD: CHANNEL/POSITION SELECT OUTPUT	B25 Indicates channel selected by CHANNEL/POSITION SELECT switch.