# This month we will take an in depth look at a new monolithic IC analog-to-digital converter set from Siliconix 

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first hybrid and now monolithic ic analog to digital converters in single and dual-chip versions are replacing expensive and complicated discrete circuitry. The A/D converter is the backbone of most digital-readout measurement equipment. Already digital readouts have replaced meter movements in many professional electronic instruments where rapid, accurate and error free readings are vital. Digital readouts are cropping up where there were no meters at all in the past. Today there are oscilloscopes that have built-in digital voltmeters, frequency counters and time-period meters. In some models, the readout is viewed on the CRT screen and there are no LED indicators. It seems that the only place where the meter movement will stay put are inexpensive voltmeters and in those applications where up and down trends are important.

An on-the-chip AC to DC converter and
resistance measurement system would be a nice addition to the $\mathrm{A} / \mathrm{D}$ complement. Even though the technology and circuits are here today, manufacturers have plenty of things to do and what seems like a good idea to us may not be one that brings the most, or for that matter even any profits to them. Operational amplifiers and hybrids handle these secondary functions well, so the AC/OHM chip may be a little while off

Nevertheless, the monolithic A/D converter is a new powerful tool for the engineer, technician, and experimenter. I'm sure the usual ingenuity of the nonprofessional technical society, applied to this previously out of reach technique will lead to some intriguing contrivances.

## Siliconix 3½-digit A/D converter

By adding some external components to Siliconix's (2201 Laurelwood Rd., Santa Clara, CA 95054) LD110-LD111

IC team, a $31 / 2$-digit 0 to $\pm 200-\mathrm{mV}$ or 0 to $\pm 2$-volt digital voltmeter can be easily constructed. Frequency, temperature, AC voltage and other variables of interest can be measured by putting the corresponding variable-to-DC converter in front of the analog-to-digital converter set.
The LD110 is a PMOS $p$-channel metal-oxide semiconductor synchronous digital processor, and the LD111 is an analog processor made with combined bipolar-PMOS technology. Fig. 1 is a block diagram that shows the internal partitioning of the 2 -chip system. Fig. 2 details the hook up for the $\pm 2$-volt DVM.
As with many A/D conversion techniques, this system uses a comparator to balance the input voltage against an analog voltage derived from the system's digital output. In other words, there is a digital-to-analog converter in a feedback


FIG. 1-SILICONIX'S ANALOG-TO-DIGITAL CONVERTER consists of the LD110 and LD111 IC's.

path of the $A / D$ converter. In the LDIIO-LDIII charge-balancing scheme, an up-down counter is controlled by a comparator to step in one direction or the other depending on whether the input is higher or lower than the accumulated number in a $B C D$ counter. The $D / A$ conversion is done by adding or depleting charge on an integrating capacitor. When the system stabilizes, the net count on the $31 / 2$-digit decade counter is stored in binary latches and multiplexed or sequentially sampled to drive a binary-to-7segment decoder to operate the LED display segments.

A buffer amplifier gives the LDIII its high input impedance at pin 15. At room temperature the input bias current is specified as 4 picoamperes typical. With the system set up for 2 volts full scale. the smallest input voltage of interest would be 100 mV . Dividing voltage by current $0.1 / 4 \times 10^{-12}=25 \times 10^{9}$ ohms. At $70^{\circ} \mathrm{C}$ the input current increases an order of magnitude to 40 pA , but $25 \times$ $10^{*}$ ohms is still a formidable number, 2500 megohms. High input impedance is essential to maintain accuracy because of loading on the input attenuator and series filter resistance.

The output of the buffer feeds the integrator through $\mathbf{R 2}$ to pin 9. This circuit is an operational integrator with a negative feedback path between the input and output of the high-gain amplifier through $\mathrm{C}_{\text {in }}$. Like all operational amplifiers, the feedback keeps the am-
plifier's differential input stage very close to balance. This means that the positive and negative inputs are very nearly the same voltage. The positive input is grounded so the negative input is forced to stay close to 0 volts. Current into the negative input terminal is stored by the capacitor. Held at a virtual ground the pin 9 side of the capacitor cannot change potential, so the pin 11 side, the integrator output, changes potential as charge flows in and out of the capacitor. Three inputs feed the virtual ground integrator input: the huffered input voltage through $R 2$, the up-down counter switched reference voltage through R1, and the auto-zero amplifier output $\mathrm{V}_{\mathrm{A} \%}$ through R3.
Before looking at the details of the measurement process, let's see how the auto-zero system works to cancel the effects of offset along with temperature and component drifts. The analog-todigital conversion set operates synchronously. All processing is timed in relation to an externally supplied clock frequency between 2 and 76 kHz . A complete measurement and auto-zero sequence is made up of 6144 clock cycles. Dividing $30,720 \mathrm{~Hz}$ by 6144 tells us that this particular choice of clock frequency results in 5 measurements per second. The 6144 cycles are subdivided into 4096 cycles for the measurement, and half this count or 2048 is for the automatic zeroing process. Selecting the clock frequency so its period is an integral
multiple of the AC line period gives the meter its best $60-\mathrm{Hz}$ rejection. Fo example, $24,576 \mathrm{~Hz}$ gives a sampling frequency of 4 per second or a period of $1 / 4$ second. One third of this time, the shorter of the two intervals spent in the autozero mode, is $1 / 12$ second. This is five times the $1 / 60$-second power line pariod and the rejection condition is satisfied.

When the LD110 control logic initiates the auto-zero interval, the input 0 : the huffer amplifier is grounded through LD111 pin 2, and the measure/zero mode switch is changed to the zero position. One other change takes slace in this system configuration; after a short initial interval which corrects fo: an error discussed later, the UP/D(IWN switch in the analog processor is to gled with a $50 \%$ duty cycle. For 4 lock pulses the switch is in the UP position and for 4 counts it is in the DOWN position. The three switches in the LD I 1 I are PMOS enhancement devices. The somparator performs no useful funztion during the zeroing process and the updown counter is reset. There is a leedback path paralleling $\mathrm{C}_{\text {INT }}$ by the connection of the auto-zero amplifier through the measure/ZERO switch.

Starting at the output of the integrator, the path is traced through the auto zero amplifier and through R3 to the int:grator input node. The auto-zero loop selfadjusts so the net integrator imput current is zero towards the end of the interval. The current through R 3 is $V_{A z} /$

R3 and must equal the current through R1. R1 is connected to the $50 \%$ duty cycle waveform that has an average value of $\mathrm{V}_{\text {HEF }} / 2$. Therefore $-\mathrm{V}_{\mathrm{Az}} / \mathrm{R} 3=$ $\mathrm{V}_{\mathrm{HEF}} / 2 \mathrm{R} 1$, or $\mathrm{I}_{3}=\mathrm{V}_{\mathrm{AZ}} / \mathrm{R} 3=-\mathrm{V}_{\mathrm{BEF}} /$ 2RI. An approximation sign is used because an input offset error in the buffer amplifier produces an off-zero buffer output voltage and adds another current through R2.
Offset errors in the integrator cause it to seek equilibrium at some slightly offzero potential. $\mathrm{V}_{\mathrm{A} /}$ holds a small component on top of its $\mathrm{V}_{\text {GEF }}$ component that compensates for these errors through the following measurement interval. Any error drifts between any two successive sampling times are corrected during the next auto-zero interval. In effect, an extremely high dc gain negative feedback loop reduces the errors to a miniscule value. $\mathrm{V}_{\mathrm{A}}$ is held by $\mathrm{C}_{\text {sтик; }}$ retaining the voltage when the measure/zero switch disconnects the capacitor from R4.

At the 2048th clock count, the system switches to the measurement mode and the comparator takes over control of the up-down counter. Counting up when the comparator output is low, the UP/ down switch is up for seven clock pulses and down for one and the inverted output of the comparator ramps downward. The duty cycle is reversed for a high comparator output, seven cycles down and one up, and the comparator output ramps upward. Don't be confused by the labeling of the UP-IDOWN switch that is connected to the reference supply in the DOWN state and to ground in the UP state. Integration of the net six counts, up or down, by the current through R 1 is the mechanism of the digital-to-analog conversion mentioned earlier.

It is now possible to calculate what the digital output will read to figure out what relationship between R1 and R2 must be satisfied to calibrate the converter. Once again, the net current at the input node of the integrator must be zero at equilibrium, after the system reacts to a possibly changed input and then settles down. The current in R1 is $\mathrm{V}_{1 \mathrm{~N}} / R 2$ and the current in R3 was already calculated to be $\mathrm{V}_{\text {rerer }} /$ 2R1. R1 conducts an average current dependent on the net count. If the up and down counts are equal or NETCOUNT $=$ UPCOUNT - DOWNCOUNT $=\mathrm{O}$, the UP-DOWN switch will be in one position for the same time as in the other position so the average current is one-half the peak $V_{\text {Hef }} / R 1$ or $\mathrm{V}_{\mathrm{rer}} / 2 \mathrm{R} 1$. Some deduction leads to the expression:

$$
I_{i}=\frac{V_{\mathrm{REF}}}{2 \mathrm{R} 1}\left(1-\frac{\mathrm{NETCOUNT}}{4096}\right)
$$

The expression is tested by setting the net count to its top extreme. If it were possible for the switch to be UP, switched to ground for the full 4096 possible counts, $I$, should be zero and the equation agrees. Equating the sum of the currents during the measurement period to zero gives:

$$
\begin{aligned}
& \frac{\mathrm{V}_{1:}}{\mathrm{R} 2}-\frac{\mathrm{V}_{\mathrm{nEF}}}{2 \mathrm{R} 1}+ \\
& \left(1-\frac{\text { NETCOUNT }}{4096}\right)=0 \text { and }
\end{aligned}
$$

NETCOUNT $=8192 \times \mathrm{R} 1 / \mathrm{R} 2 \times \mathrm{V}_{\mathrm{IN}} /$ $\mathrm{V}_{\text {kef }}$.

Picking $V_{\text {ner }}=6.8$ volts as in Fig. 2 and choosing a full-scale reading of 2000 for an input $\mathrm{V}_{1 \mathrm{~N}}=2$ volts:
$2000=8192 \times \mathrm{R} 1 / \mathrm{R} 2 \times 2 / 6.8$ and $R 1 / R 2=6.8 / 2 \times 2000 / 8192=0.83$.
Significantly, the frequency of the oscillator does not enter the calculation so conversion accuracy does not depend on its stability! The accuracy specified by Siliconix is $0.05 \% \pm 1$ count. After the system settles down, the integrator current hunts above and below the comparator reference voltage $\mathrm{V}_{\text {stir }}$ because the integrator must charge and discharge with the discrete net 6 count stimulus of the UP/Down switch. The error is predictable and is compensated for by the short override period at the start of the auto-zero process. Input polarity is sensed by whether the system is counting up or down when its net count passes through zero.

The digital voltmeter in Fig. 2 is calibrated to read $\pm 2.000$ volts fullscale. R1 composed of the fixed part R1-a and potentiometer R1-b is adjustable between 75 and 95 K , and R 2 is a 100 K resistor. The R1/R2 combination can be varied from 0.75 to 0.95 straddling the 0.83 number calculated. These resistors are picked to be temperature and time stable since they determine the instrument's calibration.

Common-cathode type LED's are used in the design and their cathodes are driven from 4 of the sections of a 7416 hex inverter. Excecding 1.999 volts at the input triggers an over-range alarm by blinking the display at the sampling rate- 4 times a second. To conserve IC terminals, reduce the number of necessary decoders to one, and increase the efficiency of the ILED emission; the display is multiplexed or scanned one digit at a time in an interlaced 1-3-2-4 pattern. An FET constant-current source biases the 6.8 -volt reference Zener and a 555 timer IC generates the $24.5-\mathrm{kHz}$ clock waveform.

Over-range and under-range conditions are coded on the 3rd and 4th bits of the LD110 BCD output during the 4th digit strobe time. Under-range, predetermined as $5 \%$ of full scale, is indicated by a 1 in the bit 3 position. Over-range is detected by sensing all four digits in a zero state. Not used in the illustrated DVM, this feature is useful in building automatic ranging voltmeters.

One last point: the A/D converter is capable of operating beyond the 2000 count to 3100 . Each 7 up and 1 down count or the reverse situation requires 6 of the 8 pulses. The useable number of clock cycles is then $3 / 4$ of 4096 or about 3100 leading to the maximum useable count. An erroneous display shows up in the fourth digit place when an extended count is allowed unless bit 3 and 4 inputs to the BCD to 7 -segment decoder are grounded during the digit strobe time.

## Class E citizen band transistors

Motorola Semiconductor Products has two new transistors, the MRF225 and

MRF226, which have maximum RF output powers of 1.5 and 13 watts respectively at 225 MHz . Both transistors have a minimum 9 dB power gain. The coordinates of the cross mark on Fig. 3 are 1.3 watts in, 13 watts out. Power gain calculates as $10 \log \frac{13}{1.3}=10 \log 10=10$ dB gain.


FIG. 3-OUTPUT POWER vs. INPUT POWER for Motorola's MRF-226 Citizen Band RF power transistors.

The driver-output pair sell for $\$ 2.50$ for the MRF225 and $\$ 11.70$ for the MRF226 in small quantities. R-E

## R-E's Substitution guide for

## replacement transistors

## PART XXVII

## by ROBERT \& ELIZABETH SCOTT

ARCH-Indicates the Archer brand of semiconductors sold only by Radio Shack and Allied Radio stores. Allied Radio Shack, 2725 W. 7th St., Ft. Worth, Texas 76107
DM-D. M. Semiconductor Co., P.O. Box 131, Melrose, Mass. 02176
G-E-General Electric Co., Tube Product Div., Owensboro, Ky. 42301

ICC-International Components, 10 Daniel Street, Farmingdale, N.Y. 11735
IR-International Rectifier, Semiconductor Div., 233 Kansas St., El Segundo, Calif. 90245
MAL-Mallory Distributor Products Co., 4760 Kentucky Ave., Indianapolis, Ind. 46241
MOT-Motorola Semiconductors, Box 2963 , Phoenix, Ariz. 85036
RCA-RCA Electronic Components, Harrison, N.J. 07029
SPR-Sprague Products Co., 65 Marshall St., North Adams, Mass. 01247
SYL-SyIvania Electric Corp., 100 1st Ave., Waltham, Mass. 02154
WOR-Workman Electronic Products, Inc., Box 3828, Sarasota, Fla. 33578
ZEN-Zenith Sales Co., 5600 W. Jarvis Ave., Chicago, III. 60648

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