Specification 754
November 15, 1976

ENGINEERING INSTRUMENT SPECIFICATION

CP4165 CONTROLLER

FOR INTERNAL USE ONLY
TEKTRONIX, INC.

Specification 754

November 15, 1976

ENGINEERING INSTRUMENT

SPECIFICATION

CP4165

CONTROLLER

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PREFACE

This Engineering Instrument Specification (EIS) is the reference document for company activities concerned with the electrical environmental and physical characteristics of the subject product.

The information in this document is generally intended for use in customer-oriented publications such as the Catalog and Instruction Manual. However, performance characteristics in Section 2 are specifically classified for use in the Catalog and in certain sections of the Instruction Manual (see page 2-1 for further information concerning the tabular data).

A copy of this EIS appears in Product Reference Book with additional copies available from Product Specifications in the Manuals department.

Changes to the EIS may be made only via the Change Request form of which 3 are included at the back of this document (contact Product Specifications for additional copies).

Approved changes are issued in the form of replacement pages slit-punched for easy insertion in the EIS. Changed information appears in italicized print with a cross-hatch symbol in the left margin opposite the latest change. The data of the latest change appears at the bottom left corner of the page.

The following publications contain reference information relative to this document:

Abbreviations and Symbols, Tektronix Part No. 062-1737-00.

Glossary of Technical Terms, Tektronix Standard No. A-101

Manuals Production
April 1, 1976

CHANGE INFORMATION LOG

This page is used as a guide to insure that all change pages have been inserted. When change pages are received, log them on this page, then insert the change pages in their appropriate place. Change numbers (located in upper right corner of Change Notice form) are assigned in sequence. Absence of a number from the sequence indicates a change which has not been inserted.

CHANGE NOTICE NUMBER	EFFECTIVE DATE OF CHANGE	DESCRIPTION

SECTION 1

GENERAL DESCRIPTION

1.1 Introduction

The CP 4165 Controller is a minicomputer suitable for use in many instrumentation systems. The standard CP 4165 is equipped with a 16-bit processor module (the Digital Equipment Corporation LSI-11), 28K words of volatile memory, a combination serial interface - ROM bootstrap program - bus termination (SBT) module, and short-term battery backup. Both CP - and IEE-488-Bus interfaces are optionally available, as is extended battery back-up. With certain bus location constraints, DEC peripherals designed for their LSI-11 systems (eg. PDP-11/03) are compatible with the CP 4165. The controller is housed in a 5 1/4" high rack mountable enclosure. The CP4165 is CSA certified and designed to meet UL 1244 and IEC 348 standards. UL and IEC listings have been applied for.

1.2 Front Panel

The CP 4165 front-panel includes:

1. DC ON/DC OFF switch. Controls DC power to the bus modules. Does not Switch the primary AC line.
2. LINE indicator. When lit, indicates that the DC power source is the line-operated power supply.
3. BATTERY indicator. When lit, indicates that the DC power source is the battery-operated power supply.
4. BUS BUSY indicator. When lit, indicates that data transfer protocol is occurring on the CP 4165 bus (excluding REFRESH cycles).
5. PROCESSOR BUSY indicator- When lit, indicates that the processor module is fetching and executing instructions.
6. RUN/HALT switch. When in the HALT position, forces the processor to stop after executing the current instruction. Resetting the switch to RUN allows the program to be continued, but does not perform the restart operation.
7. RESTART switch. When pressed and released, forces the processor to execute a power-up sequence and then begin execution of the Bootstrap program.

1.3 Bus Modules

The CP 4165 circuit modules are interconnected by a multiwire bus called the Q-bus. Each functionally distinquishable circuit card is called a bus module. Three different card shapes, or form factors, of bus modules are used in the CP4165. Outlines of these different form factor boards are shown in figures 1.1, 1.2, and 1.3. Both the quad- and dual-size boards conform to DEC standards for the PDP-11/03. The short quad form factor does not conform. The standard CP4165 contains one quad form factor board, the LSI-11 processor module. The optional LEEE-488 interface is also a quad module. Dual form factor boards include the three 8K memory modules. Short quad boards include the SBT module and the optional CP bus interface module.

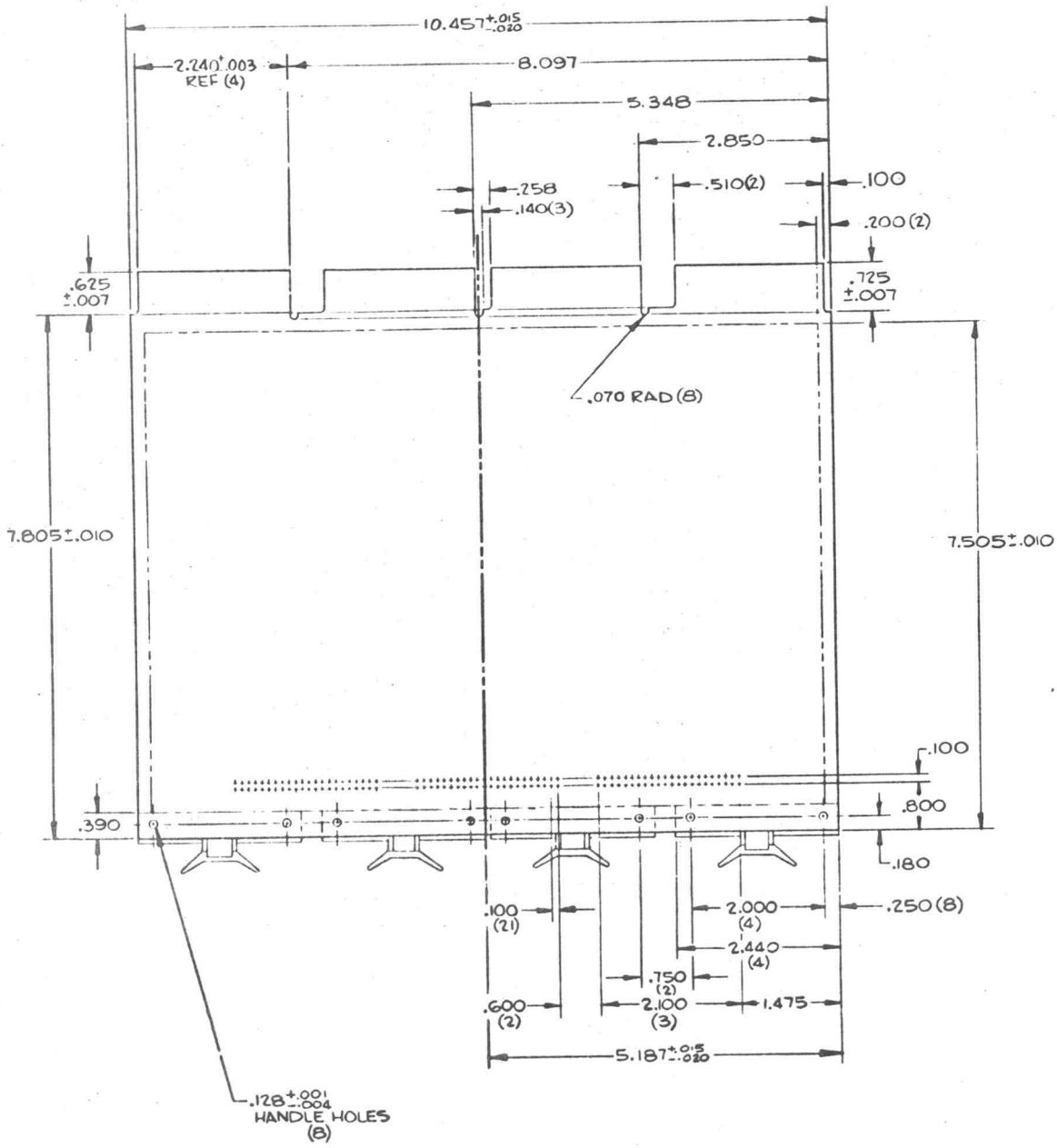


Figure 1.1 Quad-Size Form Factor

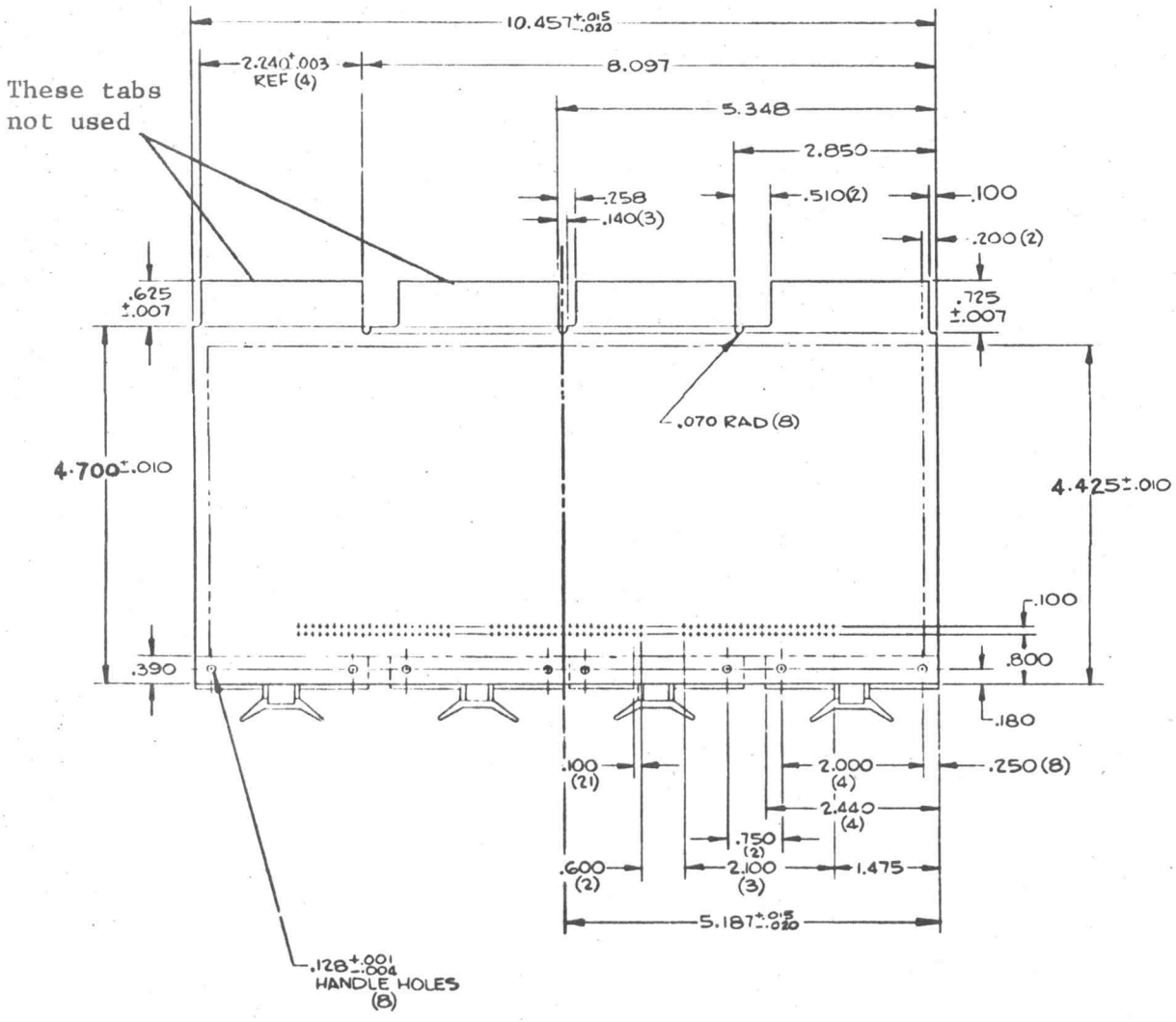


Figure 1.2 Short Quad Form Factor

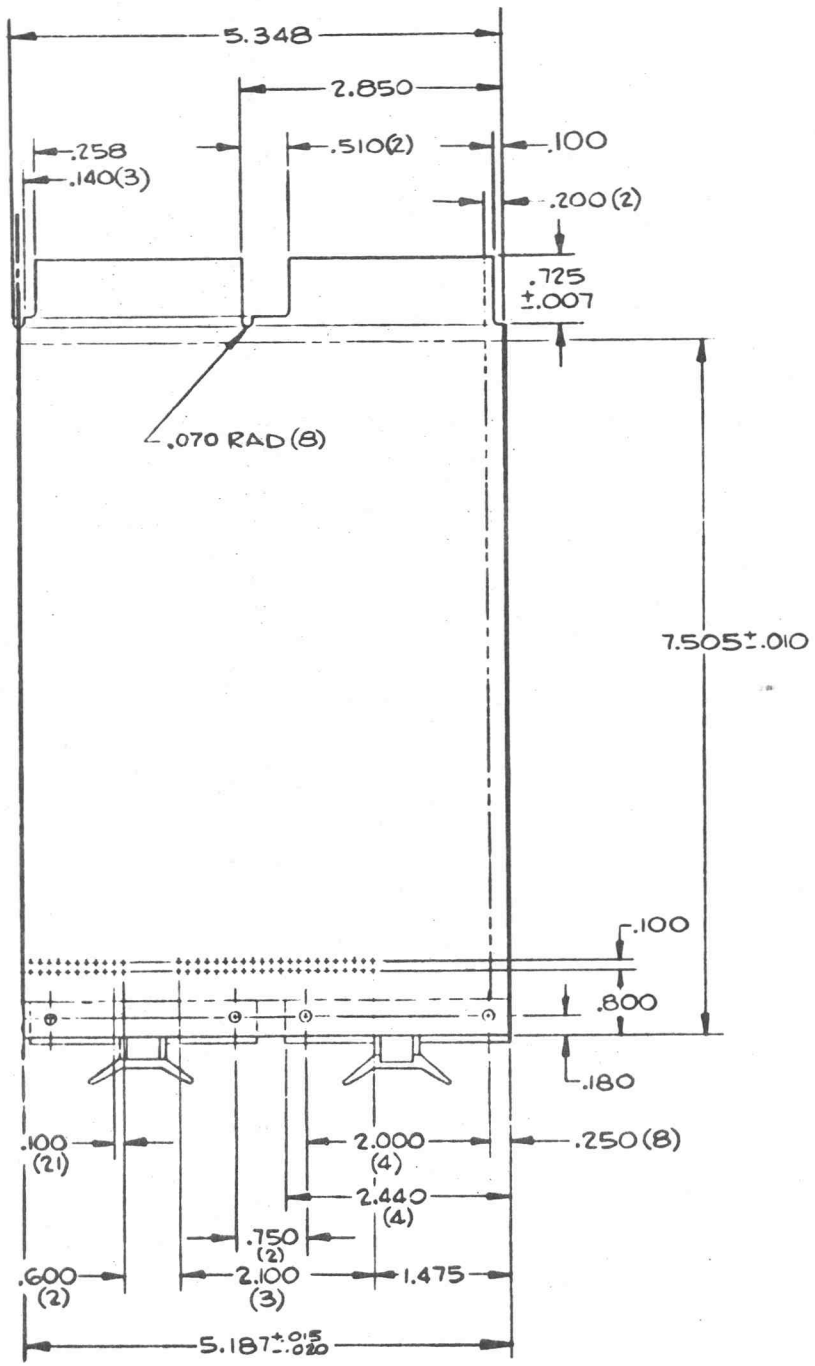


Figure 1.3 Dual Form Factor

1.4 Card Cage Configuration

The CP4165 card cage is divided into two sections. The right-hand (as viewed from the front) section, called the short quad section, accepts only short quad form-factor boards. The left-hand section is called the processor section. The processor section can accept any of the three form factors. There are 15 bus positions available in the CP4165, 10 on the processor side and 5 on the short-quad side. Each dual form-factor module requires two bus positions. Short-quad modules require two bus positions if used on the processor side, but only one if used in the short-quad section. Bus configuration is shown in figures 1.4 and 1.5.

The IEEE-488- and CP-bus interface modules are optional. When installed in the CP4165, they should be located as shown in fiqures 1.4 and 1.5. The RXV-11 (CP114) floppy-disc interface is an available peripheral for the CP4165. If the RXV-11 floppy-disc is added to the CP4165, the interface card should be located as shown. Numbers in parenthesis at each bus position indicate the relative interrupt and DMA priority associated with that position. Highest priority is the lowest-numbered connector pair. Grant Continuity cards are inserted in the left-hand connector of all vacant bus positions, one card per connector pair.

1.5 CP4165 Bus

The CP4165 bus is called the Q-bus. All peripherals, memory, instrument interfaces, and the processor interface to the Q-bus.

Bus Master. Modules on the Q-bus communicate in a master-slave relationship. Only one module can be bus master at any given time. The processor module is normally bus master, but can temporarily pass bus mastership to a requesting DMA interface. The optional IEEE-488 interface has DMA (Direct Memory Access) capability. Passing bus mastership is accomplished by a DMA Request/Grant protocol. A timing diagram describing the protocol is shown in figure 1.6. The signal names shown are those of Q-bus signal lines. Non-DMA-equipped interfaces located between the processor and the requesting DMA device do not participate in the protocol, but do provide daisy-chained signal paths for such signals as DMR, DMG and SACK. If multiple DMA devices are connected, simultaneous DMA requests are prioritized according to bus position. The bus position electrically nearest the processor module (lowest numbered) has highest priority. The bus positions and priorities are shown in figures 1.4 and 1.5. Since memory refresh is normally processor-initiated, DMA interfaces must either relinquish bus mastership at a 600 Hz rate, or provide alternate refresh protocol.

Numbers in parentheses indicate bus position and interrupt/DMA priority: Lowest numbers have highest priority.

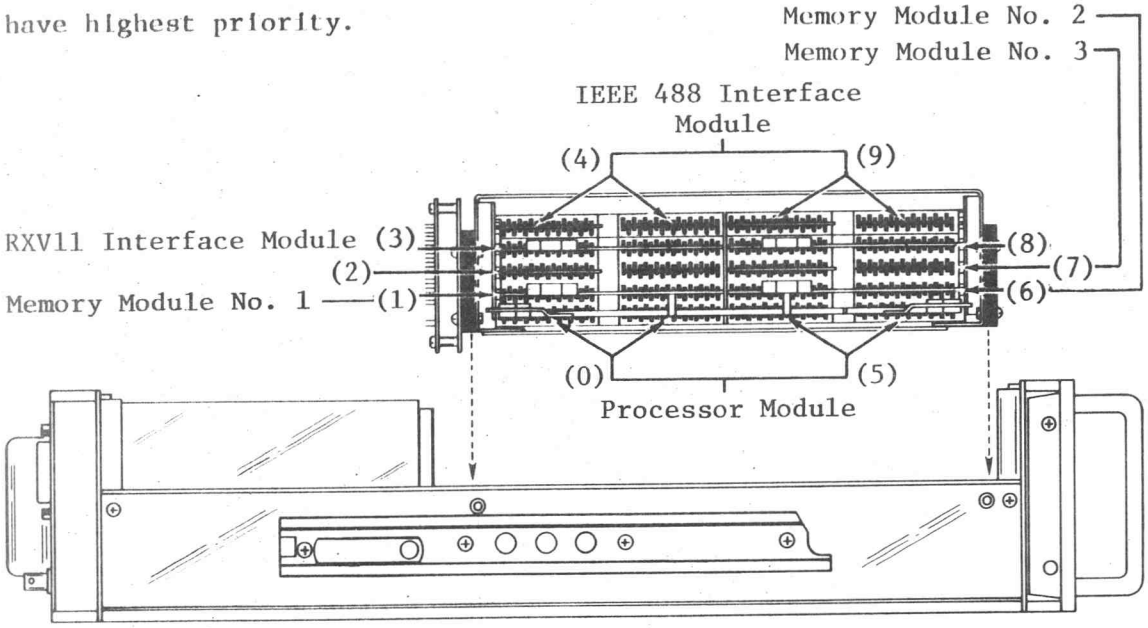


Fig. 1.4. Processor Section Bus Module Configuration.

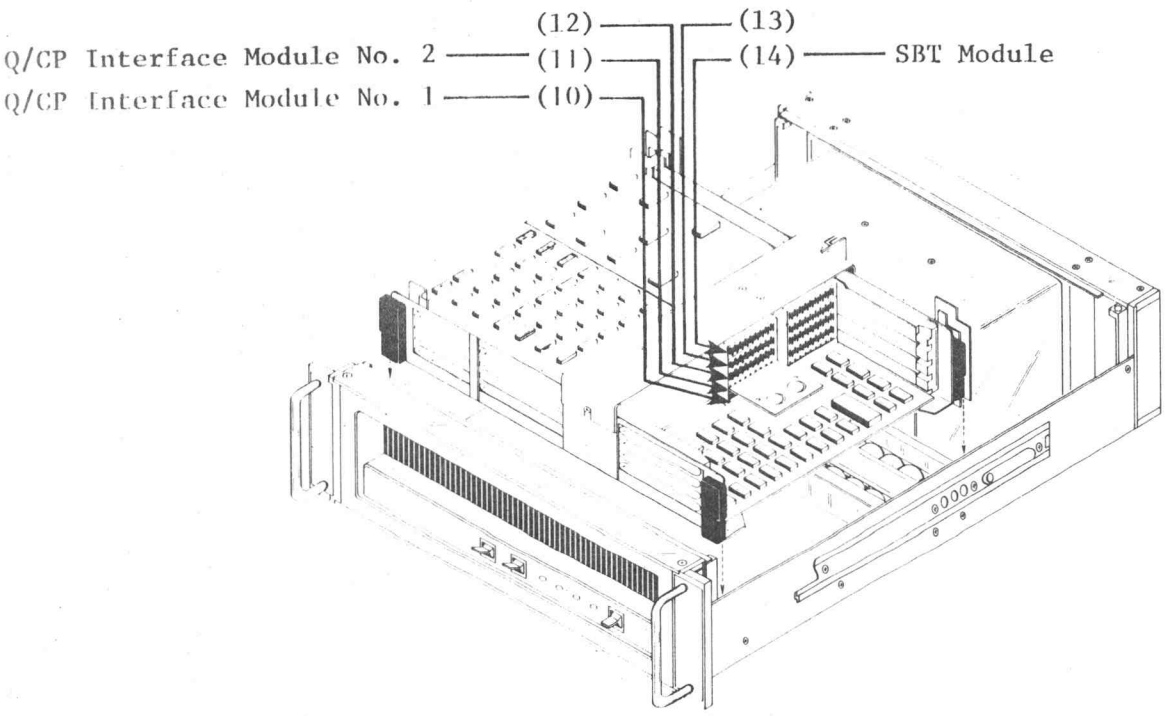
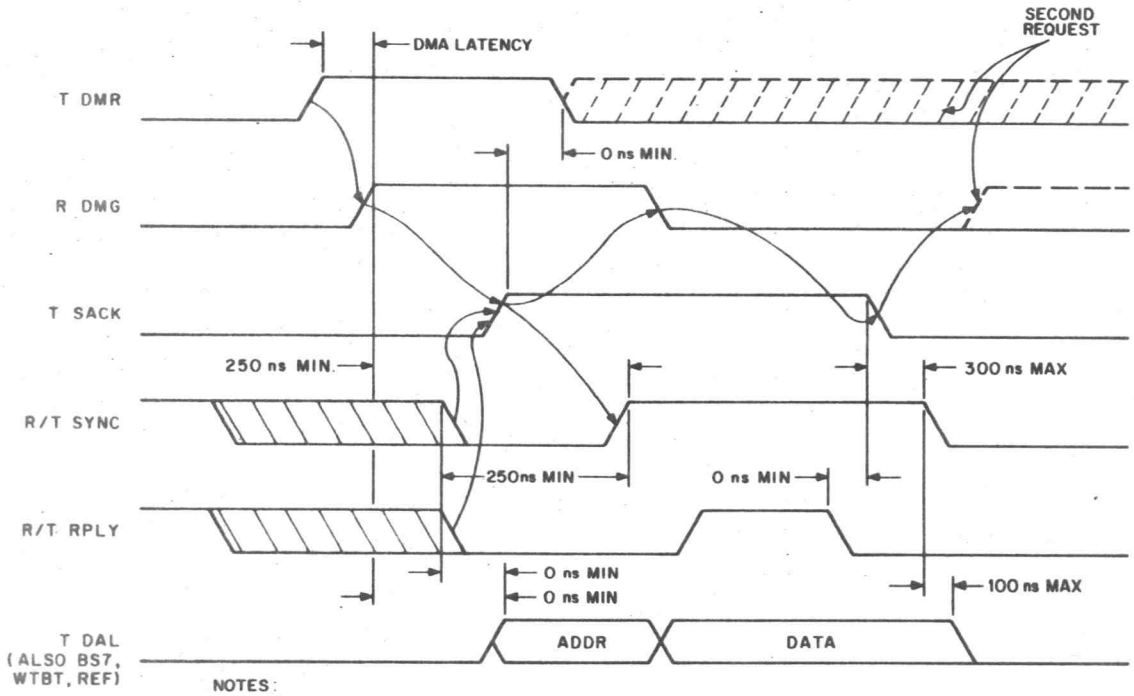


Fig. 1.5. Short Quad Section Bus Module Configuration



NOTES:
1. Timing shown at requesting bus module driver inputs and bus receiver outputs.
2. Signal name prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.

Figure 1.6 DMA Request/Grant Protocol

Data Transfer. Q-bus data transfer protocols are DATI (Read Word), DATIO (Read-Modify-Write Word), DATIOB (Read-Modify-Write Byte), DATO (Write Word), and DATOB (Write Byte). Timing diagrams for these operations are shown in figures 1.7, 1.8, and 1.9. As before, the slave module is addressed by the bus master.

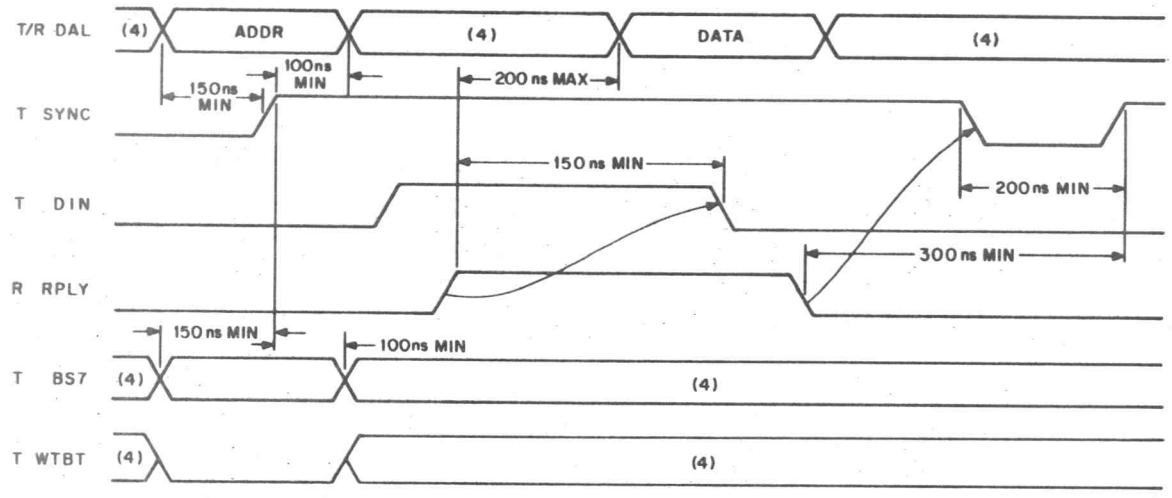
Interrupts. The CP4165 processor provides for interruption of normal processing by recognizing vectored interrupts. The bus module requesting interrupt provides vector address to the processor, allowing an appropriate service routine to be initiated. A timing diagram of the Q-bus interrupt protocol is shown in figure 1.10. Bus modules not capable of interrupt provide daisy-chained continuity paths for IRQ (Interrupt Request) and IAK (Interrupt acknowledge) signals. Multiple interrupts are prioritized according to bus position.

Power Up/Down. Q-bus power up/down protocol timing diagrams are shown in figures 1.11 and 1.12. Three signals are significant during power up/down. BDCOKH high indicates that the DC power to the modules is correct. BPOKH indicates that line power is all right. BINITL low causes the processor and all bus modules to initialize. The processor module asserts BINITL, while BPOKH and BDCOK are controlled by the power supply. The SBT module also controls B DCOK.

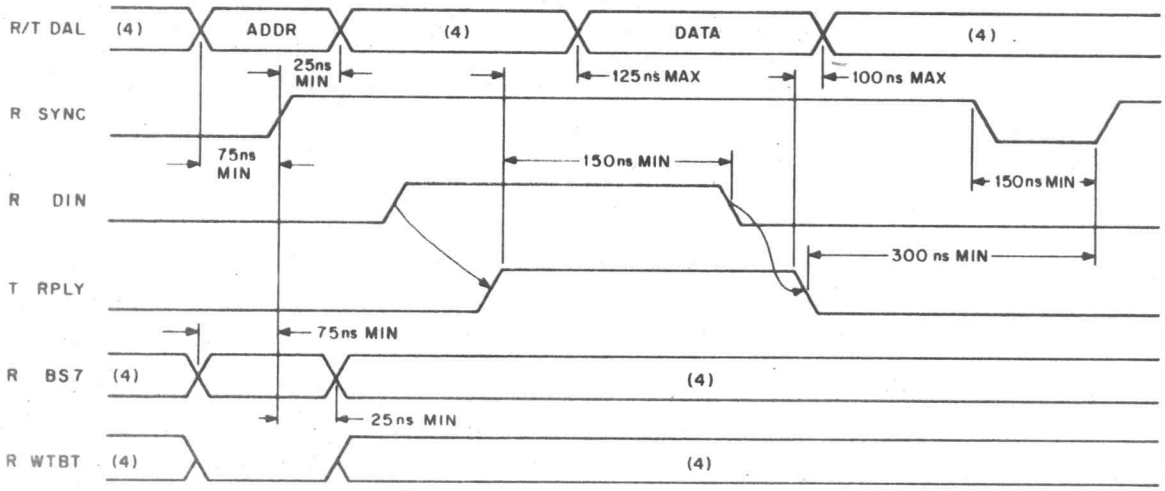
Refresh. The CP4165 memory is dynamic. The processor module refreshes all memory at a 600 Hz rate. A complete refresh cycle requires 64 memory refresh transactions. A memory refresh cycle consists of the DATI data transfer protocol shown in figure 1.7 with the processor asserting the BREFL signal during the address portion. All 64 permutations of the six Q-bus address lines BDAL1-6 are asserted by the processor during a refresh cycle.

Initialize. All Q-bus modules are initialized when the BINITL signal is asserted. Only the processor asserts BINITL.

Halt. Whenever the BHALT L signal is asserted the processor halts and enters the resident ODT (online debugging technique) routine. The front panel RUN/HALT switch controls the BHALT L line.



TIMING AT MASTER BUS MODULE

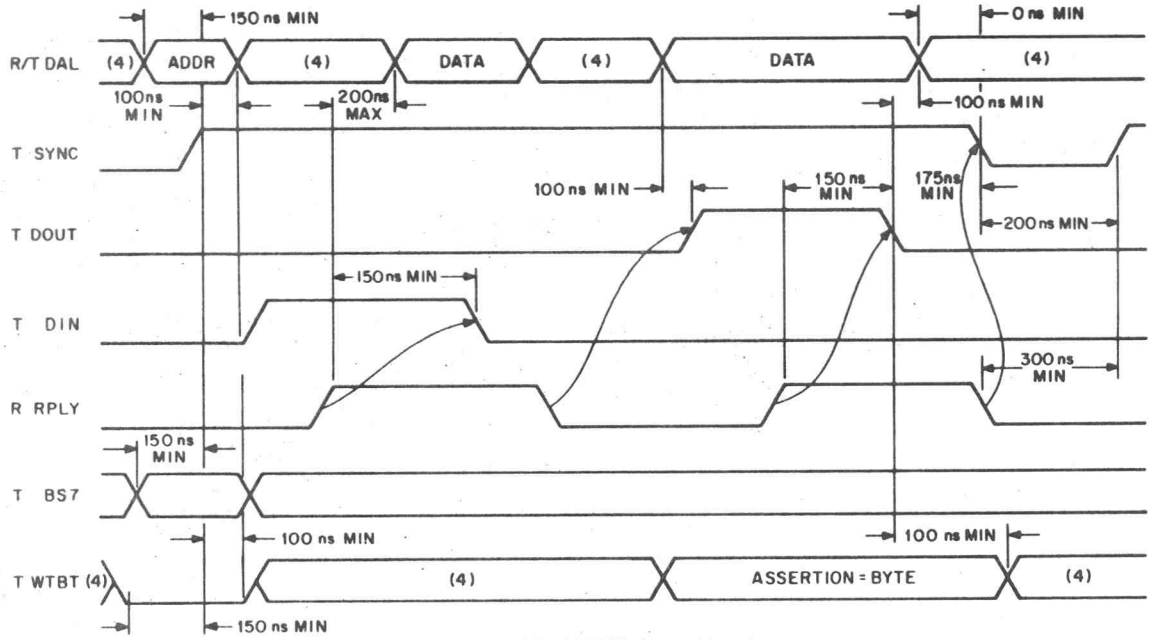


TIMING AT SLAVE BUS MODULE

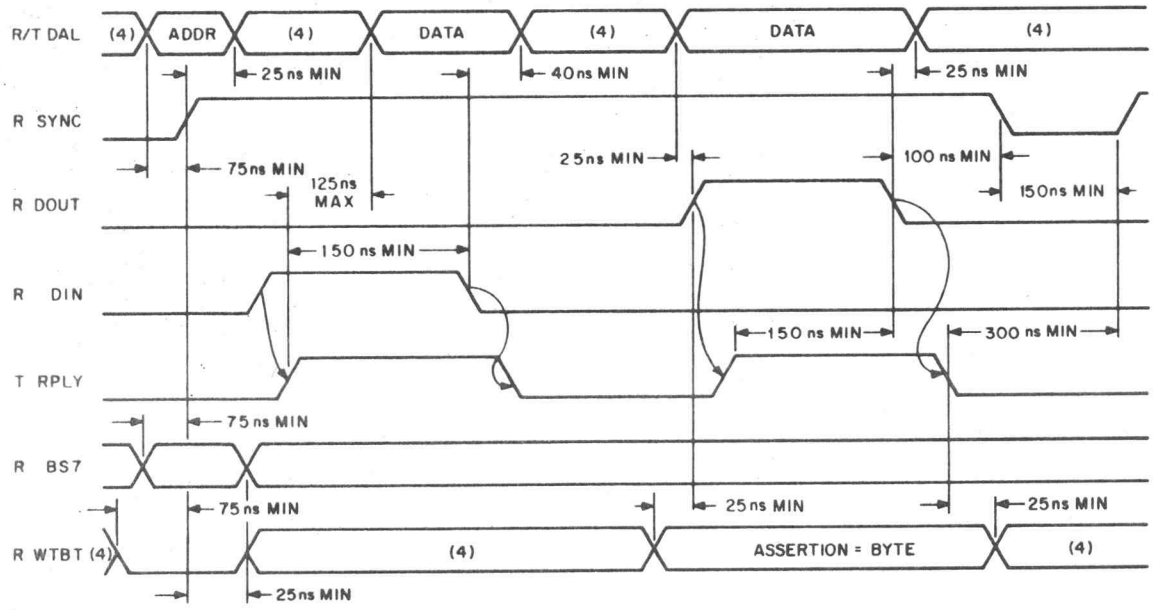
NOTES:

1. Timing shown at Master and Slave Device Bus Driver inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   $\overline{T}$ = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.
4. Don't care condition.

Figure 1.7 DATI Protocol



TIMING AT MASTER BUS MODULE

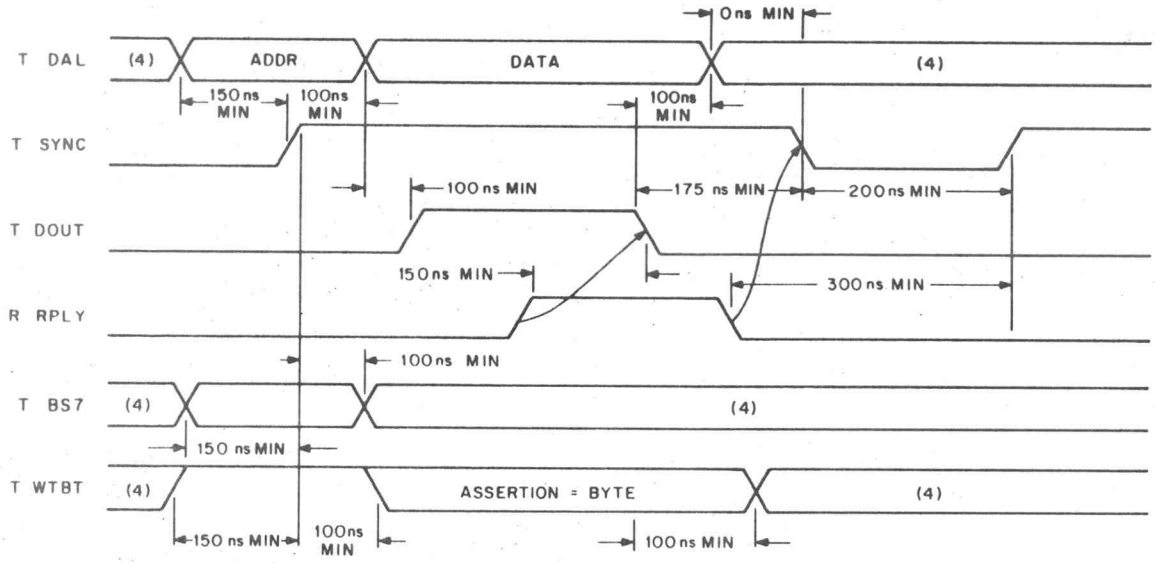


TIMING AT SLAVE BUS MODULE

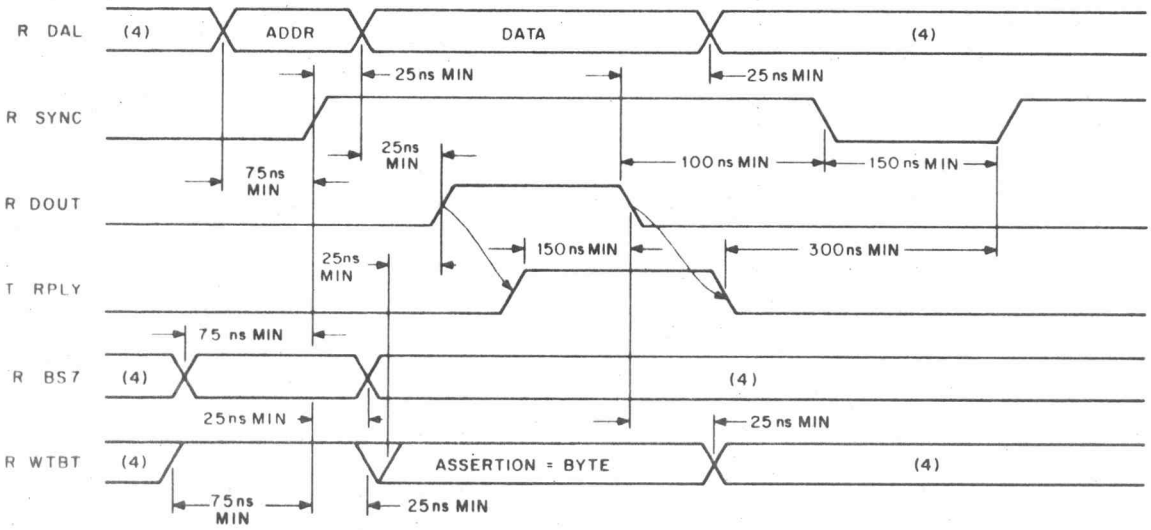
NOTES:

1. Timing shown at Requesting Device Bus Driver Inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.
4. Don't care condition.

Figure 1.8 DAT10 Protocol



TIMING AT MASTER BUS MODULE

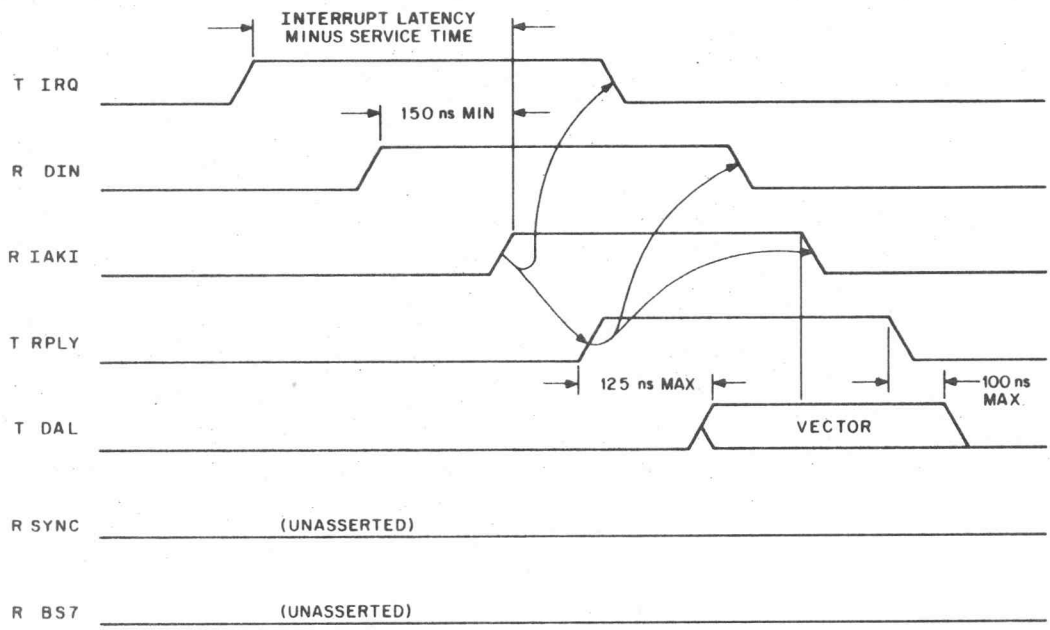


TIMING AT SLAVE BUS MODULE

NOTES

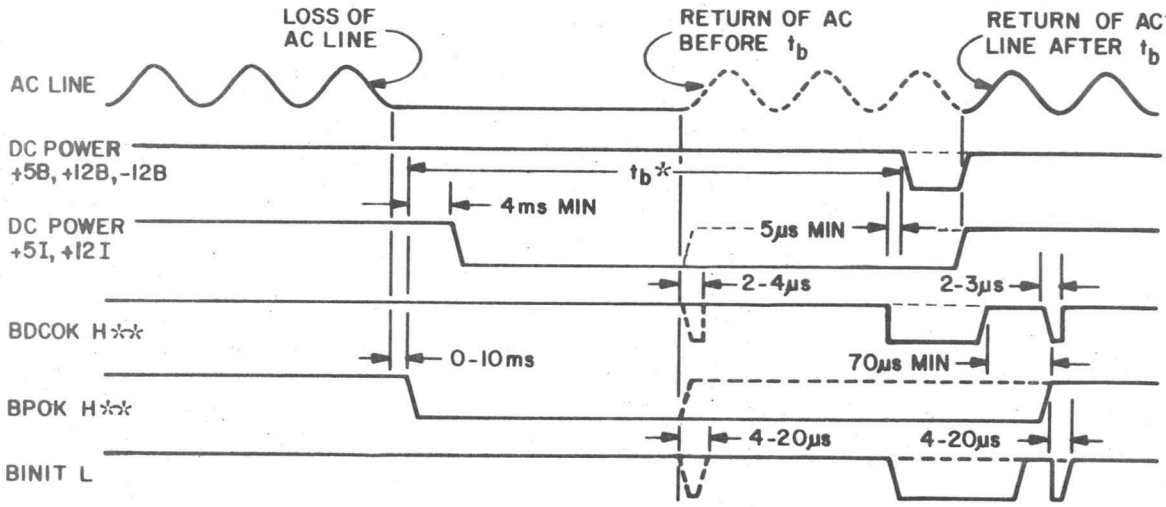
1. Timing shown at Master and Slave Device Bus Driver Inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.
4. Don't care condition.

Figure 1.9 DATO and DATOB Protocol



NOTES:
1. Timing shown at Requesting Bus Module Driver Inputs and Bus Receiver Outputs.
2. Signal Name Prefixes are defined below
   T = Bus Driver Input
   R = Bus Receiver Output
3. Bus Driver Output and Bus Receiver Input signal names include a "B" prefix.

Figure 1.10 Interrupt Transaction Timing



NOTE:

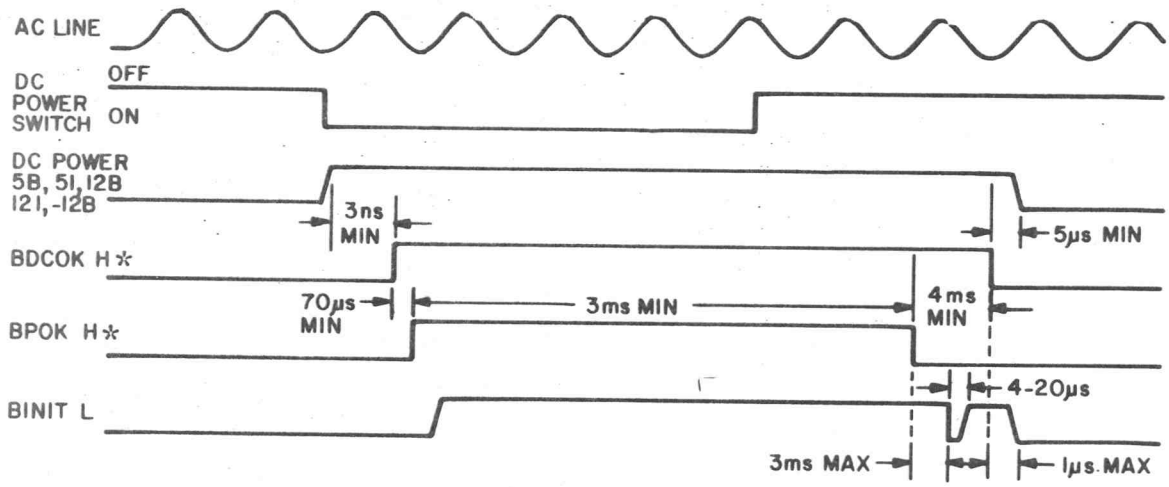
---- Dashed lines show protocol for the condition where ac line power returns before batteries are completely discharged.

*†b Is dependent on battery option and state of battery charge (4ms MIN).

** Asserted by power supply.

Figure 1.11

Power Up/Down Protocol for Loss of AC Line

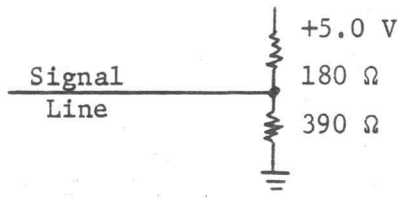


* Asserted by power supply. Also asserted by the SBT Module during restart.

Figure 1.12

Power Up/Down Protocol For Front-panel Power Switch

Electrical Specification - Q-Bus

CHARACTERISTICS	DESCRIPTION
Bus Drivers	(National 8838 or equivalent)
Low State	≤ 0.4 V at 48 ma (sink)
High State	≥ 2.4 V at -5.2 ma (source)
Bus Receivers	(National 8838 or equivalent)
Low State	Input threshold voltage 0.8 V max. Input current -1.6 ma max.
High State	Input threshold voltage 2.0 V min. Input current 40 µa max at 2.4 V.
Bus Impedance	120 Ω nominal.
Bus Termination	As shown: 
Bus Module Stub Length	2 inches max.
Data Rate	833 x 10^3 Data transfers per second.

1.6 Standard Accessories

1) Power Cord
1) 220-V Line Fuse
1) Operator's Manual #070-2271-00
1) Service Manual #070-2278-00
1) Check-out Software

1.7 Optional Accessories

-Card Cage Interconnect Cable	PN-175-5064-00
-Power Supply Extension Cable	PN-067-0809-00
-Quad Extender Card	PN-119-0901-00

1.8 Options

Option 2 - 3 additional battery packs.

Option 31 - IEEE-488 Bus Interface, with
Instruction manual #070-2179-00

Option 32 - CP-Bus Interface, with
Instruction manual #070-2174-00

1.9 Environmental Specifications

CHARACTERISTICS	DESCRIPTION
Temperature	
Non-Operating	-40°C to 60°C.
Operating	5°C to 50°C. Derate at 0.5°C/1000 ft. above 5000 ft.
Altitude (Operating)	50,000 ft. max.
Vibration (Non-Operating)	0.01" P-P 10-55 Hz each major axis. (DELETED)
Shock (Non-Operating)	30 g, 11 ms, half sine, each major axis.
Humidity (Operating)	10% to 95% Non-condensing.

1.10 Physical Specifications

CHARACTERISTICS	DESCRIPTION
Dimensions Height Width Length	See figure 1.13.
Shipping Weight	70 lbs. (82 lbs. with option 2)

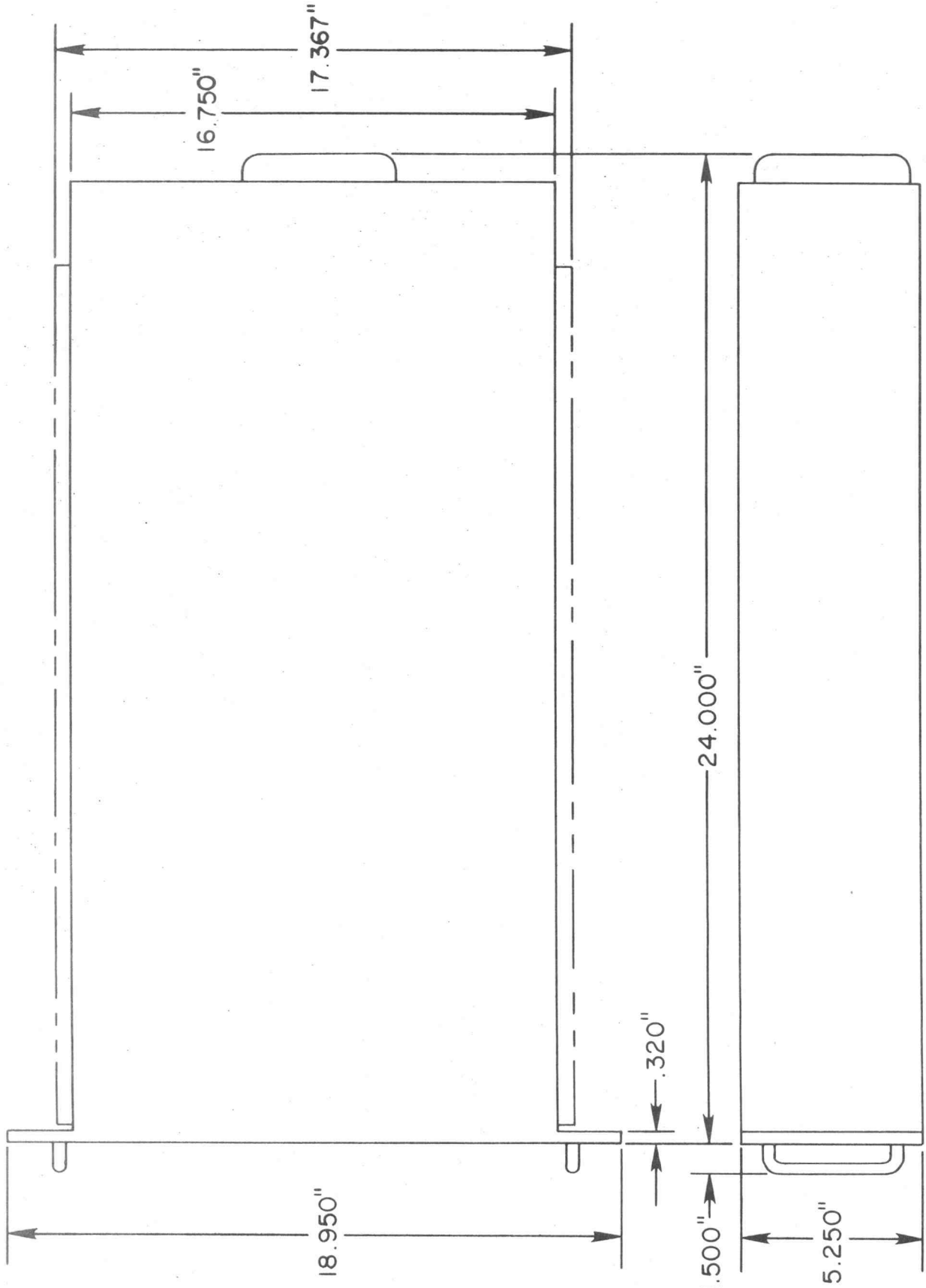


Fig. 1.13 CP4165 Dimensions

NOTES

SECTION 2

POWER SUPPLY

2.1 Introduction

The CP4165 power supply provides operating power to all backplane connectors in the CP4165 mainframe. The supply also provides charge current for backup battery packs and 117-volt 60 Hz AC for two cooling fans. If the primary AC line power fails, the power supply switches to the backup battery pack. During this power-loss condition, the supply continues to provide DC power to selected backplane positions and AC power to one of the fans. The battery-sustained backplane positions are used for the processor module and all memory modules. The standard battery pack can maintain the power supply for about 15 minutes. Option 2 increases the number of battery packs, extending backup operation to 1.5 hours, minimum.

Power Supply

CHARACTERISTICS	DESCRIPTION
Line Voltage Range	Four nominal voltage ranges can be selected by positioning an etched circuit board in the rear-panel fuse assembly. The nominal voltages and the acceptable range for each are listed below:
Line Frequency Range	48-440 Hz.
Power Consumption	350 watts max @ 115 V AC 4 amperes surge max.
Short-Circuit Protection	Each supply is current limited to 1.5 times normal rating.
Over-voltage Protection	SCR (Crowbar) protected as follows: +5B and +5I limited to +6.3 V ± 10%. +12 B and +12 I limited to +15.7 V ± 10%. -12 B limited to -15.7 V ± 10%.

Nominal Setting	Range
100 V	90-110 V RMS
120 V	108-132 V RMS
220 V	198-242 V RMS
240 V	216-250 V RMS

Power Supply (cont.)

CHARACTERISTICS	DESCRIPTION
Output Voltages "I" supplies interrupted by loss of primary AC line. "B" supplies maintained by battery backup during line power loss.	<u>Supply</u> — <u>Output Voltage</u> +5I — +5 V ± 2% +5B — +5 V ± 2% +12I — +12 V ± 3% +12B — +12 V ± 3% -12B — -12 V ± 3%
Output Currents and Ripple	<u>Supply</u> — <u>Output Current</u> — <u>Ripple</u> +5I — 1-15.0 Amperes — 50 mV p-p +5B — 1-8.0 Amperes — 50 mV p-p +12I — 0.2-2.0 Amperes — 150 mV p-p +12B — 0.5-2.0 Amperes — 150 mV p-p -12B — 0-0.2 Amperes — 100 mV p-p
Ripple and Noise Bandwidth	1 MHz.
Output Regulation ($\Delta I/\Delta T<0.1$ A/μs) Line and Load	+5I, +5B: 1.0% max all other supplies: 0.5% max.
Load Interaction	1% max.
Stability	0.2%/1000 hrs. maximum drift, all supplies.

Power Supply (cont.)

CHARACTERISTICS	DESCRIPTION
Line Protection	
100/120 V Line	4 A, 250 V fast-blow fuse.
220/240 V Line	2 A, 250 V fast-blow fuse.
Remote Power Enable (rear-panel connector)	Open-collector output asserted low (< 0.4 V) whenever +5I supply is operating.
Sink capability	16 milliamperes max at 0.4 V.
Off voltage (Externally applied)	30 V max.
Battery Backup	Sealed lead-acid batteries provide minimum 15 minutes operation. Option 2 extends battery operation to 1.5 hrs, min.
Battery Terminal Voltage	22 V nominal. 17 V minimum.
Battery Charger	
Output Voltage	25.7 V $\pm$ 2% @ 25°C.
Temp Coefficient	-30 mV/°C.
Line Time Clock	Q-bus compatible signal with a frequency equal to the primary AC line frequency.

Power Supply (cont.)

CHARACTERISTICS	DESCRIPTION
Efficiency	65% overall minimum.
Cooling (two fans)	Each fan rated @ 33 CFM at 0.1 inch water back pressure. Both fans run during line operation; one during battery operation.
Power up/Power down Protocols	Provides two Q-bus compatible signals (BDCOK L and BPOK L) to initiate the power up/down protocols illustrated in figures 1.11 and 1.12.

NOTES

SECTION 3

PROCESSOR MODULE

3.1 Introduction

The CP4165 processor module is an LSI-11 board purchased from Digital Equipment Corporation. The module consists of a 5-chip processor, interface and driver circuitry for the Q-bus, 4K x 16 bits of dynamic RAM and other support hardware mounted on a Quad form factor circuit card. Several etch revisions of the LSI-11 module exist. The current CP4165 uses revisions D and E.

Since the CP4165 processor module is a purchased item, all support literature provided by DEC for the LSI-11 module is directly applicable. This includes instruction set, programming considerations, timing, and Q-bus protocols. Some of the text and illustrations in this document are reprinted courtesy of Digital Equipment Corp.

3.2 Strap Configuration

The processor module has several strap options. Etch revision E boards have eleven strap options, while the revision D boards have only six. The straps must be installed or removed as shown in Tables 3.1 and 3.2 for use in the CP4165. Figures 3.1 and 3.2 detail the jumper locations for the revision E and the revision D boards respectively.

TABLE 3.1

JUMPER CONFIGURATION

Revision E

Jumper Number	Remove/Install	Description
W1	Remove	Locates CPU resident memory in bank 0.
W2	Install	
W3	Install	Disables Event-line interrupt.
W4	Remove	Enables CPU-initialed memory refresh.
W5	Remove	Causes CPU to power-up via the bootstrap program (location 173000_8).
W6	Install	
W7	Install	Selects proper memory bias voltages.
W8	Install	
W9	Remove	Enables CPU resident memory address response.
W10	Remove	Enables CPU resident memory refresh response.
W11	Install	Enables CPU resident memory.

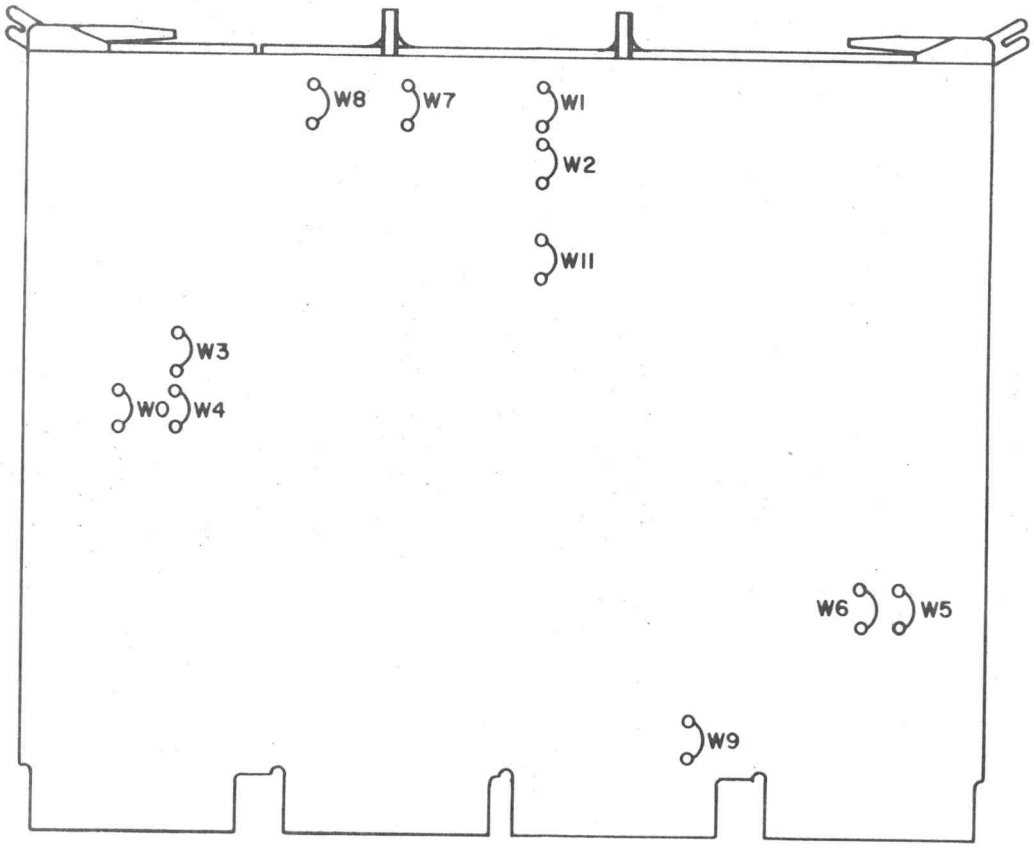


Figure 3.1 Revision E Jumper Locations

TABLE 3.2

JUMPER CONFIGURATION

Revision D

Jumper Number	Remove/Install	Description
W1	Remove	Locates CPU resident memory in bank 0.
W2	Install	
W3	Install	Disables Event-line interrupt.
W4	Remove	Enables CPU-initiated memory refresh.
W5	Remove	Causes CPU to power-up via the bootstrap program (location 173000_8)
W6	Install	

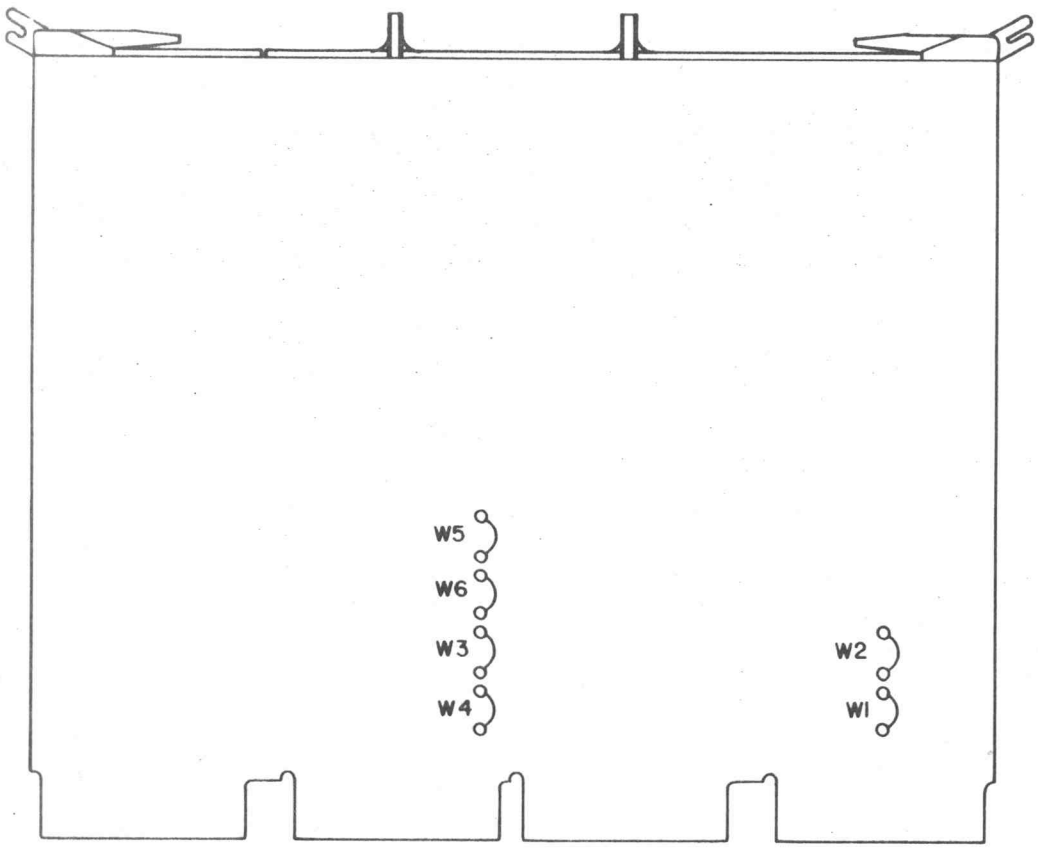


Figure 3.2 Revision D Jumper Locations

3.3 Protocols and Trap Vectors

Protocols. The CP4165 bus supports master-slave data transfers. The processor module is usually the bus master, transferring data to or from slave devices such as memory or peripheral interfaces. Some types of interfaces (such as the optional IEEE-488 interface) are capable of direct memory access (DMA) transfers. When such a device requests bus mastership, the processor module passes control via the protocol described in section 1.5. Only the processor and a DMA-equipped device can gain bus mastership. Since memory refresh is processor-initiated, DMA devices must either relinquish bus mastership at a 600 Hz rate or provide other means of refresh.

When the processor is executing instructions that do not require use of the bus, it is not bus master. It operates as a processor or arbitrator only. Table 3.3 lists the role played by the processor for various types of operations.

TABLE 3.3

PROCESSOR ROLES

Protocol	Processor Role
DATI	Bus Master
DATO	Bus Master
DATOB	Bus Master
DATIOB	Bus Master
Refresh	Bus Master
DMA Request/Grant	Arbitrator
Interrupt Request/Acknowledge	Arbitrator
Power up/down	Processor
Initialize	Processor

Trap Vectors. A trap vector is a consecutive pair of dedicated memory locations that contain a new processor status word (PSW) and a new program counter (PC) value. Some program instructions and many error conditions cause the processor to obtain new PSW and PC values from specific trap vectors. The procedure is called trapping. For example, if the processor references a peripheral device with an address and the addressed device fails to respond within a preset length of time, a bus time-out error occurs. When the processor detects the time-out condition, it immediately traps to memory location 004_8 and loads a new PC value. A new PSW is loaded from the next consecutive memory location, 006. Depending upon the software being used, the new PC and PSW usually cause the processor to begin executing a service routine to handle the error. Table 3-4 lists the dedicated trap vectors for various instructions and error conditions for the CP4165.

TABLE 3-4

TRAP VECTORS

Condition	PC Location (octal)	PSW Location (octal)
CPU Reserved Location	000	002
Bus time-out and other errors	004	006
Illegal and/or reserved instruction	010	012
BPT (Breakpoint) instruction	014	016
IOT instruction	020	022
Power fail	024	026
EMT instruction	030	032
TRAP instruction	034	036
FIS instruction	244	246
Event Line	100	102

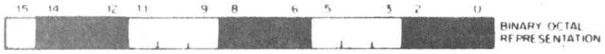
3.4 On-Board Memory

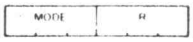
The CP4165 processor module includes a resident 4096 word x 16-bit memory. The memory responds as a slave to all memory-reference protocols (DATI, DATO, etc.) and responds to refresh with BREPLY L. The address range of the resident memory is 0000_8 to 17777_8.

The memory is dynamic, and must be refreshed at a 600 hz rate. All 64 combinations of the six address bits BDAL 1 - BDAL 6 must be exercised for refresh. Refresh protocol is automatically executed by the CP4165 processor module.

3.5 CP4165 Instructions, Execution times, and ODT (Online Debugging Technique) Commands.

WORD FORMAT





Mode	Name	Symbolic	Description
0	register	R	(R) is operand [ex. R2=%2]
1	register deferred	(R)	(R) is address
2	auto-increment	(R)+	(R) is adrs; (R) + (1 or 2)
3	auto-incr deferred	@(R)+	(R) is adrs of adrs; (R) + 2
4	auto-decrement	-(R)	(R) − (1 or 2); is adrs
5	auto-decr deferred	@-(R)	(R) − 2; (R) is adrs of adrs
6	index	X(R)	(R) + X is adrs
7	index deferred	@X(R)	(R) + X is adrs of adrs

PROGRAM COUNTER ADDRESSING Reg = 7

2	immediate	#n	operand n follows instr
3	absolute	@#A	address A follows instr
6	relative	A	instr adrs + 4 + X is adrs
7	relative deferred	@A	instr adrs + 4 + X is adrs of adrs

LEGEND

Op Codes

■	= 0 for word/1 for byte
SS	= source field (6 bits)
DD	= destination field (6 bits)
R	= gen register (3 bits), 0 to 7
XXX	= offset (8 bits), +127 to −128
N	= number (3 bits)
NN	= number (6 bits)

Operations

( )	= contents of
s	= contents of source
d	= contents of destination
r	= contents of register
←	= becomes
X	= relative address
%	= register definition

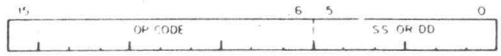
Boolean

∧	= AND
∨	= inclusive OR
⊻	= exclusive OR
~	= NOT

Condition Codes

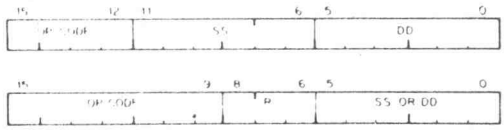
*	= conditionally set/cleared
–	= not affected
0	= cleared
1	= set

SINGLE OPERAND: OPR dst



Mnemonic	Op Code	Instruction	dst Result	N	Z	V	C
General							
CLR(B)	■ 050DD	clear	0	0	1	0	0
COM(B)	■ 051DD	complement (1's)	~ d	*	*	0	1
INC(B)	■ 052DD	increment	d + 1	*	*	*	–
DEC(B)	■ 053DD	decrement	d − 1	*	*	*	–
NEG(B)	■ 054DD	negate (2's compl)	−d	*	*	*	*
TST(B)	■ 057DD	test	d	*	*	0	0
Rotate & Shift							
ROR(B)	■ 060DD	rotate right	→ C, d	*	*	*	*
ROL(B)	■ 061DD	rotate left	C, d ←	*	*	*	*
ASR(B)	■ 062DD	arith shift right	d/2	*	*	*	*
ASL(B)	■ 063DD	arith shift left	2d	*	*	*	*
SWAB	0003DD	swap bytes		*	*	0	0
Multiple Precision							
ADC(B)	■ 055DD	add carry	d + C	*	*	*	*
SBC(B)	■ 056DD	subtract carry	d − C	*	*	*	*
SXT	0067DD	sign extend	0 or −1	–	*	0	–
Processor Status (PS) Operators							
MFPS	1067DD	move byte from PS	d ← PS	*	*	0	–
MTPS	1064SS	move byte to PS	PS ← s	*	*	*	*

DOUBLE OPERAND: OPR src, dst OPR src, R or OPR R, dst



Mnemonic	Op Code	Instruction	Operation	N	Z	V	C
General							
MOV(B)	■ 1SSDD	move	d ← s	*	*	0	–
CMP(B)	■ 2SSDD	compare	s − d	*	*	*	*
ADD	06SSDD	add	d ← s + d	*	*	*	*
SUB	16SSDD	subtract	d ← d − s	*	*	*	*
Logical							
BIT(B)	■ 3SSDD	bit test (AND)	s ∧ d	*	*	0	–
BIC(B)	■ 4SSDD	bit clear	d ← (~s) ∧ d	*	*	0	–
BIS(B)	■ 5SSDD	bit set (OR)	d ← s ∨ d	*	*	0	–
XOR	074RDD	exclusive OR	d ← r ⊻ d	*	*	0	–

EIS

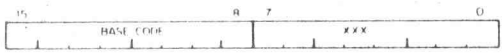
MUL	070RSS	multiply	r ← r x s	•	•	0	•
DIV	071RSS	divide	r ← r/s	•	•	•	•
ASH	072RSS	shift arithmetically		•	•	•	•
ASHC	073RSS	arith shift combined		•	•	•	•

FIS

FADD	07500R	floating add	•	•	0	0
FSUB	07501R	floating subtract	•	•	0	0
FMUL	07502R	floating multiply	•	•	0	0
FDIV	07503R	floating divide	•	•	0	0

BRANCH: B location

If condition is satisfied:
Branch to location,
New PC ← Updated PC + (2 x offset)
adrs of br instr + 2



Op Code = Base Code + XXX

Mnemonic	Base Code	Instruction	Branch Condition	
Branches				
BR	000400	branch (unconditional)	(always)	
BNE	001000	br if not equal (to 0)	≠ 0	Z = 0
BEQ	001400	br if equal (to 0)	= 0	Z = 1
BPL	100000	branch if plus	+	N = 0
BMI	100400	branch if minus	−	N = 1
BVC	102000	br if overflow is clear		V = 0
BVS	102400	br if overflow is set		V = 1
BCC	103000	br if carry is clear		C = 0
BCS	103400	br if carry is set		C = 1
Signed Conditional Branches				
BGE	002000	br if greater or equal (to 0)	≥0	N ⊻ V = 0
BLT	002400	br if less than (0)	<0	N ⊻ V = 1
BGT	003000	br if greater than (0)	>0	Z v (N ⊻ V) = 0
BLE	003400	br if less or equal (to 0)	≤0	Z v (N ⊻ V) = 1
Unsigned Conditional Branches				
BHI	101000	branch if higher	>	C v Z = 0
BLOS	101400	branch if lower or same	≤	C v Z = 1
BHIS	103000	branch if higher or same	≥	C = 0
BLO	103400	branch if lower	<	C = 1

JUMP & SUBROUTINE

Mnemonic	Op Code	Instruction	Notes
JMP	0001DD	jump	PC ← dst
JSR	004RDD	jump to subroutine	use same R
RTS	00020R	return from subroutine	use same R
MARK	0064NN	mark	aid in subr return
SOB	077RNN	subtract 1 & br (if ≠ 0)	(R) − 1, then if (R) ≠ 0: PC ← Updated PC − (2 x NN)

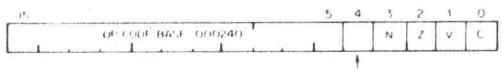
TRAP & INTERRUPT:

Mnemonic	Op Code	Instruction	Notes
EMT	104000 to 104377	emulator trap (not for general use)	PC at 30, PS at 32
TRAP	104400 to 104777	trap	PC at 34, PS at 36
BPT	000003	breakpoint trap	PC at 14, PS at 16
IOT	000004	input/output trap	PC at 20, PS at 22
RTI	000002	return from interrupt	
RTT	000006	return from interrupt	inhibit T bit trap

MISCELLANEOUS:

Mnemonic	Op Code	Instruction
HALT	000000	halt
WAIT	000001	wait for interrupt
RESET	000005	reset external bus
NOP	000240	(no operation)

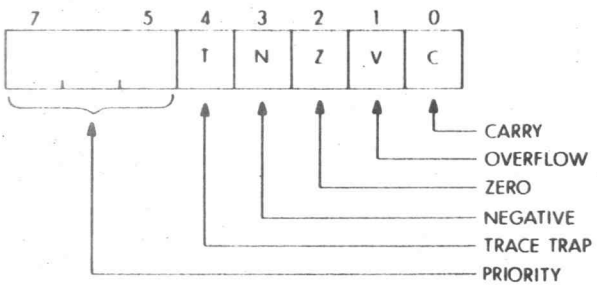
CONDITION CODE OPERATORS:



0 = CLEAR SELECTED COND. CODE BITS
1 = SET SELECTED COND. CODE BITS

Mnemonic	Op Code	Instruction	N	Z	V	C
CLC	000241	clear C	–	–	–	0
CLV	000242	clear V	–	–	0	–
CLZ	000244	clear Z	–	0	–	–
CLN	000250	clear N	0	–	–	–
CCC	000257	clear all cc bits	0	0	0	0
SEC	000261	set C	–	–	–	1
SEV	000262	set V	–	–	1	–
SEZ	000264	set Z	–	1	–	–
SEN	000270	set N	1	–	–	–
SCC	000277	set all cc bits	1	1	1	1

PROCESSOR STATUS WORD



POWERS OF 2

n	2^n	n	2^n
0	1	10	1,024
1	2	11	2,048
2	4	12	4,096
3	8	13	8,192
4	16	14	16,384
5	32	15	32,768
6	64	16	65,536
7	128	17	131,072
8	256	18	262,144
9	512	19	524,288

ABSOLUTE LOADER

Starting Address — 500
Memory Size
4K 017
8K 037
12K 057
16K 077
20K 117
24K 137
28K 157

BOOTSTRAP LOADER

Address	Contents	Address	Contents
— 744	016 701	— 764	000 002
— 746	000 026	— 766	— 400
— 750	012 702	— 770	005 267
— 752	000 352	— 772	177 756
— 754	005 211	— 774	000 765
— 756	105 711	— 776	177 560 (TTY)
— 760	100 376		
— 762	116 162		

NUMERICAL OP CODE LIST

OP Code	Mnemonic
00 00 00	HALT
00 00 01	WAIT
00 00 02	RTI
00 00 03	BPT
00 00 04	IOT
00 00 05	RESET
00 00 06	RTT
00 00 07 – 00 00 77	(unused)
00 01 DD	JMP
00 02 0R	RTS
00 02 10 – 00 02 27	(reserved)
00 02 40	NOP
00 02 41 – 00 02 77	cond codes
00 03 DD	SWAB
00 04 XXX	BR
00 10 XXX	BNE
00 14 XXX	BEQ
00 20 XXX	BGE
00 24 XXX	BLT
00 30 XXX	BGT
00 34 XXX	BLE
00 4R DD	JSR
00 50 DD	CLR
00 51 DD	COM
00 52 DD	INC
00 53 DD	DEC
00 54 DD	NEG
00 55 DD	ADC
00 56 DD	SBC
00 57 DD	TST
00 60 DD	ROR
00 61 DD	ROL
00 62 DD	ASR
00 63 DD	ASL
00 64 NN	MARK
00 67 DD	SXT
00 70 00 – 00 77 77	(unused)
01 SS DD	MOV
02 SS DD	CMP
03 SS DD	BIT
04 SS DD	BIC
05 SS DD	BIS
06 SS DD	ADD
07 0R SS	MUL
07 1R SS	DIV
07 2R SS	ASH
07 3R SS	ASHC
07 4R DD	XOR
07 50 0R	FADD
07 50 1R	FSUB
07 50 2R	FMUL
07 50 3R	FDIV
07 50 40 – 07 67 77	(unused)
07 7R NN	SOB
10 00 XXX	BPL
10 04 XXX	BMI
10 10 XXX	BHI
10 14 XXX	BLOS
10 20 XXX	BVC
10 24 XXX	BVS
10 30 XXX	BCC, BHIS
10 34 XXX	BCS, BLO
10 40 00 – 10 43 77	EMT
10 44 00 – 10 47 77	TRAP
10 50 DD	CLRB
10 51 DD	COMB
10 52 DD	INCB
10 53 DD	DECB
10 54 DD	NEGB
10 55 DD	ADCB
10 56 DD	SBCB
10 57 DD	TSTB
10 60 DD	RORB
10 61 DD	ROLB
10 62 DD	ASRB
10 63 DD	ASLB
10 64 SS	MTPS
10 67 DD	MFPS
11 SS DD	MOVB
12 SS DD	CMPB
13 SS DD	BITB
14 SS DD	BICB
15 SS DD	BISB
16 SS DD	SUB

TRAP VECTORS

000	(reserved)	024	Power Fail
004	Time Out & other errors	030	EMT instruction
010	illegal & reserved instr	034	TRAP instruction
014	BPT instruction	244	FIS (optional)
020	IOT instruction		

Instruction Execution Times

The execution time for an instruction depends on the instruction itself, the modes of addressing used, and the type of memory referenced. In most cases the instruction execution time is the sum of a Basic Time, a Source Address (SRC) Time, and a Destination Address (DST) Time.

INSTR TIME = Basic Time + DST Time

(BASIC Time = Fetch Time + Execute Time)

Some of the instructions require only some of these times. All timing information is in microseconds, unless otherwise noted. Times are typical and can vary $\pm$ 20%.

SOURCE (SRC) AND DESTINATION (DST) TIME

MODE	SRC TIME (Word)	SRC TIME (Byte)	DST TIME (Word)	DST TIME (Byte)
0	0	0	0	0
1	1.40 µsec	1.05 µsec	2.10 µsec	1.75 µsec
2	1.40	1.05	2.10	1.75
3	3.50	3.15	4.20	4.20
4	2.10	1.75	2.80	2.45
5	4.20	3.85	4.90	4.90
6	4.20	3.85	4.90	4.55
7	6.30	5.95	6.65	7.00

NOTE FOR MODE 2 and MODE 4. If R6 or R7 used for Byte operation, add 0.35 µsec to SRC time and 0.70 µsec to DST time.

INSTRUCTION TIME

	Data Mode	
Instruction	DM0	DM1-7
DOPS		
MOV	3.50 µsec	2.45 µsec
ADD, XOR, SUB BIC, BIS	3.50	4.20
CMP, BIT	3.50	3.15
MOVB	3.85	3.85
BICB, BISB	3.85	3.85
CMPB, BITB	3.15	2.80
SOPS		
CLR	3.85 µsec	4.20 µsec
INC, ADC, DEC, SBC	4.20	4.90
COM, NEG	4.20	4.55
ROL, ASL	3.85	4.55
TST	4.20	3.85
ROR	5.25	5.95
ASR	5.60	7.00
CLRB, COMB, NEGB	3.85	4.20
ROL, ASLB	3.85	4.20
INCB, DECB, SBCB, ADCB	3.85	4.55
TSTB	3.85	3.50
RORB	4.20	4.90
ASRB	4.55	5.95
SWAB	4.20	3.85
SXT	5.95	6.65
MFPS (106700)	4.90	6.65
MTRS (106486)	7.00	7.00*

* For MTPS use Byte DST time not SRC
Add 0.35 µsec to instr. time if Bit 7 of effective OPR = 1

JMP/JSR MODE	DST TIME
1	0.70 μsec
2	1.40
3	2.10
4	1.40
5	2.80
6	2.80
7	4.90

INSTRUCTION	TIMES
JMP	3.50 μsec
JSR (PC=LINK)	5.25
JSR (PC≠LINK)	6.40
ALL BRANCHES	3.50 (CONDITION MET OR NOT MET)
SOB (BRANCH)	4.90
SOB (NO BRANCH)	4.20
SET CC	3.50
CLEAR CC	3.50
NOP	3.50
ATS	5.25
MARK	11.55
RTI	10.50*
RTT	10.50*+
TRAP EMT	16.80*
IOT RPT	18.55*
WAIT	6.30
HALT	5.60
RESET	5.95 + 10.0 μsec for INIT + μsec
MAINT INST. (00021R)	20.30
RSRVD INST. (00022X)	5.95 (TO GET TO ADDRESS 3000)

* IF NEW PS HAS BIT 4 or BIT 7 SET ADD 0.35 μsec FOR EACH
\+ IF NEW PS HAS BIT 4 (T BIT) SET ADD 2.10 μsec

EXTENDED ARITHMETIC INSTRUCTION TIMES

EIS INSTRUCTION TIMES

MODE	SRC TIME
0	0.35 (time in μsec)
1	2.10
2	2.80
3	3.15
4	2.80
5	3.85
6	3.85
7	5.60

INSTRUCTION	BASIC TIME
MUL	24.0 to 37.0 μsec If both numbers less than 256 in ABS value
	64.0 μsec Worst Case 16 bit multiply
DIV	78.0 μsec Worst Case
ASH (RIGHT)	10.1 + 1.75 per shift
ASH (LEFT)	10.8 + 2.45 per shift
ASHC (RIGHT)	10.1 + 2.80 per shift
ASHC (LEFT)	10.1 + 3.15 per shift

FIS INSTRUCTION TIMES

INST TIME = BASIC TIME + SHIFT TIME FOR BINARY POINTS + SHIFT TIME FOR NORMALIZATION

INSTRUCTION	BASIC TIME
FADD	42.1 μsec
FSUB	42.4

EXPONENT DIFFERENCE	ALIGN BINARY POINTS
0 - 7	2.45 per shift
8 - 15	3.50 + 2.45 per shift over 8
16 - 23	7.00 + 2.45 per shift over 16

EXPONENT DIFFERENCE	NORMALIZATION
0 - 7	2.1 per shift
8 - 15	2.1 + 2.1 per shift over 8
16 - 23	4.2 + 2.1 per shift over 16

INSTRUCTION	BASIC TIME
FMUL	52.2 + 3.85 If either argument has 8 bits of precision
	93.7 Worst Case
FDIV	232 Worst Case
	151 Typical

IV. CP4165 Instruction, Execution Times, and ODT Commands

3. ODT Commands (entered from system terminal)

Format	Description
RETURN	Close opened location and accept next command.
LINE FEED	Close current location; open next sequential location.
↑	Open previous location.
←	Take contents of opened location, index by contents of PC, and open that location.
@	Take contents of opened location as absolute address and open that location.
r/	Open the word at location r.
/	Reopen the last location.
$n/or Rn/	Open general register n (0-7) or S (PS register).
r;G or rG	Go to location r and start program.
nL	Execute bootstrap loader using n as device CSR. Console device address is 177560.
P or P	Proceed with program execution.
RUBOUT	Erases previous numeric character. Response is a backslash (\).

Processor Module

CHARACTERISTICS	DESCRIPTION
Power Consumption	
+12 B	1.6 Amperes max.
+5 B	2.4 Amperes max.
Form Factor	Full Quad (Drawing in section 1.3)

NOTES

SECTION 4

8K Memory Module

4.1 Introduction

The CP4165 8K Memory Module consists of two 4K x 16-bit dynamic RAM arrays mounted on a dual form-factor circuit card. Each array incorporates 16 4K x 1-bit semiconductor RAM packages arranged in a parallel bus configuration. The standard CP4165 uses three 8K modules, or 24K x 16-bit words. The additional 4K x 16-bit memory resident on the processor card brings the total to 28K words.

4.2 Strap Configuration

The relative position of each block of memory within the controller address space is determined by soldered-on strap options on each card. Seven straps are available. The W, X, Y, and Z straps select the address range of each bank of memory, and the R-S straps allow either the upper or lower 4K bank of a module to be disabled. The T strap allows the memory control logic to reply to Q-bus refresh protocol. The memory acts as a slave in all data transfer protocol.

Each strap is a soldered-in jumper that resembles an unmarked resistor. Figure 4.1 details the strap locations and table 4.1 lists their functions and standard configuration. Figure 4.2 shows a map of the CP4165 address space. Included in the map is the standard strap configuration for each bank of memory.

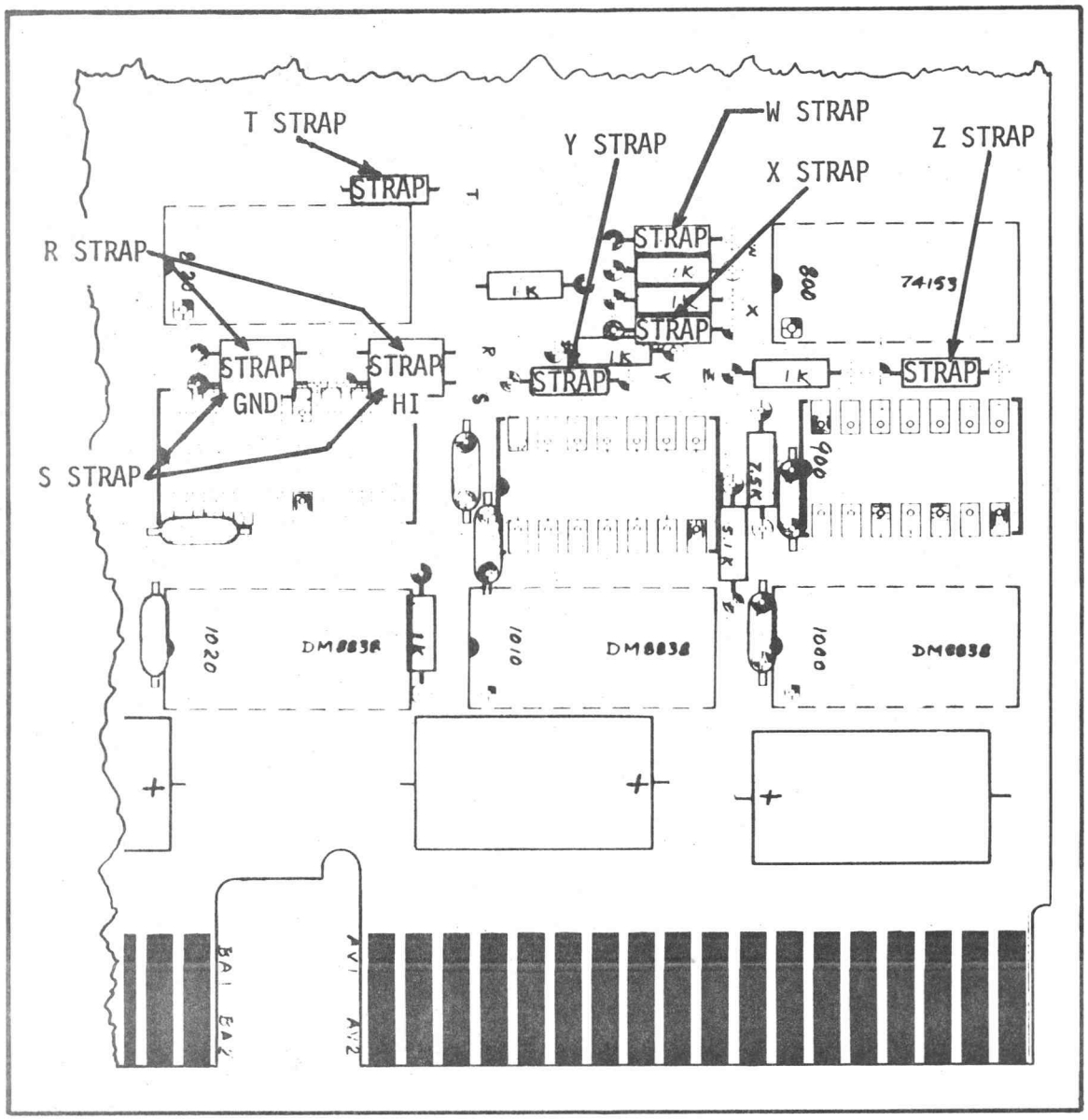


Figure 4.1

Strap Locations on the 8K Memory Module

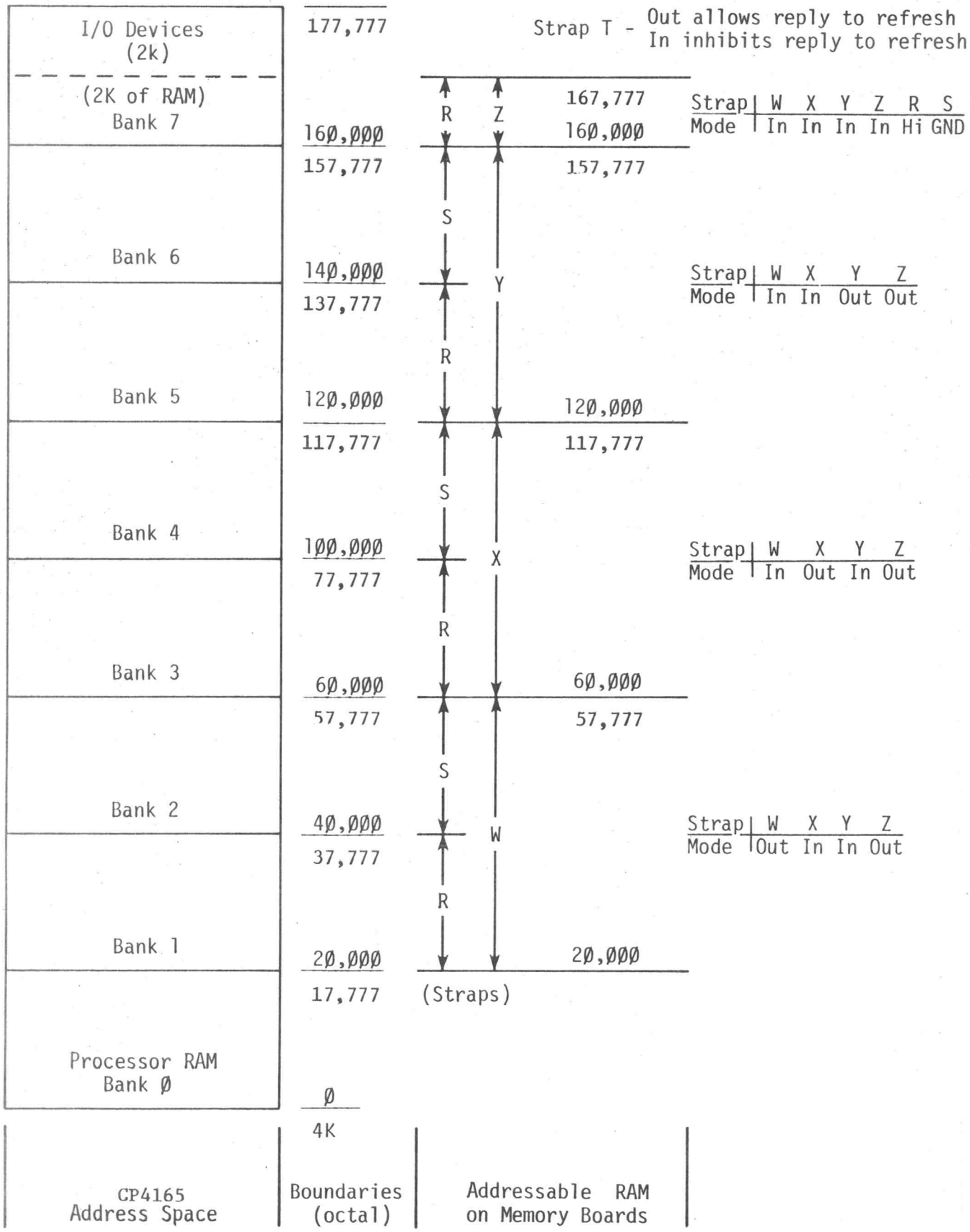

I/O Devices (2k)
(2K of RAM) Bank 7
Bank 6
Bank 5
Bank 4
Bank 3
Bank 2
Bank 1
Processor RAM Bank Ø
177,777
160,000
157,777
140,000
137,777
120,000
117,777
100,000
77,777
60,000
57,777
40,000
37,777
20,000
17,777
Ø
4K
(Straps)
Strap T - Out allows reply to refresh
In inhibits reply to refresh
R
Z
S
Y
R
S
X
R
S
W
R
167,777
160,000
157,777
120,000
117,777
60,000
57,777
20,000
Strap Mode | W In | X In | Y In | Z In | R Hi | S GND
Strap Mode | W In | X In | Y Out | Z Out
Strap Mode | W In | X Out | Y In | Z Out
Strap Mode | W Out | X In | Y In | Z Out
CP4165 Address Space
Boundaries (octal)
Addressable RAM on Memory Boards

Figure 4.2

TABLE 4.1

STRAP FUNCTION AND CONFIGURATION

Strap	Banks	Address Range (bytes)	Strap Function		Standard Configuration
W	1 and 2	$20,000_8$ to $57,777_8$	Address select	Remove to select	Removed Module 1 only
X	3 and 4	$60,000_8$ to $117,777_8$	Address select		Removed Module 2 only
Y	5 and 6	$120,000_8$ to $157,777_8$	Address select		Removed Module 3 only
Z	7	$160,000_8$ to $167,777_8$	Address select	Leave in to select	Removed all modules
R			Strap in disables lower 4K block of memory		Removed all modules
S			Strap in disables upper 4K block of memory		Removed all modules
T			Strap in inhibits reply to refresh		Installed all modules

4.3 Refresh

The 8K Memory module is dynamic, and must be refreshed at regular intervals. Refresh in the CP4165 is processor-initiated and occurs at a 600 Hz rate (1.67 millisecond intervals). Any Q-bus master capable of DMA-type transfers must either relinquish bus control at that rate or perform the refresh itself. Refresh exercises all 64 combinations of the six address bits BDAL1 - BDAL6.

8K Memory Module

CHARACTERISTICS	DESCRIPTION
Power Consumption Per Module	+12B 1.5A Max (Peak). +5B 1.2A Max -12B 1.5A Max
Q-Bus Interface	Complies with section 1.5.
Board Outline	Dual - See section 1.3 for drawing.

SECTION 5

Serial-Bootstrap-Termination (SBT) Module

5.1 Introduction

The SBT Module provides three basic functions: serial interface, bootstrap program, and Q-bus termination. The serial interface provides an asynchronous communication link to computer display terminals and teletypewriters. Current loop and RS232C protocols are supported.

The Bootstrap program is stored in ROM (Read Only Memory) on the SBT board. The program allows properly formatted programs to be loaded from either a floppy-disc drive or a terminal-interfaced paper-tape reader. Simple keyboard commands (TT, DX0, DX1) start bootstrap execution.

Termination resistors on the SBT board electrically terminate the Q-bus lines. To provide proper termination and to minimize reflections, the SBT module must be located in the most distant (electrically) slot from the processor module. The topmost bus connector in the short quad section (#14-see figure 1-5) is the normal SBT location in the CP4165.

Logic on the SBT Module also controls the front-panel BUS BUSY indicator and responds to the RESTART switch.

SBT Module

CHARACTERISTICS	DESCRIPTION
See Figure 5.1 for location of all strap options.	
Baud Rate Selection	

Straps

Baud Rate	K4	K3	K2	K1
50	0	0	1	0
75	0	0	1	1
110	1	1	1	1
134.5	0	1	0	0
150	1	1	1	0
200	0	1	0	1
300	1	1	0	1
600	0	1	1	0
1200	1	0	1	1
1800	1	0	1	0
2400	0	1	1	1
4800	1	0	0	1
9600	1	0	0	0
EXTERNAL* (via DH1, CC)	0	0	0	1

* Selected at time of manufacture.
Maximum external rate: 9600 Baud.

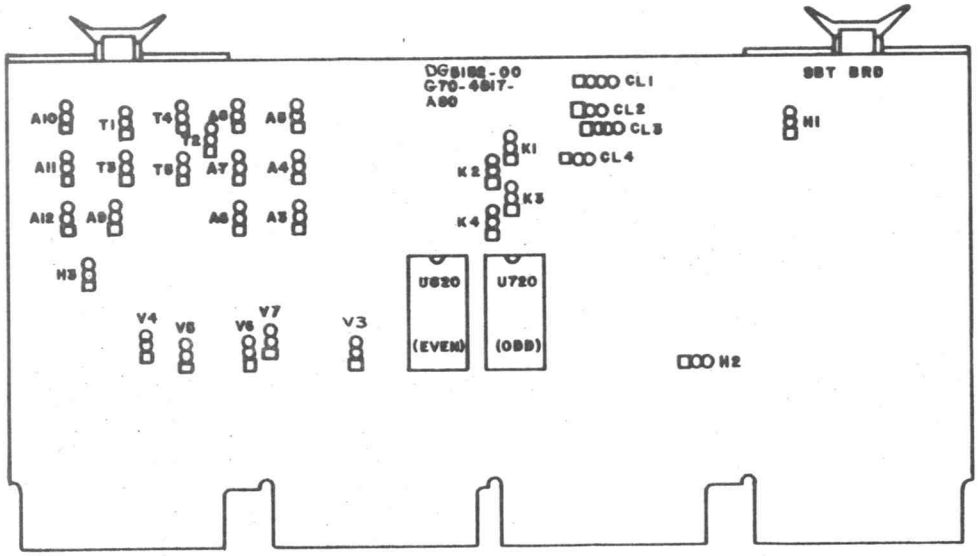


Figure 5.1 SBT Module Strap Locations

SBT Module

CHARACTERISTICS	DESCRIPTION
Number of data bits	
Number of stop bits	
Parity	

#BITS	T1	T2
5	0	0
6	1	0
7	0	1
8*	1	1

#SB	T5
1	0
2*	1

Parity	T4	T3
ODD Parity	0	0
No Parity*	0	1
Even Parity	1	0

* Selected at time of manufacture.

SBT Module

CHARACTERISTICS	DESCRIPTION

Address Selection:

Straps A3-A12

Console address range: $160{,}000_8$ - $177{,}776_8$

$177{,}560_8$ selected at time of manufacture as shown:

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3
1	1	1	1	1	0	1	1	1	0

Vector Address:

Straps V3 - V7

Range: $0 - 370_8$

60_8 selected at time of manufacture as shown:

V7	V6	V5	V4	V3
0	0	1	1	0

Current Loop Control:

		SBT Not Current Source (Passive Mode)		
			Grounded Input/Output	
Jumper	SBT Current Source (Active mode)	Floating Input/Output	Positive Ext. Current Source	Negative Ext. Current Source
CL1	1-2, 3-4	2-3	1-2	2-3*
CL2	1-2	2-3	2-3	1-2*
CL3	1-2, 3-4	2-3	1-2	2-3*
CL4	1-2	2-3	2-3	1-2*

*Selected at time of manufacture.

Place strap between pins shown for each jumper.

SBT Module

CHARACTERISTICS	DESCRIPTION
Break Halt Enable (H1 strap)	
Restart Switch Option (H2 strap)	
Bootstrap Enable (H3 strap)	

H1	Action when BREAK Pusled
0	Halt not asserted
1*	Halt asserted

H2	Action when RESTART Pressed
0*	Selected Power Up Option executed
1	Terminal mode entered

H3	Result
0*	Bootstrap Program Enabled
1	Bootstrap Program Disabled

*Selected at time of manufacture.

SBT Module

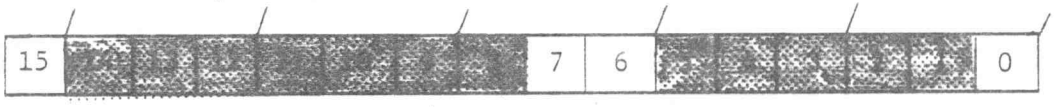
CHARACTERISTICS	DESCRIPTION
Bus Protocols	The SBT module participates in the following Bus Protocols:

Protocol	Role
DATI	Slave
DATIO	Slave
DATO	Slave
DATOB	Slave
DMA*	Requestor
Interrupt	Requestor
Power-up/down	BDCOKH CONTROLLER

* Front-panel RESTART switch uses DMA protocol.

SBT Module

CHARACTERISTICS	DESCRIPTION
Receiver Control/Status Register (RCSR)	Address: $177,560_8$ assigned at manufacture.



(Shaded bits not used-read as 0)

Bit 15: Dataset Status (read only)

Set: When an EIA device asserts "Carrier" or "Clear to Send" and "Data Set Ready" signals at I/0 connector.

Bit 7: Receiver Done (read only)

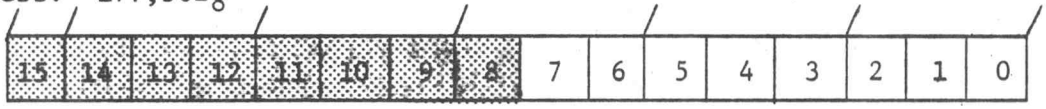
Set: When an entire character has been received and is ready for input to the processor.

Cleared: When RBUF is addressed or when BDCOK H on the Q Bus goes false (low).

Function: The interface generates an interrupt to the controller when this bit is set and Interrupt Enable (bit 6) is also set.

SBT Module

CHARACTERISTICS	DESCRIPTION
RCSR (cont)	Bit 6: Interrupt Enable (read/write) Set: Under control of software. Cleared: Under control of software or BINITL signal on the Q Bus. Function: Enables an interrupt request when Receiver Done (bit 7) is set. Bit 0: Reader Enable (write only) Set: Under program control. Cleared: Automatically by the new character's start bit. Function: Advances the paper tape reader on a teletypewriter device to input a new character.
Receiver Data Buffer (RBUF)	Address: $177,562_8$

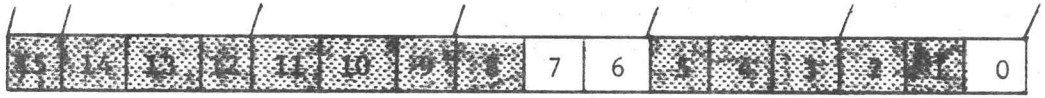


Shaded bits not used - read as 0.

Bits 7-0: Data from device. Contains eight data bits in a right-justified format.

SBT Module

CHARACTERISTICS	DESCRIPTION
Transmit Control/Status Register (XCSR)	Address: 177564_8



(Shaded bits not used-read as 0)

Bit 7: Transmit Ready (read/write)

Set: When XBUF is empty and can accept another character for transmission. It is also set during the power-up sequence by BDCOK H on the Q Bus.

Cleared: Automatically when XBUF is loaded.

Function: An interrupt request to the processor is asserted when this bit is set and Interrupt Enable (bit 6) is set.

Bit 6: Interrupt Enable (read/write)

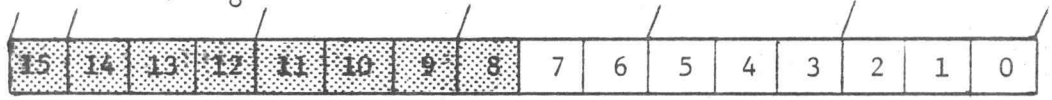
Set: Under software control.

Cleared: Under software control or by BINITL on the Q Bus.

Function: Enables an interrupt request to the processor when Transmit Ready (bit 7) is set.

SBT Module

CHARACTERISTICS	DESCRIPTION
XCSR (cont)	Bit 0: Break (read/write) Set: Under software control. Cleared: Under software control or BINITL on the Q Bus. Function: Causes a continuous space level to be transmitted to the device.
Transmit Data Buffer (XBUF)	Address: $177,566_8$



(Shaded bits not used-read as 0)

Bits 7-0: Eight right-justified data bits (write only).

Set: Under software control.

Function: Contains data to be transmitted to a device.

5.5 Bootstrap Program

The bootstrap program on the SBT Module is contained in PROM. The bootstrap enables the CP4165 to boot from floppy drive 0 or 1, and paper tape in LDA format. The bootstrap program also enables the CP4165 to resume program execution after a power-fail condition.

The bootstrap program is executed on power up or when the front panel "RESTART" switch is depressed.

5.5 Bootstrap Program

SBT Module

CHARACTERISTICS	DESCRIPTION
Floppy-disc bootstrap	The floppy-disc bootstrap program first disables interrupts. It uses the operator-entered drive number (DX0 or DX1)and then sizes memory. Any errors detected while sizing memory halt the processor. A message is printed on the console terminal detailing the memory location where the error occurred. The program then loads block 0 of the selected floppy drive and begins execution at memory location 0000.
Paper-tape bootstrap	The paper tape bootstrap program can load properly formatted (absolute loader) tapes from a terminal-interfaced paper tape reader. The operator enters "TT", then the program sizes memory and disables interrupts. Errors are printed on the terminal as for the floppy program. Checksums are computed for each block and a checksum error will halt the processor. A "checksum" message is printed in that case. After loading, program control is transferred to the transfer address specified in the loaded program. If no transfer address is specified, the bootstrap program halts and passes control to ODT.

Paper Tape Format (LDA)

CHARACTERISTICS	DESCRIPTION
Absolute binary format (LDA)	A block of data punched on paper tape in absolute binary format has the following format. FRAME 1 001 start frame 2 000 null frame 3 xxx byte count (low 8 bits) 4 xxx byte count (high 8 bits) 5 yyy load address (low 8 bits) 6 yyy load address (high 8 bits) . data is . placed . here zzz last frame contains a block checksum A program on paper tape may consist of one or more blocks of data. Each block having a byte count (frames 3 and 4) greater than six will cause subsequent data to be loaded into memory (starting at the address specified in frames 5 and 6 under a normal load). The byte count is a positive checksum. When the byte count of a block is equal to six, the specified load address is checked to see whether the address is to an even or to an odd location. If even, the Loader will transfer control to the address specified. Thus the loaded program will be run upon completion of loading. If odd, the loader halts.

CHARACTERISTICS	DESCRIPTION
Program Re-execution on power-up	1. Interrupts are disabled. 2. The operator inputs PU. 3. PSW is loaded from location 26_8. PC is loaded from location 24_8. 4. The CP4165 begins execution of a user provided power up program, the starting address of which is stored in location 24_8.

5.5 Bootstrap Program (cont)

The odd and even byte bootstrap programs are shown in Tables 5.1 and 5.2. See figure 5.1 for odd and even byte ROM locations.

N	N	N+1	N+2	N+3	N+4	N+5	N+6	N+7	N+10	N+11	N+12	N+13	N+14	N+15	N+16	N+17	Byte Address
000/	000	003	020	011	000	011	000	013	201	220	001	213	003	011	377	012	
020/	113	125	000	000	001	020	012	021	021	027	000	215	027	000	011	000	
040/	020	011	000	000	120	000	012	377	213	377	200	027	377	140	105	377	
060/	012	000	025	000	021	145	000	020	215	025	000	025	377	045	377	002	
100/	012	013	003	013	011	376	012	101	040	105	040	122	000	000	001	045	
120/	013	000	011	377	065	000	003	000	001	020	377	377	377	377	377	377	
140/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
160/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
200/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
220/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
240/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
260/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
300/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
320/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
340/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
360/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
400/	025	000	215	021	012	024	022	020	025	377	012	013	012	011	000	012	
420/	117	124	126	061	063	012	105	040	000	011	000	220	000	011	000	120	
440/	045	120	003	045	124	003	045	104	002	011	000	025	200	025	200	240	
460/	000	002	145	000	001	213	377	200	227	377	213	377	200	020	377	105	
500/	377	000	023	213	377	200	224	377	002	020	000	025	000	011	000	020	
520/	025	376	261	003	225	000	020	020	001	025	000	014	207	225	222	061	
540/	003	201	207	213	201	012	045	000	002	245	000	013	012	025	000	011	
560/	000	020	012	011	000	012	002	011	000	013	002	011	000	345	000	045	
600/	000	003	020	011	000	011	000	013	201	220	001	213	003	011	377	012	
620/	113	125	000	000	001	020	012	021	021	027	000	215	027	000	011	000	
640/	020	011	000	000	120	000	012	377	213	377	200	027	377	140	105	377	
660/	012	000	025	000	021	145	000	020	215	025	000	025	377	045	377	002	
700/	012	013	003	013	011	376	012	101	040	105	040	122	000	000	001	045	
720/	013	000	011	377	065	000	003	000	001	020	377	377	377	377	377	377	
740/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
760/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	

TABLE 5.1

Odd Byte ROM Program (U720)

(All Numbers In Octal)

N	N	N+1	N+2	N+3	N+4	N+5	N+6	N+7	N+10	N+11	N+12	N+13	N+14	N+15	N+16	N+17	Byte Address
000/	002	120	102	367	062	367	076	302	002	021	372	305	345	367	146	015	
020/	103	123	115	000	335	306	000	020	110	300	026	000	307	024	367	014	
040/	001	367	006	300	001	207	237	160	337	160	375	300	162	005	300	000	
060/	302	207	300	004	301	301	064	120	310	300	032	310	377	310	377	004	
100/	010	320	370	340	367	370	015	102	104	113	113	100	063	000	376	226	
120/	340	207	367	224	301	001	002	000	376	107	377	377	377	377	377	377	
140/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
160/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
200/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
220/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
240/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
260/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
300/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
320/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
340/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
360/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
400/	300	200	000	203	000	004	005	006	300	160	020	320	010	367	146	015	
420/	102	117	040	060	055	015	104	126	075	367	064	002	302	367	054	002	
440/	302	125	162	302	124	107	302	130	344	367	024	304	247	302	207	027	
460/	061	002	302	020	026	337	160	375	300	162	337	164	375	037	166	300	
500/	200	207	201	337	164	375	137	166	372	116	207	306	030	367	306	006	
520/	301	170	011	376	303	007	100	220	002	310	001	203	002	311	023	011	
540/	376	356	366	311	371	000	310	240	347	302	207	100	007	306	030	367	
560/	202	006	005	367	142	300	373	367	132	300	367	367	102	301	004	301	
600/	002	120	102	367	062	367	076	302	002	021	372	305	345	367	146	015	
620/	103	123	115	000	335	306	000	020	110	300	026	000	307	024	367	014	
640/	001	367	006	300	001	207	237	160	337	160	375	300	162	005	300	000	
660/	302	207	300	004	301	301	064	120	310	300	032	310	377	310	377	004	
700/	010	320	370	340	367	370	015	102	104	115	115	100	060	000	376	226	
720/	340	207	367	224	301	001	002	000	376	107	377	377	377	377	377	377	
740/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	
760/	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	377	

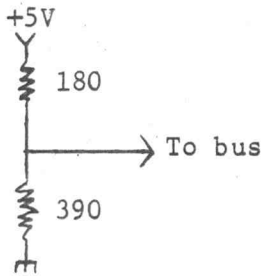
TABLE 5.2

Even Byte ROM Program (U620)

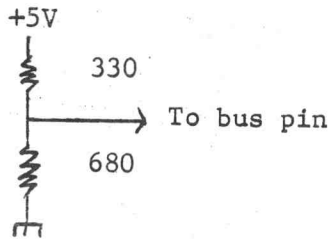
(All Numbers In Octal)

5.6 Bus Termination

SBT Module

CHARACTERISTICS	DESCRIPTION
Termination Network 120 Ω	 Equivalent resistance = 120 Ω Equivalent voltage = 3.5 Volts This circuit connected to the following bus pins: CA1 BSPARE1 CB1 BSPARE2 CC1 BSPARE3 CD1 BSPARE4 CN1 BDMRL CP1 BHALTL CR1 BREFL CE2 BDOUTL CF2 BRPLYL CH2 BDINL CJ2 BSYNCL CK2 BWTBTL CL2 BIRQL CP2 BBS7L CT2 BINITL CU2 BDAL0L CV2 BDALIL DA1 BDCOKH DB1 BPOKH DN1 BSACKL DP1 BSPARE6 DE2 BDAL2L DF2 BDAL3L DH2 BDAL4L DJ2 BDAL5L DK2 BDAL6L DL2 BDAL7L DM2 BDAL8L DN2 BDAL9L DP2 BDAL10L DR2 BDAL11L DS2 BDAL12L DT2 BDAL13L DU2 BDAL14L DV2 BDAL15L

SBT Module

CHARACTERISTICS	DESCRIPTION
Termination Network 250 Ω	 Equivalent resistance = 220 Ω Equivalent voltage = 3.5 V This circuit connected to the following bus pins: CM2 BIAKIL CN2 BIAKOL CR2 BDMGIL CS2 BDMGOL These two pins are connected together and to one termination resistor network.

SBT Module

CHARACTERISTICS	DESCRIPTION
Power Consumption	+5B (5V) 0.4 A max. +5I (5V) 0.75 A max. +12I (12V) 0.1 A max. -12B (-12V) 30.0 MA max.
Q Bus Interface	Complies with section 1.05
Board Outline	Short Quad - See section 1.03 for drawing.
I/O Interface	
20 MA current loop	
Active Mode	Supplies current from 20 MA source using +12V DC as per CCITT specifications.
Passive Mode (selected at manufacture)	Sinks 20 MA.
EIA Mode	Supplies or senses nominal ± 12V DC as per EIA spec. RS232C.

NOTES

SECTION 6

Backplane

6.1 Introduction

The CP4165 Backplane assembly interconnects the Q-Bus between the processor board and up to 13 additional CP4165 interface or memory modules. The backplane is contained within a card guide assembly that provides mechanical stability for the modules installed in the backplane. Power, ground, and control signals are supplied to the backplane through a 38-pin square-pin connector. All interface cabling connects to a set of connectors along the back of the card guide assembly. These connectors correspond on a one to one basis to connectors located just below the backplane module positions. Certain positions of the backplane have full power provided during battery back-up operation. These positions are normally dedicated to the processor and memory modules.

6.2 Backplane Description

Backplane Position Designations

Figure 6.1 shows the numbering scheme used to specify bus positions for the two backplane sections.

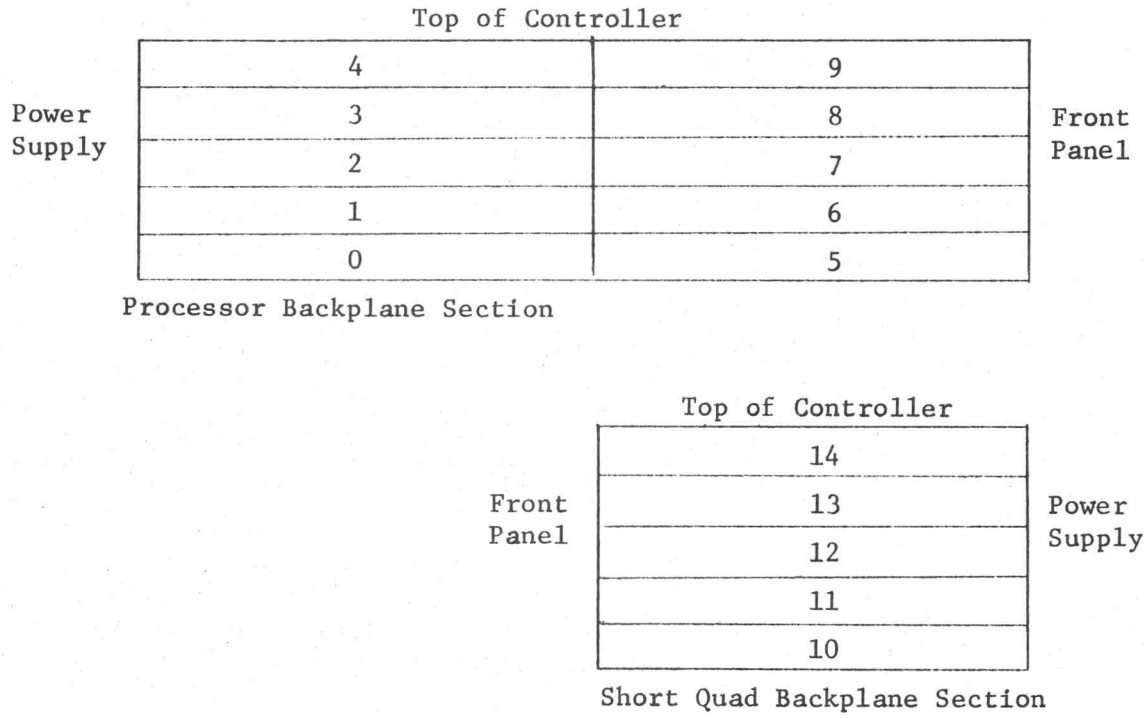


Figure 6.1: CP4165 Backplane Position Numbers

6.3 BIAK/BDMG BUS Grant Chain

Referring to Figure 6.1, the two grant lines (BIAKI/0, BDMGI/0) go from bus position to bus position as shown in Table 6.1.

Table 6.1

BIAK/BDMG Bus Grant Chain

1-2-3-4-5-6-7-8-9-10-11-12-13-14

6.4 Quad and Short Quad Module Locations

The backplane is designed to accept the processor module in any horizontal pair of bus positions on the processor side of the backplane assembly except the 4-9 pair. Other Quad and Short quad modules are accepted in any bus position on the processor side. Short quad section. If the SBT board is located in any bus position other than 14, the termination resistors must be disconnected and other means of termination provided at position 14. See figures 1.4 and 1.5.

6.5 Dual Module Locations

The 8K memory modules can be placed in any bus position from zero through nine except bus position three. Other dual modules can be placed in any bus position on the processor side. See figures 1.4 and 1.5.

6.6 Power Distribution

The backplane is designed to provide power to certain modules during short term loss of ac line power. To accomplish this, the backplane is partitioned into two sections for power distribution. During battery operation, one section provides full power to the modules. The other section loses all power except -12 V and +5 V supplied through the 5B bus pins. Note that the power partitions do not correspond to the physical partitions of the processor and short-quad sections.

Battery Back-up Power Distribution

Table 6.2 lists the pin assignments for the power supplies.

Table 6.2

Power Supply Bus Pin Assignments

+5B	AV1, BV1, CV1, DV1
+5	AA2, BA2, CA2, DA2
+12	AD2, BD2, CD2, DD2
-12	AB2, BB2, CB2, DB2

To supply all necessary power (+5, +12, -12) to the modules during battery operation, bus positions 0-2 and 5-7 have all supply pins connected to battery backed-up power supplies. In addition, bus position 3 has one +12 pin connected to the battery supply. All other positions supply only +5B and -12B power during battery back-up. Bus position 3 is reserved for an interface module that requires +12V. Some modules interconnect pins AD2 and BD2. Such modules must not be placed in position 3.

Table 6.3

Battery Back-up Power Supply Bus Pin Assignments

Supply	Pins	Bus Position
+5B	AV1, BV1, CV1, DV1	Ø-14
+5B	AA2, BA2, CA2, DA2	0-2, 5-7
+12B	AD2, BD2, CD2, DD2	0-2, 5-7
+12B	AD2	3
-12B	AB2, BB2, CB2, DB2	Ø-9
-12B	CB2, DB2	1Ø-14

Interruptible Power Distribution

The second backplane power partition (bus positions 3, 4, 8, 9, 10, 14) does not receive +5 and +12 power during loss of ac line power except as shown in Table 6.3. The power supplies for these positions are interruptible and are designated 5I and 12I. Table 4 below lists the pin assignments for the interruptible supplies.

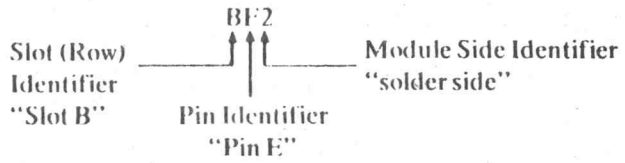
Table 6.4

Interruptible Power Supply Bus Pin Assignments

Supply	Pins	Bus Position
+5I	AA2, BA2, CA2, DA2	6-9
+5I	CA2, DA2	1Ø-14
+12I	BD2	6
+12I	AD2, BD2, CD2, DD2	7-9
+12I	CD2, DD2	1Ø-14

6.7 Backplane Connector Description

Figures 6.2a and 6.2b show the module contact-pin identification scheme for the plug-in modules in the CP4165. The pin identification numbering scheme is as follows: slots, shown as ROW A and ROW B in Figure 6.2a include a numeric identifier for each side of the module. The component side is designated "1" and the solder side is designated "2". Letters ranging from A through V (except G, I, O and Q) identify a particular pin on one side of a slot. Hence, a typical pin is designated as:



6.8 Q-Bus Pin Assignments

Table 6.5 is a list of the Q-Bus pin assignments. Briefly, any signal mnemonic that starts with B (e.g., BHALT) is a bus signal. These signals are routed to all bus positions shown in Figure 6.1 via the pins assigned in Table 6.5. Signal mnemonics that start with S (e.g., SSPARE1), are not generally routed to every bus position. They are used to interconnect specific bus positions or for special purposes. The CP4165 uses two special SSPARE pins to provide signals for the bus busy and processor busy front-panel indicators.
A third SSPARE line routes the front-panel RESTART switch signal to the SBT board. Table 6.6 shows which of the SSPARE pins are used and how they are connected. Several bus positions have been connected together by SSPARE4 for future use.

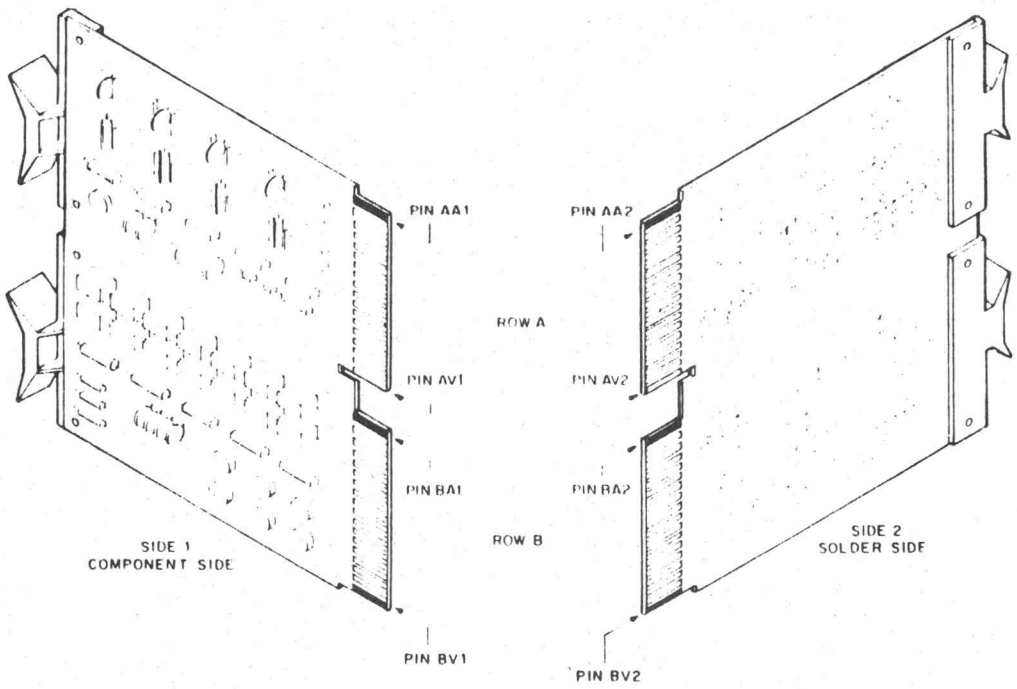


Figure 6.2a: Dual Module Contact Finger Identification

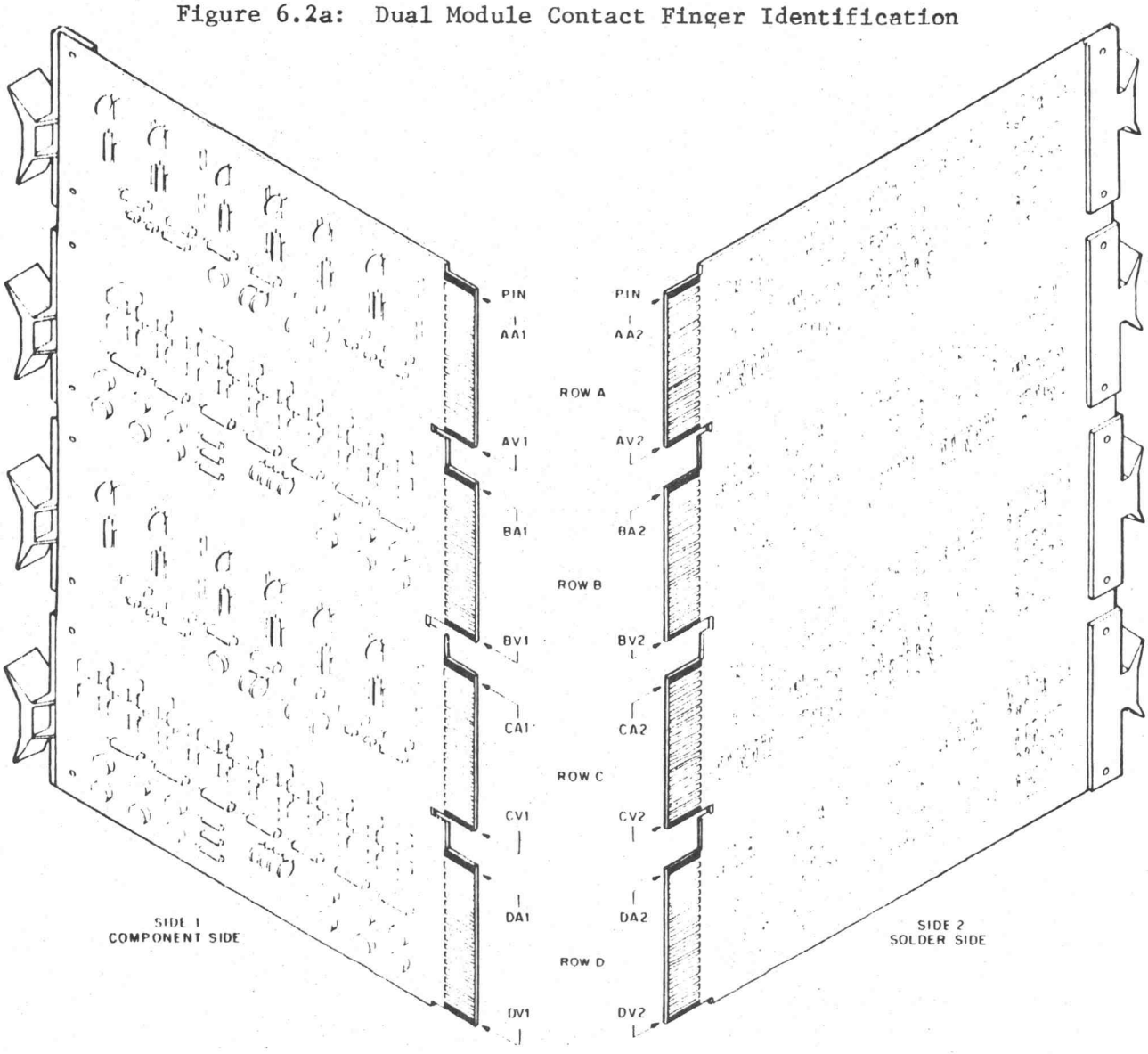


Figure 6.2b: Short Quad & Quad Module Contact Finger Identification.

Table 6.5
Q-Bus Pin Assignments

Row A (Same as Row C)		Row B (Same as Row D)	
Module Side 1 (Component Side)			
AA1	BSPARE1	BA1	BDCOK H
AB1	BSPARE2	BB1	BPOK H
AC1	BSPARE3	BC1	SSPARE4
AD1	BSPARE4	BD1	SSPARE5
AE1	SSPARE1	BE1	SSPARE6
AF1	SSPARE2	BF1	SSPARE7
AH1	SSPARE3	BH1	SSPARE8
AJ1	GND	BJ1	GND
AK1	MSPARE A	BK1	MSPARE B
AL1	MSPARE A	BL1	MSPARE B
AM1	GND	BM1	GND
AN1	BDMR L	BN1	BSACK L
AP1	BHALT L	BP1	BSPARE6
AR1	BREF L	BR1	BEVNT L
AS1	PSPARE3	BS1	PSPARE4
AT1	GND	BT1	GND
AU1	PSPARE1	BU1	PSPARE2
AV1	See Table 6.3	BV1	See Table 6.3
Module Side 2 (Solder Side)			
AA2	See Tables 6.3/6.4	BA2	See Tables 6.3/6.4
AB2	See Table 6.3	BB2	See Table 6.3
AC2	GND	BC2	GND
AD2	See Tables 6.3/6.4	BD2	See Tables 6.3/6.4
AE2	BDOUT L	BE2	BDAL2 L
AF2	BRPLY L	BF2	BDAL3 L
AH2	BDIN L	BH2	BDAL4 L
AJ2	BSYNC L	BJ2	BDAL5 L
AK2	BWTBT L	BK2	BDAL6 L
AL2	BIRQ L	BL2	BDAL7 L
AM2	BIAKI L	BM2	BDAL8 L
AN2	BIAKO L	BN2	BDAL9 L
AP2	BBS7 L	BP2	BDAL10 L
AR2	BDMGI L	BR2	BDAL11 L
AS2	BDMGO L	BS2	BDAL12 L
AT2	BINIT L	BT2	BDAL13 L
AU2	BDAL0 L	BU2	BDAL14 L
AV2	BDAL1 L	BV2	BDAL15 L

Table 6.6
SSPARE Assignments

Signal	Pin	Bus Positions	Purpose
SSPARE1	AE1;CE1	9,14	Restart (RST) signal from Front-Panel to SBT board.
SSPARE2	AF1;CF1	9,14	Bus Busy (BRUN) from SBT board to Front-Panel.
SSPARE3	CH1	0-4	Proc Busy Signal (SRUN) from Processor Module to Front-Panel.
SSPARE4	BC1	5-9	Not defined, for future use (SSPR4).

6.9 Power/Control Signal Connector

On one end of the backplane there is a 38 pin power/control signal

the pin assignments.

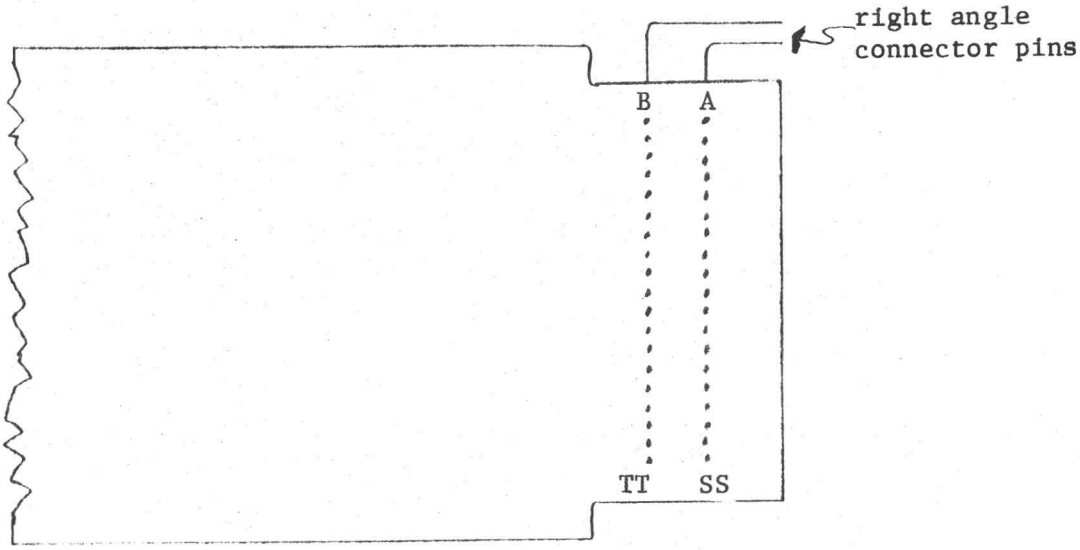


Figure 6.3: Backplane Power/Control Signal Connector

Table 6.7

Backplane Power/Control Signal Connector Pin Assignments

Pin	Mmenonmic	Description
A	SRUN	Signal to drive PROC BUSY Front-Panel Indicator.
B	12I	Interruptible +12 V power supply.
C	BPOK	Signal indicating ac line power is present.
D	12I	Interruptible +12 V power supply.
E	BHALT	Signal from front-panel RUN/HALT switch to Processor Module.
F	12IS	12I supply sense line.
H	BEVNT	50/60 Hz real-time clock input to Processor Module.
J	12BS	12B supply sense line.
K	BDCOK	Signal indicating 5B and 12B supplies are operating correctly.
L	12B	Battery backed-up +12 V power supply.
M	BRUN	Signal to drive BUS BUSY front-panel indicator.
N	12B	Battery backed-up +12 V power supply.
P	RST	Signal from front-panel RESTART switch.
R	-12B	Battery backed-up -12 V power supply.
S	SSPR4	Not defined. For future use.
T	Gnds	Ground sense line for all power supplies.
U-Z	5I	Interruptible 5V power supply.
AA	5BS	5B supply sense line.
BB	5IS	5I supply sense line.
CC-FF	5B	Battery backed-up 5V power supply.
HH-TT	Gnd	Ground return.

6.10 Peripheral I/O Wiring

All peripheral I/O cabling, except for the terminal cable to the SBT module, connects to a set of eight 40-pin connectors located on the rear of the card cage assembly. The terminal cable connects directly to the SBT card.

The eight connectors on the rear of the card cage are divided into two groups of four, one group on each of the outer edges of the card cage assembly. Each connector corresponds to an identical connector located directly below the handle side of the module boards. The connectors are identified at each end and pin A is marked in each case.

6.11 Mechanical Specifications

Backplane Module Connector

The backplane-to-module connection requires two types of connector blocks. One of the blocks is shown in Fig. 6.4a and the other in Fig. 6.4b. Both of these connector blocks are obtained from DEC. The backplane is made up of three of the H803 blocks and six of the H807 blocks. The ears on the H807 block must be removed prior to installation on the backplane boards.

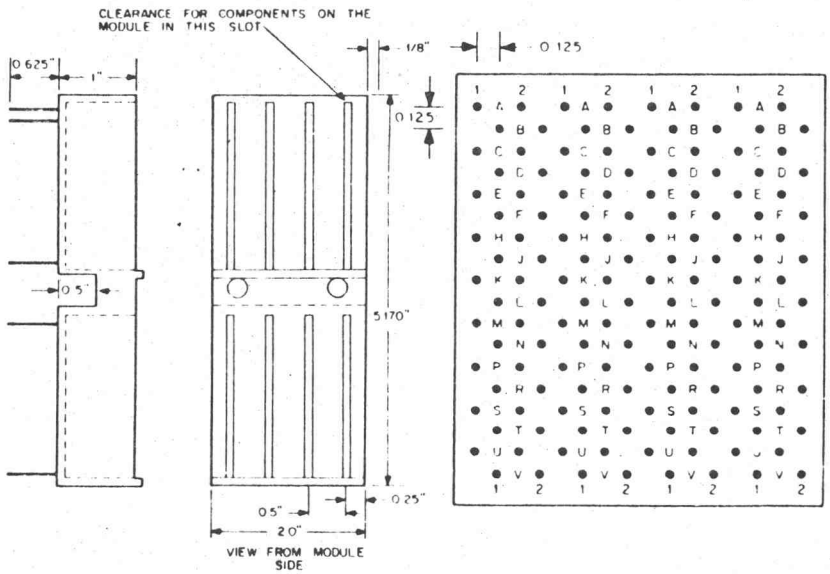


Figure 6.4a: DEC H803 Connector Block

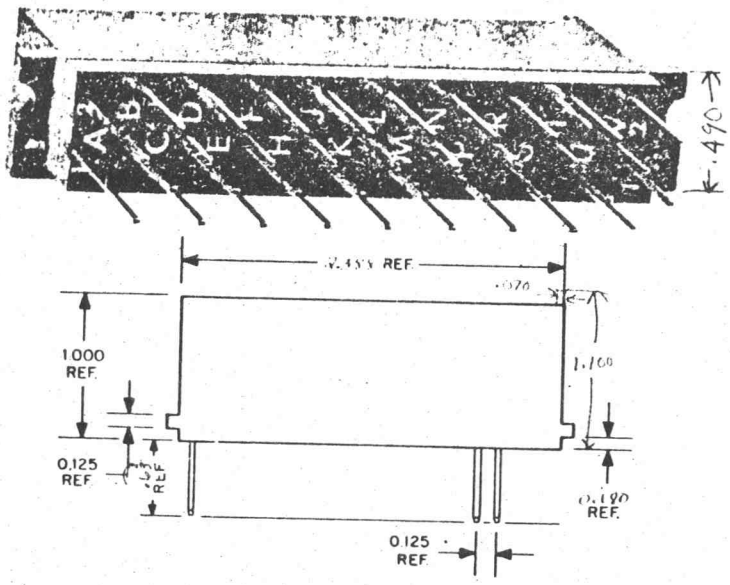
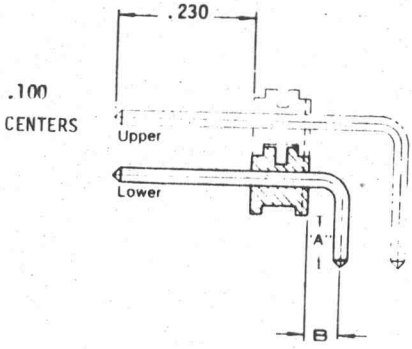


Figure 6.4b: DEC H807 Connector Block

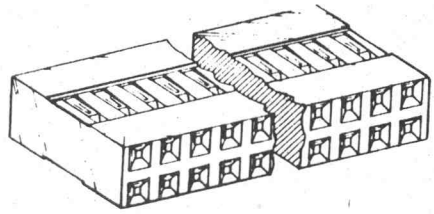
Backplane Power/Control Connector

Figure 6.5a shows the connector pins and Fig. 6.5b the terminal holder used on the backplane Power/Control connector.



	NUMBER OF CONTACTS	DIMENSIONS A	DIMENSIONS B
UPPER	1 X 19	.195	.160
Lower	1 X 19	.090	.060

Figure 6.5a: Power/Control Connector Pins



CONTACT CENTERS	NUMBER OF CONTACTS
0.100	2 X 19

Figure 6.5b: Power/Control Terminal Holder

ENGINEERING INSTRUMENT SPECIFICATION

CHANGE REQUEST

This form is a worksheet used to make changes in an Engineering Instrument Specification (EIS) or (for the case when an EIS does not exist) in performance claims quoted in other publications.

Return completed form to Product Specifications 76-440 for action and distribution.

Product: _____

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Recommended Action	Prog. Mgr.	Proj. Eng.	Eval. Mgr.	Eval. Eng.	CRT Eng.	Manual Writer
Approve						
Reject						

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ENGINEERING INSTRUMENT SPECIFICATION

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Approve						
Reject						

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Change: Subject: _____ Page No. _____

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Reason for change: _____

Initial in appropriate space

Recommended Action	Prog. Mgr.	Proj. Eng.	Eval. Mgr.	Eval. Eng.	CRT Eng.	Manual Writer
Approve						
Reject						

Date Received in Product Spec's _____ by: _____

Change No. 754-4

ENGINEERING INSTRUMENT SPECIFICATION

CHANGE NOTICE

Product CP4165

Publication Affected Engineering Instrument Specification **No.** 754 **Dated** 11/15/76

Page 6-4 **Subject** Interruptible Power Supply Bus Pin Assignments

CHANGED FROM

Supply	Pins	Bus Position
+5I	AA2, BA2, CA2, DA2	6-9
+12I	BD2	6
+12I	AD2, BD2, CD2, DD2	7-9

CHANGED TO

Supply	Pins	Bus Position
+5I	AA2, BA2, CA2, DA2	3, 4, 8, 9
+12I	BD2	3
+12I	AD2, BD2, CD2, DD2	4, 8, 9

Reason For Change Error in original text.

Approved By Wayne Eskelman (Program Manager) **Effective Date** 9-12-77

6.5 Dual Module Locations

The 8K memory modules can be placed in any bus position from zero through nine except bus position three. Other dual modules can be placed in any bus position on the processor side. See figures 1.4 and 1.5.

6.6 Power Distribution

The backplane is designed to provide power to certain modules during short term loss of ac line power. To accomplish this, the backplane is partitioned into two sections for power distribution. During battery operation, one section provides full power to the modules. The other section loses all power except -12 V and +5 V supplied through the 5B bus pins. Note that the power partitions do not correspond to the physical partitions of the processor and short-quad sections.

Battery Back-up Power Distribution

Table 6.2 lists the pin assignments for the power supplies.

Table 6.2

Power Supply Bus Pin Assignments

+5B	AV1, BV1, CV1, DV1
+5	AA2, BA2, CA2, DA2
+12	AD2, BD2, CD2, DD2
-12	AB2, BB2, CB2, DB2

To supply all necessary power (+5, +12, -12) to the modules during battery operation, bus positions 0-2 and 5-7 have all supply pins connected to battery backed-up power supplies. In addition, bus position 3 has one +12 pin connected to the battery supply. All other positions supply only +5B and -12B power during battery back-up. Bus position 3 is reserved for an interface module that requires +12V. Some modules interconnect pins AD2 and BD2. Such modules must not be placed in position 3.

Table 6.3

Battery Back-up Power Supply Bus Pin Assignments

Supply	Pins	Bus Position
+5B	AV1, BV1, CV1, DV1	Ø-14
+5B	AA2, BA2, CA2, DA2	0-2, 5-7
+12B	AD2, BD2, CD2, DD2	0-2, 5-7
+12B	AD2	3
-12B	AB2, BB2, CB2, DB2	Ø-9
-12B	CB2, DB2	1Ø-14

Interruptible Power Distribution

The second backplane power partition (bus positions 3, 4, 8, 9, 10, 14) does not receive +5 and +12 power during loss of ac line power except as shown in Table 6.3. The power supplies for these positions are interruptible and are designated 5I and 12I. Table 4 below lists the pin assignments for the interruptible supplies.

Table 6.4

Interruptible Power Supply Bus Pin Assignments

	Supply	Pins	Bus Position
#	+5I	AA2, BA2, CA2, DA2	*3, 4, 8, 9*
	+5I	CA2, DA2	1Ø-14
#	+12I	BD2	*3*
#	+12I	AD2, BD2, CD2, DD2	*4, 8, 9*
	+12I	CD2, DD2	1Ø-14

9/6/77

Change No. 754-4

ENGINEERING INSTRUMENT SPECIFICATION

CHANGE NOTICE

Product CP4165

Publication Affected Engineering Instrument Specification **No.** 754 **Dated** 11/15/76

Page 6-4 **Subject** Interruptible Power Supply Bus Pin Assignments

CHANGED FROM

Supply	Pins	Bus Position
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+12I	BD2	6
+12I	AD2, BD2, CD2, DD2	7-9

CHANGED TO

Supply	Pins	Bus Position
+5I	AA2, BA2, CA2, DA2	3, 4, 8, 9
+12I	BD2	3
+12I	AD2, BD2, CD2, DD2	4, 8, 9

Reason For Change Error in original text.

Approved By Wayne Eskelman (Program Manager) **Effective Date** 9-12-77

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The 8K memory modules can be placed in any bus position from zero through nine except bus position three. Other dual modules can be placed in any bus position on the processor side. See figures 1.4 and 1.5.

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Power Supply Bus Pin Assignments

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Supply	Pins	Bus Position
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+12B	AD2, BD2, CD2, DD2	0-2, 5-7
+12B	AD2	3
-12B	AB2, BB2, CB2, DB2	Ø-9
-12B	CB2, DB2	1Ø-14

Interruptible Power Distribution

The second backplane power partition (bus positions 3, 4, 8, 9, 10, 14) does not receive +5 and +12 power during loss of ac line power except as shown in Table 6.3. The power supplies for these positions are interruptible and are designated 5I and 12I. Table 4 below lists the pin assignments for the interruptible supplies.

Table 6.4

Interruptible Power Supply Bus Pin Assignments

Supply	Pins	Bus Position
# +5I	AA2, BA2, CA2, DA2	3, 4, 8, 9
+5I	CA2, DA2	1Ø-14
# +12I	BD2	3
# +12I	AD2, BD2, CD2, DD2	4, 8, 9
+12I	CD2, DD2	1Ø-14

9/6/77

Change No. 754-3

ENGINEERING INSTRUMENT SPECIFICATION

CHANGE NOTICE

Product CP4165

Publication Affected Engineering Instrument Specification **No.** 754 **Dated** 11/15/76

Page 1-15 **Subject** Incorrect Spec.

CHANGED FROM

Bus Drivers

High State	≥ 2.4 V at -5.2 ma (source)

CHANGED TO

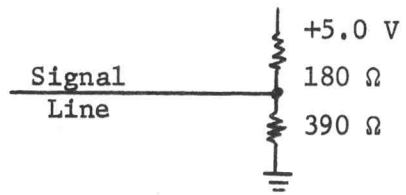
Bus Drivers

High State	Open-collector

Reason For Change Incorrect high state spec.

Approved By Wayne Eskelman 8-24-77 **Effective Date** _____
(Program Manager)

Electrical Specification - Q-Bus

CHARACTERISTICS	DESCRIPTION
Bus Drivers	(National 8838 or equivalent)
Low State	≤ 0.4 V at 48 ma (sink)
# High State	*Open-collector.*
Bus Receivers	(National 8838 or equivalent)
Low State	Input threshold voltage 0.8 V max. Input current -1.6 ma max.
High State	Input threshold voltage 2.0 V min. Input current 40 μa max at 2.4 V.
Bus Impedance	120 Ω nominal.
Bus Termination	As shown: 
Bus Module Stub Length	2 inches max.
Data Rate	833 x 10^3 Data transfers per second.

1.6 Standard Accessories

1) Power Cord
1) 220-V Line Fuse
1) Operator's Manual #070-2271-00
1) Service Manual #070-2278-00
1) Check-out Software

1.7 Optional Accessories

-Card Cage Interconnect Cable	PN-175-5064-00
-Power Supply Extension Cable	PN-067-0809-00
-Quad Extender Card	PN-119-0901-00

1.8 Options

Option 2 - 3 additional battery packs.

Option 31 - IEEE-488 Bus Interface, with Instruction manual #070-2179-00

Option 32 - CP-Bus Interface, with Instruction manual #070-2174-00

Change No. 754-3

ENGINEERING INSTRUMENT SPECIFICATION

CHANGE NOTICE

Product CP4165

Publication Affected Engineering Instrument Specification **No.** 754 **Dated** 11/15/76

Page 1-15 **Subject** Incorrect Spec.

CHANGED FROM

Bus Drivers

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CHANGED TO

Bus Drivers

High State	Open-collector

Reason For Change Incorrect high state spec.

Approved By Wayne Eskelman 8-24-77 **Effective Date** _____
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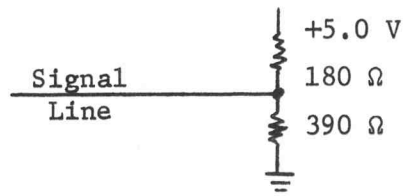
High State	Input threshold voltage 2.0 V min. Input current 40 μa max at 2.4 V.
Bus Impedance	120 Ω nominal.
Bus Termination	As shown: 
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Data Rate	833 x 10^3 Data transfers per second.

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