TEKTRONIX®

OPTIONAL DATA COMMUNICATIONS INTERFACE

021-0074-00

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97005

Serial Number _____

070-1379-00

1172

WARRANTY

All TEKTRONIX instruments are warranted against defective materials and workmanship for one year. Any questions with respect to the warranty should be taken up with your TEKTRONIX Field Engineer or representative.

All requests for repairs and replacement parts should be directed to the TEKTRONIX Field Office or representative in your area. This will assure you the fastest possible service. Please include the instrument Type Number or Part Number and Serial Number with all requests for parts or service.

Specifications and price change privileges reserved.

U.S.A. and foreign TEKTRONIX products covered by U.S. and foreign patents and/or patents pending.

TABLE OF CONTENTS

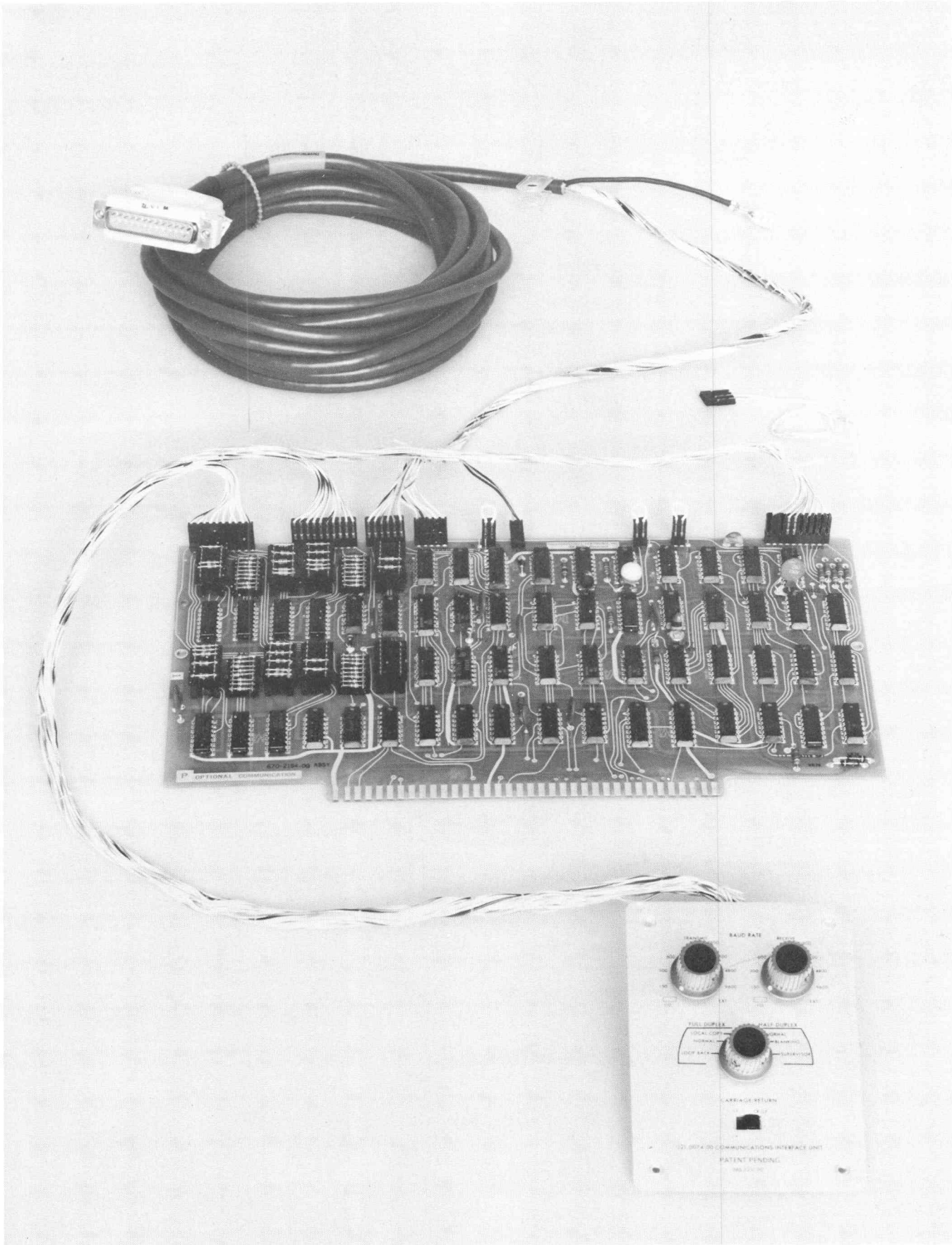


Fig. 1-1. Optional Data Communications Interface.

DESCRIPTION AND OPERATION

Introduction

The 021-0074-00 Optional Data Communications Interface connects the 4010 Series Computer Display Terminal to a modem to permit communication between the terminal and a computer. The Interface features externally mounted switches which control six operating modes and independently selectable transmit and receive baud rates. It also makes the Terminal Carriage Return option selection available externally. The Interface consists of a circuit card (which mounts on the motherboard within the pedestal), a switch panel, (which installs in the pedestal so that the switches are externally accessible at the back), and cable assemblies which connect between the card, the switch panel, TC-1 in the Terminal, and a modem.

General Characteristics

The operating modes are controlled by a six-position switch labeled FULL DUPLEX/HALF DUPLEX. This switch permits operation in any one of six modes, as follows.

Full Duplex-Loop Back, during which time the Terminal is isolated from the computer.

Full Duplex-Normal, during which time the Interface permits the Terminal to communicate with the computer.

Full Duplex-Local Copy, where an $\overline{\text{ECHO}}$ signal is provided to the Terminal to permit it to write a copy of the transmitted data.

Half Duplex-Normal, during which time transmission can only occur in one direction at a time, with the Terminal controlling the direction of transmission.

Half Duplex-Blanking, where the Terminal employs blanking signals to avoid receipt of erroneous data.

Half Duplex-Supervisory, where the computer controls the direction of transmission.

Programming

This is a summary of the programming considerations. For additional information, refer to the Specification Section.

Full Duplex Mode

No special considerations.

Half Duplex Normal Mode

Transmitting direction is controlled by the Terminal.

Either EOT or ETX (but not both) can be selected by a strap within the Interface to cause the Terminal to permit the CPU to transmit. Characters must be entered by the Terminal.

Either CR or LF entered at the Terminal can also permit the CPU to transmit if selected within the Interface.

The Terminal regains control of transmission by entering a character at the keyboard. Wait for INDICATOR 1 to go out before sending additional data.

Half Duplex-Blanking Mode

Same information as for Half Duplex-Normal Mode.

Turn-around characters entered by the Terminal also cause Terminal blanking.

CPU transmission must start with SOH or STX, as selected by strap within Interface, to unblank Terminal.

CPU transmission should end with EOT or ETX, as selected by strap within Interface, to blank Terminal.

Half Duplex-Supervisor

CPU controls line turn-around, holding Terminal in transmit mode when CPU is not transmitting.

CPU starts transmission with SOH or STX (as strapped in the Interface) to cause unblanking, and ends it with EOT or ETX (as strapped in Interface) to cause blanking.

Operator can interrupt CPU with BREAK key.

Strap Options

A TTY MASTER OPTION is available on this Interface. Unlike the blanking, unblanking, and turn-around, the TTY MASTER OPTION must be soldered in. All options are contained on the Interface Card and are explained in the Servicing section of this manual.

Baud Rates

The 1800 and 110 baud rates are established by diode packs on the Interface Card. These packs are plug-in type and permit rapid change of baud rates, once the packs are properly loaded with diodes.

The replacement of diodes in the pack controls the baud rate by "programming" a computer circuit. Diode selection for these packs is explained in the Servicing section of this manual.

Switches

FULL DUPLEX/HALF DUPLEX

Mode switch with six positions. Names and operating features are explained under Operating Modes in section 2.

LF/LF-CR

Permits selection of whether LF causes only line feed, or if it causes both line feed and carriage return (LF-CR position). THIS SWITCH HAS NOTHING TO DO WITH TURN-AROUND OR BLANKING.

BAUD RATE, TRANSMIT

Ten-position switch which provides any one of nine internally controlled transmit rates, or permits control by the modem. Two of the switch positions (110, 1800) are factory-assembled to provide the named rate, but can be modified to produce any rate between 75 Hz and 12 kHz. Switch positions are as follows: 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600, EXT.

BAUD RATE, RECEIVE

The receive switch has the same characteristics as the transmit switch.

Installation

Complete installation instructions are given in the Servicing section.

Connections

Connections between the switch panel and the Interface Card are by harmonica connectors. A cable connects the Interface Card to the modem. Connection information is given in the Servicing section.

SPECIFICATION

OPERATING MODES

Full Duplex-Local Copy

This mode permits simultaneous transmission and receipt of data when coupled to a modem having this capability. In addition, the Interface asserts an $\overline{\text{ECHO}}$ signal which causes the Terminal to display keyboard characters on the screen as they are sent to the CPU.

Full Duplex-Normal

With this mode selected, the Terminal is capable of simultaneous transmission and receipt of data. It differs from Local Copy Mode in that the $\overline{\text{ECHO}}$ signal is not applied by the Interface. Keyboard characters must therefore be echoed by the CPU or the modem if they are to be displayed on the Terminal screen. This prevents double letters from being displayed, which would occur if Local Copy Mode were in effect and characters were being echoed.

Full Duplex-Loop Back

Data entered at the Terminal is looped back to the Terminal Control circuits to be executed without being transmitted to the computer. The Terminal is isolated from the modem and from the computer. Data from the computer is looped back to the computer. This mode is beneficial for formatting, programming development, servicing, operator training, etc.

Half Duplex-Normal

Under this condition, the Terminal is capable of receiving or transmitting data, but not simultaneously. Transmitting direction is dependent upon the status of the REQUEST TO SEND (CA) and SECONDARY REQUEST TO SEND (SCA) signals from the Interface, and upon the status of CLEAR TO SEND (CB) signal from the modem. Turn-around is controlled within the Interface. Entering a character at the keyboard raises CA and lowers SCA. When the modem responds with CB, the Terminal transmits. If the transmission is terminated with an EOT or ETX (depending on which one is selected by a strap within the Interface), the Interface lowers CA and raises SCA, permitting the modem to turn the line around and listen to the CPU. Either CR or LF (but not both) can also be sent as a terminating character to cause line turn-around if selected by a strap within the Interface.

The Terminal can control turn-around if the CPU is not sending. No turn-around characters are required from the CPU. INDICATOR 1 on the Terminal keyboard (second red light from left) shows the direction of transmission. Off indicates CLEAR TO SEND. If the light is on and the Terminal is to transmit, enter only one character; then wait for the light to go out before additional characters are entered. Failure to do so may result in loss of data.

As in Local Copy Mode, the $\overline{\text{ECHO}}$ signal is sent from the Interface to the Terminal to permit a local copy of transmitted data.

Half Duplex-Blanking

This mode has all the features of Half Duplex-Normal, plus providing receiver blanking. The turn-around character which ends transmission from the Terminal also causes it to blank its receiving circuits. The CPU must start its transmission with an SOH or STX to cause unblanking before sending other data. If the CPU ends its transmission with EOT or ETX, the receiver circuits again become blanked. Although CR or LF (if selected by a strap) cause trun-around and blanking when sent by the Terminal, they cannot blank the Terminal receiver when sent by the CPU. Again, if INDICATOR 1 is on, enter only one character and wait until the light goes out before proceeding.

Half Duplex-Supervisor

Here, the CPU has full control of line turn-around. The Terminal is held in a transmitting state unless the CPU has data for it. No turn-around or blanking signals need be sent by the Terminal. The CPU starts transmission with an SOH or STX (as strapped in the Interface) to unblank the Terminal receiver. Transmission is ended with EOT or ETX (as strapped in the Interface) to again blank the receiver. If the CPU is transmitting (as indicated by INDICATOR 1), pressing the BREAK key will be accepted at the CPU as a line turn-around request.

During transmission, REC LINE SIG DET (CF) is present. In Terminal transmitting state, SEC REC'D LINE SIG DETECTOR (SCF) signal is also on. The computer indicates its intent to send by causing the SCF line to turn off. Both signals are off for a period of time and the Interface alternately "looks" at the CF line for 200 ms and the SCF line for one second until it finds one of them on; it then remains in this condition until turn-around again occurs.

ELECTRICAL CHARACTERISTICS

Baud Rates, Factory Installed

110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600.

Accuracy

Equal to or better than ±0.1%.

Baud Rates, Modifiable

Baud rates between 75 Hz and 12 kHz can be obtained by modifying the 110 and 1800 baud circuits.

Accuracy

TRANSMIT

Equal to or better than ±0.223%. (±0.223% improves to ±0.1% if no rounding off is required in the calculation which determines diodes to be used. See Baud Rate Modification, Section 3.)

RECEIVE

Equal to or better than ±2.1% at 12 kBaud, decreasing to ±0.125% at 75 baud. (Improves to ±0.1% if no rounding off is required in the calculation which determines diodes to be used. See Baud Rate Modification, Section 3.)

Signal Lines

Conform with RS232-C.

Line Drivers

Nominal Output Voltage: ±8 V

Will Withstand: ±25 V

Line Receivers

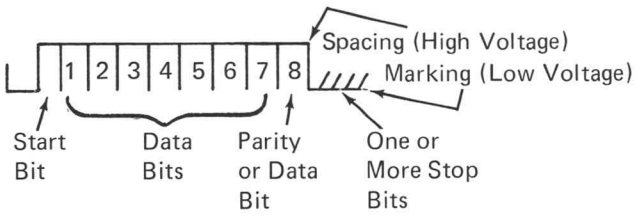
Minimum Input: ±3 V

Resistance: Within 3 kΩ to 7 kΩ

Will Withstand: ±25 V

Data Format

Standard serial data format of one spacing start bit. 8 data bits, one or more marking stop bits.



Break Signal

Continuously adjustable from 15 ms to 200 ms.

Parity Transmission

The 8th bit contains even parity when the Terminal $\overline{\text{SEND 8}}$ signal is false; otherwise bit 8 is transmitted as received by the Terminal bus.

Signal Ground

Connected from the Terminal bus to pin 7 of output connector J261.

Chassis Ground

Connected to the shield of the output cable.

ENVIRONMENTAL CHARACTERISTICS

Conforms with environmental specification for the 4010 Series Terminal. Refer to its specification for details.

SERVICING

Installation Instructions

1. Turn the Terminal off and disconnect the line cord from the power source.

2. Remove the front cover from the Terminal pedestal. (Some Terminals may have a hinged front cover, permitting access without removal.)

3. Remove the four screws which hold the access port plate to the back panel of the pedestal. Remove the plate.

4. The cable which connects to the modem has two connectors on the Terminal end. From the back of the Terminal, insert this end of the cable into the long cable slot near the center of the Pedestal. Put the cable in beyond the end of the insulation and fasten the cable to the sill of the access slot, using a cable clamp.

5. At the inside of the pedestal, slip the cable ground lead lug onto one of the spades available just above the cable access slot.

6. Put the Interface Switch plate in place from the inside of the Pedestal. Insert the four screws from the outside to secure the switch plate in place.

7. Note the two adjacent ten-pin connectors on the switch plate cable. Attach these connectors to the pins near diode packs A1 and A4 on the Interface Card (J360 and J362). Match the index markings on the plugs with those on the card. The first plug should go on the pins nearest diode pack Al (J360).

8. Connect the two-pin connector to the pins between U9 and U10, (J370), again matching the index markings.

9. Place the remaining ten-pin connector on the pins near U16B (J375).

10. Remove the plug from the pins between U9 and U11 on the TC-1 circuit card in the Pedestal. Connect the three-pin connector (on the switch cable) to those pins, locating pin 3 of the plug toward the center of the card.

11. Connect the Terminal connectors on the modem cable (installed in step 4) to the Interface Card near A6 and U7, (J364 and J366) matching the index markings.

12. Install the Interface card in the pedestal minibus connector.

13. Replace the pedestal cover.

14. At the Interface switch panel, select the desired mode, baud rates, and carriage return control.

15. Connect the communication connector to the modem. The Interface is now ready to be put into use.

Refer to Fig. 3-1.

NOTE

Wiring differences may exist between this Interface and certain modems. If necessary, contact your TEKTRONIX Applications Engineer for additional information.

Strap Options

Blanking, unblanking and line turn-around are available by proper strapping on the Interface Card.

Refer to Fig. 3-2.

The SOH-STX OPTION will cause unblanking when the selected character is send by the CPU during Half Duplex-Blanking mode or Half-Duplex-Supervisor mode.

The EOT-ETX OPTION causes line turn-around if the selected character is entered at the Terminal when in Half Duplex-Normal mode or Half Duplex-Blanking mode. This option will also cause blanking when the selected character is entered by either the Terminal or the CPU in Half Duplex-Blanking mode, or by the CPU if in the Half Duplex-Supervisor mode.

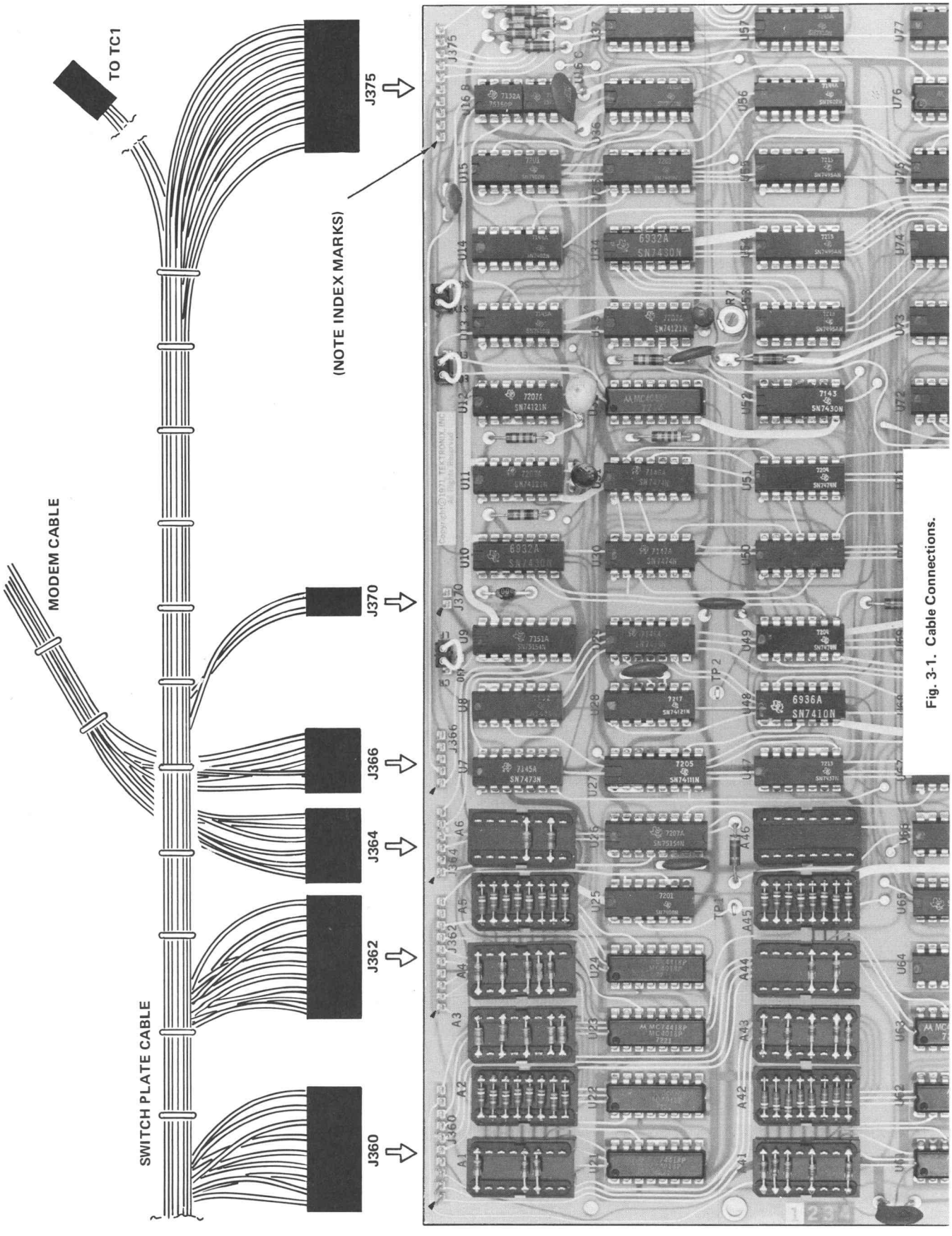


Fig. 3-1. Cable Connections.

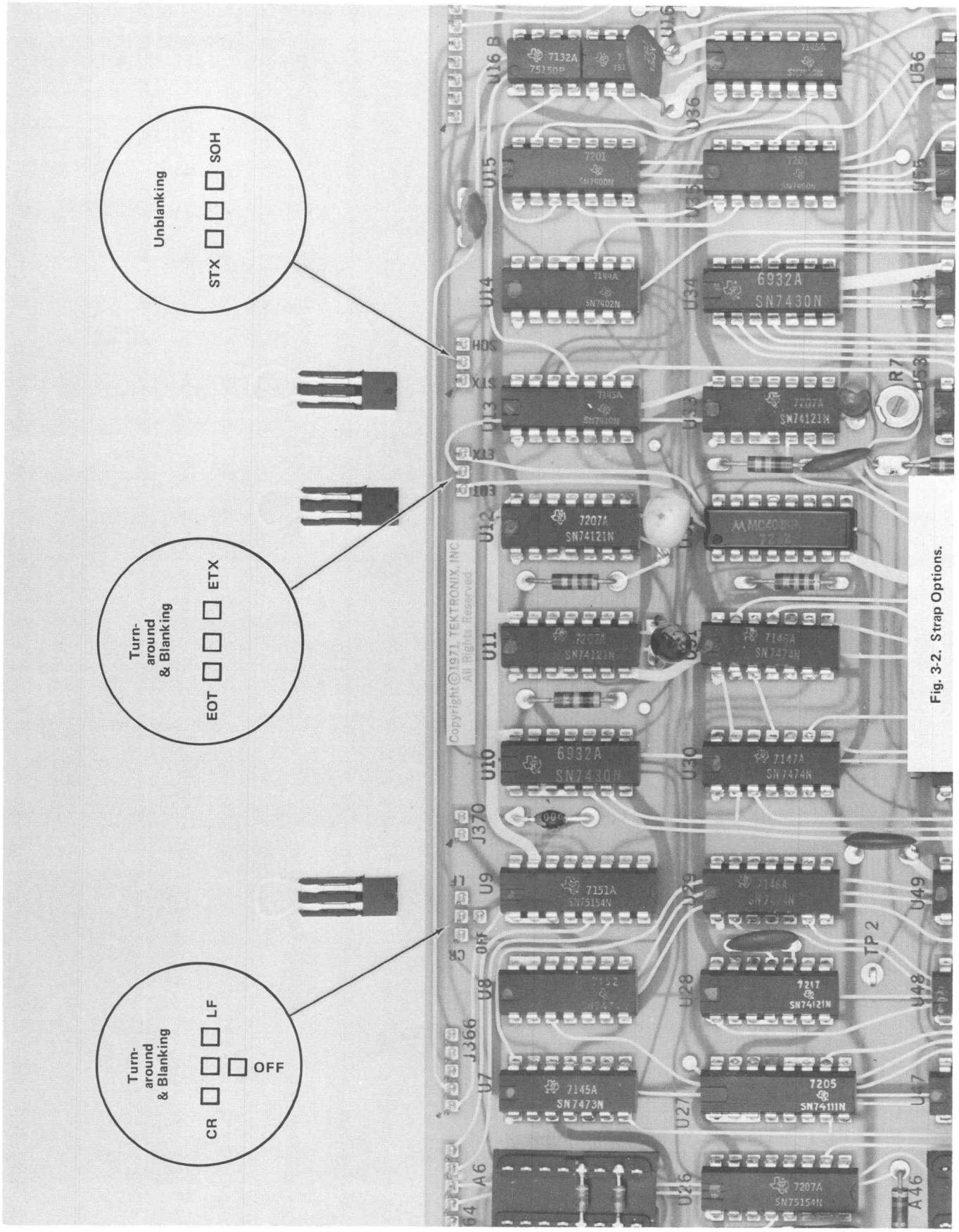


Fig. 3-2. Strap Options.

The CR-LF-OFF OPTION. The selected character entered at the Terminal, causes line turn-around in the Half Duplex-Normal mode. In the Half Duplex-Blanking mode the selected character will cause line turn-around and blanking.

The TTY MASTER OPTION prevents the Interface from outputting data when a low is placed on the appropriate bus line. Unlike the options described above, the TTY MASTER OPTION must be soldered in. Solder a strap from pin 21, 23, 28, 29, or 31 (as appropriate) to pin 13 of U75. Solder holes are provided. (Normal connection is to pin 23.)

Baud Rate Modification

As indicated in Electrical Characteristics the factory installed baud rates are 110 to 9600 in certain steps. It is possible to modify these baud rates by installing the proper diodes. Baud rates between 75 Hz and 12 kHz can be obtained by modifying the 110 and 1800 baud circuits.

There are two switches on the Switch panel, labeled "Transmit" and "Receive". They both have the same characteristics.

The ten position switches permit any one of nine internally controlled rates, and the other position permits control by the modem.

The 110 and 1800 rates are established by the diode packs on the Interface card as follows:

RATE	DIODE PACKS
110 Transmit	A1 and A4
1800 Transmit	A3 and A6
110 Receive	A41 and A44
1800 Receive	A43 and A46

The replacement of diodes in these packs controls the baud rate. The packs are plug-in type to permit rapid change of rate once the packs are properly loaded with diodes. Loading of the diodes requires the use of 16 "bit" numbers. The 16 "bit" location numbers also indicate locations on the diode packs as shown in Fig. 3-3.

The baud rate in these packs is controlled by the placement of diodes in the packs. To illustrate the placement of diodes in the packs, the following examples are given. Once the packs are loaded with the proper diodes, they become plug-in units. The diode pack should be removed from the socket for soldering in the replacement diodes. The new rate should be recorded in the block on the Switch plate.

Transmit Example

a. Determine the Transmit baud rate to be used. In this example, it is assumed that a Transmit Rate of 110 baud is desired.

b. Use the formula OSCILLATOR FREQUENCY ÷ DESIRED TRANSMIT RATE to obtain the first results required in determining diode requirements. (OSCILLATOR FREQUENCY is fixed at 4915200 Hz.) The solution becomes:

$$4915200 \div 110 = 44684_{10}$$

(Note that results are rounded off to nearest unit.)

c. Convert to binary equivalent: $44684_{10} = 1010111010001100_2$

d. Determine which bit locations contain ones, counting from right to left, as illustrated:

Bit Value	1	0	1	0	1	1	1	0	1	0	0	0	1	1	0	0
Bit Location	16		14		12	11	10		8				4	3		

e. The bit locations indicated above show where the diodes should be located on the packs A1 and A4. All diodes should be removed from locations corresponding to zeroes.

Receive Example

a. Determine the receive baud rate to be used. This example assumes that the 1800 baud receive position is to be set up for 1000 baud.

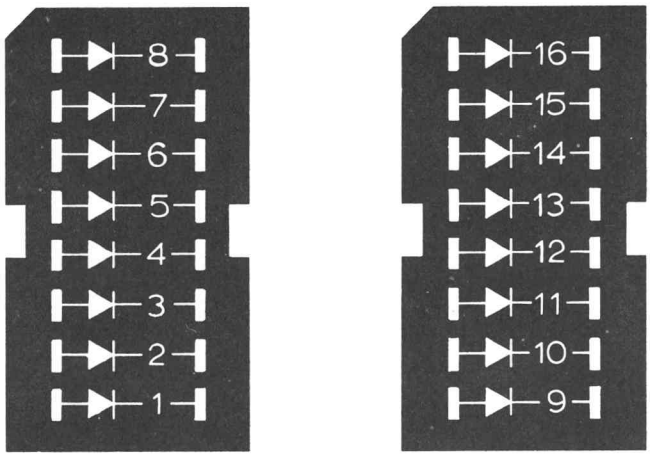


Fig. 3-3. Diode placement.

b. Use the formula OSCILLATOR FREQUENCY ÷ (16 x DESIRED RECEIVE BAUD RATE) to obtain the first results. (OSCILLATOR FREQUENCY is fixed at 4915200 Hz.)

$$4915200 \div (16 \times 1000) = 307_{10}$$

(Again note that rounding off is required.)

c. Convert to binary equivalent:

$$307_{10} = 0000000100110011_2$$

d. Determine which bit locations contain ones, counting from right to left:

Bit Value	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1
Bit Location								9			6	5			2	1

e. Install diodes on A43 and A46 in the diode locations corresponding to a bit value of one as indicated in step d. Remove all other diodes. The diode packs should be removed for soldering.

f. Write 1000 in the block at the 1800 baud position of the receive switch.

Connector Information

P261-Modem Connector

The cable installed in step 4 and connected in step 11 is the modem connector. This connection is external to the Interface.

P261-Modem Connector

Pin	Name
-2	Transmitted Data (BA)
-3	Received Data (BB)
-4	Request To Send (CA)
-5	Clear To Send (CB)
-7	Signal Ground (AB)
-8	Received Line Signal Detector (CF)
-12	Sec. Rec'd Line Sig Detector (SCF)
-15	Transmission Signal Element Timing (DB)
-17	Receiver Signal Element Timing (DD)
-19	Secondary Request To Send (SCA)
-20	Data Terminal Ready (CD)

P360 and P362 on the Interface Card connect to the switch panel. P360 to S5 and P362 to S15.

P364 and P366 on the Interface Card connect to the modem connector (P261).

P370 and P375, also on the Interface Card, connect to the switch panel. P370 to S6 and S15, P375 to S25.

P379 connects from S30 on the switch panel to TC-1 in the Terminal. It is mounted with pin 3 toward board center. Connections are: Pin 1, blank. Pin 2, +5 V or LF to TC-1. Pin 3, LF from TC-1.

Details of the above connectors are available on the Interface schematic diagram and on the connector diagram.

CIRCUIT DESCRIPTION

In full-duplex operation there are three modes provided; Normal, Loop-Back and Local Copy.

Full-Duplex Normal Mode

This mode allows the terminal to communicate with the computer. In this mode the transmitting and receiving circuits are able to operate simultaneously.

First, consider the transmitting circuits. Refer to the schematic diagram. Assume that data is available on Bit 1 through Bit 8 lines and that a CSTROBE occurs. CSTROBE loads the data into output latches U72 and U73. If $\overline{\text{SEND 8}}$ is low, U65C permits BIT 8 to process through to control U65D to determine the polarity of the Bit 8 signal into U73. However, if $\overline{\text{SEND 8}}$ is high, the U65C output is held low and U74 is permitted to control U65D, providing a parity signal as Bit 8. The C STROBE which loaded the data into the latches also goes to U8A. If U8A is receiving a high from computer-suppress gate U69A, the CSTROBE clocks U8A to a one-set condition. This puts a low on the $\overline{\text{CBUSY}}$ line.

If the register is empty, U34 and U35B provide lows to U56A and also send a high to U75B, permitting it to develop a low output. Since U14A is receiving a low on pin 2 from U15D, it sends a high to U69B. Assuming that CLEAR TO SEND is high, U15B sends a high to U69B. This combination applies a high pulse to U53, U54, and U55, thus loading data into these registers. The foregoing action causes the U34A and U35B outputs to go high and the output of U56A to go low. This ends the pulse out of U75B, which in turn ends the pulse out of U14A. The U69B output goes low and permits the registers to go into serial operation. (Note that this also causes U7A to clock one-set.) Assuming that an internal clock position is selected by the Transmit Baud Rate switch, +5 Volts is applied through the switch position and through the selected diodes to program the U21, U22, U23, and U24 count-down devices. The 4.9 MHz clock signal which is applied to these devices counts down by the selected value and generates a clock pulse on the clock bus line, which goes to pin 4 of U25B. Each clock pulse to arrive at that device causes U25A to advance the data bits one position in the registers. The serial output of pin 10 of U53 is applied through U35D, U56D, and U56C to generate transmitted data signals from driver U16B. When the entire character has been clocked through the parallel to serial output shift registers, the U35B and U34A outputs return low, causing U56A's output to go high, to again apply enabling voltage to the SEND INITIATE circuits.

If the Transmit Baud Rate had been at external position, U25B would have been disabled and U25D would have been enabled. This would permit the XMIT SIG EL TIMING signal through U26A to control advancement of data through the Parallel to Serial Shift Registers.

As noted above, when the Load Parallel signal ends, it causes U7A to clock one-set. The next 4.9 MHz pulse causes U8B to one-set, causing a reset signal to go back to U7A, resetting that device to a zero-set condition. The next 4.9 MHz pulse causes U8B to return to its previous zero-set condition. The resultant pulse from U8B causes the SEND INITIATE flip-flop U8A to return zero-set in preparation for the next command.

The diodes which are used to control or program the U21, U22, U23, U25 counters are contained in diode packs A1, A3, A4, and A6. Details regarding these diode packs and how to determine diodes to be used in them are found in Section 3.

Assume that data is to be **received** by the interface, and that the Receive Baud Rate switch is at one of its internal positions. +5 volts is applied through the switch and the appropriate diodes to the U61, U62 and U63 counter circuits. Data from the Receive Data line passes through U26C and is clocked into U66B where the zero output is applied as data to U49A. As long as this is low, it has no effect upon the input registers since all devices in the register are zero-set. When a Start bit arrives it does two things: It applies a high to U49A and it causes U64 to become reset. Subsequent clock pulses cause the Start bit and the accompanying data bits to be clocked into the Data Input Register until a Stop bit is clocked in. U49A, U31A, and U29A then simultaneously apply highs to U48C which sends a low signal to one-shot U28. U28 delivers a negative pulse of approximately 15 microseconds through U48B and U68A to develop the $\overline{\text{CPUNT}}$ signal to prepare the terminal for receiving data. When the signal ends, U27B clocks one-set and its zero output holds the CPUNT signal low. This same output from U27B goes through U47A and U69C to gate the data to the output gates. The output U27B causes U27A to become one-set at the next negative transition of the 614 kHz clock. The zero output of U27A continues the $\overline{\text{CPUNT}}$ signal and the data bit output. It also causes U27B to become zero-set. The one output from U27A generates $\overline{\text{TSTROBE}}$ and also applies a high to U7A. The next negative transition of the 614 kHz clock causes U27A to zero-set and causes U7A to one-set. The output from U7A is processed by U47D to generate a CLEAR signal to clear the input register. With the register cleared the U48C output returns high, the U67C and U52 outputs return low.

If the EXT position had been selected by the Receive Baud Rate switch, U67B would be disabled and U67A enabled. This would permit the REC SIG EL TIMING signal to control the clock inputs to the data input register.

Full Duplex—Loop-Back Mode

In this mode, the Terminal is isolated from the computer. With the Interface control switch in Loop-Back position, transmitted data is routed directly on to the data line and to the input registers. The Interface sends the Terminal output signal back to the Terminal. Data received from the computer is placed on the transmitted data line and sent back out.

Full Duplex—Local Copy Mode

When this mode is selected, operation is essentially the same as explained for Normal, but an ECHO signal is developed. This signal is sent back to the Terminal, permitting the Terminal to process the same data that it is sending out.

There are also three modes provided in Half Duplex operation. They are Normal, Blanking, and Supervisor.

Half Duplex—Normal Mode

This operation uses line-turn-around features to permit the Terminal to either Transmit or to Receive from the computer, regardless of the status of the line when a character is entered at the Terminal and a $\overline{\text{CSTROBE}}$ is developed. $\overline{\text{CSTROBE}}$ passes passes through U47C and one-sets flip-flop U8A. The high into U75B causes the output register to load as previously explained. The high from U8A also generates the $\overline{\text{CBUSY}}$ signal. In addition to this, the high into U36A causes a low from that device to ensure that the U15D-U36B flip-flop is set with the U15D output low. This does several things. It causes U17A to develop a REQUEST TO SEND signal. It causes TRANSMIT SUPERVISOR to be low by way of U15A and U16A. It causes the Receive Seek Timer U11A to be disabled. As soon as the interface responds with a CLEAR TO SEND signal, transmission occurs just as was explained for Full Duplex-Normal operation. When the Terminal transmits either an EOT or ETX, depending upon which one is selected by the strap option, or an LF or CR if one of these two is selected by strap option, it is detected by U32A and either U35C or U36C. This detection occurs because all data being transmitted is echoed back into the data input register by the Modem. When one of the specified characters is detected, U69D develops a low output which creates a high out of U13C and a low out of U14D.

This low causes U15D to generate a high output and U36B to develop a low output. The high from U15D disables U14A and causes U17 to put a low on the REQUEST TO SEND line. It also causes the TRANSMIT SUPERVISOR signal to go high. The low from U36B disables U36C to prevent LF or CR from affecting this circuit when received from the computer. No turn-around is required when the computer starts transmitting, since the Terminal is already listening. No turn-around is required when the computer finishes transmitting, since simply entering a keyboard character at the Terminal automatically causes line turn-around to permit the Terminal to transmit to the computer.

Half Duplex—Blanking Mode

Operation in this mode is very similar to that described for Half Duplex-Normal. The difference is that when the Terminal has finished transmitting, it can blank the receiver circuits with the same signal as used for line turn-around. When the computer starts transmitting, it must precede its data with an unblanking signal. When blanking is selected, U37B applies a high to the blanking flip-flop U76A and releases it for operation when the Terminal finishes transmission and sends EOT or ETX or an LF or CR, U69D sends a low to U13C which applies a high to U14D. The high being applied to U14D causes a low on U76A and causes it to become zero-set. The one output of U76A applies a low to U57B, causing it to place a high on U56B. This high on U56B places a low on the TSTROBE and CPUNT gates U68B and U68A. With these two gates disabled, the Terminal is unable to receive data, even though it may be loaded into the Data Input Register. However, if the first character sent by the computer is either SOH or STX (depending upon which is strapped into the Interface), this character is detected by U32A and U15C. The resulting high pulse from U75A causes U76A to become one-set. With this device one-set, the low is removed from U57B and this permits U68B and U68A to develop strobes to accept data. If the computer ends its transmission with an EOT or EXT, depending upon which is strapped in the Interface, U35C sends a low to U69D which causes U13C and U14D to zero-set U76A, and again blank the receiver.

Half Duplex—Supervisor Mode

In this mode, the computer takes charge of line turn-around. Blanking or turn-around is not affected by characters from the Terminal. However, blanking and turn-around can be controlled by signals from the computer. In the supervisor position, the selected low on that input is inverted by U37A, placing a high on Transmit Seek Gate U13B and on Supervisor Transmit Gate U37C. The high is also applied to Receive Seek Gate U13A. The one of principal convern here is the Supervisor Transmit Gate U37C, which holds a disabling low on U10 during Transmit operation. Data being echoed back into the input registers is prevented from causing an output of U32C through this device. When the Terminal transmits, U15D has its output low and the Request to Send line high. When the computer

wants to transmit it causes the DATA CARRIER and RECEIVE SUPERVISOR lines to go low. A data carrier low causes a high to be placed on the Receive Seek Gate U13A and the Receive Supervisor signal causes a high to be placed on Transmit Seek Gate U13B. U13B is thus receiving three highs and causes a low output. This low output causes a high from U13C, causing a low from U14D, which causes U15D to generate a high output. This sends the U36B output low, making the U37C output high, enabling the control character detect circuits. The U15D output going high causes a short pulse out of the Receive Timing one-shot U11. The output of U11 goes low, and at the end of the time interval returns high, causing U13A to send a low signal to U36B. This causes U15D to generate a low signal, which causes U12 to develop a one-second low output at its zero out, and allows U13B to send a high to U13C. When the U12 pulse ends, it applies another low to U13C, causing it to send a low to U15D to again reset the U15D-U36B flip-flop. This sequence occurs back and forth until such time as either RECEIVE SUPERVISOR or DATA CARRIER signal goes high. Assume that the DATA CARRIER signal goes high. The output of U9A is low, inhibiting the U13A gate. With U13A inhibited, U36B cannot cause U15D to generate a low output, and the interface is thus held in a Receiving mode. Although the Interface is in a Receiving mode, it remains blanked until either an SOH or an STX is detected by U32 and U15C. When this happens, U15C sends a low to U75A which applies a high pulse to U76A and causes the Blanking flip-flop to become one-set and unblank the circuit. When a computer is through transmitting it terminates its transmission with either an EOT or an ETX which again causes the Terminal to become blanked. With the Data Carrier signal removed the U11 and U12 one shots again resume their one-second transmit seeking, 200-millisecond receive seeking time cycles. Let's now assume that the Terminal is to be placed in Transmit Mode by the computer. It indicates this by causing the RECEIVE SUPERVISE line to go high. When this occurs, the low from U9C inhibits U13B. As soon as the RECEIVE SEEK TIMER U11 finishes its Clock pulse and returns high, it causes U13A to deliver a low to U36B. This causes the U15D output to go low, placing the Terminal in a Transmit status.

This Interface controls one of the indicator lights on the keyboard. At any time the CLEAR TO SEND signal is high, the low from U9A causes a high out from U77B and that indicator is off. However, when the CLEAR TO SEND signal goes low, the high from U9A causes U77B to turn on the INDICATOR 1, as long as the Terminal is not in Local operation.

ELECTRICAL PARTS LIST

Replacement parts should be ordered from the Tektronix Field Office or Representative in your area. Changes to Tektronix products give you the benefit of improved circuits and components. Please include the instrument type number and serial number with each order for parts or service.

ABBREVIATIONS AND REFERENCE DESIGNATORS

A	Assembly, separable or repairable	FL	Filter	PTM	paper or plastic, tubular molded
AT	Attenuator, fixed or variable	H	Heat dissipating device (heat sink, etc.)	R	Resistor, fixed or variable
B	Motor	HR	Heater	RT	Thermistor
BT	Battery	J	Connector, stationary portion	S	Switch
C	Capacitor, fixed or variable	K	Relay	T	Transformer
Cer	Ceramic	L	Inductor, fixed or variable	TP	Test point
CR	Diode, signal or rectifier	LR	Inductor/resistor combination	U	Assembly, inseparable or non-repairable
CRT	cathode-ray tube	M	Meter	V	Electron tube
DL	Delay line	Q	Transistor or silicon-controlled rectifier	Var	Variable
DS	Indicating device (lamp)	P	Connector, movable portion	VR	Voltage regulator (zener diode, etc.)
Elect.	Electrolytic	PMC	Paper, metal cased	WW	wire-wound
EMC	electrolytic, metal cased	PT	paper, tubular	Y	Crystal
EMT	electrolytic, metal tubular				
F	Fuse				

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
SWITCHES				
S5	260-1251-01			Rotary RECEIVE
S15	260-1251-01			Rotary TRANSMIT
S25	260-1434-00			Rotary DUPLEX
S30	260-0960-00			Slide LF—LF→CR
ASSEMBLY				
	670-2194-00			OPTIONAL COMMUNICATION Circuit Card Assembly
DIODE PACKS				
A1	152-0141-02			Silicon, 1N4152 (Qty 3)
A3	152-0141-02			Silicon, 1N4152 (Qty 5)
A4	152-0141-02			Silicon, 1N4152 (Qty 5)
A6	152-0141-02			Silicon, 1N4152 (Qty 2)
A41	152-0141-02			Silicon, 1N4152 (Qty 5)
A43	152-0141-02			Silicon, 1N4152 (Qty 5)
A44	152-0141-02			Silicon, 1N4152 (Qty 2)
A46	152-0141-02			Silicon, 1N4152 (Qty 0)
RESISTOR PACKS				
A2	317-0391-00			390 Ω, 1/8 W, 5% (Qty 8)
A5	317-0391-00			390 Ω, 1/8 W, 5% (Qty 8)
A42	317-0391-00			390 Ω, 1/8 W, 5% (Qty 8)
A45	317-0391-00			390 Ω, 1/8 W, 5% (Qty 8)

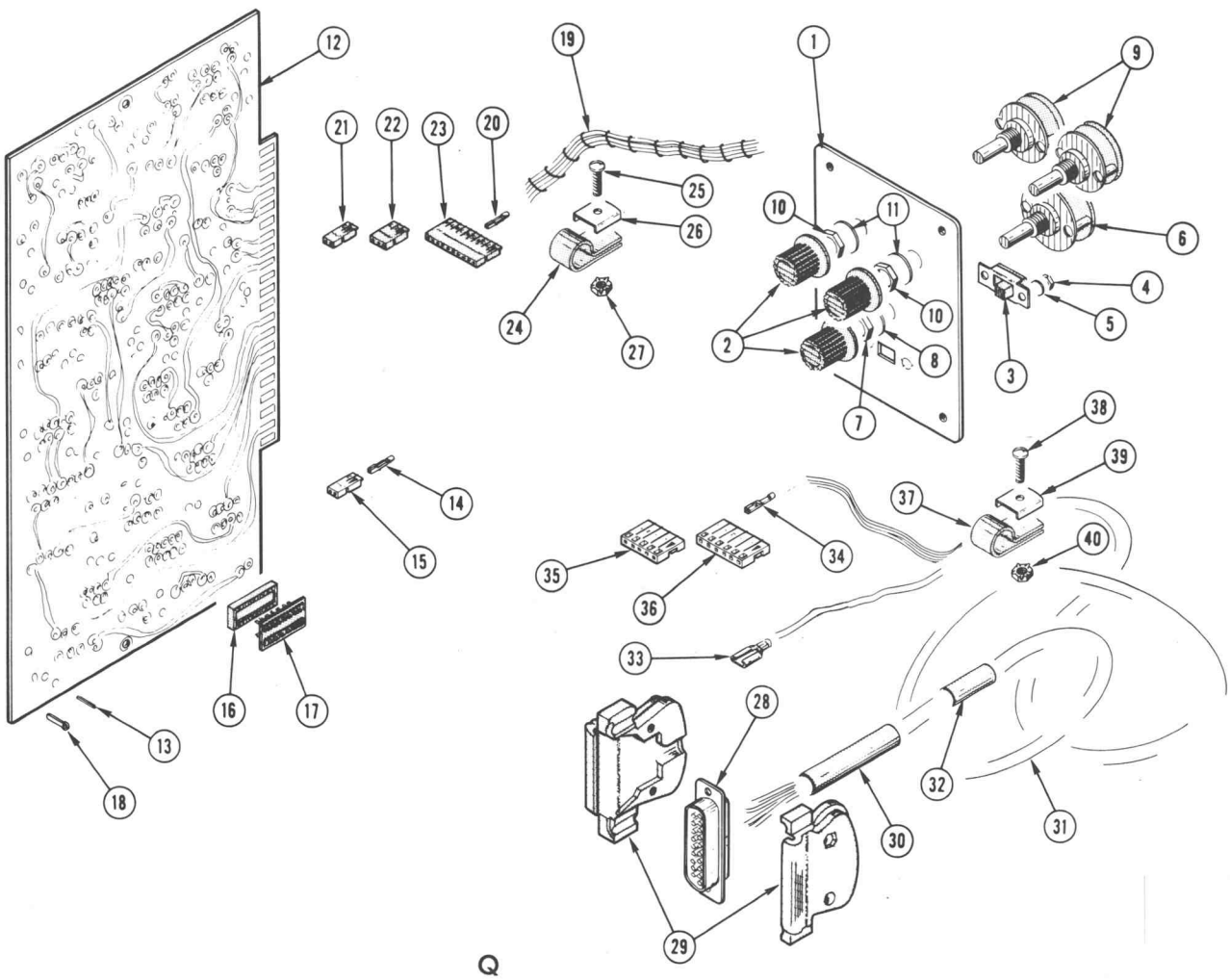
ELECTRICAL PARTS LIST (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
CAPACITORS				
C1	283-0003-00			0.01 μF, Cer, 150 V, +80%-20%
C7	290-0536-00			10 μF, Elect., 25 V, ±20%
C25	290-0536-00			10 μF, Elect., 25 V, ±20%
C30	290-0529-00			47 μF, Elect., 20 V, ±20%
C35	283-0000-00			0.001 μF, Cer, 500 V, +100%-0%
C38	283-0003-00			0.01 μF, Cer, 150 V, +80%-20%
C40	283-0114-00			0.0015 μF, Cer, 200 V, ±5%
C50	283-0003-00			0.01 μF, Cer, 150 V, ±80%-20%
C51	283-0003-00			0.01 μF, Cer, 150 V, +80%-20%
C52	283-0003-00			0.01 μF, Cer, 150 V, +80%-20%
C53	283-0003-00			0.01 μF, Cer, 150 V, +80%-20%
C54	283-0003-00			0.01 μF, Cer, 150 V, +80%-20%
DIODES				
CR20	152-0066-00			Silicon, 1N3194
VR78	152-0278-00			Zener, 1N4372A, 0.4 W, 3 V, 5%
VR79	152-0278-00			Zener, 1N4372A, 0.4 W, 3 V, 5%
RESISTORS				
R1	315-0105-00			1 MΩ, 1/4 W, 5%
R3	315-0103-00			10 kΩ, 1/4 W, 5%
R5	315-0433-00			43 kΩ, 1/4 W, 5%
R7	311-0614-00			30 kΩ, Var
R10	315-0472-00			4.7 kΩ, 1/4 W, 5%
R12	315-0472-00			4.7 kΩ, 1/4 W, 5%
R14	315-0472-00			4.7 kΩ, 1/4 W, 5%
R16	315-0472-00			4.7 kΩ, 1/4 W, 5%
R18	315-0472-00			4.7 kΩ, 1/4 W, 5%
R20	315-0472-00			4.7 kΩ, 1/4 W, 5%
R25	315-0303-00			30 kΩ, 1/4 W, 5%
R30	315-0363-00			36 kΩ, 1/4 W, 5%
R40	315-0221-00			220 Ω, 1/4 W, 5%
R50	315-0472-00			4.7 kΩ, 1/4 W, 5%
INTEGRATED CIRCUITS				
U7	156-0039-00			Dual 15 MHz J-K master-slave flip-flop, SN7473N
U8	156-0041-00			Dual 2-bit bistable latch, SN7474N
U9	156-0138-00			Quad line receiver--TTL compatable, SN75154N
U10	156-0035-00			Single 8-input positive nand gate, SN7430N
U11	156-0072-00			Single monostable multivibrator-one shot, SN74121N
U12	156-0072-00			Single monostable multivibrator-one shot, SN74121N

ELECTRICAL PARTS LIST (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U13	156-0047-00			Triple 3-input positive nand gate, SN7410N
U14	156-0043-00			Quad 2-input positive nor gate, SN7402N
U15	156-0030-00			Quad 2-input positive nand gate, SN7400N
U16	156-0139-00			Dual line driver--TTL compatable, SN75150P
U17	156-0139-00			Dual line driver--TTL compatable, SN75150P
U21	156-0202-00			Single 8 MHz 4-bit modulo-N ripple counter, MC4018P
U22	156-0202-00			Single 8 MHz 4-bit modulo-N ripple counter, MC4018P
U23	156-0202-00			Single 8 MHz 4-bit modulo-N ripple counter, MC4018P
U24	156-0202-00			Single 8 MHz 4-bit modulo-N ripple counter, MC4018P
U25	156-0030-00			Quad 2-input positive nand gate, SN7400N
U26	156-0138-00			Quad line receiver--TTL compatable, SN75154N
U27	156-0174-00			Dual 20 MHz J-K master-slave flip-flop, SN74111N
U28	156-0072-00			Single monostable multivibrator-one shot, SN74121N
U29	156-0041-00			Dual 2-bit bistable latch, SN7474N
U30	156-0041-00			Dual 2-bit bistable latch, SN7474N
U31	156-0041-00			Dual 2-bit bistable latch, SN7474N
U32	156-0159-00			Single one-of-eight decoder, MC4048P
U33	156-0072-00			Single monostable multivibrator-one shot, SN74121N
U34	156-0035-00			Single 8-input positive nand gate, SN7430N
U35	156-0030-00			Quad 2-input positive nand gate, SN7400N
U36	156-0047-00			Triple 3-input positive nand gate, SN7410N
U37	156-0030-00			Quad 2-input positive nand gate, SN7400N
U47	156-0150-00			Quad 2-input positive nand buffer, SN7437N
U48	156-0047-00			Triple 3-input positive nand gate, SN7410N
U49	156-0041-00			Dual 2-bit bistable latch, SN7474N
U50	156-0041-00			Dual 2-bit bistable latch, SN7474N
U51	156-0041-00			Dual 2-bit bistable latch, SN7474N
U52	156-0035-00			Single 8-input positive nand gate, SN7430N
U53	156-0120-00			Single 4-bit right/left shift register, SN7495N
U54	156-0120-00			Single 4-bit right/left shift register, SN7495N
U55	156-0120-00			Single 4-bit right/left shift register, SN7495N
U56	156-0043-00			Quad 2-input positive nor gate, SN7402N
U57	156-0047-00			Triple 3-input positive nand gate, SN7410N
U61	156-0202-00			Single 8 MHz 4-bit modulo-N ripple counter, MC4018P
U62	156-0202-00			Single 8 MHz 4-bit modulo-N ripple counter, MC4018P
U63	156-0202-00			Single 8 MHz 4-bit modulo-N ripple counter, MC4018P
U64	156-0032-00			Single 10 MHz 1-&-3 bit binary ripple counter, SN7493N
U65	156-0043-00			Quad 2-input positive nor gate, SN7402N
U66	156-0041-00			Dual 2-bit bistable latch, SN7474N
U67	156-0030-00			Quad 2-input positive nand gate, SN7400N
U68	156-0145-00			Quad 2-input positive nand buffer, SN7438N
U69	156-0129-00			Quad 2-input positive and gate, SN7408N
U70	156-0145-00			Quad 2-input positive nand buffer, SN7438N
U71	156-0145-00			Quad 2-input positive nand buffer, SN7438N
U72	156-0040-00			Dual 2-bit bistable latch, SN7475N
U73	156-0040-00			Dual 2-bit bistable latch, SN7475N
U74	156-0088-00			Single 8-bit parity generator/checker, SN74180N
U75	156-0030-00			Quad 2-input positive nand gate, SN7400N
U76	156-0042-00			Dual 15 MHz J-K master-slave flip-flop, SN7476N
U77	156-0144-00			Triple 3-input positive nand gate, SN7412N

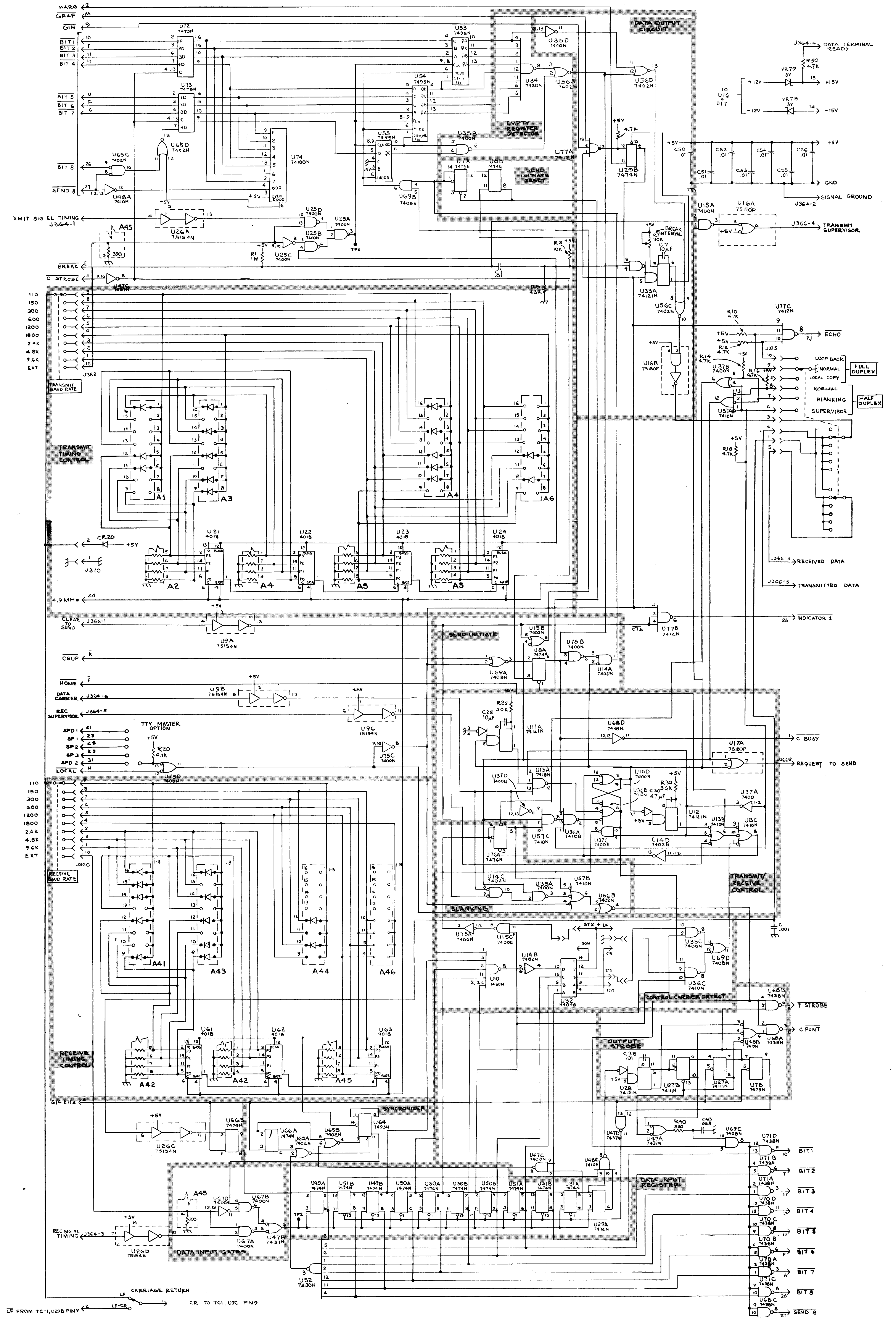
MECHANICAL PARTS LIST



Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description
	021-0074-00			1	INTERFACE--OPTIONAL DATA COMMUNICATIONS
	- - - - - -			-	interface includes:
1	386-2231-00			1	PANEL, rear
2	366-1024-00			3	KNOB, gray--TRANSMIT-RECEIVE-DUPLEX
	- - - - - -			-	each knob includes:
	213-0153-00			2	SETSCREW, 5-40 x 0.125 inch
3	260-0960-00			1	SWITCH, slide--LF-LF→CR
	- - - - - -			-	mounting hardware: (not included w/switch)
4	210-0405-00			2	NUT, hex., 2-56 x 0.187 inch
5	210-0001-00			2	WASHER, lock, internal, #2
6	260-1434-00			1	SWITCH, rotary--DUPLEX
	- - - - - -			-	mounting hardware: (not included w/switch)
7	210-0590-00			1	NUT, hex., 0.375 x 0.438 inch
8	210-0978-00			1	WASHER, flat, 0.375 ID x 0.50 inch OD

Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description
9	260-1251-01			2	SWITCH, rotary--TRANSMIT-RECEIVE
	- - - - - -			-	mounting hardware for each: (not included w/switch)
10	210-0590-00			1	NUT, hex., 0.375 x 0.438 inch
11	210-0978-00			1	WASHER, flat, 0.375 ID x 0.50 inch OD
12	- - - - - -[1]			1	CIRCUIT CARD ASSEMBLY-OPTIONAL COMMUNICATION
	- - - - - -			-	circuit card assembly includes:
13	131-0608-00			53	TERMINAL, pin, 0.365 inch long
	131-0993-00			3	LINK, terminal connecting
	- - - - - -			-	each link includes:
14	131-0707-00			2	CONNECTOR, terminal
15	352-0169-00			1	HOLDER, terminal connector, 2 wire (black)
16	136-0260-01			8	SOCKET, integrated circuit, 16 pin
17	136-0503-00			12	SOCKET, interconnect, 16 pin, DIP
18	214-0579-00			2	PIN, test point
19	179-1816-00			1	WIRING HARNESS, main
	- - - - - -			-	wiring harness includes:
20	131-0707-00			33	CONNECTOR, terminal
21	352-0169-00			1	HOLDER, terminal connector, 2 wire (black)
22	352-0161-00			1	HOLDER, terminal connector, 3 wire (black)
23	352-0168-00			3	HOLDER, terminal connector, 10 wire (black)
24	343-0003-00			1	CLAMP, cable, plastic, 0.25 inch diameter
	- - - - - -			-	mounting hardware: (not included w/clamp)
25	211-0638-00			1	SCREW, 6-32 x 0.738 inch, THS
26	210-0863-00			1	WASHER, loop clamp
27	210-0457-00			1	NUT, keps, 6-32 x 0.312 inch
	012-0400-00			1	CABLE, interface, 16 feet long
	- - - - - -			-	cable includes:
28	131-0570-00			1	CONNECTOR, receptacle, electrical, 25 pin, male
29	200-1055-00			1	COVER, connector, plastic
30	200-0192-00			1	COVER, rubber, strain relief
31	175-1081-00			ft	CABLE, special purpose, electrical, 16 feet
32	334-1941-00			1	SLEEVE, marker, cable
33	131-1159-00			1	CONNECTOR, receptacle, electrical
34	131-0707-00			11	CONNECTOR, terminal
35	352-0163-00			1	HOLDER, terminal connector, 5 wire (black)
36	352-0164-00			1	HOLDER, terminal connector, 6 wire (black)
37	343-0003-00			1	CLAMP, cable, plastic, 0.25 inch diameter
	- - - - - -			-	mounting hardware: (not included w/clamp)
38	211-0511-00			1	SCREW, 6-32 x 0.50 inch, PHS
39	210-0863-00			1	WASHER, loop clamp
40	210-0457-00			1	NUT, keps, 6-32 x 0.312 inch
					ACCESSORIES
	070-1379-00			1	MANUAL, instruction (not shown)
	020-0066-00			4	OPTIONAL BAUD DIODE PACK (not shown)
	- - - - - -			-	each optional baud diode pack includes:
	136-0503-00			1	SOCKET, interconnect, 16 pin, DIP
	152-0141-02			8	DIODE, silicon, replaceable by 1N4152

[1]Refer to Electrical Parts List for part number.



021-0074-00
(4010 SERIES)

OPTIONAL DATA COMMUNICATION INTERFACE

Ⓐ

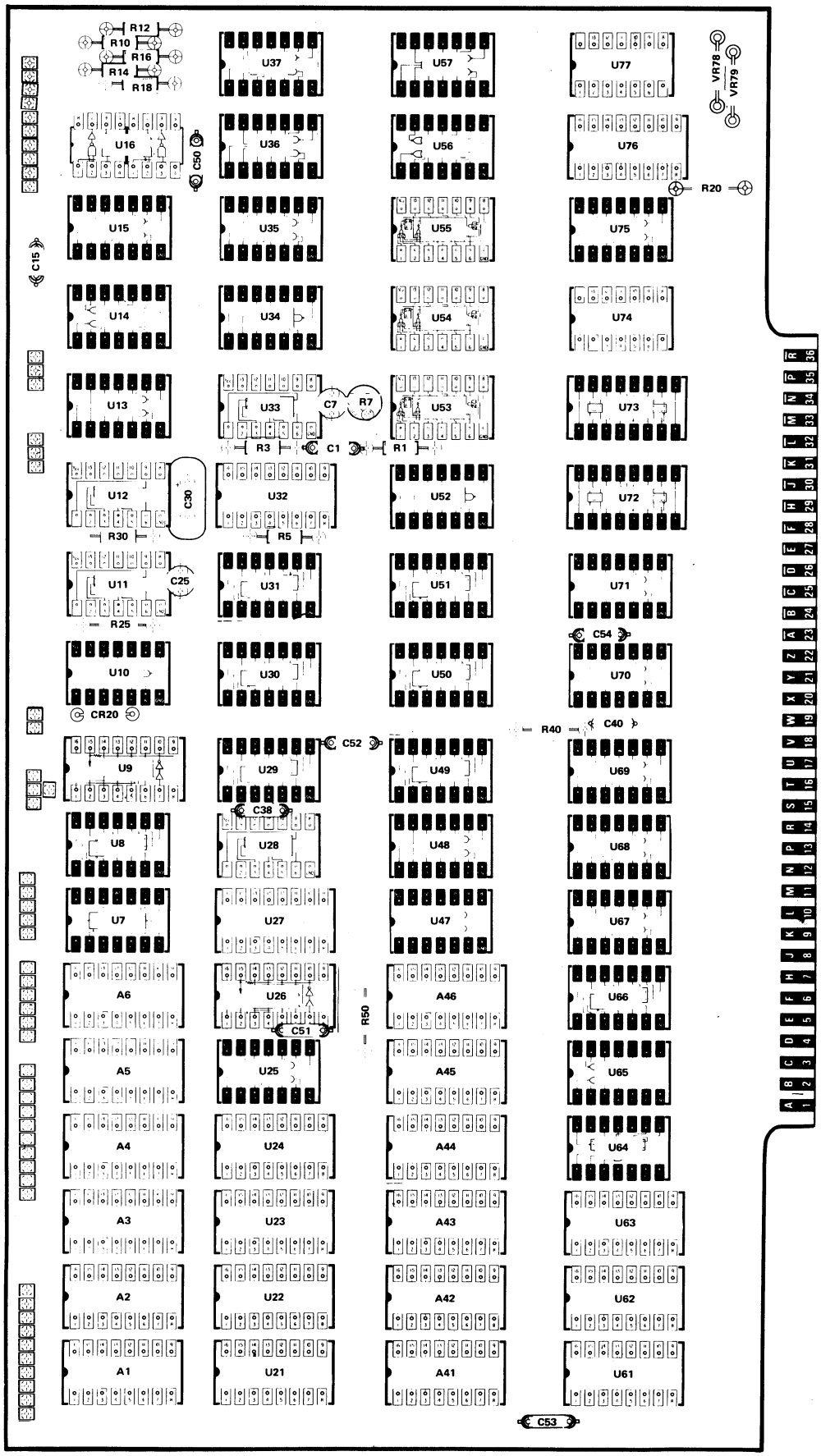
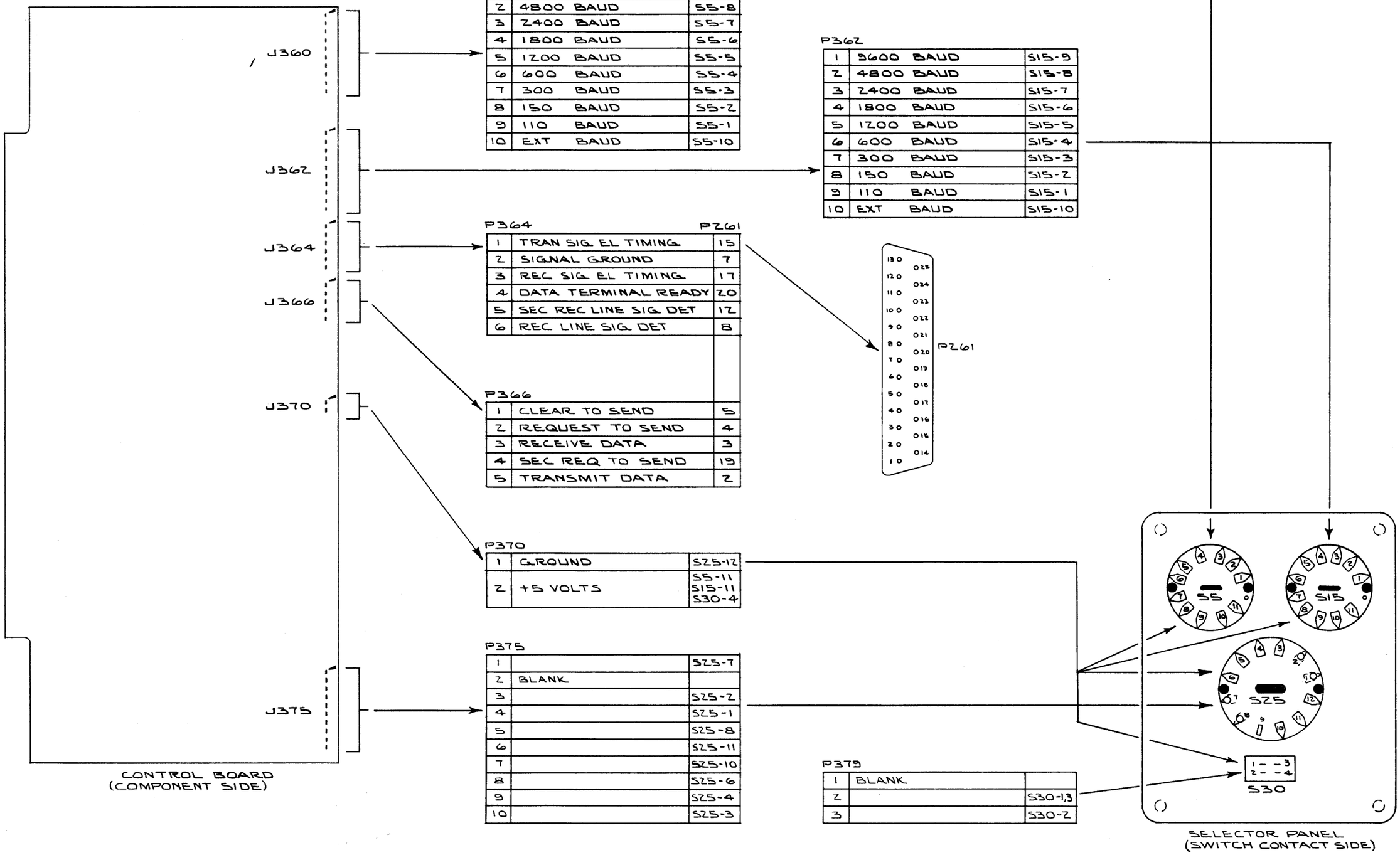


Fig. 7-1. Component locations.



021-0074-00

Ⓐ

OPTIONAL DATA COMMUNICATION
INTERFACE CONNECTORS

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Sections of the manual are often printed at different times, so some of the information on the change pages may already be in your manual. Since the change information sheets are carried in the manual until ALL changes are permanently entered, some duplication may occur. If no such change pages appear in this section, your manual is correct as printed.

TEXT CORRECTIONS

SECTION 2 SPECIFICATION

Page 2-1 Paragraph 5, line 3

DELETE: (second red light from left)

SECTION 3 SERVICING

Page 3-1 Right column

ADD to Note the following information:

If the interface is used in an environment in which the Supervisory channels are used, check compatibility with the Modem.

This device is wired to provide TRANSMIT SUPERVISOR on Pin 19 and RECEIVE SUPERVISOR on Pin 12. It may be necessary to move wires in the cable plug to achieve compatibility.

If the interface is used in an environment where the supervisory channels are used but the blanking convention is not followed, (see page 3-1) cut and lift pin 4 of U37 and connect +5 volts to the lifted leg of U37. (Pin 4)

Page 3-4 Fig. 3-3

ADD: Under left figure (diodes 1 through 8)
A1, A41, A3, A43

ADD: Under right figure (diodes 9 through 16)
A4, A44, A6, A46

Page 3-5 Connector Information

Paragraph 4, Line 2

CHANGE: S6 to S5

SECTION 4 CIRCUIT DESCRIPTION

Page 4-1 Full-Duplex Normal Mode

Paragraph 3, Lines 8 and 26

CHANGE: U34A to U34.

Paragraph 6, Line 2

CHANGE: U25 to U24

Paragraph 7, Lines 27, 28 and 29

CHANGE: U7A to U7B

Paragraph 7, Line 30

DELETE: CLEAR

Page 4-2 Half Duplex - Normal Mode

Paragraph 1, Line 20

CHANGE: U32A to U32

Paragraph 2, Line 3

CHANGE: U17 to U17A

Page 4-2 Half Duplex - Blanking Mode

Paragraph 1, Line 8

ADD: Period after word "operation" and capital "W" for next word (When).

Paragraph 1, Line 20

CHANGE: U32A to U32

Page 4-3 Half Duplex Supervisor Mode

Left column, Line 23

CHANGE: U9A to U9B

SCHEMATIC CORRECTIONS

TRANSMIT TIMING CONTROL: U22

CHANGE: A4 to A2

TRANSMIT RECEIVE CONTROL

CHANGE: U11A to U11

CONTROL CARRIER DETECT

ADD: Circle to pin 11 of U69D