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MANUAL CHANGE INFORMATION

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Product: 12RM99 OPT. 03 8031 Manual Part No. 070-6160-00

Mnemonics ROM Pack DESCRIPTION

THIS IS A PAGE PULL AND REPLACEMENT PACKAGE FOR THE 12RM99 OPTION 03 8031 MNEMONICS ROM PACK INSTRUCTIONS MANUAL

1. Remove the designated pages from your manual and insert the following pages 3, 4, 7, 8, 19, and 20.
2. Keep this cover sheet in the Change Information section at the back of your manual for a permanent record.

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CONNECTING TO THE MICROPROCESSOR

CONNECTION OVERVIEW

Table 1 provides an overview of the connections between the 1240 Logic Analyzer equipped with an 8031 Mnemonics ROM Pack and your 8031 microprocessor.

NOTE

Be sure to connect a USER'S GND lead from each acquisition probe to the microprocessor ground. Otherwise, invalid data may be acquired.

NOTE

To ensure proper operation, verify the connections shown in Table 1.

Table 1
1240 SCREEN TO 8031 SIGNAL MAP

1240 SCREEN			CONNECTIONS		8031	
GROUP	BIT	C/Q	POD*	CHAN	SIGNAL	PIN
CNTL	7	-	2	7	RST	9
	6	-	2	6	$\overline{EA}$	31
	5	-	2	5	P3.2/INT0	12
	4	-	2	4	P3.3/INT1	13
	3	-	2	3	P3.7/RD	17
	2	-	2	2	P3.6/WR	16
	1	-	2	1	PSEN	29
	0	-	2	0	ALE	30
ADDR	15	-	3	7	$P2.7/A_{15}$	28
	14	-	3	6	$P2.6/A_{14}$	27
	13	-	3	5	$P2.5/A_{13}$	26
	12	-	3	4	$P2.4/A_{12}$	25
	11	-	3	3	$P2.3/A_{11}$	24
	10	-	3	2	$P2.2/A_{10}$	23
	9	-	3	1	$P2.1/A_9$	22
	8	-	3	0	$P2.0/A_8$	21
	7	-	0	7	$P0.7/AD_7$	32
	6	-	0	6	$P0.6/AD_6$	33
	5	-	0	5	$P0.5/AD_5$	34
	4	-	0	4	$P0.4/AD_4$	35
	3	-	0	3	$P0.3/AD_3$	36
	2	-	0	2	$P0.2/AD_2$	37
	1	-	0	1	$P0.1/AD_1$	38
	0	-	0	0	$P0.0/AD_0$	39
DATA	7	-	1	7	$P0.7/AD_7$	32
	6	-	1	6	$P0.6/AD_6$	33
	5	-	1	5	$P0.5/AD_5$	34
	4	-	1	4	$P0.4/AD_4$	35
	3	-	1	3	$P0.3/AD_3$	36
	2	-	1	2	$P0.2/AD_2$	37
	1	-	1	1	$P0.1/AD_1$	38
	0	-	1	0	$P0.0/AD_0$	39
(none)	-	P3	3	C/Q	PSEN	29
	-	P2	2	C/Q	P3.6/WR	16
	-	P1	1	C/Q	P3.7/RD	17
	-	P0	0	C/Q	ALE	30

* Pod numbers are shown for a 1240 with a total of two acquisition cards installed. For each additional acquisition card installed, add 2 to the pod numbers given.

MODIFYING A UPIK40 OR DAS 9100 PROBE INTERFACE

If you purchase a 40-pin Universal Probe Interface Kit (UPIK40), it should be labeled so the connections correspond to the information shown in Table 2. You should label the lead sets in the UPIK40 with pod numbers appropriate to your 1240.

The connections shown below are the same (with the following exceptions) as for the DAS 9100 8031-configured probe interface, 91TM07 Option 01 (order part numbers 015-0015-00 and 012-1065-00). If you order these part numbers, the clock wiring must be changed to correspond to the information shown in Tables 1 and 2. If you use the DAS 9100 probe interface, you should re-label the lead sets with the pod numbers appropriate to your 1240 pod and lead assignments (Pod 1A = Pod 0, Pod 1B = Pod 1, Pod 1C = Pod 2, Pod 2A = Pod 3). Add two to the pod number for each additional acquisition card installed.

NOTE

Be sure to connect a USER'S GND lead from each acquisition probe to the microprocessor ground. Otherwise, invalid data may be acquired.

To ensure proper operation, verify the connections shown in Table 2.

Table 2
PROBE INTERFACE CONNECTIONS*

1			40
2		Pod 0 - black	39
3		Pod 0 - brown	38
4		Pod 0 - red	37
5		Pod 0 - orange	36
6		Pod 0 - yellow	35
7		Pod 0 - green	34
8		Pod 0 - blue	33
9	Pod 2 - violet	Pod 0 - violet	32
10		Pod 2 - blue	31
11		Pod 0 - white; Pod 2 - black	30
12	Pod 2 - green	Pod 3 - white; Pod 2 - brown	29
13	Pod 2 - yellow	Pod 3 - violet	28
14		Pod 3 - blue	27
15		Pod 3 - green	26
16	Pod 2 - white; Pod 2 - red	Pod 3 - yellow	25
17	Pod 1 - white: Pod 2 - orange	Pod 3 - orange	24
18		Pod 3 - red	23
19		Pod 3 - brown	22
20	Grounds	Pod 3 - black	21

*Pod numbers are shown for a 1240 with a total of two acquisition cards installed. For each additional card installed, add 2 to the pod numbers given. Connections are shown from the wire-insertion side of the male-to-female harmonica adapter.

DATA QUALIFICATION AND TRIGGERING

IDENTIFYING CYCLE TYPES

To use either the Global or Sequential Event Recognizers effectively, you need to be able to identify cycle types. Table 3 gives the names of the signals in the CNTL group.

Table 3
CNTL GROUP SIGNALS

CHAN.	SIGNAL NAME
7	RST
6	$\overline{EA}$
5	P3.2/INT0
4	P3.3/INT1
3	P3.7/RD
2	P3.6/WR
1	PSEN
0	ALE

The 8031 microprocessor has two different methods of indicating processor cycle types: *alternate mode* and *standard mode*. The mode the processor is operating in will determine how the 8031 Mnemonics ROM Pack identifies cycle types.

Alternate Mode. The 8031 uses P3.6/WR to indicate data memory write operations and P3.7/RD to indicate data memory read operations. Cycle types are decoded from the channels of the CNTL group according to the relationships shown in Table 4.

Table 4
IDENTIFYING ALTERNATE-MODE CYCLE TYPES

CYCLE TYPE	CNTL CHAN. 7654	3210
READ	XXXX	011X
WRITE	XXXX	101X
FETCH	XXXX	110X

Standard Mode. The 8031 gives no indication that an external memory cycle is taking place. P3.6/WR and P3.7/RD are not used as write and read strobes. External data memory reads and writes cannot be distinguished from program memory fetches and reads. This is because the read and write control lines are not used by the 8031 during standard operations.

SPECIFYING CYCLE TYPES

To specify a particular cycle type as a condition for data qualification or triggering, enter the values shown in Table 4 for that cycle type in the CNTL field of the event recognizer.

CNTL Group Modification. You may split up the CNTL group, rearrange its channels, or change its radix without affecting disassembly. The ROM Pack maintains for its internal use a version of the group as it originally set it up. This allows you to take individual channels out of the CNTL group or create your own sub-groups with names that suggest the sub-set of channels you include or the way you are using them. (Of course, reorganization of the CNTL group means that you can no longer use the values in Table 4.)

8031 CYCLE TYPE DEFINITIONS

READ A cycle where data is read from external program memory.

WRITE A cycle where data is written to external program memory.

FETCH A cycle where an instruction opcode is fetched from external program memory.

MARK OPCODE KEY

This soft key is present in the State Table when the 8031 ROM Pack is installed. Since the 8031 indicates which cycles are fetches, this key does not perform the functions described in the *Mark Opcode Key* section of your 12RM99 ROM Pack manual. Instead, pressing the mark opcode key will re-run the algorithm that creates the values in the reserved channels as described in the reserved channels section below.

8031 DISASSEMBLY LIMITATIONS

This package does not support 8031 serial operations.

This package does not flag interrupts. Instead, it will indicate which interrupt is active by the status of the signals INT0 and INT1 in the CNTL group. The interrupt routines are treated like any other software routine.

The 8031 often places the same address and data information on the bus during instruction fetch and execution cycles. The 8031 Mnemonics ROM Pack will clock in these duplicate cycles and display, but not mark, them as a particular type of 8031 instruction cycle.

Since the RD and WR control lines are not used by the 8031 during standard mode, external data memory reads and writes cannot be distinguished from program memory fetches and reads. Refer to *Identifying Cycle Types* in this manual.

When internal memory is accessed in the 8031, neither the address or data will come out on the bus. When internal memory is accessed there is no cycle that is present externally. Therefore, no data is acquired by the 1240.

RESERVED CHANNELS

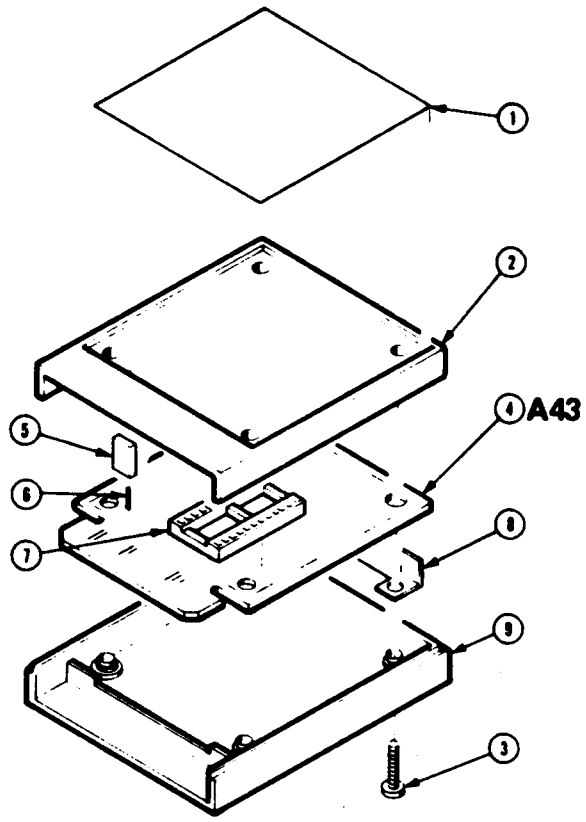
Channel 8 of the first pod (pod 0) is reserved for use by the 1240 in postprocessing the acquired data. Do not attempt to acquire data on this channel.

If you edit a portion of your reference memory, you should also edit the reserved channel associated with that portion of memory to avoid disassembly anomalies. One channel is reserved by the ROM Pack for post-acquisition processing of data to determine when to suppress cycles in SOFTWARE format. Channel 8 of the lowest-numbered acquisition pod will have a 1 stored in it on these cycles which are to be suppressed when SOFTWARE is the selected display format. These cycles are always memory reads that occur on consecutive cycles after the fetch.

If you edit your reference memory, you will need to assign this channel to a group and follow the principles described above to edit the reserved channel.

REPLACEABLE PARTS LIST
12RM99 MNEMONICS ROM PACK — OPTION 03

NUMBER	TEK. P/N	DESCRIPTION
ELECTRICAL (REFER TO SCHEMATIC IN 1240 SERVICE MANUAL)		
A43	670-8172-00	CRT. BOARD ASSY: 32/64K MEMORY ROM PACK (U200, U300 EPROMs ARE NOT PART OF A43)
A43C100	281-0775-00	CAP, FIXED, CER, DI: 0.1 uF, 20%, 50V
A43C400	281-0775-00	CAP, FIXED, CER, DI: 0.1 uF, 20%, 50V
		CHASSIS PARTS
U200	160-4032-00	MICROCKT, DGTL: 16384 x 8 EPROM, PRGM
U300	160-4002-00	MICROCKT, DGTL: 16384 x 8 EPROM, PRGM
MECHANICAL (REFER TO EXPLODED VIEW DRAWING)		
1	334-6106-00	1 MARKER, IDENT: MKD 12RM99 ROM PACK
2	200-2503-01	1 COVER, ROM PACK: TOP
		(ATTACHING PARTS)
3	211-0012-00	4 SCREW, MACHINE: 4.40 x 0.375, PHD, STL
		— — * — —
4	- - - - -	CKT BOARD ASSY: 32/64K MEMORY ROM PACK (SEE A43 REPL)
5	131-0993-00	2 • BUS CONDUCTOR: 2 WIRE, BLACK
6	131-0608-00	6 • TERMINAL, PIN: 0.365 L x 0.025 PH BRZ GOLD
7	136-0755-00	2 • SKT, PL-IN ELEC: MICROCIRCUIT, 28 DIP
8	337-3122-00	1 SHIELD, ELEC: STATIC
9	200-2504-01	1 COVER, ROM PACK: BOTTOM
		STANDARD ACCESSORIES
	070-5527-00	MANUAL, TECH: INSTRUCTION
	070-6160-00	MANUAL, TECH: INSTRUCTION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4 A43
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