DESCRIPTION

Each M175 integrated circuit contains two complete strobed voltage comparators. A strobed comparator is different from the more familiar continous duty comparator in that comparison decisions are made only on the strobe edge. This is a high performance component for clock-driven A/D converters, logic analyzer inputs, and digital test systems.

Internally each comparator is arranged in a master-slave configuration which holds the output data valid for a complete clock cycle. Output is a fixed current steered through either collector of a pair of common base NPN transistors. The output current will give sufficient voltage at the remote end of properly terminated transmission lines to accurately drive ECL or TTL differential line re-Strobe inputs are level shifted and attenuated differential ECL signals. Only a few hundred millivolts of strobe inputs are needed to operate the comparators. Though full ECL swings can be used, this unnecessarily brings large signal transients onto the die. For the strobe low input, the Master stage functions as a wide-band differential cascode amplifier. The Slave stage now performs as an amplifier in transmitting the decision state of the Master to the outputs. On return to strobe low input, the Slave stage latches and holds these outputs until the next time that the strobe input goes high. Intended voltage supplies are $\emptyset.\emptyset$ volts and -12.0 volts. Intended voltage inputs are -6.38 ± 0.125 volts. Voltage supply and input levels can be shifted together as needed for other applications. In doing so, the user must take care that the strobe inputs and current outputs will function correctly. input voltage swings are allowed within the positive limit of the cascode bias volate and the negative limit of the current source and switch. Signal distortion and slew rate limiting will occur as usual for a small signal amplifier driven outside of its linear region.

DUAL STROBED COMPARATOR

Comparison Decision Time	< 500 pS
Strobe Maximum Repetition Rate (Period)	200 MHz (95 nS)
Input Bandwidth (As An Amplifier)	> 800 MHz
Input Resolution Plus Offset	\pm 5 mV or Less
Input Range	± 125 mV Around -6.38V
Output	8 mA Through Either Of Two Common-Base Buffer Transistors
Power	1.2 Watts
PROCESS	SHF III
POWER SUPPLY	Ø - 12 Volts, 100 mA
PACKAGE	Hybrid
DESIGNER	Steve Wetterling
INSTRUMENT USAGE	7612D

