

1220/1225/1230 LOGIC ANALYZER

# PM406 6809 Microprocessor Probe

# **Operator's Manual**

The PM406 has a software version number of 2.51. For use with the PM406, the 1220 and 1225 Logic Analyzers require software versions of 2.5 or above; the 1230 Logic Analyzer requires a software version of 3.03 or above.

> Please check for change information at the back of this manual

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## OVERVIEW

The PM406 6809 Microprocessor Probe Personality Module consists of a disassembly probe (with ribbon cables) and this user's manual. This manual shows you how to connect and use the PM406 disassembly probe with the 1220/1225/1230 Logic Analyzers. This manual does not teach you how to use analyzer keypads or menus. For information on using the logic analyzer, refer to the operator's manual for your particular logic analyzer. For more information about the 6809 microprocessor, refer to your microprocessor data book.

The PM406 Version 2.51 firmware works having 1220/1225 Logic Analyzers having software version number 2.5 or higher, and with 1230 Logic Analyzers having software version numbers 3.03 or higher. if you're using a 1220/1225 version 2.5 or higher, or a 1230 version 3.03 or higher, you must use the version 2.51 PM406. You can see what version of analyzer system software you are using by reading the opening menu when you turn on the unit. You can see what version of the PM406 on the first page of Notes in the Disassembly menu. The PM406 must be connected properly to the analyzer.

The PM406 gives you an interface between the 1220/1225/1230 Logic Analyzer and 6509-based systems under test (SUT). Along with regular analyzer features, the PM406 interface lets you sample data synchronously using the SUT clock, and lets you display disassembly data in hardware and software formats.

Conventions. This manual uses these conventions:

- The term analyzer refers to the 1220, 1225, and 1230 Logic Analyzers unless otherwise specified.
- The term SUT refers to the 6809 system under test.
- Active low signals are identified by a bar over the signal name, for example, NMI.

## ANALYZER CONFIGURATION

You must have at least 32 channels in the analyzer to use the PM406. This is because the probe uses 32 channels to acquire synchronous data from the 6809-based SUT. You must also use a version 2.51 PM406 if you're using either a 1220/1225 version 2.5 (or higher) or a 1230 version 3.03 (or higher). Figure 1 shows the analyzer and expansion card configuration.

## CONNECTING AND POWERING UP

The PM406 has two probe cables that connect to the analyzer. Figures 1 and 2 show how the analyzer connects to your SUT.



Figure 1. Analyzer configuration with PM406 probe. Note that the bottom cable plugs into probe slot A and the top cable plugs into probe slot B.

To connect the PM406 to your SUT, follow these steps:

1. Make sure that the power to the analyzer and SUT is off.



Do not connect the PM406 to the analyzer unless power to analyzer is off. Do not connect the PM406 disassembly probe to the SUT unless power to the SUT is off. If you connect the disassembly probe to the SUT when power to the SUT is on and power to the analyzer is off, too much power can flow through the probe's inputs and damage the probe.

- 2. With the PM406 label side up, connect the bottom cable from the probe to input A on the front of the analyzer.
- 3. Connect the top cable from the probe to input B on the front of the analyzer.



Figure 2. Connecting the DIP clip and SUT.

- 4. Connect the PM406 probe clip to the SUT as shown in Figure 2 (power to the SUT should be off). The brown lead labeled PIN 1 on the PM406 goes to pin 1 on the 6809 microprocessor. Figure 3 shows the 6809 pinout, and Table 1 lists analyzer-to-6809 signal line connections. Figure 3 and Table 1 are shown after this procedure.
- Turn on the analyzer; this also supplies power to the probe. The analyzer screen now displays the Initialization menu (Figure 4, shown after this procedure).
- 6. Press ENIER to upload the PM406 disassembly setup into the analyzer. Pressing ENIER overwrites the existing setup and changes probe links, channel groups, and defined conditions for 6809 disassembly. If you press MENU, the PM406 setup is not uploaded and the analyzer's current setup is unchanged.
- 7. Turn on power to the SUT.

At this point the analyzer displays the Main menu (Figure 5), which lists setup, data, and utility menus. Since the default disassembly setup defines the setup parameters for you, (probe links, sampling rate and format, conditions, and so on), you can press START at any time to acquire data from your SUT. Example 1, later in this manual, shows a data acquisition with the default setup.

Signal Name	68 Pin Nu	09 Imbers	Signal Name
Vss	1	40	HALT
NMI	2	39	XTAL
IRQ	3	38	EXTAL
FIRQ	4	37	RESET
BS	5	36	MRDY
BA	6	35	Q
Vcc	7	34	E
A0	8	33	DMA/BRE
A10	9	32	R/W
A2	10	31	DO
A3	11	30	D1
A4	12	29	D2
A5	13	28	D3
A6	14	27	D4
A7	15	26	D5
A8	16	25	D6
A9	17	24	D7
A10	18	23	A15
A11	19	22	A14
A12	20	21	A13

6596-03

Figure 3. 6809 pinout.

000	s Signais anu	Analyzer C	indimeis
6809 Signals	122x/1230 Channels	Channel Groups	Description
A15-A00	B15-B00	ADD	Address bus
D07-D00	A15-A08	DAT	Data bus
BA BS	A02 A01	BUS	Processor state
R/₩	A00	BUS	Read/Write
nmi Firq Irq	A05 A04 A03	INT	Interrupts
HALT DMA/BREQ	A07 A06	CTL	Program control

 Table 1

 6809 Signals and Analyzer Channels

HED, JUN 01, 1988

#### 88 23 🖬 6889

6596 04

Tektronix 1230/48 Channel Logic Analyzer, V3.05 (C) Tektronix, Inc. 1987, 1988 All rights reserved.

Use the NOIES key whenever information is needed, or consult the Operator's Manual.

X represents DON'I CARE condition.

OK to load setup from Personality Module? (Overwrites current setup and System Links!) Press ENTER to confirm, MENU to abort

#### Press ENTER to confirm, MENU to abort.

Figure 4. Initialization menu. When you turn the analyzer on with the PM406 plugged in, the Initialization menu includes a message telling you that you can now upload the disassembly setup by pressing ENIER.

#### HED, JUN 01, 1988 08:23 6809

Tektronix 1230/48 Channel Logic Analyzer, V3.05 (C) Tektronix, Inc. 1987, 1988 All rights reserved.

SETUP	DATA		UTILITY
Timebase	6 Men Select	B	Storage
Channel Groups	7 State	c	Sys Settings
2 Trigger Spec	8 Disassembly		
3 Conditions	9 Timing	1	
4 Run Control			
		1	
Select Screen: Hex	Key or Aver for	CURS	or, then ENTE
			659

Figure 5. Main menu. The Main menu always shows disassembly as a menu selection. However, you can display acquired data in disassembly format only when the PM406 is plugged in. As long as the acquisition memory is valid, you can display valid disassembly data.

Loading Disassembly Setups. You don't have to upload the disassembly setup when you see the Initialization menu. However, if you don't, you must enter the disassembly setup manually or reset the analyzer so that the PM406 can upload the disassembly setup for you. You can reset the analyzer by firmly pressing NOTES and ENTER at the same time.

## **Using Probes**

-

The PM406 must always be plugged into slots A and B on the analyzer front panel. If you have a 1220/1225 Logic Analyzer, you can use slot C for an acquisition probe. If you have a 1230 Logic Analyzer, you can use slots C and D for acquisition probes.

You can use both an acquisition probe and the disassembly probe. The acquisition and disassembly probes can be used together or separately without unplugging either of these.

The probe in slot A must always be connected to the clock in your SUT. If the probe in slot A is not connected to your SUT clock, the analyzer won't trigger when you press SIARI. If you're using more than one probe and the probes are linked synchronously, each probe must be connected to the same clock point in your SUT. Therefore, your connection to the SUT clock is assured.

## Using the Menus and Cursor

The PM406 is controlled by selections you make in the analyzer's menus. You can always call up the Main menu by pressing MENU.

The analyzer looks at the probe inputs to find out if the PM406 is connected. For more information about using the menus and cursor, refer to the operator's manual for your particular logic analyzer.

#### **Online Help**

At the bottom of the disassembly screen, a one-line help message tells you which keys to press for disassembly functions. If you need more help, press NOTES while the disassembly screen is displayed. The analyzer then displays six pages of in-depth information about 6809 disassembly, including the disassembler's software version number which appears on the first page of disassembly notes. You can press MENU at any time to exit the notes and return to the previous display.

## SETTING UP TO ACQUIRE DATA

This discussion shows you how the PM406 sets up the analyzer for 6809 disassembly. The setups shown here are for an analyzer with 32 channels. Example 1, later in this manual, shows a data acquisition using this 32-channel default setup.

A setup is a set of parameters that describes the current analyzer configuration for data acquisition and storage. For example, the setup injudes information about probe links, acquisition rates, threshold voltage, and 6809 trigger conditions.

You can use the setup as it is uploaded from the PM406, or you can change any part of the configuration. While the discussion in this section is about the default PM406 setup, you are free to change any part of the analyzer configuration manually.

## Timebase

The acquisition timebase, probe links, and threshold voltage for 6809 disassembly are shown in Figure 6. If you're using a 1230, the PM406 uses the synchronous clock rate of your SUT. If you're using a 1220 or 1225, the PM406 is set up for synchronous acquisition at 100 ns or slower.





Figure 6. Timebase menu. Probes A and B must be linked synchronously for correct disassembly.

**Probe Links.** The PM406 is a 32-channel disassembly probe which uses probe slots A and B. For 6809 disassembly, probes A and B are linked together synchronously in timebase T1 so that all disassembly is done with the same acquisition format and rate. If you're also using one or more acquisition probes in addition to the PM406, the acquisition probes are linked asynchronously in T2.

**Clocking.** The default disassembly clock format is synchronous so that you use the clock rate in your SUT as the data sampling rate. The PM406 automatically qualifies your SUT clock with software internal to the probe. There are no external clock qualifiers for th. PM406.

For the 1230, the clock rate is set by your SUT. For the 1220/1225, the clock rate is set to  $\ge$  100 ns by default. For 6809 disassembly, you must use a clock rate of  $\ge$  100 ns if you're using a 1220/1225.

Glitch Capture. The PM406 does not acquire glitches.

### **Channel Grouping**

The PM406 sets up five channel groups: ADD, DAT, BUS, INT, and CTL, as shown in Figure 7. The screen is large enough to see four groups. To see more groups, scroll up or down the screen. The Channel Grouping menu shows how the channel groups are named; for example, ADD for the address bus. The control lines are separated into three channel groups: BUS, INT (interrupt), and CTL (control). Channels of extra probe(s) are assigned to the asynchronous timebase (T2) are in the unused list. If you want to use those channels, you must manually add them to a group.

HED, .	JUN 01, 1	988	hannel Grouping	88:24	6889
Group	p Radix	Pol TE	Channel Definit	ions ·	
add	HEX	+ 11	BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB	B 9 9	
DAT	HEX	+ 11	AAAAAAAA 11111100		
BUS	BIN	+ 11	54321098		
			000 210		
INT	BIN	+ 11	AAA 909 543		
robe			UNUSED CHANNELS	- ala sinter a <u>sint</u> er a sinte	alan dan dari dari dari dari dari dari dari dari
A	an Ang Baranga	and the second			and and a second
B C	15 14 13	12 11	10 09 08 07 06 05	04 03 02	91 99
Curso	p: 47 47	Edi t	name: ENTER De	efaúlt Gr	oups:F
					6596 0

Figure 7. Channel Grouping menu. The screen shows four channel groups. To see more channel groups, scroll up or down the screen.

## **Trigger Conditions**

The Conditions menu lets you define data conditions which the analyzer can recognize and trigger on. When you upload the 6809 setup, the 6809 input signals are already grouped to correspond to the analyzer channels as listed earlier in Table 1. The conditions listed in Table 2 show the logic states corresponding to 6809 operations.

Signal Line	ADD hex	DAT hex	BUS bin	INT bin	CTL bin
MEM READ	XXXX	XX	001	xxx	xx
MEM WRIT	XXXX	XX	000	XXX	XX
INT ACK	XXXX	XX	011	XXX	XX
SYC ACK	XXXX	XX	10X	XXX	XX
HALT ACK	XXXX	XX	11X	XXX	ox
HALT REQ	XXXX	XX	XXX	XXX	ox
BG ACK	XXXX	XX	11X	XXX	xo
BG REQ	XXXX	XX	XXX	XXX	xo
VMA CYC	FFFF	XX	X 0 1	XXX	xx
RESET	FFFE	XX	XXX	XXX	xx
NMI	XXXX	XX	XXX	oxx	хx
FIRQ	XXXX	XX	XXX	xox	XX
IRQ	XXXX	XX	XXX	XXO	XX
SWI1	FFFA	XX	XXX	XXX	XX
SWI2	FFF4	XX	XXX	XXX	XX
SWI3	FFF2	XX	XXX	XXX	XX

Table 26809 Cycle Types and Analyzer Conditions

All signals are sampled synchronously with a 6809 machine cycle, except for  $\overline{\text{NMI}}$  (nonmaskable interrupt).  $\overline{\text{NMI}}$  is displayed only at the negative edge for one cycle.

Figure 8 shows the Conditions and Trigger Spec menus. The trigger statement shown in the figure is for a 1230. If you're using a 1220/1225, the default trigger action is START instead of TRIG.

1 1	F	[]	MEN	READ	]*[8	991)	THEN	1	TRIC	1		I FI	11	
2														
					COND	ITIO	IS		1997 (1997) 1997 (1997)					
Symbol		ADD	DAI	BUS bin	INT	CIL								
HEN_REA	D:	XXXX	XX	991	XXX	XX								
NEN_HRI	I:	XXXX	XX	999	XXX	XX								
INT_ACH	::	XXXX	XX	911	XXX	XX								
SYC_AC	::	XXXX	XX	10X	XXX	XX								
•	E	lit S	mbo	1: EI	NTER		-				141.14			
*	H	Indow	Down	: F n: C										

Figure 8. Conditions and Trigger Spec menus. The default condition window is large enough to show four defined conditions. Table 2 lists all signals/conditions defined for the PM406. The default trigger statement is an if-then statement with the first condition, MEM READ, as the trigger condition. For the 1230, the trigger action is TRIG. For the 1220/1225, the trigger action is START.

## **Trigger Specification**

The default trigger statement is an if-then statement. At initialization, the analyzer is set to trigger and fill memory when the condition MEM READ occurs. Figure 8 shows the Trigger Spec menu along with the Conditions menu.

## **Run Control**

When you load the 6809 setup, the Run Control menu is set up as shown in Figure 9. The default display for acquired data is a disassembly display. The trigger position is set at memory location 1024, and the analyzer looks for the trigger after the pretrigger memory is full.

The Run Control menu also sets the memory-compare mode to Manual and tells you that the default channel mask for comparing memories is MEM READ, which is also the default trigger condition. A window (or viewport) at the bottom of the screen lists the value for MEM READ. Remember that channels set to X (don't care) are masked, or not compared, during a memory comparison.

ED, JUN 9	L, 1988	Run	Control	88 26	6889
Update Me	MORY :	11	Display:	[Disassem	bly]
Irigger P	osition:	[1924]	8	anta ing tanan s	28
Look for	Trigger:	[After P	re-Irigye	r Menory F	u11)
Compare	· ·	[Manual]			
Compare M	emory 1 t	o Menory	: [2]		
Compare Mo Use Channo	en Locatio el Mask	ons: [99 : [NE	90] to [1 M_READ]	747]	
Display D	ata at le	ast: [5]	seconds		
	ADD DAI	BUS INT	CIL		
Symbol	hex hex	bin bin	bin		
MEN_READ:	XXXX XX	991 XXX	XX		
Cursor: .	• 4> S	elect: 8	, 2		
					6596-09

Figure 9. Run Control menu. The defaults in this menu include the display format set to disassembly and the trigger position set to 1024.

#### SETTING UP TO DISASSEMBLE CODE

Once you've set up the analyzer for disassembly, you can start to acquire and display data from your SUT. The operator's manual for your particular logic analyzer tells how to display data in state and timing formats. This discussion shows you how to display disassembled 6809 data, which you can do only when the PM406 is connected to the analyzer.

As long as the acquisition memory is valid the disassembly display is also valid. Channel grouping is only used for the timing and state displays.

**Disassembly Mnemonics.** The PM406 lets you display acquired data in disassembly mnemonics. Disassembly mnemonics are assembly-language instructions that have been disassembled from a machine-language program. For example, 6809 disassembly mnemonics include JMP, CMP, NOP, and DEC instructions. An actual disassembly line might read ADDD, which means "add the memory byte to the D accumulator." Figures 12 and 13 show examples of disassembly mnemonics.

Displaying in Hardware or Software Mode. With the PM406 attached, you can display disassembled data in hardware or software mode. In hardware display mode, the analyzer shows all bus operations and displays every acquired cycle. In software display mode, the analyzer shows only instructions; reads and writes are suppressed so that the display looks like an assembly listing. You can toggle between display modes by pressing DON'T CARE.

After an acquisition, the PM406 deduces when opcode fetches occurred by analyzing acquired data and cycle types. The PM406 then displays disassembled instructions from the *location of the cursor* to the end of memory. If the cursor is near the end of memory, no instructions (or very few) may be displayed. Figures 10 and 11 show hardware and software mode examples where few disassembled instructions are shown because the cursor was positioned at the end of memory.

To re-disassemble the entire memory, use the Jump function to move the cursor to memory location 0000 (press ENIER then type 0000 on the hex keypad). Then, press 6 to mark the first valid opcode fetch. Figures 12 and 13 show re-disassembled data.

Mark Opcode. The Mark Opcode function lets you indicate the beginning of an opcode sequence. To mark an opcode, move the cursor to a Memory Read cycle then press the 6. The acquisition memory is re-disassembled from that location. If the selected cycle is not a Memory Read, then marking starts at the next Memory Read available. Marking can only be done in hardware mode.

HED, J	UN 01,	, 198	8 Dis	asn:	Henory	1	88:27	6889
Loc	Addr	Data	6889	Disa	ssembly	Ope	ration	Status
2035	FFFF	91				NOT	VHA	DMA/BREQ
2036	F573	26				HEP	READ	DMA/BREQ
2037	F574	F4				MEN	READ	DMA/BREQ
2038	FFFF	91				NOT	UMA	DMA/BREQ
2039	F569	BD				MEP	READ	DMA/BREQ
2040	F56A	F6				MEN	READ	DMA/BREQ
2941	F56B	DB				MEP	READ	DHA/BREQ
2042	FFFF	91				NOT	NMA	DMA/BREQ
2943	F6DB	A6				MEP	READ	DMA/BREQ
2944	FFFF	01				NOI	UMA	DMA/BREQ
-2945-	-CF63	-60-	an an an Arran an Arra		1965 (1997) (1977) 1977 - 1977) (1977) 1977 - 1977) (1977)	MEN	WRITE-	-DMA/BREQ
2046	<b>CF62</b>	FS				MER	HRITE	DMA/BREQ
2947	F6DB	A6				MEN	READ	DMA/BREQ
9999	8888	99	NEG	(28		OPO	FETCH	HALT
8891	F6F1	20				MER	READ	DMA/BREQ
9992	F6F2	EE				MEN	READ	DMA/BREQ
8883	FFFF	91				NOT	VHA	DMA/BREQ
0004	F6E1	E7				MEN	READ	DMA/BREQ
9995	F6E2	84				MEN	A READ	DMA/BREQ
Func:	F	Scrol	1: **	Cur	50r: 4)		Jump: El	ITER

Figure 10. Disassembly mnemonics in hardware mode. This data was displayed immediately after acquisition was completed. Because the cursor was near the end of memory, very little data was disassembled.

HED, J	UN 91,	1988	Disasn:	Memory 1	88 27	6889
Loc	Addr	Data	6889	Disassembl	y Ope	ration
9999	9999	9929	NEG	(29		
9991	F6F1	20EE	BRA	F6E1	CF6	2=F5A6
9999	8999	9929	NEG	(29		
9991	F6F1	29EE	BRA	F6E1	CF6	2=F5A6
9999	9999	8828	NEG	(29		
9991	F6F1	20EE	BRA	F6E1	CFE	2=F5A6
9999	9999	9929	NEG	(29		
-9991-	-F6F1	-20EE-	BRA-	F6E1	CF6	2=F5A6—
9999	9999	9929	NEG	(28		
9991	F6F1	20EE	BRÁ	F6E1	CF	2=F5A6
9999	8998	8828	NEG	(29		
9991	F6F1	20EE	BRA	F6E1	CF	52=F5A6
8698	8888	9929	NEG	(28		
8881	F6F1	20EE	BRA	F6E1	CF	52=F5A6
Func:	F	Scroll	Rate: 7,8	[82] No	le: X [So	ftwarel
						6596-1

Figure 11. Disassembly mnemonics in software mode. This is the corresponding software display for Figure 10. Note that the information displayed is not valid.

LocAddrData6889DisassemblyOperationStatus-0000-0000-NEG-(20)-OPCFETCH-HALT-0001F6F120BRAF6E1OPCFETCH-HALT-0002F6F2EEMEMREADDMA/BRI0003FFFF01NOTUMADMA/BRI0004F6E1E7STB,XOPCFETCH0005F6E284MEMREADDMA/BRI0006F6E3A6MEMREADDMA/BRI0007C874AAMEMMERADDMA/BRI0008F6E3A6LDA,XOPCFETCH0009F6E484MEMREADDMA/BRI0010F6E534MEMREADDMA/BRI0011C874AAMEMREADDMA/BRI0012F6E534PSHSBOPCFETCH0013F6E604MEMREADDMA/BRI0013F6E604MEMREADDMA/BRI0014FFFF01NOTUMADMA/BRI0015FFFF01MOTMA/BRI0018F6E7A0SUBAS+OPC0019F6E8E0MEMREADDMA/BRI0019F6E8E0MEMREADDMA/BRI0019F6E8E0MEMREADDMA/BRI0019F6E8E0MEM </th <th>HED, J</th> <th>IUN 91</th> <th>, 198</th> <th>8 Dis</th> <th>asn: Me</th> <th>nory 1</th> <th>8 41</th> <th>6809</th>	HED, J	IUN 91	, 198	8 Dis	asn: Me	nory 1	8 41	6809
-0000         -00000         -0000         -0000 <t< th=""><th>Loc</th><th>Addr</th><th>Data</th><th>a 6809</th><th>Disasse</th><th>nbly Open</th><th>nation</th><th>Status</th></t<>	Loc	Addr	Data	a 6809	Disasse	nbly Open	nation	Status
0001         F6F1         20         BRA         F6E1         OPC         FETCH         DMA/BRI           0002         F6F2         EE         MEM         READ         DMA/BRI           0003         FFFF         01         NOT         UMA         DMA/BRI           0004         F6E1         E7         SIB         ,X         OPC         FETCH         DMA/BRI           0005         F6E2         84         MEM         READ         DMA/BRI           0006         F6E3         A6         MEM         READ         DMA/BRI           0007         C874         AA         MEM         MEAD         DMA/BRI           0009         F6E3         A6         LDA         ,X         OPC         FETCH         DMA/BRI           0009         F6E5         34         MEM         READ         DMA/BRI           0010         F6E5         34         PSHS         B         OPC         FETCH         DMA/BRI           0011         C874         AA         MEM         READ         DMA/BRI           0013         F6E6         04         MEM         READ         DMA/BRI           0013         F6E6 <t< td=""><td>-0000-</td><td>-0000</td><td>-00-</td><td>-NEG</td><td>~20</td><td>OPC</td><td>FETCH-</td><td>HALT</td></t<>	-0000-	-0000	-00-	-NEG	~20	OPC	FETCH-	HALT
9092         F6F2         EE         MEM         READ         DMA/BRI           9093         FFFF         91         NOT         UMA         DMA/BRI           9094         F6E1         F7         STB         ,X         OPC         FETCH         DMA/BRI           9095         F6E2         84         MEM         READ         DMA/BRI           9095         F6E2         84         MEM         READ         DMA/BRI           9096         F6E3         A6         MEM         READ         DMA/BRI           9097         C874         AA         MEM         NRI READ         DMA/BRI           9098         F6E3         A6         LDA         ,X         OPC         FETCH         DMA/BRI           9098         F6E3         34         MEM         READ         DMA/BRI           9099         F6E4         84         MEM         READ         DMA/BRI           9010         F6E5         34         PSHS         B         OPC         FETCH         DMA/BRI           9013         F6E6         94         MEM         READ         DMA/BRI           9014         FFFF         91         NOT         <	0001	F6F1	20	BRA	F6E1	OPC	FETCH	DMA/BREQ
0003         FFFF 01         NOT UMA         DMA/BRI           0004         F6E1         E7         STB         ,X         OPC         FETCH         DMA/BRI           0005         F6E2         84         MEM         READ         DMA/BRI           0006         F6E3         A6         MEM         READ         DMA/BRI           0007         C874         AA         MEM         READ         DMA/BRI           0008         F6E3         A6         LDA         ,X         OPC         FETCH         DMA/BRI           0009         F6E4         84         MEM         NEAD         DMA/BRI           0010         F6E5         34         OPC         FETCH         DMA/BRI           0011         C874         AA         MEM         READ         DMA/BRI           0011         F6E5         34         PSHS         B         OPC         FETCH         DMA/BRI           0011         C874         AA         MEM         READ         DMA/BRI           0012         F6E5         34         PSHS         B         OPC         FETCH         DMA/BRI           0013         F6E6         04         MOT	8992	F6F2	EE			MEM	READ	DMA/BREQ
0004         F6E1         E7         STB         ,X         OPC         FETCH         DMA/BR           0005         F6E2         84         MEM         READ         DMA/BR           0006         F6E3         A6         MEM         READ         DMA/BR           0006         F6E3         A6         MEM         READ         DMA/BR           0008         F6E3         A6         MEM         WEM         WA/BR           0008         F6E3         A6         MEM         WEM         WA/BR           0008         F6E3         A6         MEM         MEM         MA/BR           0009         F6E4         84         MEM         READ         DMA/BR           0011         C874         AA         MEM         READ         DMA/BR           0011         C874         AA         MEM         READ         DMA/BR           0012         F6E5         34         PSHS         B         OPC         FETCH         DMA/BR           0013         F6E6         04         MEM         READ         DMA/BR           0013         F6E6         04         MOT         UMA         DMA/BR	8983	FFFF	91			NOT	UMA	DMA/BREQ
9985         F6E2         84         MEM         READ         DMA/BRI           9986         F6E3         A6         MEM         READ         DMA/BRI           9986         F6E3         A6         MEM         READ         DMA/BRI           9987         C874         AA         MEM         MEM         READ         DMA/BRI           9888         F6E3         A6         LDA         ,X         OPC         FEICH         DMA/BRI           9899         F6E4         84         MEM         READ         DMA/BRI           9899         F6E4         84         MEM         READ         DMA/BRI           9899         F6E4         84         MEM         READ         DMA/BRI           9891         F6E5         34         MEM         READ         DMA/BRI           9811         C874         AA         MEM         READ         DMA/BRI           9912         F6E5         34         PSHS         B         OPC         FEICH         DMA/BRI           9913         F6E6         94         MOI         MA/BRI         MA/BRI         MA/BRI           9915         FFFF         91         MOI	8884	F6E1	E7	STB	,χ	OPC	FETCH	DMA/BREQ
9996         F6E3         A6         MEM         READ         DMA/BRI           9997         C874         AA         MEM         MRITE         DMA/BRI           9998         F6E3         A6         LDA         ,X         OPC         FEICH         DMA/BRI           9999         F6E4         84         MEM         READ         DMA/BRI           9010         F6E5         34         MEM         READ         DMA/BRI           9011         C874         AA         MEM         READ         DMA/BRI           9011         C874         AA         MEM         READ         DMA/BRI           9011         C874         AA         MEM         READ         DMA/BRI           9012         F6E5         34         PSHS         B         OPC         FEICH         DMA/BRI           9013         F6E6         94         MEM         READ         DMA/BRI           9014         FFFF         91         NOT         UMA         DMA/BRI           9016         CF61         DA         MEM         READ         DMA/BRI           9016         CF61         DA         MEM         READ         DMA/BRI <td>9995</td> <td>F6E2</td> <td>84</td> <td></td> <td></td> <td>MEH</td> <td>READ</td> <td>DHA/BREQ</td>	9995	F6E2	84			MEH	READ	DHA/BREQ
0007         C874         AA         MEM         WRITE         DMA/BRE           0008         F6E3         A6         LDA         , X         OPC         FETCH         DMA/BRE           0009         F6E4         84         MEM         READ         DMA/BRE           0010         F6E5         34         MEM         READ         DMA/BRE           0011         C874         AA         MEM         READ         DMA/BRE           0012         F6E5         34         PSHS         B         OPC         FETCH         DMA/BRE           0013         F6E6         04         MEM         READ         DMA/BRE           0013         F6E6         04         MEM         READ         DMA/BRE           0014         FFFF         01         NOT         UMA         DMA/BRE           0015         FFFF         01         NOT         UMA         DMA/BRE           0016         CF61         DA         MEM         READ         DMA/BRE           0018         F6E7         AQ         SUBA         S+         OPC         FETCH         DMA/BRE           0019         F6E8         EQ         MA/BRE	8886	F6E3	A6			NEH	READ	DMA/BREQ
9008         F6E3         A6         LDA         , X         OPC         FEICH         DMA/BRI           9009         F6E4         84         MEM         READ         DMA/BRI           9010         F6E5         34         MEM         READ         DMA/BRI           9011         C874         AA         MEM         READ         DMA/BRI           9012         F6E5         34         PSHS         B         OPC         FEICH         DMA/BRI           9013         F6E6         04         MEM         READ         DMA/BRI           9014         FFFF         01         NOI         UMA         DMA/BRI           9015         FFFF         01         NOI         UMA         DMA/BRI           9016         CF61         DA         MEM         READ         DMA/BRI           9017         CF60         AA         MEM         READ         DMA/BRI           9018         F6E7         AQ         MEM         READ         DMA/BRI           9019         F6E8         EQ         SUBA         S+         OPC         FEICH         DMA/BRI           9019         F6E8         EQ         MEM	9997	C874	AA			MEM	WRITE	DMA/BREQ
0009         F6E4         84         MEM         READ         DMA/BRI           0010         F6E5         34         MEM         READ         DMA/BRI           0011         C874         AA         MEM         READ         DMA/BRI           0012         F6E5         34         PSHS         B         OPC         FETCH         DMA/BRI           0013         F6E6         04         MEM         READ         DMA/BRI           0014         FFFF         01         NOT         UMA         DMA/BRI           0015         FFFF         01         NOT         UMA         DMA/BRI           0016         CF61         DA         MEM         READ         DMA/BRI           0017         CF60         AA         MEM         READ         DMA/BRI           0018         F6E7         AG         SUBA         S+         OPC         FETCH         DMA/BRI           0019         F6E8         E0         MEM         READ         DMA/BRI           0019         F6E8         E0         MEM         READ         DMA/BRI	8888	F6E3	A6	LDA	,X	OPC	FETCH	DMA/BREQ
0010         F6E5         34         MEM         READ         DMA/BRI           0011         C874         AA         MEM         READ         DMA/BRI           0012         F6E5         34         PSHS         B         OPC         FETCH         DMA/BRI           0013         F6E6         04         MEM         READ         DMA/BRI           0014         FFFF         01         NOT         UMA         DMA/BRI           0015         FFFF         01         NOT         UMA         DMA/BRI           0016         CF61         DA         MEM         READ         DMA/BRI           0017         CF60         AA         MEM         NEI         DMA/BRI           0018         F6E7         AG         SUBA         ,S+         OPC         FETCH         DMA/BRI           0019         F6E8         E0         MEM         READ         DMA/BRI           0019         F6E8         E0         MEM         READ         DMA/BRI           FUnct:F         Scroll         Rate:         7,8         (021         Mode:         X	8889	F6E4	84			MEM	READ	DMA/BREQ
0011         C874         AA         MEM         READ         DMA/BRI           0012         F6E5         34         PSHS         B         OPC         FETCH         DMA/BRI           0013         F6E6         04         MEN         READ         DMA/BRI           0013         F6E6         04         MEN         READ         DMA/BRI           0013         F6E6         04         MEN         READ         DMA/BRI           0014         FFFF         01         NOT         UMA         DMA/BRI           0015         FFFF         01         NOT         UMA         DMA/BRI           0016         CF61         DA         MEM         READ         DMA/BRI           0017         CF60         AA         MEM         READ         DMA/BRI           0018         F6E7         AQ         SUBA         S+         OPC         FETCH         DMA/BRI           0019         F6E8         EQ         MEM         MEAD         DMA/BRI           Funct:F         Scroll         Rate:         7,8         (021         Mode:         X         Hardware	9919	F6E5	34			HEM	READ	DMA/BREQ
0012         F6E5         34         PSHS         B         OPC         FEICH         DMA/BRI           0013         F6E6         04         MEM         READ         DMA/BRI           0014         FFFF         01         NOI         UMA         DMA/BRI           0015         FFFF         01         NOI         UMA         DMA/BRI           0016         CF61         DA         MEM         READ         DMA/BRI           0016         CF61         DA         MEM         READ         DMA/BRI           0017         CF60         AA         MEM         REI         DMA/BRI           0018         F6E7         AO         SUBA         ,S+         OPC         FEICH         DMA/BRI           0019         F6E8         E0         MEM         READ         DMA/BRI           Func: F         Scroll         Rate:         7,8         (92)         Mode:         X         Hardware	9911	C874	AA			HEN	READ	DMA/BREQ
0013         F6E6         04         MEM         READ         DMA/BRI           0014         FFFF         01         NOT         UMA         DMA/BRI           0015         FFFF         01         NOT         UMA         DMA/BRI           0016         CF61         DA         MEM         READ         DMA/BRI           0017         CF60         AA         MEM         READ         DMA/BRI           0018         CF62         AA         MEM         HIT         DMA/BRI           0018         F6E7         AO         SUBA         ,S+         OPC         FEICH         DMA/BRI           0019         F6E8         EQ         MEM         READ         DMA/BRI           Func: F         Scroll         Rate:         7,8         (82)         Mode:         X         (Hardware)	9912	F6E5	34	PSHS	B	OPC	FEICH	DMA/BREQ
0014         FFFF         01         NOT         UMA         DMA/BRI           0015         FFFF         01         NOT         UMA         DMA/BRI           0016         CF61         DA         MEM         READ         DMA/BRI           0017         CF60         AA         MEM         MEITE         DMA/BRI           0018         F6E7         AO         SUBA         S+         OPC         FETCH         DMA/BRI           0019         F6E8         E0         MEM         READ         DMA/BRI           Func:F         Scroll         Rate:         7,8         (02)         Mode:         X         (Hardware)	9913	F6E6	94			HEN	READ	DMA/BREQ
0015         FFFF         01         NOT         UMA         DMA/BRE           0016         CF61         DA         MEM         READ         DMA/BRE           0017         CF60         AA         MEM         NRITE         DMA/BRE           0018         F6E7         AO         SUBA         S+         OPC         FETCH         DMA/BRE           0019         F6E8         E0         MEM         READ         DMA/BRE           Func:F         Scroll         Rate:         7,8         (02)         Mode:         X         (Hardware)	0014	FFFF	91			NOT	UMA	DMA/BREQ
0916CF61DAMEMREADDMA/BRE0917CF60AAMEMWRITEDMA/BRE0918F6E7AOSUBA,S+OPCFETCHDMA/BRE0919F6E8EOMEMREADDMA/BREFunc:FScrollRate:7,8(82)Mode:X	0015	FFFF	91			NOT	UNA	DMA/BREQ
0017     CF60 AA     MEM WRITE DMA/BRI       0018     F6E7 AQ     SUBA     ,S+     OPC FETCH DMA/BRI       0019     F6E8 EQ     MEM READ     DMA/BRI       Func:F     Scroll Rate: 7,8 [82]     Mode: X [Hardware]	0016	<b>CF61</b>	DA			HEM	READ	DMA/BREQ
0018         F6E7         AO         SUBA         S+         OPC         FEICH         DMA/BRE           0019         F6E8         EO         MEM         READ         DMA/BRE           Func:F         Scroll         Rate:         7,8         [82]         Mode:         X         [Hardware]	9917	CF60	AA			HEN	HRITE	DMA/BREQ
BOI9         F6E8         E0         MEN         READ         DMA/BRE           Func:F         Scroll         Rate: 7,8         [82]         Mode: X         [Hardware]	9918	F6E7	AQ	SUBA	,S+	OPC	FEICH	DMA/BREQ
Func:F Scroll Rate: 7,8 [82] Mode: X [Hardware]	0019	F6E8	EØ			HEN	READ	DMA/BREQ
	Func	F	Scrol	I Rate:	7,8 [82	] Mode	X [Ha	rdware]

Figure 12. Re-disassembled disassembly mnemonics in hardware mode. Now that the cursor has been jumped to location 0000 and an opcode fetch has been marked, the analyzer now displays valid data.

HED,	JUN 81	, 1988	Disasm:	Menory 1	98:41 6899
Loc	Addr	Data	6889	Disassembl	y Operation
-0000		-9929	NEG-		
0001	F6F1	20EE	BRA	F6E1	
8884	F6E1	E784	STB	.X	C874=AA
8998	F6E3	A684	LDA	,X	C874=AA
8912	F6E5	3494	PSHS	B	CF61=DAAA
8918	F6E7	AGEO	SUBA	, S+	CF69=AA
0924	F6E9	269E	BNE	F6F9	
0927	F6EB	C155	CMPB	#55	
0029	F6ED	2694	BNE	F6F3	
0032	F6F3	3592	PULS	A	CF61=DAF5
8838	F6F5	A784	STA	,Χ	C874=DA
0042	F6F7	4F	CLRA		
0844	F6F8	39	RTS		CF62=F56C
8849	F56C	2697	BNE	F575	
8852	F56E	3001	LEAX	91,X	
0857	F578	BCCF33	CMPX	CF33	CF33=D999
8864	F573	26F4	BNE	F569	
8867	F569	BDF6DB	JSR	F6DB	CF63=6CF5
0075	F6DB	A684	LDA	,Χ	C875=DA
0079	F6DD	3492	PSHS	A	CF62=F5DA
Func	F	Scroll R	ate: 7,8	[82] Nod	le: X [Software]
Sumal charle	A CONTRACTOR OF STREET	and the second second	A Charles and A states	den en e	6506 1

Figure 13. Re-disassembled disassembly mnemonics in software mode. Here is the software display which corresponds to Figure 12. Now the analyzer displays valid data.

**Invalid Codes.** The analyzer displays question marks (???) when there isn't enough information to determine the beginning of a valid opcode fetch. Figure 14 shows an example. Use the Mark Opcode function to indicate the beginning of an opcode sequence.

HED, JU	N 01,	1988	Disasm	: Nei	nory 1	89 2	2 6889
Loc	Addr	Data	68	09 Di	sassen	bly I	Operation
0099 9091	<b>0000</b> F3F9	0002 02	NE ??	G ?	(82		F3F0=3402
8999 8991	<b>0080</b> F3F9	8992 92	NE ?7	G ?	<b>&lt; 8</b> 2	:	F3F8=3492
9999 9991	0000 F3F9	9992 92	NE ??	.G ?	<b>&lt; 8</b> 2		F3F0=3402
9999 -9991	<b>0000</b> F3F9	9992 92	NE??	:G ?	(82		F3F0=3402
9999 9991	0000 F3F9	9992 92	NE ??	:G ??	(82		F3F0=3402
0009 0001	0000 F3F9	9992 92	NI ?1	G ?	<b>(8</b> 2		F3F0=3402
9999 9991	<b>8000</b> F3F9	9992 92	NI ?1	:G ?	<b>&lt; 9</b> 2		F3F0=3402
Fune 'F			D-4-1 7	0 1 30		- 1- 1 V	

Figure 14. Invalid or unknown opcode displayed in hardware mode. An opcode which the PM406 cannot interpret is shown as ???.

Searching for Events. Searching for events in the Disassembly menu works the same as searching for events in the State Menu. Press 0 or 2 to cycle through the available conditions (including ".e trigger event). Press 1 to perform the search.

When the analyzer finds the search event, it redisplays the disassembly screen so that the cursor is positioned in the middle of the screen indicating the search event. If you searched for an event that did not occur, the analyzer displays the message Not Found. One of the menu bars at the bottom of the screen lists the current search event. For more information about searching, refer to the operator's manual for your particular logic analyzer.

The analyzer can display and search for opcode fetches in software mode. However, since reads and writes (which are not opcode fetches) are suppressed in software mode, the analyzer cannot display those instructions if you try to search for them. In software mode, if you search for an event that is not an opcode fetch and it is found, the analyzer sets the cursor to the previous opcode fetch and displays the the search event in the middle of the screen.

## Using the Hardware Display Mode

For disassembly displays in hardware mode, the analyzer displays each sample location with address and data from the 6809 bus cycle. Disassembled instructions are displayed at the beginning of each valid machine cycle. Figure 12, earlier in this discussion, shows a hardware disassembly display.

In the displays, the Loc column shows memory locations. The Addr column shows the address, and the Data column displays the data bus. When the PM406 recognizes the beginning of an instruction, the analyzer disassembles that instruction and displays it in the middle column.

BA, BS and R/W are decoded into cycle-type information and displayed in the Operation column. Table 3 shows each Operation type display and its definition.

	Table	e 3
0	peration	Column

Cycles	Description
OPC FETCH	Opcode fetch
MEM READ	Memory read
MEM WRITE	Memory write
INT ACK	Interrupt acknowledge
SYNC ACK	Sync acknowledge
HALT ACK	Halt acknowledge
NOT VMA	Not valid memory address
Manager and the Point and the second second	· · · · · · · · · · · · · · · · · · ·

The last column displays the status of interrupt lines. In this column, the interrupt with the highest priority is listed. For example, if an NMI and IRQ occur at the same time, the NMI signal is listed in the display. Table 4 lists interrupt priorities.

Active Line	Description
HALT	Halt
DMA/BREQ	Direct memory
	access/bus request
NMI	Nonmaskable
and the second	interrupt
FIRQ	Fast interrupt request
IRQ	Interrupt request

## Table 4 Status Column Interrupt Priorities

Pressing DON'T CARE while in the hardware display mode toggles the disassembly screen to the software display mode, and vice versa.

When you press DON'T CARE to switch display modes, the analyzer goes through memory to find the opcode fetch closest to the cursor position. When it inds the opcode fetch, the analyzer displays the disassembly in software mode with the cursor in the middle of the screen. If it can't find an opcode fetch, the analyzer returns to hardware mode.

## Using the Software Display Mode

The software display mode is useful because it displays only instructions; memory reads and writes are suppressed. The display resembles an assembly or program listing because it shows only one opcode fetch per line and each line must be the start of an instruction sequence. Because of this, the locations displayed are not contiguous. Figure 13, earlier in this discussion, shows a software disassembly display.

The Operation column lists the bus operations for the instruction sequence. For each instruction cycle, the analyzer uses the Operation column to tell you the memory address and data activity for that cycle. In this column, the address is displayed on the left of the equals sign; data is displayed on the right. Figure 13 shows address and data information.

Searching for Events. You can search for events in the software disassembly display the same as you search for events in the State menu. However, because memory reads and writes are suppressed, if you search for an event that occurs on a memory read or write cycle, the analyzer displays the instruction that caused the memory read or memory write. To search for a memory read or write cycle, press DON'T CARE to toggle to hardware mode, then select the search event, and then press 1 to search.

### EXAMPLES

These four examples show you how to acquire data for disassembly, how to display the data in hardware and software modes, how to trigger on a specific event, how to use multiple levels of triggering, and how to cross-trigger the disassembly probe from a different timebase (using an acquisition probe).

The first example uses the default setup for a simple acquisition. In the second example, you define a specific event on which you want to trigger. The third example uses two levels of triggering. In the fourth example, you cross-trigger the PM406 from an acquisition probe using a different timebase than the disassembly probe.

## Example 1. A Simple Acquisition

This example uses the default 6809 setup uploaded when you connected the analyzer to a SUT and initialized the analyzer. This example shows you how to:

- acquire and disassemble data
- jump to a specific location
- re-disassemble data using the Mark Opcode function
- search for a particular event
- toggle between display modes

Follow these steps to make a simple acquisition and begin manipulating data:

1. Make sure the PM406 is connected to your SUT and the analyzer is initialized with the default disassembly setup.

- 2. Press START to acquire data. In the default setup, the analyzer will trigger on the first memory read that occurs after the pre-trigger memory is full. The Acquisition Process screen is displayed, telling you the status of the acquisition. When the acquisition is complete, the analyzer stops and displays the data in disassembly since that is the default data format.
- Data is disassembled from the cursor location to the end of memory. Data above the cursor is not disassembled.
   Figure 15 shows an example of this.

In order to disassemble the entire memory, you must jump to the beginning of memory and use the Mark Opcode function.

- 4. Press ENIER to tell the analyzer you want to enter a new location to be displayed, then enter 0000 to jump to the beginning of memory. As you finish entering the digits, the analyzer jumps to the selected memory address and displays the new information, as shown in Figure 16.
- Press 6 to mark the first opcode forch. This forces the PM406 to re-disassemble the data in its memory. The analyzer now displays opcode fetches from location 0000 throughout memory. See Figure 17.
- 6. Press 0 or 2 to cycle through available search functions and choose the trigger as the search event.
- 7. Press 1 to search for the trigger. Figure 18 shows the trigger event in hardware mode.
- Press DON'T CARE to toggle to software display mode. In software display mode, only instructions are displayed.
   Figure 19 shows the software display which corresponds to the hardware display in Figure 18.

When you switch disassembly modes, the analyzer goes through memory to find the opcode fetch closest to the cursor. If it can't find an opcode fetch, it returns to hardware mode.

The scroll rate, jump, and search features for disassembly displays work the same as they do in the State menu. For more information about these features, sefer to the operator's manual for your particular logic analyzer.

THU,	JUN 02,	1988	Dis	asn: H	enory 1	9	8:93	6889
Loc	Addr	Data	5889	Disass	embly O	per	ation	Status
9938	F405	27			K	EM	READ	DMA/BREQ
8839	F496	F9			K	EM	READ	DMA/BREQ
8848	FFFF	91			N	IOT	UMA	DMA/BREQ
8941	F499	BD			tin t	EN	READ	DMA/BREQ
9942	F401	F3			K	EN	READ	DMA/BREQ
8843	F402	ED			K	EN	READ	DMA/BREQ
9944	FFFF	01			N	IOI	UNA	DMA/BREQ
0045	F3ED	B6			K	EN	READ	DMA/BREQ
9946	FFFF	01			N	IOI	VMA	DMA/BREQ
0047	CF65	83			K	EM	WRITE	DMA/BREQ
-0048	-CF64	-F4			H	EN	WRITE-	-DMA/BREQ
0049	F3ED	B6	LDA	BF82	0	PC	FETCH	DMA/BREQ
9959	F3EE	BF				EM	READ	DMA/BREQ
9951	F3EF	82			<b>-</b>	EN	READ	DMA/BREQ
0052	FFFF	81				IOI	VMA	DMA/BREQ
8853	BF82	89			H	EM	READ	DMA/BREQ
0054	F3F8	34	PSHS	A	(	PC	FETCH	DMA/BREQ
9955	F3F1	82			S	EM	READ	DMA/BREQ
9956	FFFF	01			N	IOI	UMA	DMA/BREQ
9957	FFFF	<b>8</b> 1			1	IOI	UNA	DMA/BREQ
Fund	:F	Scroll	: **	Curso	P: 4)	J	IMP: E	ITER
and the second			(Television)	Steller State		Sinter.		6596-15

Figure 15. Hardware disassembly display immediately after acquisition is complete. Data is disassembled starting at the cursor location.

THU,	JUN 92,	1988	Disas	a: Menory	1 6	88:04	6889
Loc	Addr	Data 6	889 D	isassembly	Oper	ration	Status
-0000	-0000-	-00		ED	-OPC	FETCH-	HALT
8891	F492	ED	an Brittan -		MEH	READ	DMA/BREQ
8992	FFFF	91			NOT	UNA	DMA/BREQ
8883	F3ED	B6			MEN	READ	DMA/BREQ
8984	FFFF	91			NOT	UMA	DMA/BREQ
8985	5 CF65	93			MEN	HRITE	DMA/BREQ
9998	5 CF64	F4			MEN	HRITE	DMA/BREQ
8993	F3ED	B6			MEN	READ	DMA/BREQ
8998	F3EE	BF			HEN	READ	DMA/BREQ
8999	F3EF	82			HEN	READ	DMA/BREQ
9910	FFFF	91			NOI	UNA	DMA/BREQ
9911	BF82	88			MEN	READ	DMA/BREQ
9912	E F3F8	34			MEN	READ	DMA/BREQ
001:	3 F3F1	82			HEN	READ	DMA/BREQ
9814	A FFFF	01			NOT	UNA	DMA/BREQ
881	5 FFFF	91			NOT	UNA	DMA/BREQ
991	5 CF64	F4			MEM	READ	DMA/BREQ
991	7 CF63	88			MEN	HRITE	DMA/BREQ
881	B F3F2	84			HEH	READ	DMA/BREQ
991	9 F3F3	7F			MEH	READ	DMA/BREQ
Fun	::F	Scroll	T	Cursor: 4	J	unp: Et	TER
ale ale				and the second second			6596-16

Figure 16. Hardware disassembly display after jumping to location 0000. As you finish entering the digits for the location, the analyzer displays the new information starting at the top of the screen.

THU,	JUN 02,	1988	Di	sasm:	Nenory		8:94	6899
Loc	Addr	Data	6889	Disa	ssembly	Oper	ation	Status
-0000	-0000-	-00	NEG-	(ED-		-OPC	FETCH-	HALT-
0001	F402	ED	SID	01,X		OPC	FETCH	DMA/BREQ
0002	FFFF	01				NOT	UMA	DMA/BREQ
8993	F3ED	B6				MEM	READ	DMA/BREQ
0004	<b>FFFF</b>	91				NOT	UMA	DMA/BREQ
0005	CF65	03				MEM	HRITE	DMA/BREQ
9998	CF64	F4				MEM	HRITE	DMA/BREQ
8997	F3ED	B6	LDA	<b>BF82</b>		OPC	FETCH	DMA/BREQ
0008	F3EE	BF				MEM	READ	DMA/BREQ
0009	F3EF	82				MEM	READ	DMA/BREQ
0010	FFFF	91				NOT	UMA	DMA/BREQ
0011	BF82	99				HEM	READ	DMA/BREQ
0012	F3F8	34	PSHS	A		OPC	FETCH	DMA/BREQ
9913	8 F3F1	92				MEN	READ	DMA/BREQ
9914	<b>I</b> FFFF	01				NOT	UMA	DMA/BREQ
9915	5 FFFF	91				NOT	UMA	DMA/BREQ
9910	5 CF64	F4				MEM	READ	DMA/BREQ
9917	? CF63	99				MEN	HRITE	DMA/BREQ
9918	3 F3F2	84	ANDA	#7F		OPC	FETCH	DMA/BREQ
9919	F3F3	7F				MEN	READ	DMA/BREQ
Fund	::F *	Mark O	pcode	: 6				
- particular	AND NO SAN TANK	(historia)	all the second	No. 1 Contactor	and the stand sec	Succession - A	ACCOUNTS	6596-17

Figure 17. Hardware disassembly display after marking the first opcode fetch. The Mark Opcode function re-disassembles memory from the cursor location, in this case location 0000.

THU, J	UN 02,	1988	Dis	asm:	Henory	1	8:05	6889
Loc	Addr	Data	6889	Disa	ssembly	Oper	ration	Status
1914	CF64	F4				MEH	WRITE	DMA/BREQ
1015	F3ED	B6	LDA	<b>BF82</b>		OPC	FETCH	DMA/BREQ
1016	<b>F3EE</b>	BF				MEM	READ	DMA/BREQ
1917	<b>F3EF</b>	82				MEM	READ	DMA/BREQ
1918	FFFF	01				NOT	UNA	DMA/BREQ
1019	<b>BF82</b>	89				NEM	READ	DMA/BREQ
1929	F3F8	34	PSHS	A		OPC	FEICH	DMA/BREQ
1921	<b>F3F1</b>	92				MEM	READ	DMA/BREQ
1922	FFFF	91				NOI	UNA	DMA/BREQ
1823	FFFF	91				NOT	VHA	DMA/BREQ
-TRIC	-CF64	-F4	Stephensky powe	elet de la comp	gen operation (and an	HEM	READ-	-DMA/BREQ
1925	CF63	99				NEN	WRITE	DMA/BREQ
1926	F3F2	84	ANDA	#7F		OPC	FETCH	DMA/BREQ
1927	F3F3	7F				MEM	READ	DMA/BREQ
1928	F3F4	81	CMPA	#17		OPC	FEICH	DMA/BREQ
1829	F3F5	17				MEM	READ	DMA/BREQ
1939	F3F6	24	BCC	F3FB		OPC	FETCH	DMA/BREQ
1931	F3F7	83				MEM	READ	DMA/BREQ
1832	FFFF	91				NOT	VHA	DMA/BREQ
1833	F3F8	35	PULS	A		OPC	FETCH	DMA/BREQ
Func		Search	For:	8,2 [	Trigger	1	Do Se	arch: 1
Succession and	and the second straight of	San States	South States of the	Same State Go	Section of the section of	Chick with south	and the second second second	6506 18

Figure 18. Hardware disassembly display. The search event in this example is the trigger event, which occurred at memory location 1024 as specified in the Run Control menu.

THU, J	UN 92	, 1988	Disasn:	lenory 1	88 85	6889
Loc	Addr	Data '	6889 1	disassenbl	ly Op	eration
8978	F3F0	3492	PSHS	A	CF	4=F400
8984	F3F2	847F	ANDA	#7F		
8986	F3F4	8117	CHPA	#17		
8988	F3F6	2493	BCC	F3FB		
8991	F3F8	3592	PULS	A	CF	53=00F4
8997	F3FA	39	RTS		CF	54=F403
1992	F403	8589	BITA	#89		
1994	F495	2759	BEQ	F400		
1997	F400	BDF3ED	JSR	F3ED	CF	5=03F4
1915	F3ED	B6BF82	LDA	BF82	BF	32=00
-1929-	-F3F8	-3402	-PSHS-	A	CF	4=F400-
1826	F3F2	847F	ANDA	#7F		
1928	F3F4	8117	CMPA	#17		
1939	F3F6	2493	BCC	F3FB		
1833	F3F8	3592	PULS	A	CF	3=90F4
1039	F3FA	39	RTS		CF	4=F403
1844	F403	8588	BITA	889		
1846	F405	2759	BEQ	F499		
1849	F400	BDF3ED	JSR	F3ED	CE	5=03F4
1057	F3ED	B6BF82	LDA	BF82	BF	32=00
Suga	5	Canall D.		001 Ma		
rune		SCPUIL Ra	ite: 7,8 La	ABI NOC	ie: x LS	II THAPE I

Figure 19. Corresponding software disassembly. Because the trigger was not an opcode fetch, this software disassembly display (corresponding to the hardware display shown in Figure 18) does not show the trigger event at the cursor. The Operation column shows the address (left side of equals sign) and data information for the instructions that occurred.

## Example 2: Trigger on a Specific Event

This example shows you how to trigger on an event which you specify. In this example, a program is yielding unexpected results. The program contains a BEQ, branch on equal, instruction and you suspect the program is branching incorrectly. The BEQ has a data value of 27hex. You want to see where this command makes the program go. You need to define the BEQ as the trigger and then move the trigger towards the beginning of the memory, so that there is enough memory space for the results you want to see.

This example uses the default setup except for defined conditions and trigger specification and the location of the trigger in memory. You don't need to change the timebase or the channel grouping from the default settings. Follow these steps to trigger on the specific event.

- In the Conditions menu, rename the Q condition word to BRANCH and define it as DAT 27. Figure 20 shows the new BRANCH condition word definition: XXXX 27 XXX XXX XX.
- In the Trigger Spec menu, define the condition in the level 1 trigger statement to BRANCH. Figure 20 shows this. When the analyzer finds 27hex on the data lines, it triggers and fills the memory with data.
- 3. In the Run Control menu, move the trigger position to 128 as shown in Figure 21. This position provides a large portion of memory to store the data occurring after the branch, thereby allowing you to see what happens to your program after executing the BEQ command.
- 4. Start the acquisition by pressing START. The analyzer will display data in hardware mode.
- 5. In order to have the maximum amount of disassembled data, jump to location 0000 and mark the first opcode fetch.
- Use the search function to find the trigger event. Figure 22 shows the cursor on the trigger event, BEQ, in hardware display mode. This is the beginning of the branch you were looking for.
- Press X to toggle to software display mode. Figure 23 shows the trigger event again. You can use the displayed information to see where the branch has led the program.

1 11	F	BRAN	CH	D*( 8	001)	THEM	1	IR	IG	1	å	(	FI	LL	3
2															
•															
3															
4															
5															
									1						
CONDITI	ON:	DAT	DIIC	INT	CTI										
Sumbol	hex	hex	bin	Lin	bin										
BRANCH	:XXXX	27	YYY	VUV	VV										
re 20.	Condi fined a	Selec tions as DA	and T 27	2 1 Tri 7hex Bun	ggei and	victi Spe as th	ec r ie t	ne rig	nu: gei	A. s. r C	BF	RA Idi		CH	-20 I i
re 20. IU, JUN	Condi fined a 92, 1	Selec tions as DA 988	and T 27	2 1 Tri 7hex Run	gger and Cont	vucti Spe as th rol	e r ie t	ne rig	nu gei 7:5	A. S. C	BFon	RA Idi		CH on.	-20   i
re 20. IU, JUN Ipdate	Condi fined a 02, 1 Henory	Selec tions as DA 988 :	and T 27	,2 d Tri Thex Run	ggei and Conti Dis	vucti Spe as th rol play	ec r ie t	ner rig Ø	nu: gei 7: S	A. 5. 10 18	BF on	RA idi 68	ee e Ni itic	CH on.	-20 I i
ensor re 20. IV, JUN Ipdate Irigger Look fo	Condi lined a 02, 1 Menory Posit r Trig	tions as DA 988 : ion: ger:	and T 27	2 1 Tri 7hex Run 281 ter 1	ggei and Conti Dis	vucti Spe as th rol play g	ec r ie t : []	ne rig Ø Dis	nu: gei 7:5 ass	A 5. 10 18 18	BF on	RA idi 68 9 ]	109 109	CH on.	20
re 20. IU, JUN Ipdate Irigger Look fo	Condi fined a 92, 1 Menory Posit r Trig	Selec tions as DA 988 : ion: ger: ;	and T 27 [1] [1] [0] [Aft] [Mar	2 1 Tri 7 hex Run 283 ter 1 hual 2	ggei and Conti Dis Pre-I	vucti Spe as th Fol play 9 rigge	er l	ne rig O Dis Men	nu gei 7: S as:	A 5. 58 58 58 58	BF on	AA adi 68 y 1	6 6 109 1 2 1	CH on.	-2( 
re 20. IV, JUN Ipdate Irigger Look fo Compare	Condi lined a 02, 1 Menory Posit r Trig Menor	Selec tions as DA 988 : ion: ger: ; y 1 t	and T 27 [1] [1] [0]2 [Af1 [Mar 0 Me	2 3 7 7 7 7 7 7 7 7 7 7 7 7 7	ggei and Dis Pre-I	victi Spe as th rol Play 0 _ rigg	ec r le t : []	nei rigi Di s	DE gei 7:5 ass	A. 5. 58 58 59	BF on	11		CH on.	2( 
re 20. IU, JUN Ipdate Irigger Look fo Compare	Condi fined a 02, 1 Menory Posit r Trig Menor	Selec tions is DA 988 : ion: ger: : y 1 t	and T 27 [1] [1] [0]2 [Aft [Mar o Me ons	AAA Tri Thex Run (8) ter 1 mual: emory : [00	ggei and Dis Pre-I	ucti Spe as th rol Play 0 _ rigg	2001 C r ie t : [] : []	ne rig Ø Dis Men	nu gei 7:5 ass	A.	BF on	11	109 1	CH On.	20
re 20. IU, JUN Ipdate Irigger Look fo Compare Compare Use Cha	Condi fined a 02, 1 Menory Posit r Trig Memor Mem 1 nnel P	Selections as DA 988 : ion: ger: : y 1 t .ocati lask	and T 27 [1] [1] [Aft] [Mar o Me ons	AAA 2 Tri 7 hex Run 28] ter 1 ter 1 ter 1 1 Tu 1 Tu 1 Tu	Institution           gggei           and           Conti           Dis           Pre-I           i           i; (2           0001           2	vucti r Spee as th rol play 0 riggo riggo 1 to [	on: ie t : [] er	Dis Men	nu: gei 7:5	A 5. 58 58 59	BF on	11 68 91		CH on.	- 2¢
ensors re 20. IU, JUN Ipdate Irigger Look fo Compare Compare Compare Se Cha Display	Condi fined a 02, 1 Menory Posit r Trig Menor Men I nnel P Data	Selec tions is DA 988 : ion: ger: ; y 1 t .ocati lask at le	and T 27 [1] [1] [Aft] [Mar o Me ons east	2 1 Tri 7hex Run 28] ter 1 28] ter 1 20 20 20 20 20 20 20 20 20 20 20 20 20	AA           Institution           ggei           and           Continue           Dis           Pre-I           I	vucti r Spee as th rol Play 8 rigg rigg rigg rigg rigg rigg rigg	on: ie t : [] er	Dis Men 71	Di gei 7:5 ory	A.	BF on abl	AA idi 68 91		CH on.	2
re 20. IU, JUN Ipdate Irigger Look fo Compare Compare Use Cha Display	Condi fined a 92, 1 Menory Posit r Trig Menor Men 1 nnel 1 Data AD	Stolec tions is DA 988 : ion: ger: : y 1 t	and T 27 (11) (11) (11) (11) (11) (11) (11) (11	1     Tri       2     1       1     Tri       7     Tri       7     Tri       80     1       80     1       1     1       1     1       1     1       1     1       1     1       1     1       1     1       1     1       1     1       1     1       1     1       1     1       1     1       1     1       1     1       1     1       1     1       1     1	AA           Institution           ggei           and           Conti           Dis           Pre-I           I           I:           I: <td>vection - Spectro - Spectro -</td> <td>on: e t : [] :r ]</td> <td>Dis Men 71</td> <td>Dia gen 7:5 ass</td> <td>A.</td> <td>BF on</td> <td>11</td> <td></td> <td>CH Don.</td> <td>2</td>	vection - Spectro -	on: e t : [] :r ]	Dis Men 71	Dia gen 7:5 ass	A.	BF on	11		CH Don.	2

Figure 21. Run Control menu for example 2. The trigger position has been changed to 128, leaving most of memory to store the data that occurs after the trigger event.

1

THU.	JUN 02	1988	Dis	asn: Henory		8:99	6899
Loc	Addr	Data	6889	Disassembly	Oper	ation.	Status
R118	FFFF	81			NOT	UMA	DMA/BREQ
0119	CF63	99			MEM	READ	DMA/BREQ
9120	CF64	F4			MEM	READ	DMA/BREQ
0121	FAFA	39	RTS		OPC	FEICH	DMA/BREQ
0122		96			HEN	READ	DMA/BREQ
0122	CELA	FA			NEM	READ	DMA/BREQ
012		02			NEN	READ	DMA/BREQ
012		03			NOT	UMA	DMA/BREQ
012		01		***	APC	TETCH	DMA/RRED
012	1993	80	BIIH	<b>#08</b>	MTM	DEAD	DMA/RRFD
012	1 1999	80		F 400	ADC	TTTCU_	-DMA / PPEO
-1:11	-1485	-27-	-BFA	-1 4VV	UTU	DEAD	DMA / DDEO
012	9 F406	F9			nLn	REHD	DMA /DDEO
013	<b>B</b> FFFF	01			NOI	VIIH	DAN DALA
913	1 F499	BD	JSR	F3ED	OPC	FEICH	DHA/BREY
013	2 F401	F3			MEM	READ	DHA/BREY
913	3 F492	ED			MEM	READ	DHA/BREY
913	4 FFFF	01			NOT	UMA	DMA/BREQ
813	5 F3EL	B6			MEM	READ	DMA/BREQ
Q13	6 FFFF	81			NOT	UNA	DMA/BREQ
913	7 CF65	6 83			MEN	WRITE	DMA/BREQ
Fun	c:F	Searc	h For:	8,2 [Trigge	r 1	Do Se	earch: 1

Figure 22. Trigger event in hardware display mode. The cursor marks the trigger event, BEQ.

THU.	JUN 82,	1988	Disasm:	Nemory 1	98:91 📱 6889
Loc	Addr	Data	6889	Disassenb	ly Operation
9986	F495	2759	BEQ	F499	
8089	F4RQ	BDF3ED	JSR	F3ED	CF65=03F4
0097	FSFD	B6BF82	LDA	BF82	BF82=00
0107	FILA	3492	PSHS	A	CF64=F400
0100	5352	8475	ANDA	17F	
0110	FILA	8117	CMPA	117	
0112	1314	2403	BCC	F3FB	
0110	5 5350	2502	PHILS	A	CF63=99F4
011	TOTA	3000	219		CF64=F403
0121	TA02	0500	RITA	899	
0120	5 1983	0100	BITH	F400	erander, også blikketsburgs
	1483	-2117	ICP	1300	CE65-83E4
W13.	1 1999	BUIJED	JSR	DE03	BE82-00
013	9 FJED	BPBISS	LUN	Brog	CT(A-TA00
914	4 F3F8	3485	PSHS	H	CL04-1400
915	<b>B</b> E3E5	847F	ANDA		
015	2 F3F4	8117	CMPA	#17	
015	4 F3F6	2493	BCC	F3FB	
915	7 F3F8	3592	PULS	i A	CF63=00F4
916	3 F3FA	39	RIS		CF64=F403
	A T403	0500	RITA	889	

Figure 23. Trigger event in software display mode. The cursor marks the trigger event, BEQ. This figure corresponds to the hardware display mode of Figure 22.

## **Example 3: Triggering with Two Levels**

You can work through this example only if you have a 1230 logic analyzer. If you have a 1220 or 1225 analyzer, you should go on to example 4.

This example shows you how to acquire a block of specific data. In this example, a particular subroutine occurs a number of times in the program. You want to acquire only the subroutine. You need to define two conditions: the beginning of the subroutine and the end of the subroutine. The beginning of the subroutine is JSR (jump to new location saving return address) and has a data value of BDhex. The end of the subroutine is RTS (return from subroutine) and has a data value of 39hex.

In order to show an example of a multi-level acquisition, you'll have the analyzer acquire the subroutine, then loop back and acquire it again until we stop the acquisition manually.

This example uses the default setup except for defined conditions and trigger statements. You don't need to change the timebase or channel grouping control information from the default 32-channel setup for this example. Follow these steps to trace a subroutine and trigger on the subroutine:

- In the Conditions menu, rename the Q condition word to JUMP and define it as DAT BDnex. Figure 24 shows the new JUMP condition word definition: XXXX BD XX XXX.
- Rename the R condition word to RETURN and define it as DAT 39hex. Figure 24 shows the new RETURN condition word definition: XXXX 39 XX XXX.
- 3. In the Trigger Spec menu, define four levels of if-then trigger statements as shown in Figure 25. The analyzer starts storing information immediately, so you want to turn off storage at level 1. Level 2 indicates that when the analyzer finds BDhex on the data lines (the beginning of the subroutine) it starts to store data, then moves on to level 3.

Because the RTS (return from subroutine) is actually five hex data numbers long, you can't just turn storage off when the analyzer encounters a 39hex. If you did this, the

PM406 would not have enough information to disassemble the command. So level 3 indicates that when the analyzer finds 39hex on the data lines, the analyzer stores that information and goes on to level 4. Level 4 indicates that after four more hex numbers occu." (the end of the RTS command), the analyzer stops storing data, then loops back up to level 2 again to look for BDhex.

- 4. In the Run Control menu, the data display should default to Disassembly. Because you will halt the acquisition manually, the stop point will be the trigger position. Change the Trigger Position to 1920 so that the stop point is near the end of memory allowing for more storage of data. Figure 26 shows the Run Control menu for this example.
- 5. Press START. At the first occurance of the subroutine, the analyzer starts storing the information. When the return is encountered, the analyzer waits until the end of the RTS command, then stops storage and loops back up to level 2 to search for the next occurance of JUMP.
- After a few seconds, press STOP. The analyzer stops acquiring data and displays the acquisition in disassembly format.
- Jump to location 0000 and mark the first opcode fetch. Figure 27 shows the hardware mode display for this acquisition.
- 8. Press X to toggle to software display mode. You can see in Figure 28 that the software display stops listing instructions after location 1919.
- Toggle back to hardware display mode and search for the trigger. Figure 29 shows that there were no valid opcode fetches after the trigger event. This happens when you stop the acquisition by pressing STOP.

RI, JU Level	N 83	3, 19 Con	88	T	rigg Coun	er S: t	PEC	Act	89	: 35		6809 Dest	anta a
1	IF	[	s		)*[9	001 J	THEN	٤S	IRO	FF)	å	[ G010	2
2	IF	t,	JUMP		]*[9	001 )	THEN	[5]	IR	сио	å	[ G010	3
3	IF	[]	RETU	RN	]*[0	0011	THEN	[]	NOP	3	å	[ G010	4
Cumbal			RAT	DUC		0110	15						
SYNDUI		hex	hex	bin	bin	bin							
JUKP	:	XXXX	BD	XXX	XXX	XX							
RETURN	:	XXXX	39	XXX	XXX	XX							
S	:	XXXX	XX	XXX	XXX	XX							
•	Ed	lit Sy	mbol	I: E	NTER								
< >	Hi	ndow	Up	: F									

Figure 24. Conditions setup. The two new conditions define the beginning and end of the subroutine you're tracing.

FRI,	JUN 03,	1988	Trigger S	pec	89 34	6889
Leve		Condition	Count	1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.	Action	Dest
1	IF		<b> </b> *[ 9991 ]	THEN	[STROFF]	& [GOTO 2]
2	IF	( JUMP	)×(0001)	THEN	[STR ON]	& [GOTO 3]
3	IF	[ RETURN	]×[0001]	THEN	[ NOP ]	a [GOIO 4]
4	IF	[\$	]*[9994]	THEN	(STROFF)	# [GOTO 2]
5						

CONDITI	ON:		1827	in states in	
	ADD	DAT	BUS	INT	CIL
Symbol	hex	hex	bin	Lin	bin
S	:XXXX	XX	XXX	XXX	XX

#### Cursor: ++++ Select: 8,2 Instruction: ENTER Advanced: 1 6596-25

Figure 25. Trigger Spec setup. The four levels of trigger statements tell the analyzer to store everything between the beginning and end of the subroutine, and then loop back up to level 2, search for the beginning of the next occurance of the same subroutine, and store it again.

THU, JUN 02, 1988	Run Control	08:14 📱 6809
Update Memory :	[1] Display:	[Disassembly]
Irigger Position:	0	- SK
Look for Trigger:	lAfter Pre-Irigge	r Memory Full]
Compare :	[Manual]	
Compare Memory 1	to Memory: [2]	
Compare Mem Locat Use Channel Mask	ions: [9999] to [1 : [MEM_READ]	747]
Display Data at li	east: [5] seconds	

Symbol MEM_READ:	ADD hex XXXX	DAI hex XX	BUS bin 991	INT bin XXX	CIL bin XX	
Cursor: A	<b>T {}</b>	Se	lec	: 8	2	
	10.000	a States and States	1405.00	21-21.7		6596-2

Figure 26. Run Control menu. The default display is set to Disassembly and the trigger position is changed to 1920.

FRI,	JUN 03,	1988	Dis	asm:	Menory		9 51	6889
Loc	Addr	Data (	6889	Disa	ssembly	Oper	ation	Status
2040	9999	89				MEN	HRITE	HALT
2941	9999	89				MEM	HRITE	HALT
2042	9999	99				MEM	HRITE	HALT
2043	9999	99				MEM	HRITE	HALT
2044	9999	99				MEM	WRITE	HALT
2945	0999	99				MEN	WRITE	HALI
2946	9999	99				MEN	WRITE	HALT
2947	9999	99				MEM	WRITE	HALI
9999	EF64	91	???			OPC	FETCH	DMA/BREQ
-8891	-F3ED	-BD	JSR-	-F3ED		-OPC	FETCH-	-DMA/BREQ
0002	F3EE	F3	ADDD	ED91		OPC	FETCH	DMA/BREQ
9993	F3EF	ED	SID	81,X		OPC	FETCH	DMA/BREQ
9994	FFFF	91				NOI	VMA	DMA/BREQ
999	5 BF82	B6				MEN	READ	DMA/BREQ
9999	F3F0	91				MEH	READ	DMA/BREQ
9997	7 F3F1	83				MEH	WRITE	DMA/BREQ
9998	FFFF	F4				MEH	HRITE	DMA/BREQ
888	FFFF	B6				NOT	UMA	DMA/BREQ
991	EF64	BF	SIX	8291		OPC	FETCH	DMA/BREQ
Fund	:E	Scroll	Rate:	7,8	[20]	Node	: X [Ha	rdware]

Figure 27. Hardware display. Location 0000 shows the end of an instruction. The analyzer displays question marks (???) because it doesn't have enough information to disassemble this instruction.

FRI,	JUN 03,	1988	Disasm:	Menory 1	89 5	1 6809
Loc	Addr	Data	6889	Disassemb	ly	Operation
1896	F3ED	B6BF82	LDA	BF82		BF82=00
1991	F3F8	3492	PSHS	A		EF64=F400
1997	F3F2	847F	ANDA	#7F		
1989	F3F4	8117	CMPA	#17		
1911	F3F6	2493	BCC	F3FB		
1914	F3F8	3592	PULS	A		
1918	EF63	99F4	NEG	(F4		
1919	EF64	F49999	ANDB	9999		8888=8888
9999	EF64	91	???			
-0001	-F3ED	-BDF3ED	JSR-	-F3ED-		
9993	F3EF	ED91	SID	91, X		F3F0=0193
0010	EF64	BF8201	SIX	8291		F3F8=00
8828	F3F9	847F	ANDA	#7F		
0023	EF63	172493	LBSR	1369		
0027	EF64	3592	PULS	A		F499=9191
0031	F492	BOF4	NEG	(F4		EF64=0301
8938	F3EE	BDF3ED	JSR	F3ED		F3F9=B691
8846	EF64	B6BF82	LDA	BF82		F3F4=00
0051	F3F5	3492	PSHS	A		
Func	:F	Scroll	Rate: 7,8	[28] No	de: X	[Software]
						6596-2

Figure 28. Software display. You can see the subroutine sequence in a more compact form in software mode since only instructions are displayed.

FRI, J	JUN 03, 19	88 Di	sasn: Menory	99 52	6889
Loc	Addr Dat.	a 6889	Disassembly	Operation	Status
1918	F3F5 17			MEM READ	DMA/BREG
1911	F3F6 24	BCC	F3FB	OPC FETCH	DMA/BREG
1912	F3F7 83			MEM READ	DMA/BREG
1913	FFFF 01			NOT UMA	DHA/BREG
1914	F3F8 35	PULS	A	OPC FETCH	DMA/BREG
1915	F3F9 82			MEM READ	DMA/BREG
1916	FFFF 81			NOT UMA	DMA/BREG
1917	FFFF 01			NOT UMA	DMA/BREG
1918	EF63 88	NEG	<b>(F4</b>	OPC FEICH	DMA/BREG
1919	<b>EF64 F4</b>	ANDB	9999	OPC FEICH	DMA/BREG
-TRIC	-9999 -99-			MEN WRITE	HALT
1921	99999 99			MEN HRITE	HALT
1922	99999 99			MEM HRITE	HALT
1923	9999 99			MEN HRITE	HALT
1924	9999 99			MEN WRITE	HALT
1925	9999 99			MEN WRITE	HALT
1926	9999 99			MEN WRITE	HALT
1927	9999 99			MEN WRITE	HALT
1928	9999 99			MEN WRITE	HALT
1929	8888 88			MEN HRITE	HALT
Func	:F Sear	ch For:	8,2 [Trigger	1 Do S	earch: 1
C. There are an	and the second second		and the second second second	Sector Sector Sector	6596-2

Figure 29. Hardware display at trigger event. Notice that there are no more opcode fetch instructions after the trigger. This is a result of using STOP to end the acquisition.

## **Example 4: Cross-Triggering**

If you're using a 1225 or 1230 Logic Analzyer, you can acquire data on a 16-channel acquisition probe at the same time you use the PM406. You can also set the PM406 to trigger off the timebase of the acquisition probe, or vice versa. This example shows you how to set up the PM406 to trigger off the acquisition probe.

**Configuration**. This example uses a 1225/1230 with 48 channels. The PM406 is still plugged into probe slots A and B. The 16-channel acquisition probe (P6443 or P6444) is plugged into probe slot C.

What This Example Shows. This example shows how to set up an acquisition probe to trigger on a condition, then set up the disassembly probe to automatically cross-trigger and show the acquired information in disassembly display. In this example, you want to know how the code is executed when you trigger the acquisition probe on a particular event. The analyzer then automatically cross-triggers the disassembly probe so that you can display the disassembly data for that acquisition.

Figures 29 through 34 show the setup menus for this example. The menus show how to set up the 1225/1230 with these parameters:

- Probes A and B are in T1; probe C is in T2.
- Channel group GPF is renamed to TST and contains 16 channels from probe C.
- The trigger condition GET is defined for the specific event upon which you wish to trigger.
- The trigger timebase is T2 (the acquisition probe) so that the 1225/1230 recognizes the trigger condition GET and automatically cross-triggers the disassembly probe when GET occurs.

The Steps for Cross-Triggering. Follow these steps to crosstrigger the PM406 off the acquisition probe and search for the trigger event in the resulting disassembly display:

 In the Timebase menu, probes A and B are linked by default in timebase T1 (separately from probe C, which should be in T2). Change the rate of timebase T2 to 1 μs. Refer to Figure 30.

- 2. In the Channel Grouping menu, scroll to channel group GPE and change the channel group name to TST. Add channels C15-C00 to this new group. Refer to Figure 31.
- In the Conditions menu, define a condition GET to the value D4F1nex in group TST. Figure 32 shows the Trigger Spec menu and the value of the trigger condition GET.
- 4. In the Trigger Spec menu, set the trigger condition to GET. Figure 32 shows the Trigger Spec menu.
- 5. Look at the menu bar at the bottom of the Trigger Spec menu, and press D to toggle the trigger timebase to T2. Refer to Figure 32.
- In the Run Control menu, make sure the 1225/1230 looks for the trigger GET after the pretrigger memory is full. The default data display format should still be set to Disassembly.
- 7. Press START. When the analyzer recognizes the trigger condition, the analyzer triggers all modules, fills memory, and stops. The disassembly screen is displayed.
- Press 0 or 2 to cycle through available search events until you select Trigger, then press 1 to locate the trigger. Figure 33 shows the trigger event in a hardware disassembly display. The corresponding software mode display is in Figure 34.
- 9. In order to view the data from the acquisition probe, you must display data from a different timebase (T2). Go to the State display and you'll see the disassembly information in state format. Press F until you see the Timebase: field at the bottom of the screen. Press 9 to change to Timebase T2. The State display will now show the data that was acquired on the acquisition probe. Figure 35 shows the state display for channel TST on probe C.

Once you've made the acquisition, you can call up state, disassembly, and timing displays for the acquired data. Since you used two timebases to make the acquisition, you must change pages to display what happened in T2 on the acquisition probe, and then what happened in T1 on the disassembly probe. To change the timebase in the State menu, use the 9. To change the timebase in the Timing menu, use the 0 and 1.



Figure 30. Timebase for cross-trigger. Probes A and B (the PM406) are linked in T1, and probe C (the acquisition probe) is in T2. This lets you acquire data with different timebases.

FRI, JUI	N 83, 1	988	Ch	annel Grouping	89	35	6889
Group	Radix	Pol	TB	Channel Definitio	ns		
ADD	HEX	•	<b>T</b> 1	BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB			
DAT	HEX	٠	TI	AAAAAAAA 11111100 54321098			
BUS	BIN	•	11	AAA 999 219			
INT	BIN	٠	T1	AAA 999 543			
CIL	BIN	٠	11	AA 00 76			
ISI	HEX	٠	12	CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC			6596

Figure 31. Channel Grouping for cross-trigger. The analyzer screen shows only four channel groups at a time. This figure is a modification of two combined screens so you can see all five channel group definitions. The channel group shows that the fifth channel group is renamed to TST and contains 16 channels for acquisition probe C (timebase T2).

HU, JU Level	N 82, 19 Cor	988 188	1 on	rigg Cour	er S	pec	Ac	88 1 i on	29		68	109 31	
1	IF į	GET	and	<b>]</b> *( (	9991 1	THEN	ſ	TRIG	)	*	ſ	FILL	Distance of the
2													
3													
4													
5													
CONDIT	10N:		DUC										No. of the second
Synbol GET	hdd hex :XXXX	he× XX	bin XXX	bin XXX	bin XX	hex D4F1							
Curt	+++ Sel	: 8, 2	Ins	PIE	NTER	Irigl	B:	DI 121	R	dv	an	ced:1	1

Figure 32. Conditions and Trigger Spec for cross-trigger. The trigger condition GET is defined as D4F1hex. The menu bar at the bottom of the Trigger Spec screen shows that the trigger timebase is T2.

THU, .	JUN 82,	1988	Dis	asn: Menory		8:31 📱	6889
Loc	Addr	Data	6889	Disassembly	Oper	ation	Status
1914	F3F4	81	CMPA	#17	OPC	FETCH	DMA/BREQ
1015	F3F5	17			MEN	READ	DMA/BREQ
1016	F3F6	24	BCC	F3FB	OPC	FETCH	DMA/BREQ
1017	F3F7	83			MEN	READ	DMA/BREQ
1018	FFFF	81			NOT	UMA	DMA/BREQ
1019	F3F8	35	PULS	A	OPC	FETCH	DMA/BREQ
1020	F3F9	82			MEM	READ	DMA/BREQ
1921	FFFF	01			NOT	UMA	DMA/BREQ
1922	FFFF	81			NOT	UMA	DMA/BREQ
1923	<b>CF63</b>	99			MEM	READ	DMA/BREQ
TRIG	CF64	-F4	ant in Anna Maria.		HEM	READ-	-DMA/BREQ
1925	F3FA	39	RTS		OPC	FEICH	DMA/BREQ
1026	F3FB	86			MEM	READ	DMA/BREQ
1927	CF64	F4			NEN	READ	DMA/BREQ
1928	CF65	83			MEN	READ	DMA/BREQ
1929	FFFF	01			NOT	UMA	DMA/BREQ
1030	F403	85	BITA	88	OPC	FETCH	DMA/BREQ
1931	F494	88			MEN	READ	DMA/BREQ
1032	F495	27	BEQ	F490	OPC	FEICH	DMA/BREQ
1033	F406	F9			MEM	READ	DMA/BREQ
Func	15	Search	For:	8,2 [Trigger	1	Do Se	arch: 1
Card and		e and speciality			- Telebook	North States	6596 33

Figure 33. Hardware disassembly display. After searching for the trigger event, the cursor is on IRIG. IRIG marks the event that occurred in timebase T1 when trigger event GET occurred in timebase T2.

THU.	JUN 82,	1988	Disasn:	Menory 1	08:31 🖸 6809
Loc	Addr	Data	6889	Disassemb	ly Operation
897	7 F3F8	3592	PULS	A	CF63=00F4
898	3 F3FA	39	RTS		CF64=F403
898	8 F493	8588	BITA	888	
099	G F495	2759	BEQ	F499	
000	3 5400	RDF3FD	JSR	F3ED	CF65=83F4
100	1 2320	BERER2	LDA	<b>BF82</b>	BF82=00
100	6 2320	3402	PSHS	A	CF64=F400
100	2 5252	0475	ANDA	875	
101	6 F3F6 A F2FA	0117	CHPA	#17	
101	4 1314	2402	900	FIFR	
101	0 1710	2503	PULC		CF63=88F4
-101	9-1310	-3382-	PTC	- "	CF64=F493
102	5 131A	37	RIS		
103	8 1483	8288	BIIN	5400	
193	2 1403	2719	BEQ	1488	CE45-02EA
103	5 F400	BDF3ED	JSN	FJED	000-00
194	I3 F3ED	B6BF82	LDA	8182	BF64-66
194	18 F3F8	3492	PSHS	i A	C104=14RR
195	4 F3F2	847F	ANDA	17F	
195	6 F3F4	8117	CMPA	1 117	
195	58 F3F6	2493	BCC	F3FB	
Fut	nc:F	Scroll	Rate: 7.8	[28] No	ode: X [Software]
			Service and service and services	Service Contraction Contractor	E506 33

Figure 34. Software disassembly display. This software display corresponds to the hardware display shown in Figure 34. Note that the trigger event was in the middle of an instruction, so the cursor in the display is near the trigger event, not on it.

THU.	JUN 82,	1988	State:	Nenory	1	88	32	680	9
Loc	TST								
19788	hex								
191	4 387F								
181	5 397F								
181	6 397F								
101	7 397F								
101	8 397F								
191	9 D4FO								
192	e D4Fe								
192	1 D4FO								
192	2 DAFO								
192	3 DAFO								ant turas
-131	C-D4F1-			an fan te ster ster ster ster ster ster ster s	Section 1	1.00	(1 N)(1	Service States	gen ingen
182	5 D4F1								
182	6 D4F1								
192	7 D4F1								
192	8 D4F2								
192	9 D4F2								
183	8 D4F2								
193	1 D4F2								
103	2 D4F2								
103	3 7CF3				Service !!	Sugar Sugar	all and		
Fur	IC:F SCP	oll Ra	te:7,8[28	l Timeba	se:	9[12	Asy	IUC	L US I
Section and									0590

Figure 35. State display for timebase T2. Condition GET (D4F thex) is the trigger event.