TECHNICAL
INSTRUCTION and
TRAINING for the

TYPE 6RIA
NOTES

TYPE 6RIA NOTES

Written and Produced in Field Training

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6R1A CONTENTS

SECTION I

CHARACTERISTICS

A. OPERATING CHARACTERISTICS

1. INPUT

   Internally from horizontal and vertical plug-in units.

2. UNITS OF MEASURE

   Volts: Readout in millivolts (MV) and volts (V).

   Time: Readout in nanoseconds (NS), microseconds (μS), milliseconds (MS), and seconds (S).

3. NUMERICAL RANGE

   Readout from .0000 to 9999.

4. ACCURACY OF READOUT

   The accuracy of the number shown on the readout depends on the accuracy of the plug-in units, the difference in comparator delay, start and stop multivibrators, counters, and pickoff ability. Readout accuracy is always better than that of an operator reading from the CRT.

5. DISPLAY TIME

   Variable from ≈0.1 second to ≈5 seconds.

6. PRESET NO-GO LIMITS

   Front-panel controls set lower and upper limits. Front panel indicator lights show whether the number on the readout is less than, between, or greater than the preset limits.

7. START AND STOP TIMING

   A or B Trace %: Seven fixed percentages (10% through 90%), accurate to within 0.25%.

   Manual Control: Uncalibrated.

   Start and Stop Voltages: Precision dials to measure CRT divisions from the 0% Zone, accurate to within 1% at about 8 cm of deflection.

8. MAXIMUM SWEEP RATE

   Non-Sampling Sweep: 20 μsec/div maximum useful rate.

   Sampling Sweep: Not limited.

   NOTE: When the memory RESPONSE switches are set to FAST and the memory MODE switches are set to PEAK (these switches are all on the Memory circuit cards), the memories will charge

4 volts in 2 μsec. With these switch settings, the leakdown rate is 300 mv/sec. If the RESPONSE switches are set to SLOW, the memories charge to 4 volts in 20 μsec, and the leakdown rate is 6 mv/sec. With the RESPONSE switches set to SLOW, the memories will charge with no more than 2 dots delay even at the fastest sampling sweep rate. Because of the previously listed leakdown rates, the switch combination of PEAK mode, FAST response, and AVERAGE OF TEN SWEEPS resolution should not be used with real-time sweep speeds of 0.1 cm/sec or slower, or with sampling rates less than 1000 samples/sec.

9. EXTERNAL PROGRAMMING

The Type 6R1A can be programmed externally from remote or automatic equipment. Readout information is available for external readout.

B. MECHANICAL CHARACTERISTICS

1. CONSTRUCTION

Aluminum-alloy chassis. Photo-etched anodized aluminum front panel

2. NET WEIGHT

10.2 pounds

C. CIRCUIT CARD IDENTIFICATION

The end plate of each circuit card contains the name or function of the card, such as Counter, Voltmeter, etc , and a letter to show its location in the Type 6R1A chassis The Counter cards, for example, have the letter A as a location guide; the Voltmeter card has the letter E as a location guide.

Circuit cards now under development for other instruments may also operate in the Type 6R1A These cards may be identified by two location guide letters For example, a new Counter card may be identified as A/Z. This card will fit location A in the Type 6R1A, and location Z in another instrument.

6R1A BLOCK DISCUSSION

The Block Discussion is divided into three sections.

SECTION 2

Discusses general operation of a digital measurement system. Digital time measurement. Digital voltage measurement. Connection of digital system to oscilloscope display. Scaling the display to fit the calibration of the oscilloscope.

SECTION 3

A block discussion of each function found in the 6R1A. Block discussion is oriented around layout of circuits on circuit cards.

SECTION 4

A discussion of the logic levels and signals found in 6R1A. Discusses each logic level or signal, and its effects on parts of the circuit.

SECTION 2

6R1A BLOCK DISCUSSION

I. REVIEW OF DIGITAL READOUT TECHNIQUE, AS USED IN 6R1A

A. The digital readout itself is a pulse counter, with an accurate pulse generator, or clock. A gate circuit is used to connect the clock to the digital counter. Figure 2-1 shows the relationship. The counter advances one count with each pulse received. For the moment, ignore the actual workings of the counter circuit, and think of it only as a device that displays the number of pulses sent to it through the gate. The counter, to be practical, has a display period following the count period, and then resets to zero before the gate allows pulses to pass through for a new count.

B. The period the gate allows pulses to pass to the counter is measured directly as time by the counter. For example, assume a 1 megacycle clock (such as the 1 microsec markers from a 180A). If the gate is on (allows signal to pass) for 283 microseconds, 283 pulses will pass to the counter. The counter will count to 283. Thus, the period that the gate is on is read directly by the counter. Figure 2-2 shows a time measurement system.

1. This time measurement function is the same as that obtainable with any of the commonly used digital time readout devices, such as the Berkely and Hewlett-Packard counters. These counters also have other functions, which are not important to us here.

C. Voltage can be measured by making a period of time equal to the voltage. Here, a smaller voltage must turn on the gate for a shorter period of time, and a larger voltage must turn it on for a longer period of time. The system still makes a time measurement, since a time interval is made equivalent to the voltage.

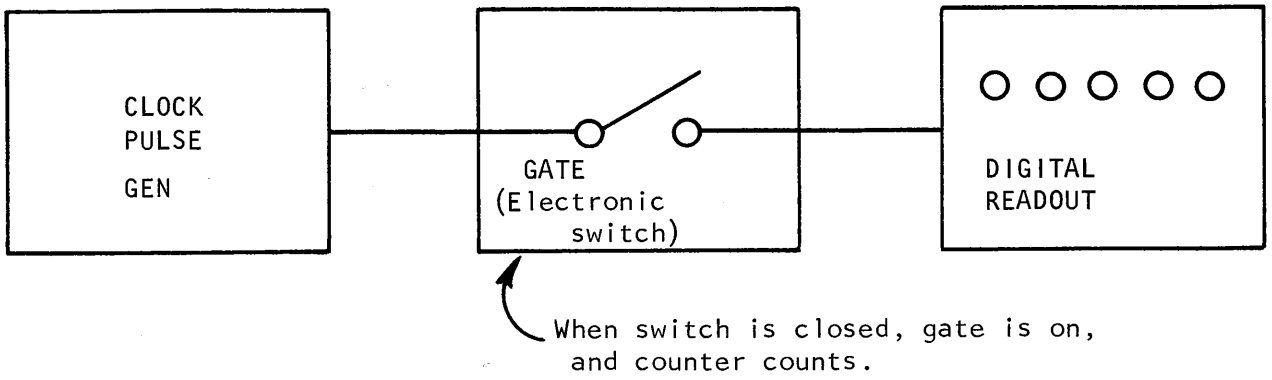

Figure 2 - 1

BASIC DIGITAL READOUT SYSTEM

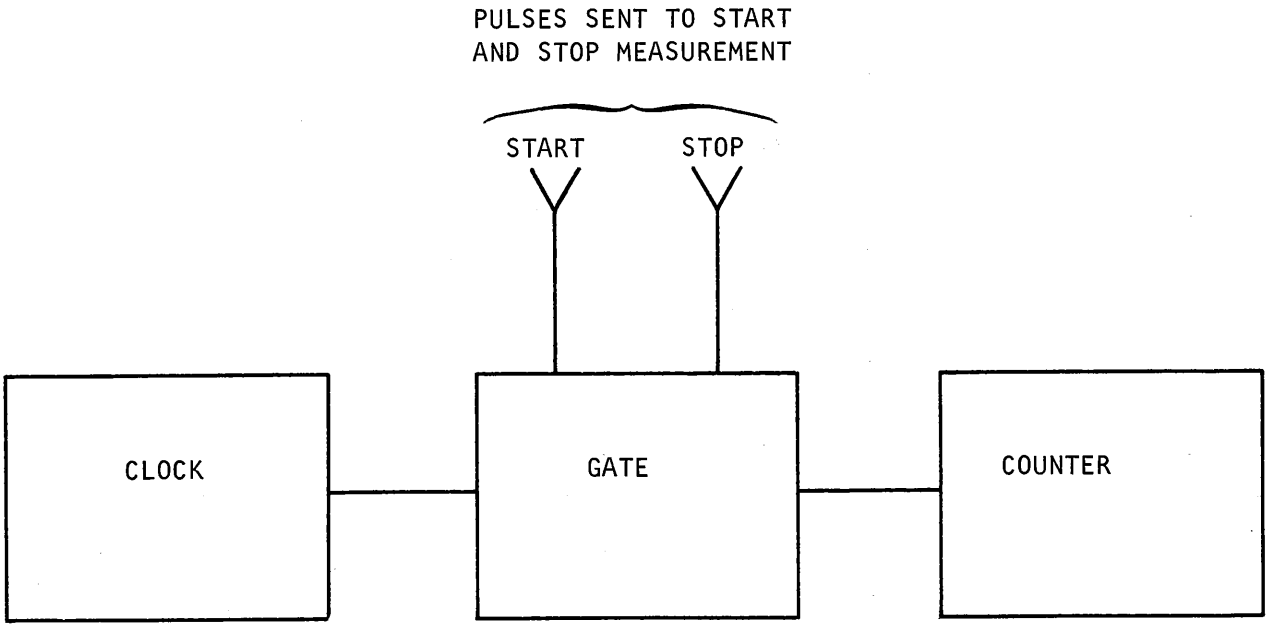

FIGURE 2 - 2

TIME MEASUREMENT SYSTEM

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The method used in most digital voltmeters is to use a calibrated sweep generator similar to the fast ramp and comparator used in sampling oscilloscopes.

The gate is turned on when the ramp voltage passes a beginning voltage level and turned off when the ramp passes an ending level. DC levels representing the voltage differences to be measured are each applied to one side of comparators. The ramp voltage is applied to the other side. When the voltages match, a pulse from the comparator is fed to the gate. One turns it on, starting the count; the other turns it off, stopping the count. The comparators are like the delayed sweep comparator in the 535-545 scopes.

1. Figure 2-3 is a block diagram of this type of system. One is for the start pulse and the other provides the stop pulse. Each of the comparators must be fed a DC level. This is the function of the memories, described later. The two DC levels correspond to the voltage difference to be measured.
2. The sweep, or ramp, voltage is held to an accurate slope. The slope of the ramp voltage is related to the clock time. For instance, if the ramp voltage rises 1 volt per 100 μsec, and the voltage to be measured is 3 volts (start to stop), the gate will be on for 300 μsec. If the clock operates at a 1 megacycle rate (1 pulse per microsecond), there will be 300 counts while the gate is on. The decimal point is placed after the 3 by mechanical switching. (Some digital voltmeters have circuits that automatically determine the range and place the decimal point. The 6R1A does not do this, since the volts/cm control on the vertical plug-in determines the range). The reading given in this example is 3.00.

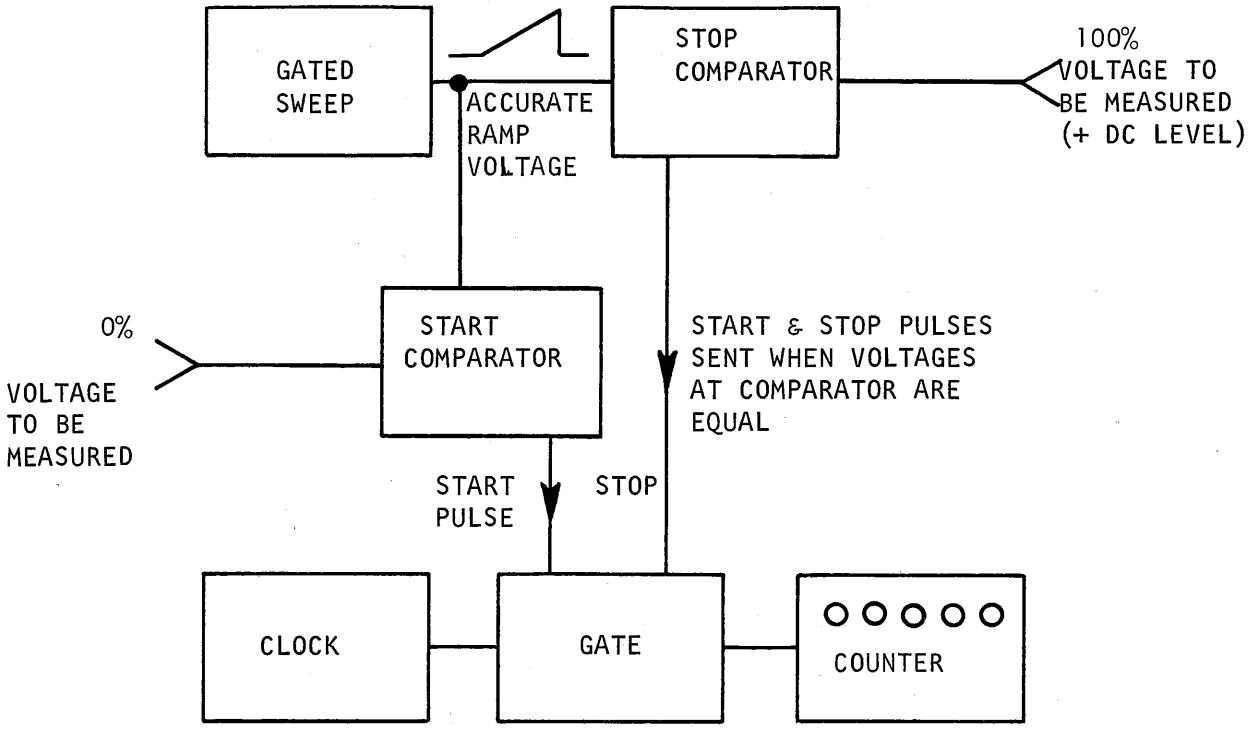

Figure 2 - 3
BLOCK DIAGRAM OF DIGITAL SYSTEM MEASURING VOLTAGE

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3. Resolution of the voltmeter is one clock pulse interval. Accuracy is determined by the accuracy of the voltages sent to the gate control circuits, the jitter and error in the gate control circuits, the accuracy of the voltmeter ramp voltage, and the accuracy of the clock pulse generator.

D. Comparator circuits used for determining the start and stop points in voltage measurements were mentioned earlier. In the 6R1A, these comparator circuits are also used to start and stop the measurement when measuring time.

E. These are the basic circuit blocks, listed in a table, with the function of each described.

1. COUNTER:

   Advances one count each time a pulse is received. Displays count in decimal numbers (decimal numbers are the scale of 0 through 9). Counter has provision for display period after counting has ended, and reset to 0 before next count. Display has separately controlled decimal point and units of measure (mv, nsec, etc.).

2. CLOCK:

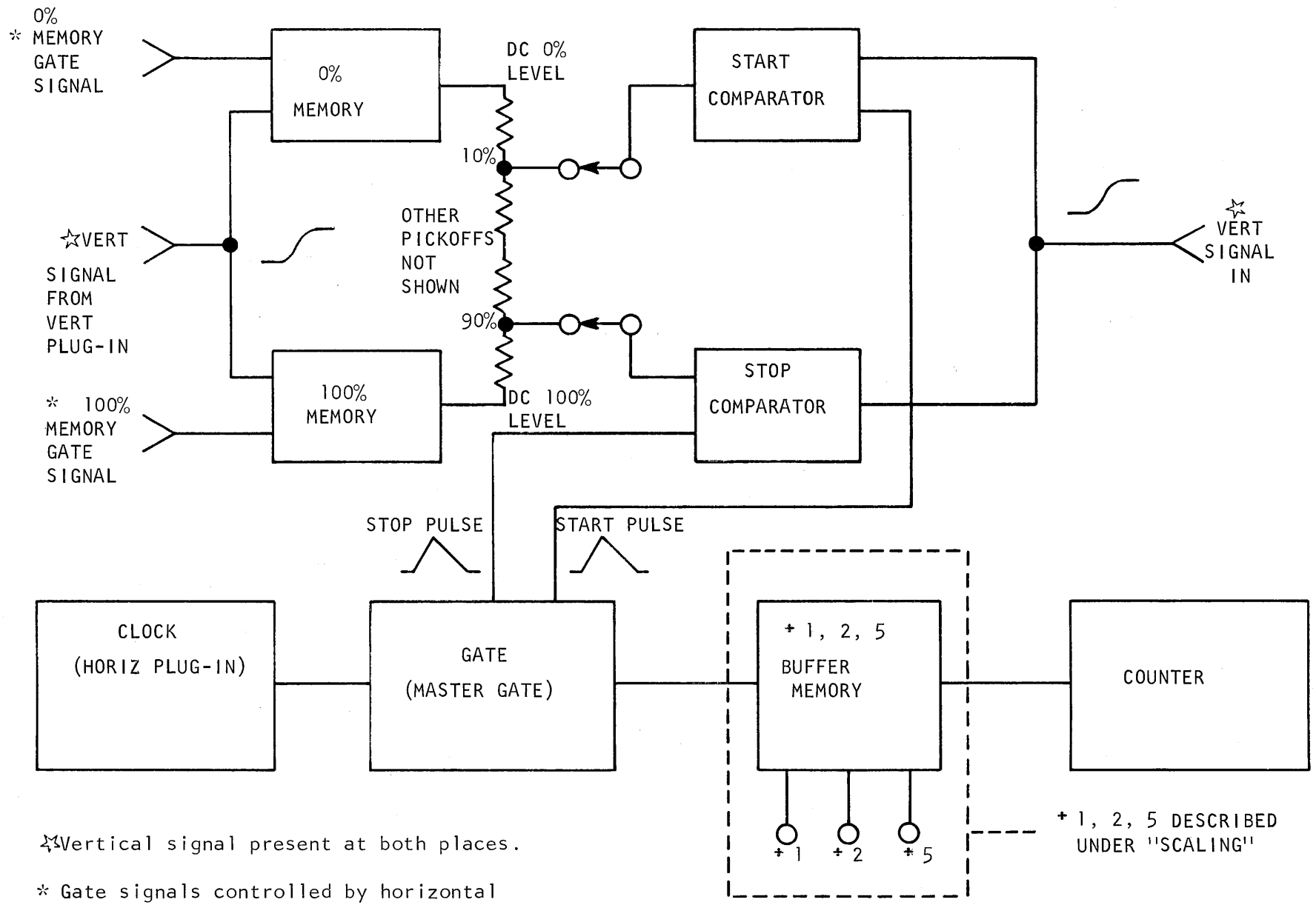
   A pulse generator that provides time-spaced pulses to operate the counter. In the 6R1A system, the clock for time measurements is located in the horizontal plug-in. When a 3T77 is used, clock pulses are taken from the blocking oscillator that operates the staircase generator. These pulses represent fixed increments of time, and are equivalent to the crystal-controlled pulses in the real time (3B2) system. The voltmeter clock in the 6R1A system is separate, and is located on the voltmeter circuit card.

3. GATE:

   Connects pulses from clock to counter for the desired counting time interval. Gate receives a start pulse and a stop pulse to set counting interval. In the 6R1A system, the gate is on the master gate card.

4. COMPARATOR:

   Compares a rising voltage with a fixed one; when the voltages are equal, a pulse is generated. In the digital system, the moving voltage represents the quantity that is being measured. The DC level represents the criterion for measurement, set in by the operator. In the 6R1A system, two identical comparator cards are used; one for start, one for stop.



☆Vertical signal present at both places.

* Gate signals controlled by horizontal deflection signal + operator controls.

Figure 2 - 4
TIME MEASUREMENT IN 6R1A

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II. Connecting the digital readout described to an oscilloscope display.

A. An oscilloscope generally is used to measure moving signals (signals with AC components). The digital readout needs pulses that can be used to operate the gate.

1. For time measurements, the gate needs start and stop pulses that relate to the time between two events. For example, to measure risetime, the gate must turn on at 10% and turn off at 90% of the signal rise, allowing the counter to count in the interval between 10% and 90%. The comparators must supply a start pulse when the rise is at 10% and a stop pulse when it is at 90%. To establish the 10% and 90% points, the 6R1A system samples the signal at an operator-selected 0% point and stores the level and at a similar 100% point. Divider resistors can divide these stored levels to give the 10% and 90% (as well as a number of other) points. Figure 2-4 shows the circuit blocks used in the 6R1A.

2. To make voltage measurements, the same sampling of 0% and 100% points and storing in memories provide the voltages to be measured. With the ramp (sweep) voltage technique described, the ramp starts at some low voltage. As it rises through the 0% voltage stored in the memory, a comparator (start comparator) sends a gate-closing pulse. The counter then counts until the ramp passes the 100% voltage, when the stop comparator sends a pulse that stops the count (opens the gate).

B. The two measurements just described are examples of analog to digital conversion. The memories remember any voltage entered into them. The digital circuit counts to a number equivalent to the voltages, or the time that the signal takes to go between the two voltages.

1. ANALOG:

A measurement that is expressed in terms of a voltage,

shaft angle, or similar technique. The measurement is analogous to the quantity measured. An example is the horizontal deflection seen on a sampling oscilloscope, where the deflection is provided by a voltage analogous to time after a trigger signal. An analog readout can express an irrational number, such as pi (3.141, 592, 653, 589, 793, 238, 462, 643, 383, 28 .....) exactly.

2. DIGITAL:

A quantity that is expressed in numbers, a number of pulses, or any discrete quantity. There can be no irrational numbers, since each digit is a significant figure. The difference between analog and digital can be seen on an automobile speedometer. The speed needle is an analog display. The odometer is a digital display. The gearing that works the odometer is an example of analog to digital conversion.

C. Two memories and two comparators are used. One memory stores a 0% voltage; the other, a 100% voltage. The signals stored are the DC levels fed to the comparators. In the case of time measurements between 10% and 90%, the voltage difference between the memories is divided, before providing the DC levels to the comparators. (In some cases, set by the operator, the memories are not used. These will be discussed later). The moving level sent to the other side of the comparators, simultaneously, is the signal voltage, tapped off from a circuit in the vertical plug-in.

In the case of voltage measurements, the memories store the 0% and 100% voltages, and these are fed directly to one side of each comparator. The other side of each comparator is fed the calibrated ramp voltage. The time required for the ramp voltage to traverse the difference between the two stored memory voltages is the time the gate is closed, and analogous to the voltage difference.

D. The memories must be gated on for a short period of the display sweep to sample the 0% and 100% voltages. The locations of these zones, horizontally on the display, are determined by the operator. The horizontal deflection voltage is analogous to the horizontal position, and is used to let the memories sample at the desired points, horizontally. Operating controls allow the 0% and 100% zones to be placed anywhere on the horizontal display, independently, and separately for A and B signals. The memories are cathode followers with a capacitor across each grid circuit. The vertical signal is gated in for a short period at the selected point, and the memories retain the voltage until the next sample is taken.

E. The oscilloscope display shows the vertical and horizontal signals sent to the 6R1A. The 0% and 100% are movable, and the display must show where each zone is positioned. The 6R1A provides an intensification signal for the display when the memory gates are closed, to show this position. The horizontal position of each zone is shown by a short intensified portion of the trace. The zones can be identified by moving the zone positioning knobs and watching the display. A slide switch allows the intensification to be turned off, if desired. Another intensification circuit intensifies the trace for the duration of time measurements (while the signal gate is on). This intensification may also be shut off by a separate slide switch.

   1. When voltage measurements are made, there is no start-to-stop intensification. Voltage measurements are made between the 0% and 100% zones, independent of signal waveform.

F. SCALING: 1-2-5 sequence. The period of time or dimension of voltage that is actually measured is related to the display. If 2 cm are required to show a risetime, and the horizontal

display is 20 nsec/cm, the risetime is 40 nsec. If the display is at 5 msec/cm, the risetime is 10 nsec. The display must be scaled to show this.

1. Means must be provided (with sampling system) to allow for the 1-2-5 sequence of sweep time/cm settings. In the case of readings with the 3T77, the clock output from the timing unit drives the counter directly in the .1 μsecond/cm (and all other 1 positions) setting. With 100 dots/cm, 100 counts equals 0.1 μsec (or 100 nsec). In the next faster position 50 nsec/cm, 100 counts equals 50 nsec, half the former amount. Therefore, the counter has a divide-by-two circuit between the clock input and the readout sections. The counter counts only every other dot, and thus counts 50 counts for each centimeter the horizontal display traverses. In the next position, 20 nsec/cm, a divide-by-five circuit is used, and the counter advances once for every five dots, giving 20/cm. In the next position, 10 nsec/cm, the decimal is moved and the counter reads clock pulses directly, so that 100 pulses are read as 10.0 nsec on the counter. The dividing circuit is controlled by contacts on the time/cm switch. With real time display, no division is needed, because a real time clock is used.
2. With the real time and sampling systems, the voltage display must be similarly scaled by the divide-by two or five buffer memory to correct the reading taken in the 5 or 2 positions of the volts/cm (or millivolts/cm) switch. In the 1 positions, no division is necessary, and the counter reads the clock directly.
3. In the 6R1A, the divider-by circuit may be set in the undivided position (1 position) by moving the RESOLUTION control to UNSCALED. No change in a count will be seen with a voltage reading in the 1 position of the volts/cm

control, but the change will be seen in 2 or 5 positions of the volts/cm control. This is a simple check for proper operation of the buffer circuit.

G. SCALING: Decimal position. The decimal point and the units multiplier must be chosen, also. The units multiplier (μ, n, etc., in the right nixie) is contolled by the plug-in controls. The decimal is controlled both by plug-in controls and by the RESOLUTION switch on the 6R1A.

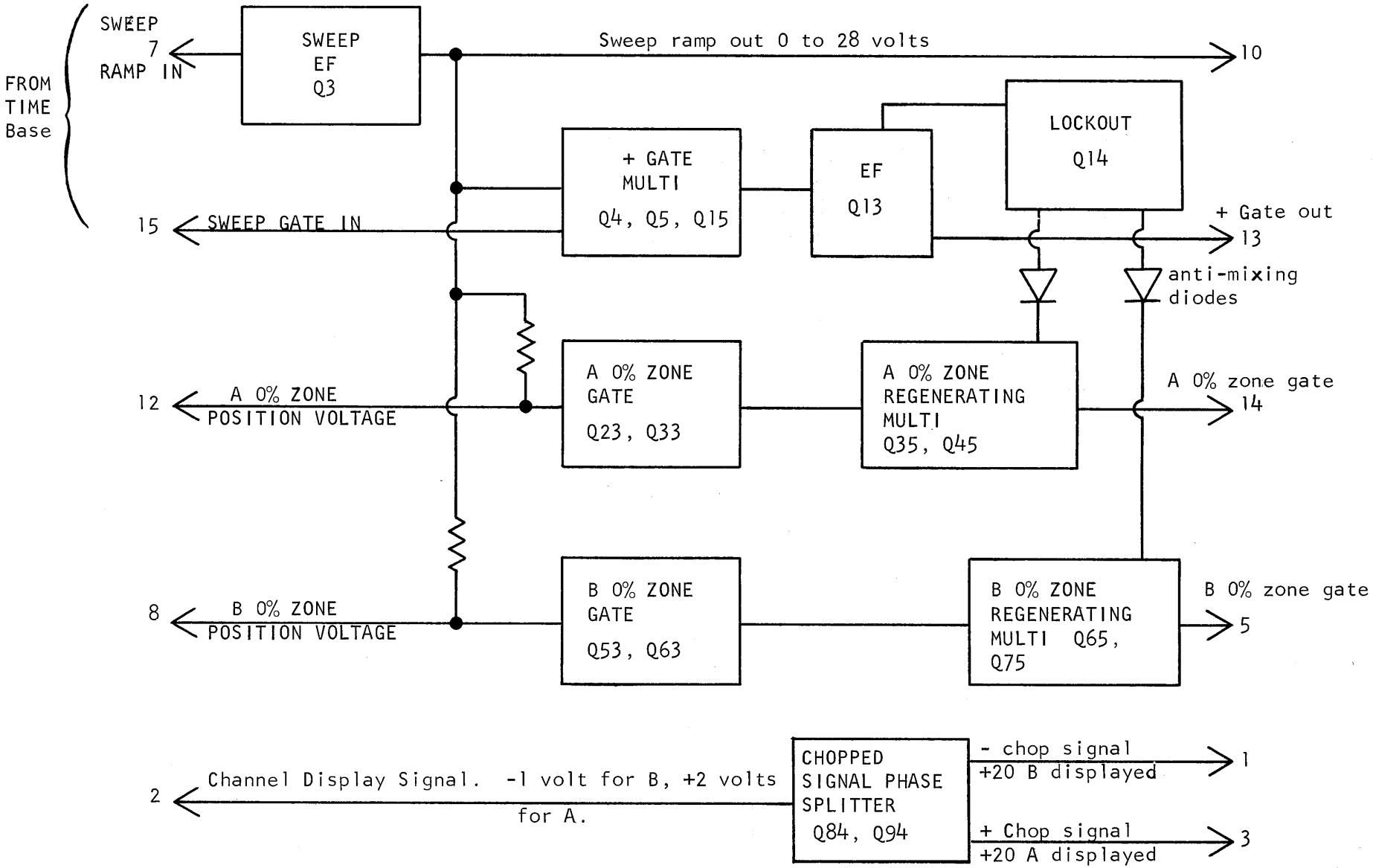
1. With the 3T77, the decimal position and units multiplier are both set by the TIME/CM control. The setting remains constant through the 1 position and next faster 5 and 2 positions. The multiplier changes from μ to n as the rate is increased from 20 to 10 nsec/cm. In addition, the decimal point is shifted by the DOTS/CM switch. The equivalent time/cm in 100 dots/cm is ten times that in 10 dots/cm, as seen by the counter, thus the decimal must be moved one place left in 100 dots/cm.
2. With the 3B2, the clock rate is counted down from the basic 1 mc rate by four counters. Each of these divides the preceding rate by ten, giving clock rates of 1 μsec, 10 μsec, 100 μsec, 1 millisec, 10 millisec. Any one of these rates may be selected by a separate control. This control, labeled DIGITAL RESOLUTION also controls the decimal location and the units multiplier. Since all measurements are made in real time, and the clock sends pulses related to 1 μsec by powers of 10, there is no need for the divide-by two or five buffer memory to divide pulses. With the 3B2, the pulses are always fed directly to the counter.
3. With either system, the voltage measurements are controlled as described for the 3T77 time measurements. Both the divide-by two or five buffer memory and the decimal and units multipliers are selected by VOLTS/CM (MILLIVOLTS/CM on 3S3 or 3S76).

SECTION 3

BLOCK DISCUSSION OF THE CIRCUITS USED IN THE 6R1A

1. INTRODUCTION

The block discussion of the circuits refers to the actual circuits used in the 6R1A, and their location. A number of logic levels, important to the operation of the system, are mentioned. These levels are catalogued in Section 4, telling from what circuit they are derived, and their function in the system. It is more convenient to discuss the circuits themselves first. You may wish to refer to Section 4, if you find a logic level mentioned that you are not familar with. The logic levels in the 6R1A operate between ground and approximately +20 volts. The block discussion should be studied with a schematic of the particular circuit at hand. The block diagrams in this section are designed as aids in studying the full schematic. Block diagrams are not supplied for some circuits, since studying the actual circuit is easier than first studying representations. Block diagrams are provided where they aid the understanding of a circuit.



0% ZONE BOARD

Non-displayed channel is at ground.

Figure 3 -1

2. 0% ZONES

The A and B 0% zone gate generators are located on the same card. See Figure 3-1. These circuits mix the horizontal display ramp signal with a DC level set by the operator, and form short gate periods in which the 0% memories are allowed to take a sample. The DC levels and the sweep signal set the horizontal position of the 0% gate on the display.

1. The 0% zones are formed by gate-forming circuits. The output of Schmitt circuit is at ground, except for the +20 volt 0% memory "on" point. There are two identical circuits for A and B, that operate independently.

+ Gate (Plus Gate).

This circuit is also located on the 0% card. The circuit is an "and" circuit that requires sweep gate to be "on", and that the sweep be run up past the first 7%. This + gate signal, which rises to +20 volts after the first part of the sweep, is used to lock out the measurement functions for the first 7% of sweep. The + gate prevents a 0% zone from being formed until the + gate has risen to +20 volts. The "off" state of the + gate is ground. This circuit has outputs fed to the analog display (dead zone), memories, Master Gate, Voltmeter, and Comparators. When the + gate is in its "on" state, with an output of +20 volts, it allows the remainder of the 6R1A to operate.

Chopped signal circuit:

The A display signal from the vertical unit appears at the 0% zone board as a +2 volt signal when channel A is being displayed, and a -1 volt signal when channel B is being displayed. This appears regardless of the display mode setting. The signal is fed to polarity splitter circuit Q84 and Q94. When the A signal is displayed, the - CHOP output is at ground, and the + CHOP output at +20 volts. The reverse is true when the B signal is being displayed.

The chopped signal outputs are fed to the analog display circuit to control intensification of the desired trace.

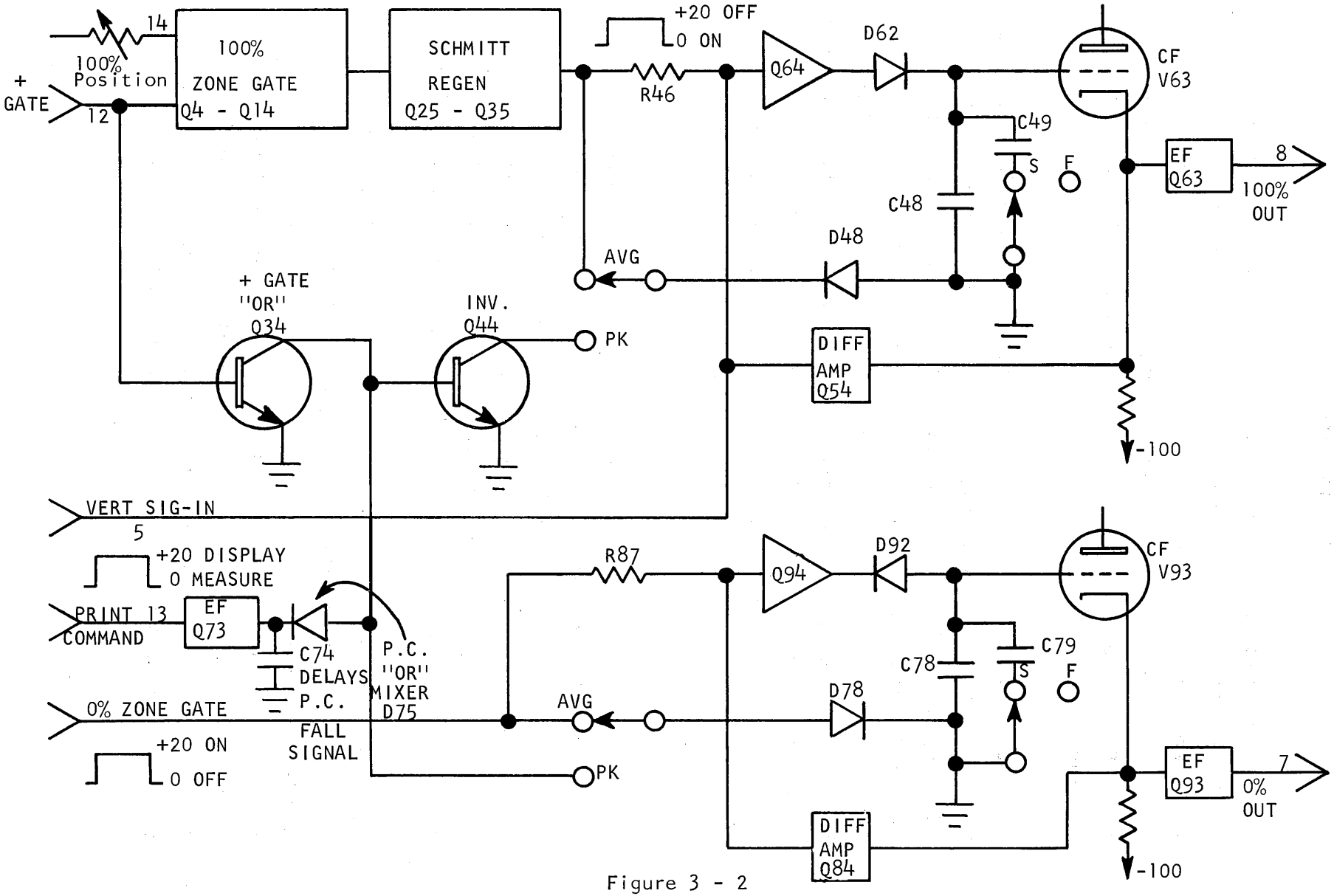


Figure 3 - 2
MEMORY BOARD

3. MEMORIES

The memories sample the vertical signal at specified points and retain the voltage levels for measurement. The sample points are determined by the 0% and 100% zone circuits. The 0% zone circuit is on a separate card, and the 100% zone circuit is on the Memory Card. One memory is used for each channel. Figure 3-2 is a block diagram.

Two operating modes are possible. When the memory is "averaging", the signal stored is the average voltage seen during the sample (shown by intensification on the CRT). When the memory is operated in "peak", the signal stored is the peak voltage seen during the sample period. The 0% memory remembers the negative peak, and the 100% memory remembers the positive peak. This polarity is independent of the START and STOP SLOPE switch settings on the 6R1A front panel. The 0% and 100% memory peak or averaging modes for each channel are individually controllable by slide switches on the memory board end.

1. 0%, Averaging Mode:

V93 is the memory cathode-follower. Capacitors C78 and C79 are connected between the grid and ground, and store a voltage that sets the cathode voltage. C79, the larger capacitor, may be disconnected for FAST response that allows the memory output voltage to change more quickly. Q93 is an emitter follower that isolates the V93 cathode circuit from the circuits connected to the memory output.

Q94 is the memory input amplifier. It is held turned off by bias source until the memory gate signal (0% zone) arrives. This signal brings Q94 base into the conducting range. The gate signal is mixed with the vertical signal which is inverted by Q84A. Q84 is two transistors in one case, and operates as a differential amplifier. Q84B base is fed current from the cathode circuit of V93, and allows Q84A to provide a signal that drives Q94 in the direction

needed to charge the memory capacitors.

D78 and D92 keep the collector circuit of Q94 disconnected from the memory capacitors except when the 0% zone gate signal is being received.

2. 0% zone, Peak Mode:

Operation is similar to that described for averaging. However, D78 and D92 take a different role. D78 is no longer connected to the + gate, but is connected to an "or" circuit that mixes the + gate and the print command signal. The print command signal is at ground when the system is measuring (master gate on), and this holds the emitter of Q73 near ground. The + gate is connected to inverter Q34, and when the + gate is at +20 volts (see 0% zone board), the collector of Q34 is near ground. Either of these states will hold D78 cut off. Q94 will conduct when the 0% zone signal is present, and discharge memory capacitors C78 and C79 through D92 to the lowest vertical signal level seen during the gate on period. Note that the charge voltage on the memory capacitors can only go down through D92. The capacitors will discharge to the negative peak seen in the gate period. The negative peak will be the 0% voltage measured.

When the measurement is completed, the master gate turns off, and the print command signal rises to +20 volts. This removes the ground signal present through Q73. When the + gate returns to 0 volts (at sweep end), the collector of inverter Q34 rises, allowing D78 to be forward biased, and the memory capacitors charge up to +20 volts, clamped by D34.

If the display period is through several sweeps, the memory capacitors will be charged down to vertical signal level during each sweep (when the + gate is up) and be discharged up during retrace. After the display ends, the print command signal goes down and Q73 holds D78 cut off.

The emitter of Q94 is also grounded by the PEAK switch to allow faster response in peak mode operation. This is needed because of the charge and discharge cycling of the memory capacitors. With fast real time measurements, using the 3A2-3B2, the FAST memory operation allows the voltage to change more quickly. Sampling systems are limited to 100 kc, and SLOW memory operation may be used. SLOW operation stabilizes the memory, since larger signals are needed to move the output.

A strap is provided to allow either the 0% zone signal or the + gate signal to operate the memory amplifier, Q94. The + gate position allows the memory to store the peak signal during the whole horizontal display, less the 7% dead zone where the + gate is at 0 volts. This is for use with the older 6R1, where the 0% zone position cannot be adjusted.

3. 100%, Averaging Mode:

Operation is similar to that of the 0% memory in averaging mode. However, the 100% zone forming circuit is located on the memory card. The zone forming circuit is similar to that of the 0%, with a gate circuit that requires the + gate signal plus a sweep ramp combined with offset signal that actually positions the 100% zone. This drives a Schmitt circuit that regenerates the gate signal into a 20 volts OFF, 0 volts ON signal. In the averaging mode, the 100% zone gate signal forward biases D48 and D62 during the measurement period. Differential amplifier Q54 provides a signal proportional to the change needed that drives the base of Q64. Q64 is reverse biased except when the 100% zone gate signal is on (at 0 volts). C48 is the fixed memory capacitor, and C49 is switched in by the SLOW position of the SLOW-FAST switch. V63 is the memory cathode follower, and Q63 the isolating emitter follower. Note that the operating polarities in the 100% memory (except the CF and EF) are opposite those of the 0% memory. This is important in peak operation, when the positive peak is to be measured.

The 100% zone gate, when on, is allowed to operate the analog display through D46. No inversion for the 100% signal is necessary, because the zone gate is inverted from that of the 0% zone gate.

4. 100% Peak Mode:

Operation is similar to that of the 0% peak mode, except that the polarity operating D48 and D62 is inverted. The "or" signal from Q34 and Q73 is inverted by Q44, which is turned off while the memory is measuring. This back-biases D48, allowing the most positive signal to flow through D62, charging up the memory capacitors. When both "or" signals are positive, Q44 is forward biased, and D48 is forward biased, discharging the memory capacitors. Note that in this case, the positive peak is stored, and the capacitors are discharged in the negative direction. The discharge takes place during display (print command at +20) and retrace-dead zone (when the + gate is at 0 volts).

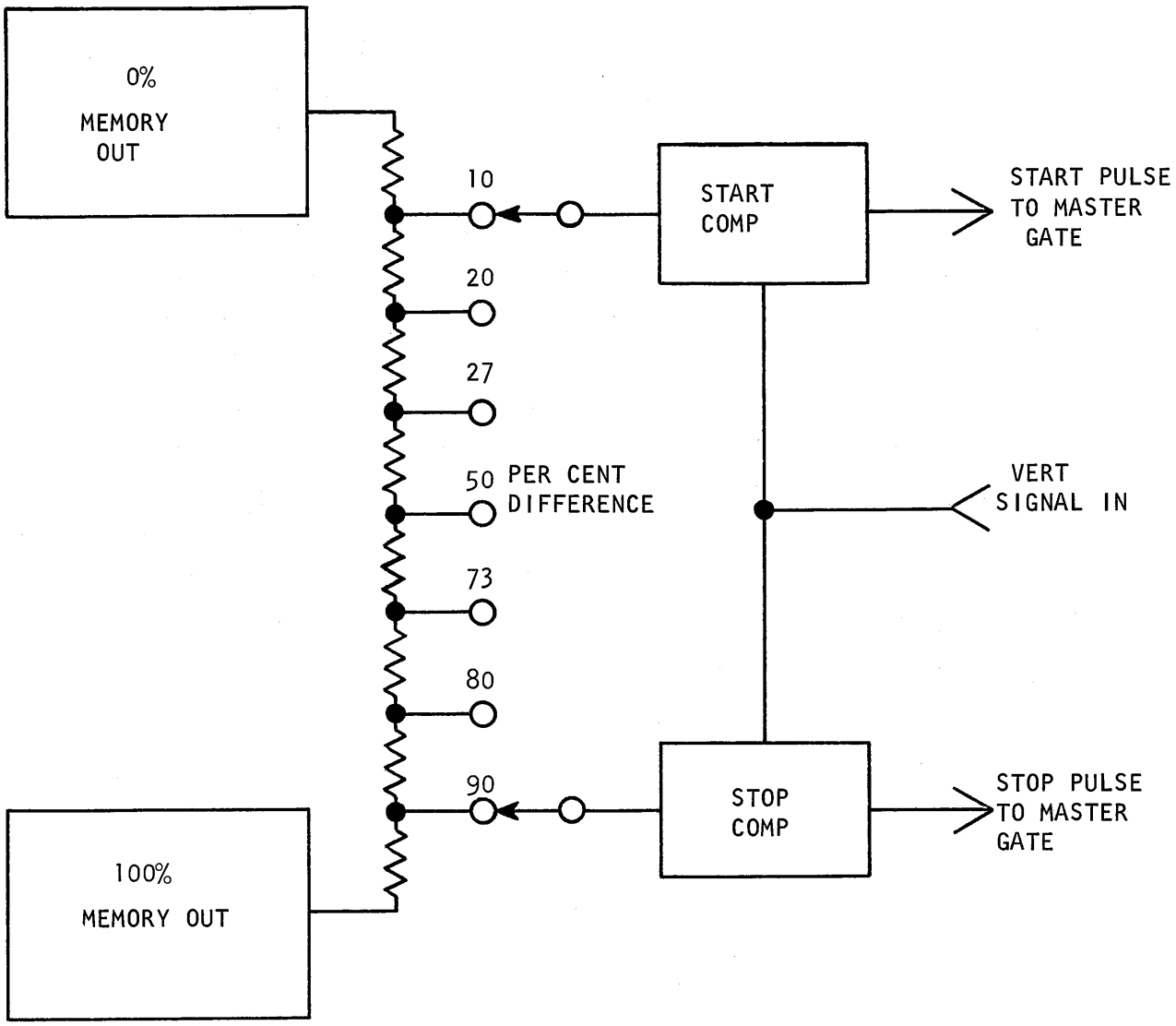


Figure 3 -3

TIMING START-STOP
TIME COMPARISON

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4. COMPARATOR

There are two identical comparators, one for start, and one for stop. The comparator receives two signals: One is a DC level that comes from one of four sources, depending on MODE switch setting and, in TIME mode, on the settings of the TIMING START and TIMING STOP switches.

1. + VOLTAGE MODE

The DC level for the Start Comparator (fed to pin 9) comes from the 0% memory directly; and for the Stop Comparator, from the 100% memory directly. The moving level comes from the voltmeter ramp directly to pin 8 of each comparator.

- VOLTAGE MODE

Same as + voltage mode, except that the 100% signal goes to pin 9 of the Start Comparator, and the 0% signal goes to pin 9 of the Stop Comparator. This allows the rising ramp voltage to compare at the Start Comparator first, and at the Stop Comparator second.

2. TIME MODE Start & Stop selected by TIMING START (STOP) switches.

The start and stop DC levels are selected by a resistive divider that divides the voltage difference between the 0% and 100% memory output. See Figure 3-3 for a diagram of the divider in relation to the comparators and memories. The illustration shows the setup for a typical 10 to 90 per cent measurement. The diagram is simplified. Actually, two dividers, one for start and one for stop, are used. The memories can be either the A trace or B trace memories. When + slope is selected, the DC level is fed to pin 9, and the moving vertical signal to pin 8. For - slope comparison, the connections are reversed. This is because the comparator must see either a rising voltage at pin 8, or a falling voltage at pin 9.

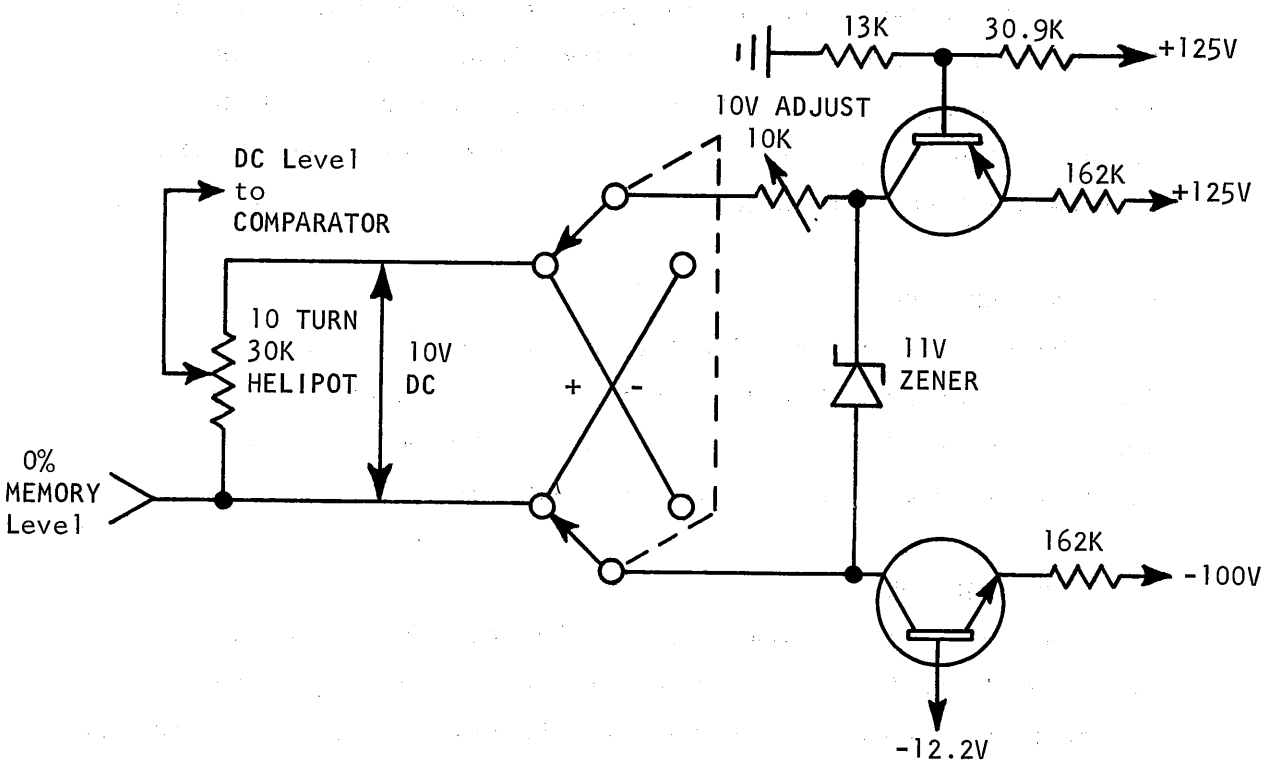


Figure 3 - 4
COMPARATOR
FLOATING VOLTAGE SUPPLY

3. TIME MODE Start and Stop selected by MANUAL knobs (red knobs).

The horizontal deflection signal from the time base unit is fed to the comparators pin 8. A fixed signal is obtained from each MANUAL potentiometer and fed to each comparator pin 9 as the DC level.

4. TIME MODE Start and Stop selected by Helidial.

There are two floating voltage supplies, located on the voltmeter circuit card. These supplies are fed by two constant current transistors that allow voltage isolation of the supply. A diagram of the start circuit is shown in Figure 3-4. The stop circuit is identical.

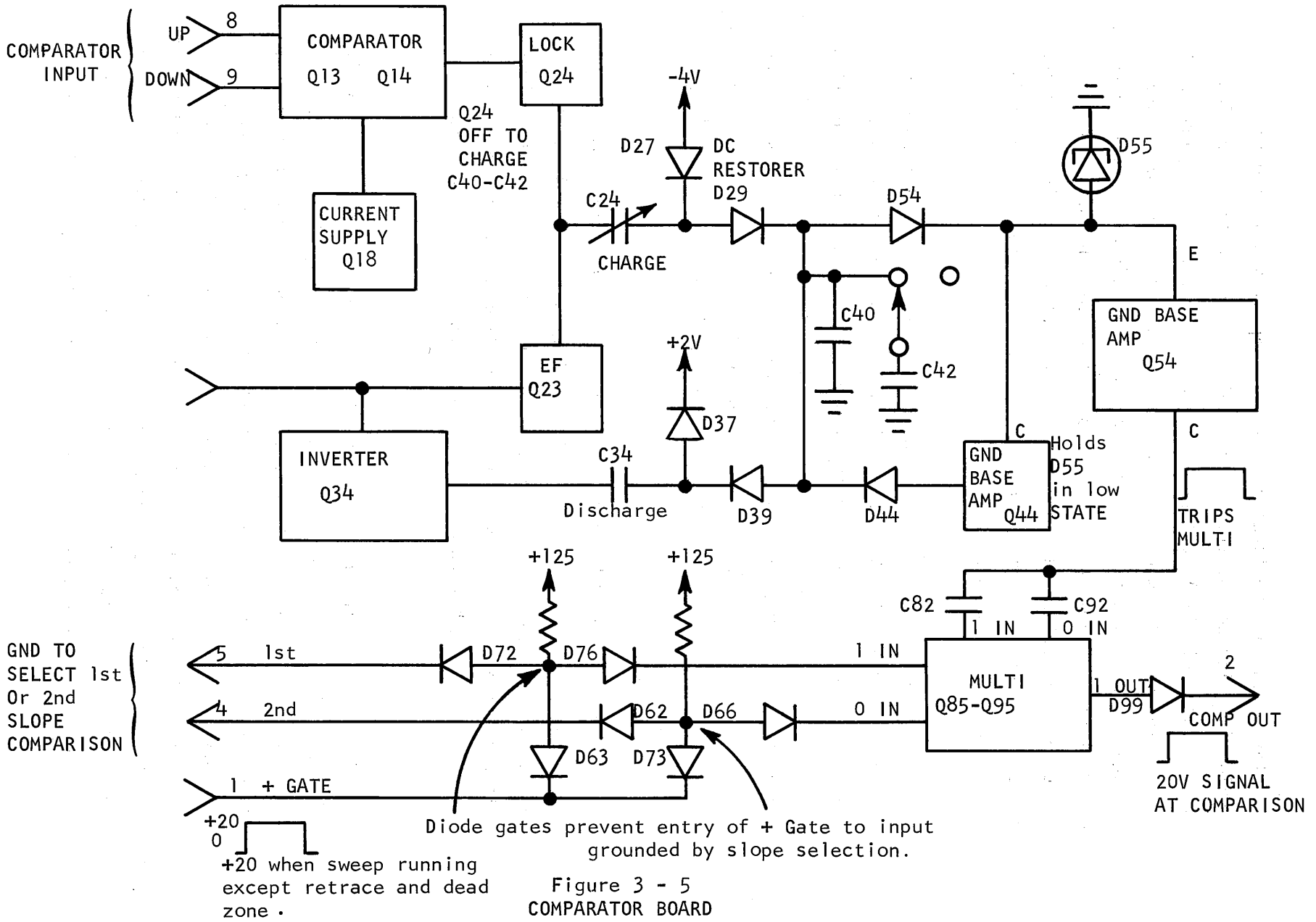


Figure 3 - 5
COMPARATOR BOARD

The output of the floating voltage supply is adjusted to provide 10 volts across the 10 turn helipot. Since the input from the vertical unit is 1 volt per vertical centimeter of display, each turn of the helipot equals 1 centimeter of offset. The 0% memory voltage is used as a ground reference, and the offset is referenced to the 0% zone. A polarity reversing switch allows the offset to be positive or negative. The 0% zone plus offset voltage is fed as the DC level to the comparator, and the vertical display voltage is fed to the moving level input.

The signal comparator provides an output signal pulse when the moving voltage equals the fixed voltage. Figure 3-5 shows a block diagram . The input to pin 8 must move up with relation to the input to pin 9; in practice a rising signal is connected to pin 8 or a falling signal to pin 9. Operation is similar to that of the delayed trigger comparator in a 535. Q18 is a constant current transistor that allows a sharp output when Q13 and Q14 shift conduction, as input voltages become equal.

The output from Q13B cuts off inhibiting transistor Q24. Clock pulses then may be seen at the emitter of Q23. Clock pulses pass through a diode to charge capacitors C40 and C42. After three clock pulses are charged into the charging capacitors, a tunnel diode (D55) is lifted to the high state. The tunnel diode drives grounded base amplifier Q54.

The charging circuit is balanced by discharging circuit Q34 and Q44. When inhibiting transistor Q24 is conducting (before comparison), clock pulses discharge C40 and C42. When the voltage on C40 and C42 reaches about -5 volts, D44 and grounded base amplifier Q44 pass the discharge current. This keeps D55 in the low state. When comparison is reached, Q24 is cut off. Clock pulses pass through C24 and transfer a higher positive charge to C40 and C42 than the discharging circuit draws out. C24 is adjusted so that three clock pulses must charge C40 and C42 before D55 can be raised to the high state. The delay is

provided so that the comparator must remain in the "compared" condition (Q24 cut off) for three clock pulses. This delay prevents noise from switching the comparator and tunnel diode, preventing false start or stop signals from reaching the multivibrator. The delay can be switched out, if desired; the switch was installed to guard against some future application that might require comparing on one dot. The delay should be left switched in on both comparators, allowing the 3 dot delay to cancel itself out. Generally, switching the 3 dot delay out introduces random errors in measurement, and use of the OUT position is confined to calibrating.

Multivibrator:

The multivibrator regenerates the tunnel diode signal for use by the Master Gate. It is also used to divide by two, allowing comparison to take place on the second slope selected, rather than the first. There are two inputs to the multi. One is a selected "jam" circuit that presets the multi, using the + gate signal as a trigger signal. The other is the tunnel diode output, that is commutated by a pair of capacitors and diodes. When the collector of Q95 is at +20 volts, the multi is in the "one" state. Turning on Q95 raises its collector from ground to +20 volts, and provides the signal that operates the master gate. The return to the "zero" state provides no output pulse.

The transistor to be turned off, in the multi, is selected by three diode logic in each base circut. Grounding the three diode logic in the base circuit of Q85 allows the + gate signal to enter the base circuit of Q95, turning Q95 off. This puts the multi in the "zero" state. This is followed by D55 switching to the high state, as a comparison is made. The signal from D55 is fed to the base of Q85, turning it off and putting the multi in the "one" state. The first signal that operates the comparator will operate the multi to regenerate a positive signal and operate the master gate. This is FIRST SLOPE operation. In SECOND SLOPE operation, selected by the operator, the three diode logic in the base circuit of Q95 is

grounded, allowing Q85 to be turned off by the + gate signal. This puts the multi in the "one" state. When the first comparison occurs, Q95 is turned off, and the multi is put in the "zero" state. No signal is sent to the master gate. When the second comparison occurs, the multi is switched back to the "one" state, and a signal sent to the master gate. Note that the comparator must switch to the compared state, raising D55, return to the low state again, dropping D55, and rise back to the compared state, raising D55 to the high state a second time.

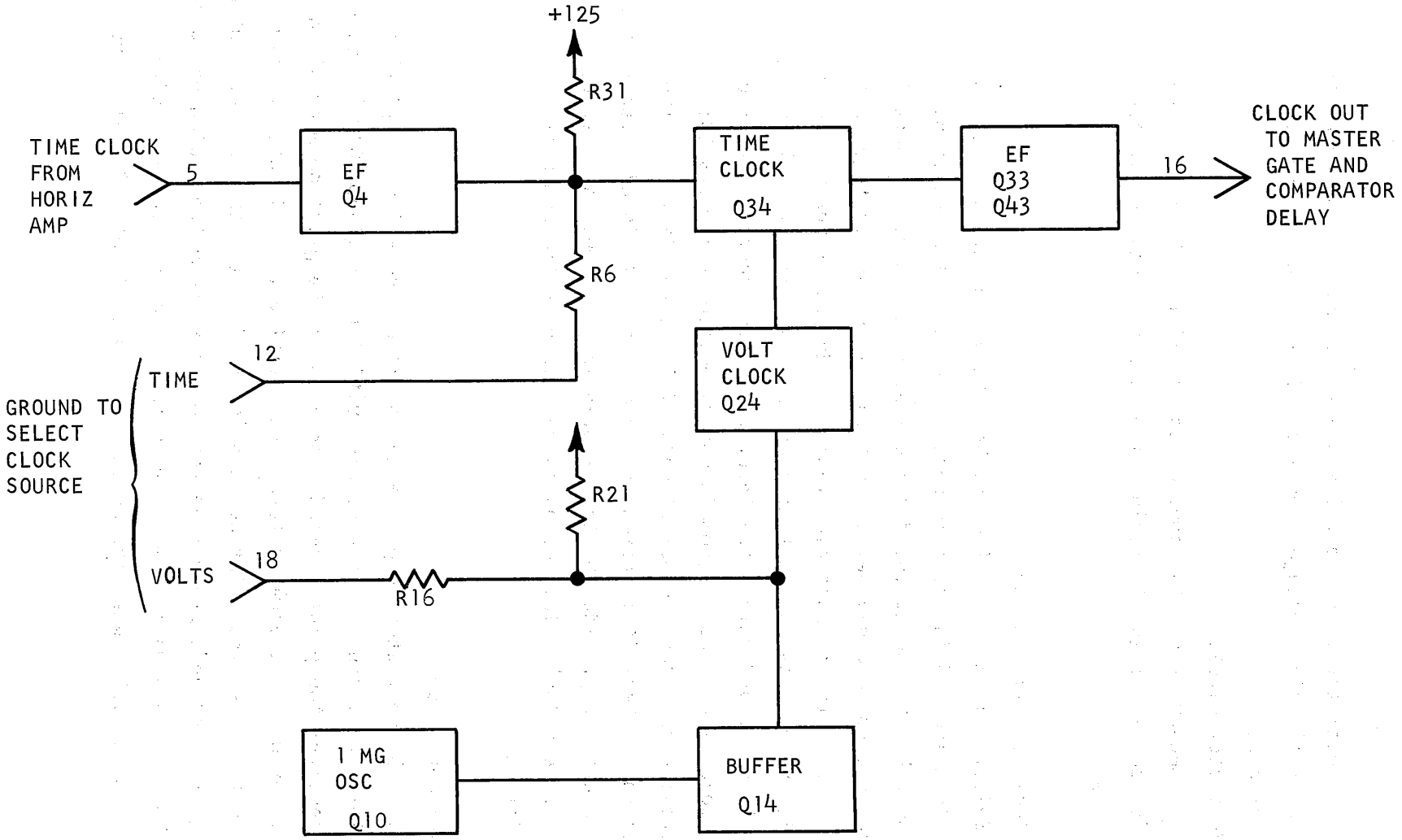


Figure 3 - 6

VOLTMETER CLOCK
AND CLOCK SELECTION

5. VOLTMETER

The voltmeter board contains several sections, including the comparator floating voltage supplies. Sections other than the supplies are:

1. Voltmeter clock.

A 1 megacycle crystal controlled oscillator (Q10) followed by a buffer amplifier (Q14) provides 1 mc clock signal for voltage measurements.

2. Clock selection circuit.

Selects clock pulses from either the voltmeter clock or the time clock located in the time-base plug-in. Selection is by the MODE switch. Grounding the desired lead (see diagram, Figure 3-6) completes a voltage divider circuit that sets base voltage on a transistor in the forward bias region. Q24 passes the voltage clock signal, and Q34 passes the time clock signal. Inverter Q4 in the time circuit standardizes the input for proper operation of the clock selection circuit. Complementary emitter followers Q33 and Q43 provide the clock output signal. This signal is fed to the master gate, where it is gated to the counter. It is also fed to the comparators, to provide the three-dot-delay in comparison (three clock pulse delay). This delay is described in the comparator description.

3. Voltmeter ramp.

a. The voltmeter ramp is a gated miller operational amplifier. The gate circuit is a bistable multivibrator (Q115, Q125). Q104 receives the print command signal; when the print command signal is at 0 volts, Q104 is turned on, raising its collector to +20 volts. When the print command is at 20 volts, the collector of Q104 goes to ground, preventing the voltmeter ramp from being gated on. The + gate signal is mixed with the collector signal of Q104, through C102. When the collector of Q104 is at +20 volts, the

rising signal of the + gate turning on (0 to 20 volts) passes through D105 to turn Q115 off. The collector of Q115 drops from +20 volts to ground, cutting off the reset current through R1130 and D1132.

The output signal of the voltmeter ramp, rising toward +20, is fed through D156 to the other multivibrator transistor, Q125. When the output voltage reaches about 18 volts, D156 is forward biased to turn Q125 off, Q115 on, and reset the voltmeter ramp. At the same time the voltmeter ramp voltage is fed to the base circuit of Q104, where it prevents the signal from the + gate from entering the multi again until the voltmeter ramp has been reset.

b. The ramp generator is an operational amplifier with capacitive feedback (Miller integrator). Q141 is the amplifier, and Q153 is an emitter follower, supplying the low impedance output current. During the runup cycle, current through R140 and R141 (adjusted to give 100 μsec/volt rise) charges C140; the amplifier raises the voltage on the other side of C140 to keep the current through the resistors relatively constant. The resulting linear voltage ramp is fed through pin 17 and the mode switch to both comparators as the moving voltage, comparing with the fixed memory levels (0% and 100%).

c. The ramp gate (+20 off, ground on) is fed to the master gate. This gate signal is used to prevent reset of the counter gate before the voltmeter ramp has completed its runup.

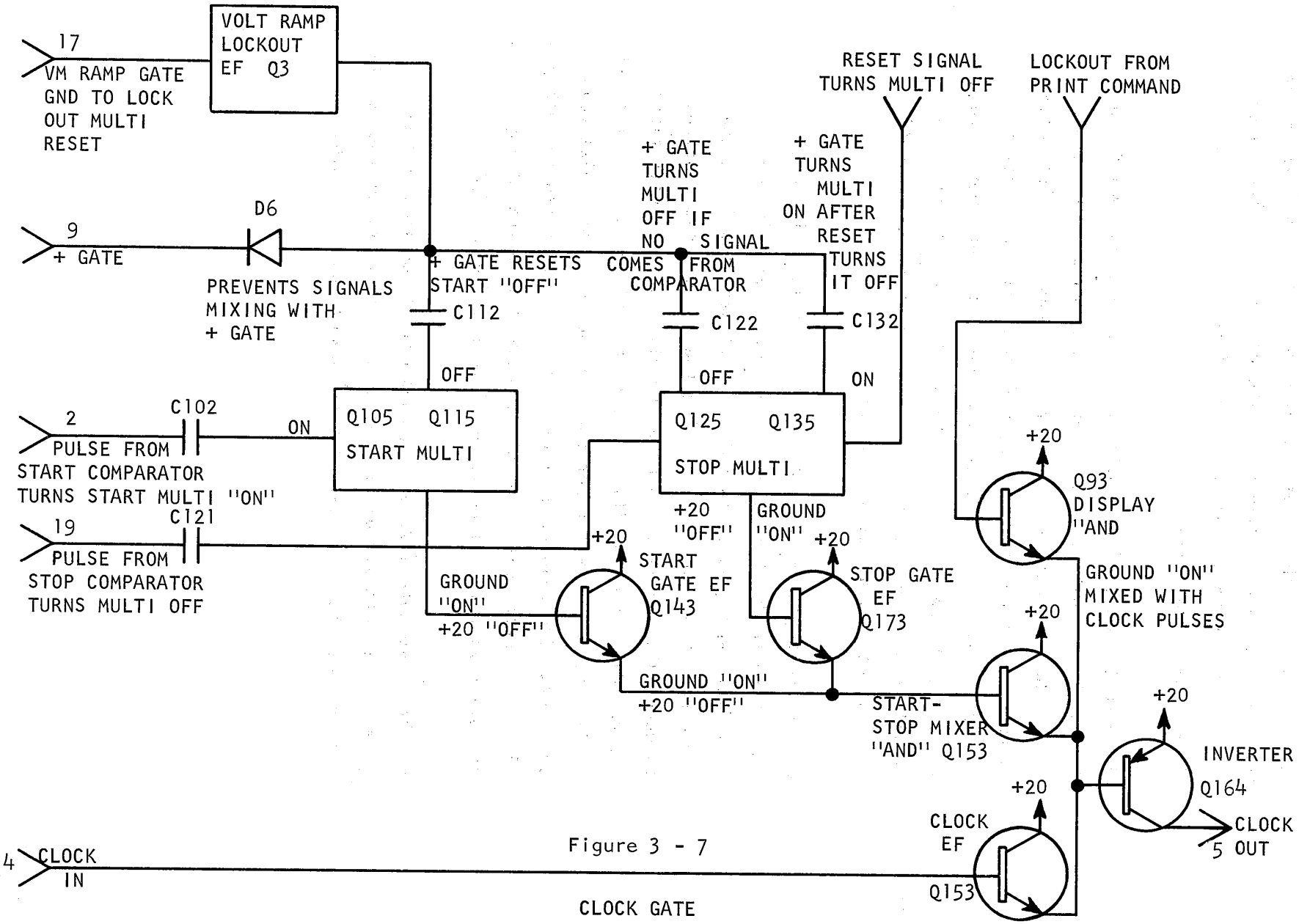

17
VM RAMP GATE GND TO LOCK OUT MULTI RESET
VOLT RAMP LOCKOUT EF Q3
RESET SIGNAL TURNS MULTI OFF
LOCKOUT FROM PRINT COMMAND
9
+ GATE
D6
PREVENTS SIGNALS MIXING WITH + GATE
+ GATE RESETS START "OFF"
C112
+ GATE TURNS MULTI OFF IF NO SIGNAL COMES FROM COMPARATOR
C122
+ GATE TURNS MULTI ON AFTER RESET TURNS IT OFF
C132
OFF
OFF
ON
2
PULSE FROM START COMPARATOR TURNS START MULTI "ON"
C102
ON
Q105 Q115
START MULTI
Q125 Q135
STOP MULTI
19
PULSE FROM STOP COMPARATOR TURNS MULTI OFF
C121
+20
"OFF"
GROUND
"ON"
+20
Q93
DISPLAY
"AND
+20
START GATE EF Q143
GROUND "ON"
+20 "OFF"
+20
STOP GATE EF Q173
GROUND "ON" MIXED WITH CLOCK PULSES
GROUND "ON"
+20 "OFF"
+20
START-STOP MIXER "AND" Q153
+20
INVERTER Q164
CLOCK 5 OUT
+20
CLOCK EF Q153
4
CLOCK IN
CLOCK GATE

Figure 3 - 7

6. MASTER GATE

The master gate has the clock gate circuit that controls the period that the clock pulses reach the counter. It also has a circuit that provides the display interval, and resets the counters.

1. Start and stop multis and clock gate.

The start and stop multivibrators are bistable multivibrators. Of the several possible combinations of stable steps that the two multis can be in, only one will allow the clock gate to pass clock signals to the counter. This will be called the "on" combination, when both multis are in the "on" state.

The clock gate (see Figure 3-7) consists of a series of emitter followers with emitters connected together. Raising the voltage on any one base will raise the emitter voltage on the bus, cutting off all the other transistors. There are three of these emitter followers. One (Q93) receives a lockout signal from the print command (display) circuit. The second (Q153) receives a signal from either stop or start multi (through separate emitter followers). The third (Q163) is not a lockout transistor, but is an emitter follower that transfers the clock signal to the common bus when Q93 and Q153 are cut off. This series of transistors is known as an "and" gate because the base voltage on Q93 and Q153 must be at ground for the clock signal on Q163 to pass into the emitter bus.

2. Display circuit.

The display circuit provides a print command logic level that divides the count and the display periods. The print command signal is at ground potential during the counting period, during which time measurements are being made. In peak memory mode, the memories are not being discharged during retrace. A block diagram is shown in Figure 3-8.

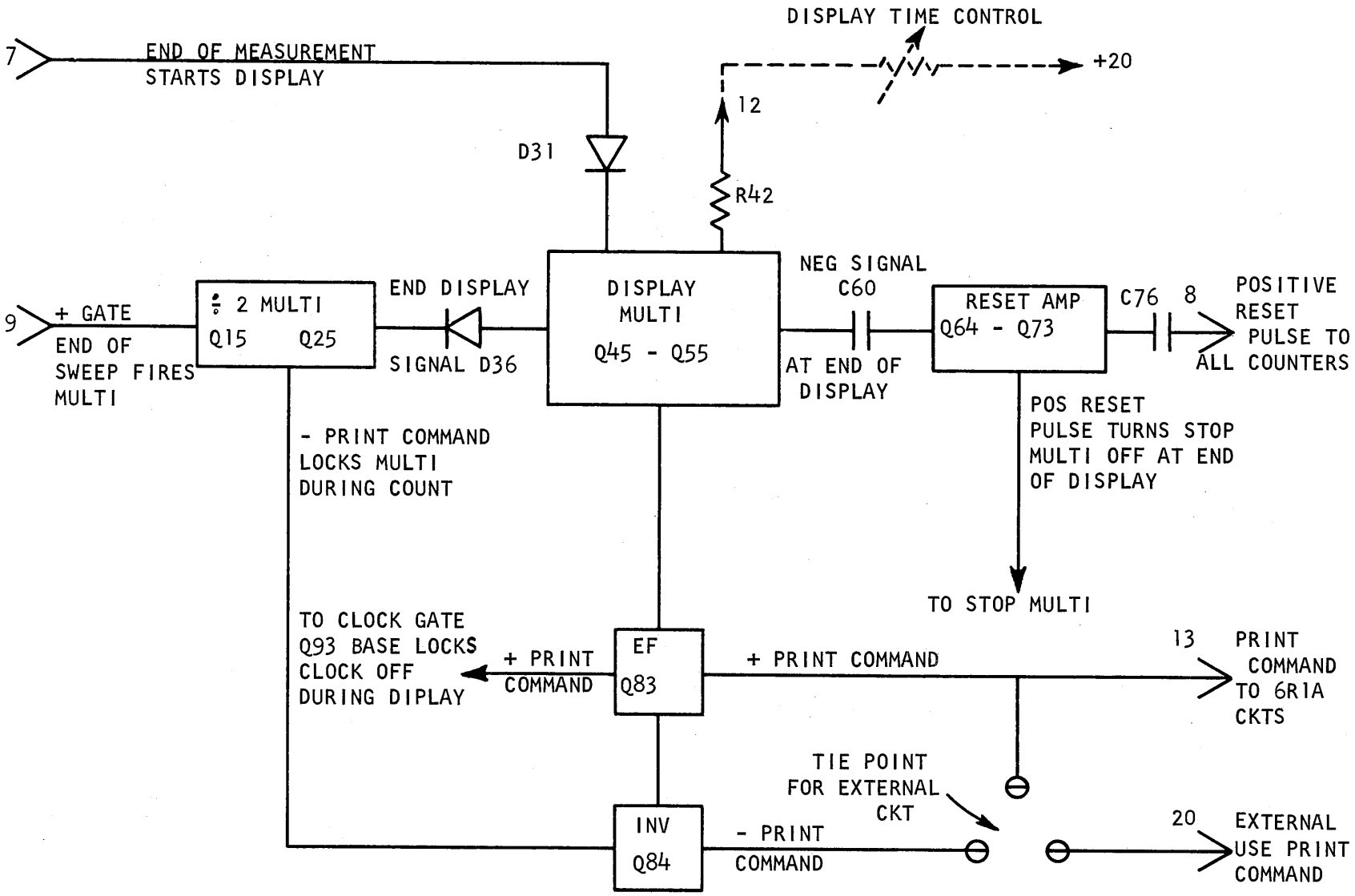


Figure 3 - 8
DISPLAY CIRCUIT

When the display period starts, at the end of a measurement, the signal from the stop multi trips another multi to raise the print command signal to +20 volts. This signal remains at +20 volts for the duration of the display period. The 20 volt print command signal allows the memories to be cycled (peak mode operation) and prevents the voltmeter from operating the clock gate from turning on. It also operates the analog display that operates the limit lights. A positive or a negative print command pulse may be taken from pin 20 of the master gate by making an interconnection on the master gate board between two of three studs located near the board plug.

The multivibrator used is not an Eccles-Jordan type, but a circuit that has both transistors (Q45 and Q55) either off or on simultaneously. During the count period, the transistors are both on. The end of measurement pulse, that comes through terminal 7, is obtained through the **RESOLUTION** switch from either the stop multi directly or the divide-by-ten circuit. In high resolution, ten stop pulses must be received by the divide-by-ten circuit (located on its own circuit board) before a regenerated signal is fed to the display multi.

The positive end of measurement pulse turns both multi transistors off. Q45 takes no base current, once turned off, and C42 charges toward +20 volts through the **DISPLAY TIME** control. At the end of this charging, both transistors have neither forward nor reverse bias (no voltage from base to emitter).

Before the end of measurement, the negative print command output from Q84 (used only as a logic level for the divide by two multi in the 6R1A) lifts the base of Q25, keeping it on and Q15 off. At the end of measurement, the divide by two multi becomes balanced, and can operate in the normal Eccles-Jordan manner. The + gate will switch it back and forth on each sweep. Assume a condition where the end-of-measurement (coincident with stop multi switching) occurs in mid-sweep,

but after zone measurements. The end of measurement signal will cause the peak memory to discharge at the end of the sweep. If the display period were short, measurement could begin on the very next sweep, assuming a long sweep time/cm. With nothing stored in the memories, at the beginning of sweep, the comparators could not operate properly, and a false measurement would be made, even though the memories received level information during the sweep. The divide-by-two multi provides a pulse that returns the print command to ground (back to count) only at the end of a sweep, when the + gate drops down. The memories will not be discharged when the print command is reset because there is some delay in the logic for the peak memories (on memory boards). Thus, the delay while circuits operate between drop of the plus gate and reset of the print command is not seen in the memory, because of delay provision. This keeps the memory charged for the next measurement.

Assume another case, with the same conditions. We have a short display time, a long sweep time/cm, and will now assume that the end of measurement comes near the beginning of the sweep. If there were not a dividing counter, the display interval could be over and the print command would reset at the end of the same sweep, with no whole sweep intervening between end of measurement and end of display. There would be no discharge of memory capacitors. Any leakage currents could drift the charge on the memory capacitors away from the actual peak signal stored on them, and spoil the next measurement. The drift would have to accumulate over several measure and display cycles; however, this could easily happen, since the end of measurement will come at the same place with a repetitive signal. While direction of drift cannot be predicted, we must assume that the 0% memory will drift more negative, and the 100% memory more positive, over a period of time.

The divide-by-two circuit must provide a negative pulse to turn the display multi on at the end of a sweep. The - print command signal holds the divide-by-two multi so that the next + gate return will

provide a positive signal at the collector of Q25. This will not reset the display multi, and will allow the memories to discharge during reset to the next sweep, even if the display circuit is ready to return to the counting mode.

3. Print command

The print command gate used in the 6R1A is a signal that is provided by the display multi, driving emitter follower Q83 for isolation. It is at ground when the system is counting, and at +20 volts when the system is displaying. The - print command signal provided by inverter Q84 is not used by the 6R1A except to hold Q25 on during the count period.

7. DIVIDE-BY-TEN

This card has four Eccles-Jordan multivibrators. The function is to provide an end-of-measurement signal when the tenth stop pulse is received from the master gate. The divide-by-ten board provides the end of measurement signal only when the RESOLUTION switch is in the AVERAGE OF TEN SWEEPS positions. In the ONE SWEEP position, the divide-by-ten board is bypassed.

The first bistable multivibrator, Q5 and Q15, is conventional, and divides the signal by two. The second, third, and fourth have feedback coupling that reduces the divide-by-eight that would normally come from a series of three binary counters to a divide by five.

The feedback is from the collector of Q45 to the base of Q35. Assume that the multis are in the 1 (one) state when the left transistor is on, and in the zero state when the left transistor is off. To identify the multis, the second multi is Q25-Q35, the third multi is Q45-Q55, and the fourth multi is Q65-Q75. In normal notation, 1011 would indicate that the fourth multi is in the one state; the third in the zero state; the second and first in the one state. In normal counting, the second pulse received by a multi would return it from the one to the zero state, and advance the next multi one count.

Operation of the feedback with binary counting is thoroughly explained in the instruction manual for the 6R1A.

8. DIVIDE BY 1, 2, 5 BOARD

This board is used for scaling clock pulses before they are fed to the counter, and can supply clock pulses directly ($\div$ 1) or through either of two buffer memory circuits ($\div$ 2 or $\div$ 5). Selection of the desired output is accomplished through grounding a voltage divider resistor for the base circuit of one of three transistors. Q44 provides the divide-by-five output; Q74 the divide-by-two output; Q84 the straight through divide-by-one output.

The divide-by-one circuit is simply a straight through inverter, Q84.

The divide-by-two circuit is a single Eccles-Jordan multivibrator, Q65 and Q75. It provides an output pulse each time Q75 turns on, turning Q74 off. The reset pulse at the end of display returns this multi to the Q74 off state at the beginning of each measurement. This means that odd numbered clock pulses (first, third, etc.) will provide a count to the counter, and that even numbered pulses will not. This gives a uniform count, and allows a single pulse to indicate that the circuit is measuring a sufficient value to allow a clock pulse to pass through the master gate.

The divide-by-five circuit has three multivibrators, with feedback from the third to the first two. The first three counts are normal (001, 010, 011). The fourth count raises the third multi to a 1, and the feedback loop prevents the other multis from resetting; thus the fourth count is 111. The fifth count resets the three multis to zero, providing an output signal from inverter Q44. The reset pulse resets the multis to zero to assure the same starting point for counts. Notice that in the AVERAGE OF TEN SWEEPS mode there is no reset during the ten sweeps, thus, the buffer counters can retain a remainder count between sweeps and provides a significant figure in the display.

9. COUNTER

There are four counters, for each power of ten displayed by the 6R1A. The counters themselves are four Eccles-Jordan multivibrators with feedback, the operation of which is described in the discussion of the divide-by-ten board. In addition, ten "nixie" light drivers are provided, one for each digit in the nixie (0 through 9). The outputs from the binary counter are connected to the digit driver transistors (Q100 through Q109) so that only one of these transistors will be forward biased on any of the ten counts.

The nixie tubes are neon bulbs with a common electrode formed into a shield on the tube sides and a screen in the front. This is the positive electrode, and does not glow. The ten numbers are separate negative electrodes inside the tube, with insulated pigtails connecting them. Thus only the number will glow. The screen and shield form a relatively even potential so that the numbers will glow evenly. The numbers are arranged in the tube so that they will block off a minimum area of each other. A nixie will light up several numbers if they are grounded, and a proper display depends on only one number being grounded at a time.

The binary to decimal conversion may take some study to understand. First, here are the states of the four binaries in each of the ten counts. We will reverse the notation, with the zero and one binary being at the left of the notation. Figure 3-9 and 3-10 may aid in explaining the binary states. This is also covered in the 6R1A manual.

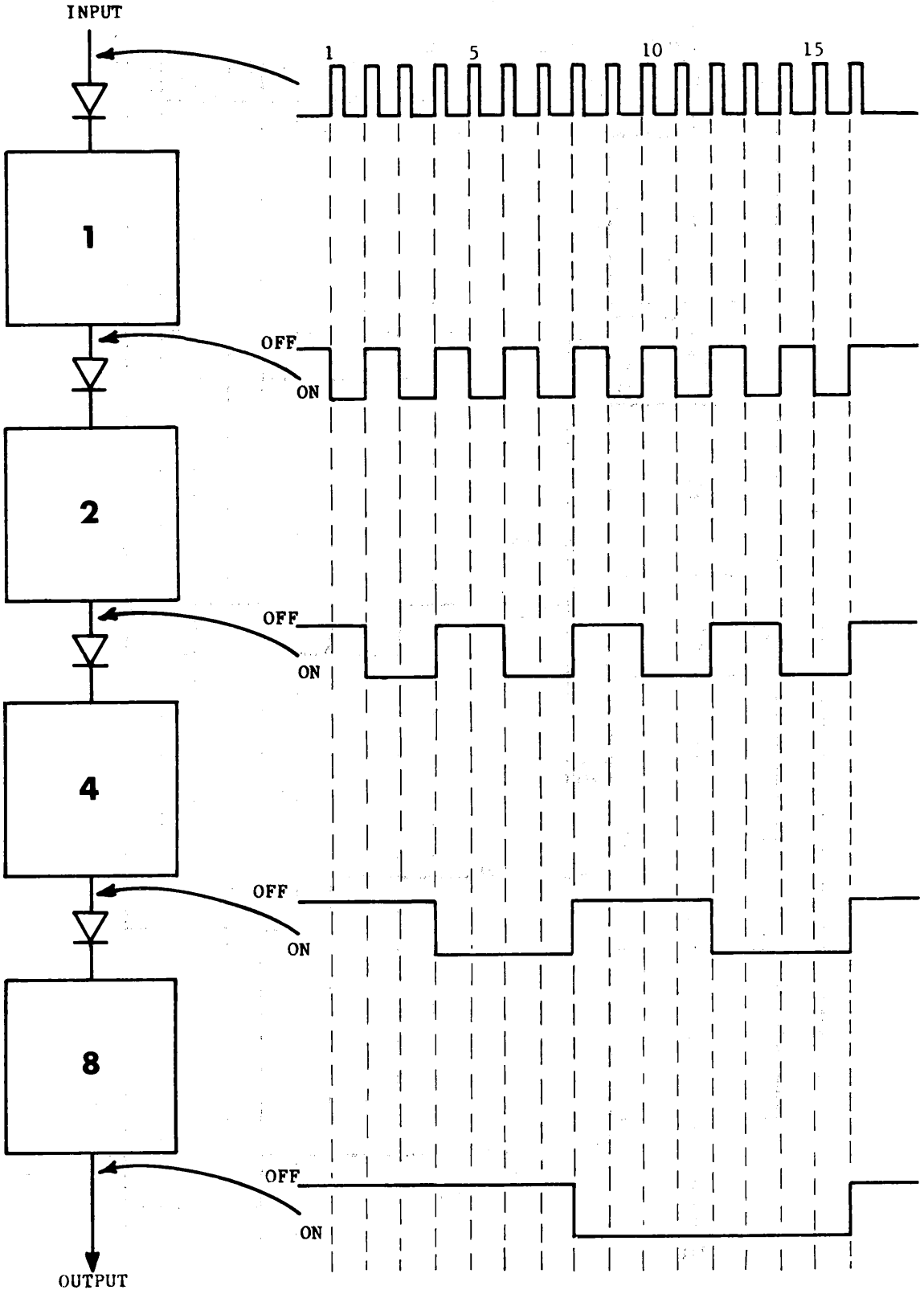


Figure 3-9

WAVEFORMS ILLUSTRATING OPERATION OF SCALE-OF-16 BINARY COUNTER

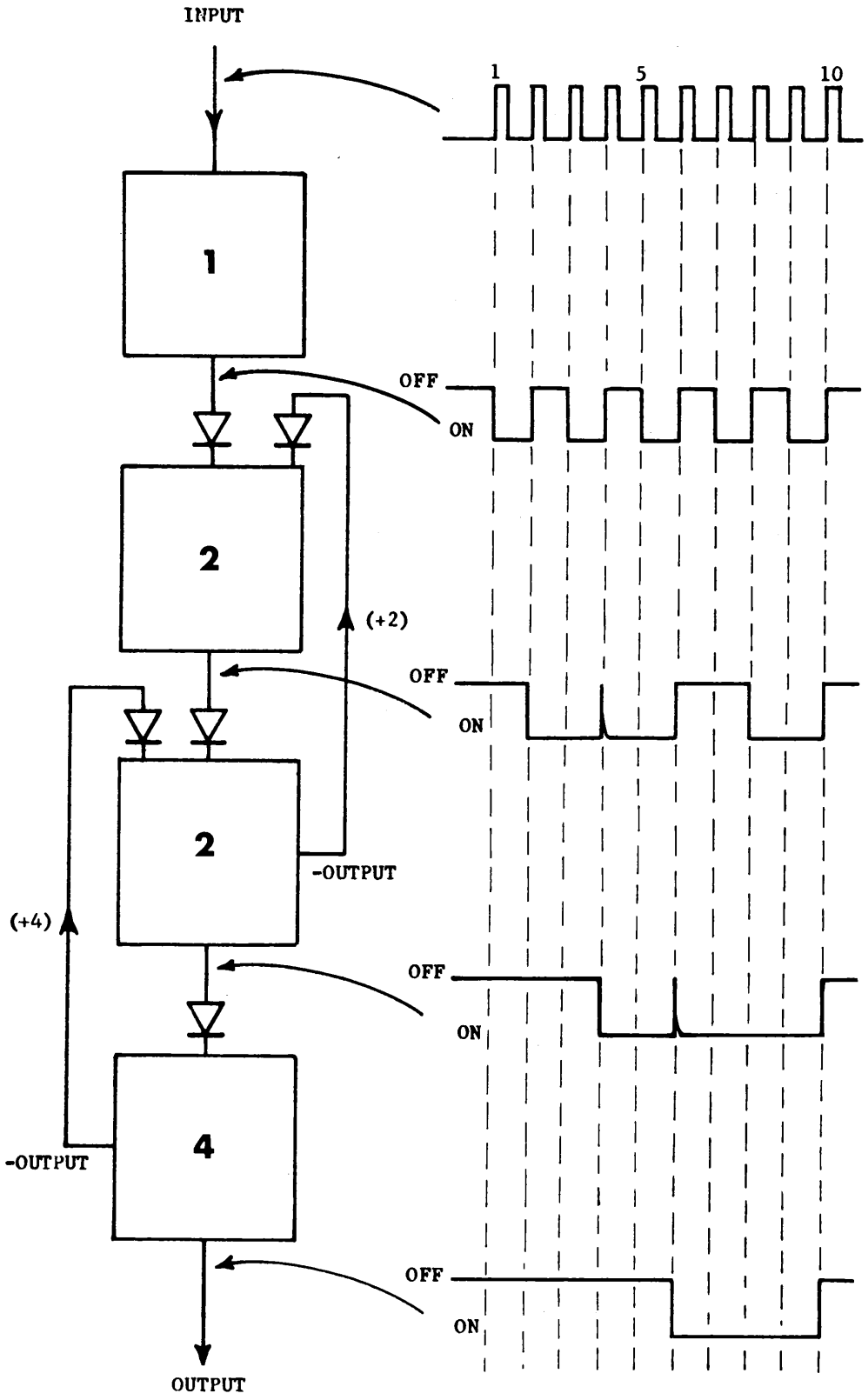


Figure 3-10

WAVEFORMS ILLUSTRATING OPERATION OF A SCALE-OF-10 PERMUTATED SCALE-OF-16 BINARY COUNTER.

Decimal	Binary
0	0000
1	1000
2	0100
3	1100
4	0110 (feedback prevents 0010)
5	1110
6	0011 (feedback prevents 0001)
7	1011
8	0111
9	1111
0 (again)	0000

The transistors are divided into pairs. The even numbered transistors display even numbers (Q100 a zero, Q102 a 2, etc), and the odd numbered transistors express odds. Notice that the odd numbers all have the first binary in 1, and the evens in 0. The first binary controls the emitter voltage on the display transistors; when Q5 is off, the first binary is in the 0 state, and all the even numbered transistor emitters at about 1/2 volt. Q15 is on, and all the odds emitters are at about 1-1/2 volts, preventing these transistors from being on.

The four multis can be called a, b, c and d, referring to Q5-Q15, Q25-Q35, Q45-Q55, and Q65-Q75. The multis can be in a 1 or a 0 state; we shall define the 0 state as the right transistor on (conducting) and the left transistor off.

Each odd-even pair of digit drivers receives a signal from two multi transistors, through separate 4.3K resistors. The transistor collectors whose signal these resistors are connected to must both be conducting for sufficient current to be drawn through the resistors to forward bias a transistor of the pair. Of course, only the transistor whose emitter is connected to the "on" transistor in multi a will conduct.

Multi a does not provide current for the transistor bases, but controls the emitter voltage instead. The combinations used for each pair of digit drives is as follows:

Q100, Q101: b0 d0
Q102, Q103: b1 c0
Q104, Q105: c1 d0
Q106, Q107: b0 d1
Q108, Q107: b1 d1

A study of the multi states during the count will show that the conditions selected exist only for the pair of numbers to be displayed, and that multi a can then select the transistor of the pair to be used in making the display.

A staircase signal is provided for use by the limit circuit. Currents through R3, R23, R43, and R63 add together so that the output will rise from ground in ten 1.67 volt steps as the count progresses.

10. ANALOG DISPLAY

The analog display circuit provides intensification of the CRT presentation in three instances.

1. During the period the memories are making a measurement. (zone gates).
2. In time measurements, the portion of the signal that is being measured.
3. The "dead" zone before the + gate is on.

The 0 and 100% memory and dead zones may be switched off, and the start-to-stop zone may be switched off. The "dead" zone warns against attempting to make measurements in that region.

Intensification is obtained by grounding the base of either Q53 or Q83. This forward biases inverter Q94, raising its collector. This signal is sent to the 567 main frame to intensify the display. The 0 and 100% and dead zones ground the base of Q53, and the start-to-stop zone grounds the base of Q83. Switching the intensification off is obtained by holding the base of either transistor at +20 volts through the controlling switch and a diode (D52 holds Q53 off and D82 holds Q83 off when the switches are OFF).

The 0 and 100% zones for each channel are mixed on the memory boards, with the output being near 20 volts except when the zone measurements are being made, when the output is grounded. A signal from the vertical plug-in is used to determine which channel is being displayed; when alternate-chopped display is presented, the signal moves back and forth to control which trace is to be intensified. The A memory zones and the - chop gate are fed to the bases of Q13 and Q3 respectively, both bases must be grounded for intensification to take place. The - chop gate and + chop gate are obtained by an emitter coupled amplifier on the 0% board. The - chop gate is grounded when channel A is being displayed, and the + chop gate is grounded when channel B is being displayed. The B memory zones and + chop gate are similarly fed to the bases of Q33

and Q23, and require that both be grounded to obtain intensification. D32 and D12 isolate the non-intensified channel from the intensified channel, allowing intensification when only one circuit calls for it.

The + gate signal is fed, independently, to the base of Q43, and calls for intensification when the + gate is at ground. This brightens the display for the first 7% of the trace.

The start-to-stop intensification circuit operates somewhat differently. Blocking diodes D63 and D73 allow the Q63 and Q73 circuits to inhibit intensification when the diodes are forward biased. A third blocking diode is located in the input to this circuit, but placed on the master gate board (D143). Start-to-stop intensification can occur only when all three diodes are back biased.

The + and - chop gates are fed to the bases of Q73 and Q63, respectively. When the - chop gate is grounded, the + chop gate is near +20, and channel A is being displayed (by the vertical plug-in). This holds the emitter of Q63 at ground, back biasing D63. If a channel A measurement is being made, the START and STOP TIMING SWITCHES ground pin 5 of the connector, forward biasing D72. This holds D73 back biased. While the measurement is being made, D143 is also back biased by the master gate, and the base of Q83 becomes grounded through R74. This allows intensification. When channel B is displayed, under the same conditions, Q63 is back biased, and current through R63 can forward bias D63 and inhibit intensification. When a channel B measurement is selected, the opposite is true, with pin 10 of the connector grounded to prevent inhibition through Q63, and Q73 being forward biased to hold D73 back biased.

When a voltage measurement is made, pin 1 of the connector is raised to +20 volts by contacts on the MODE switch. This inhibits

start-to-stop intensification, which is not needed since voltage measurements are keyed to the voltmeter ramp rather than the vertical signal.

11. UPPER LIMIT NO-GO

The upper limit no-go compares each significant figure's staircase voltage with a staircase voltage generated by a voltage divider output selected by the front panel switches. The no-go provides a -12.2 volt drive signal when the number displayed is higher than the limit number selected. The mid-range includes the number equal to the display or lower. A lower limit no-go also is provided, as a separate circuit.

There are three cases where no-go must be indicated: Assume a setting of 1357 on the switches.

1. The case where all digits are above the setting, such as 3699.

2. The case where most significant digits are above the setting, and others equal or below, such as 3357.

3. The case where the most significant digits are equal to the setting, and a less significant digit is above the setting, such as 1378. Conversely, there must be no over-limit signal in such cases as:
   a. Digits equal to the setting, such as 1357.
   b. Less significant digits only over the setting, such as 0089.

Because the transfer from 9 to 10 (9 to 0 on one counter) represents a shift to a more significant digit of the count in the counter, the zero is the lowest number, with the staircase rising to the 9.

Figure 3-11 shows a block diagram of the thousands section of the upper limit no-go. There are two circuits. One is the thousands comparator, Q124 and Q134. The other is a lockout circuit, Q104 and Q114, that prevents over-limit indication when the 1000's

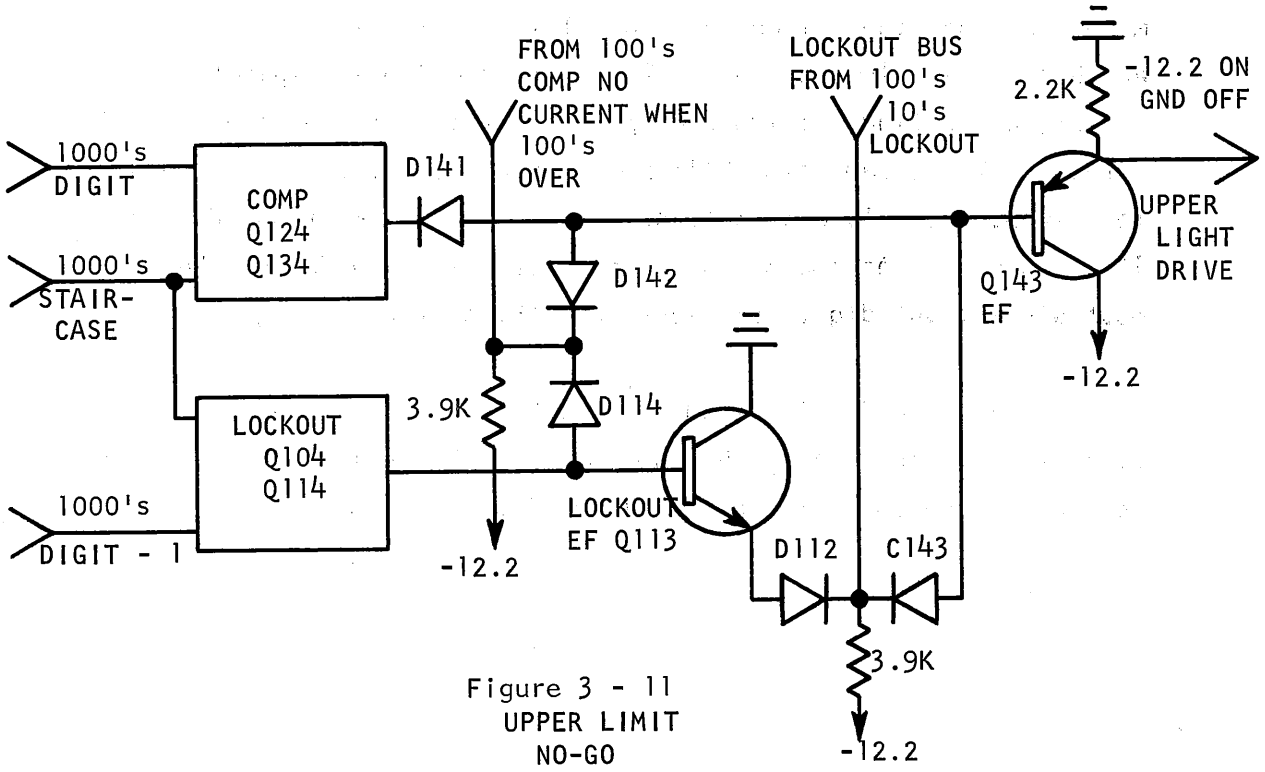


Figure 3 - 11
UPPER LIMIT
NO-GO

digit is under limit. If the less significant figures are over limit, such as the 0089 example display and 1357 set in the switches, the lockout prevents an over-limit indication.

The voltage fed to each of the three lockouts (no units lockout required) from the switches is about 2/3 volt more than the corresponding voltage from the staircase. The comparators receive the signal from the next lower tap on the divider, giving them about one volt less from the switches than the corresponding staircase output. When the 1000's measurement is less than or equal to the switch setting, Q134 will remain forward biased, holding D141 back biased. When the 1000's

measurement becomes more than the switch setting, Q134 will cut off, allowing current through R134 to flow through R141 into the base circuit of Q143.

To operate the lockout, the thousands digit must be one or more less than the switch setting. This keeps Q114 forward biased, and D114 will allow current to flow into the 100's comparator output, preventing the 100's comparator from operating the over-limit output. At the same time Q113 provides current through D112 and D113 to prevent the 10's and units comparators from operating the over-limit output. The lockout prevents over-limit indication when the most significant digits are less than the switch settings.

The 100's and 10's circuits have both comparator and lockout circuits that operate in the same manner. The units circuit has no lockout, since there is no less significant figure.

12. LOWER LIMIT NO-GO

This circuit is similar to the upper limit no-go except that the inputs to the comparators and lockouts are reversed. This allows the most significant figure to prevent the less significant figures from showing under-limit if the more significant figures are within range.

13. LIMIT LIGHT DRIVER

The limit light driver has three driver transistors that drive the number 47 limit lamps. Three signals are fed to the circuit.

1. Print Command: Provides collector current for the "or" circuit that drives the limit light drivers, when the print command is at +20 volts.

2. Upper Limit No-Go: When at -12.2V, forward biases emitter follower Q23. This forward biases upper limit light driver Q33 and raises voltage across R60 to forward bias Q64. Q64 collector rises, holding mid-zone driver Q63 off.

3. Lower Limit No-Go: When at -12.2 volts, forward biases emitter follower Q43. This forward biases lower limit light driver Q53 and raises voltage across R60 to forward bias Q64, holding mid-zone lamp off.

When both upper and lower limit no-go inputs are at ground, Q23 and Q43 are back biased. No voltage is developed across R60, and Q64 remains back biased. In this case, current through Q13 (when print command is at +20) forward biases Q63, lighting the mid-zone lamp.

SECTION 4

LOGIC LEVELS IN 6R1A

1. The following list describes logic levels found in the 6R1A. The signals described control the functioning of parts of the 6R1A, and a knowledge of their nature can help in understanding the operation.

2. + Gate. The + Gate is formed on the 0% zone board. The inputs are the sweep gate and sweep sawtooth signal from the horizontal amplifier. The + Gate rises from ground to +20 volts when the sweep gate is calling for sweep and the sweep has passed its first 7%. The + Gate continues at +20 volts until the end of the sweep, when it returns to ground. The + Gate controls the following:

a. Memories: +20 level must be present to allow 0% and 100% zones to form. When + Gate is at ground and print command at +20 volts, peak memory capacitors are discharged.

b. Voltmeter: When + Gate is at +20 and print command is at ground, voltmeter ramp rise starts as + Gate rises to +20.

c. Comparators: + Gate rise to +20 is used to set the first second slope multi in desired state (selected by FIRST-SECOND switches) for comparison.

d. Master Gate: Rise of + Gate to +20 sets start multi off, stop multi on, normally. If stop multi was already on, + Gate rise turns it off, with no measurement until following sweep (preventing lockup with no end-of-measurement). Return of + Gate to ground operates divide-by-two multi to reset display circuit to count mode at end of a sweep following end of display period.

e. Analog Display: First 7% of sweep is intensified by + Gate being in ground, showing the duration of the "dead zone" in which measurement cannot be made. Dead zone allows sweep to start before measurements are made.

3. Print Command: The print command signal is formed on the master gate board. The level is ground during measurement and +20 during display. The print command rises to +20 volts when the end-of-measurement signal from the stop multi or divide-by-ten is received. Reset to ground occurs after the adjustable display period, at the end of the sweep that turns Q25 in the divide-by-two multi on, resetting the display circuit. There is also a - print command signal that is at +20 during measurement dropping to ground during display, provided by an inverter driven by the + print command signal. The - print command signal can be made available externally, and is used to set the divide-by-two multi during measurement, its only internal use. The print command signal may be also made available for external use. Internal use of the print command is:

a. Memories: When in peak memory mode, with the print command at +20 and the + Gate at ground, the memory capacitors are discharged.

b. Voltmeter: The print command, when at +20, prevents the voltmeter ramp from operating.

c. Limit light driver: When at +20, the print command allows the limit light driver to light the appropriate limit light.

d. Clock Gate: The print command, when at +20 volts, prevents the clock signal from passing through to the counter.

4. Reset pulse: The reset pulse is formed by the display circuit at the same time the print command returns from +20 to ground. The following are reset:

a. Divide-by-two or five scaling multis.

b. Counters

c. Divide-by-ten

d. Stop Multi (set to on)

5. Stop pulse and end of measurement pulse: The stop multi provides a pulse when it trips to stop the clock pulses at the end of a count. This pulse is fed to the RESOLUTION switch. In ONE SWEEP, the stop

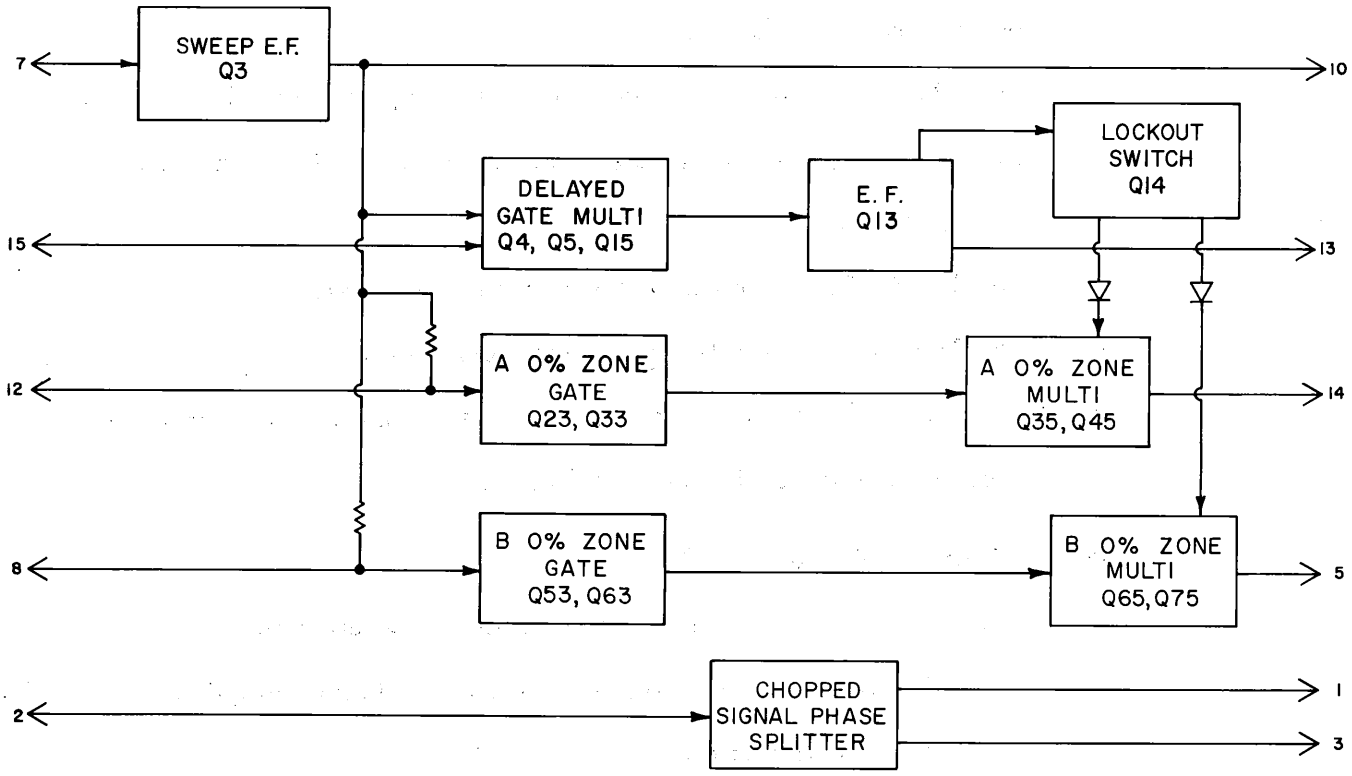
pulse goes directly to the display circuit to switch the system to display. In AVERAGE OF TEN SWEEPS, the stop pulse goes to the divide-by-ten multi. At the tenth stop pulse, the multi provides the end of measurement signal to the display circuit.

TYPE 6R1A

V. 0% ZONE CARD

A. The 0% zone circuits generate three sets of pulses related to the Horizontal Sweep ramp.

1. The delayed plus gate pulse.
2. The A 0% zone memory gate pulse (time variable).
3. The B 0% zone memory gate pulse (time variable).
4. Also a phase splitter converts the A chopped trace from the vertical plug-in to a push-pull signal.



TYPE 6RIA 0% ZONE
BLOCK DIAGRAM

B-6RIA-0001
5-21-'64 dl

B. Inputs

1. 50v positive going sweep ramp or staircase from the horizontal plug-in (pin 7).
2. A 3v sweep gate from the horizontal plug-in (pin 15).
3. Variable DC offset voltage (0 to -100v) from the A and B 0% zone position controls (pins 12 and 8)
4. A 2.8v peak-to-peak Channel A chopped trace square wave from the vertical plug-in (pin 2).

C. Outputs

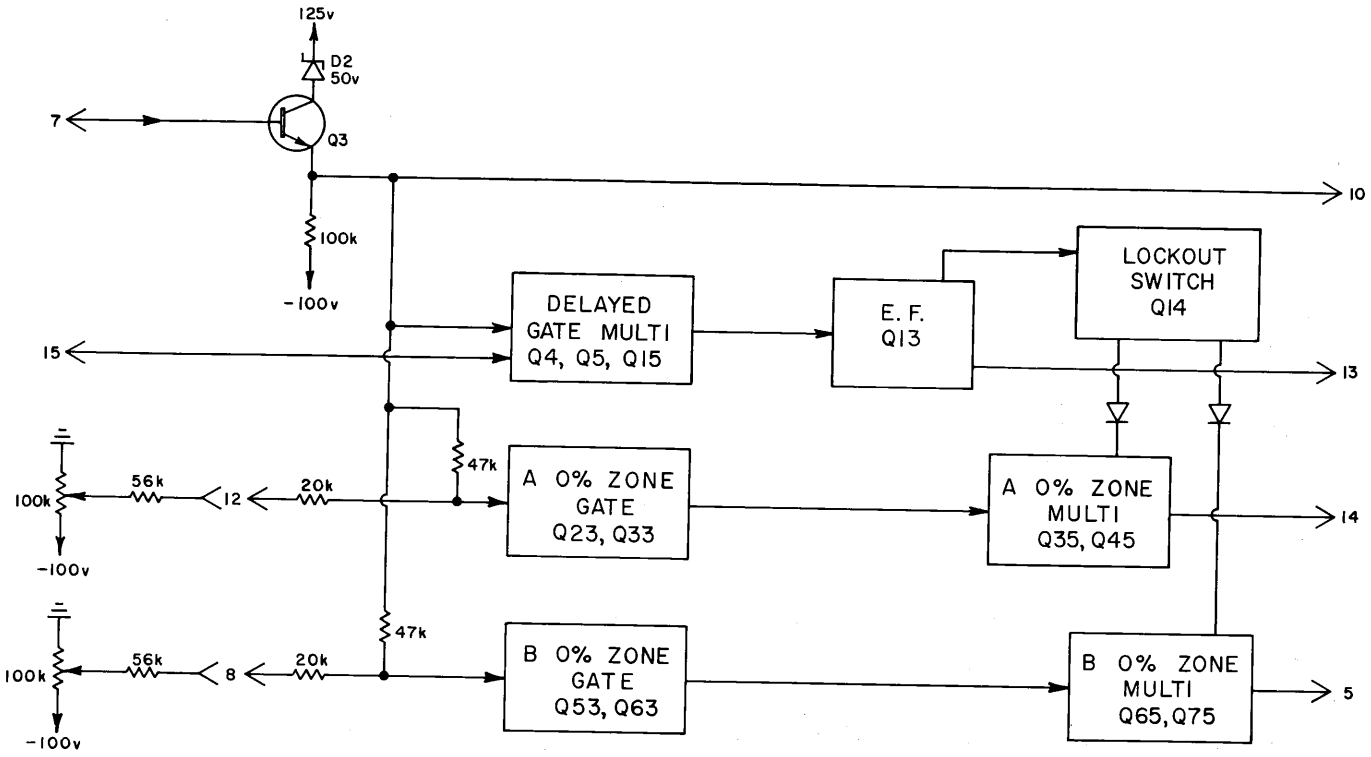
1. A 50v positive going sweep ramp (or staircase) to the timing switches and the memories (pin 10).
2. The 18v delayed gate waveform that is used by the memories, the voltmeter, the master gate, and signal comparators and analog display (pin 13).
3. The 17v A 0% zone pulse to the A memory (pin 14).
4. The 17v B 0% zone pulse to the B memory (pin 5).
5. The push-pull chopped trace square wave, about 40v peak-to-peak used in the analog display (pins 1 and 3).

D. Preamp Emitter Follower -- Q3

1. Q3 provides a low impedance source for the sweep ramp to:
   a. The timing switches and the memories (through pin 10).
   b. The delayed gate multi.
   c. The A and B 0% zone gating transistors.
2. Q3 is a 151-096 selected 2N1938 silicon NPN transistor.
3. D2 is a 152-096, a M50Z10, 3/4W, 50v 10% zener diode.

4. D2 provides a 50v DC offset from the 125 regulated supply, placing Q3 collector at 75v.

   a. 75v is the optimum collector supply for a 50v emitter swing.



TYPE 6RIA 0% ZONE
SWEEP E. F.

B-6RIA-0002
5-22-'64 dl

5. Q3 is long-tailed to -100v.

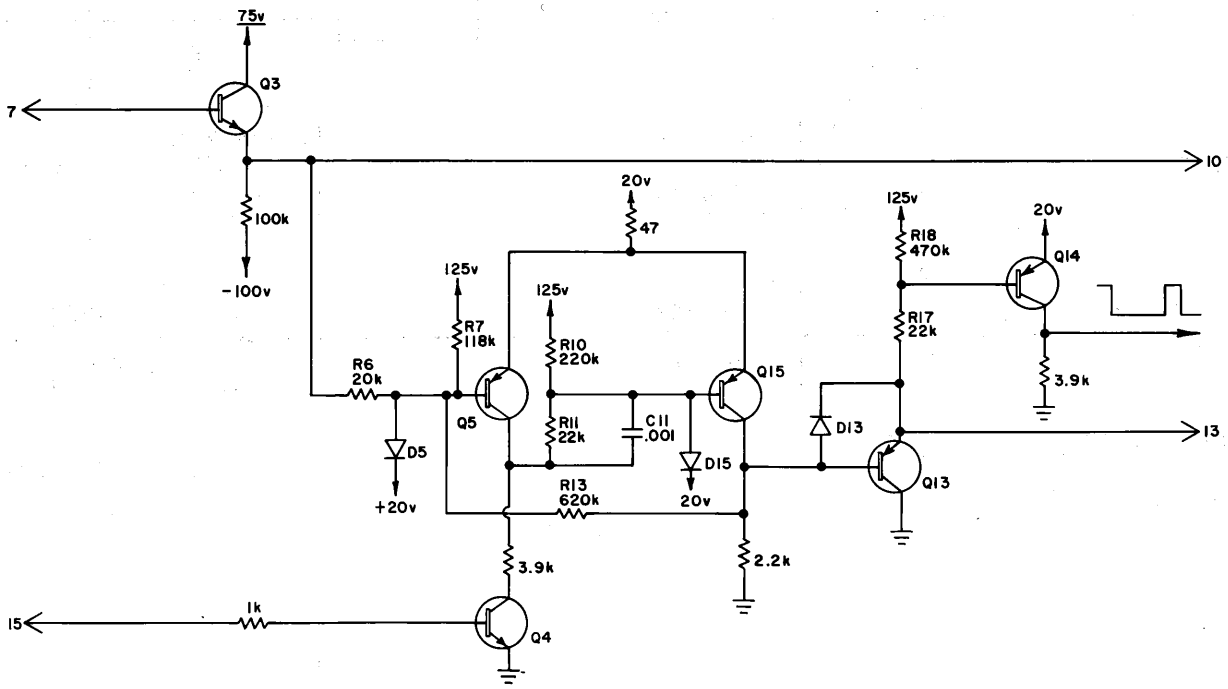
   a. The 0% zone position controls form part of the emitter return.

E. Delayed Gate, Q4, Q5, Q13, Q14, Q15

1. The Delay Gate circuit provides a gate pulse, delayed by about 5% of sweep time (about 5 mm of graticule space).

   a. The delay allows the sweep to get started and the display unblanked before the measurements start -- the 6R1A cannot start measuring information that is invisible to the operator.

   b. The delayed period is called the Dead Zone.



TYPE 6RIA 0% ZONE
DELAYED GATE

B-6RIA-0003
5-25-'64 dl

2. Five transistors and three diodes are used in the circuit.

   a. Q4 is a 151-103 selected 2N2219 silicon NPN transistor.

   b. Q5, Q13, Q14 and Q15 are 151-054 selected Motorola 5M474 or Philco 2N1754 germanium PNP transistors.

   c. D5, D13 and D15 are 152-075 selected GD238 germanium diodes.

3. Q5 and Q15 comprise a schmitt multi.

   a. Q4, Q13 and Q14 are switches.

4. Conditions prior to sweep:

   a. Q4 is cut off.

      (1) Q4 base sets at -1.5v.

      (2) The collector raises toward 125v to be clamped at 20.3v by D15.

   b. Q15 is cut off.

      (1) The emitter sets at 20v and the base at 20.3v.

      (2) Q15 collector is at ground.

   c. Q5 is saturated.

      (1) Base-emitter current will pull the base up to 19v (the divider R6, R7 would set the base at 17.7v).

      (2) The collector-base junction is forward biased, but current limited by R11.

      (3) D15 clamps the top of R11 at 20.3v so a maximum of 60 μa of collector current can flow through R10 and R11.

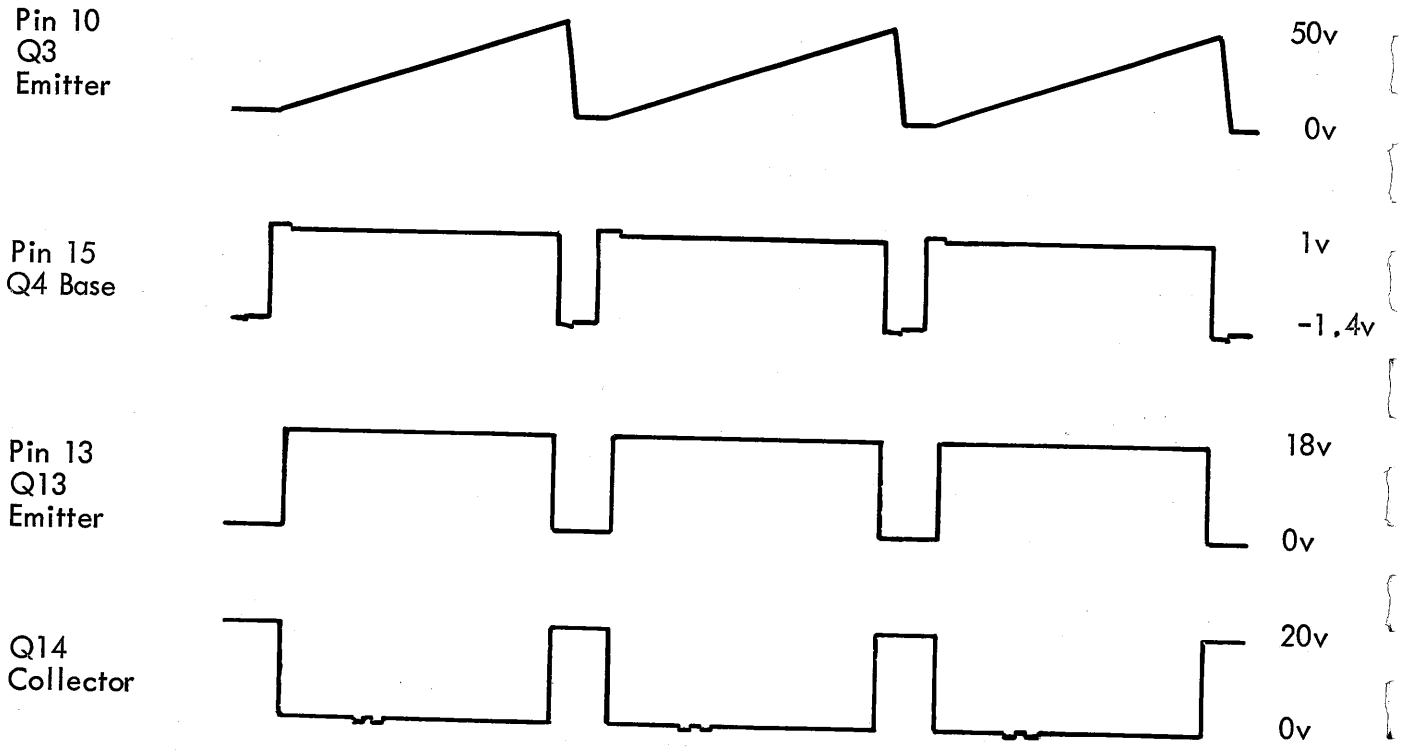
   d. Q13 is saturated.

      (1) All elements are at ground.

e. Q14 is saturated.

(1) All elements are set by the emitter at 20v (the divider R17, R18 would set the base at 5.5v but base-emitter current pulls it up to 20v).

5. At the start of sweep the Sweep Gate lifts Q4 base, forward biasing the transistor to conduction.



a. The collector pulls down to ground as the transistor saturates.

b. Q5 now has a normal collector supply.

c. Q4 collector supplies Q5 collector current.

(1) Q5 collector holds the top of R5 up while Q4 collector pulls the bottom of R5 down.

d. Q15 remains cut off with its base at 20v.

6. When the sweep ramp reaches about 2v, Q5 base is raised to 20v cutting off the transistor (the transistor is actually cut off through multi action).
   a. D5 limits further base rise to 20.3v protecting Q5 from base-emitter breakdown.
   b. As current in Q5 is cut off, its collector drops.
   c. Q4 collector is now supplied through R10, R11 to 125v.
   d. Q15 base is pulled down (R10, R11 would pull the base to 11.3v).
   e. D15 cuts off.
   f. C11 is a speed-up cap.
7. As Q15 base drops, the transistor turns on as the multi flips.
   a. Q15 collector pulls up to about 20v.
   b. Positive feedback through R13 aids in the multi action.
8. The positive step from Q15 collector couples through D13 to form the output delayed gate at pin 13.
   a. Q13 emitter follows its base to 20v.
   b. D13 overcomes the inherent slow risetime of an EF when the base is pulled up by a large step.
   c. Current through D13 can charge the relatively high capacitance load through pin 13 and provides a fast rise gate.
9. The positive step turns off Q14.
   a. Its collector drops to ground.
10. The waveform at Q14 collector is a 20v negative going delayed gate.
   a. The gate is used to prevent generation of the A and B 0% zone pulses during the hold-off period and the first 5% of the sweep.

11. At the end of sweep retrace, Q4 and Q15 turn off and Q5 base drops Q5 into conduction.

    a. The multi flips.

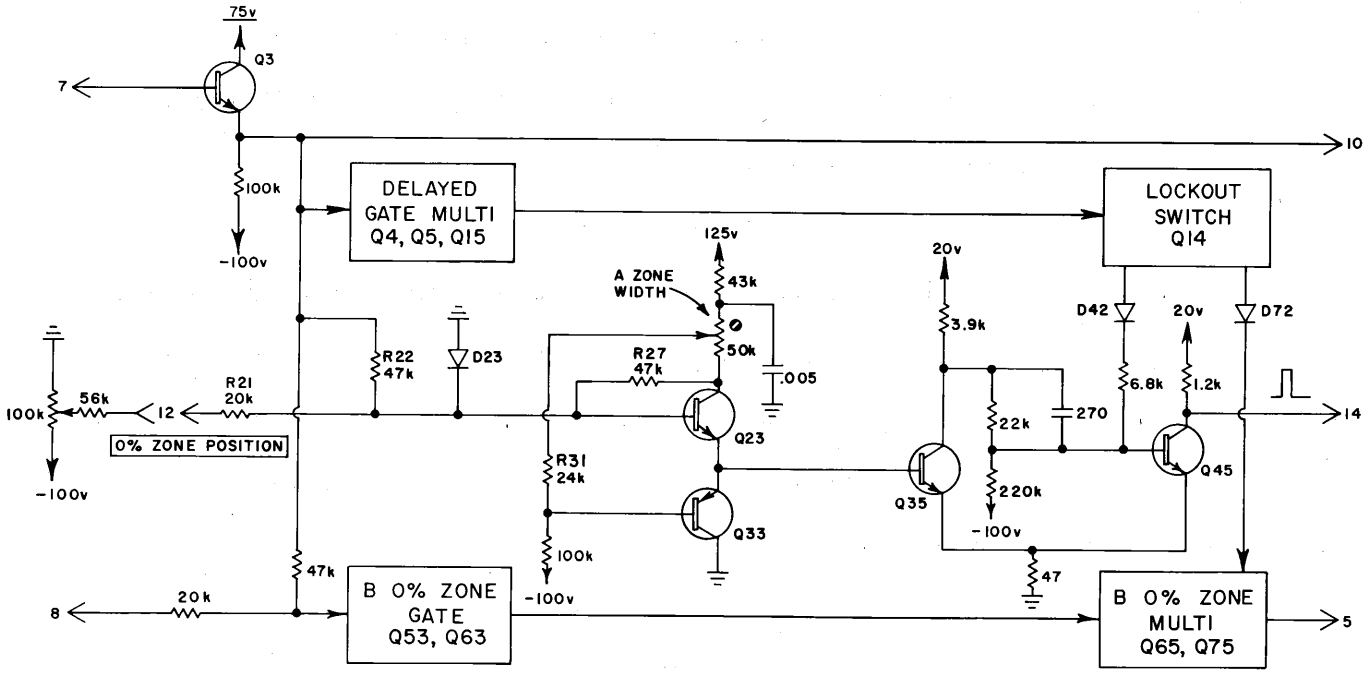
    b. All circuits reset to the quiescent state.

F. A 0% Zone Gate

1. The A 0% zone gate provides a 17v positive going pulse of variable width and variable position relative to sweep.

    a. The pulse is fed to the A Memory (via pin 14) where it gates on the memory.

    b. The pulse is also used (inverted in the memory circuit) to intensify a portion of the analog display.



TYPE 6RIA 0% ZONE
A 0% ZONE GATE

B-6RIA-0004
5-28-'64 dl

2. Four transistors and two diodes are used in the circuit.
   a. Q33 is a 151-071, TI 2N1305 germanium PNP transistor.
   b. Q23, Q35 and Q45 are 151-103 selected 2N2219 silicon NPN transistors.
   c. D23 and D42 are 152-075 germanium diodes.
3. Q23 and Q33 (a variable hysteresis schmitt multi) develop the variable width gate and Q35, Q45 (a conventioanl schmitt multi) provide consistent amplitude and risetime.
4. The 50v sweep ramp from Q3 and the 100v 0% ZONE POS information is mixed in R21, R22.
   a. The sweep ramp starts at 0v and raises to about 55v.
   b. The 0% ZONE POS is a DC voltage from -100v to ground.
5. The 0% ZONE POS control provides a DC offset voltage so that by varying the control, <u>any</u> portion of the sweep ramp can be made to pass through 2 volts at Q23 base.
   a. D23, however, keeps the base from dropping below -.3v thereby preventing base-emitter breakdown.
   b. The 2v point on the ramp will be used to start the 0% zone gate.
   c. By rotating the 0% ZONE POS control, the 0% zone gate can be made to start at any time during sweep.
   d. The 0% zone pulse is stopped at a point further along the sweep ramp at a point determined by the ZONE WIDTH control.
   e. 0% zone width can be adjusted from zero to 4 cm, then the width jumps to full screen width.
6. Q23 is an operational amplifier.
   a. R27 is R_f.

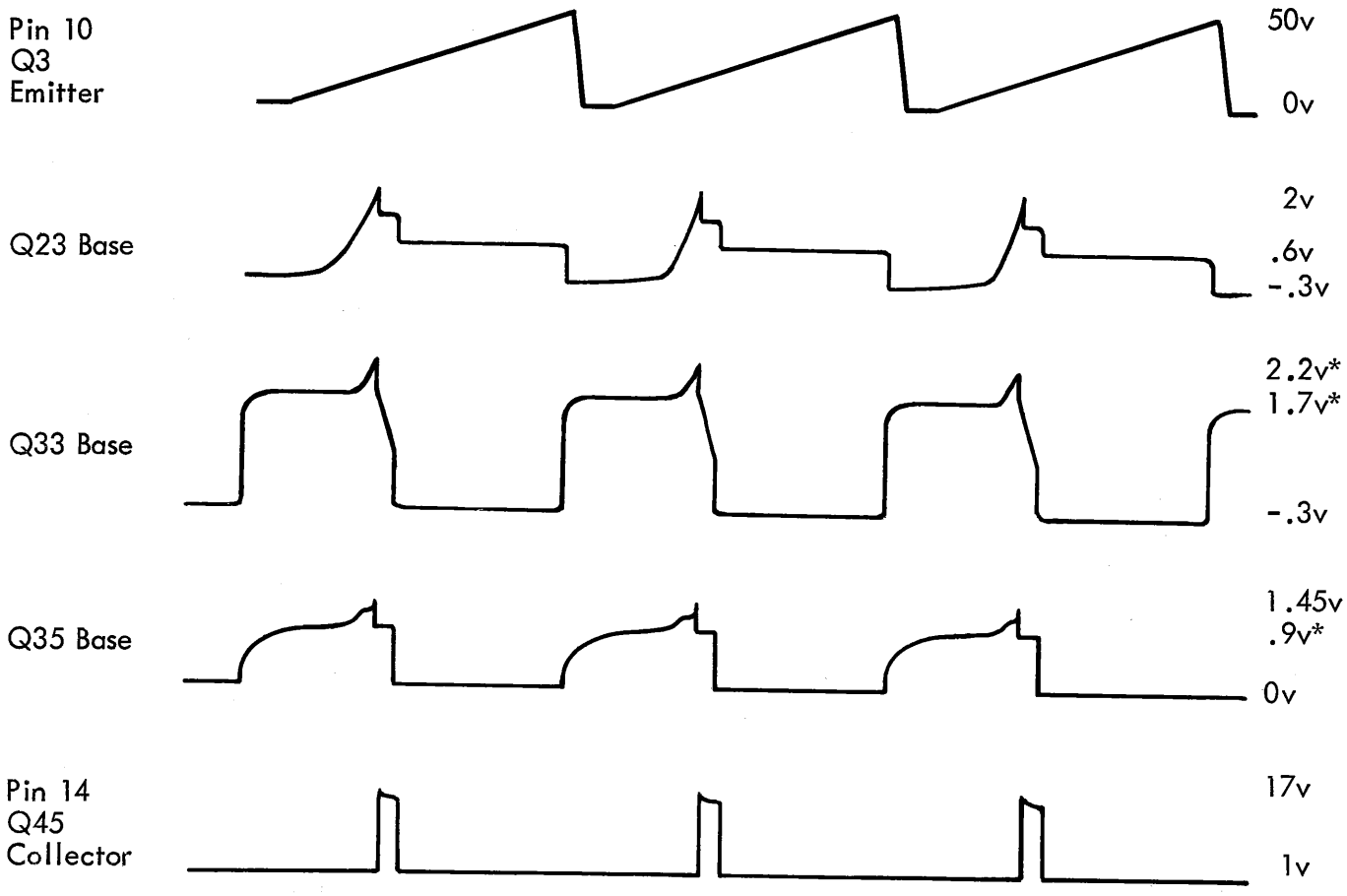
b. R22 is R_i for the sweep ramp.

c. R21 is R_i for the 100% zone positioning.

7. Prior to sweep, both Q23 and Q33 are cut off.

a. Q35 is off and Q45 is saturated, with its collector pulled down to 1v.

b. Q23 base is clamped at -.3v.



*Will vary with zone width.

8. As the sweep ramp lifts Q23 base to 2v, the transistor begins to conduct.

a. Since Q33 is cut off, Q23 emitter current must be suppled by Q35 base.

b. The base current turns on Q35.

c. The multi flips and as Q45 cuts off, it collector rises to 17v forming the start of the 0% zone pulse.

9. As Q23 conducts and its collector drops, Q33 base voltage also drops (through R31).

a. The A ZONE WIDTH sets the level to which Q33 base drops initially.

b. With a zone width of 3 mm, Q33 base will drop to about +1.7v.

c. This base potential is not low enough to forward bias the transistor.

(1) Q23, Q33 emitters are setting at about +1.2v.

(2) Q33 base must drop just below this point to conduct.

d. As the sweep ramp continues, Q23 collector will drop Q33 base into conduction.

10. When Q33 conducts (saturates) its emitter is pulled down to ground.

a. Q35 base is pulled down to ground, cutting off Q35.

b. As Q35 cuts off, the multi flips.

c. Q45 collector drops to 1v stopping the pulse.

11. The 0% zone gate pulse, therefore, is started when Q23 base reaches 2v and stopped when Q33 conducts.

a. With the width control full clockwise, the 0% zone pulse will continue for the duration of sweep.

b. In this case, the 0% zone is stopped at the end of the Delayed Gate.

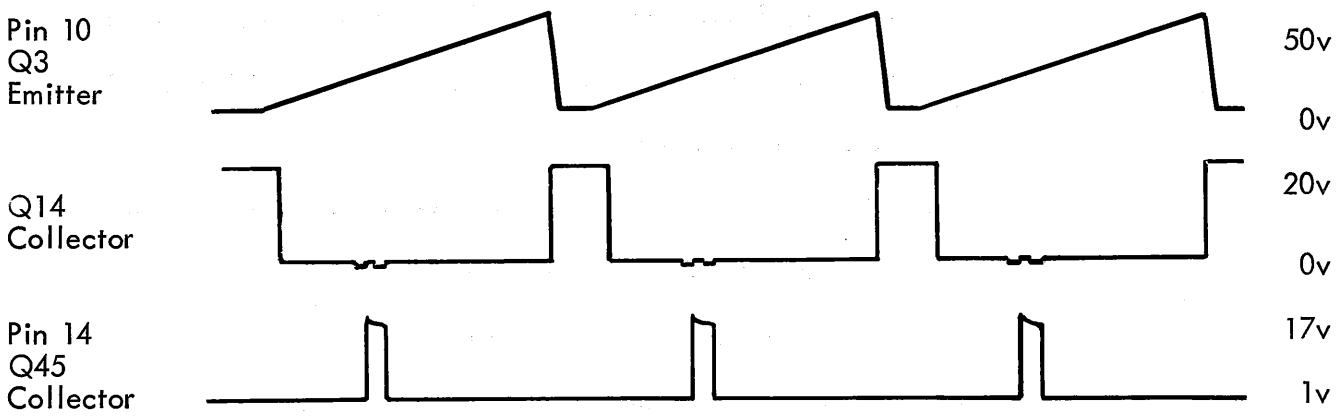
12. At the end of sweep, retrace drops Q23 base to cut off.

    a. As Q23 collector rises, Q33 base is pulled up cutting it off.

    b. With Q23, Q33 and Q35 cut off, the bus that ties the three transistors together rises slowly with Q33 base-emitter leakage current.

    c. This floating junction cannot rise above 1.7v -- Q33 base level.

13. A lockout gate from Q14 lifts D42 anode to 20v except for the duration of the Delayed Gate.



    a. The 0% zone schmitt multi cannot flip to form a 0% zone pulse during this period.

    b. Q45 is turned on; the multi cannot function.

    c. The 0% zone gate is locked out then from the end of sweep until the start of the Delay Gate.

14. At the start of the Delayed Gate, D42 anode drops to 0v.

    a. D42 cuts off.

    b. The 0% zone multi is free to generate the 0% zone pulse.

15. At tne end of the Delayed Gate (end of sweep) the 0% zone multi is again locked out.

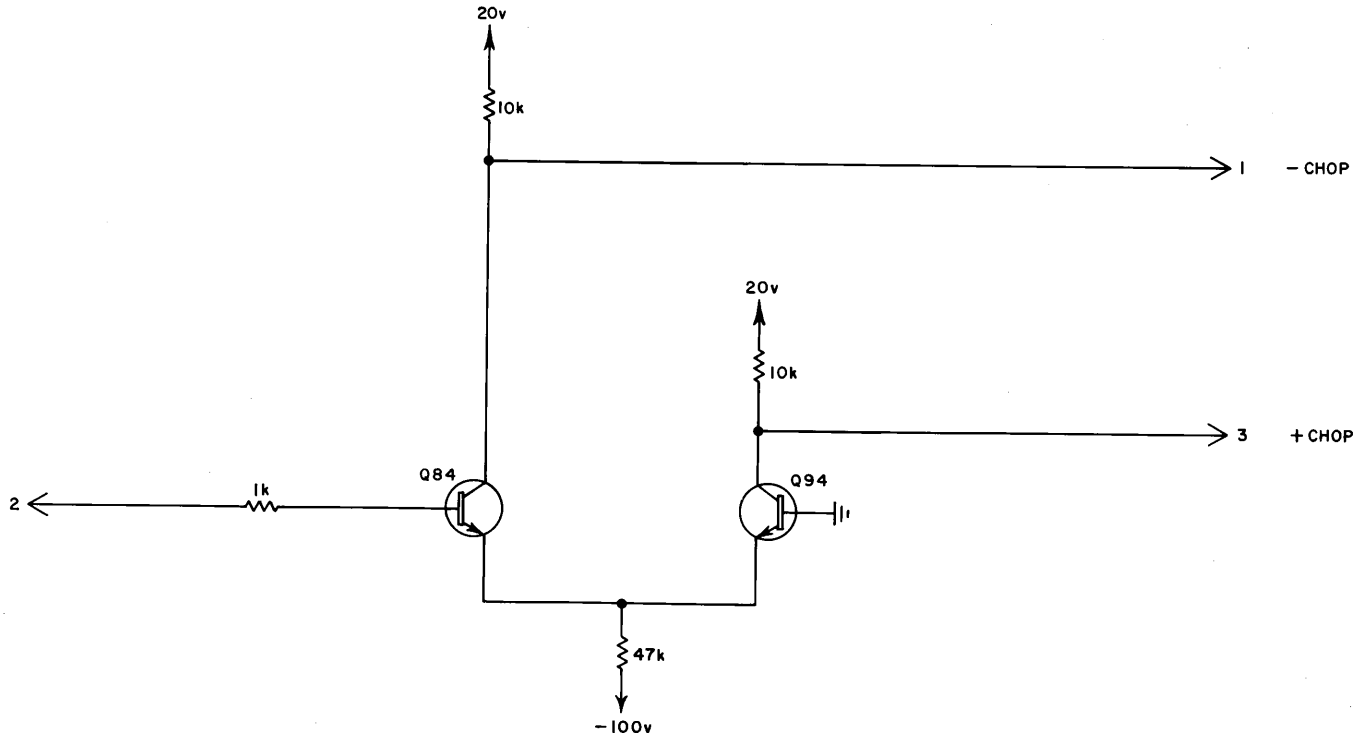
G. B 0% Zone Gate

1. The B 0% zone gate is the same as the A 0% zone gate except for component numbers.

2. The gate pulse is 17v peak-to-peak at pin 5.

H. Channel A Chopped Signal Phase Splitter

1. The chopped waveform from Channel A of the vertical plug-in appears at pin 2 as a 2v square wave (-1v to +1v).



TYPE 6RIA 0% ZONE
CHANNEL 'A' CHOP PHASE SPLITTER

B-6RIA-0005
5-27-'64 dl

2. The output at pins 1 and 3 is a 40v push pull square wave (20v each side) to be used in the analog display.
3. A transistorized paraphase inverter is used to develop the push pull signal.
   a. Q84 and Q94 are 151-103 silicon NPN transistors.
4. There is a slight difference in amplitude in the output voltages because of the inherent unbalance in a paraphase inverter.

TYPE 6R1A

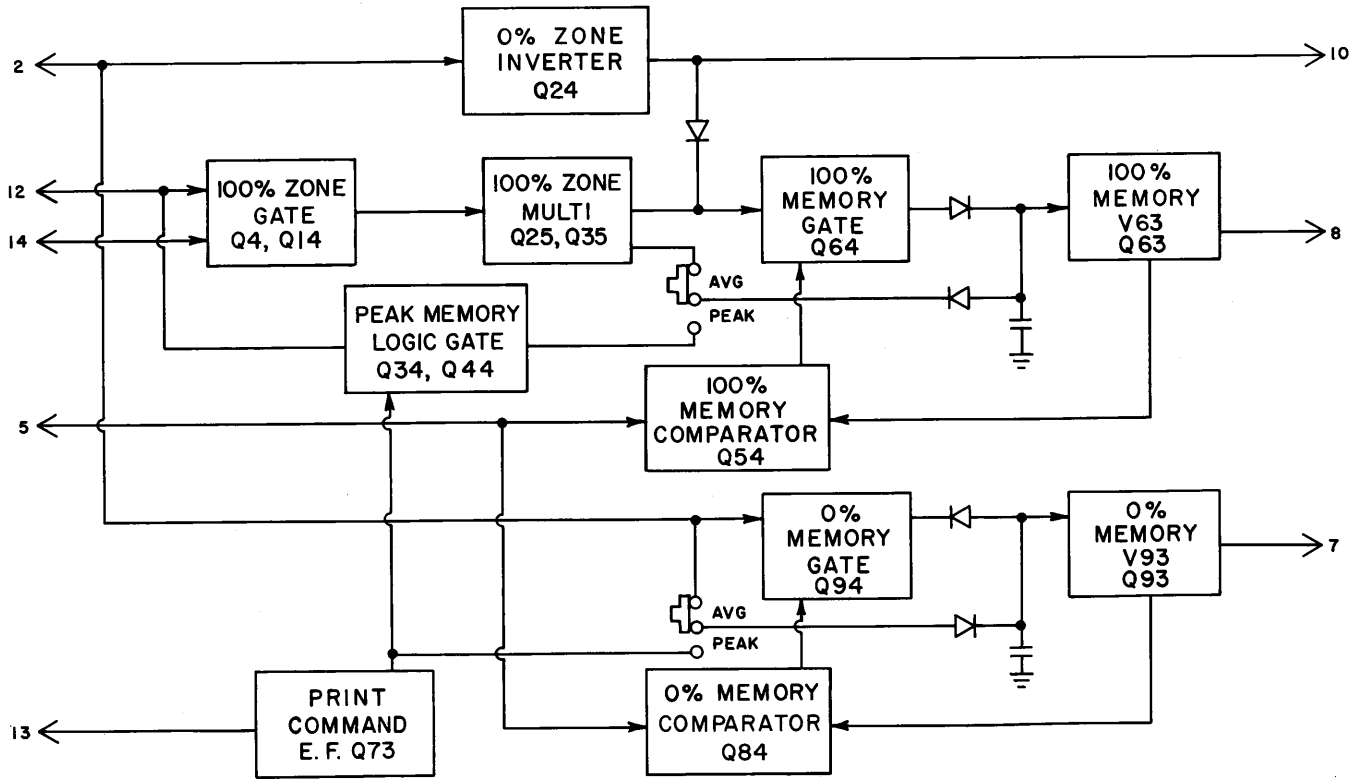
VI. 0% AND 100% MEMORIES CARD

A. Two identical and interchangeable 0% and 100% memory cards are used in each Type 6R1A; one for Channel A and one for Channel B.

B. The card contains the following circuits:

1. 0% zone inverter, Q24.
2. 100% zone memory gate, Q4, Q14, Q25, Q35.
3. 100% memory, Q64, V63, Q63, Q54.
4. 0% memory, Q94, V93, Q93, Q84.
5. Peak memory logic gate, Q34, Q44.

C. Block Diagram



TYPE 6RIA 0% AND 100% MEMORIES CARD BLOCK DIAGRAM

B-6RIA-0006
6-2-'64 dl

D. Inputs

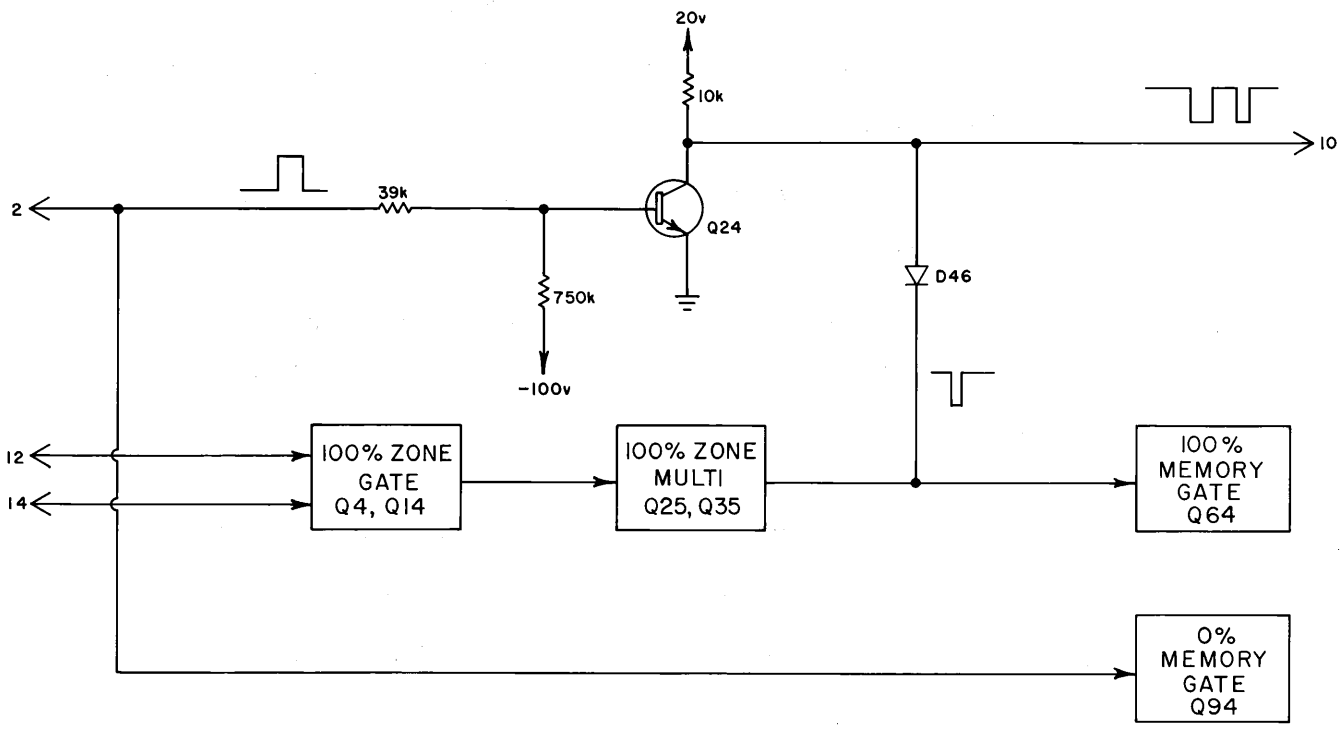
1. The 0% zone pulses from the 0% zone card on pin 2.
   a. A 17v positive going pulse from 0v to 17v.
2. The Delayed Gate from the 0% zone card on pin 12.
   a. A positive going 18v gate from 0v to 18v.
   b. The Gate is delayed about 5 mm* from the start of sweep.
3. A positive going sweep ramp on pin 14.
   a. The ramp is mixed with a -100v DC offset voltage from the 100% (ZONE) control.
4. The output from Vertical plug-in on pin 5.
   a. The A Memory Card receives the output from Multi Trace Channel A, etc.
   b. The signal has a value of 1 v/div.
   c. Center screen has a value of 10v.
5. The Print Command waveform from the Master Gate Card on pin 13.
   a. The waveform is at 2v during count state and 20v in display state.

E. Outputs

1. The composite 0% and 100% zone pulses on pin 10.
   a. The pulses are negative going 20v pulses from 20v to 0v.
   b. The pulses are used in the Analog Display.
2. The 100% Memory on pin 8.
   a. A DC voltage (AVG mode) of the same level as the Vertical input on pin 5 at the time of the 100% zone.
   b. The Memory is used in the Signal Comparators.
3. The 0% Memory on pin 7.
   a. A DC voltage (AVG mode) that represents the level of the Vertical signal on pin 5 at the time of the 0% zone.
   b. Used by the Comparators.

* See 0% Card, page 5-4.

F. 0% Zone Inverter, Q24



TYPE 6RIA MEMORIES CARD
0% ZONE INVERTER

B-6RIA-0007
6-4-'64 dl

1. The 0% zone inverter inverts the positive going 0% zone gate from the 0% zone card and mixes it with the 100% zone.
2. The input at pin 2 is the 17v (0v to 17v) 0% zone.
3. The output (pin 10) is the composite 0% and 100% zones.
   a. The waveform is composed of negative going 20v zone pulses (from 20v to 0v).
4. The inverter, Q24, is a 151-069, 2N1304 germanium NPN transistor.
5. The 0% zone waveform lifts the base into saturation.
   a. Q24 base sets quiescently at -4v.

b. Q24 collector drops to 0v, disconnecting D46 and forming the 0% portion of the output composite waveform.

6. The 100% zone multi output drops D46 cathode from 20v to 0v, forming the 100% portion of the composite signal.

a. 100% zone switching spikes appear capacitively coupled on Q24 base.

(1) Spikes swing the base negative to -8.5v and up to -1v.

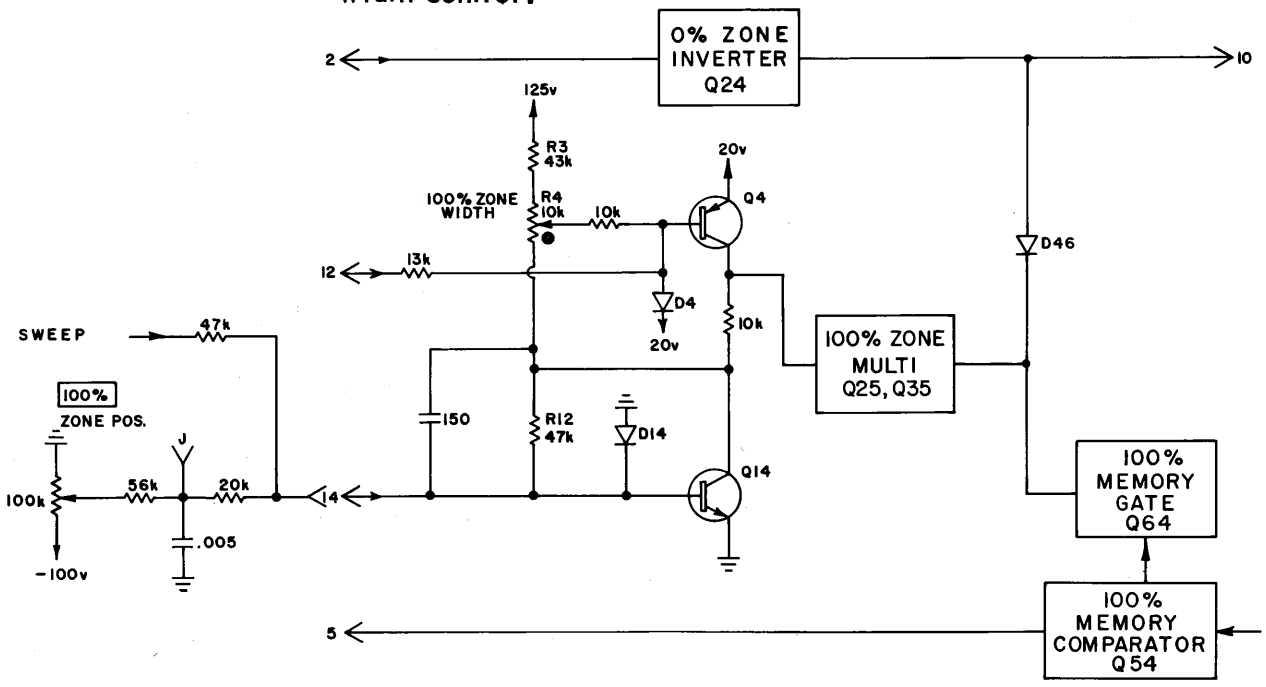
(2) The spikes are not used -- they are just aberrations.

G. 100% Zone Memory Gate, Q4, Q14, Q25, Q35

1. The circuit provides a negative going 100% zone gate for use in the analog display and to gate on the 100% memory.

a. The 100% zone gate occurs at a time after the start of sweep selected by the 100% zone position control.

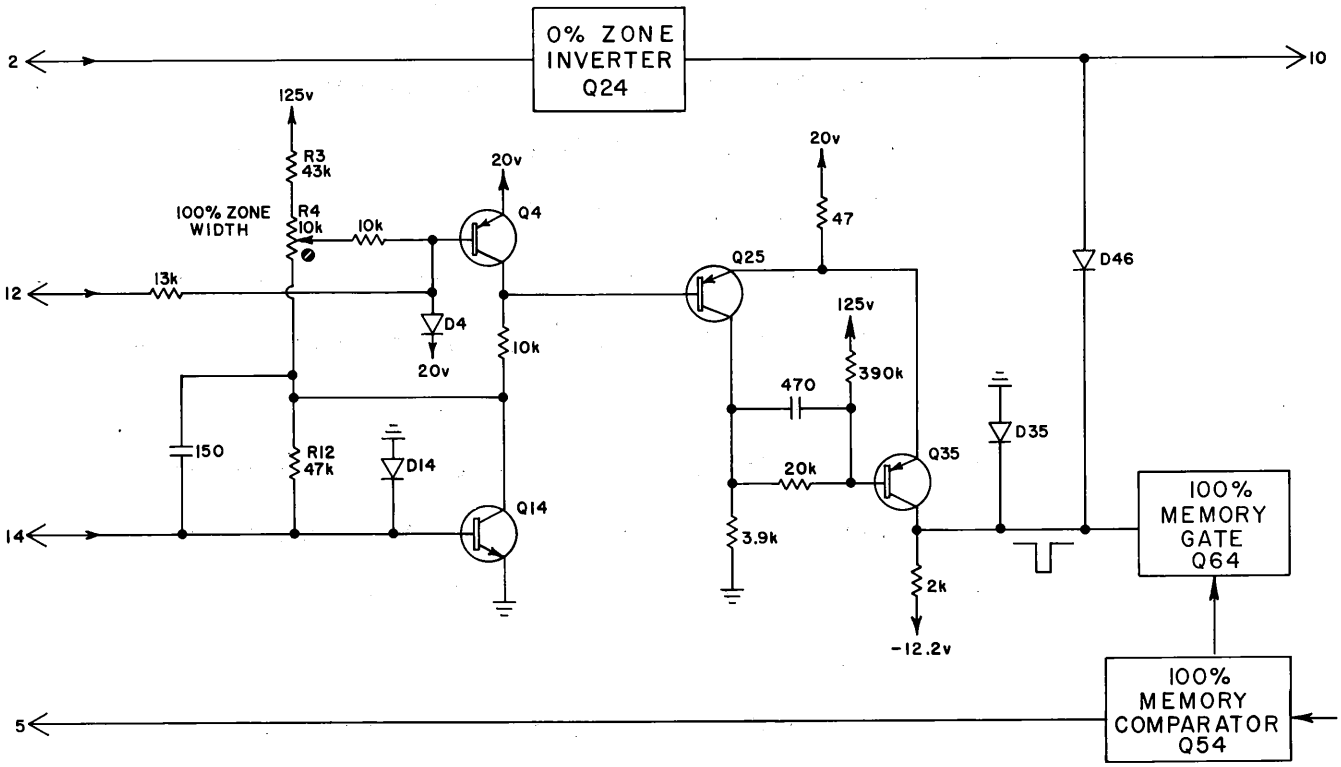
b. The 100% zone has variable width controlled by the 100% zone width control.



TYPE 6RIA 0% AND 100% MEMORIES CARD
100% ZONE GATE

B-6RIA-0008.1
10-1-'64 dl

2. The circuits that comprise the 100% memory gate:
   a. 100% zone gate, Q4, Q14.
   b. 100% zone multi, Q25, Q35.
3. The circuit uses four transistors, one nuvistor and four diodes.
   a. Q4 is a 151-087 selected TI, J3138 silicon PNP transistor (2N1131 will substitute).
   b. Q25 and Q35 are 151-054 germanium PNP transistors.
   c. Q14 is a 151-103, 2N2219 silicon NPN transistor.
   d. D4, D14, D35, D46 are 152-075 germanium diodes.
4. Block logic:
   a. After the start of sweep, at a time chosen by the 100% zone control, the 100% memory gate switches the multi.
   b. The multi (a bistable Schmitt multi) output drops from 20v to 0v.
   c. At a time chosen by the 100% zone width control, the memory gate switches the multi back.
   d. The multi output returns to 20v.
   e. The result is a variable width, negative going 20v pulse, delayed after the start of sweep by the 100% zone position control.
   f. The pulse is mixed with the 0% zone and fed to the analog display through pin 10 (via D46).
   g. The pulse also opens the 100% memory gate.
5. 100% zone gate and multi:
   a. Prior to sweep, the gate is off, placing pin 12 at 0v.



b. Pin 14 and Q14 base is clamped by D14 at -.3v.

(1) Q14 is cut off.

c. Q4 is saturated with all elements at about 20v.

(1) Q4 base is pulled toward ground by the + Gate on pin 12.

d. Q25 is cut off and Q35 is saturated.

(1) Q35 collector is pulled up to 20v.

e. In this condition (Q4 saturated), a counter clockwise setting of the 100% zone could bring Q14 into conduction.

(1) The absence of a gate voltage at pin 12, however, holds Q4 saturated.

(2) Q4 collector is held up to 20v.

(3) Q25 remains cut off.

(4) The gate circuit can be considered locked out.

f. Just after the start of sweep, the gate (delayed in 0% zone card) lifts pin 12 to 17v.

g. Q4 base rises to 20.3v (clamped by D4).

h. Q4 cuts off.

(1) The divider composed of R3, R4, R12 tries to pull Q4 collector up toward 65v, but is clamped by the Q4 base-collector junction.

(2) As the base collector junction becomes forward biased, the collector is clamped at 21v (diode action of Q4 base-collector junction).

i. As the sweep ramp begins to raise Q14 base (pin 14), the transistor begins to conduct.

(1) Q14 base has been clamped at -.3v by D14.

(2) The 100% zone position control sets the point in time when the sweep ramp cuts off D14 and lifts Q14 base into conduction.

j. Q14 ciruict is an operational amplifier (R12 is R_f).

(1) When D14 cuts off, the base rises with the sweep ramp to .6v.

(2) As Q14 conducts, its collector falls as an inverted linear ramp.

(3) While Q14 conducts, a feedback through R12, the base-emitter junctions holds the base at .6v.

k. As Q14 collector runs down, Q25 base is pulled down.

(1) At about 18.8v, Q25 base is pulled into conduction and the multi flips.

(2) By multi action, Q25 saturates as Q35 cuts off.

(3) Q35 collector drops (from 20v) to be caught by D35 at -.3v.

l. As Q14 collector continues to run down, Q4 base is pulled down through the 100% zone width control.

(1) When the base reaches 19.4v, Q4 conducts.

(2) The 100% zone width adj. sets the point on the sweep ramp when Q4 conducts.

(3) Zone width is variable up to about 4 cm when it abruptly increases to full screen width.

m. As Q4 conducts, its collector pulls up to 20v.

(1) Q25 cuts off and the multi flips.

(2) Q35 saturates.

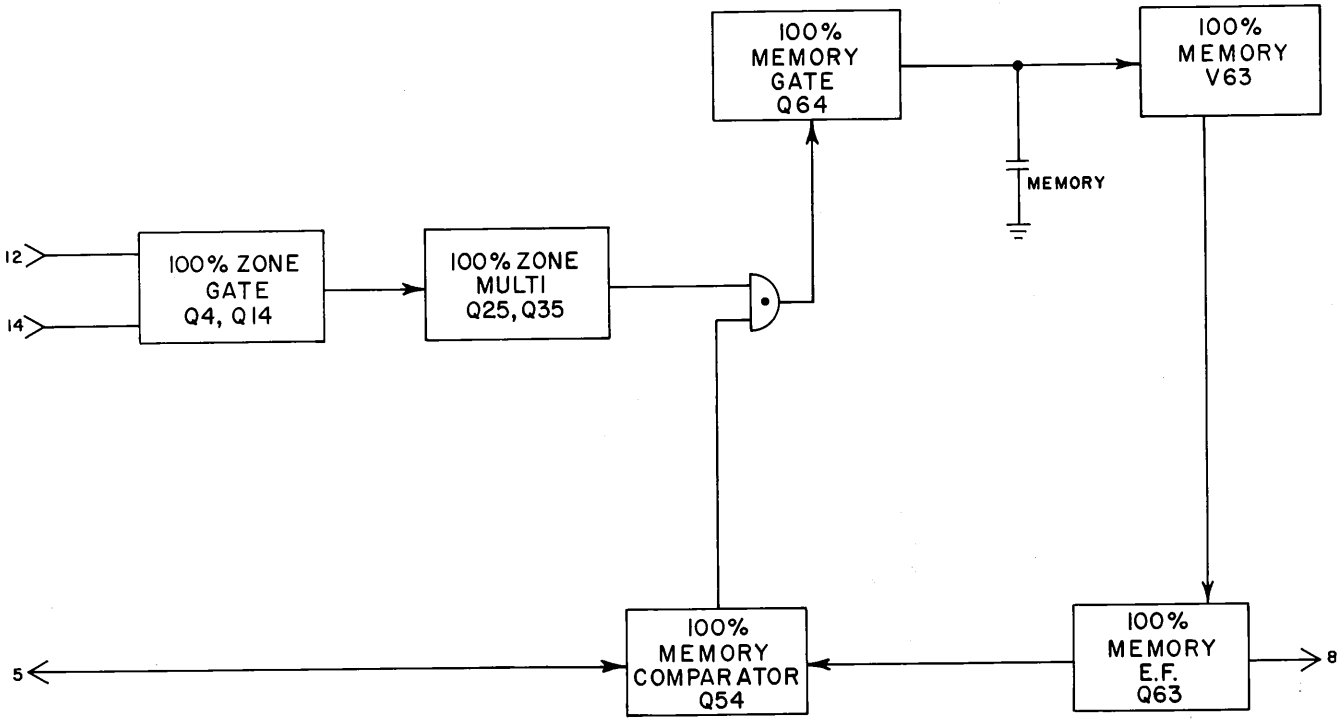
(3) Q35 collector pulls up to 20v.

n. The variable width pulse is completed.

o. At the end of sweep, retrace cuts off Q14 and the end of gate pulls Q4 into saturation. locking out the circuit.

H. The 100% Memory, Q64, V63, Q63

1. The 100% memory circuit provides a DC voltage representing a sample of the vertical signal during a time indicated by the 100% zone.



TYPE 6RIA MEMORIES CARD
100% ZONE MEMORY (AVG) BLOCK

B-6RIA-0009
6-5-'64 dl

2. Circuits that comprise the 100% zone memory:

a. 100% memory gate, Q64.

b. 100% memory, V63.

c. 100% memory EF, Q63.

d. 100% memory comparator, Q54.

3. The circuit uses three transistors, a nuvistor, and ten diodes.

a. Q63 is a 151-103, 2N2219 silicon NPN transistor.

b. Q64 is a 151-133 Motorola MM999 silicon PNP transistor.

c. V63 is a 6CW4 nuvistor.

d. Q54 is a 151-104 selected Fairchild SP8481 dual silicon NPN transistor.

e. D52, D59, D61 and D65 are 152-075 germanium diodes.

f. D57, D58 and D64 are 152-143 Raytheon RD800 silicon diodes.

4. Block Logic

a. A feedback loop is composed of the memory gate (Q64), the memory tube (V63) and capacitor, the memory EF (Q63) and the memory comparator (Q54).

b. When the 100% zone arrives, the loop is coupled to the vertical signal at pin 5.

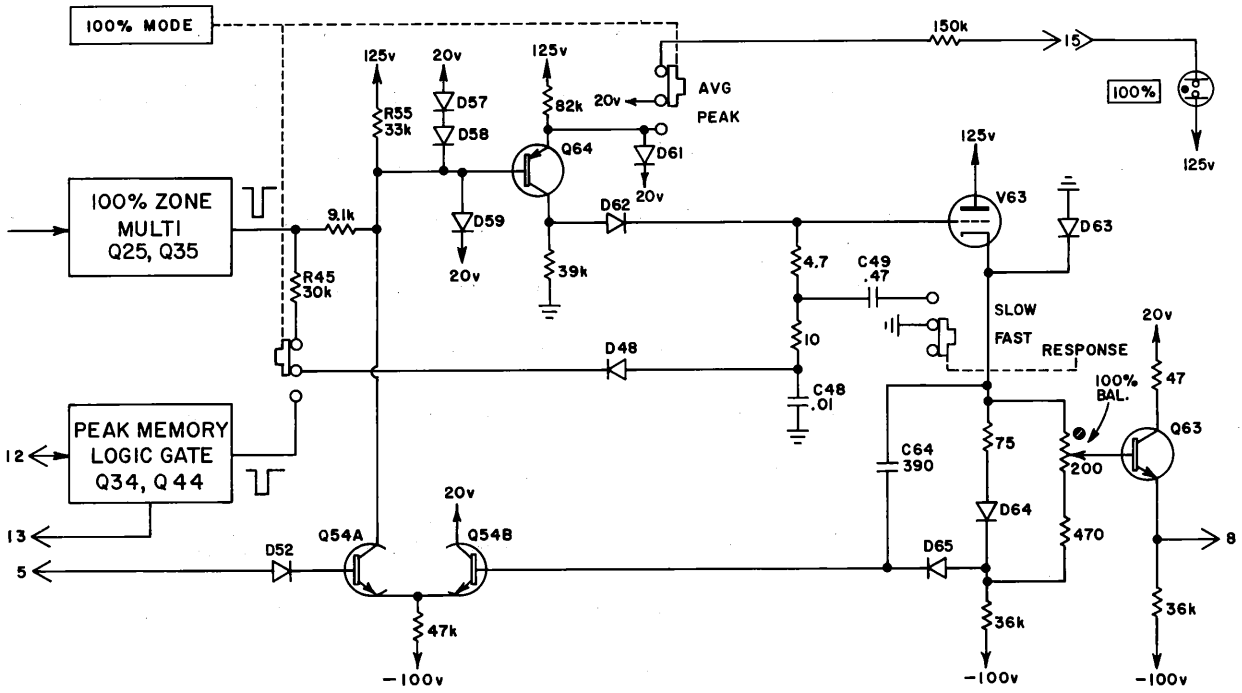
c. The memory capacitor is charged to the level of the vertical signal.

d. After the 100% zone has passed, the loop opens, allowing the charge on the memory cap to remain.

e. With the arrival of subsequent 100% zones, the comparator compares the charge on the memory cap with the input vertical signal and either verifies the level of the charge or corrects the different (AVG mode).

f. The memory output on pin 8 is a DC voltage equal in amplitude to the signal on pin 5 during the 100% zone.

g. The feedback loop works to retain this condition.



TYPE 6RIA MEMORIES CARD
100% MEMORY (AVG)

B-6RIA-0010
6-8-'64 dl Ⓐ

5. Two switches select memory circuit modes of operation.

a. The RESPONSE switch selects either FAST or SLOW response.

(1) The SLOW position uses a .47 μf memory cap in parallel with .01.

(2) The FAST position selects a .01 μf memory cap.

(3) FAST memory is useful when SLOW memory could not become charged in the time available.

(4) For sampling displays, the SLOW memory tends to average many 100% zone samples, thereby reducing the chance of noise influencing the count.

(5) The larger SLOW memory cap will drift less with leakage currents between 100% zone samples.

b. The 100% MODE switch selects either AVG (average) or PEAK.

(1) In AVG mode, the memory cap stores its charge from one 100% zone to the next.

(2) Noise or ripple, riding on a waveform, does not influence the readout in the AVG mode.

(3) In the PEAK mode, the memory cap is discharged at the end of each trace, except when print command is negative (count condition).

(4) PEAK memory stores the peak of the last 100% zone before the count.

(5) PEAK memory is useful for waveforms that do not contain a flat top; a sinewave for example.

(6) AVG position lights the 100% ZONE indicator light.

6. Prior to the arrival of the 100% zone, the 100% zone multi output is at 20v.

a. Q64 is cut off, breaking the feedback loop.

(1) Q64 base is clamped at 20.3v by D59.

(a) D59 current flows through R55 to 125v.

(2) D61 clamps Q64 emitter at 20.3v.

(3) The collector is at 0v.

b. D62 is cut off.

c. D48 is cut off (AVG position).

d. V63 grid is sitting at a level equal to the charge on the memory cap (C48 and/or C49).

e. V63 is conducting with the cathode about 1.6v above its grid.

f. Q63 is conducting.

(1) Q63 base and emitter potentials (relative to V63 grid) are subject to a setting of the 100% BAL control.

(2) The emitter (pin 8) usually sets about 800 mv above V63 grid.

(3) The base sets at 1.4v above V63 grid.

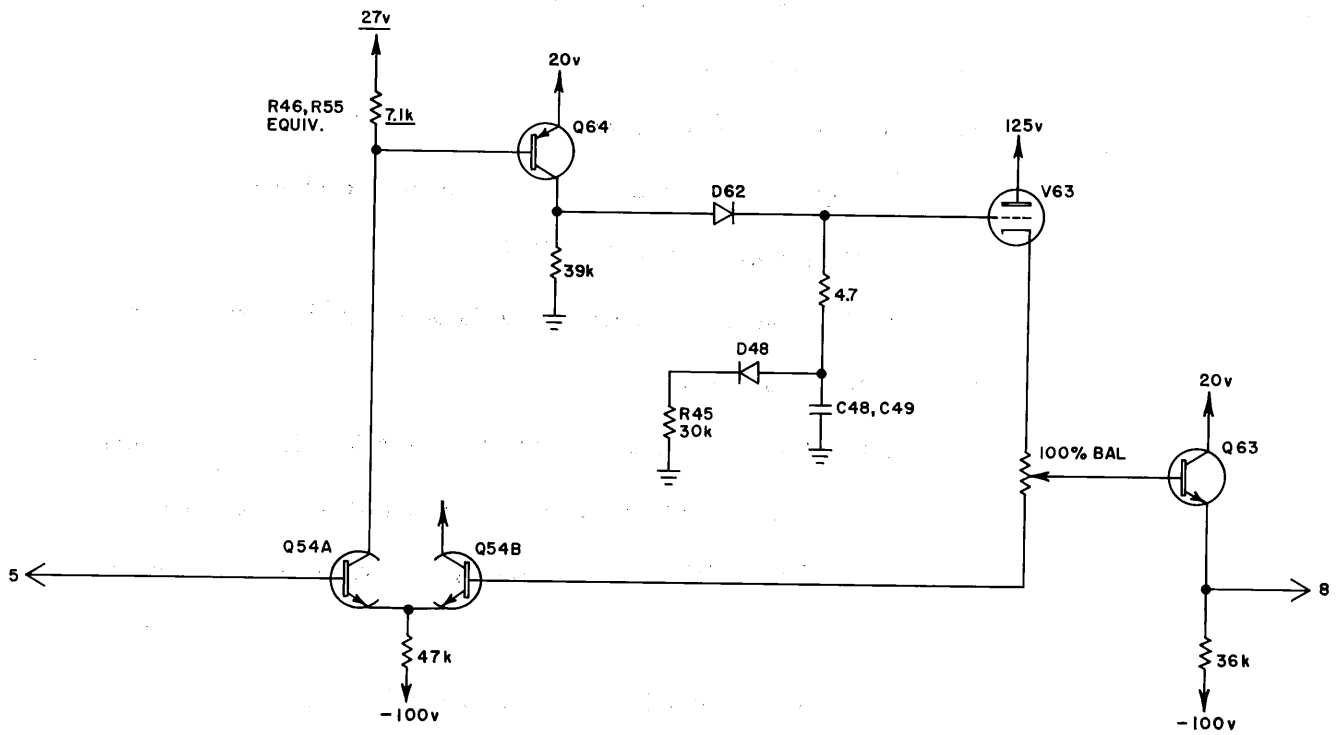
7. Both sides of Q54 may be conducting or only one side conducting.

a. If the vertical signal swings Q54A base .6v more negative than Q54B base (Q54B base level is set by the charge on the memory cap), Q54A cuts off.

b. If Q54A base swings .6v more positive than Q54B, Q54B cuts off.

c. Since the feedback loop is open, the condition of Q54 at this time is irrelevent.

8. The 100% zone drops the 100% zone multi output to 0v.



TYPE 6RIA MEMORIES CARD
100% MEMORY (AVG) SIMPLIFIED FEEDBACK LOOP

B-6RIA-0011
6-9-'64 dl

a. R46 and R55 now form an equivalent 7.1k to 27v as Q54A collector load resistor.

b. If the comparator bases are at about the same level, Q54A and B will conduct connecting the Vertical signal on pin 5 to the Memory loop.

c. Q54A collector pulls Q64 base to 20v.

d. D59 cuts off.

e. Q64 conducts.

f. As Q64 collector pulls up, D62 conducts.

g. D48 conducts, connecting R45 (AVG position).

(1) The top of R45 is held at 0v by the 100% zone multi.

h. The memory capacitor C48 (with the response switch in FAST) or C49 (in SLOW) charges to Q64 collector level.

i. V63 is conducting with its cathode about 1.6v more positive than its grid.

j. Voltage-drops around the loop are such that the charge on the memory cap will set Q54B base at the same level as that on Q54A base.

k. The output level at pin 8 will equal the level on pin 5.

(1) Vertical signal sensitivity at pin 5 is 1v/div.

9. Each time the 100% zone connects the memory loop, the circuit will either confirm the fact that the level at pin 8 is the same as that on pin 5, or will correct the difference.

a. The comparator (Q54) compares the level on its bases.

(1) If a difference occurs, the error voltage is amplified in Q64.

(2) The memory cap is charged to the new level.

b. Should the level on pin 5 be much lower than that on pin 8, D62 will cut off as the memory cap discharges through D48, R45 and D35 (100% zone multi gate) toward ground.

(1) Under this condition, Q54A will cut off and its collector will rise toward 27v (R45, R55 divider voltage).

(2) The rise at Q64 base is limited at 20.3v by D59.

(3) Q64 cuts off and its collector drops to ground, cutting of D62.

(4) D52 protects Q54A from base-emitter breakdown.

c. As the memory cap discharges to its new level, Q54B base and emitter drop until Q54A again conducts.

(1) Q64 turns on, D62 conducts, confirming the new memory level.

(2) A large fast drop in level at pin 5 from one 100% zone sample to the next could require the time of several 100% zones to discharge C49 (in the SLOW response position).

(3) The time constant is 14.4 msec as C49 (and C48) discharge through R45.

(4) Since the bottom of the graticule sets the memory cap at 6v, it will never have to discharge more than from 14v (graticule top) to 6v -- center screen sets the memory at 10v.

(5) The greater the real-time width of the 100% zone, the faster the memory cap will discharge, allowing the feedback loop to reconnect.

(6) About 12 msec of zone time is required to drop the memory from 14v to 6v.

d. Should the level on pin 5 rise suddenly, there is sufficient current available through D62 and Q64 to charge the memory to its new level somewhat more rapidly than a change in the negative direction.

(1) Until the memory cap reaches its new level, Q54B will be cut off and the loop broken.

(2) With Q54B cut off, Q54A will conduct heavily, pulling Q64 base down.

(3) Q64 base is caught at 18.8v by D57 and D58.

e. As Q64 collector current exceeds 1.28 ma, D61 disconnects (AVG mode), limiting collector current.

(1) Memory charging current is limited on peaks.

(2) Peak voltage levels at the vertical input (pin 5) are averaged out by the current limiting circuit (Q64, R61, D61).

f. As the memory loop connects, an overshoot appears caused by delay in feedback.

(1) R48 and R49 allow the overshoot to pass without effecting the charge on the memory cap.

10. At the end of the 100% zone, multi output returns to 20v.

a. Q64, D62 and D48 cut off simultaneously, opening the loop.

b. The memory cap, with all discharge paths open, retains its charge until the next 100% zone.

(1) Leakage paths during this period include reverse leakage through D62 and D48, V63 grid current, and leakage through the memory cap itself.

(2) Leakage from all sources should not exceed 2.5 nanoamps.

11. All voltage levels in the circuit composed of V63, Q63, and Q64B have a fixed relationship to the charge on the memory cap.

a. These levels change only when (during the 100% zone) a difference voltage occurs between pin 5 and pin 8.

b. Emitter Follower, Q63, provides a low impedance drive for the stray capacitances present in the connectors, cables, switches, etc.

c. D64 provides temperature compensation for Q63 base-emitter junction.

d. D65 protects Q54B base emitter junction from breakdown.

(1) If the vertical input (pin 5) suddenly rises, Q45A emitter would follow its base.

(2) Q54 emitter could be pulled as much as 8v above its base.

(3) When base-emitter breakdown occurs at 5v, D65 disconnects, protecting the transistor.

e. If the charge on the memory cap is suddenly increased, the positive step gets coupled through C64 (while waiting for D65 to come into conduction), connecting the feedback loop and reducing overshoot at the memory.

f. D63 protects Q63 from base collector breakdown if V63 heater opens and protects V63 cathode during warm-up.

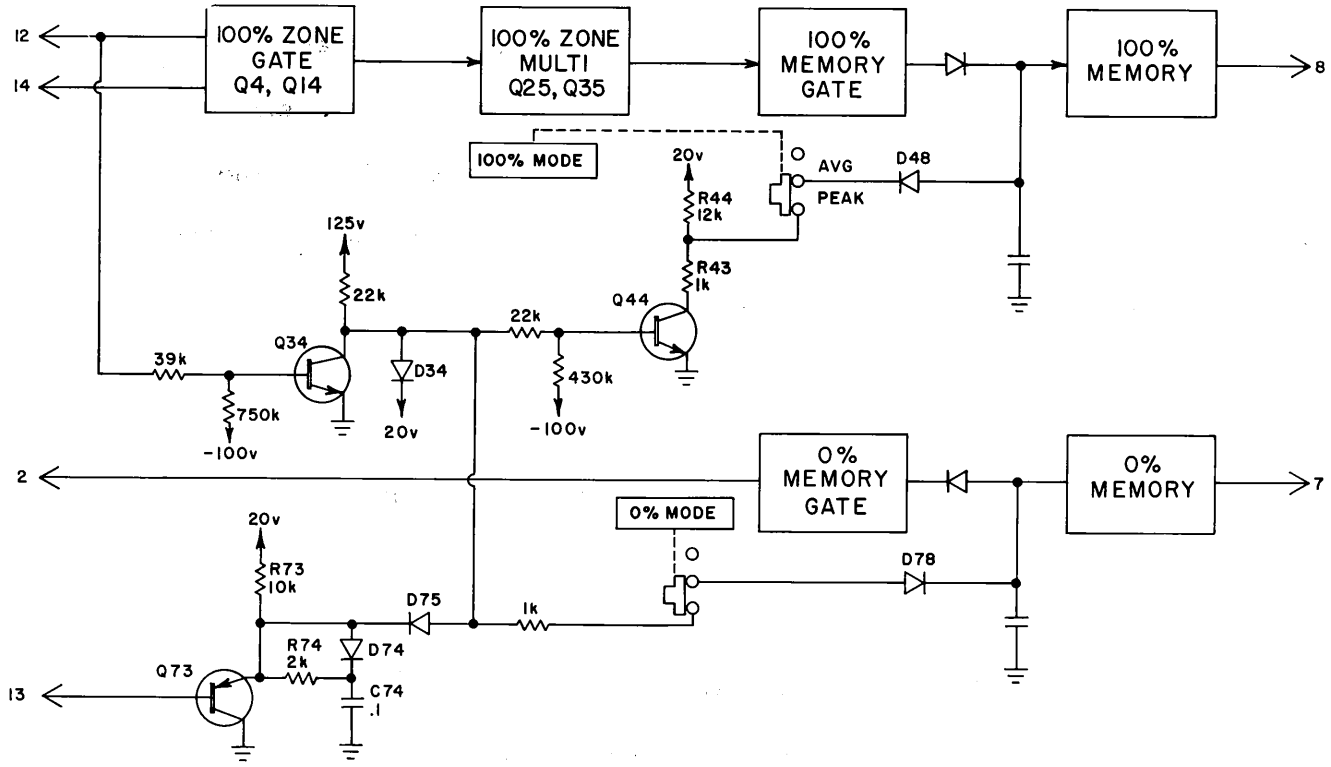
12. The 100% BAL control essentially sets the DC level at the memory output (pin 8) so that the output, as well as Q54B base, is at the same level as the vertical input (pin 5).

I. 100% Peak Memory Logic Circuit, Q34, Q44

1. The circuit uses two transistors and two diodes.

a. Q34 and Q44 are 151-069 germanium NPN transistors.

b. D34 and D75 are 151-075 germanium diodes.



TYPE 6RIA MEMORIES CARD
PEAK MEMORY LOGIC GATE AND PRINT COMMAND E.F.

B-6RIA-0013
6-11-'64 dl

2. Block Logic

a. In the PEAK position of the 100% MODE switch, D48 is connected to Q44 collector.

(1) As Q44 conducts, the memory capacitor is discharged.

(2) This occurs during retrace, except when the print command is negative.

b. The circuit can be considered an AND gate.

(1) When the sweep gate (pin 12) is NOT ON, and the print command (pin 13) is ON (print command at 20v), the circuit has an output.

(2) The output is the same duration as the sweep gate -- 20v during sweep and 1.5v during retrace.

(3) The negative going portion of the waveform is used to discharge the memory cap in 100% memory.

(4) Another output with a positive going gate charges the 0% memory cap.

3. Circuit operation:

a. During sweep, Q34 is saturated.

(1) The sweep gate waveform at pin 12 is at 18v, pulling Q34 base to .3v.

(2) The collector is at ground.

b. Q44 is cut off.

(1) The collector is at 20v.

c. D48 is cut off.

(1) The memory cap is allowed to charge to the vertical signal peak value during zone time.

d. At the end of sweep, the voltage at pin 12 drops to 0v and Q34 cuts off.

(1) The collector rises toward 125v, but is limited at 20v by D34.

e. Q44 saturates.

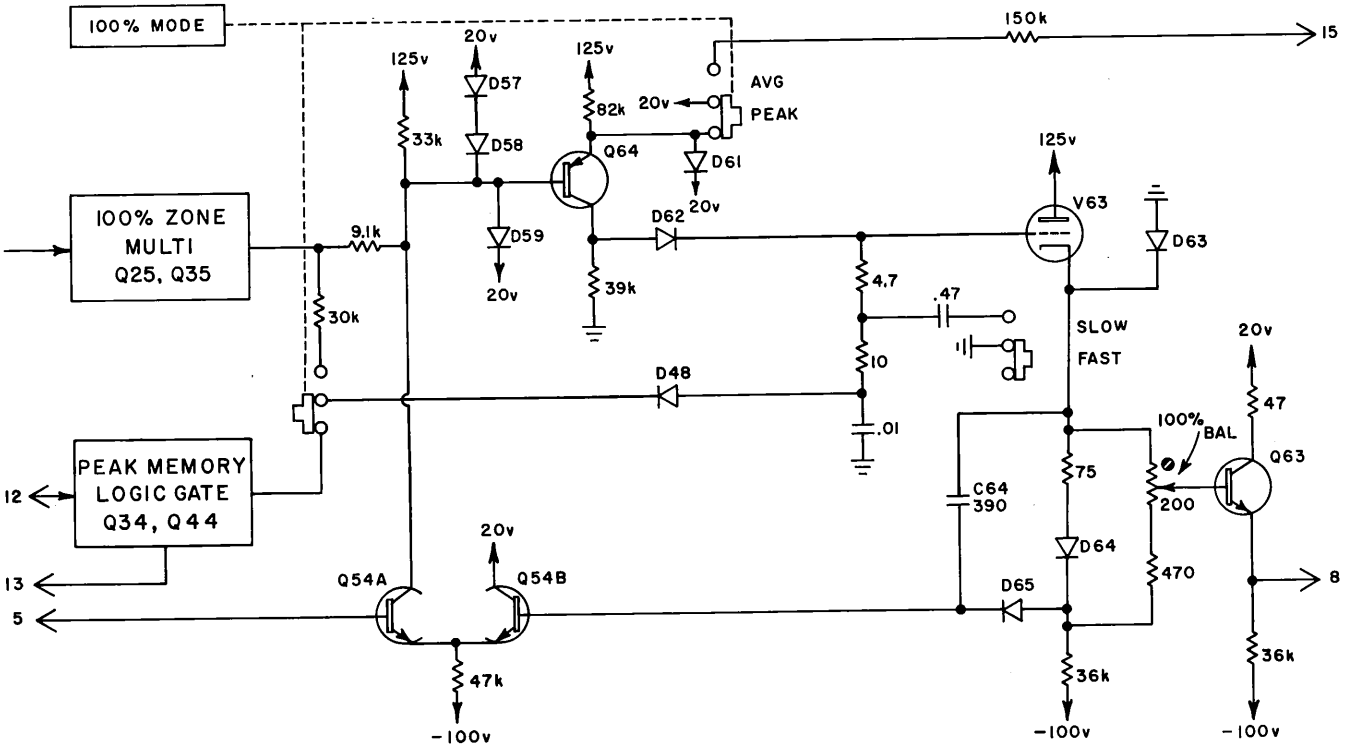
f. A tap on the divider R43, R44 discharges the memory cap to 1.6v.

(1) In SLOW position, the cap may not become fully discharged.

g. If the print command is off (count state) at the time the sweep gate is off, Q34 collector cannot raise above .6v.

(1) Q44 remains cut off.

(2) The memory cap is not discharged.



TYPE 6RIA MEMORIES CARD
100% MEMORY (PEAK)

B-6RIA-0012
6-10-'64 dl

h. When the 100% MODE switch is in the PEAK position, Q64 emitter is tied directly to 20v.

(1) Current limiting is removed.

(2) More current through Q64 is required to charge the memory cap during one 100% zone.

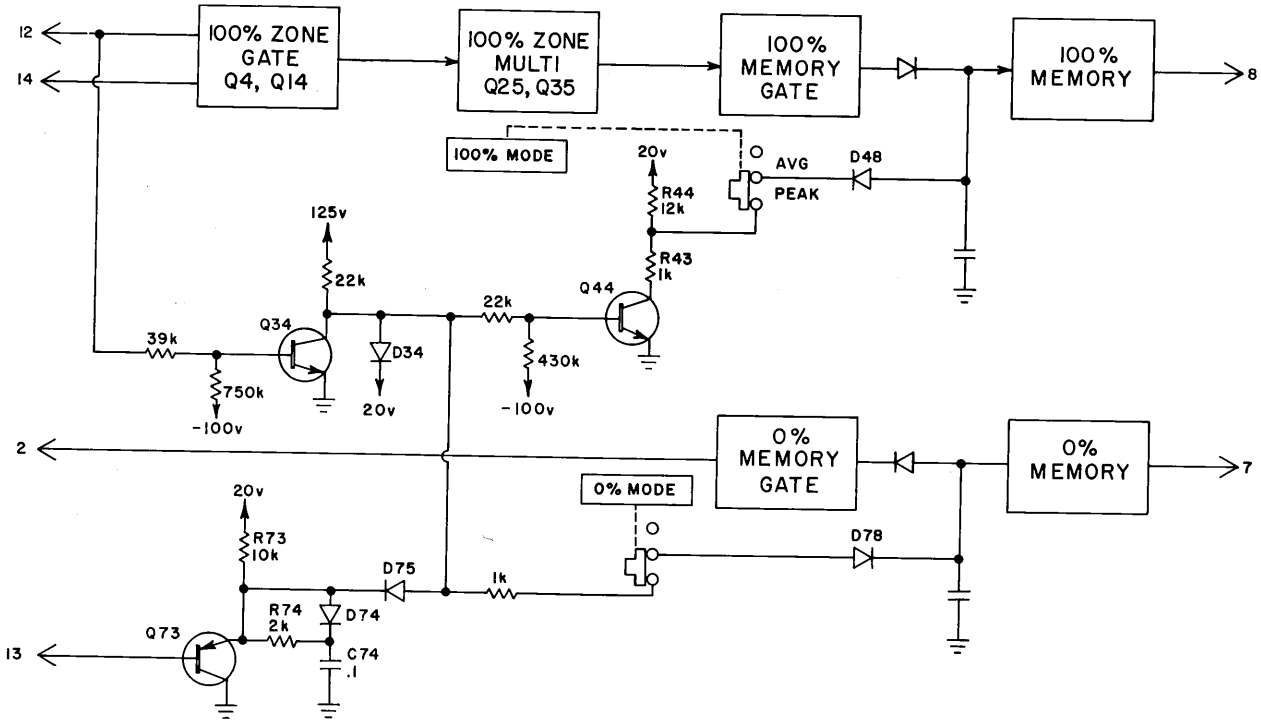
(3) The memory cap must be fully charged during the 100% zone because the cap becomes discharged each retrace.

J. Print Command EF, Q73

1. The Print Command EF and delay circuit is needed only when a Peak Memory card is used in a 6R1 with an old Master Gate card. (This combination is not recommended and the EF circuit may someday be removed.)

2. The New Master Gate board has a Print Command EF so an additional EF in the Memories card is redundant.

a. The old Master Gate card had a 4.7k output.



3. The circuit consists of one transistor and two diodes.
   a. Q73 is a 151-071, 2N1305 germanium PNP transistor.
   b. D74 and D75 are 152-075 germanium diodes.
4. When the input waveform at pin 13 drops to 0v (from 20v), Q73 saturates -- Print Command count state.
   a. The emitter drops to 0v.
   b. D74 cuts off.
   c. D75 conducts, pulling Q34 collector to ground.
   d. The Peak Memory Logic circuit is locked out -- it cannot develop the peak memory pulse to erase the memory.
5. When the print command signal raises to 20v, Q73 cuts off.
   a. As the emitter starts to rise, D74 conducts.
   b. C74 must charge through R74 and R73 before the emitter can raise to 20v.
      (1) There is about 6 msec delay.
6. The Peak Memory is locked out from the start of the Print Command negative pulse until about 6 msec after the waveform returns to 20v.
7. The delay circuit prevented a possible malfunction in the rare instance that we have an internal voltage measurement and the sweep would end when the voltmeter ramp was part way through its retrace.
   a. In this event the print command lockout would end, allowing the Peak Memory pulse to erase the 100% memory -- discharge the memory cap.
   b. When erasing, the 100% memory output, as fed to the reference side of the comparator board would be a negative going signal.

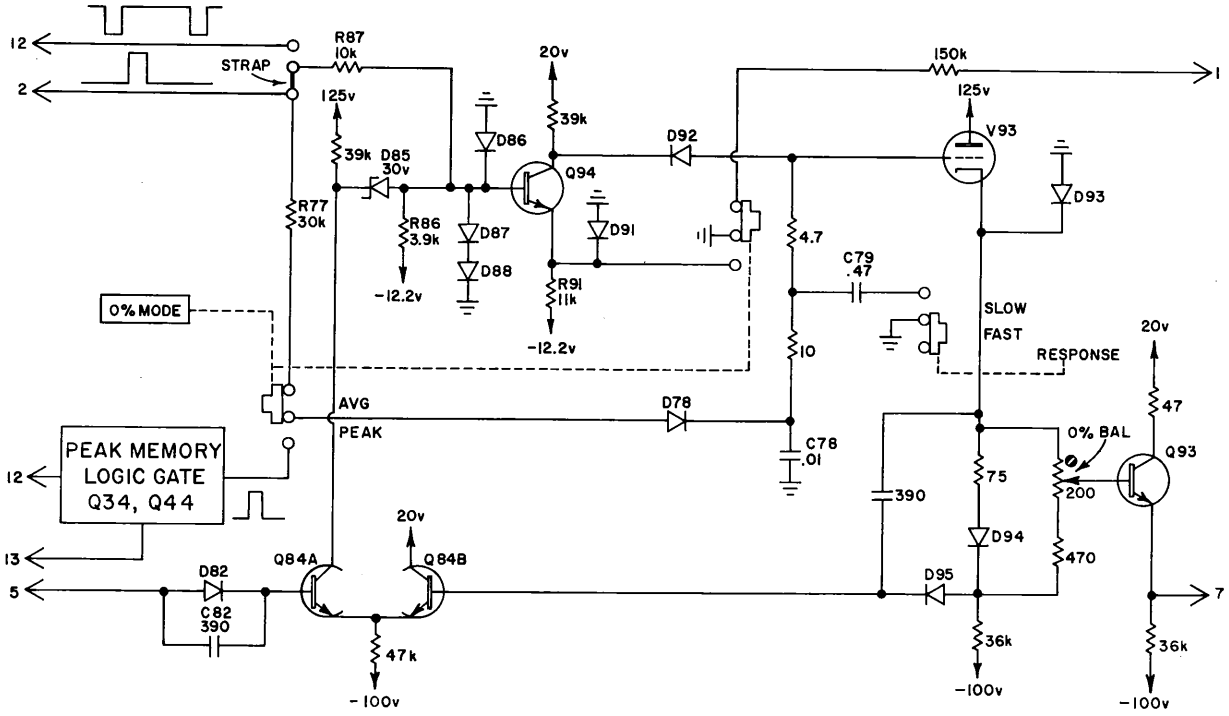
c. Since this voltage would go negative faster than the retrace of the voltmeter ramp (connected to the signal side of the comparator card) the waveform would pass the voltmeter ramp retrace.

d. The negative going memory passing the voltmeter ramp retrace will fire the comparator (just as if the ramp had been going positive through a reference level) and produce a STOP condition.

e. Since (in the 6R1) resetting the Stop Multi occurred at the end of voltmeter run-up (Ramp Gate), flipping the stop multi during retrace constitutes a malfunction.

f. In the 6R1A, Print Command cannot occur right after stop multi reset (reset occurs at the end of the deal zone). The delay network is no longer needed.

K. 0% Memory Circuit; Q94, V93, Q93, Q84



TYPE 6RIA MEMORIES CARD
0% MEMORY (AVG)

B-6RIA-0014
6-15-'64 dl

1. The 0% memory uses the same general circuit configuration, the same transistors, diodes and nuvistors as the 100% memory.
   a. An exception is the memory gate (Q94) which is a NPN instead of a PNP, as in the 100% memory.
2. Block logic:
   a. The 0% zone from the 0% zone card (via pin 2) connects the memory loop.
   b. While the loop is connected, the 0% memory cap is charged to the level of the vertical input.
   c. The 0% memory circuit works to maintain the DC level on pin 7 at the same level as that on pin 5 during the 0% zone.
3. Like the 100% memory, the circuit has two switches to select modes of operation.
   a. The RESPONSE switch is ganged with the 100% zone RESPONSE switch.
   b. The 0% MODE switch allows selection of AVG or PEAK modes.
   c. The 0% PEAK mode, however, allows the memory cap to charge to negative peaks.
   d. The AVG position lights the 0% zone indicator light.
4. Circuit conditions prior to arrival of the 0% zone.
   a. The 0% zone is a 17v positive going waveform.
      (1) 0v quiescent with a 17v pulse.
   b. Prior to arrival of the 0% zone, Q94 is cut off -- the feedback loop is open.
      (1) With pin 2 at 0v, the divider R86, R87 pulls D86 into conduction setting Q94 base at -.3v.

(2) The emitter is clamped at -.3v by D91 (AVG mode).

(3) The collector is at 20v.

c. D92 is cut off.

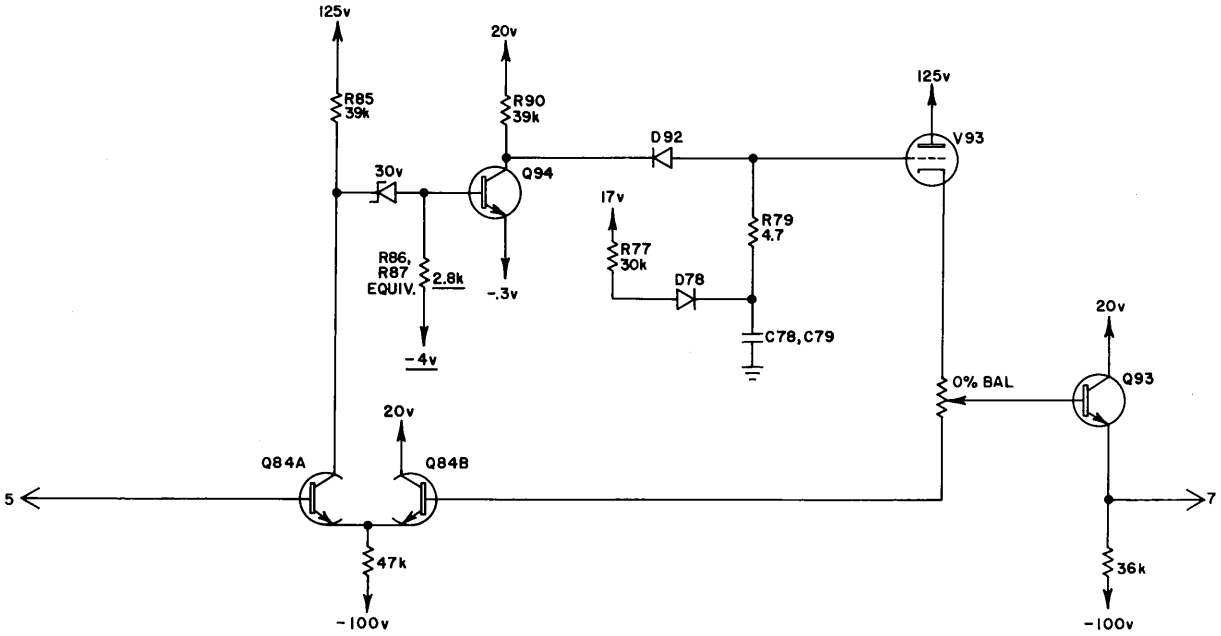
d. D78 is cut off.

(1) The 0v at pin 2 pulls D78 anode to ground.

(2) If the memory cap has a charge, D78 cuts off.

e. As in the 100% memory circuit, DC levels at V93, Q93 and Q84B are relative to the level of the charge on the memory cap.

5. The arrival of the 0% zone connects the feedback loop.



TYPE 6RIA MEMORIES CARD
0% MEMORY CARD (AVG) SIMPLIFIED FEEDBACK LOOP

B-6RIA-0015
6-16-'64 dl◀A

a. The comparator compares the levels on its bases.

6. Assume there has been little or no change in level on Q84 bases since the previous 0% zone.

a. 1 ma through Q84A, 1.4 ma through R86, R87 equivalent and 2.4 ma through R85 places Q94 base at about 0v.

(1) D86, D87 and D88 are cut off.

(2) Q94 base is free to accept vertical information from Q84A collector.

b. Q94 conducts; its collector pulls down to establish the charge on the memory cap (C79 and C78 in SLOW or C78 in FAST) to a level representative of the level at the vertical input at pin 5.

(1) The voltage on the memory cap is a function of current through Q94, D92, R79, R78, D78, R77 to the 17v (0% zone pulse) at pin 2.

7. Should the level at pin 5 be much lower than the level on Q84B base, Q84A could cut off -- or both D82 and Q84A may cut off, if pin 5 is low enough to cause Q84A base emitter breakdown.

a. Q94 base would rise, to be limited by D87, D88 at 1.2v.

b. Increased current through Q94 would pull up on the emitter disconnecting D91.

(1) Current is limited by R91.

c. As Q94 collector is pulled down, the memory cap charges to a new level.

(1) In SLOW RESPONSE it might take several 0% zone cycles to discharge the memory cap to its new level.

(2) The discharge path is through R91, Q94, D92, D78, R77 to the 17 volts on pin 2.

d. As the memory cap drops to its new level, Q84B base will also drop, bringing Q84A into conduction.

e. Q94 base will pull down cutting off D87 and D88.

f. The memory loop will again connect.

8. If the vertical level at pin 5 is suddenly moved to a higher level than during the previous 0% zone, Q84A emitter will lift Q84B emitter to cut-off, opening the memory loop.

a. As the positive change is inverted in Q84A and again in Q94, D92 will cut off.

b. The memory cap is charged to its new higher level through D78.

c. When the memory cap has charged to its new level, Q84B base will rise to the level of Q84A base and as Q84B conducts, the memory loop will connect.

9. The protective diodes serve the same purposes as those in the 100% memory.

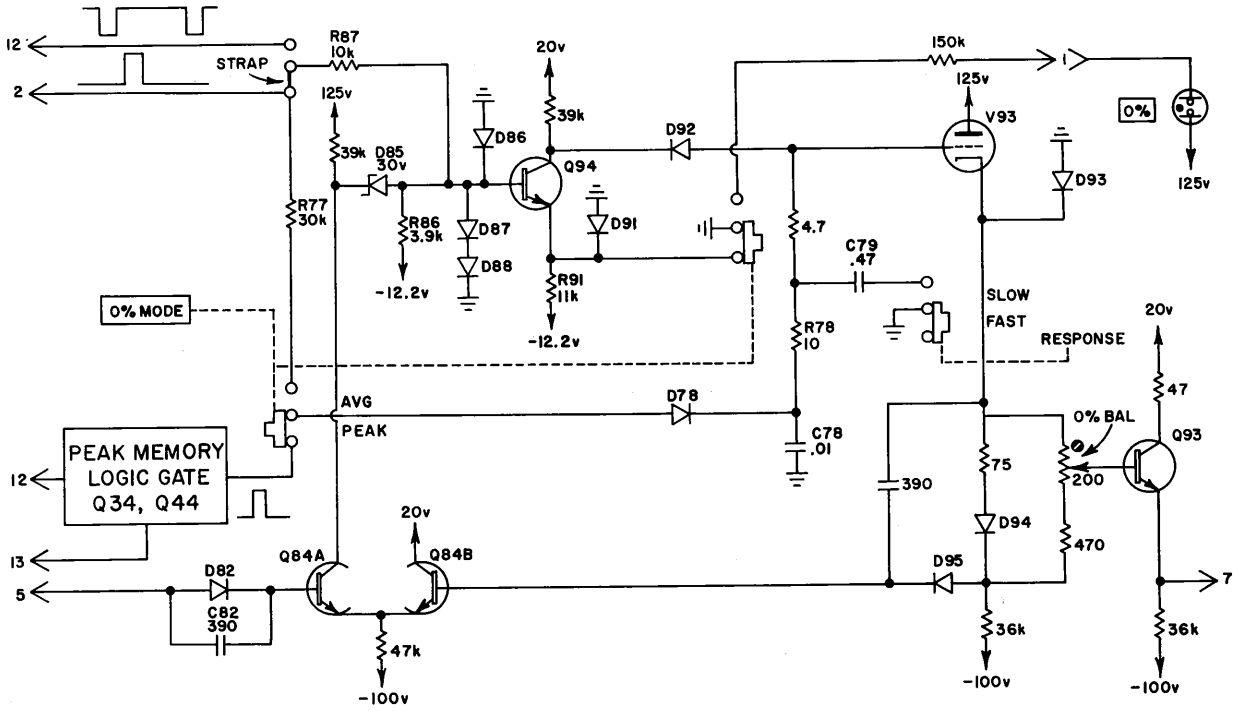
a. D82 and D95 protect Q84 from base emitter breakdown during large fast changes in vertical level or during peak memory.

(1) C82 increases D82 fixed stored charge to turn on Q84A fast.

b. D93 protects V93 cathode and protects Q93 from base collector breakdown if V93 should open.

c. D94 is temperature compensation for Q93 base emitter junction.

10. 0% Peak Memory operates in the same general manner as the 100% Peak Memory.



TYPE 6RIA MEMORIES CARD
0% MEMORY PEAK

B-6RIA-0016
6-17-'64 dl

a. Since the 0% memory <u>discharges</u> the memory cap, the peak memory must <u>charge</u> it through D78.

b. The Peak Memory gate waveform is a <u>positive</u> going pulse from the Peak Memory Logic circuit.

c. At the end of sweep, and when the print command is positive, the Peak Memory pulse charges the memory cap to 17v.

d. When the 0% zone arrives, the memory cap is discharged to the <u>negative</u> peak of the vertical signal.

11. With both the 100% MODE and the 0% MODE switches in PEAK, the 6R1A reads peak-to-peak.

a. The 100% Peak Memory reads positive peaks and the 0% Peak Memory reads negative peaks.

b. With the 0% Memory in AVG and the 100% Memory in PEAK, the reading is Zero to Peak.

12. A removable strap connects the 0% memory circuit to the 0% zone pulse on pin 2.

a. The strap may be moved (unsoldered) to connect the memory circuit to the + gate on pin 12 instead.

b. In this position, the 0% memory cap will discharge to the negative peak of the entire display instead of just the 0% zone.

c. In AVG mode, the 17v 0% zone connects D78 once each sweep cycle.

(1) If the negative peak has moved more positive since the last cycle, cutting D92 off, D78 will lift the memory until D92 connects, charging the memory cap to its new level.

d. In PEAK mode the memory will be erased (reset to 20v) each time the Peak Gate pulse arrives.

e. In the 6R1A, increasing 0% zone width to the full sweep width will serve the same purpose as the strap.

f. The strap, then, is only needed when used in a 6R1 with a 0% zone card that has a fixed width.

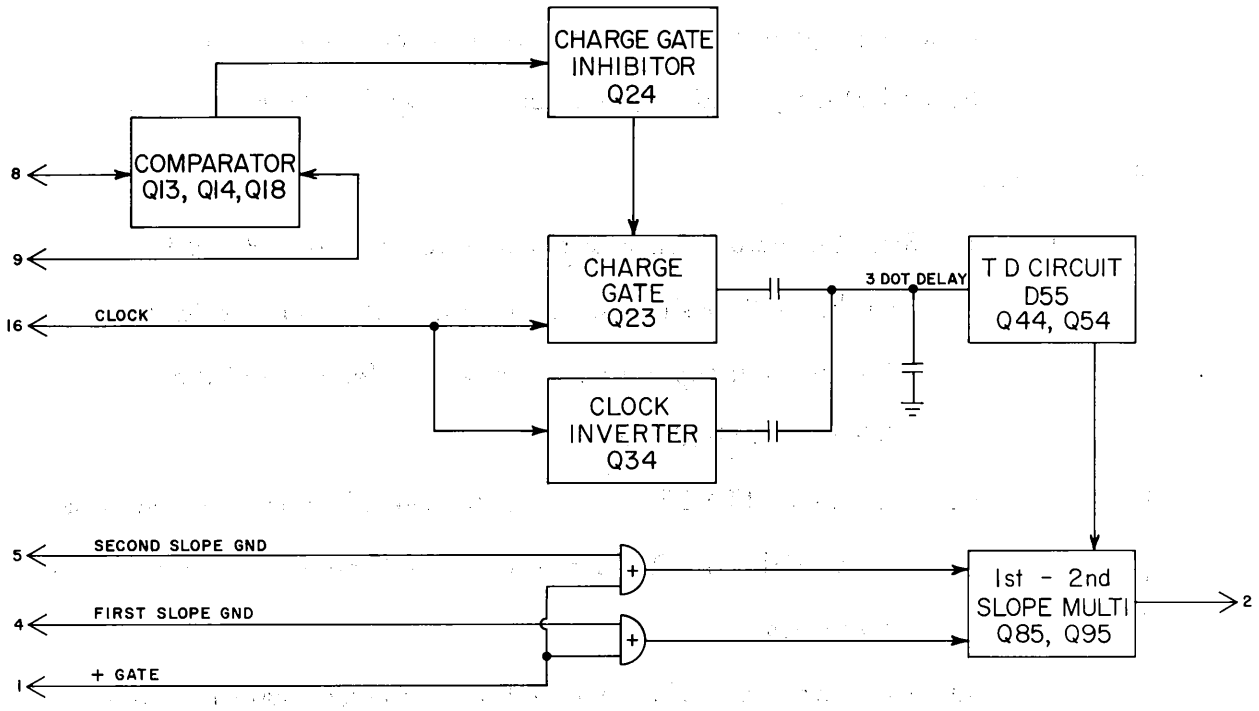
VII. SIGNAL COMPARATOR

A. Two identical and interchangeable Comparator Cards are used in each Type 6R1A.

1. One card , termed the Start Comparator, provides a positive going step to the Master Gate to start the count.

2. The other card, called the Stop Comparator, sends a positive going step to the Master Gate to stop the count.

B. Block Diagram



TYPE 6RIA SIGNAL COMPARATOR CARD BLOCK DIAGRAM

B-6RIA-0036
7-30-'64 dl

C. Circuits that comprise the Signal Comparator Card:

1. Comparator, Q13, Q14, Q18.
2. Charge Gate Inhibitor, Q24.
3. Charge Gate, Q23.
4. Clock Inverter, Q34.
5. TD Circuit, D55, Q54.
6. First-Second Slope Multi, Q85, Q95.

D. Inputs:

1. Voltage to be compared on pins 8 and 9 from the Mode switch.
2. 18v positive going clock pulses on pin 16 from the Voltmeter Card.
3. 20v + Gate from the 0% zone card on pin 1.
4. First Slope ground on pin 4 activated by the SLOPE switch.
5. Second Slope ground on pin 5 activated by the SLOPE switch.

E. System Logic

1. The Start Comparator compares two voltages on pins 8 and 9.
   a. In the TIME position of the MODE switch, one voltage is the Vertical signal and the other is referenced to the 0% and 100% Memories.
   b. In the VOLTAGE positions of the MODE switch, one voltage is the Voltmeter Ramp and the other is either the 0% or 100% Memories.
2. At first coincidence of the two voltages, the Comparator switches off Q24 which in turn opens the Charge Gate, Q23.
3. Positive clock pulses passing through the Charge Gate charge a capacitor in a bucket and ladle circuit.

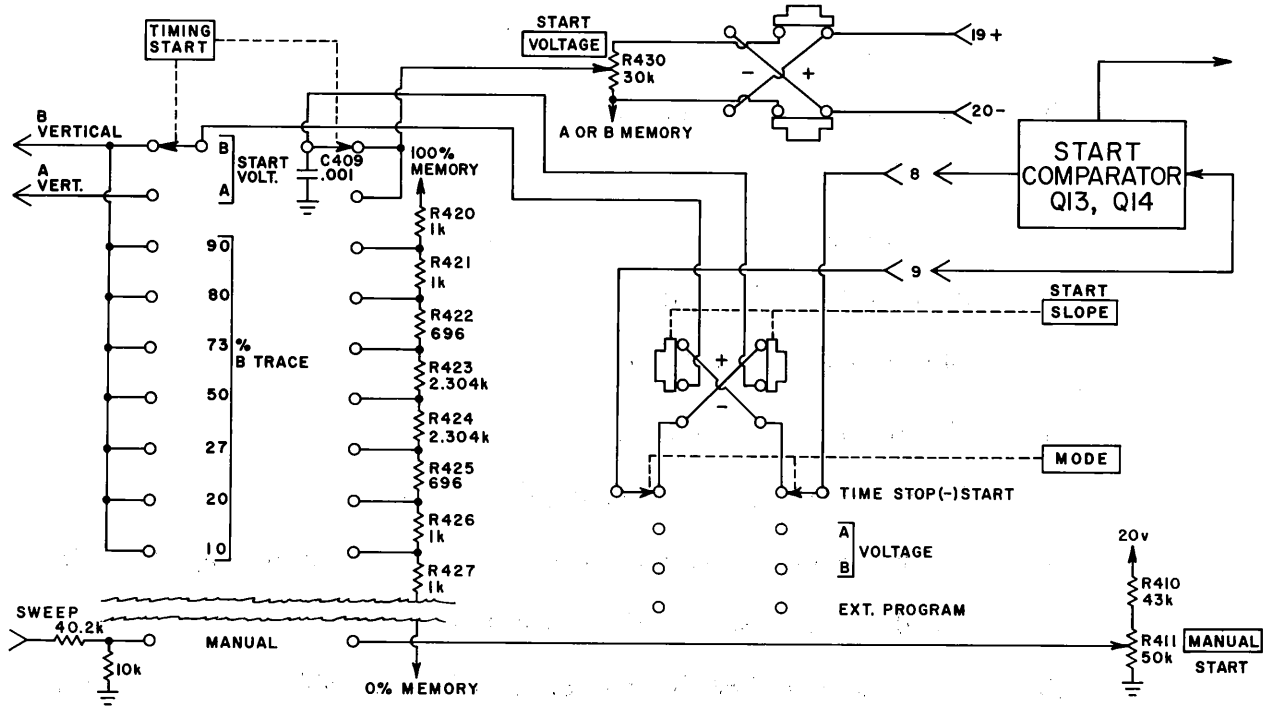
4. Three clock pulses (THREE DOT DELAY in) are required to charge the capacitor to a level where the TD will flip to its high state.
5. The TD circuit output will, in turn, flip the First-Second Slope Multi.
6. If Second Slope has been selected by the SLOPE switch, pin 5 will be grounded.
   a. As the Multi flips, a negative step appears at pin 2 -- a positive step is required.
7. If First Slope has been selected, pin 4 will be grounded.
   a. As the multi flips a positive slope appears at pin 2 to start count.
8. As coincidence again occurs at pins 8 and 9 the Comparator turns on Q24.
9. The Charge Gate is closed.
10. Clock pulses through the Clock Inverter discharge the 3 DOT DELAY cap and the TD flips to its low state.
11. The negative going output from the TD circuit has no effect on the Multi -- the Multi will react only to a plus step.
12. The First-Second Slope Multi will flip back when the signal on pin 8 (or 9) again causes the TD to switch to its high state.
13. In summary, a First Slope selection of the SLOPE switch will result in a desired output (pin 2) when the voltages first compare in the right direction at pins 8 and 9.
14. With the SLOPE switch in Second Slope position, a desired output occurs at pin 2 one complete cycle later on second comparison in the right direction of waveforms on pins 8 and 9. The circuit is a two to one countdown device.

15. The + Gate on pin 1 presets the Multi at the start of each sweep.

16. The Stop Comparator functions in the same manner.

F. Comparator Signal Sources

1. Signal sources for pins 8 and 9 of the Comparator utilize the MODE switch, the SLOPE switches, the Timing Start and Timing Stop switches, and the Start and Stop VOLTAGE POLARITY switches.



TYPE 6RIA SIGNAL COMPARATOR CARD
COMPARATOR SIGNAL SOURCE – TIME

B-6RIA-0037
7-24-'64 dl A

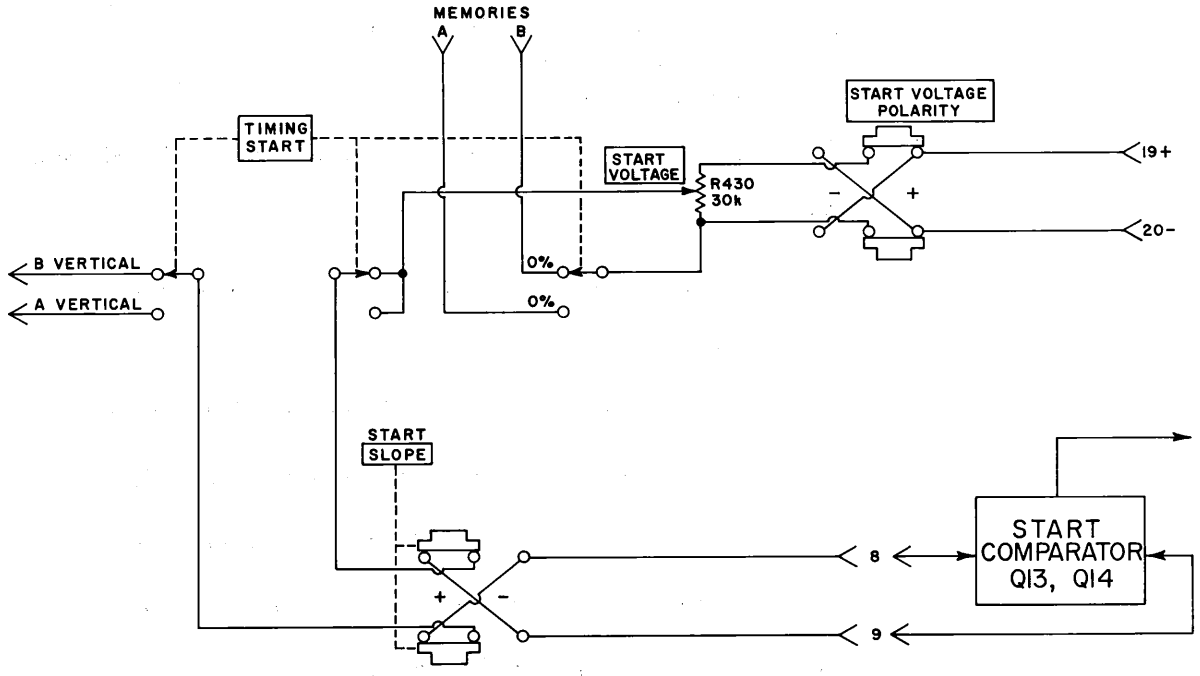
2. In the TIME position of the MODE switch, a DC reference voltage is compared with a moving vertical signal from either the A or B channel of the vertical plug-in.

   a. For + Slope comparison the DC reference voltage is applied to pin 9 and the vertical signal to pin 8.

   b. For - Slope comparison the connections are reversed by the Start SLOPE switch.

   c. To have an output, the Comparator must see either a rising voltage on pin 8 (crossing the voltage on pin 9) or a falling voltage on pin 9 (crossing the voltage on pin 8).

3. In the A Trace or B Trace positions of the TIMING START (or TIMING STOP) switch, the DC reference voltage comes from the Floating Power Supplies on the Voltmeter Card.



TYPE 6RIA SIGNAL COMPARATOR CARD
COMPARATOR SIGNAL SOURCE-TIME, A OR B TRACE

B-6RIA-0043
7-28-'64 dl

a. A separate floating supply is provided for both the Start and the Stop Comparators.*

b. Each floating supply provides exactly 10v DC.

(1) The 10 volts appears across R430, a 30k 10 turn Helipot (the START VOLTAGE or STOP VOLTAGE control).

c. The 10v floating supplies stack either above or below the A or B 0% memories.

(1) The VOLTAGE POLARITY switches reverse the polarity of the floating supplies.

(2) Since the 0% Memories have an on-screen excursion of 6v to 14v, the reference voltage at the Helipot arm has a possible excursion of -4v to +24v.

(3) In the + position of the SLOPE switch, the reference voltage is tied to pin 9.

d. The moving voltage is either the A or B vertical signal from the vertical plug-in.

(1) Signal sensitivity is 1 v/div with 10v at center screen.

(2) In the + position of the SLOPE switch, the vertical signal is applied to pin 8 of the Comparator Card.

e. In operation, the START VOLTAGE Helidial provides a precise calibrated voltage above or below the 0% zone as a reference for the START comparator.

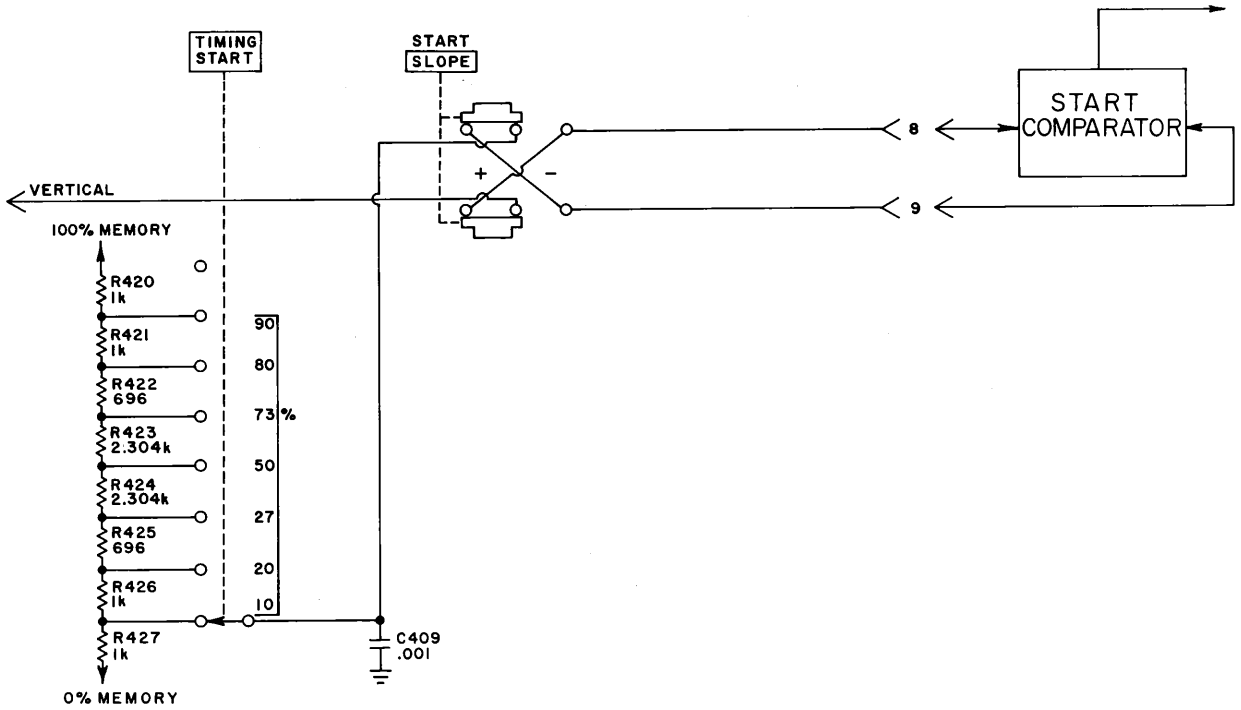
* See Voltmeter Card.

f. The STOP VOLTAGE Helidial provides a calibrated voltage from the 0% zone, a reference for the STOP comparator.

g. The Helidials are calibrated in CRT divisions from the 0% zone.

(1) Since the vertical signal has a sensitivity of 1 v/div, 1 division on the dial equals 1v.

4. In the percent positions of the TIMING START (or TIMING STOP) switch, a percent of the voltage difference between the 0% Memory and the 100% Memory is used.



TYPE 6RIA SIGNAL COMPARATOR CARD
COMPARATOR SIGNAL SOURCES - TIME, %

B-6RIA-0044
7-29-'64 dl

a. A divider is provided for Start Comparator and one for the Stop Comparator.

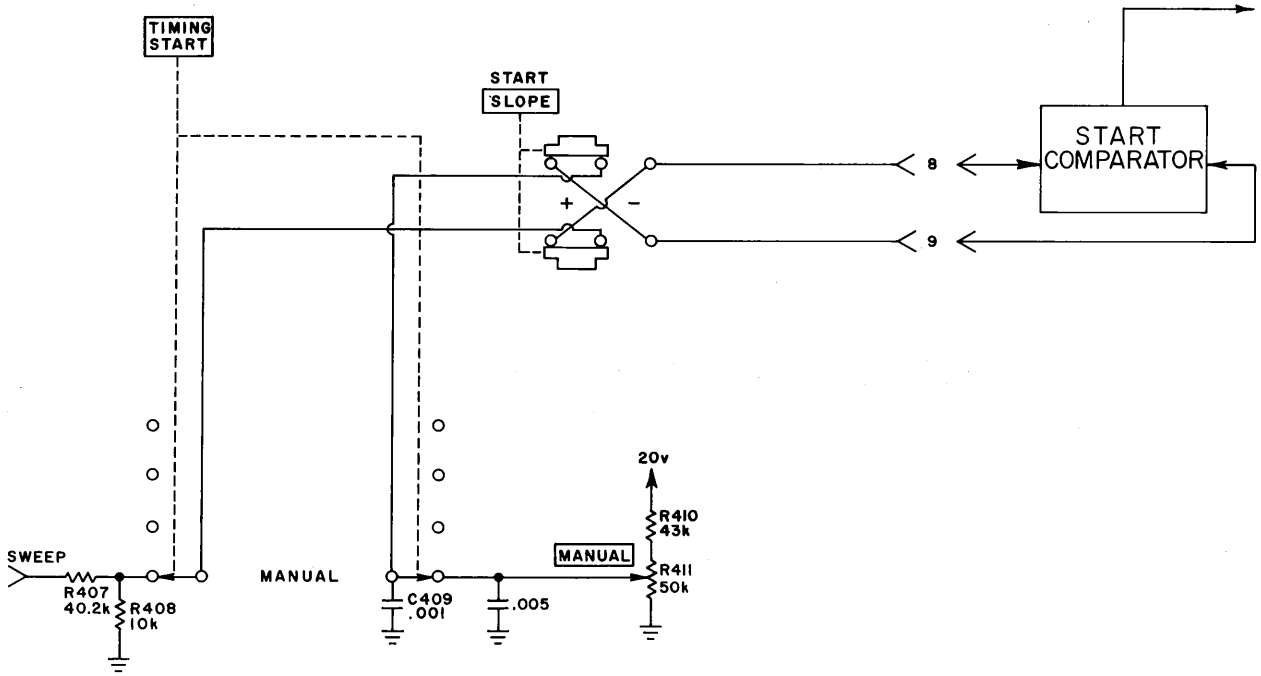
(1) 1/4% precision resistors comprise the divider to total 10.0k

(2) If the 100% zone was positioned at the top of the graticule and the 0% zone at the bottom, 0.8 ma would flow through the divider.

b. Sections of the TIME START and TIME STOP switches connect the divider to appropriate memories when the A or B vertical channel is selected.

c. The + position of the SLOPE switches connect the divider reference voltage to pin 9 of the comparator.

d. In operation, the TIME START switch would be used to select a percent of the voltage between the 0% zone and the 100% zone (perhaps 10%) and the TIME STOP switch would select a percent on its divider (perhaps 90%).



TYPE 6RIA SIGNAL COMPARATOR CARD
COMPARATOR SIGNAL - TIME, MANUAL

B-6RIA-0045
7-29-'64 dl

5. In the MANUAL position of the TIMING START (or TIMING STOP) switch, the Sweep Ramp from the 0% zone card is compared with a DC reference voltage from the MANUAL control.

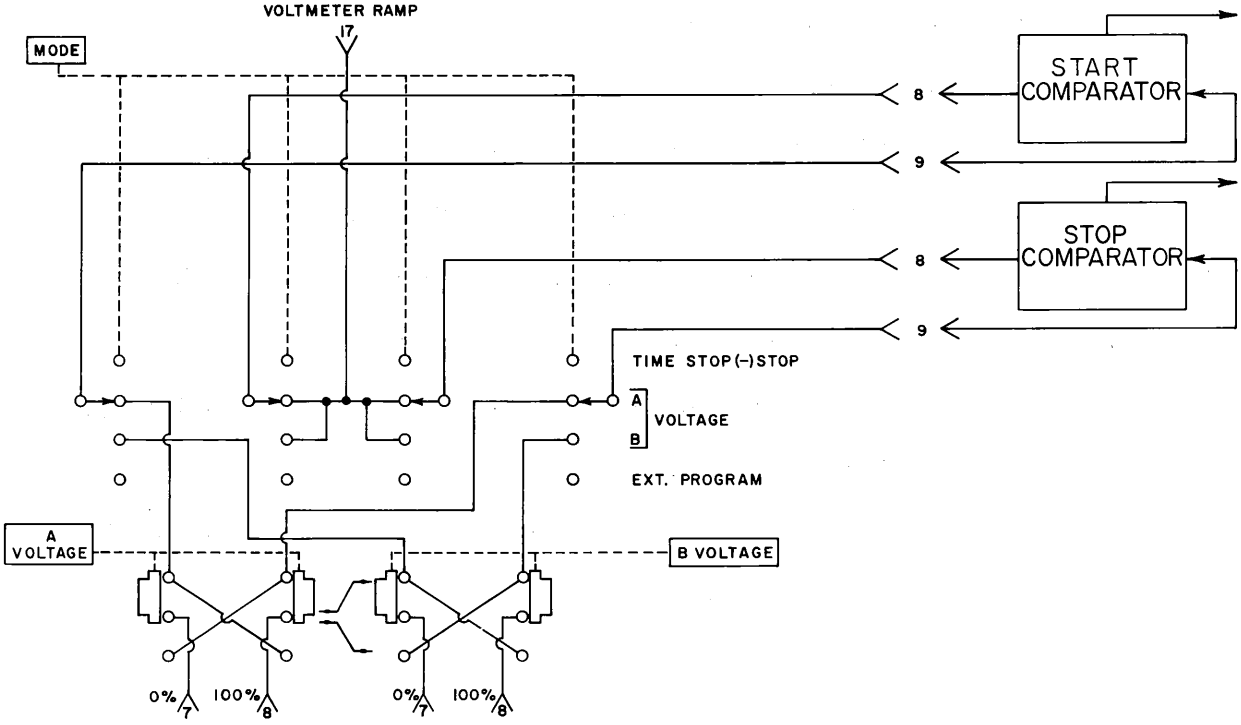
   a. The Sweep Ramp is a 50v positive going ramp (or staircase).

      (1) The ramp is attenuated by R407, R408 to 10v peak-to-peak -- 0v to 10v.

   b. The 50k MANUAL pot has a range of 10v.

   c. The MANUAL control should be used with + Slope and First Slope.

6. In the VOLTAGE position of the MODE switch, the Voltmeter Ramp, as the moving voltage, is compared with either the 0% memory or 100% memory.



TYPE 6RIA SIGNAL COMPARATOR CARD
COMPARATOR SIGNAL SOURCE – VOLTAGE

B-6RIA-0038
7-27-'64 dl

a. The Channel A or B selection is made by the MODE switch.

b. 0% and 100% memory selection is made by A or B VOLTAGE switch.

(1) The switch positions are labeled only by a sketch of a positive going step for 0% () or a negative going step for 100% memory () .

c. The moving signal (Voltmeter Ramp) is connected to pin 8 and the memories to pin 9.

(1) The SLOPE switches are not connected in the VOLTAGE modes.

d. In operation, the Voltmeter Ramp intersects one memory level to start count and the other memory to stop count.

G. Comparator, Q13, Q14, Q18

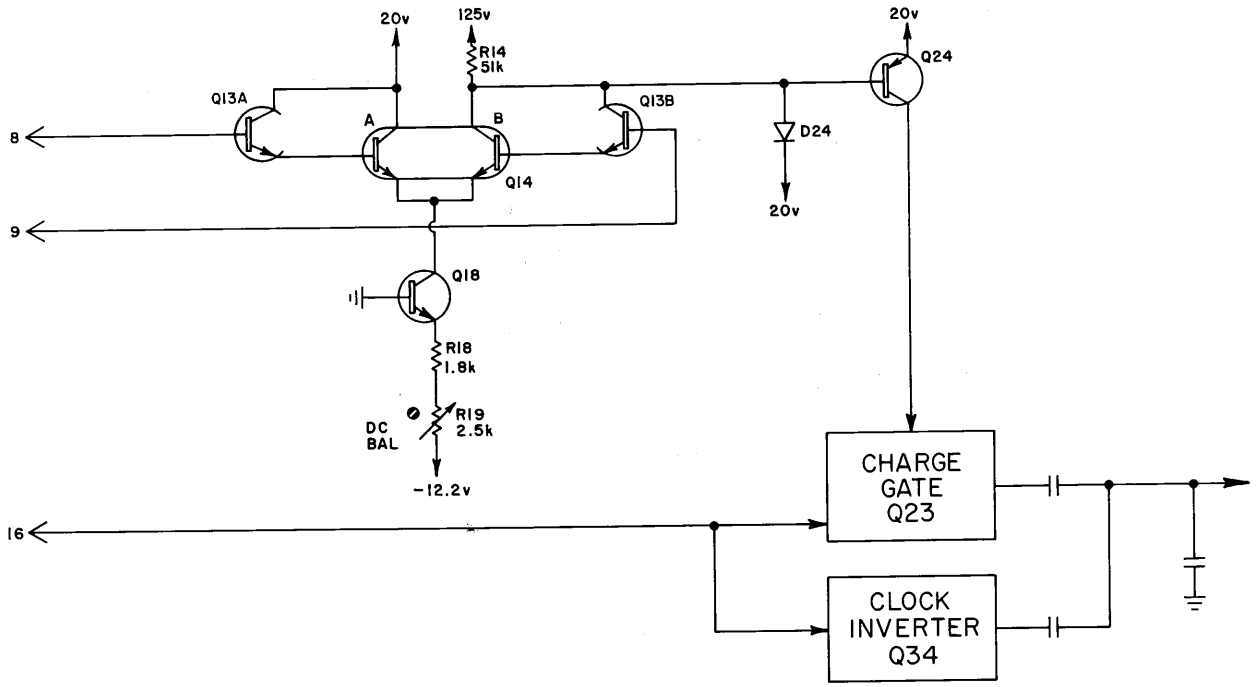
1. The function of the Comparator is to turn off Q24 when voltages on pins 8 and 9 have reached first coincidence, and turn on Q24 when the voltages have reached second coincidence.

a. To achieve first coincidence, a positive going moving voltage on pin 8 must pass through a reference voltage on pin 9 or a negative going signal on pin 9 must pass through the voltage on pin 8.

(1) This could be the first half cycle of a sine wave or complex waveform.

b. Second coincidence occurs when a negative going voltage on pin 8 passes through the reference voltage on pin 9 or when a positive going signal on pin 9 passes through the voltage level on pin 8.

(1) This could be the second half cycle of a sine wave, for example.



TYPE 6RIA SIGNAL COMPARATOR CARD
COMPARATOR AND CHARGE GATE INHIBITOR

B-6RIA-0039
7-31-'64 dl

2. The Comparator uses three transistors.
   a. Q13 and Q14 are 151-104 silicon NPN dual transistors selected from 2N2919's for BV_{EBO}.
   b. Q18 is a 151-103 silicon NPN transistor, relaxed selected from 2N2219.
3. Q13 and Q14 form a double Darlington comparator circuit.*
   a. Q18 provides a constant current long-tail emitter for the comparator.
4. With Q13A base (pin 8) and Q13B base (pin 9) at the same potential, 2 ma flows through Q14A and 2 ma through Q14B.
   a. R19, the DC BAL control, provides an adjustment to correct for transistor unbalance that might allow more or less than 2 ma to flow through Q14B.
   b. R19 is adjusted (with pins 8 and 9 strapped together) so that Q24 is just conducting.
      (1) At this point, circuit noise will begin to appear at Q24 collector.
      (2) 2 ma will flow through R14.
5. Q13 and Q14 each have a beta minimum of 100.
   a. The Darlington configuration provides a total minimum beta of 10,000 (100 x 100).
   b. Since 2 ma flows through each side of Q14, the maximum total base current flowing through the source impedance is about 200 nanoamp.
      (1) $\frac{2 \text{ ma}}{10{,}000} = 200$ nanoamp

* See Semiconductor Diodes and Transistors Program, Volume 4 - Circuit Analysis I.

c. Source impedance (to pins 8 and 9) is low in most cases.

(1) The memories have EF outputs.

(2) The worst case (highest source impedance) occurs in TIME mode, A or B Trace when a START or STOP VOLTAGE Helipot is in the center of its range.

(3) Source impedance from the 30k pot plus 10k START CAL pot is 7.5k to 10k.

(4) 10k x 200 nanoamp = 2 mv.

(5) The greatest error, then, from Comparator base current is 2 mv.

(6) Since vertical sensitivity is 1 v/div, the worst error is .2% at 1 division.

6. Quiescently, Q13A base (pin 8) is at a lower DC level than Q13B base (pin 9).

a. Q14A will be drawing less than 2 ma.

b. Q14B will draw more than 2 ma.

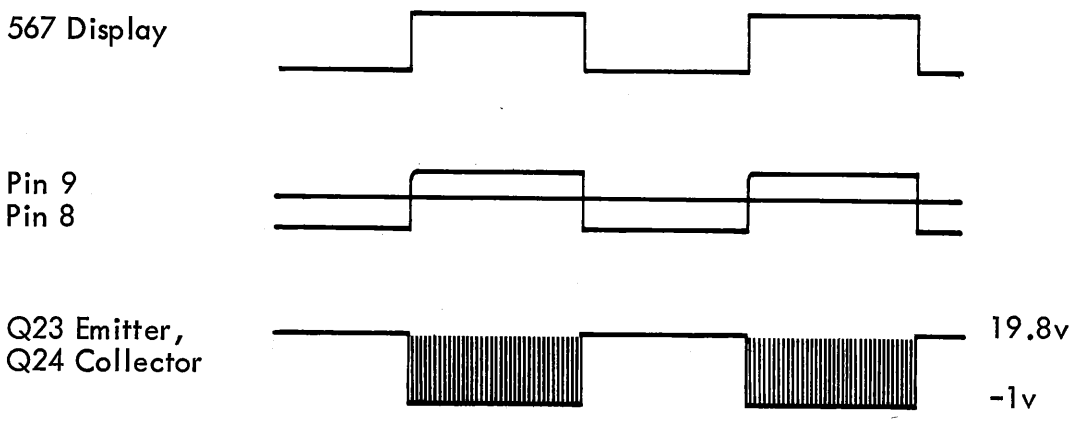
c. Q14B collector will be down.

d. Q24 will be saturated with its collector at 20v.

e. The Charge Gate Inhibitor is functioning and clock pulses cannot pass the Charge Gate.

7. As the positive going voltage on pin 8 reaches the level of the reference voltage on pin 9 (or a negative going voltage on pin 9 reaches the level of the reference voltage on pin 8), the currents through each side of the comparator equalizes at 2 ma.

a. As Q14B collector lifts Q24 base above 20v, the Charge Gate Inhibitor transistor (Q24) cuts off.



b. Q24 collector drops toward ground, opening the Charge Gate (Q23) allowing clock pulses to pass.

8. When second coincidence of the voltages on pins 8 and 9 occurs, and the comparator again swings through its balanced condition, Q14B collector will drop below 20v.

   a. Q24 will turn on.

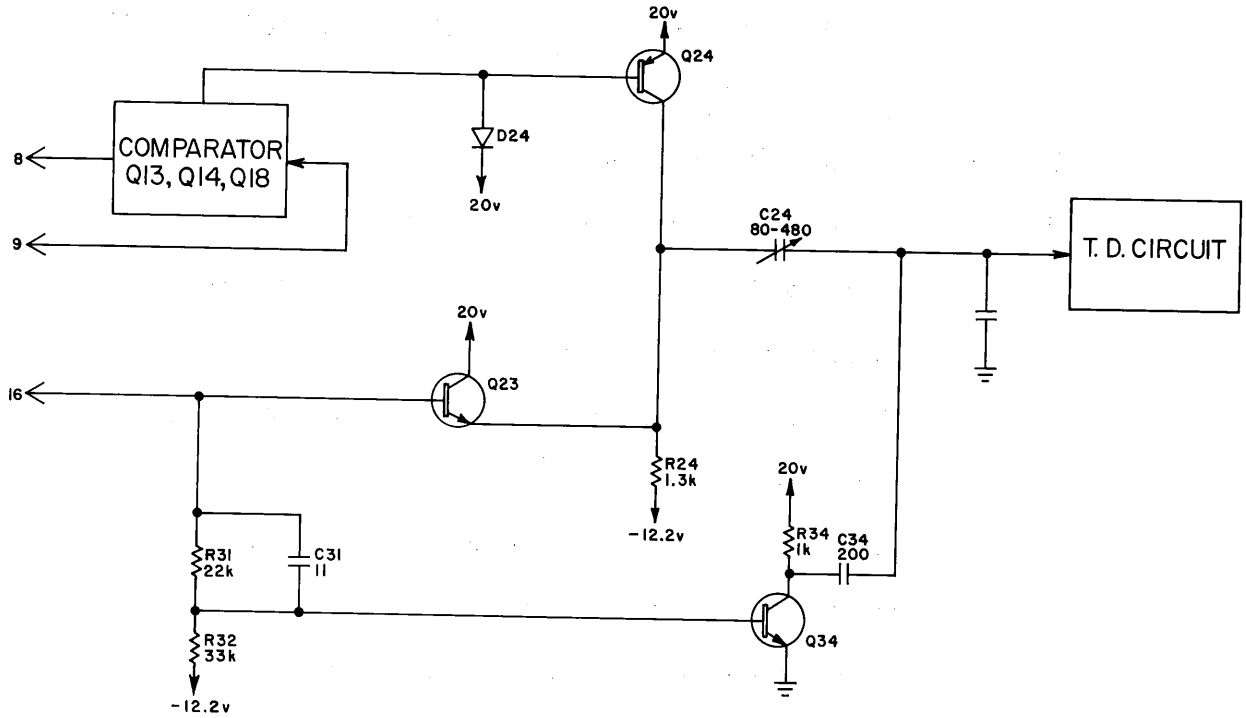
   b. As Q24 collector rises to 20v (saturated condition), the Charge Gate closes, stopping passage of Clock Pulses.

9. The cycle is complete; the circuit has returned to its quiescent state.

H. Charge Gate Inhibitor, Q24

1. Q24 operates as a switch whose purpose is to open and close the Charge Gate.
2. Q24 is a 151-054 germanium PNP transistor, selected from 2N2957 for BV_{CBO} and BV_{CEO}.
3. D24 is a 152-075 germanium diode.
4. At first coincidence of the voltages at pins 8 and 9, when the current through the "B" side of the comparator swings below 2 ma, the decreased current turns off Q24.
   a. D24 limits the base voltage rise to 20.3v, preventing Q24 base-emitter breakdown.
5. At second coincidence of the waveforms on pins 8 and 9, current through Q14B swings above 2 ma.
   a. The increased current turns on and saturates Q24.
6. When saturated, Q24 collector raises to about 19.8v and at cut-off swings from -1v to +18.5v with clock pulses through Q23.

1. Charge Gate and Clock Inverter



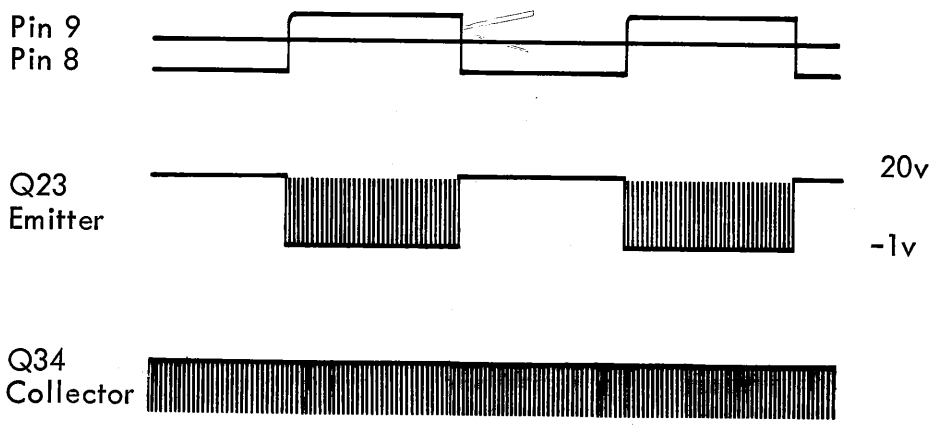
TYPE 6RIA SIGNAL COMPARATOR CARD
CHARGE GATE AND CLOCK INVERTER

B-6RIA-0040
8-3-'64 dl

1. The Charge Gate passes positive going clock pulses when gated on by Q24 and provides a low impedance charge path for C24.
2. The Clock Inverter inverts the clock pulses and provides a low impedance discharge path for C34.
3. Q23 is a 151-069 germanium 2N1304 NPN transistor.
4. Q34 is a 151-103 silicon NPN transistor relaxed selected from 2N2219.

5. In the quiescent state with Q24 conducting, Q23 emitter is pulled up to 20v, cutting off the transistor.
6. When Q24 turns off, Q23 emitter drops, biasing Q23 to conduction.
7. Clock pulses from the Voltmeter Card are fed via pin 16 to Q23 base.
    a. The pulses may be either Time Clock or Voltmeter Clock pulses depending on the mode switch setting.
    b. When Q23 is gated on the positive going clock, pulses pump charge into C24.
    c. Clock pulses on Q23 emitter swing from 0v to 20v.
8. When Q24 switches back on, Q23 emitter is pulled up to 20v turning it off.
9. Compensated divider, R31- R32, provides DC compatibility for the drive to Q34.
    a. The DC level is such that the clock pulses drive Q34 to cut off and saturation.
    b. Clock pulses are attenuated to about 6v at Q34 base -- still providing adequate drive.
        (1) Probe capacitance loading may make Voltmeter clock pulses appear to be attenuated more than time pulses.
        (2) Positive pulse excursion for both Time and Voltmeter Clock pulses is limited by Q34 base-emitter junction to .6v.
        (3) Negative excursion at Q34 base is limited by the attenuator.

10. Since Q34 switches from cut-off to saturation, the clock waveform drops Q34 collector from 20v to ground.

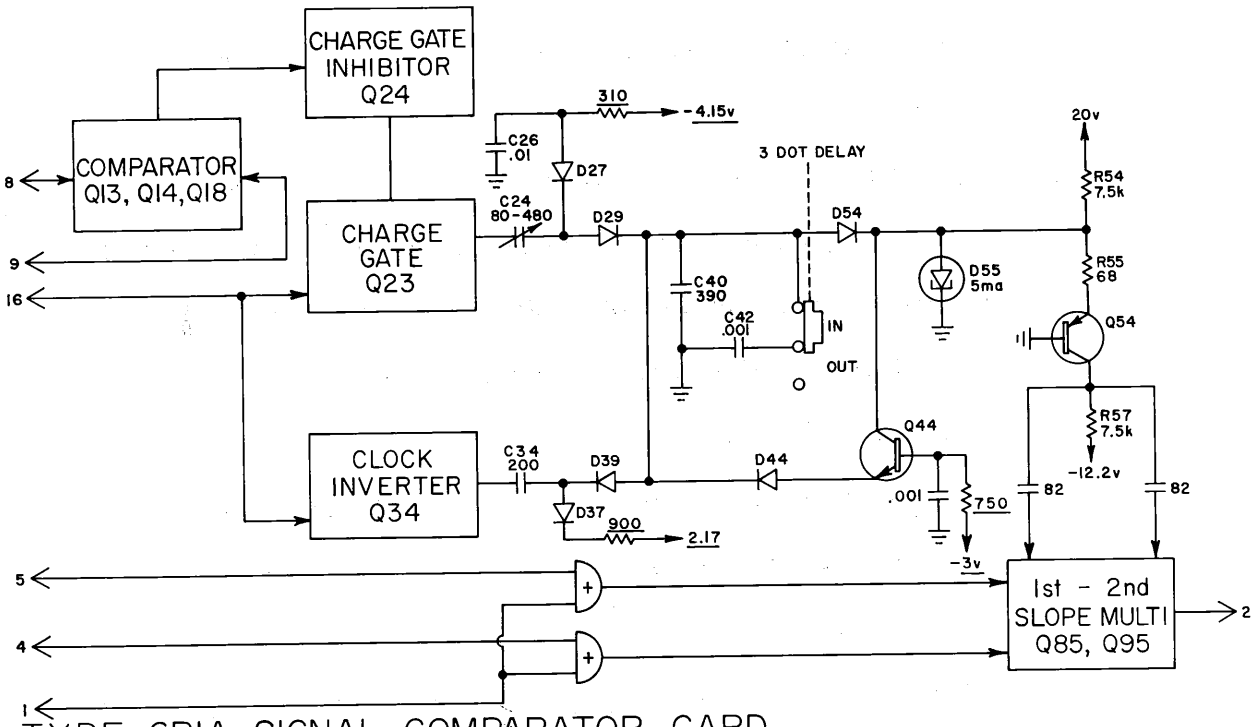


11. The output at Q23 emitter, therefore, is a train of 20v positive going clock pulses gated on by the Comparator.

12. The output at Q34 collector is a train of negative going 20v clock pulses that are <u>not</u> gated, but are present for all functions of the instrument (except perhaps a combination of MANUAL scan of a 3T77 and TIME mode of the 6R1A).

J. Tunnel Diode Circuit

1. The TD circuit provides a fast pulse trigger of uniform amplitude and duration to the first and second Slope Multi.



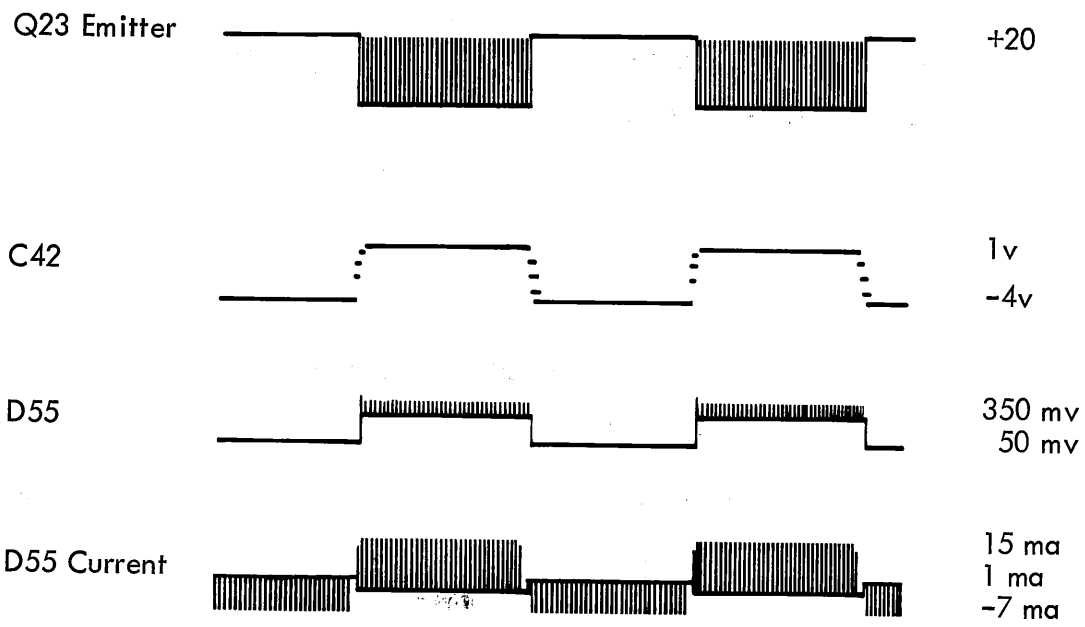
TYPE 6RIA SIGNAL COMPARATOR CARD
3-DOT DELAY AND T. D. CIRCUIT

B-6RIA-0041
8-4-'64 dl

2. The circuit includes a bucket and ladle circuit, called the 3 Dot Delay, the tunnel diode (D55), an output transistor (Q54), and a transistor (Q44) used to switch the TD to its low state when the circuit resets.

3. Q44 is a 151-103 silicon NPN transistor relaxed selected from 2N2219.

4. Q54 is a 151-1054 germanium PNP transistor, selected from 2N2957 for BV_{CBO} and BV_{CEO}.
5. D55 is a 5 ma tunnel diode, TD3, 152-093.
6. D29, D38, D39, D44 and D54 are 152-141, 1N3605 silicon diodes.
7. D27 and D37 are 152-075 germanium diodes.
8. A 3 DOT DELAY switch parallels C40 and C42 when the 3 DOT DELAY switch is IN.
   a. The switch will be considered IN for this discussion.
9. Quiescently (before coincidence of the voltages on pins 8 and 9), positive clock pulses are <u>not</u> passing the charge gate.
   a. Q34 is passing negative clock, however.
10. D55 is in its low state.
    a. Static TD current is 2.67 ma flowing through R54.
    b. The TD anode is at about 50 mv.



11. Negative clock pulses through C34 and D39 maintain a -4v charge on C40, C42.

12. With each positive going excursion of the negative clock pulses, D37 conducts establishing the charge on C34.

    a. About 5.2 ma is pulled through D37.

    b. D37 cathode ties to an equivalent 900Ω to 2.17v.

    c. When D37 conducts, its anode is pulled up to 7.2v by the current pulse.

13. When the negative going clock pulse swings negative, D37 cuts off and D39 conducts as the charge is removed from the 3 DOT DELAY cap, C42 (and C40).

    a. D39 cathode pulls down to -4.6v.

    b. Electrons are pumped into the C42, reducing the charge and dropping the DC level on the caps to -4v.

14. Between clock pulses, D44 is forward biased but not enough to supply emitter current for Q44.

    a. As a negative clock pulse arrives, D44 conducts heavily turning on Q44.

    b. A 10 ma current pulse is developed in Q44 that reverse biases D55 about 7 ma for the clock pulse duration.

15. With D55 anode at 50 mv, Q54 is cut off with its collector at -12v.

16. D29 and D27 are cut off with their junction at -4v.

17. When the Charge Gate (Q23) opens, positive going clock pulses pass through C24.

    a. C24 is usually set at about 400 pf.

    b. C24, therefore, has just twice the capacitance of C34.

18. The negative excursion of the positive going clock pulse brings D27 into conduction.

    a. About 17 ma of peak current is pulled out of C26 to charge C24.

19. The positive excursion of the clock pulse cuts off D27, lifts D29 into conduction, and dumps the charge into C42 (and C40).

    a. Electrons are pulled out of C42, increasing the positive charge on C42 and raising its DC level to +1v.

20. Negative clock pulses through C34 attempt to discharge C42 at the same time positive clock pulses through C24 attempt to charge C42.

    a. The voltage drop across C24 and C34 is about the same (14v) during the clock pulse duration.

    b. Since C34 has twice the capacitance as C24, the charge stored in C24 is twice as great as that in C34 (Q = CE).

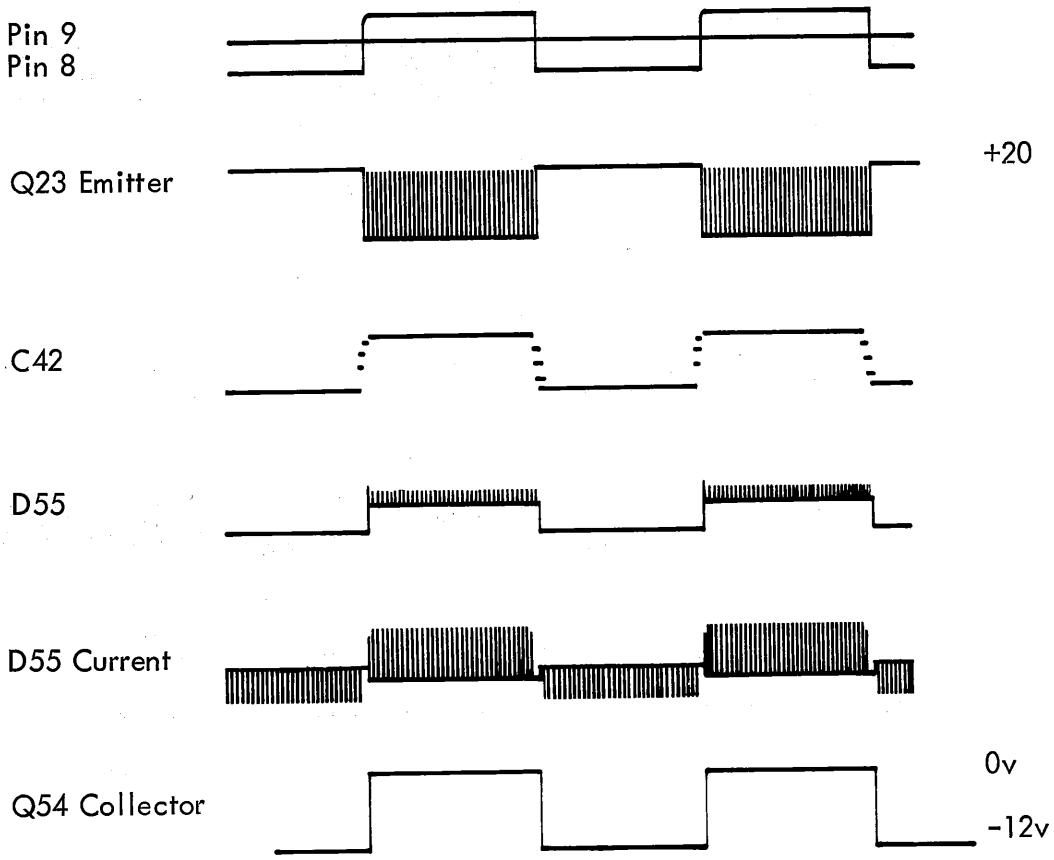
21. When C24 is properly adjusted, it takes 3 clock pulses to charge C42 from -4v to +50 mv.

    a. C24 may require adjustment when the 6R1A is used with a 3A2, depending on clock rates.

        (1) It is important that the START and STOP Comparators have the same delay.

    b. When the cap has reached 50 mv, D54 conducts with the next clock pulse.

c. The current contained in the clock pulse when added to the 2.67 ma of TD current, flips it to its high state.



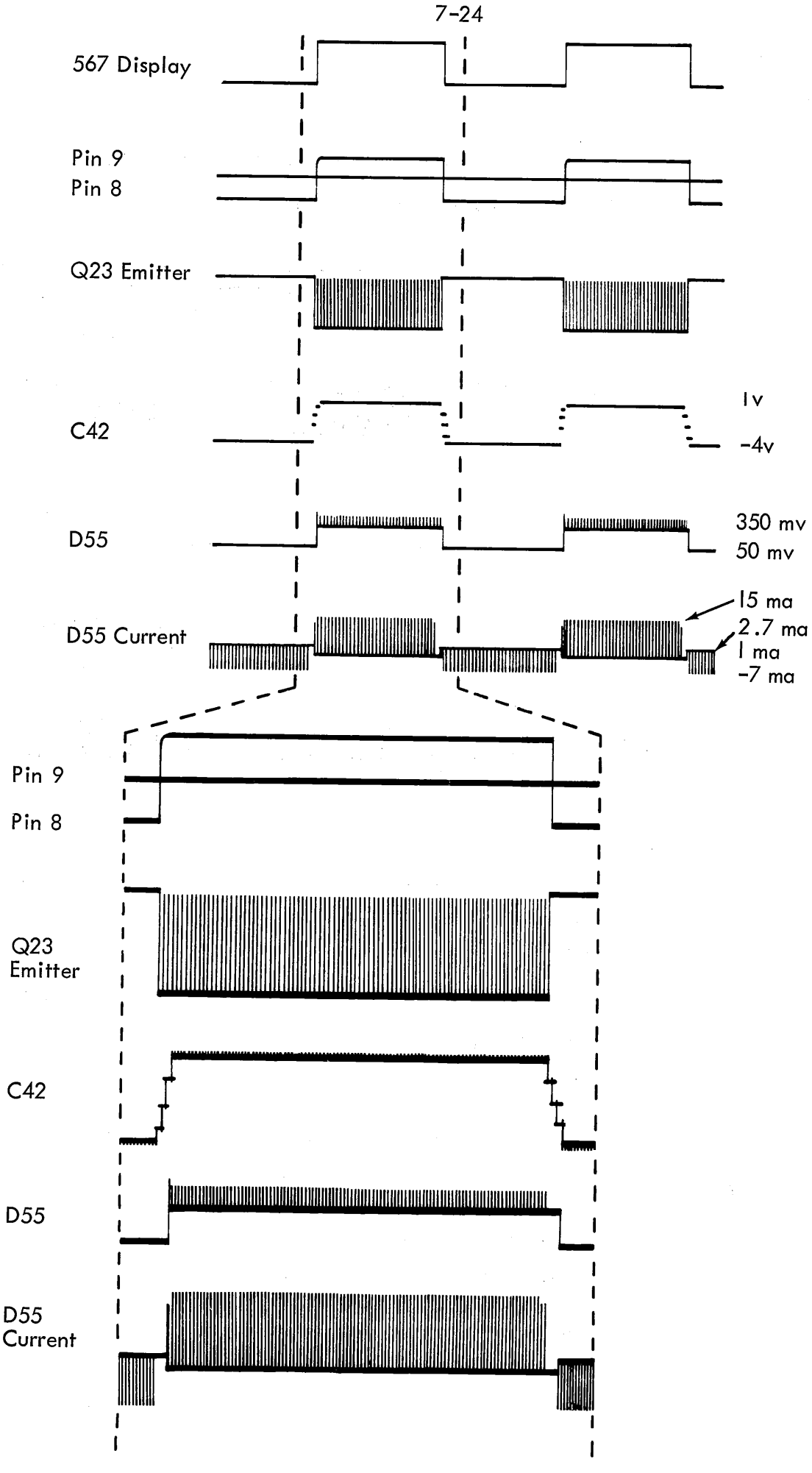
d. After the initial current pulse that flipped the TD to its high state (current pulse plus 2.67 ma must equal or exceed 5 ma), TD current drops to about 1 ma.

(1) Current through R57 and Q54 rob the TD of 1.6 ma.

22. As the level on C42 raises above -4v, D44 and Q44 cut off.

23. As clock pulses continue to arrive, D54 conducts pulling 15 ma current pulses through D55.

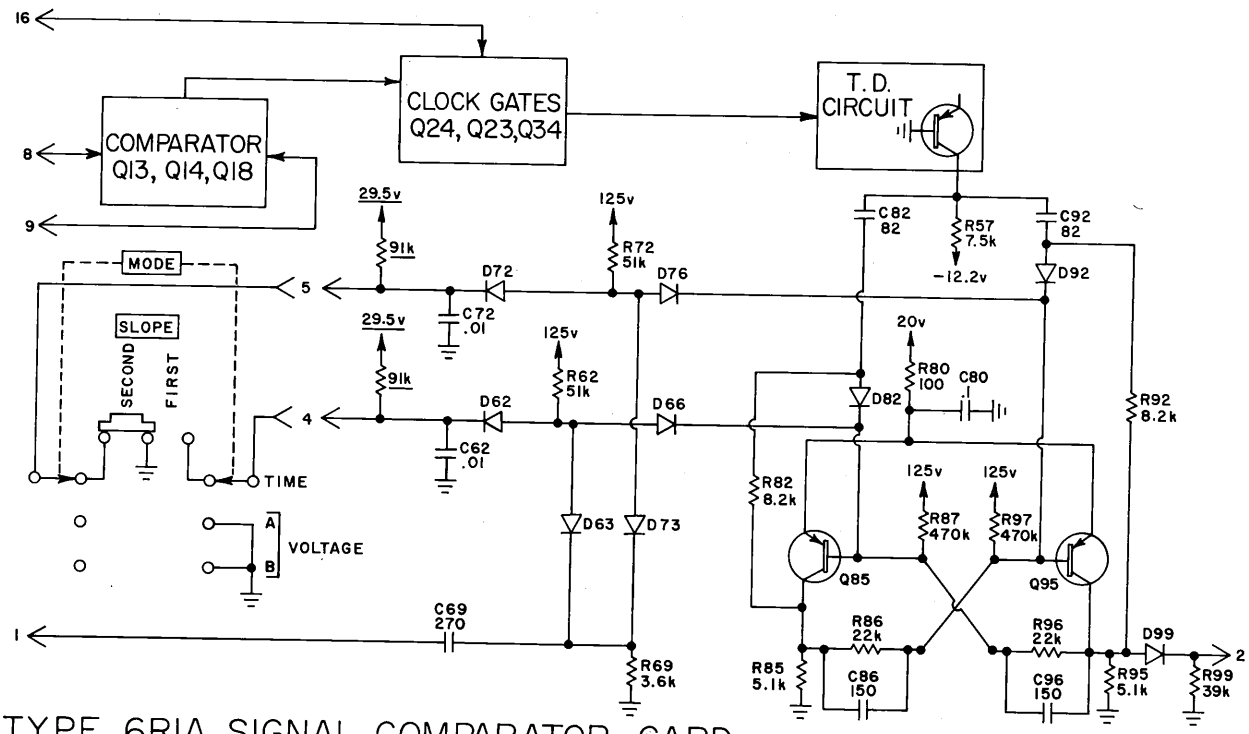
a. The TD is already in its high state so the current pulses have no effect.


567 Display
Pin 9
Pin 8
Q23 Emitter
C42
1v
-4v
D55
350 mv
50 mv
D55 Current
15 ma
2.7 ma
1 ma
-7 ma
Pin 9
Pin 8
Q23
Emitter
C42
D55
D55
Current

24. As the TD flips to its high state, the 350 mv step turns on Q54.
    a. Q54 saturates, with its collector pulling up to ground.
    b. A 12v positive step results that is coupled to the First-Second Slope Multi.
25. At second coincidence of the voltages on pins 8 and 9, the Charge Gate closes, stopping positive clock pulses.
    a. Negative pulses through C34 pump electrons into C42, discharging the cap.
    b. Three pulses are required to discharge C42 to -4v, bringing the level on D44 cathode to the point where the next pulse will turn on Q44.
    c. Current pulse through Q44 reverse biases the TD, flipping it to its low state.
    d. Q54 cuts off dropping its collector to -12v.
26. Since the First-Second Slope Multi is a 2:1 countdown device, the negative step at Q54 collector will not flip the Multi.
27. The TD circuit resets completing the cycle.

K. First-Second Slope Multi

1. The First-Second Slope Multi on the START Comparator Card supplies a positive going step to start count, and on the STOP Comparator Card supplies a positive step to stop count.



TYPE 6RIA SIGNAL COMPARATOR CARD
1st - 2nd SLOPE MULTI

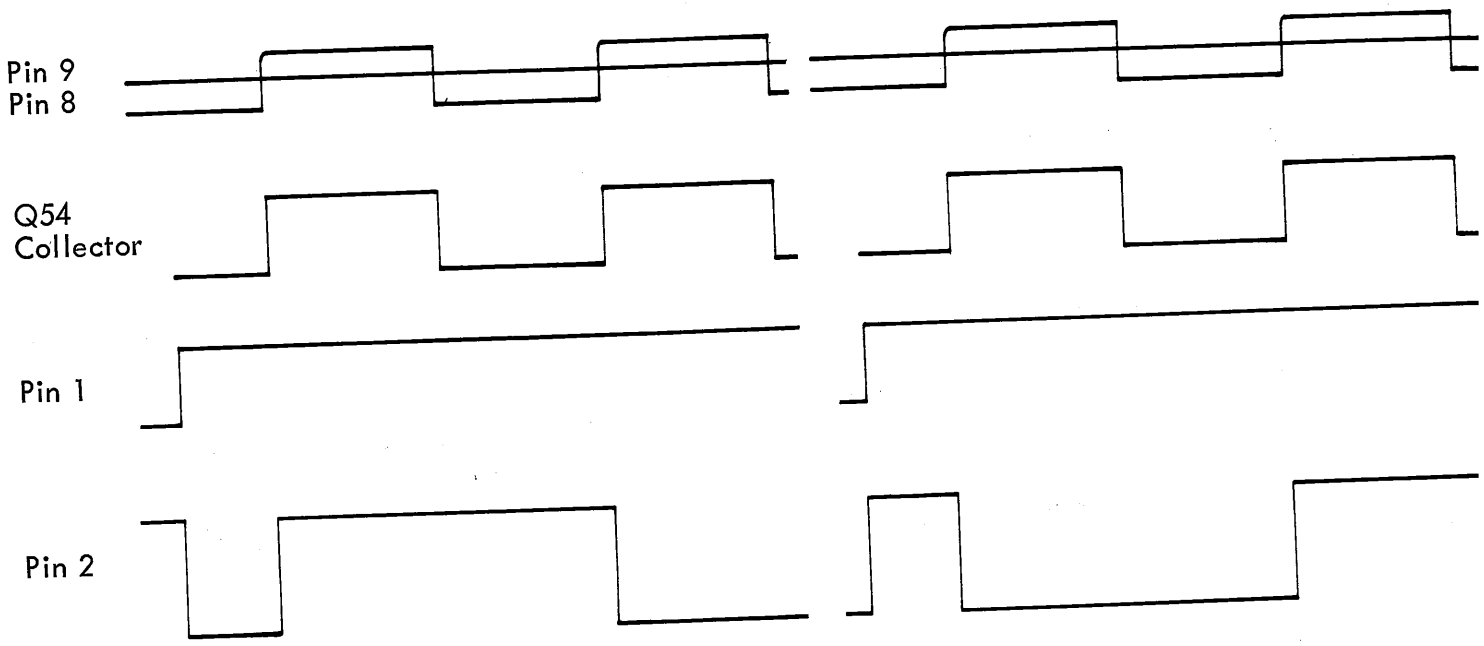
B-6RIA-0042
8-5-'64 dl

2. Logic circuits determine whether an output occurs (at pin 2) on the first or the second slope of the analog display.

a. An application would be a time measurement of a complete cycle of a square wave.

b. The START comparator would be set at 50%, + SLOPE, FIRST SLOPE.

c. The STOP Comparator would be set at 50%, + SLOPE, SECOND SLOPE.

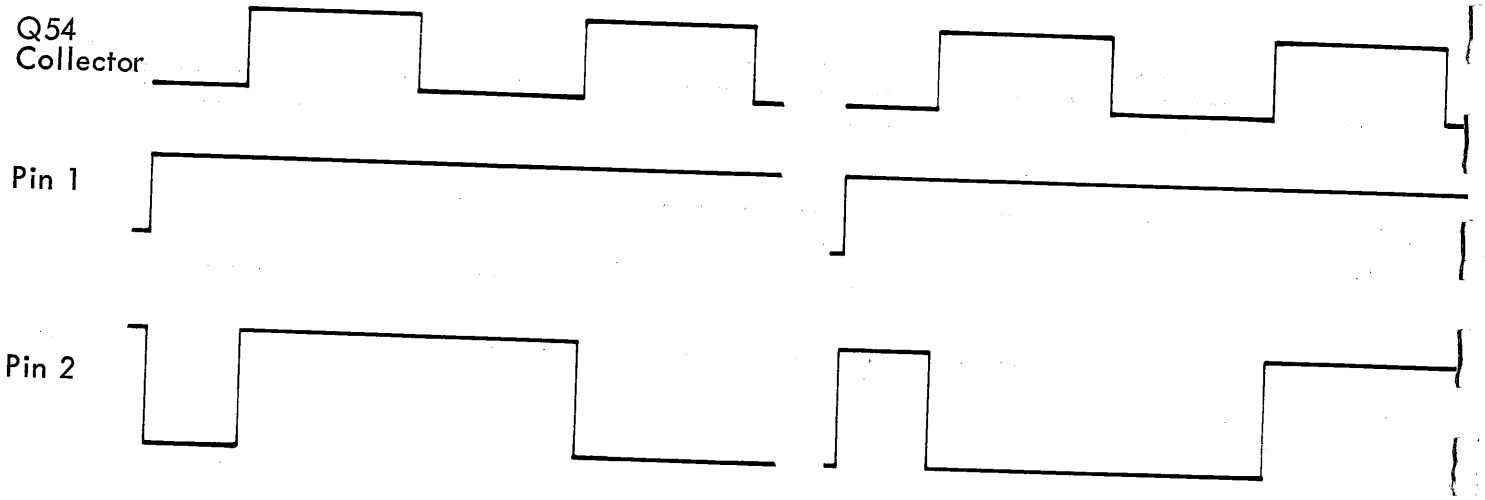


d. The START Comparator Card would have an output at the 50% point on the first positive slope on the display.

e. The STOP Comparator Card would have an output at the 50% point on the second positive slope on the display.

3. The + GATE at pin 1 presets the Multi at the start of sweep.

a. A ground at pin 4 or pin 5 determines which way the + GATE will preset the multi.



b. If pin 4 is grounded (by the MODE switch), the Gate will flip the multi at the start of sweep to a position where the first positive pulse out of the TD circuit will result in a positive step output at pin 2.

(1) If the Multi is already in the proper position at the start of sweep, the Gate will not affect the Multi.

c. If pin 5 is grounded (SECOND SLOPE GND), the Gate will preset the Multi so the first positive pulse out of the TD circuit will result in a negative output step (a positive step is required) and the second positive pulse will result in a positive output.

4. The First-Second Slope Multi is a transistorized Eccles-Jordan bistable multi.

   a. Q85 and Q95 are 151-054 germanium PNP transistors selected from 2N2957 for BV_{CBO} and BV_{CEO}.

5. Nine germanium diodes are used in the multi and logic circuits, all of which are 152-075's.

6. Assume a condition where two cycles of square wave are being displayed, pin 4 (START Comparator Card) is at ground, and the time is just prior to sweep.

   a. Assume Q95 is conducting (saturated):

      (1) Base, 19.4v.

      (2) Collector, 19.4v.

      (3) Emitter, 19.4v.

   b. Q85 is cut off.

      (1) Base, 23.8v.

      (2) Collector, 3.3v.

      (3) Emitter, 19.4v.

   c. With pin 4 at ground, D62 is conducting with about 2.5 ma flowing through R62.

   d. D63 and D66 are cut off.

   e. With pin 5 open, D72 is cut off.

      (1) The cathode returns through 91k to 29.5v.

   f. D73 is conducting.

      (1) A divider composed of R69, D73, and R72 to 125v places D73 anode at 8.2v.

      (2) 2.3 ma flows through D73.

g. D76 is cut off.

(1) The divider holds D76 anode at 8v and conducting Q95 places the diode cathode at 19.4v.

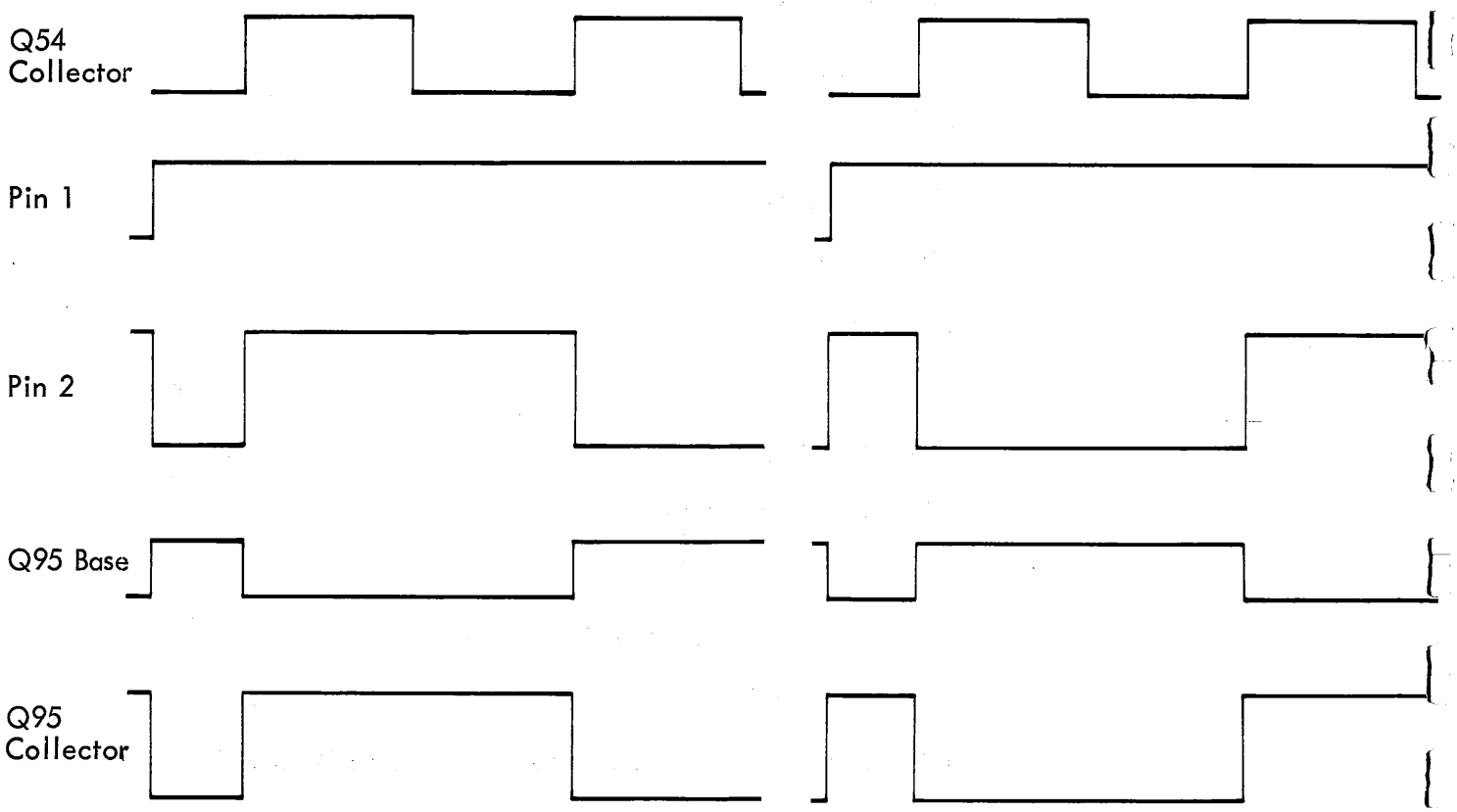
h. D82, a steering diode, is cut off.

(1) Anode at 3.3v.

(2) Cathode at 23.8v.

i. D92, the other steering diode, is zero biased (or possibly .1v forward biased) with its cathode and anode at 19.4v.

7. At the start of sweep (actually delayed about 5 mm in the 0% Zone Card), a 20v + GATE arrives at pin 1.



a. The step is differentiated by C69, R69 to a fast 18v pulse.

(1) A 5 ma current pulse is pulled through R69.

b. The pulse cuts off D73.

c. Robbed of its current, the bottom of R72 rises toward 125v to be caught by D76 at 19.4v.

d. As D76 conducts, it pulls up on Q94 base.

(1) After the initial pulse, the base rests at 24v set by the cross-coupling divider.

e. Through multi action, Q95 cuts off and Q85 conducts.

f. A negative step appears at pin 2 as Q95 collector drops to 3.3v.

(1) A negative step does not affect the Master Gate.

(2) A positive step is required.

g. D92 is cut off.

h. D82 is on the verge ot conduction with both anode and cathode at 19.4v.

i. The Multi is now preset so that when the TD circuit output swings positive, the multi will have a positive output.

8. On the first positive slope on the display when the voltages on pins 8 and 9 reach first coincidence, the TD circuit output has a 12v positive step.

a. As the step pulls current through C82, D82 conducts. (D92 is reverse biased by about 20v.)

b. Q85 base pulls up and the multi flips.

c. Q85 turns off and Q95 saturates.

d. Q95 collector pulls up to 19.4v producing the START pulse for the Master Gate.

e. The first slope has produced an output.

9. At second coincidence, the TD flips back producing a negative step at its output.

a. A negative step cannot affect the Multi as both steering diodes are cut off.

10. On the second positive slope on the display as the TD flips, a positive step again appears at its output.

a. Since the steering diode on the conducting side of the multi will be in its ready state (no voltage across it), D92 will conduct.

b. Q95 cuts off as the Multi flips.

c. A negative output appears at pin 2.

11. It requires two complete cycles of display for one cycle of the Multi.

12. During retrace, vertical information may send a signal from the TD to again flip the Multi.

a. Logic levels in the Master Gate prevent this positive output from affecting the Master Gate circuits, however.

13. If just one cycle is being displayed (no second slope to reset the Multi), the + Gate will reset it. No matter what the display, the + Gate will preset the Multi, if necessary.

14. Consider a condition when two cycles are being displayed and pin 5 is grounded (Second Slope Gnd), just prior to sweep.

    a. D72 will conduct, cutting off D73 and D76.

    b. D62 will be cut off.

    c. D63 and D66 will be conducting.

    d. At the start of + Gate, the positive pulse will cut off D63.

    e. The bottom of R62 rises, pulling up on D66 and Q85 base.

    f. The multi flips (Q95 conducting, Q85 cut off) and a positive step appears at its output.

        (1) Master Gate logic levels prevent this step from affecting the Master Gate circuit.

    g. At First slope, the TD has a positive output which flips the multi (Q95 cut off, Q85 conducting).

        (1) A negative output appears at pin 2.

    h. At the second positive slope on the display, the TD again has a positive output.

    i. Passing through C82, the TD output pulls up on the base of conducting Q85 and the multi flips.

        (1) The output is the desired positive step to be fed via pin 2 to the Master Gate.

15. D99 prevents any noise from the Master Gate from tripping the First-Second Slope Multi.

TYPE 6R1A

VIII. VOLTMETER CARD

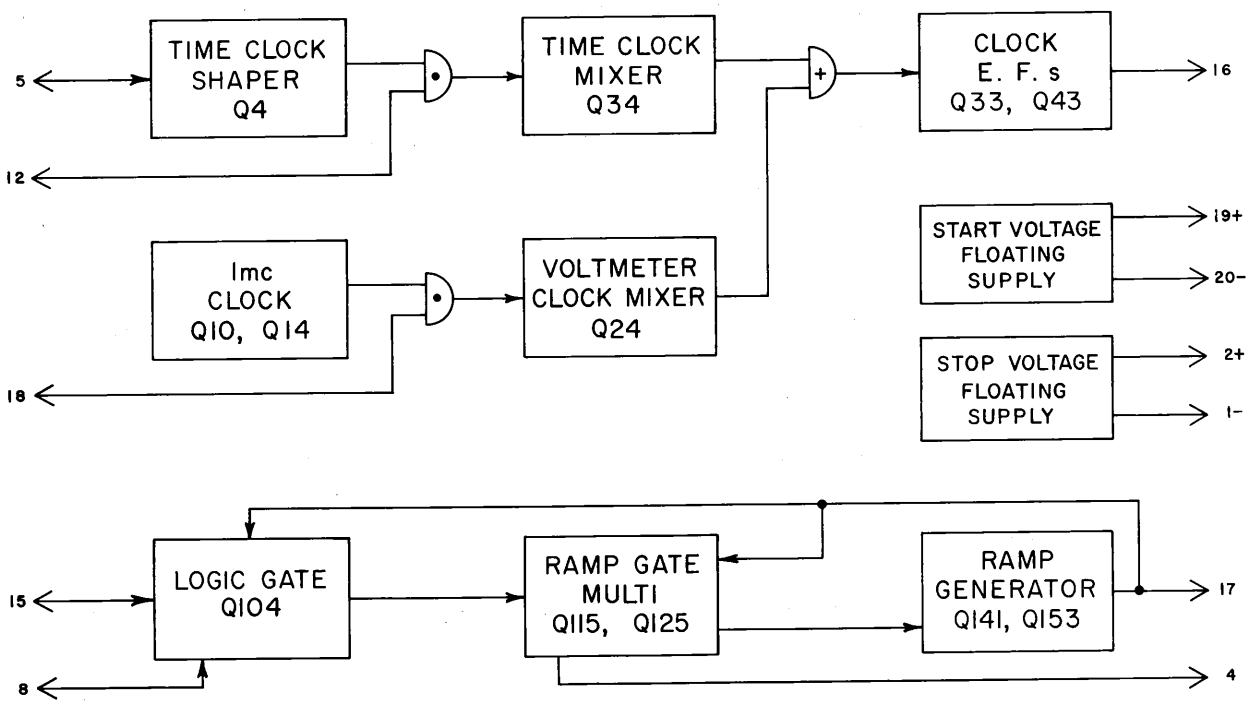
A. The Voltmeter Card contains three unrelated circuits.

1. Time and Voltmeter Clock circuits:

a. A 1 mc crystal controlled oscillator generates the Voltmeter Clock pulses.

b. Clock pulses from the time base plug-in are shaped and amplified.

c. Either the time clock pulses or the Voltmeter Clock pulses are fed (via pin 16) to the Signal comparator and Master Gate circuits.



TYPE 6RIA VOLTMETER CARD BLOCK DIAGRAM

B-6RIA-0020
7-15-'64 dl

2. Ramp Generator circuit:

   a. The circuit generates an 18v positive going ramp for use in the Signal Comparator.

   b. A negative going gate is generated for use in the Master Gate.

3. Two floating power supplies provide 10v voltage sources for the START and STOP voltage helipots.

B. Inputs

1. Clock circuit inputs:

   a. Clock pulses from the time base plug-in through pin 5 -- about 1.5v peak-to-peak.

   b. Pin 12 is grounded by the mode switch to open the Time Clock logic gate.

   c. Pin 18 is grounded by the mode switch to open the Voltmeter Clock logic gate.

2. Voltmeter Ramp inputs:

   a. Pin 8 carries the 20v positive going + gate from the 0% zone card.

   b. Pin 15 has the 20v Print Command pulse from the Master Gate.

C. Outputs

1. Pin 16 has the 20v clock pulse -- either Time Clock or Voltmeter Clock pulses.

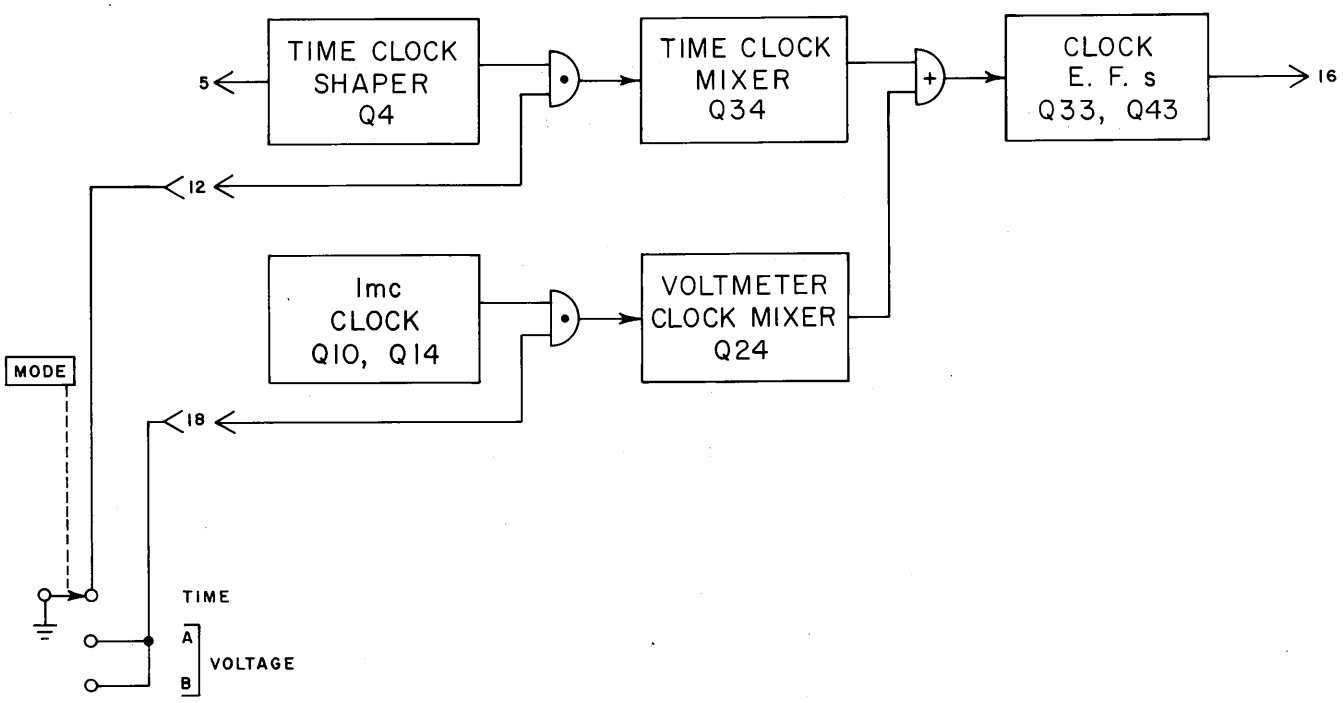
2. Pin 17 carries the 17v positive going Voltmeter Ramp.

   a. The ramp has a slope of 1v per 100 clock pulses (1v/100 μsec).

3. Pins 19 and 20 are separated by exactly 10v (pin 19 is positive) to supply the START VOLTAGE for the START helipot.

4. Pins 1 and 2 are also separated by exactly 10v (pin 2 is positive) to supply the STOP VOLTAGE for the STOP helipot.

D. Clock Circuits



TYPE 6RIA VOLTMETER CARD
CLOCK BLOCK DIAGRAM

B-6RIA-0021
7-15-'64 dl

1. The clock circuits are made of the following blocks:

   a. Time Clock Shaper, Q4.

   b. Time Clock Mixer, Q34.

c. 1 mc Clock, Q10 and Q14.

d. Voltmeter Clock Mixer, Q24.

e. Clock EF's, Q33 and Q43.

2. Q4, Q14 and Q33 are 151-103, 2N2219 silicon NPN transistors.

3. Q24, Q34 and Q43 are 151-054 germanium PNP switching transistors.

4. Q10 is a 151-069, 2N1304 germanium NPN transistor.

5. D4, D14, D24 and D34 are 152-075 germanium diodes.

6. System Logic:

a. A 1 mc oscillator (Q10) generates the Voltmeter Clock pulses.

b. System logic determines whether the Voltmeter Clock or the Time Clock pulses appear on pin 16.

c. R6, R31 and Q34 form a negative NAND or a positive NOR gate.

d. In the TIME position of the mode switch, pin 12 is grounded.

e. When pin 12 is at ground AND pin 5 receives clock pulses there is an output at Q34 collector.

f. Or one can say that when pin 12 is at ground, Time Clock pulses can pass Q34.

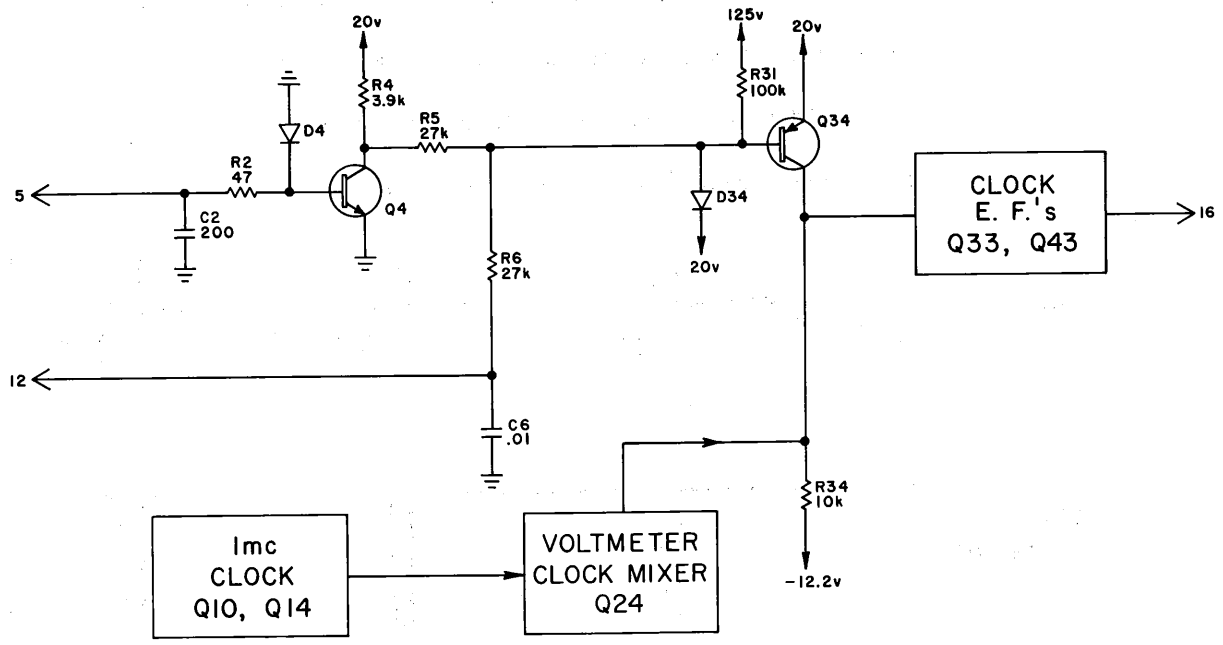
g. An identical logic gate is formed from R16, R21 and Q24.

h. When pin 18 is at ground (VOLTAGE position of the mode switch), Voltmeter Clock pulses can pass Q24.

i. Q24 and Q34 collectors are connected in parallel and tied to the bases of the clock EF's.

j. Either Q24 or Q34, then, delivers clock pulses to the output.

E. Time Clock Circuits



TYPE 6RIA VOLTMETER CARD
TIME CLOCK CIRCUIT

B-6RIA-0022
7-16-'64 dl

1. The Time Clock pulses on pin 5 come from the Time Base plug-in.

   a. From the 3T77 the pulses are 1.3v peak-to-peak (-.5v to +.8v).

   b. The negative excursion is limited by D4 to -.3v on Q4 base.

2. R2, C2 slow the pulse rise and fall time.

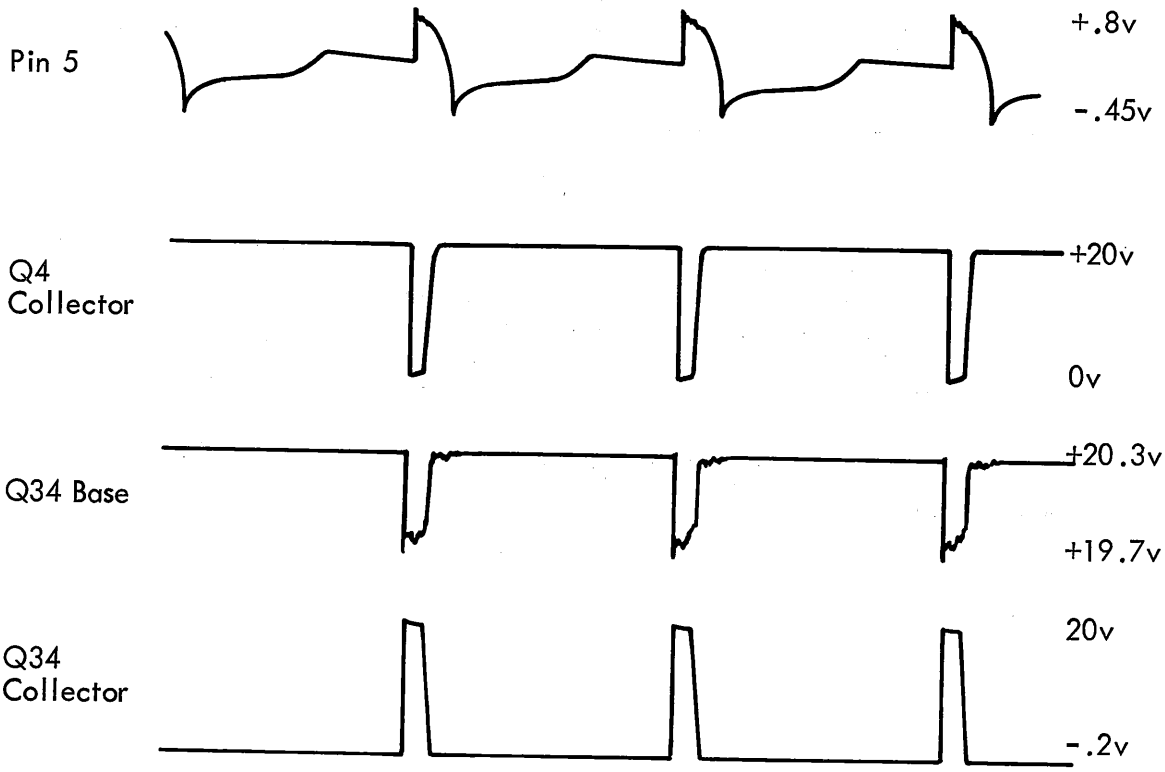
   a. After shaping and amplification the clock pulse is 20v peak-to-peak.

   b. Reducing rise and fall time reduces radiation to other circuits.

3. Q4 amplifies and shapes the Time Clock pulses.

   a. Q4 switches from cut-off to saturation.

   b. The output swings from 20v to ground.



4. When pin 12 is not grounded, D34 is conducting -- Q34 is cut off.

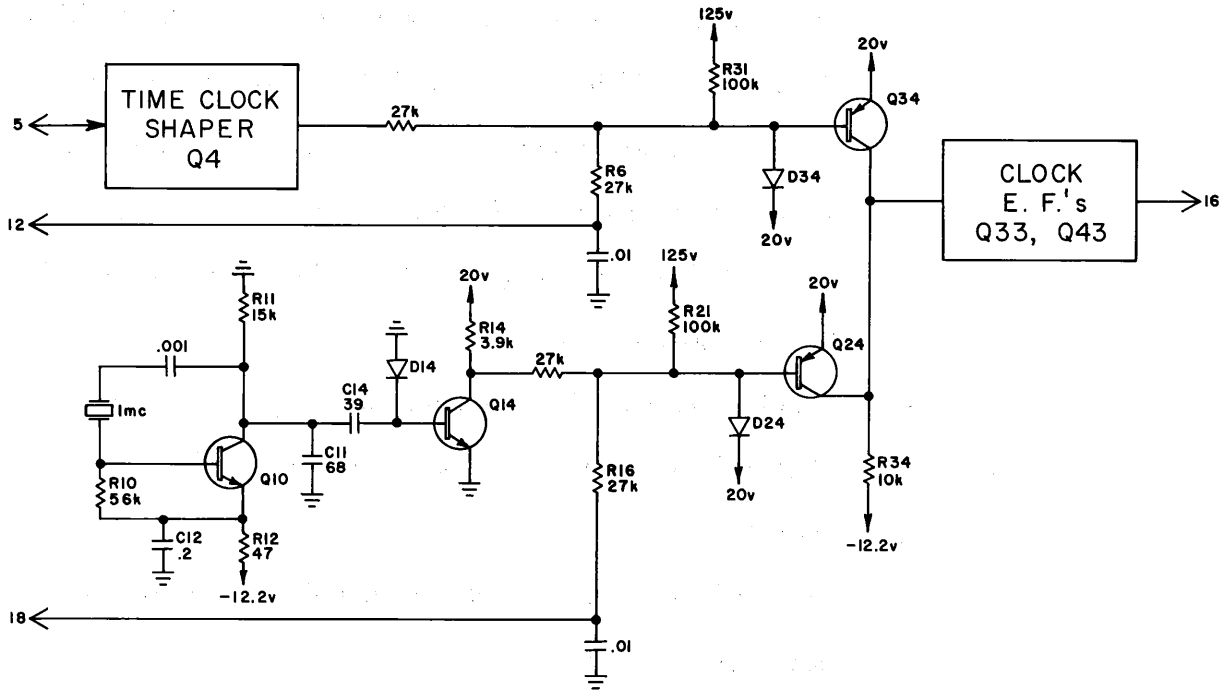
   a. When Q4 collector is at 20v, 1.05 ma flows through D34 and R31.

   b. When Q4 collector is at 0v, .75 ma flows through R5 and .3 ma through D34.

   c. With D34 anode and Q34 base at 20.3v, Q34 is cut off.

5. When pin 12 is grounded, D34 will cut off as the clock pulses pull Q4 collector to 0v.
   a. When Q4 is cut off and its collector is at 20v, about .75 ma flows through R6 leaving .3 ma to keep D34 conducting.
   b. When Q4 collector drops to 0v, .75 ma flows through both R5 and R6 robbing D34 of current -- the diode cuts off.
   c. Of the 1.5 ma through R5 and R6, 1.05 ma flows through R31; the rest turns on Q34.
   d. Q34 base is limited by the base-emitter junction at 19.7v.
6. Q34 switches from cut off to saturation to form the 20v clock pulses at its collector.
   a. Q34 collector is prevented from dropping below ground by Q43 base-collector junction.
7. C6 prevents radiated clock pulses from appearing on the Time Clock ground bus.

F. Voltmeter Clock

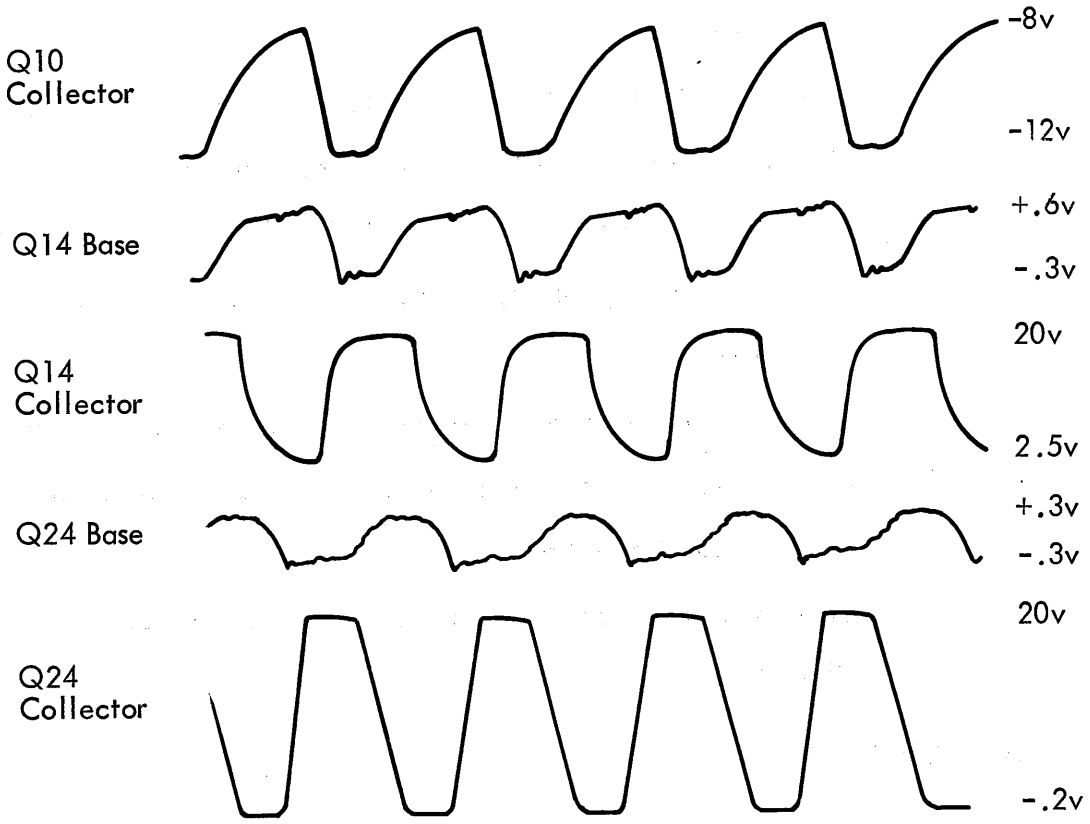


TYPE 6RIA VOLTMETER CARD
Imc VOLTMETER CLOCK

B-6RIA-0023
7-17-'64 dl A

1. The source of the Voltmeter Clock pulses is a 1 mc crystal controlled oscillator (Q10).
2. The oscillator is a transistorized Pierce.
   a. C11 and stray base to emitter capacitance form the phase shift divider.
   b. The crystal is a 1 mc Type H 17 with a ±.01% tolerance.

3. The output waveform on Q10 collector swings from -8v to -12v.



4. The bottom of the waveform is clamped at -.3 by D14, thereby establishing a starting reference for each cycle.

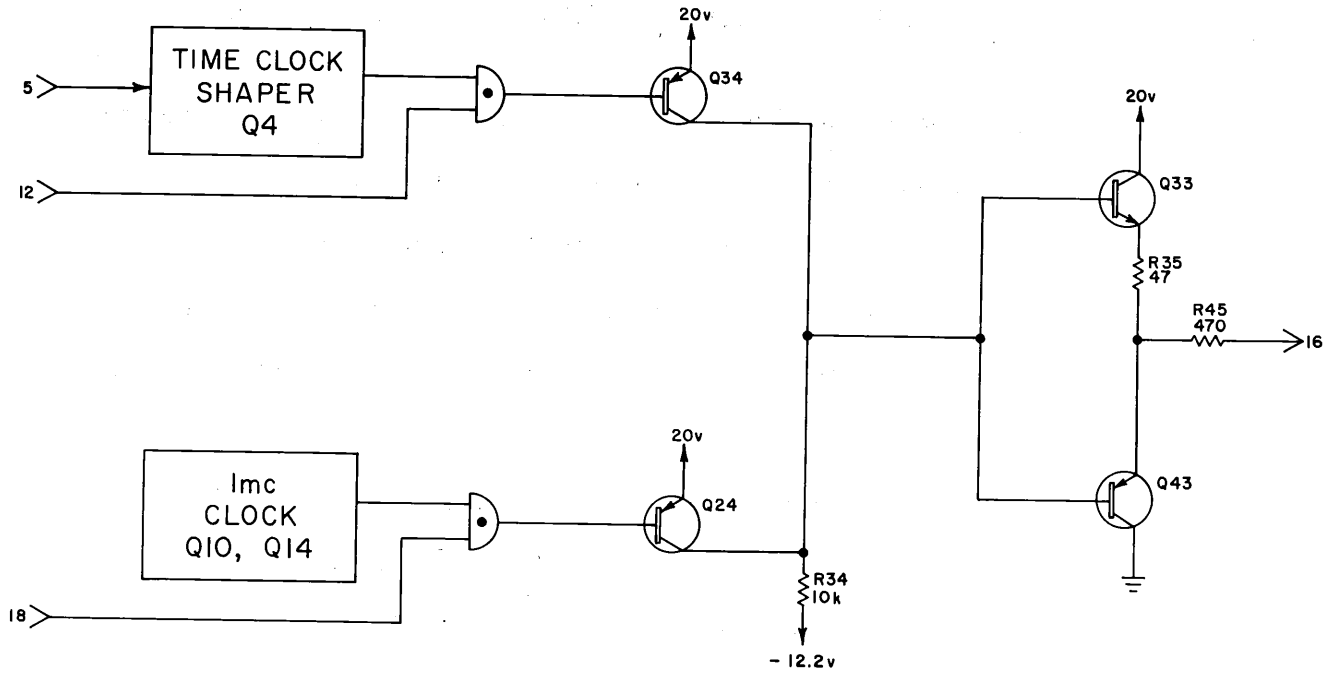
   a. Without the diode, Q14 base-emitter junction would clamp the top of the oscillator waveform at .6v with the balance of the 4v swing driving the base uselessly beyond cut-off.

   b. With the negative peak clamped at -.3v by D14, the oscillator output drives Q14 to saturation.

   c. The base waveform, then, swings from -.3v (cutting Q14 off) to +.6v where it is limited by Q14 base-emitter junction (Q14 saturated).

5. R12, C12 decouples the power supply bus from the oscillator.
6. The output waveform at Q14 collector swings from .3v (saturation) to 20v (cut-off).
7. Circuit configuration from Q14 collector through Q24 to the Clock EF's is identical to that in the Time Clock circuit.
   a. The circuit is gated to pass clock pulses when pin 18 is tied to ground by turning the mode switch to a VOLTAGE position.
   b. Stored charge in Q14 delays the clock pulses about 150 nsec.
8. Q24 further shapes the clock pulse to a 0v to 20v pulse with nearly equal rise and fall times.
9. Q24 collector (in parallel with Q34 collector) is tied to the Clock EF's.

G. Clock EF's

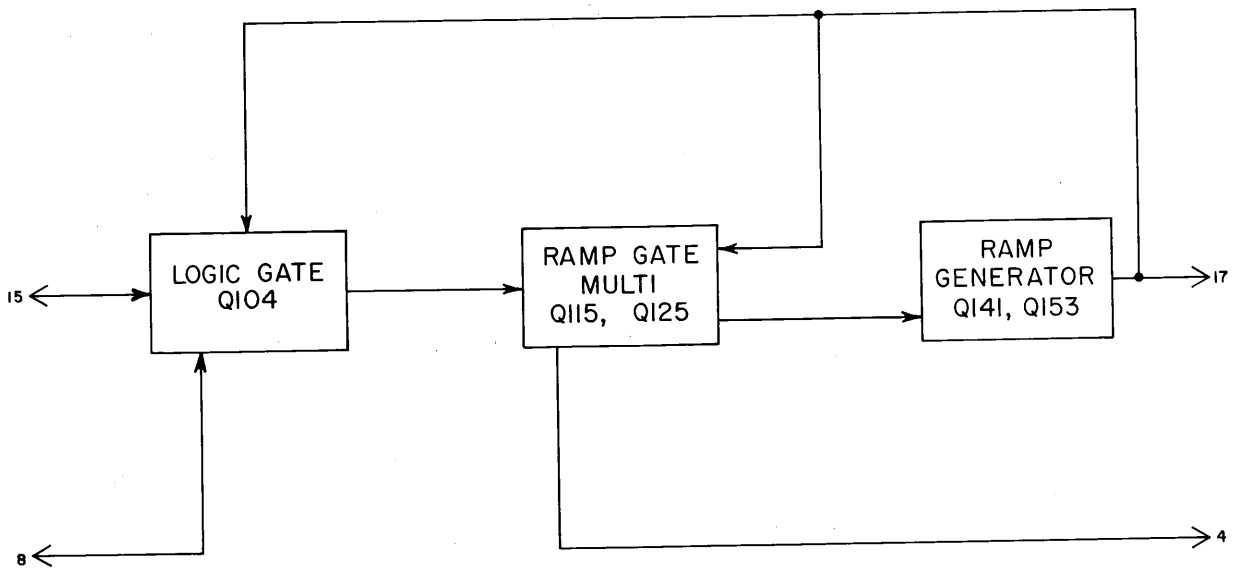


TYPE 6RIA VOLTMETER CARD
CLOCK E. F.'S

B-6RIA-0029
7-22-'64 dl

1. The Clock EF's and their connection to Q34 and Q24 can be considered an OR circuit.
   a. Since the mode switch can select only one clock source at a time, the EF's receive and pass on either the Time Clock pulses OR the Voltmeter Clock pulses.
2. The EF's provide a low impedance drive for the socket capacitance and input capacitance in the Comparator and Master Gate cards.
3. The NPN, PNP complimentary pair provides equal rise and fall time to the clock pulses.
   a. A PNP EF has good fall time while a NPN EF has good rise time.
   b. The Voltmeter Clock waveform on one sample instrument had a risetime of 30 nsec and a fall time of 35 nsec.
4. R45 together with stray C and input C slows the rise and fall time to reduce radiation from the 20v clock pulses.

H. Voltmeter Ramp Circuits

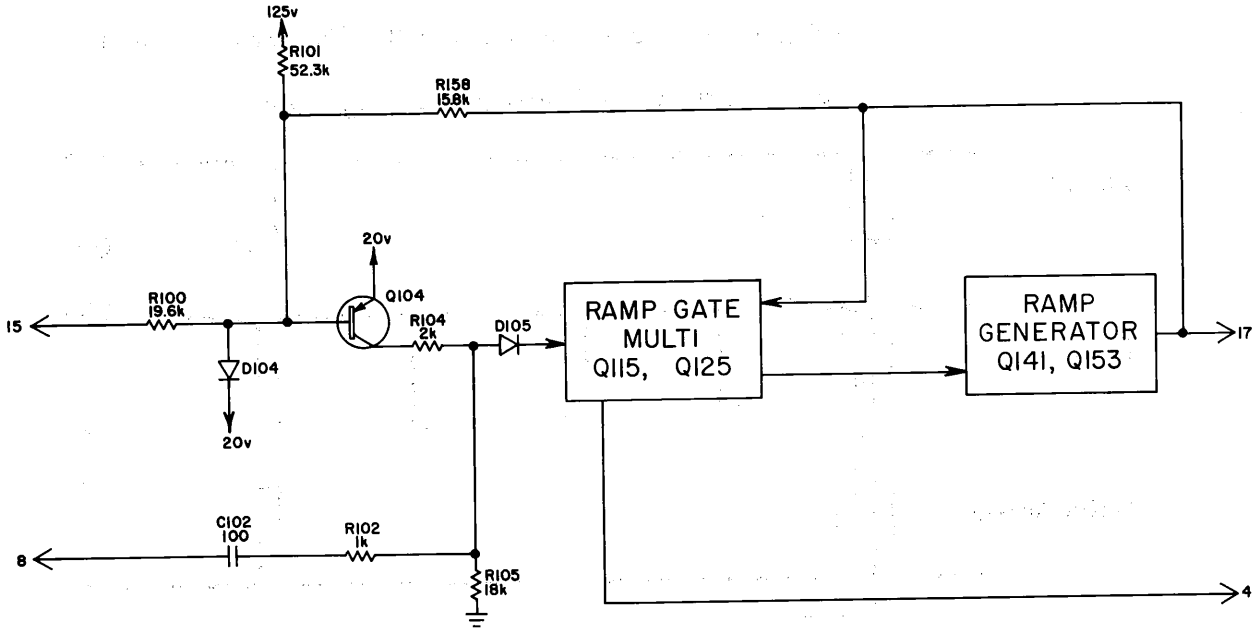


TYPE 6RIA VOLTMETER CARD
RAMP GENERATOR BLOCK DIAGRAM

B-6RIA-0024
7-17-'64 dl

1. The Ramp circuits are composed of the following blocks:
   a. Logic Gate, Q104.
   b. Ramp Gate Multi, Q115, Q125.
   c. Ramp Generator, Q141, Q153.
2. Q104, Q115 and Q125 are 151-071, 2N1305 germanium switching transistors.
3. Q141 and Q153 are 151-103, 2N2219 silicon transistors.
4. D104, D105, D115, D125, D153 and D156 are 152-075 germanium diodes.
5. D132, D140 and D141 are 152-141 silicon diodes.
6. System logic:
   a. The Logic Gate circuit can be considered an AND gate.
   b. If the print command is negative (count state) AND a positive step (Gate) arrives at pin 8, the Ramp Gate Multi will flip.
   c. When the multi switches, the ramp starts its run-up.
   d. As the ramp starts to run up, the ramp is fed back locking out the Logic Gate.
   e. The ramp is also fed back to the Ramp Gate Multi.
   f. As the ramp completes its run-up, the fed back ramp resets the multi.
   g. When the multi switches, it initiates retrace and the cycle is complete.
   h. The output ramp at pin 17 is an 18v positive going linear ramp of about 1.7 msec duration.

I. Logic Gate



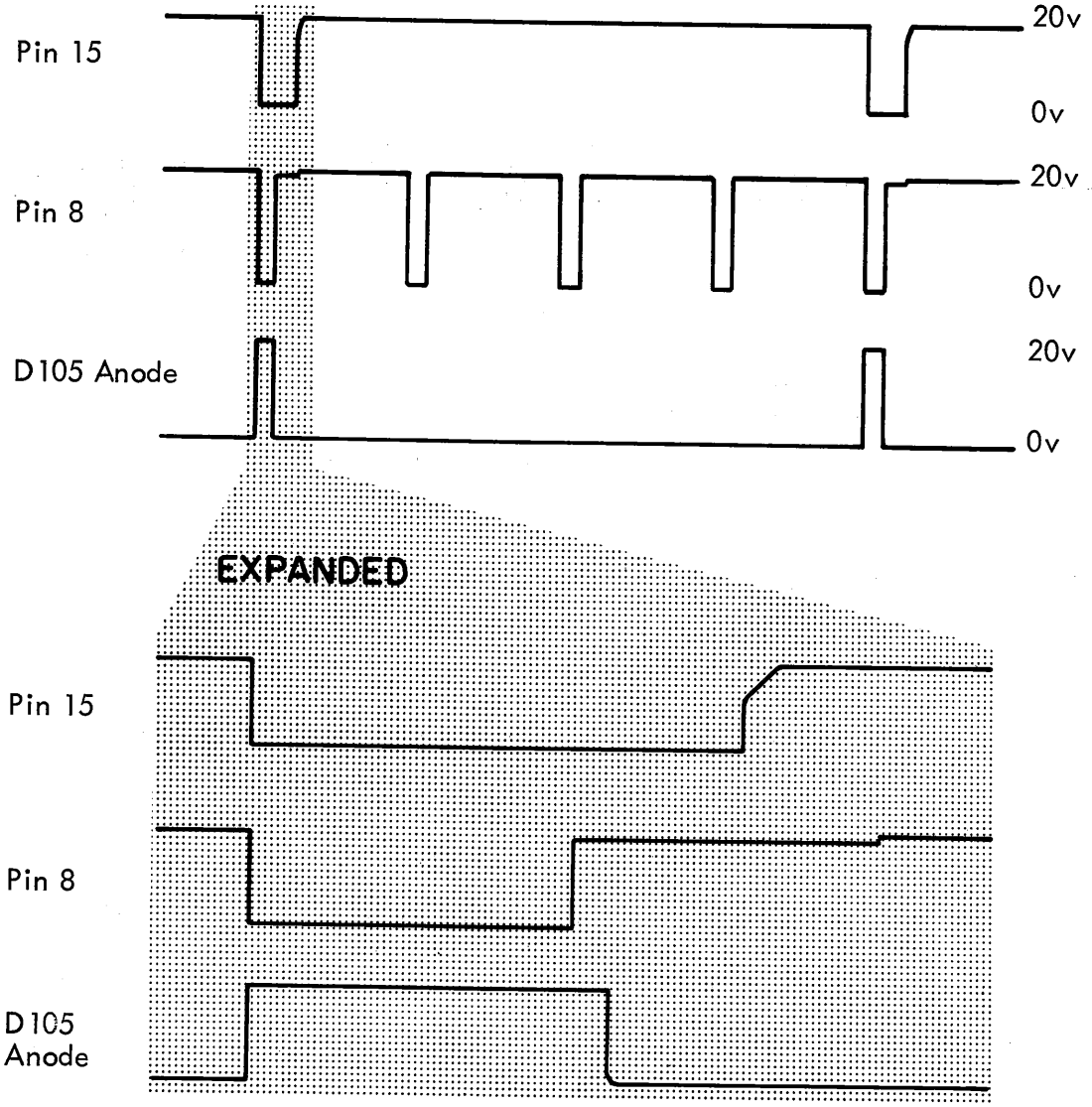
TYPE 6RIA VOLTMETER CARD
LOGIC GATE

B-6RIA-0025
7-20-'64 dl

1. The Print Command waveform drops the level on pin 15 from 20v to 0v.
   a. The Print Command comes from the Master Gate.
   b. It will drop to 0v at the <u>end</u> of a sweep (End of + DLY'D GATE).
      (1) The number of sweeps that pass before a print command pulse arrives is determined by a setting of the DISPLAY TIME control.
2. When the Print Command is at 20v, D104 is held in conduction with .75 ma through R101 (1.25 ma flows through R158 to total 2 ma through R101).
3. Q104 is cut off.
   a. D104 holds Q104 base at 20.3v.

4. The + gate waveform raises the level at pin 8 from 0v to 20v.

   a. The + gate waveform originates in the 0% Card, delayed about 5 mm*from the Sweep Unblanking Gate.

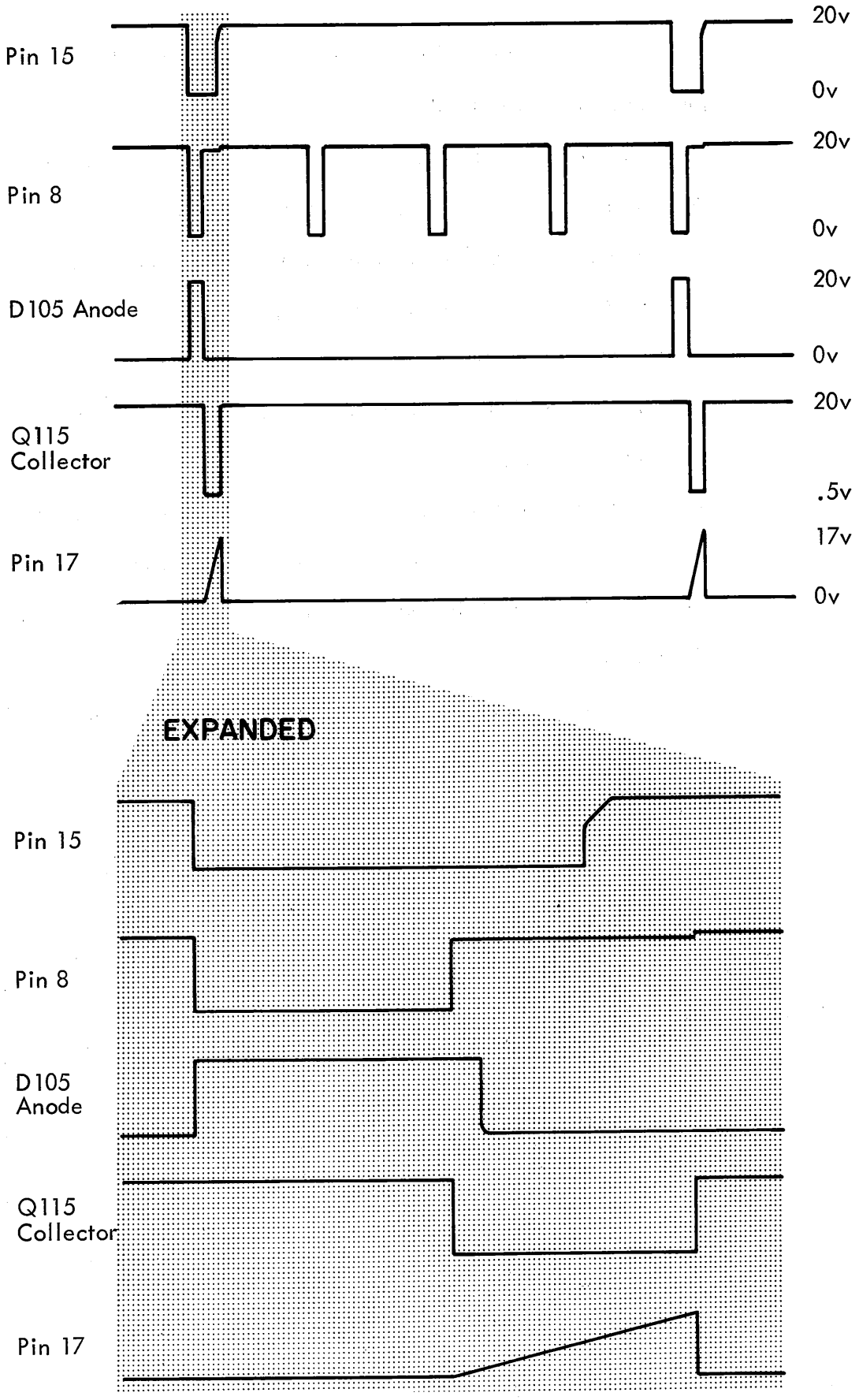


5. When the Print Command drops pin 15 to 0v, D104 cuts off and Q104 turns on.

   a. Q104 base is held at 19.7v by its base-emitter junction.

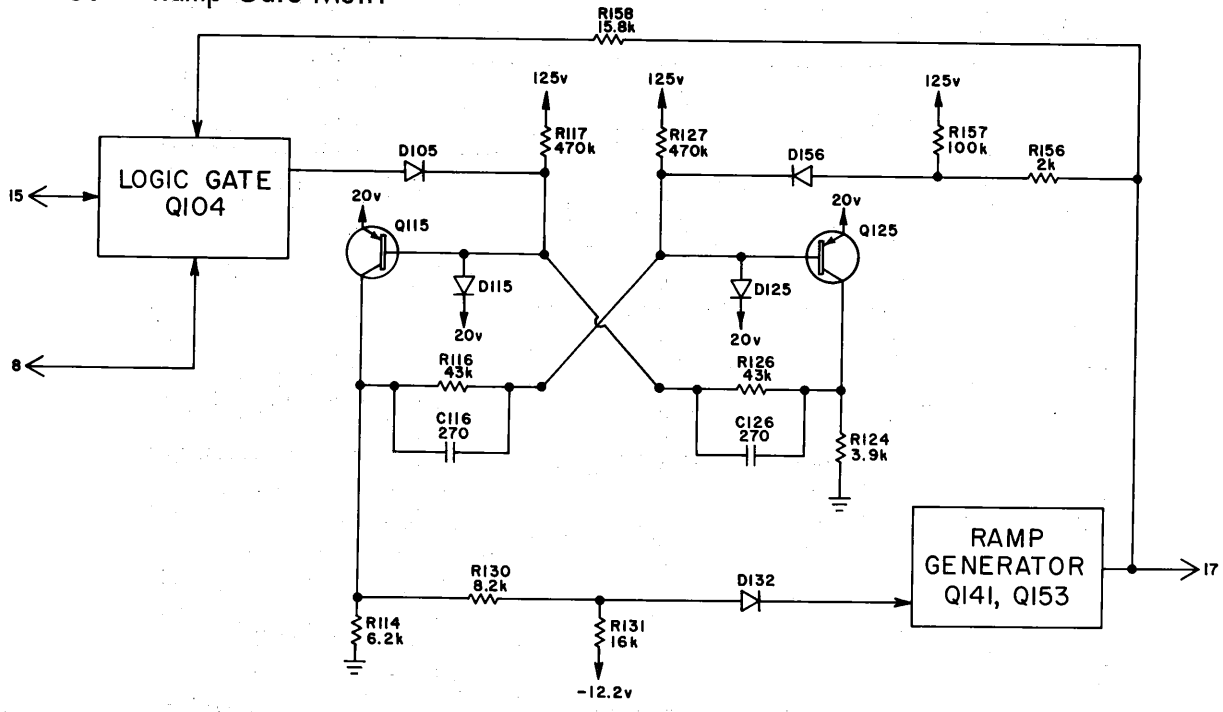
   b. Q104 collector pulls up to 20v as the transistor saturates.

* See 0% Zone Card, page 5-4.


Pin 15
20v
0v
Pin 8
20v
0v
D105 Anode
20v
0v
Q115
Collector
20v
.5v
Pin 17
17v
0v
EXPANDED
Pin 15
Pin 8
D105
Anode
Q115
Collector
Pin 17

6. With Q104 collector at 20v, a divider is formed of R104 and R105 placing D105 anode at 18v.
   a. As D105 cathode is at 19.7v, the diode remains back biased.
7. Prior to the arrival of a + Gate, C102 has an 18v charge.
   a. Pin 8 at ground and the top of R105 at 18v charges C102 to 18v.
8. As the + Gate arrives, the 20v step coupled through C102 and R102 turns on D105 and switches the multi, starting the ramp.
   a. As the multi flips, D105 cathode raises to 20.3v and conducts at this level.
   b. The balance of the 20v step through C102 appears across R102, preventing D105 from loading the + Gate source.
9. The Voltmeter Ramp is fed back through R158 to lock out the Logic Gate during Ramp run-up.
   a. As the fed-back ramp lifts Q104 base, the transistor cuts off.
   b. Q104 collector drops to ground, cutting off D105.

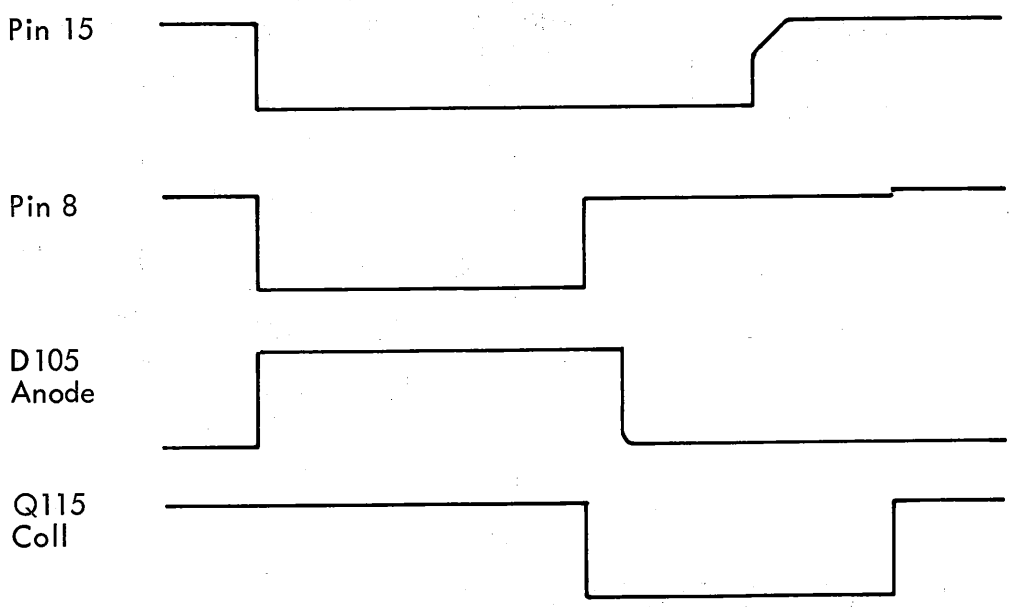
J. Ramp Gate Multi



TYPE 6RIA VOLTMETER CARD
RAMP GATE MULTI

B-6RIA-0027
7-21-'64 dl

1. The Ramp Gate Multi is a transistorized Eccles-Jordan bistable multivibrator.
2. Quiescently Q115 is conducting and Q125 is cut off.
3. Q115 base-emitter junction holds its base at 19.7v.
   a. 200 μa of base current flows in Q115.
   b. The transistor is saturated with its collector at 20v -- about 5.5 ma collector current.
4. D125 is conducting, placing Q125 base at 20.3v.
   a. 220 μa through R127 assures D125 conduction.
   b. With Q125 cut off, its collector is at 1.7v by virtue of 420 μa through R124, R126 (R117) and D115.
5. With Q115 conducting and its collector at 20v, D132 is forward biased with about 1 ma flowing.



6. The positive step from the Ramp Gate forward biases D105, which lifts Q115 base.

7. Through multi action, the multi switches with Q115 cut off and Q125 conducting.

   a. Q115 base rise is limited at 20.3v by D115.

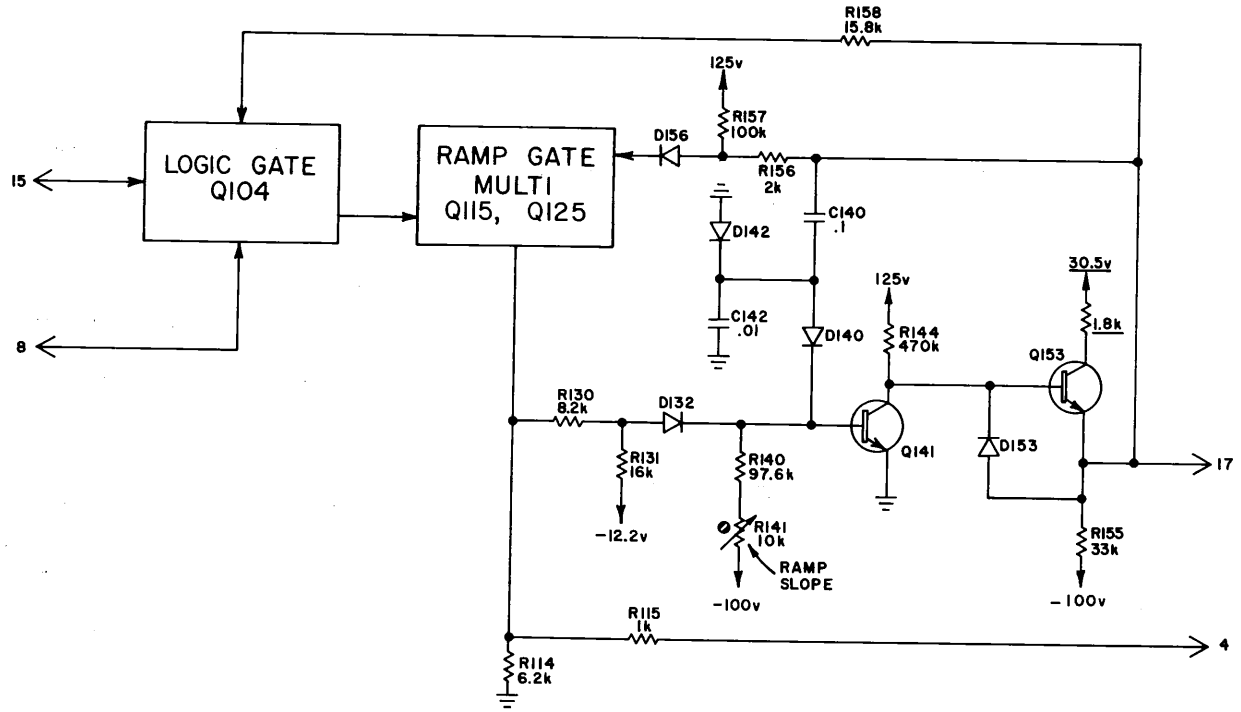
   b. D115 and D125 set the base level of the cut-off transistor instead of relying on the base-emitter breakdown of the transistor to establish the base level.

8. As Q115 collector drops to .5v, D132 cuts off.

   a. D132 anode drops to -4.14v.

9. As D132 cuts off, the ramp begins its run-up.

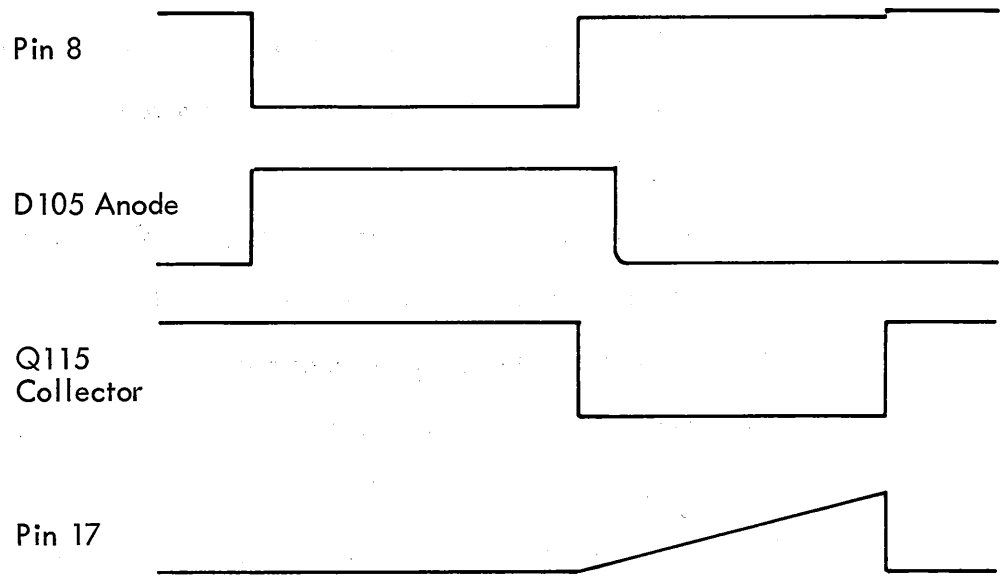
K. Ramp Generator



TYPE 6RIA VOLTMETER CARD
RAMP GENERATOR

B-6RIA-0026
7-21-'64 dl A

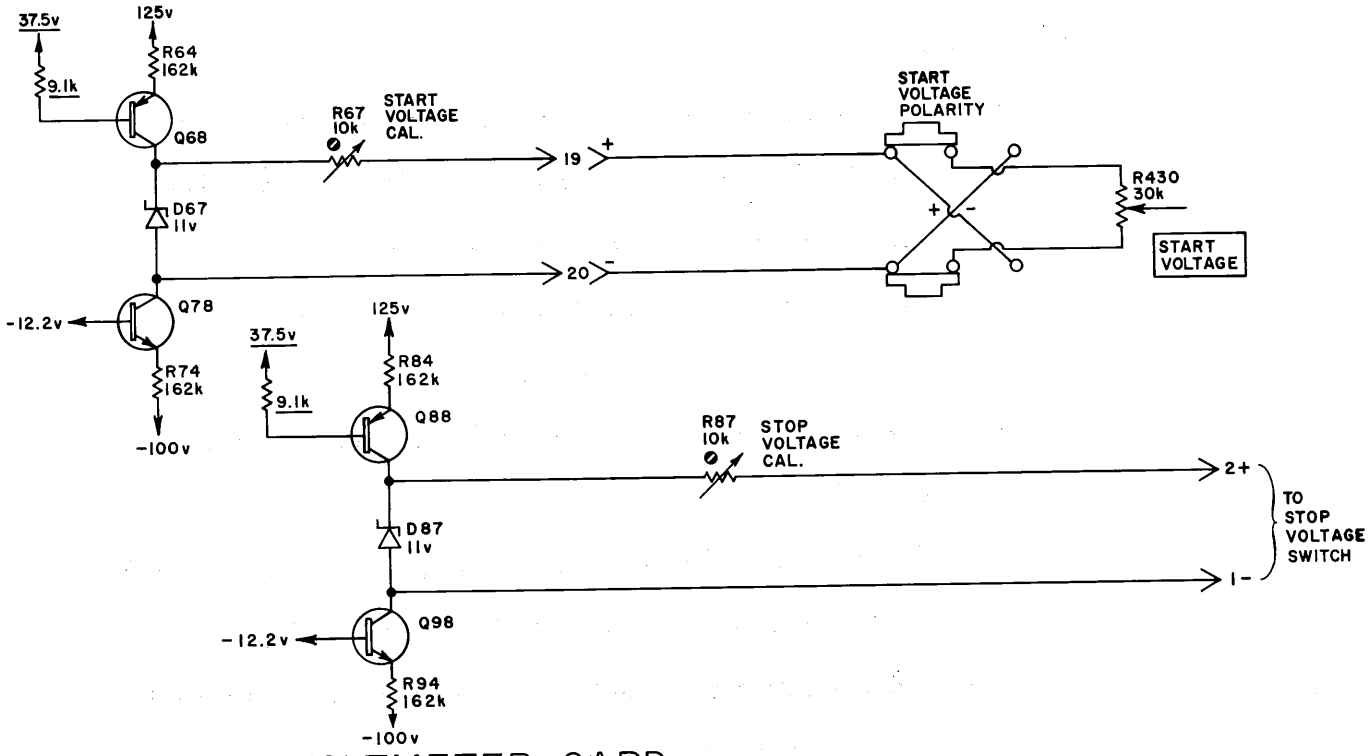
1. The Ramp Generator is a transistorized Miller Integrator.
   a. Q141 is the Miller transistor and Q153 the output EF.
2. Quiescently, Q141 is saturated, Q153 is conducting, D140 is cut off.



3. As the negative going step from the Ramp Gating Multi cuts off D132, Q141 base starts toward -100v.
4. As Q141 collector rises, the positive step passing through Q153 pulls up on C140; and as D140 conducts, charging current through D140 retards the drop at Q141 base.
   a. A step occurs at the start of the ramp as a result of D140 latch-up.
5. As Q141 collector runs up, feedback through C140 keeps Q141 base level virtually constant -- the base runs down about 70 mv.

6. Constant charging current through R140 and R141 assures a linear ramp of voltage across C140.
   a. C140 is a Tek made polycarbonate capacitor with a slight negative temperature coefficient.
   b. C140 negative coefficient is matched by the positive coefficient of the timing resistor.
   c. C140 has a 2-3% tolerance (rejects from more accurate timing requirements in other scopes) compensated by the RAMP SLOPE adj, R141.
   d. R141 adjusts the ramp slope to 1v per 100 clock pulses.
7. The ramp is fed back through R158 to the Logic Gate to lock out the circuit until after completion of the ramp.
8. The ramp is fed back through R156 to D156 anode.
   a. D156 cathode sets at 19.7v.
   b. As D156 becomes forward biased, it pulls up on Q125 base.
   c. Through multi action, the multi switches as Q125 cuts off and Q115 conducts.
9. Q115 collector pulls up to 20v, D132 conducts, D140 disconnects and Q141 saturates.
10. As Q141 collector drops to 0v, D153 conducts, providing a low Z discharge path for C140 through Q141 to ground during retrace.
    a. As retrace starts, D142 conducts completing the low Z discharge path for C140.
11. C142 keeps radiated 1 mc clock pulses out of the ramp circuit.
12. The output ramp is fed through pin 17.
    a. A negative going 20v gate with the same duration as the ramp is fed to the Master Gate via pin 4.

L. Floating Power Supplies



TYPE 6RIA VOLTMETER CARD
START-STOP VOLTAGE FLOATING SUPPLIES

B-6RIA-0028
7-22-'64

1. Two identical 10v floating supplies are provided.
   a. 10v is provided at pins 19 and 20 for the START VOLTAGE helipot.
      (1) Pin 19 is plus and pin 20 is minus.
   b. Another 10v at pins 1 and 2 supplies the STOP VOLTAGE helipot.
      (1) Pin 2 is plus and pin 1 is minus.

2. Q68 and Q88 are 151-133, selected from MM999 silicon PNP transistors.

3. Q78 and Q98 are 151-103, 2N2219 silicon NPN transistors.

4. Either of the supplies can ride either above or below the 0% memory voltage.

   a. The memory has an on-screen excursion of 6 to 14 volts.

   b. Pin 19, then, could be required to swing as high as 24v (pin 20 at 14v plus 10v across the supply).

   c. Pin 20 could be required to drop as low as -4v (pin 19 at 6v minus 10 across the supply).

   d. The STOP VOLTAGE supply would have equal possible excursions.

   e. Actually, pin 19 could swing to 37.5v and pin 20 to -12.2v (Q68 and Q78 base potentials) before "bottoming out".

5. Both Q68 and Q78 are connected in a grounded base configuration.

   a. The transistors are long-tailed to provide a constant .54 ma through the transistors -- .24 ma flows through the zener and .3 ma through R87 and the Helipot.

      (1) Q68 base potential was chosen to place the same voltage drop across R64 as that across R74.

   b. The circuit offers a very high collector impedance.

   c. This allows the supply to move quite freely over the 50v range from -12.2v to 37.5v.

6. The reference element is a 11v 5% zener.

   a. R67 (START VOLTAGE CAL) adjusts for zener error.

b. The START VOLTAGE and STOP VOLTAGE pots are 30k.

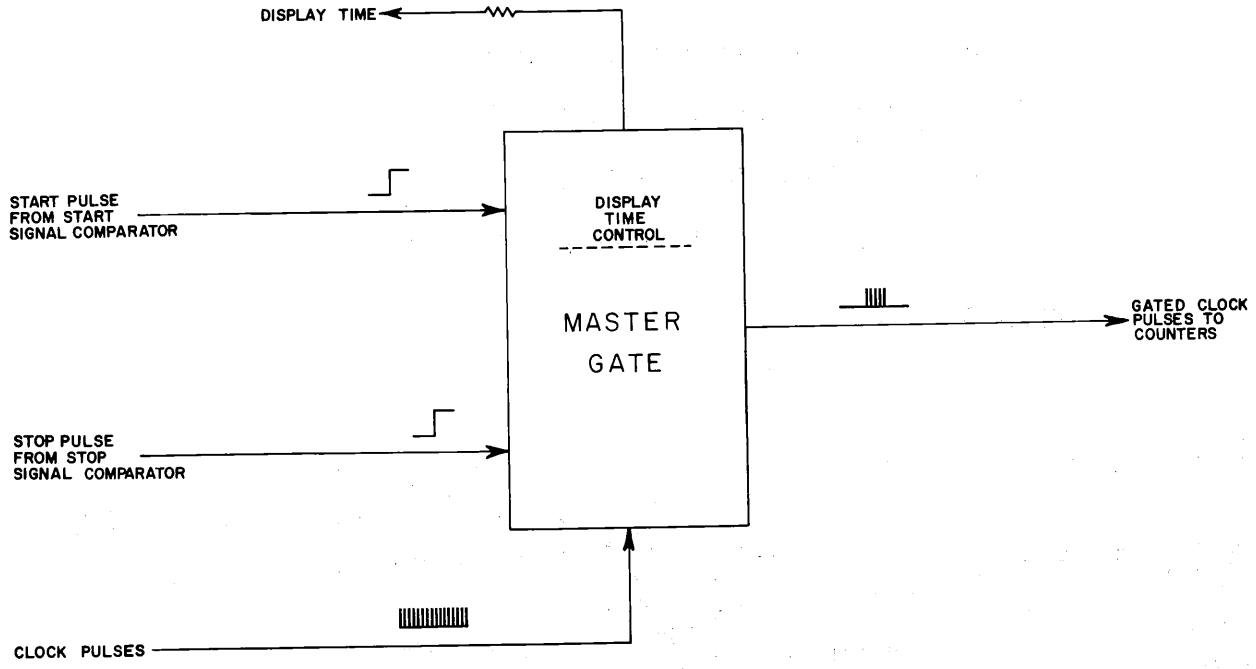
c. .33 ma flows through each pot.

d. If D67 was at the maximum of its rating at 11.55v, R67 would have 1.55v drop across it or with D67 at 10.45v would have .45v across it.

(1) R67 would have a range of 1.38k to 4.65k under these conditions.

IX. MASTER GATE

A. The main purpose of the Master Gate Card is to control the flow of clock pulses to the counter circuits.



TYPE 6RIA MASTER GATE
SIMPLIFIED BLOCK

B-6RIA-0055
5-14-'64 jg

1. The time duration of the clock pulse interval is controlled by a signal from the START and STOP Comparator circuits.
2. There is just one Master Gate Card in the Type 6R1A.

B. Two basic circuits comprise the Master Gate circuits.

1. Clock Gate circuits:

   a. Start Multi; Q105, Q115.

b. Stop Multi; Q125, Q135.

c. AND Gate; Q173, Q143, Q93, Q153, Q163.

d. Clock Inverter Amplifier, Q164.

e. Ramp Gate EF, Q3.

2. Print Command circuits:

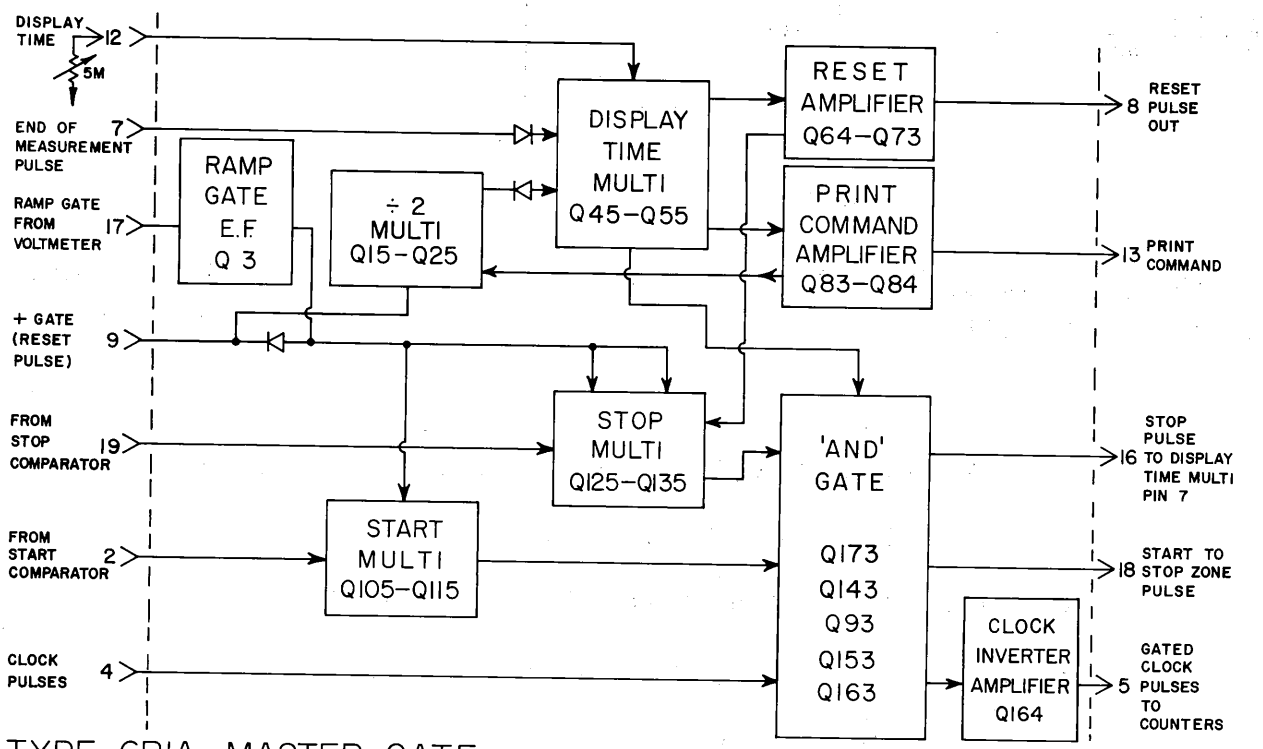
a. ÷2 Multivibrator; Q15, Q25.

b. Display Time Multi; Q45, Q55.

c. Reset Amplifier; Q64, Q73.

d. Print Command Amplifier; Q83, Q84.

C. Block Diagram



TYPE 6RIA MASTER GATE
BLOCK DIAGRAM

B-6RIA-0056
5-18-64 jg

D. Inputs to the Master Gate

1. Display Time, Pin 12: The output from the DISPLAY TIME control that controls the display period.

2. End of Measurement, Pin 7: Sets the Display Time Multi to the display state at the end of a measurement.

   a. The RESOLUTION switch selects either the Stop Pulse Out from pin 16 (ONE STEP position) or a ÷ 10 version of the pulse from the ÷10 card (AVERAGE OF 10 SWEEPS position).

3. Ramp Gate, Pin 17: A negative going gate the same duration as the Voltmeter Ramp.

   a. Prohibits the + Gate from resetting the START and STOP Multivibrators in case the time of the Voltmeter Ramp is longer than the + Gate.

4. + Gate, Pin 9: Resets the ÷ 2 Multi and the START and STOP Multivibrators at the start of sweep.

   a. This is the Delayed Gate (delayed 5 mm) from the 0% Zone Card.

5. Start Comparator, Pin 2: A positive step from the START Comparator Card.

   a. Will flip the START Multi and if the Display Multi has been set to the Count condition, will start count.

6. Stop Comparator, Pin 19: A positive going step from the STOP Comparator Card.

   a. Will flip the STOP Multi and stop count.

7. Clock In, Pin 4: Clock pulses to be counted.

   a. The clock pulses may be either Time of Voltmeter Clock pulses, depending on the setting of the MODE switch.

E. Master Gate Outputs

1. Clock Out, Pin 1: 20v clock pulses to the ÷1, 2, 5 card.
2. Start to Stop Zone, Pin 18: An 18v negative going signal to the Analog Circuit to intensify the portion of the display being measured.
3. Stop Pulse Out, Pin 16: An 18v positive going step at the end of the count period to reset the Display Multi to the display condition after the count has been taken.

   a. The step passes through the RESOLUTION switch (see End of Measurement Input, Pin 7).

4. Print Command Pulse, PLUS to Pin 13, PLUS or MINUS (optional with strap) to Pin 20.

   a. The minus Print Command (pin 20) is used only with an external programer or printer.

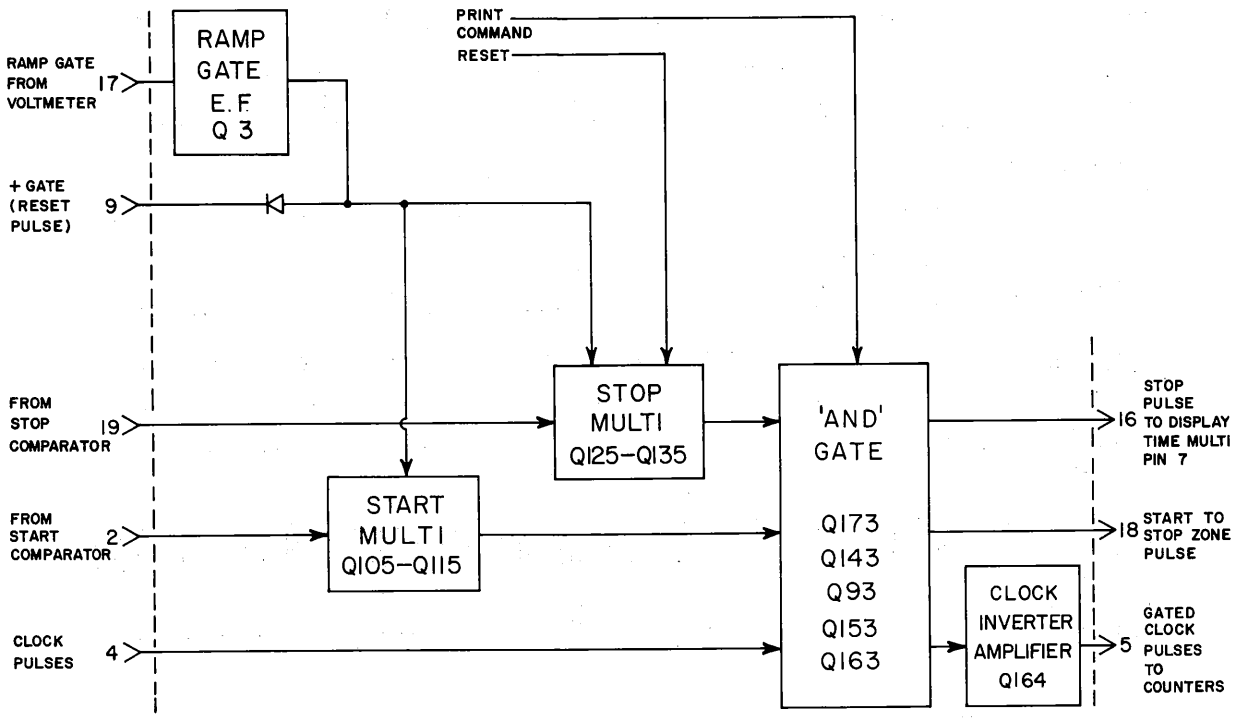
   b. The plus Print Command is at 2v for the count state and 20v in the display state.

   c. The signal is fed to the Memories, the Voltmeter Card, and the Limit Light Driver.

   d. It tells the 6R1A when to take a measurement and how long to hold the measurement.

5. Reset Out, Pin 8: 100v peak-to-peak (from 125v to 225v) to set the counters to zero count before a new count begins.

E. Clock Gate Block Logic

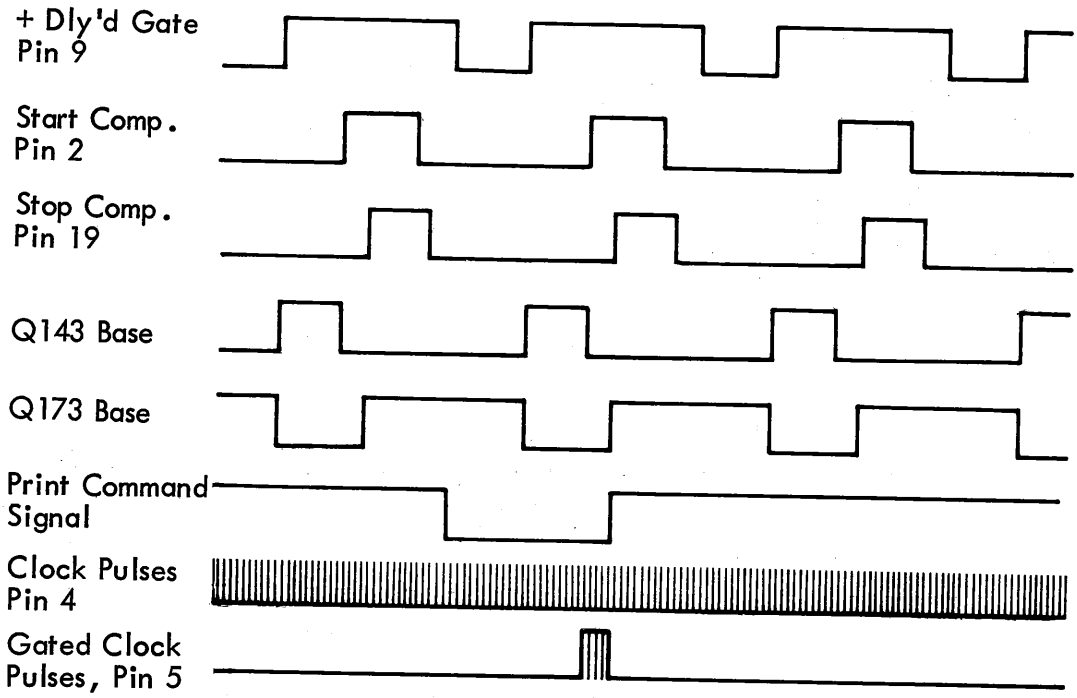


TYPE 6RIA MASTER GATE
CLOCK GATE BLOCK DIAGRAM

B-6RIA-0057
7-28-'64 jg

1. 20v clock pulses arrive continuously on pin 4 and are fed to the AND GATE.
2. At the start of sweep (actually 5 mm after the start of sweep) the start of + Gate from pin 9 presets the Start and Stop Multivibrator.

3. When the Start Comparator has an output (positive going 18v step), the Start Multi flips, providing a negative output to the AND Gate.



4. When the Stop Comparator has an output (positive going 18v step) the Stop Multi switches, providing a positive output to the AND Gate.

5. During the count state the Print Command output (LOW) is fed to the AND Gate.

6. The AND Gate, then, has four inputs.

   a. The Start Multi.

   b. The Stop Multi.

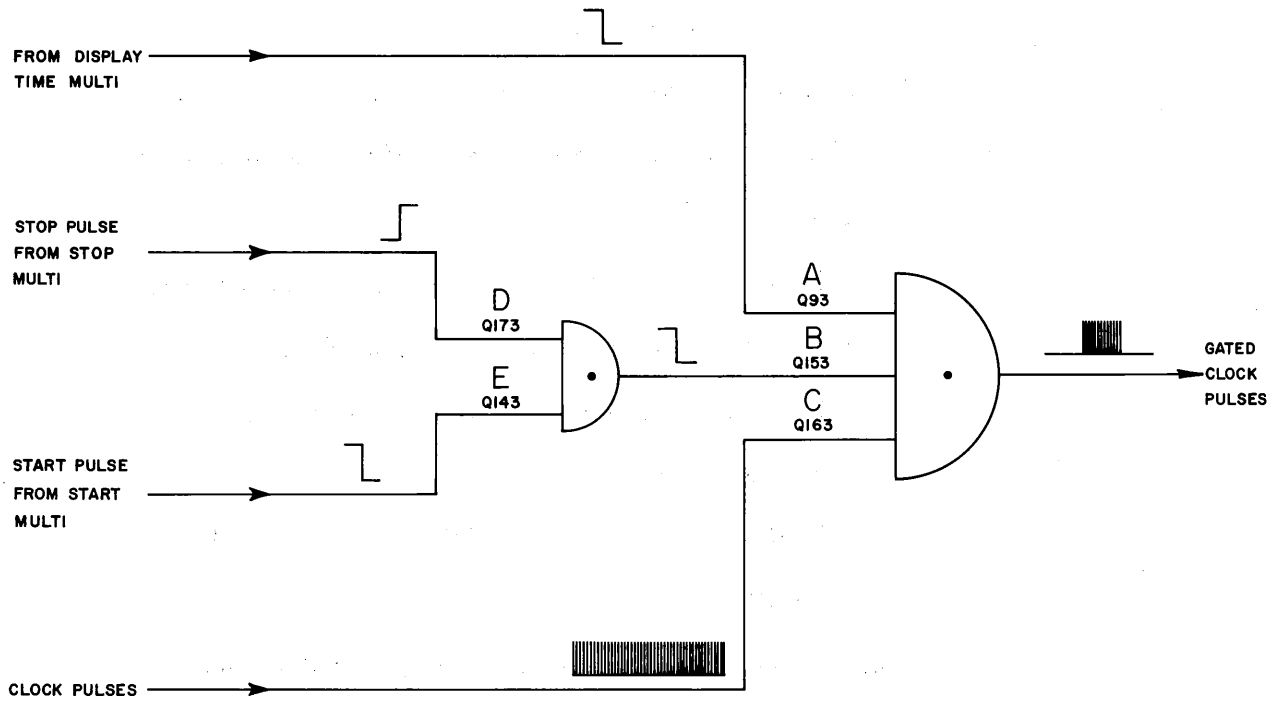
   c. Print Command.

   d. Clock Pulses.

7. The Start Multi, the Stop Multi and the Print Command inputs to the AND Gate determine the time duration of the clock pulses.

F. AND Gate; Q173, Q143, Q93, Q153, Q163 and Clock Shaper, Q164

1. The AND Gate controls the flow of clock pulses to the counters.
2. The circuit uses four 2N1304, 151-069 germanium NPN transistors.
3. Three 152-075 germanium diodes are used.
4. AND Gate logic.



TYPE 6RIA MASTER GATE
SIMPLIFIED BLOCK - 'AND' CIRCUIT

B-6RIA-0059
7-23-64 jg

a. Signals controlling inputs A and B govern the flow of clock pulses through C.

b. Input A is controlled by the Display-Time Multivibrator from the DISPLAY TIME control on the front panel.

(1) Display time varies from .1 sec to 5 sec.

c. Input B is controlled by the Start and Stop multivibrators (through Gate D,E).

(1) The Start Multi is controlled by a signal from the START Comparator.

(2) The Stop Multi is controlled by a signal from the STOP Comparator.

d. Clock pulses are always applied to input C.

e. Both input A and input B must be LOW before clock pulses can pass.

(1) If either A or B is HIGH, clock pulses cannot pass.

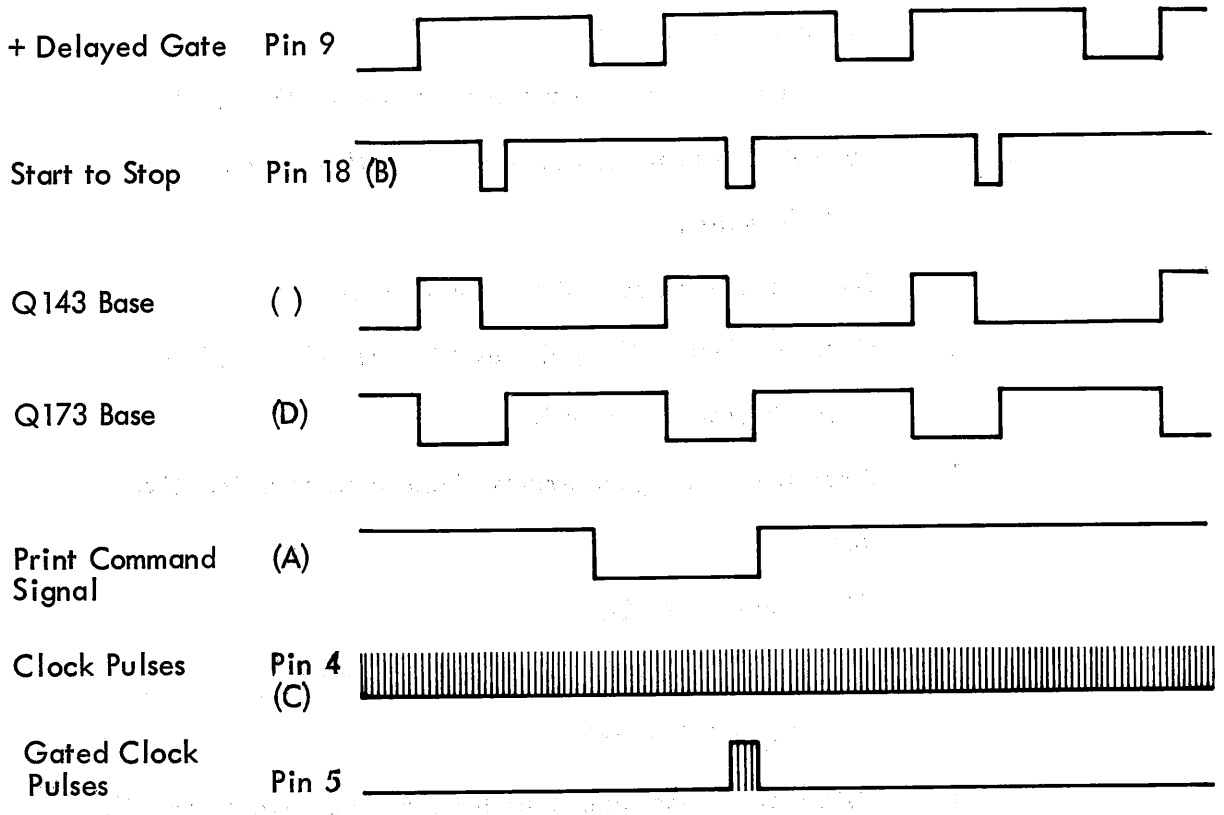
f. Input B depends on the condition of Gate D,E.

(1) If Input D is LOW and input E is LOW, input B will be LOW.

(2) If either input D or E are HIGH, input B will be HIGH.

g. Logic levels in the Master Gate are HIGH (20v) and LOW (2v).

5. Sequence of Operation.



a. Quiescently (prior to sweep), input A and input B will be HIGH.

(1) Input D will be HIGH.

(2) Input E will be LOW.

(3) Gate D,E is HIGH.

(4) Gate A, B, C has no output.

b. With the arrival of + Gate, the Start and Stop Multis reset.

(1) Input D is LOW.

(2) Input E is HIGH.

(3) The Gate has no output.

c. Arrival of a start signal on pin 2 will drop input B to its LOW state momentarily, but as long as input A is HIGH the Gate has no output.

d. At a time, variable from the front panel DISPLAY TIME control, the Print Command signal will drop input A to its LOW state.

(1) This will occur at the end of + Gate.

e. Start of + Gate will again reset the START and STOP Multivibrators (see step b).

f. When the start signal arrives, input E drops to its LOW state.

(1) Input D is LOW.

(2) Gate D, E is LOW (it has an output).

(3) Input B is LOW.

g. With input A and input B both LOW, the AND Gate will pass clock pulses.

h. When the stop signal arrives at pin 19, input D switches to its HIGH state.

(1) Gate D,E output is HIGH.

(2) Input B is HIGH.

(3) The AND Gate has no output -- clock pulses cannot pass.

i. The STOP signal (through the RESOLUTION switch) switches the Print Command to the Display State.

(1) Input A switches to HIGH.

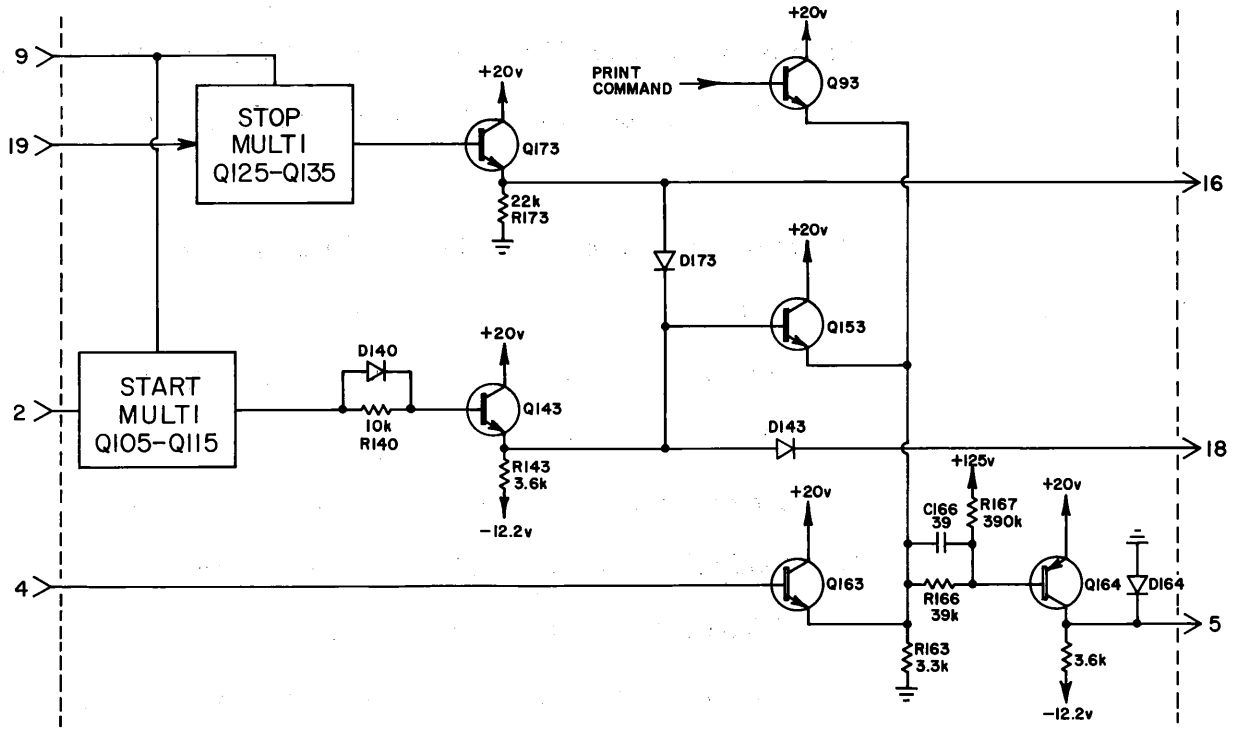
j. At the end of + Gate, a reset pulse from Display Time Multi resets the Stop Multi.

(1) This places input D in its HIGH state.

(2) It insures that no clock pulses can pass the GATE during retrace.

k. The cycle is complete.

6. AND Gate Circuit:



TYPE 6RIA MASTER GATE
'AND' GATE

B-6RIA-0061
7-27-'64 jg

a. Positive going clock pulses are applied to Q163 base (input C in the logic discussion).

(1) Time clock pulses are about 19v peak-to-peak.

(2) Voltmeter clock pulses are 18v peak-to-peak.

b. When either Q93 (input A) or Q153 (input B) is conducting (HIGH logic level), Q163 emitter is pulled up to 20v cutting off the transistor.

(1) Since the clock pulses on Q163 base never reach 20v, no part of the clock pulses can pass.

c. When both Q93 and Q153 are cut off, Q163 conducts.

(1) The clock pulses on Q163 emitter swing from 4v to 19v.

d. The base of Q93 is controlled by the Display-Time Multivibrator.

(1) The base swings from HIGH, 19.5v to LOW, about 0v.

e. The base of Q153 is driven by an AND gate formed by Q143 and Q173 (inputs D and E in the logic discussion).

(1) When both Q143 AND Q173 bases are LOW, Q153 base drops to 2v dropping Q153 emitter to 1.7v.

(2) If either Q143 or Q173 is conducting heavily, Q153 base will be at 20v (HIGH) biasing Q153 to saturation.

f. R140 in Q143 base lead prevents a capacitively coupled pulse from the STOP Multi from flipping the START Multi.

(1) When the Stop Multi flips, pulling up on Q143 emitter, the pulse would capacitively couple through the emitter-base junction and flip the Start Multi.

(2) The presence of R10, however, caused a delay when the START Multi reset.

(3) The positive step had to charge Q143 base C through R140 before it could turn on Q143.

(4) If, at reset time (start of + Gate), the STOP Multi resets before the Start Multi resets, there would be an interval when the AND Gate would allow clock pulses to pass.

(5) D140 provides a low impedance path for the charging current.

g. D173 allows Q173 emitter to pull up on Q153 base to stop the flow of clock pulses, but disconnect when the STOP Multi resets and drops Q173 emitter to ground.

(1) The START TO STOP Zone waveform on pin 18 gets the negative step from Q143 emitter at the START of count and its positive step from Q173 emitter (through D173) at the end of count.

h. D143 prevents noise from the analog circuit from reaching the emitter of Q143.

7. Clock Shaper, Q164.

a. The clock pulses on the common emitters of Q93, Q153, Q163 swing from about 2v to 18v.

b. Aberrations appear on the top and bottom of the pulses that could effect the count.

c. Q164 is biased by divider R166, R167 so that its base sets quiescently at about 25v -- 5v past cut off.

d. The peaks of the clock pulses drive Q164 to saturation.

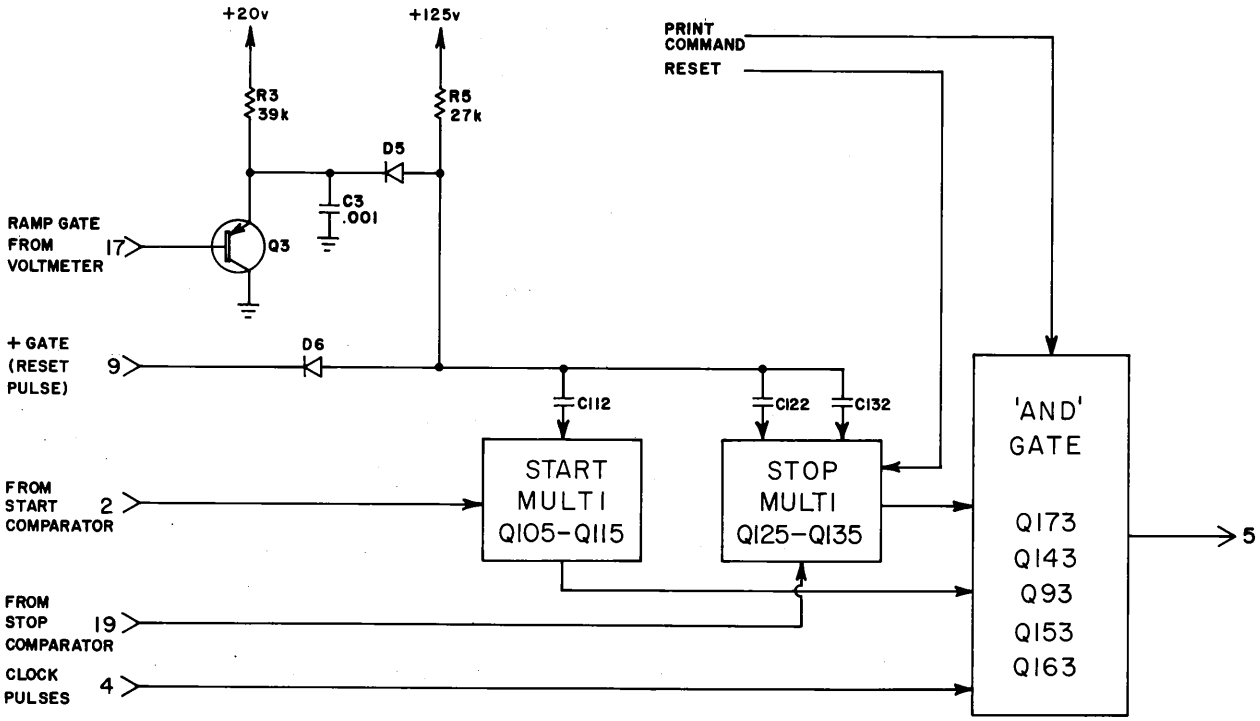
e. The pulses are shaped by both saturation and cut off.

f. The clock pulses at pin 5 swing from ground (limited by D164) to 20v (Q164 saturation).

G. Ramp Gate; Emitter Follower, Q3

1. Q3 with D5 and D6 form an AND Gate that controls the resetting of the START and STOP Multivibrators.

a. The circuit prevents the + Gate from resetting the START and STOP Multi's while a measurement is being taken.



TYPE 6RIA MASTER GATE

B-6RIA-0062

b. The Voltmeter Ramp (and the Ramp Gate) have a duration of approximately 1.7 msec.

c. For sweeps above .1 msec/div (1 msec gate signal) (3B2 Sweep Generator for example), the + Gate is shorter than the Ramp Gate.

d. Without the inhibiting action of Q3, D5, the + Gate, would reset the START and STOP Multi's before the completion of count (when reading voltage).

e. When Q3 emitter is HIGH and pin 9 goes from LOW to HIGH (start of + Gate), the START and STOP Multi's will reset.

2. Q3 is a 151-071 2N1305 germanium PNP transistor.

3. D5 and D6 are 152-075 germainum diodes.

4. If a voltage measurement is to be made:

a. Print command will be in the count state.

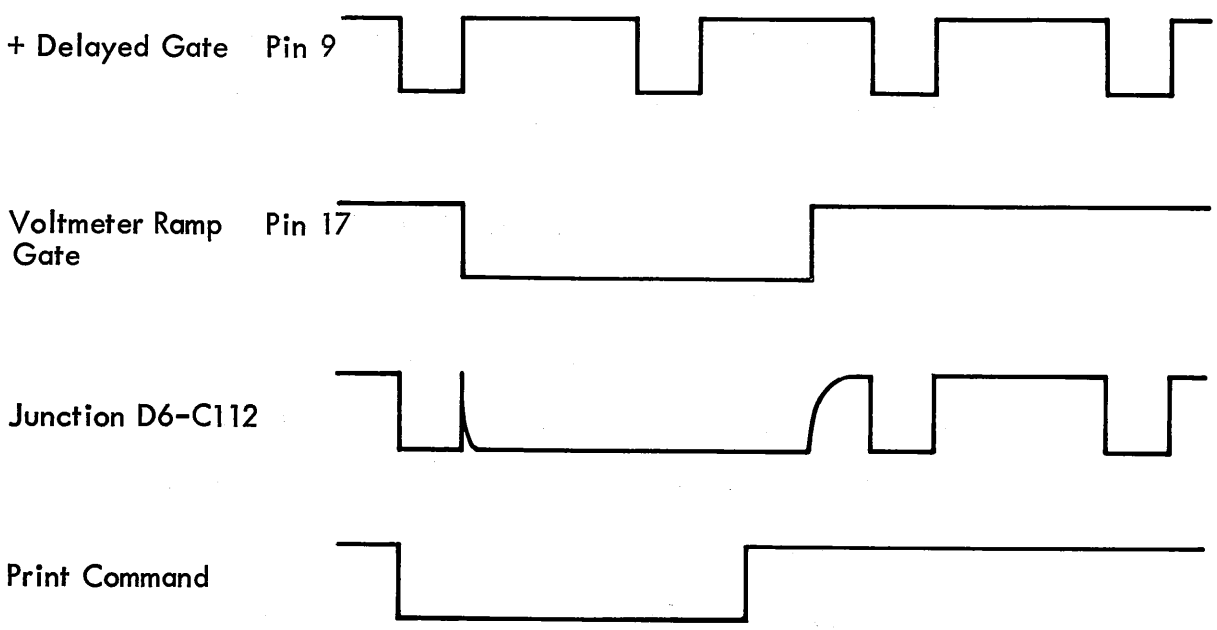
b. At the start of + Gate, a Voltmeter Ramp* will be started.

c. A negative going Ramp Gate* will be started.

d. The Delayed + Gate will place pin 9 at ground.

e. Conducting D6 will hold the junction of D5, D6 at ground.

* See Voltmeter Card.



5. The Ramp Gate (negative going) appears on pin 17 at the same time that the + Gate appears on pin 9.
   a. The negative step of the Ramp Gate drops Q3 base to zero volts.
   b. C3 must discharge through Q3 before Q3 emitter can follow.
   c. Before C3 gets a chance to discharge and Q3 emitter is still HIGH, the + Gate resets the START and STOP Multi's.

d. As C3 charges, Q3 emitter pulls down to 0v.

e. D5 pulls the junction of D5, D6 to 0v.

f. The Ramp Gate waveform holds the circuit in this state until the end of the Voltmeter Ramp.

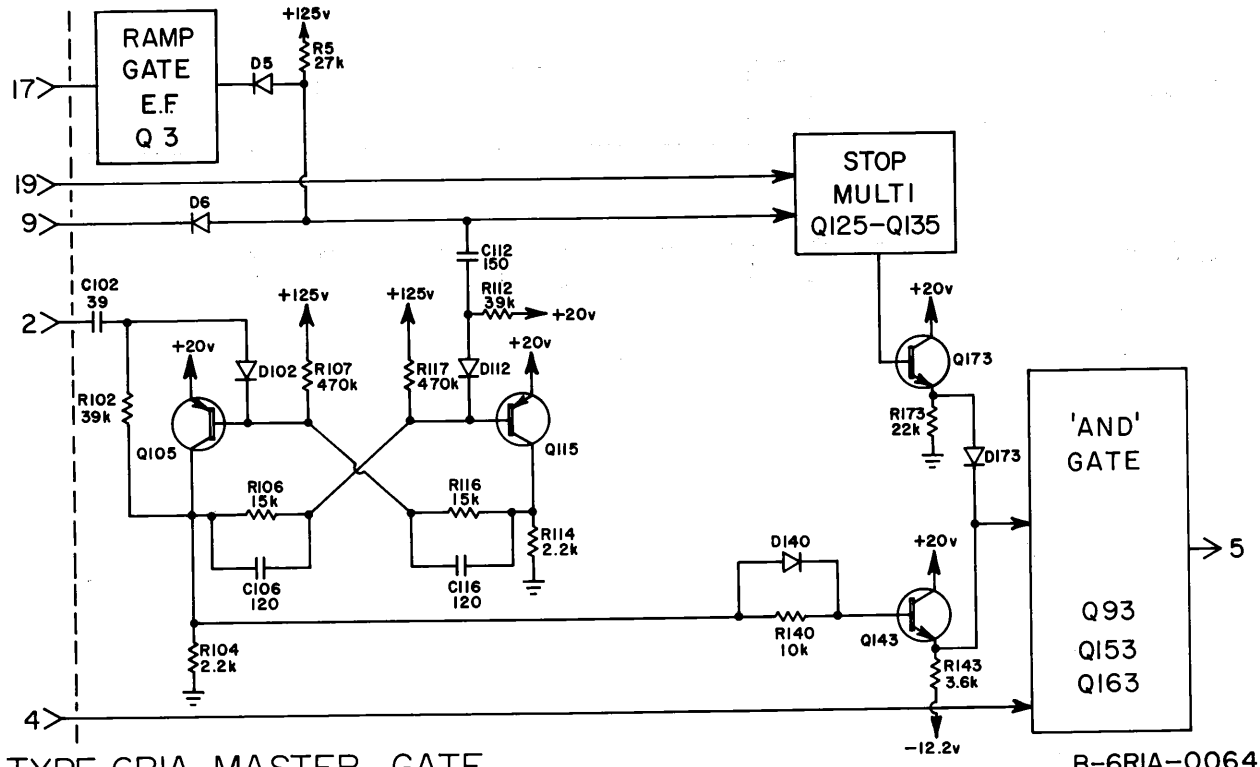
g. + Gate cannot reset the START and STOP Multi's during this period.

6. D6 allows the junction of D5, D6 to remain clamped at ground during Ramp Gate without loading the + Gate source.

7. At the end of Ramp Gate, C3 prevents the Ramp Gate step from resetting the Start and Stop Multi's.

H. Start Multi; Q105, Q115.

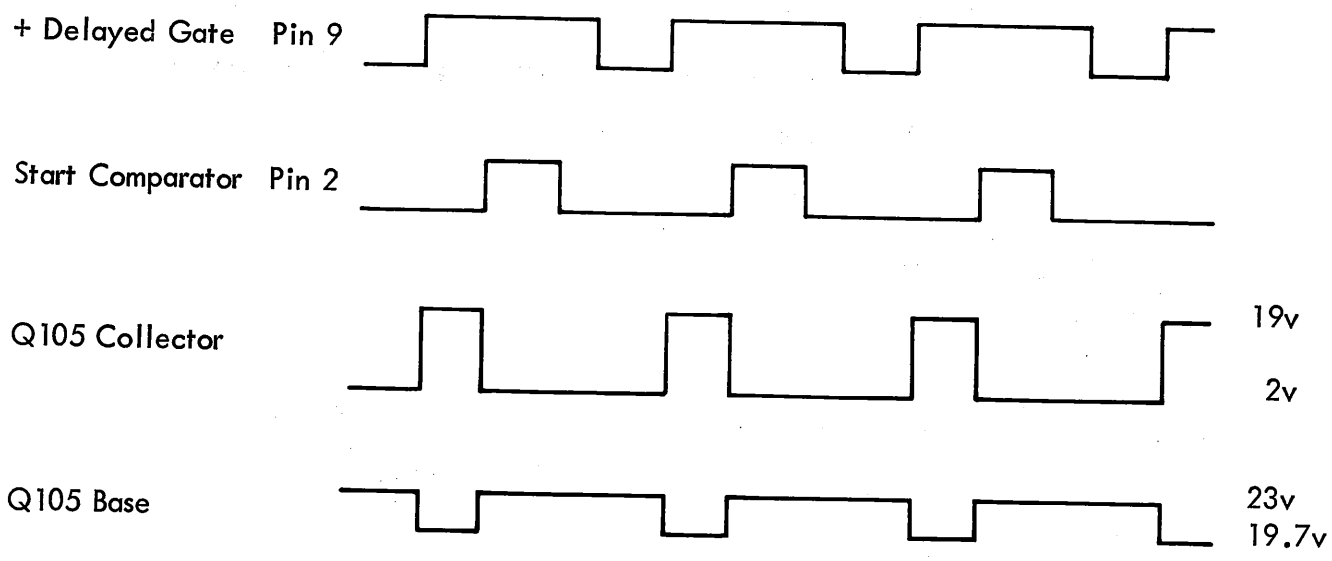
1. The Start Multi provides a negative step (LOW logic level) to the AND Gate to start count.



TYPE 6RIA MASTER GATE
START MULTIVIBRATOR

B-6RIA-0064
7-30-64 jg

2. The Multi is a transistorized Eccles-Jordan bistable multi.
3. The two transistors are 151-054 germanium PNP transistors selected for BV_{CBO} and BV_{EBO} from 2N2957.
4. D6, D102 and D112 are 152-075 germanium diodes.
5. Quiescently (prior to sweep), Q105 is off and Q115 is saturated.
   a. Q105 collector (the multi output) is held at 2v by the cross coupling divider.



6. When the + Gate (delayed 5 mm) arrives, the Multi flips (resets).
   a. The positive + Gate step cuts off D6.
   b. Released of the current through D6, the bottom of R5 moves toward 125v.
   c. The positive step through C112 lifts Q115 base (through D112).
   d. As Q115 base is pulled up, Q115 cuts off as the multi flips.
      (1) Q115 off, Q105 saturated.
   e. Q105 collector (the circuit output) raises to 20v.
   f. The Start Multi input to the AND Gate is HIGH -- clock pulses cannot pass.
   g. The Multi is reset (NOT START state).
7. The first positive signal from the Start Comparator (through pin 2) again flips the Multi.
   a. The 20v positive step through C102 pulls up on D102 and Q105 base.
   b. Q105 cuts off as the Multi flips.
   c. Q105 base raises to 23v cutting off D102.
      (1) With D102 open, further signals from the Start Comparator cannot reach the Multi until it is reset at the start of the next + Gate.
      (2) The base is limited at 23v by R116, R107.

d. As Q105 cuts off, its collector (Stop Multi output) drops to 2v.

e. The Start Multi input to the AND Gate is LOW

f. If the other inputs to the AND Gate are LOW, clock pulses can pass.

8. Only a positive step from the + Gate (pin 9) will reset the Multi.

9. Two changes to the Start Multi were made in pre-production.*

a. D112 anode was connected through R112 to 20v while D102 anode ties to Q105 collector.

(1) This places D112 closer to conduction than D102.

b. C102 was changed to 39 pf (from 100 pf) while C112 was increased to 150 pf.

(1) The larger capacitor (C112) provides more energy to turn on D112 quickly.

c. Both changes insure that if a positive pulse arrives on pin 2 at the virtually same time that + Gate goes positive, the + Gate will take priority and reset the Multi.

(1) This condition occurs when the First-Second Slope Multi (Start Comparator Card) is reset by the + Gate.

(2) Under this condition, the + Gate arrives a few nanoseconds ahead of the START Comparator pulse.

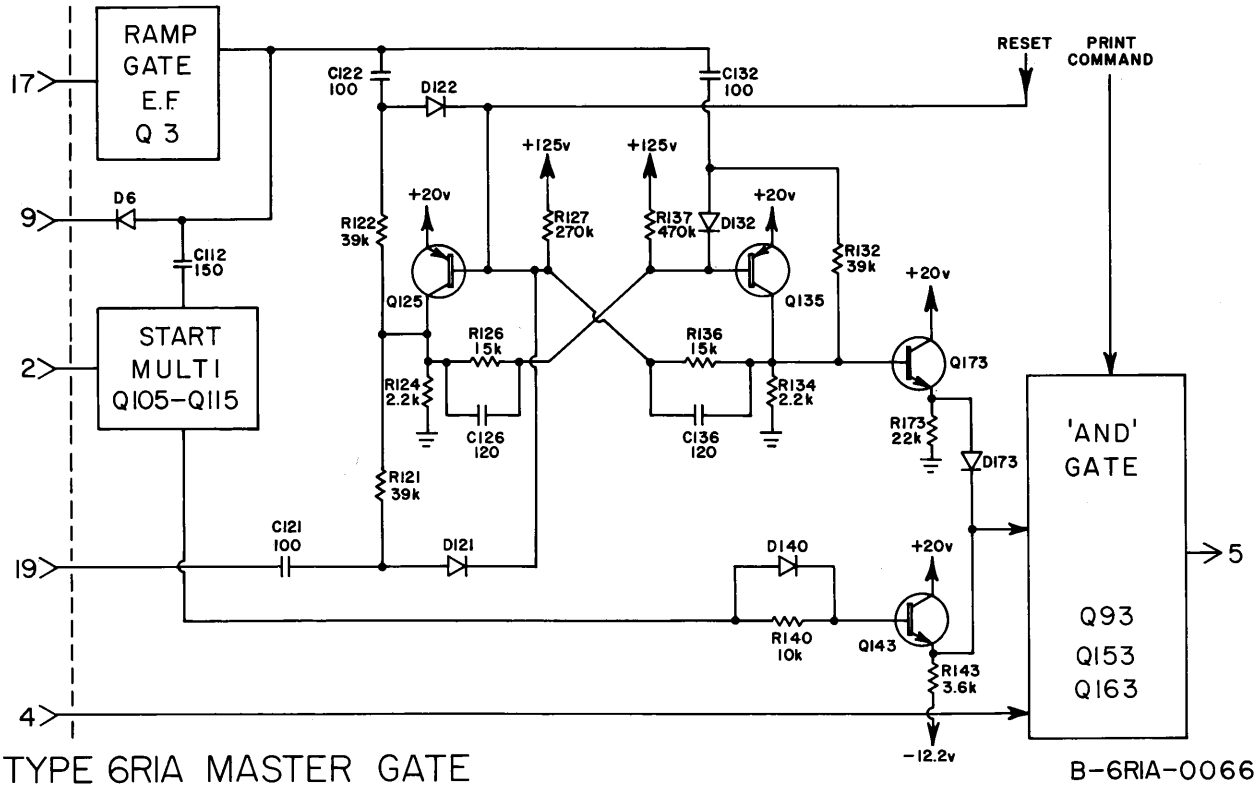
* About SN 1090.

(3) The Multi would reset, then flip again on the arrival of the START Comparator pulse.

(4) C112 stores enough energy to hold Q115 base up (cut off) until the false Start pulse has passed.

1. Stop Multi; Q125, Q135

1. The Stop Multi is the same Eccles-Jordan configuration as the Start Multi.



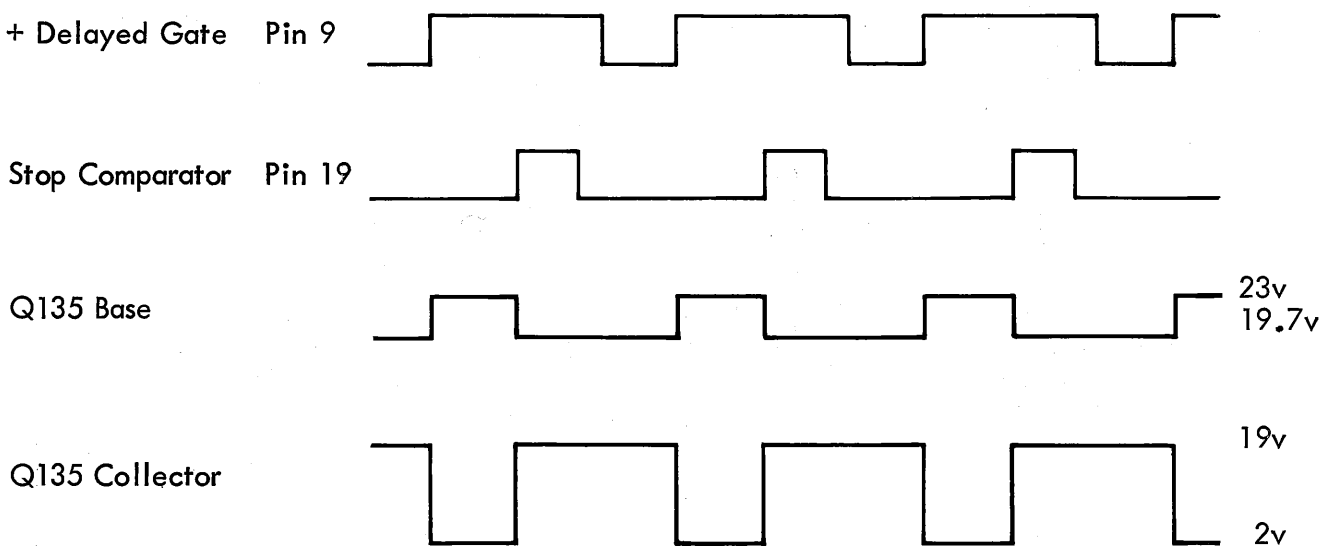
TYPE 6RIA MASTER GATE
STOP MULTIVIBRATOR

B-6RIA-0066
7-30-64 jg

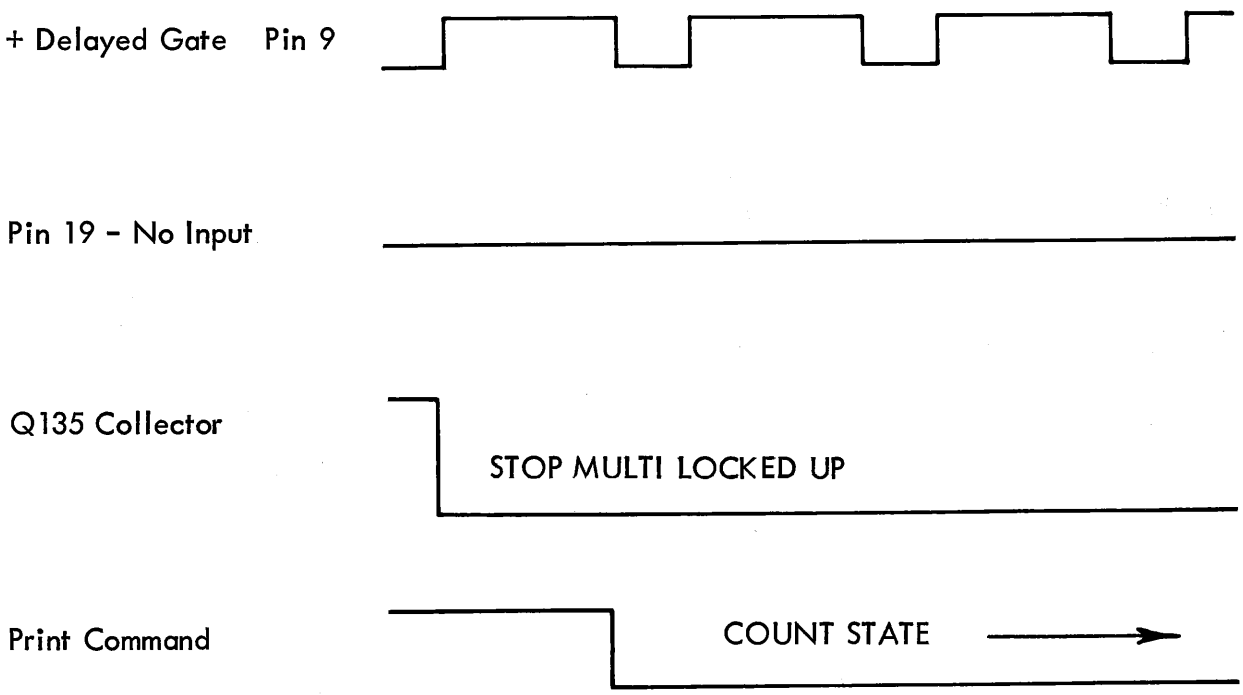
2. The Stop Multi is reset at the start of + Gate as the Start Multi with Q135 turning off and Q125 turning on.

   a. The step passes through C132 and D132 to lift Q135 base to cut off.

3. The output is taken from Q135 collector so as the Multi is reset (NOT STOP state), the input to the AND Gate drops to 2v (LOW state instead of HIGH as with the START Multi output).



4. When the Stop Comparator signal arrives on pin 19, the Multi switches with Q125 turning off and Q135 on.
5. The output at Q135 collector lifts to 20v.
   a. The AND Gate is closed -- the flow of clock pulses is stopped.
6. The STOP pulse also appears on pin 16.
   a. Passing through the RESOLUTION switch or the ÷10 circuit, the STOP pulse switches the Print Command to the DISPLAY state.
7. Two additional methods are used to assure an output from the Stop Multi.

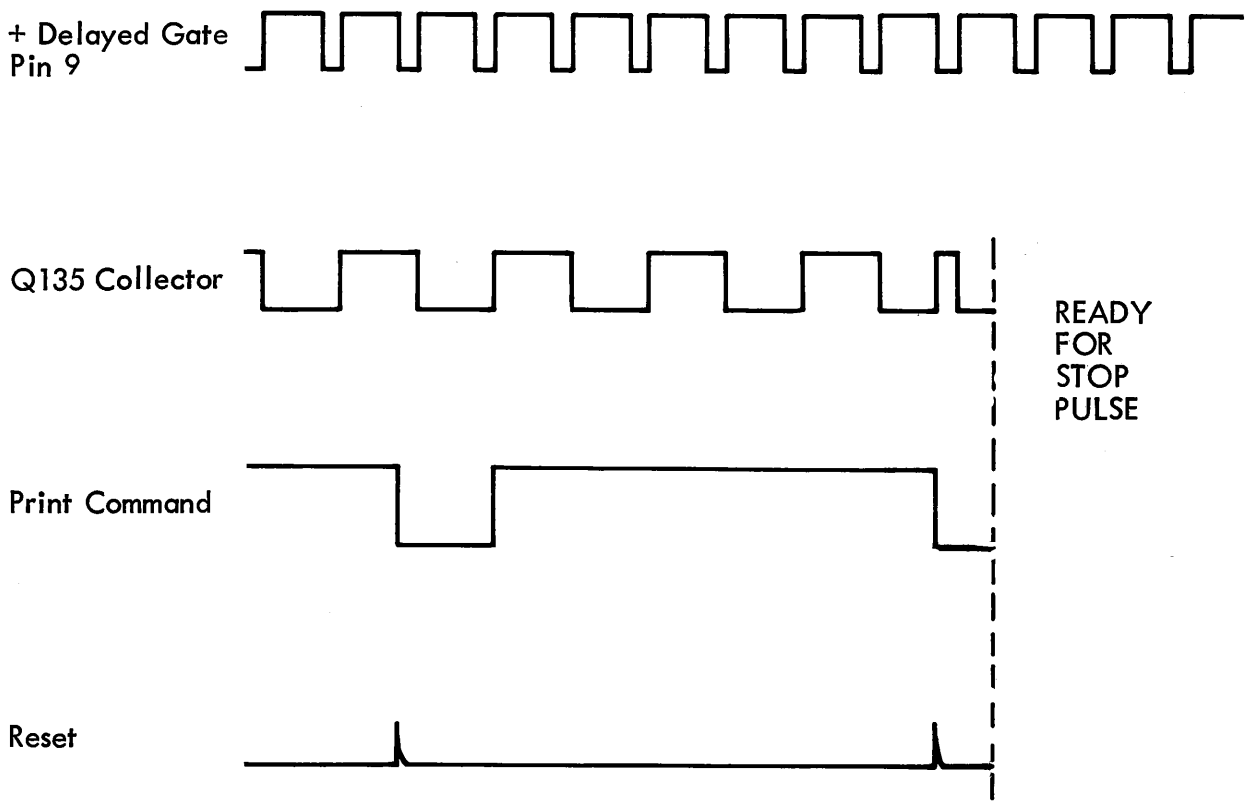


a. The Display Time Multi relies on the STOP signal from the Stop Multi to switch it to the (Print Command) Display State.

b. The 262 programmer relies on the Print Command to advance to the next measurement.

c. Should the 6R1A be set to measure voltage in a programed application, and the anticipated voltage did not exist in the equipment under test, no Stop signal would arrive from the Comparator.

d. The system could lock up.

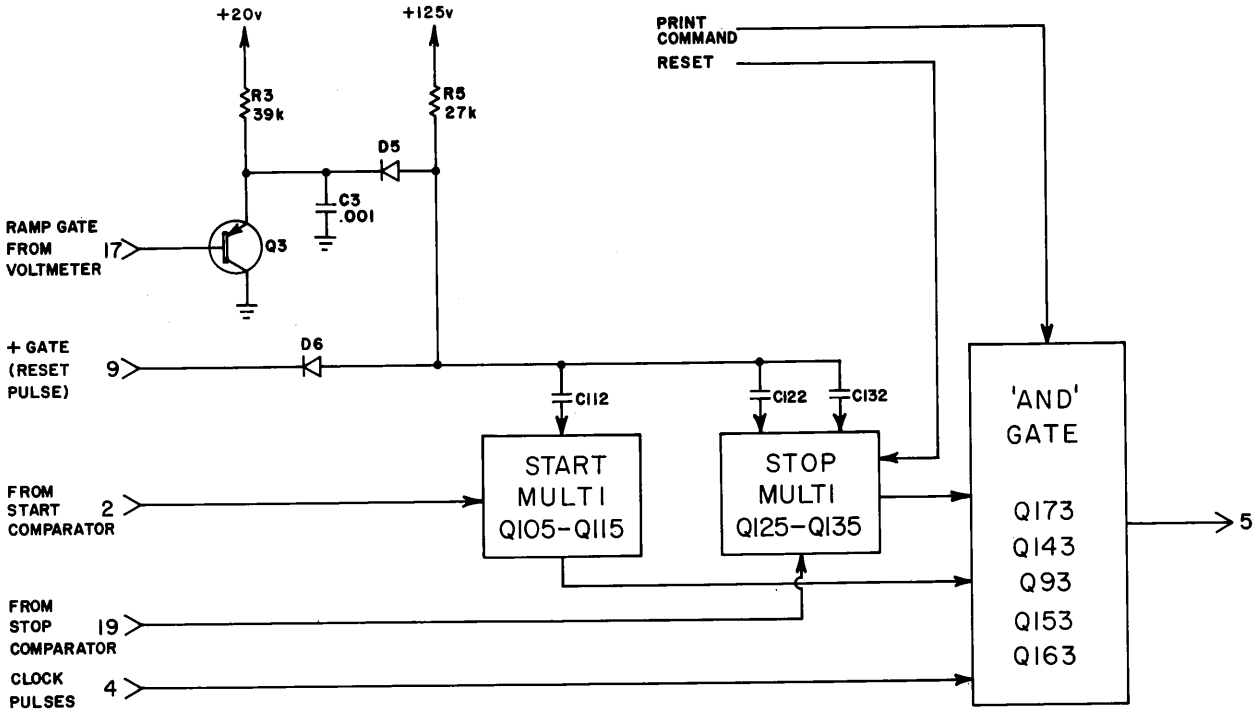


e. At the start of the next + Gate, the step will pass through C122, pull D122 into conduction and turn off Q125.

(1) D132 is back biased under this condition and is disconnected.

f. A stop pulse is generated to switch the Print Command to the Display State.

g. Under this condition (no Stop signals from the Comparator), the + Gate will reset the Stop Multi on one sweep and switch it to the STOP condition the next.



TYPE 6RIA MASTER GATE RESET CIRCUITRY

B-6RIA-0062
7-29-64 jg

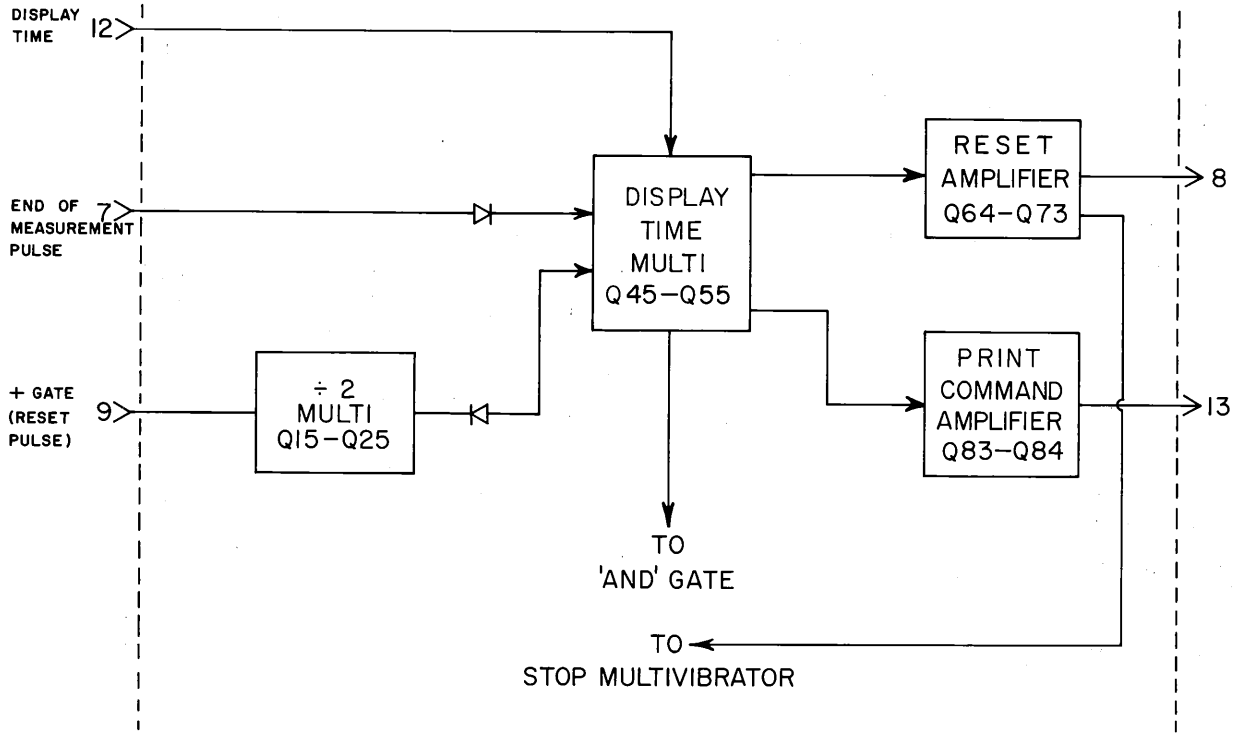
h. It is possible to catch the Stop Multi in its reset (or NOT STOP) state at the time when Print Command switches to Count.

i. In this case, a reset signal (generated by the Display-Time Multi) feeds through R74 to switch the STOP Multi to its STOP condition.

(1) This is a positive going step at the start of the Print Command Count condition.

j. Since the Print Command Count condition will always start with the end of sweep, the STOP Multi will now be in a condition to be reset (NOT STOP state) at the next + Gate.

J. Print Command Circuits Card



TYPE 6RIA MASTER GATE
PRINT COMMAND BLOCK

B-6RIA-0070
7-29-'64 jg

1. The Print Command Circuits supply the Print Command signal to the AND Gate, the Memories, and the Voltmeter Card.
   a. A reset pulse is also supplied to the ÷10, ÷1, 2, 5 and the count circuits.
2. Print Command Circuits of the Master Gate:
   a. ÷2 Multi; Q15, Q25.
   b. Display Time Multi; Q45, Q55.
   c. Reset Amplifier; Q64, Q73.
   d. Print Command Amplifier; Q83, Q84.

K. Print Command Block Logic

1. The Print Command waveform has two states.
   a. Count State: The logic level is LOW (0v at pin 13).
   b. Display State: The logic level is HIGH (20v at pin 13).
2. Occurrences during the Count Condition:
   a. A measurement is taken (or 10 measurements in AVERAGE OF TEN SWEEPS mode).
   b. Clock pulses pass the AND Gate.
   c. A Voltmeter Ramp is generated (see Voltmeter Card).
   d. If in Peak Memory mode (see Memories Card), memories will retain their charge.
3. Occurrences during the Display Condition:
   a. The count (taken during the count condition) is held in the nixie readout.
   b. The Voltmeter Ramp is inhibited from running up (see Voltmeter Card).

c. The Memory capacitors are allowed to discharge (see Memories Card, Peak Memory).

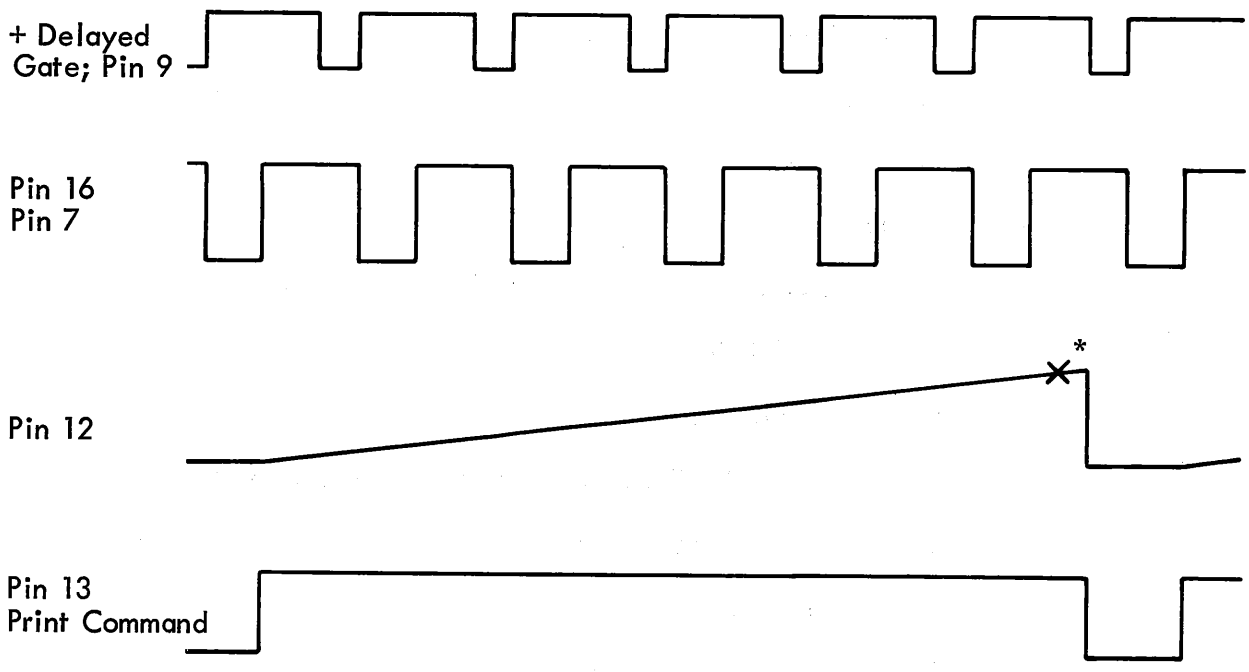
d. The Clock Pulses are prevented from passing the AND Gate.

4. Assume a condition during the Count State.

a. Resolution Switch is in the UNSCALED position.

b. The AND Gate is open and clock pulses are being counted.

5. The arrival of a signal from the STOP Comparator flips the STOP Multi.



6. The positive step at pin 16 passes through the RESOLUTION Switch to pin 7.

a. The signal at pin 7 is called "End of Measurement" pulse.

7. As the End of Measurements pulse reaches the Display Time Multi, the Multi flips -- the Print Command waveform goes to the Display State.

* Circuit is enabled.

8. After a time selected by the DISPLAY TIME control (50 msec to 5 sec), the Display Time Multi becomes enabled.

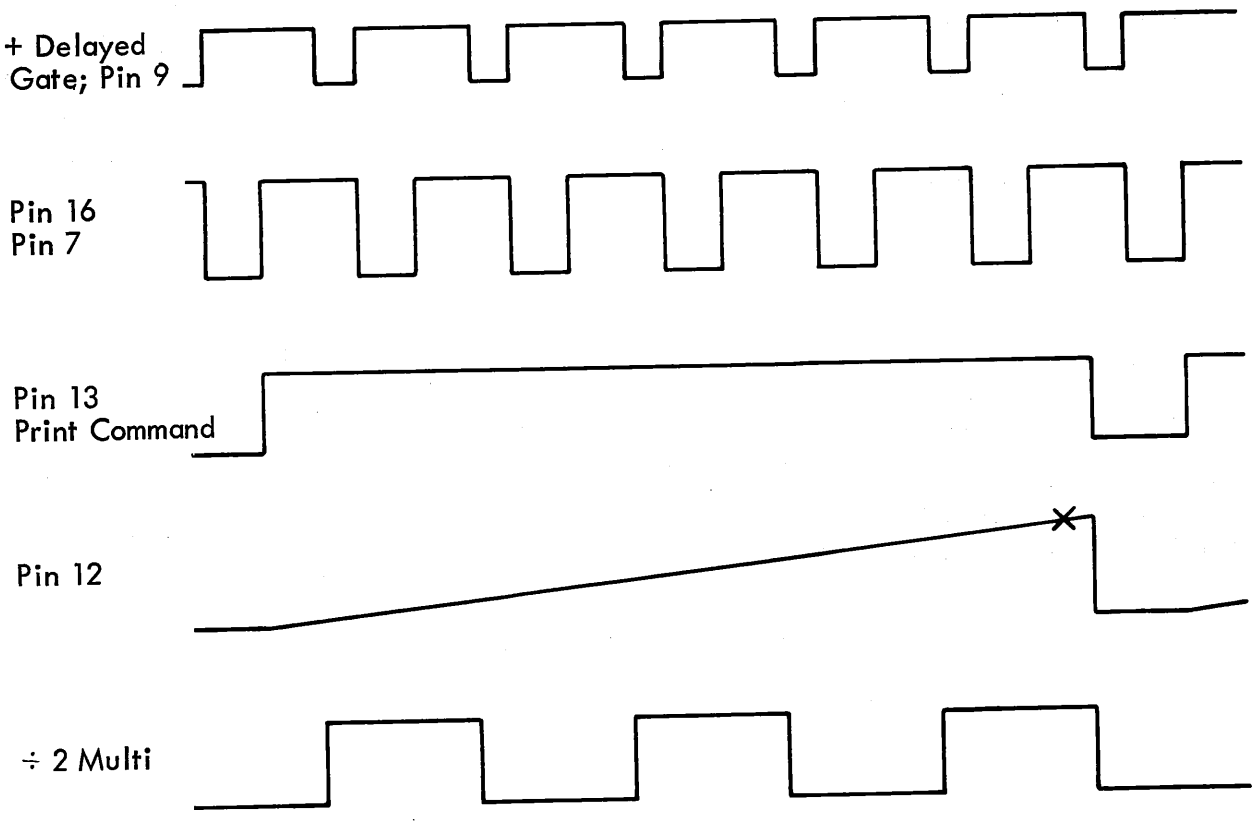
9. During the Display State, the ÷2 Multi flips with the arrival of each end of + Gate (negative step).

   a. The Multi divides by 2.

   b. The ÷2 Multi assures that at least one sweep occurs after count has been taken.

   c. This provides an opportunity for the Memories to become recharged (in Peak Memory Mode) before another count is taken.

   d. In AVG Mode, a change in vertical signal (such as in external programing) would require time for the Memories to charge to a new level.

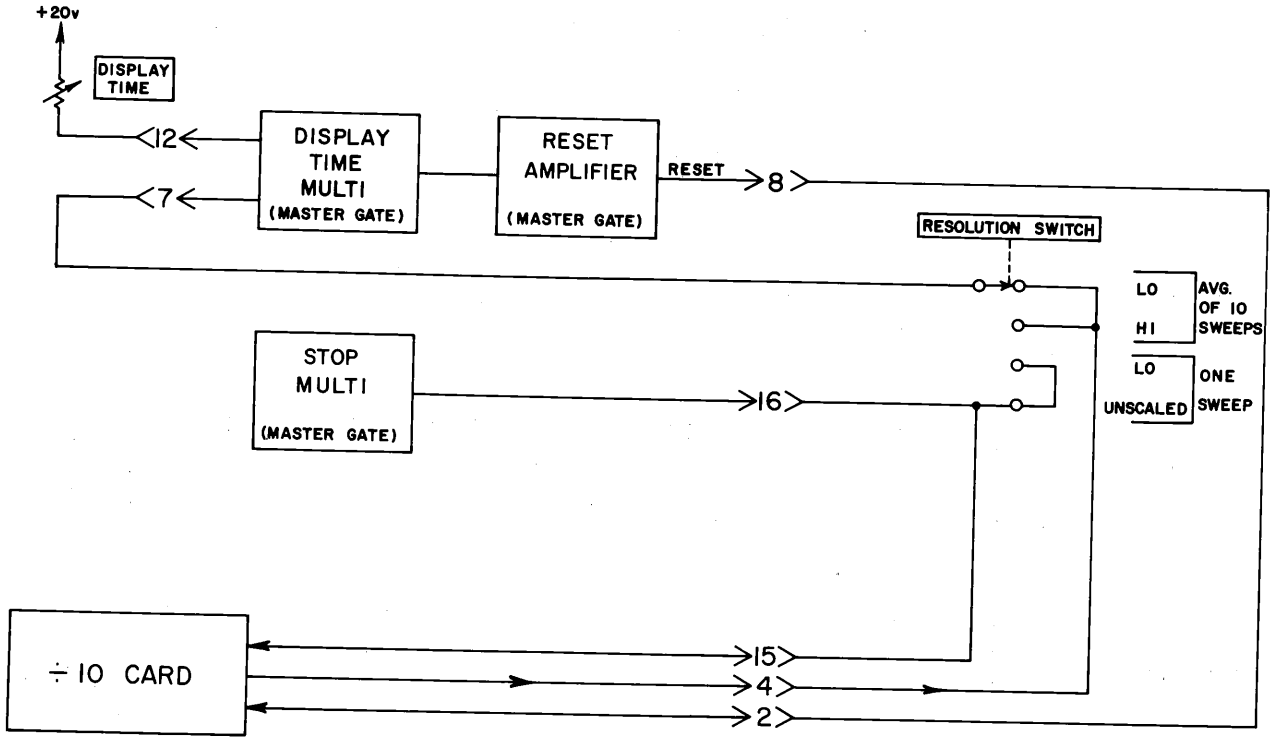


10. After the Display Time Multi has become enabled, the first flip of the ÷2 Multi that results in a negative pulse at its output will switch the Display Multi to its Count State.

11. In the AVERAGE OF TEN SWEEP mode of the RESOLUTION switch, the STOP pulse passes through the ÷10 Card before becoming the End of Measurement pulse at pin 7.

    a. Ten STOP pulses (not Sweep Gates) must be fed into the ÷10 Card before an End of Measurement Pulse reaches pin 7.

    b. The nixies count the total of the 10 measurements.



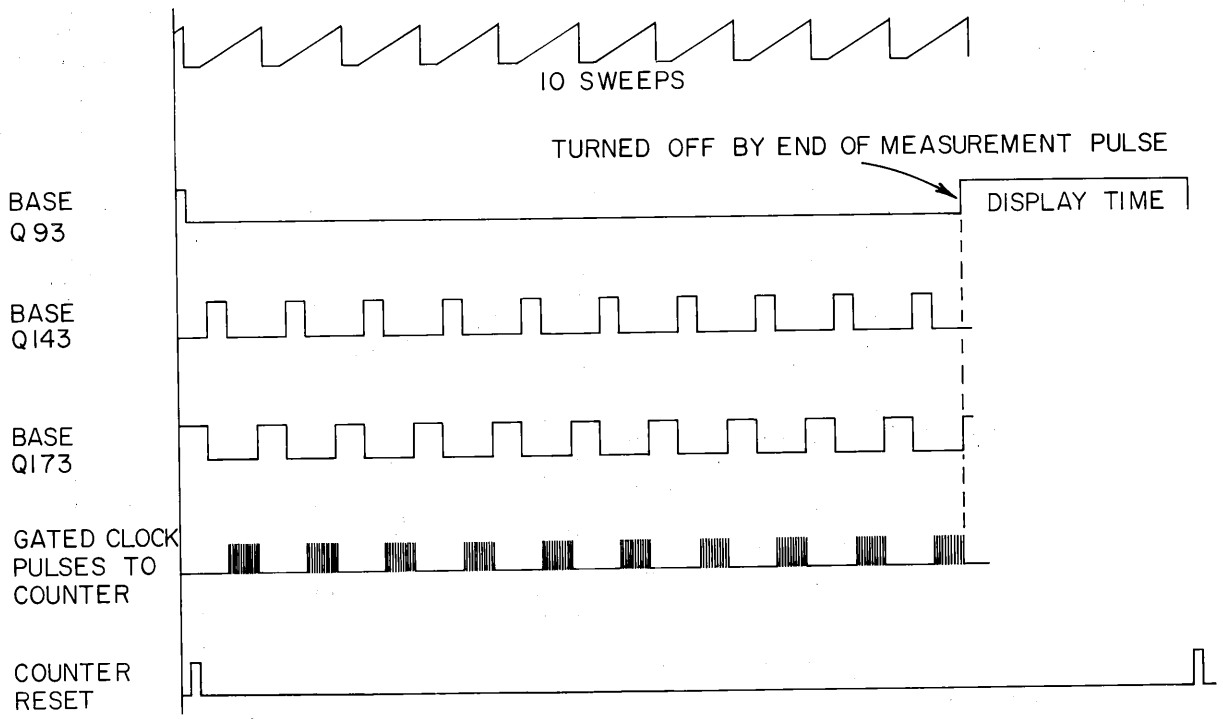
TYPE 6RIA MASTER GATE
AVERAGE OF 10 SWEEPS

B-6RIA-0073
8-6-64 jg

c. The Resolution Switch moves the decimal over to provide an average reading.

12. A holding signal (Negative Print Command) from the Print Command amplifier is fed to the ÷2 Multi.

a. The signal holds the Multi with its output LOW until the end of the Count State.



TYPE 6RIA MASTER GATE
RESOLUTION IN ÷10 MODE

B-6RIA-0125
5-20-64 jg

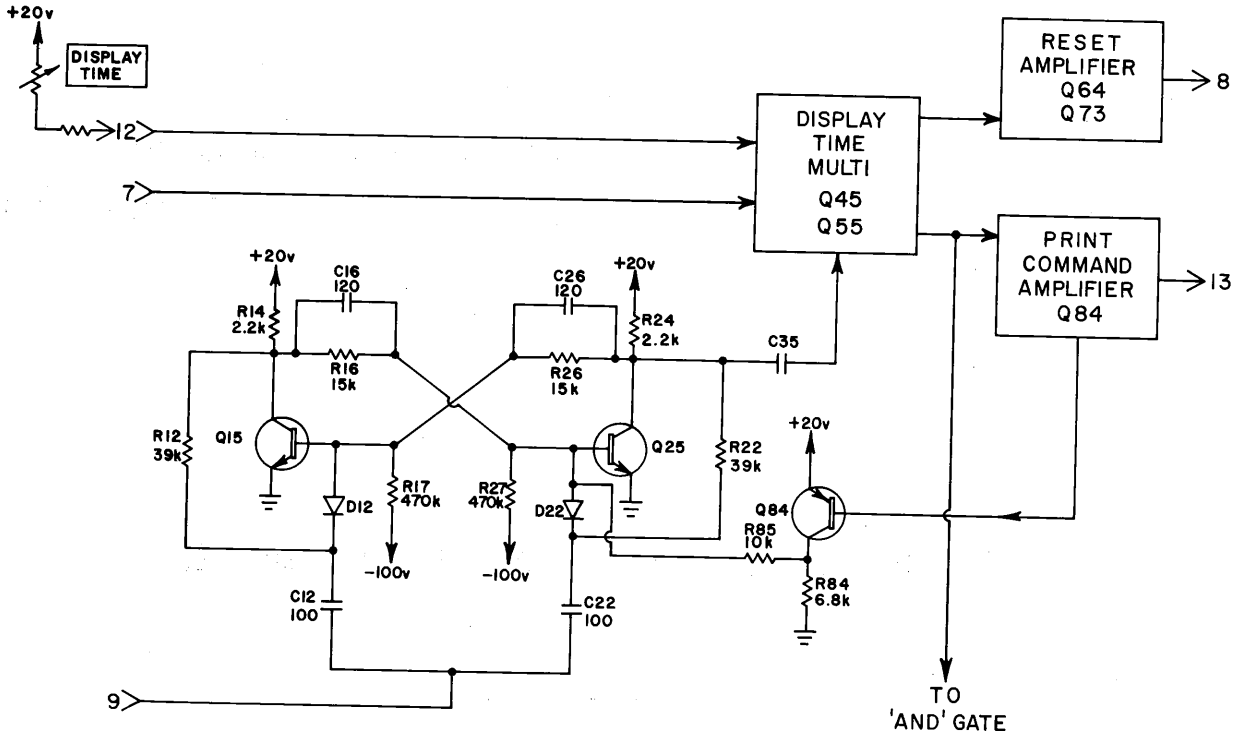
b. In this condition, two + Gate waveforms (trailing edge) are required before the ÷2 Multi can again switch the Display Multi to the count condition.

L. ÷2 Multi; Q15, Q25

1. The ÷2 Multi provides a 2:1 count down from the + Gate.

a. The Multi is triggered by the trailing edge of the + Gate.

b. The output (negative step) flips the Display Multi into the Count State -- after the Display Multi has been enabled by the DISPLAY TIME control.



TYPE 6RIA MASTER GATE
÷2 MULTI

B-6RIA-0075
8-8-'64 jg

2. The ÷2 Multi is a transistorized Eccles-Jordan bistable multi.

   a. Since only negative pulses will pass through the steering diodes to flip the multi, it is a ÷2 device.

   b. The transistors are 151-103, 2N2219 silicon NPN transistors.

   c. The steering diodes (D12 and D22) are 152-075 germanium diodes.

3. During the Count State, the minus Print Command waveform lifts R85 to 20v.

a. The Multi is held with Q25 saturated and Q15 cut off.

b. Q25 base, .6v.

c. Q25 collector, 0v.

d. Q15 base, -1.6v.

e. Q15 collector, 17v.

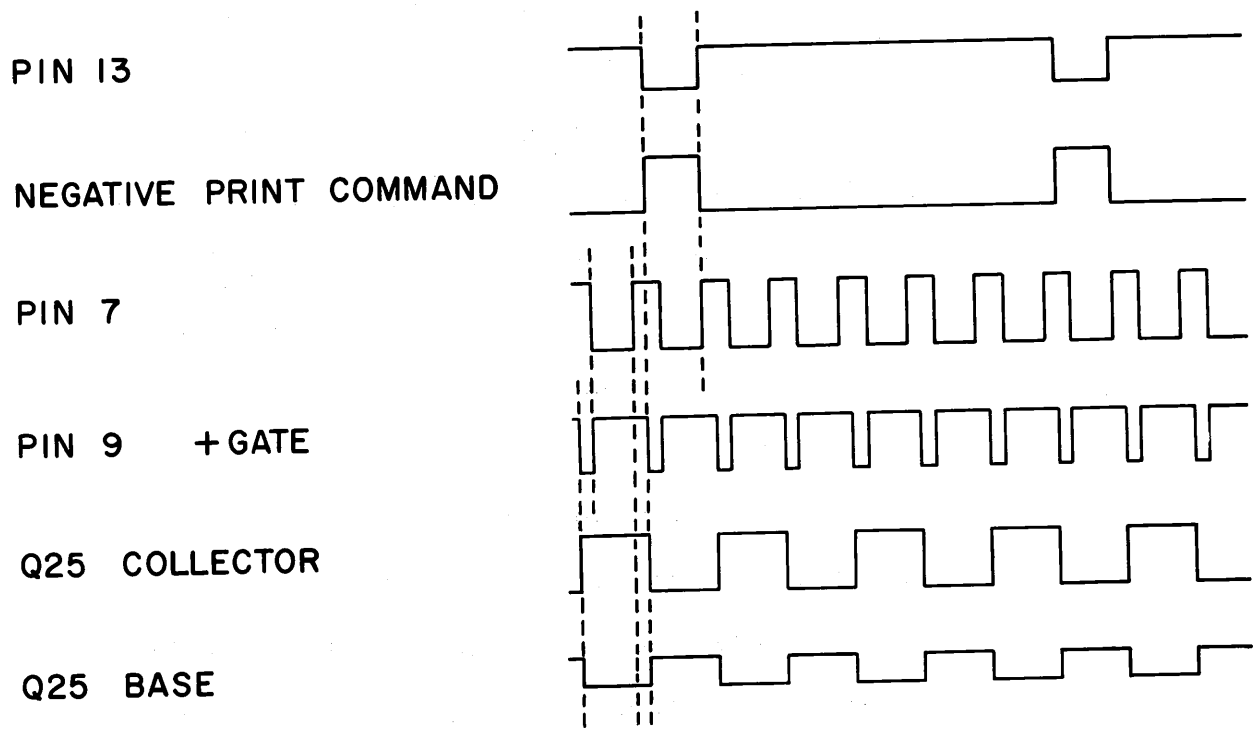
f. Q25 base is limited at .6v by the base-emitter junction.

g. D22 is slightly forward-biased but not enough to conduct.

h. D12 is back-biased 18.6v.

i. If a negative step from the trailing edge of a + Gate arrives during the Count State, the negative step pulls D22 into conduction but cannot cut off Q25.

(1) Q84 collector holds Q25 base up, keeping Q25 saturated.



TYPE 6RIA MASTER GATE
WAVEFORM NO. 10

B-6RIA-0076
(A)
8-27-'64 ms

4. At the end of Count Condition, negative Print Command drops R84 to ground.
   a. Q25 is still saturated although its base will drop a few millivolts.
      (1) The cross coupled divider pulls the base towards 14v.
5. The arrival of the first end of + Gate will flip the Multi.
   a. The negative step (trailing edge of + Gate) is differentiated in C22.
   b. The pulse pulls down on Q25 base, flipping the Multi.
   c. Q25 collector rises to 17v.
      (1) Collector level at cut off is set by the cross coupled divider.
6. The positive output step does not effect the Display Multi.
7. With Q25 cut off and Q15 saturated, D22 is back biased by 18.6v and D12 is back biased about .3v.
8. The next end of + Gate passes through C12, forward biasing D12 and pulls down on Q15 base.
   a. The Multi flips as Q15 cuts off and Q25 conducts.
   b. Q25 collector drops to ground.
9. The negative output step passes through C35.
   a. If the Display Time Multi has been enabled by the Display Time control, the Multi will flip to the Count State.
   b. If the Display Time Multi is not enabled, another two + Gates are required to again flip the ÷2 Multi through a complete cycle.

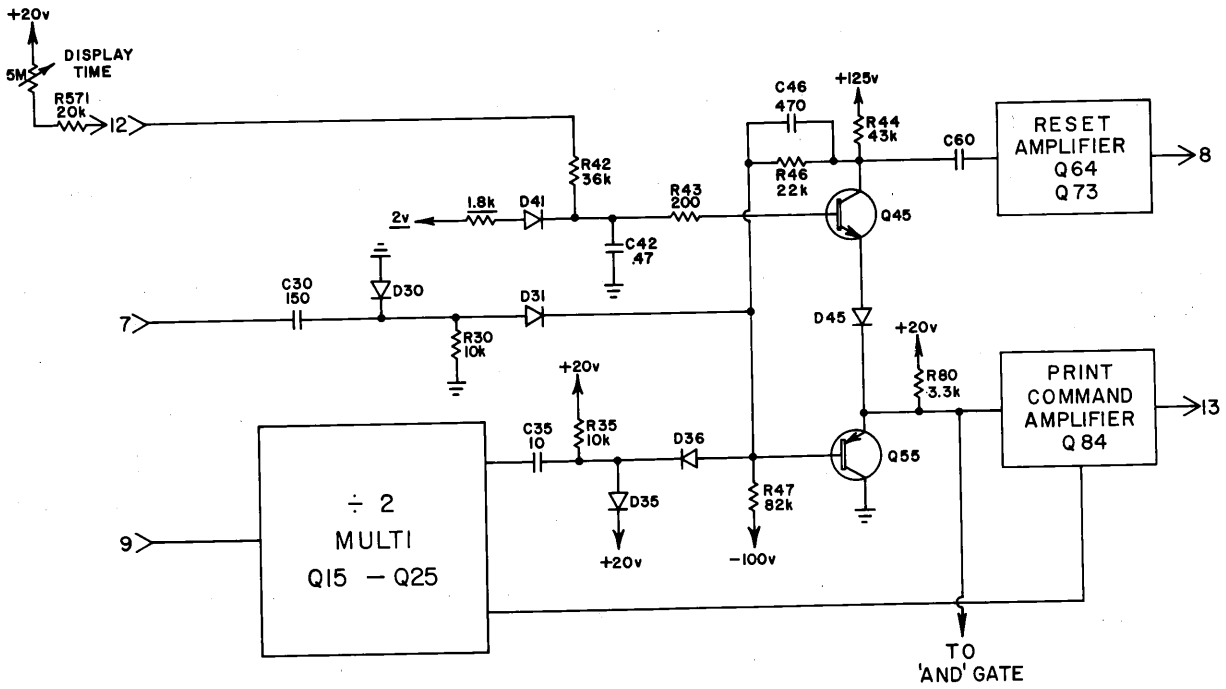
c. The first negative pulse, so generated in the ÷2 Multi after the Display Time Multi is enabled, will flip it to the Count State.

10. As Print Command goes to its Count State, the holding voltage is again placed on R85 to keep Q25 in conduction for Count State duration.

M. Display Time Multi; Q45, Q55

1. The Display Time Multi supplies the Print Command waveform to the AND Gate, the Memories, Voltmeter and Limit Light Driver.

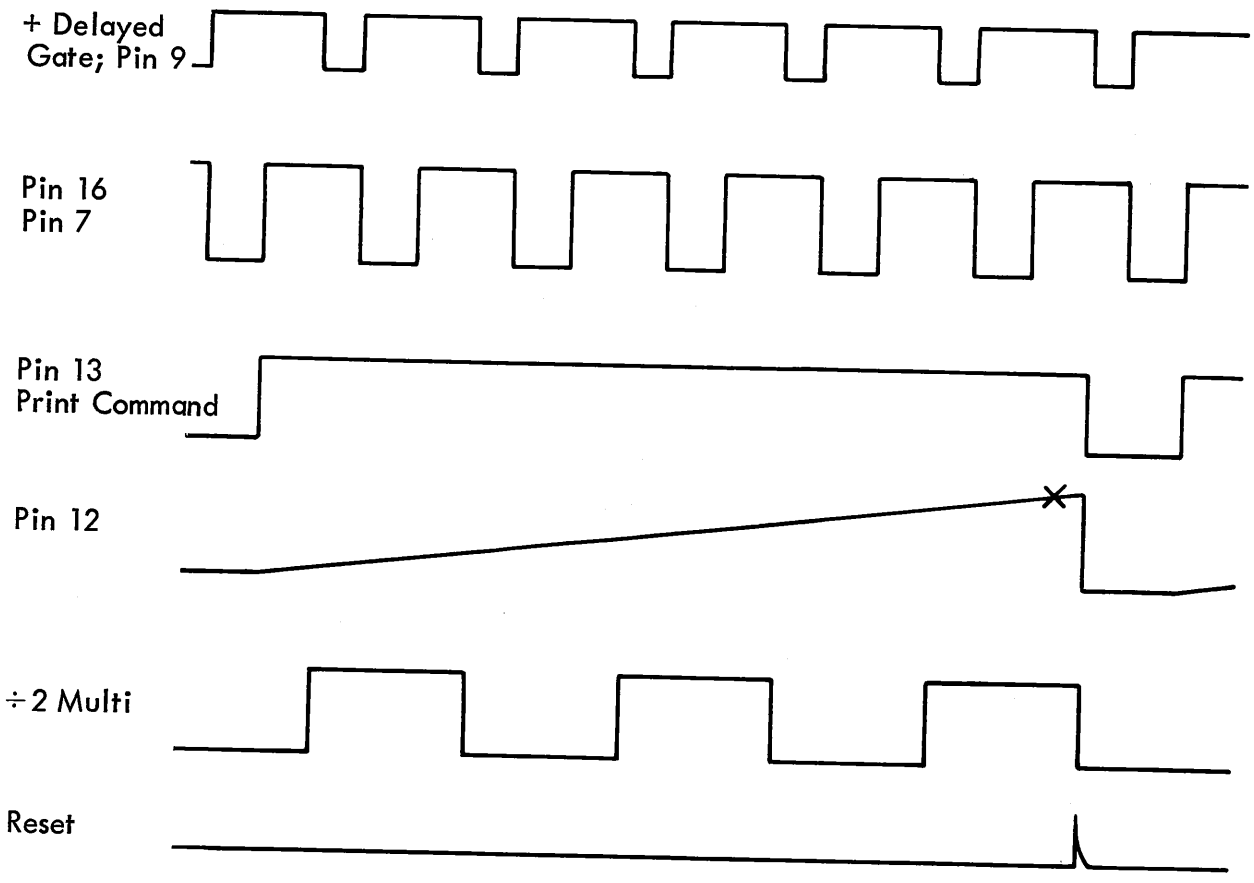
2. A Reset pulse is also generated that is used by the STOP Multi, the ÷1, 2, 5 Card, the ÷10 Card and the Counters.



TYPE 6RIA MASTER GATE
DISPLAY TIME MULTI

B-6RIA-0077
8-10-'64 jg

3. The circuit is a bistable Multi using complimentary NPN, PNP transistors.
   a. Q45 is a 151-103, 2N2219 silicon NPN transistor.
   b. Q55 is a 151-071, 2N1305 germanium PNP transistor.
   c. D30, D31, D35 and D36 are 152-675 germanium diodes.
   d. D41 and D45 are 152-141, 1N3605 silicon diodes.
4. During the count state, both transistors are saturated.
   a. All elements of both transistors are at or near ground.
5. The End of Measurements pulse passes through C30 (differentiated) forward biasing D31 and lifts Q55 base.
   a. The End of Measurements pulse is a positive going 17v step at pin 7 (3v to 20v).



b. The pulse originates as the output of the STOP Multi (through pin 16).

c. It passes through the RESOLUTION switch.

d. In the ONE SWEEP POSITIONS (RESOLUTION switch), the Stop pulse passes directly to pin 7.

e. In the AVERAGE OF TEN SWEEP positions, the Stop Pulse is divided by 10 in the ÷10 Card. (See Print Command Logic section).

6. The pulse cuts off Q55.

a. Robbed of emitter current as Q55 cuts off, Q45 turns off.

b. D30 is a DC restorer diode for C30.

7. As Q45 cuts off, its collector pulls Q55 base up to 20.6v.

a. The divider, R44, R46, R47, pulls Q55 base toward 25v, but is caught at 20.6v by D35 and D36.

8. Q55 emitter raises to 20v as current through R80 closes.

a. This forms the Print Command waveform during the Display State.

9. As Q45 cuts off its base rises toward 20v.

a. During Count condition, Q45 base current (saturated) is supplied through D41.

b. As the transistor cuts off its base rises as C42 charges through the DISPLAY TIME control.

c. The control has a range of from 50 msec to 5 sec.

d. As Q45 base rises, the emitter will follow with junction leakage (D45 is cut off with its cathode at 20v).

10. At the end of Count state, the holding signal was released from the ÷2 Multi.

    a. As the Multi flips (with + Gate trailing edges), a negative step appears at its output at the end of every other end of + Gate.

11. The ÷2 Multi output step (differentiated sharply in C35) pulls down on Q55 base.

    a. D35 disconnects momentarily.

12. The negative pulse forward biases Q55 for the pulse duration.

13. As the pulse pulls down Q55 emitter it <u>may</u> forward bias D45 and flip the Multi.

    a. If (as C42 charges) Q45 base and emitter junction is high enough (about 18v), the pulse on Q55 emitter will forward bias D45.

    b. When Q45 emitter reaches this potential, it is said to be "enabled".

    c. If D45 does become forward biased, the emitter current will turn on Q45.

    d. As Q45 collector drops, it pulls Q55 base down -- Q55 conducts.

        (1) C46 is a speed-up cap to overcompensate divider, R46, R47.

    e. Q45 emitter current is suppled through Q55, D45.

    f. The Multi switches with both transistors at saturation.

14. Q55 emitter drops to ground forming the output Print Command waveform in the Count Condition.

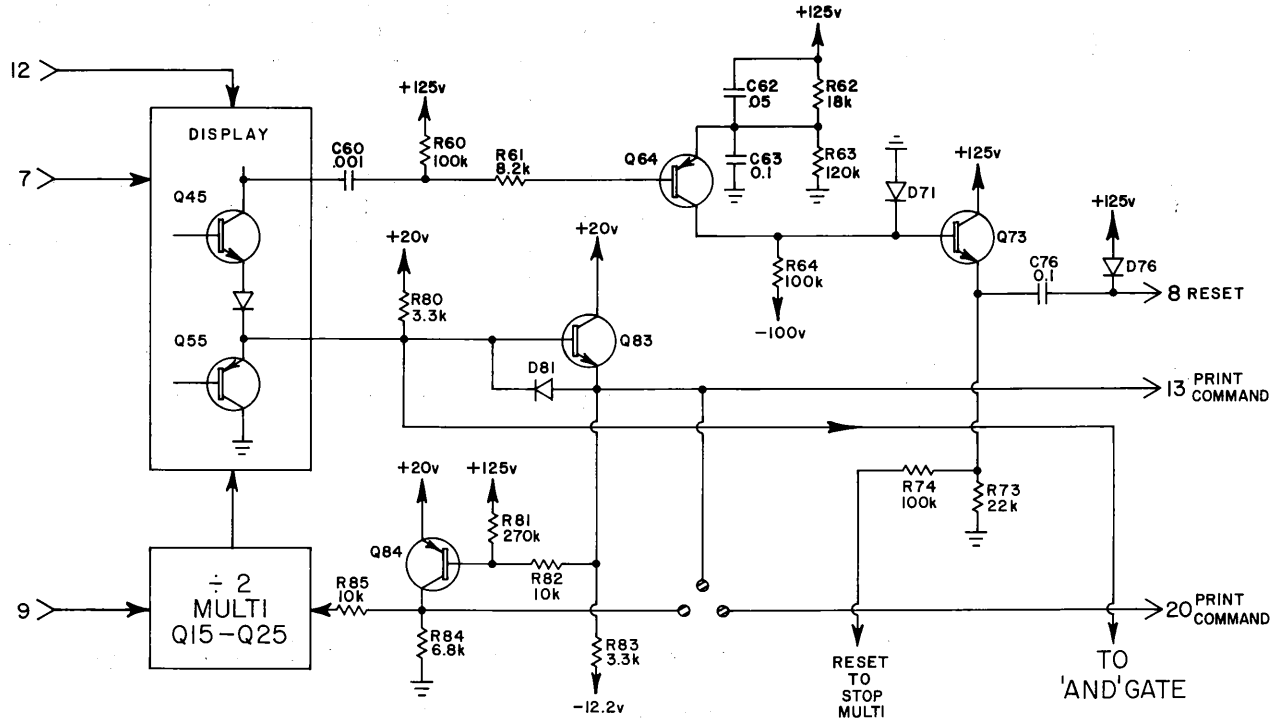
15. If, on the arrival of a negative step from the ÷2 Multi, Q45 emitter is not high enough to allow D45 to become forward biased, the Multi will not flip -- the circuit will wait until Q45 is enabled.

16. As the Multi flips to its Count State, a negative Reset pulse is formed at Q45 collector that passes through C60 (differentiated) to the Reset Amplifier.

17. The Print Command waveform is taken from Q55 emitter to feed the AND Gate and the Print Command Amplifier.

M. Print Command Amplifier; Q83, Q84

1. The Print Command Amplifier provides an emitter follower output for the Print Command waveform.



TYPE 6RIA MASTER GATE
RESET AND PRINT COMMAND AMPLIFIERS

B-6RIA-0079
8-12-'64 jg

a. An amplifier-inverter (Q84) supplies the negative Print Command holding signal to the ÷2 Multi.

b. Negative Print Command is also available at pin 20 (when connected by a strap on the Master Gate Card).

2. The circuit uses two transistors and a diode.

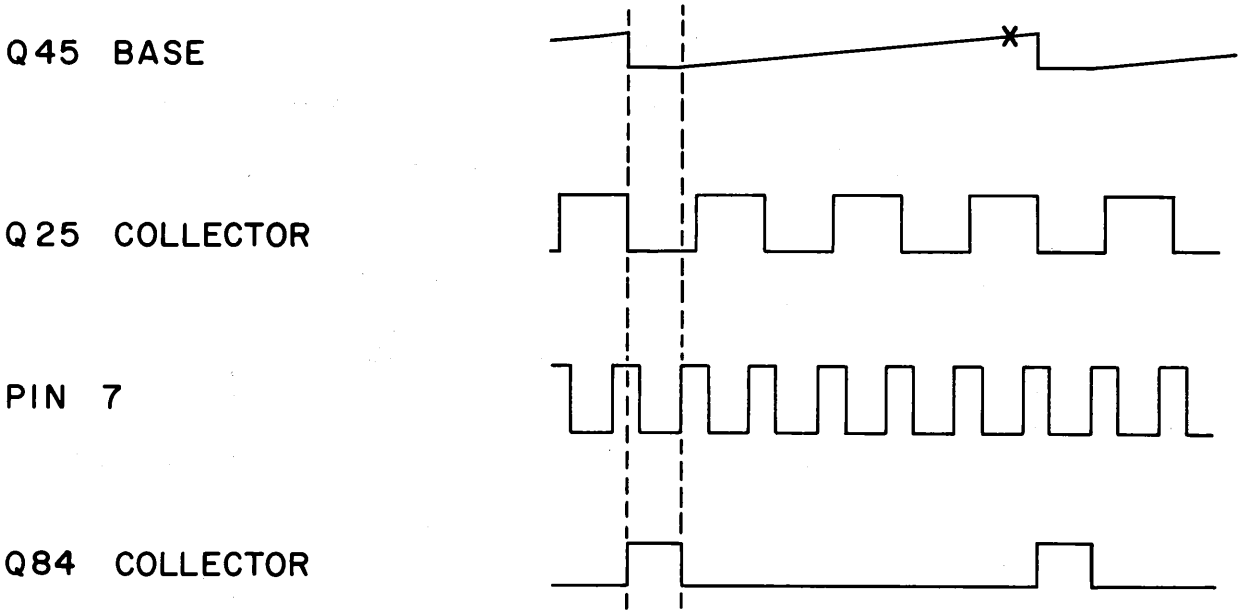
a. Q83 is a 151-069, 2N1304 germanium NPN transistor.

b. Q84 is a 151-071, 2N1305 germanium PNP transistor.

c. D81 is a 152-075 germanium diode.

3. During the Count Condition, the input waveform from the Display Time Multi is at ground.

a. About 6 ma flows through R80.



a. 3.7 ma flows through R83.

b. 2 ma flows through R82 with about 1.6 ma Q84 base current.

c. 1 ma is required in the Voltmeter Card.

5. Q84 is saturated, with all elements clamped at the 20v emitter supply.

6. With Q84 collector at 20v, about 5 ma of collector current flows.

   a. 3 ma through R84.

   b. 2 ma through R85 supplies the holding signal that keeps the ÷2 Multi from operating during the Count Condition.

7. At the end of the Count Condition, the Print Command waveform at the Display Multi output raises to 20v.

   a. Q83 emitter pulls up to 19v; but not to saturation.

   b. The 9.5 ma through R83 all flows through Q83.

8. As Q83 emitter rises, R81 pulls Q84 base up to cut off (22.5v).

9. Q83 collector drops to ground removing the hold signal from the ÷2 Multi.

   a. About 1v of ÷2 Multi switching waveform appears at Q84 collector.

10. When the Print Command waveform again goes to its Count Condition, Q83 base is dropped to ground.

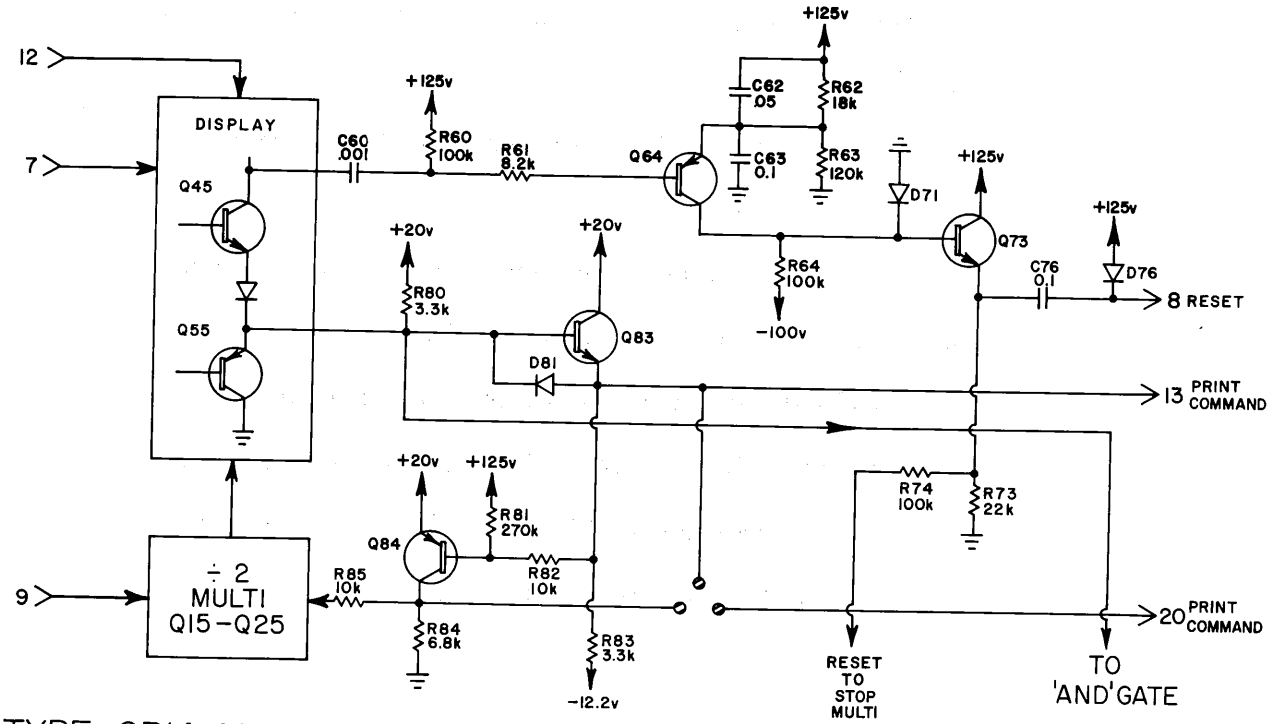
    a. Q83 will cut off as only about .7 ma is available to pull down Q83 emitter and charge stray capacitance.

    b. D81 becomes forward biased supplying the required current from the Display Time Multi.

11. Three terminals provide a method of connecting (soldered jumper) either plus or minus Print Command to pin 20.
    a. Pin 20 is connected to the External Programing jack on the rear panel.
    b. Plus Print Command is connected at the factory (prior to SN 1180 no connection was made).

O. Reset Amplifier; Q64, Q73

1. The Reset Amplifier provides a Reset Pulse to reset the ÷10, ÷1, 2, 5 and the counters.
    a. A Reset signal is also used to assure proper reset position of the Stop Multi at the beginning of the Count State (see Stop Multi).



TYPE 6RIA MASTER GATE
RESET AND PRINT COMMAND AMPLIFIERS

B-6RIA-0079
8-12-'64 jg

2. The Reset pulse occurs when Print Command goes to its Count Condition.

3. The circuit uses two transistors, and two diodes.

   a. Q64 is a 151-093, 2N2043 germanium PNP transistor.

   b. Q73 is a 151-096, 2N1893 silicon NPN transistor.

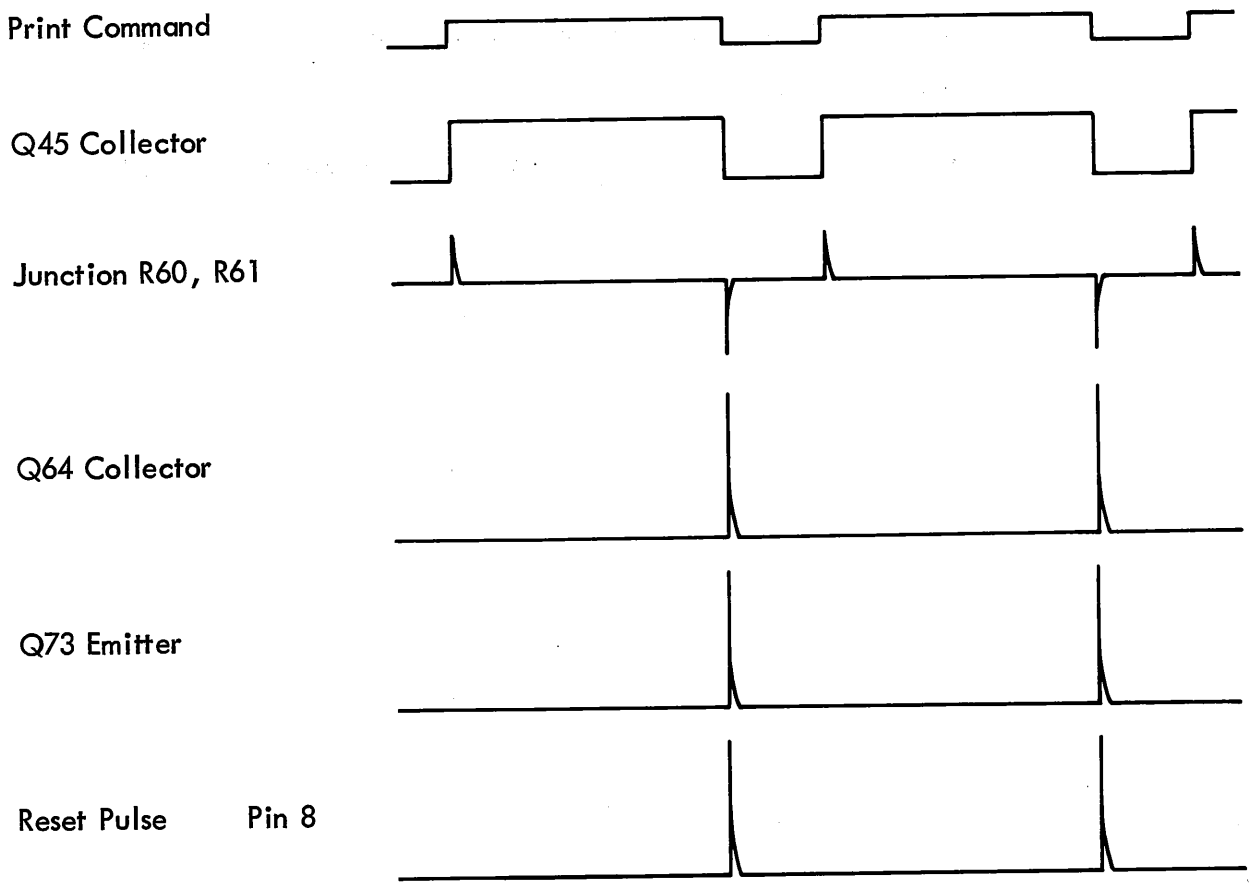
   c. D71 and D76 are 152-107 silicon diodes.

4. Quiescently, Q64 is cut off.

   a. Divider R62, R63 sets Q64 emitter at 109v.

   b. The base sets at 125v.

   c. The base emitter junction is back biased by 16v.



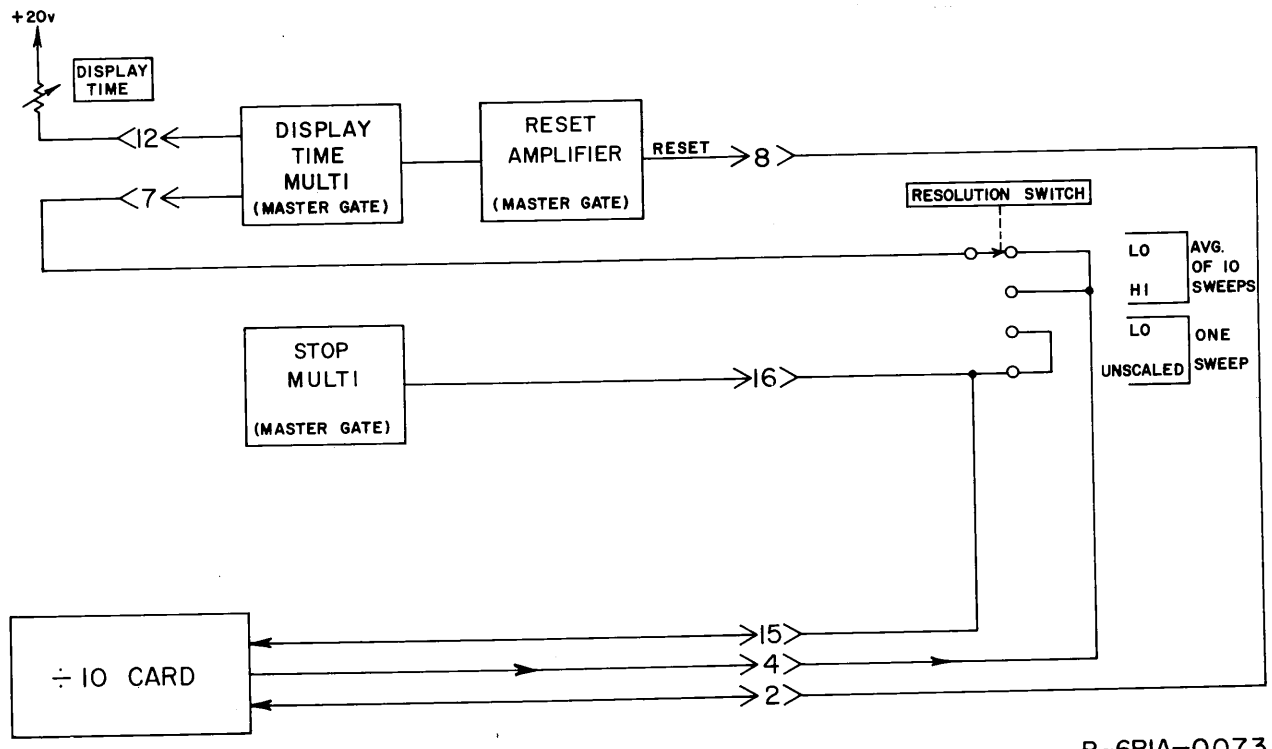
5. Q64 collector is held at .6v by 1 ma through D71.
6. Q73 is cut off, back biased .6v.
7. As the Display Multi switches, positive and negative spikes appear at Q64 base.
   a. Only the negative spikes cause conduction.
8. With each negative spike (start of Count Condition), Q64 collector pulls up to 108v as D71 disconnects.
9. As Q73 turns on, its emitter pulls up to 108v.
10. D76 maintains a 125v charge on C76.
11. The 108v pulse at Q73 emitter disconnects D76 and maintaining the charge on C76, appears at pin 8 as a pulse from 125v to 233v.
12. C63 provides emitter degeneration bypassing for the duration of the Reset pulse.
13. C62 supresses a 50 mc oscillation that occurs as Q64 turns off.

X. ÷10 CARD

A. The ÷10 circuits divide the number of STOP pulses (Stop Multi output*) by 10 before they are applied to the Display Time Multi*.

1. The ÷10 circuits function in the AVERAGE OF 10 SWEEPS position of the RESOLUTION switch.

a. The binaries actually divide whenever the circuit receives an input -- the output is selected in the AVERAGE OF 10 SWEEPS only.



TYPE 6RIA
AVERAGE OF 10 SWEEPS

B-6RIA-0073
8-6-64 jg

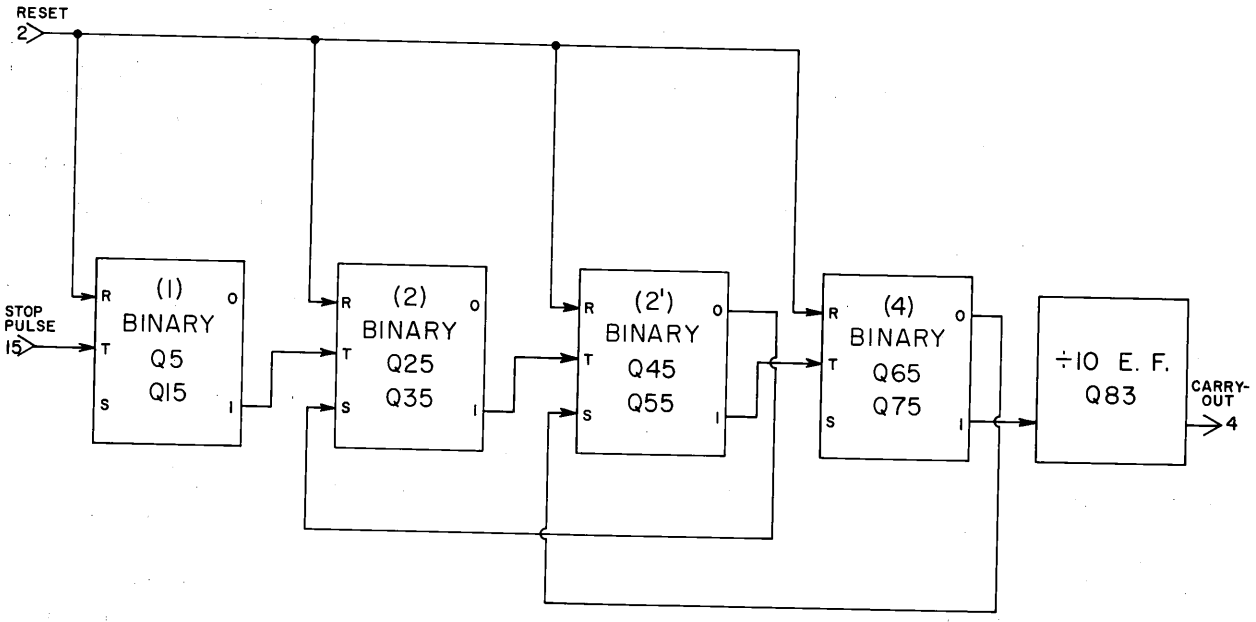
* See Master Gate Card.

2. Print Command count condition lasts for 10 sweeps.
3. The nixies count the total clock pulses that pass for 10 sweeps.
4. The Resolution Switch moves the decimal over to provide the average reading.

B. The ÷10 circuit consists of four binary counters and an output EF.

1. "1" Binary; Q5, Q15.
2. "2" Binary; Q25, Q35.
3. "2'" Binary; Q45, Q55.
4. "4" Binary; Q65, Q75.
5. Output EF, Q83.

C. Block Diagram



TYPE 6RIA ÷10 CARD
BINARY BLOCK DIAGRAM

B-6RIA-0094
8-24-'64 dl

D. Inputs

1. STOP Pulses from the Stop Multi on the Master Gate Card at pin 15.
   a. An 18v positive going step.
2. A Reset pulse from the Reset Amplifier on the Master Gate Card.
   a. A 108v positive going pulse from 125v to 233v.
   b. The pulse occurs at the start of the Print Command count condition.
   c. The pulse resets all four binaries to their "0" state.

E. Outputs

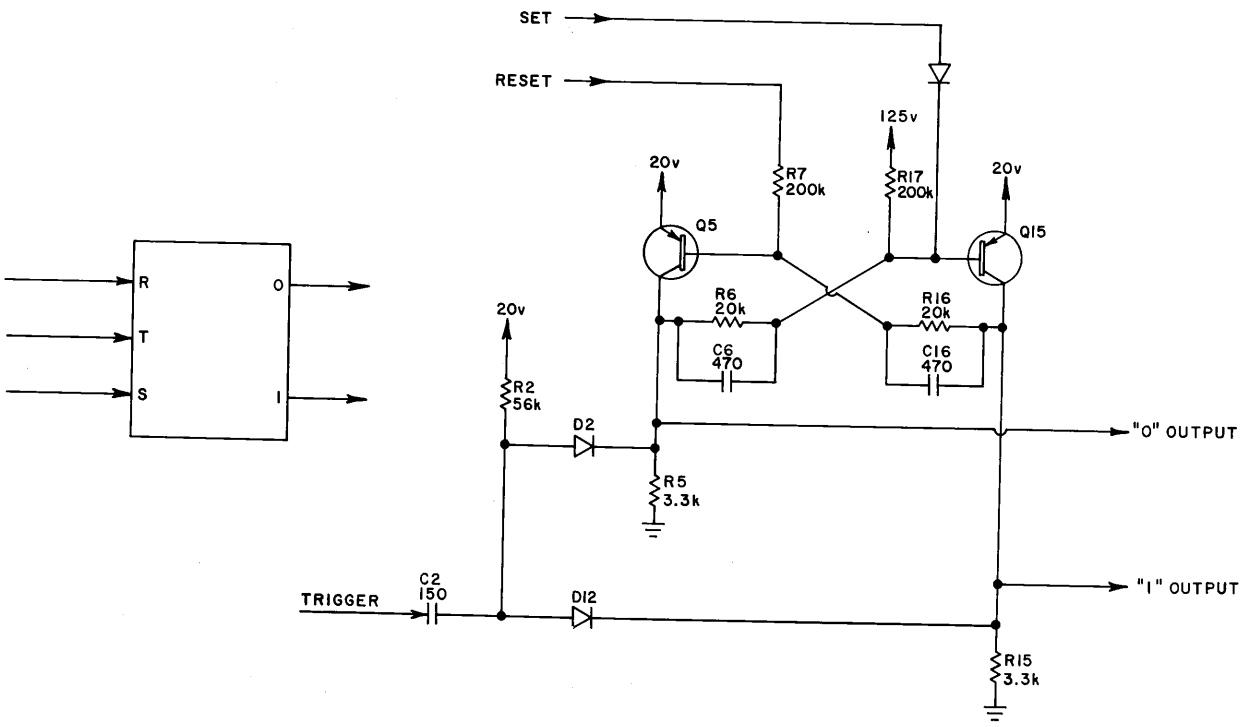
1. The only output is the carry-out from the binaries.
   a. A 17v positive going step (from 3v to 20v).
   b. The step passes through the RESOLUTION switch (in the AVERAGE OF 10 SWEEPS position) to become the End of Measurements pulse to pin 7 of the Master Gate.

F. Block Logic

1. Four binary multivibrators comprise the 10:1 countdown circuit.
2. At the start of the Print Command count condition, a Reset pulse arrives on pin 2.
3. All binaries reset to zero.
4. As STOP pulses arrive on pin 15, the binaries count down until coincident with the tenth stop pulse; an output pulse occurs.
5. Q83, the output Emitter Follower, isolates the interconnecting cable and socket capacitance from the Multi output.

G. The Basic Binary

1. The basic binary can be identified with its binary symbol.



TYPE 6RIA ÷10 CARD
BASIC BINARY

B-6RIA-0095
9-3-'64 dl

2. The "0" output is taken from the collector of the left hand transistor.

   a. In the ÷10 circuits, only the 2' and the 4 Binaries have an output taken from their 0 output.

3. The "1" output is taken from the collector of the right hand transistor (Q15 in the basic binary).

4. The binary has a carry-out when a positive step occurs at an output.
5. The binary is in its "0" state when the right hand transistor (Q15) is on and the left hand transistor (Q5) is off.
6. The binary is in its "1" state when the Q15 is off and Q5 is on.
7. The binary has a carry-out from its 1 output when it switches from its 1 state to its 0 state -- a positive step occurs at Q15 collector.
   a. Carry-out from the Binary 1 outputs are used to trigger the next Binary and in the 4 Binary, as carry-out from the ÷ 10 Card.
8. The Binary has a carry-out from its 0 output when it switches from its 0 state to its 1 state -- a positive step occurs at Q5 collector.
   a. In the ÷10 Card, carry-out from the 0 output is used only to feedback Set pulses.
9. A Reset input connects to Q5 base.
   a. All four Binaries receive Reset pulses.
10. A Set input connects to Q15 base.
   a. Only the 2 and 2' Binaries receive Set pulses.
11. A Reset pulse switches the binary to its 0 state -- Q15 on, Q5 off.
12. A Set pulse switches the binary to its 1 state -- Q15 off, Q5 on.
13. A Trigger must be a positive going step.
14. The trigger, differentiated in C2 feeds through a steering diode, D2 or D12, to flip the Multi.

H. System Logic

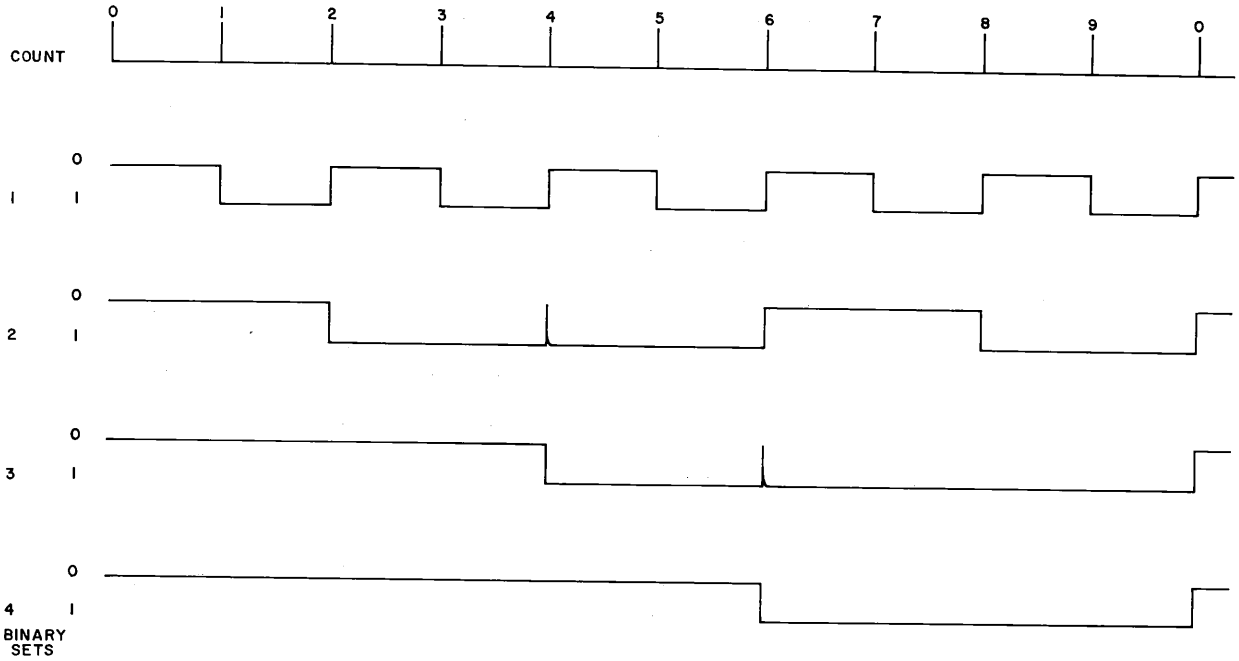
1. A four stage binary counter provides the 10:1 countdown.
   a. Normally a four-stage binary produces an output pulse for each 16 input pulses*.
   b. Feedback from the third to the second binary and from the fourth to the third modifies the count to provide the 10:1 countdown.
2. The binary stages are labeled "1" Binary, "2" Binary, "2'" Binary, and "4" Binary**.
3. Each binary has three possible inputs and two outputs.
   a. Inputs include trigger (T), Set (S), and Reset (R).
   b. Outputs are 1 amd 0.
   c. A Reset Pulse switches the binary to its 0 state.
      (1) Reset occurs only at the start of Print Command count condition.
   d. A Set Pulse switches a binary to its 1 state.
      (1) Set is the result of feedback from another Binary.
   3. A trigger pulse will result in the next successive output.
      (1) If in the 0 state, a trigger will switch the binary to its 1 state.
      (2) If in the 1 state, a trigger will switch the binary to its 0 state.
   f. A binary has a carry-out from its 1 output only when it <u>leaves</u> its 1 state.
4. At the start of Print Command Count Condition, a Reset pulse arrives at pin 2.

* See 6R1A Manual, Page 4-15 for comparison charts.

** The Language and Symbology of Digital Computer Systems, RCA.

a. The Reset pulse switches all four binaries to their 0 state.

b. The binaries may or may not require resetting.



TYPE 6RIA ÷10 CARD
BINARY RELATIONSHIPS

B-6RIA-0098
9-7-'64 dl

5. The first STOP pulse (Trigger) on pin 15 switches the 1 Binary to its 1 state.

   a. The binary has an output (positive going step) from its 1 output only when it leaves its 1 state, therefore, it has no carry-out from its 1 state at this time.

6. The Binary State as a result of the first trigger:

   1 Binary, 1

   2 Binary, 0

   2' Binary, 0

   4 Binary, 0

1 = LOW STATE

0 = HIGH STATE

PULSE NUMBER	BINARY SET			
	1 (1)	2 (2)	3 (2')	4 (4)
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
	0	1	1	0
5	1	1	1	0
6	0	0	0	1
	0	0	1	1
7	1	0	1	1
8	0	1	1	1
9	1	1	1	1
10 (0)	0	0	0	0

TYPE 6RIA ÷10 CARD
÷10 BINARY STATES

B-6RIA-0097
9-3-'64 dl

7. The second trigger (STOP pulse) switches the 1 Binary to its 0 state.

   a. The 1 Binary now has a carry-out.

8. The carry-out (positive going step) switches the 2 Binary to its 1 state.

9. Binary states as a result of the second trigger:

   1 Binary, 0

   2 Binary, 1

   2' Binary, 0

   4 Binary, 0

10. The third trigger switches the 1 Binary to its 1 state.

    a. There is no carry-out to the 2 Binary.

11. Binary states as a result of the third trigger:

    1 Binary, 1

    2 Binary, 1

    2' Binary, 0

    4 Binary, 0

12. The fourth trigger switches the 1 Binary to its 0 state.

    a. The carry-out to the 2 Binary switches it to its 0 state.

    b. As the 2 Binary switches to its 0 state (leaving its 1 state), it has a carry-out to the 2' Binary.

    c. The 2' Binary switches to its 1 state.

    d. As the 2' Binary leaves its 0 state, it has a carry-out from its <u>0 output</u>.

    e. The carry-out from the 2' Binary is fed back to the Set input to the 2 Binary.

    f. The 2 Binary switches to its 1 state.

13. The Binary state as a result of the fourth trigger:

    1 Binary, 0

    2 Binary, 1

    2' Binary, 1

    4 Binary, 0

14. The fourth trigger pulse, therefore, results in a transistional state that is immediately switched by feedback to the state shown in step 13.

15. The fifth trigger switches the 1 Binary to its 1 state.

    a. As there is no carry-out from the 1 Binary, there is no other change.

16. Binary state as a result of the fifth trigger:

    1 Binary, 1

    2 Binary, 1

    2' Binary, 1

    4 Binary, 0

17. The sixth trigger switches the 1 Binary to its 0 state.

    a. Carry-out from the 1 Binary switches the 2 Binary to its 0 state.

    b. Carry-out from the 2 Binary flips the 2' Binary to its 0 state.

    c. Carry-out from the 2' Binary flips the 4 Binary to its 1 state.

    d. As the 4 Binary leaves its 0 state, its 0 output has a carry-out through feedback to the 2' Binary Set input.

    e. The 2' Binary is immediately switched to its 1 state.

        (1) 2' Binary has a carry-out from its 0 output but does not feed back to the 2 Binary*.

18. Binary states as a result of the sixth trigger:

    1 Binary, 0

    2 Binary, 0

    2' Binary, 1

    4 Binary, 1

19. Again, feedback caused the binaries to pass through a transitional state that resulted in the state shown in step 18.

* See Page 10-14 for explanation.

20. The seventh trigger flips the 1 Binary to its 1 state.

    a. No carry-out from the 1 Binary -- no other change.

21. Binary states as a result of the seventh trigger:

    1 Binary, 1

    2 Binary, 0

    2' Binary, 1

    4 Binary, 1

22. The eigth trigger switches the 1 Binary to its 0 state.

    a. Carry-out switches the 2 Binary to its 1 state.

    b. There is no carry-out from the 2 Binary so no other change.

23. Binary states as a result of the eigth trigger:

    1 Binary, 0

    2 Binary, 1

    2' Binary, 1

    4 Binary, 1

24. The ninth trigger flips the 1 Binary to its 1 state.

    a. No carry-out -- no other change.

25. Binary states as a result of the ninth trigger:

    1 Binary, 1

    2 Binary, 1

    2' Binary, 1

    4 Binary, 1

26. The tenth trigger flips the 1 Binary to its 0 state.

    a. Its carry-out flips the 2 Binary to its 0 state.

b. The 2 Binary carry-out flips the 2' Binary to its 0 state.

c. 2' Binary carry-out flips the 4 Binary to its 0 state.

d. The 4 Binary has a carry-out.

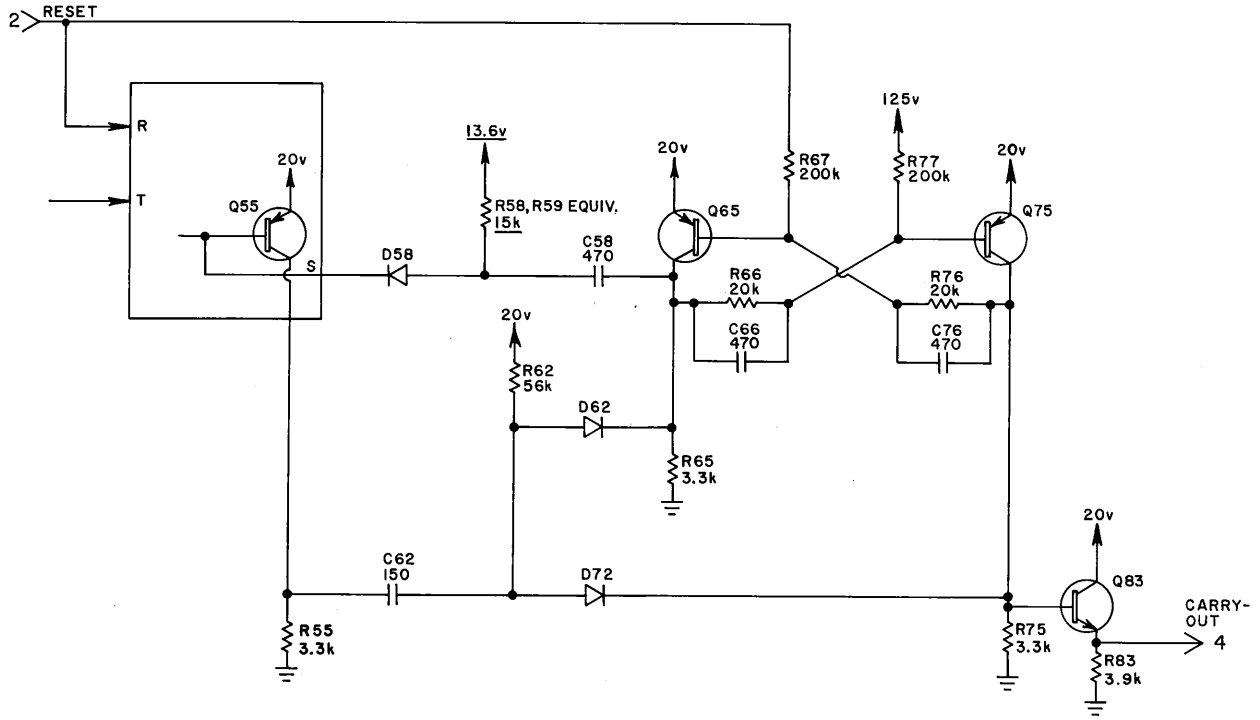
27. The tenth STOP pulse, therefore, results in an output at pin 4.

a. The carry-out is an 18v positive going step.

b. The step becomes the End of Measurements pulse that switches the Print Command to its Display State*.

c. Although the binaries function whenever STOP pulses are received, the output (through pin 4) is selected by the RESOLUTION switch in the AVERAGE OF 10 SWEEPS position.

I. The Binaries (4 Binary Illustrated; Q65, Q75) and Output EF, Q83



TYPE 6RIA ÷10 CARD
"4" BINARY AND OUTPUT E. F.

B-6RIA-0096
9-4-'64 dl

* See Master Gate Card.

1. The Binaries are transistorized Eccles-Jordon multivibrators.
   a. They are collector triggered by steering diodes to provide each binary with its 2:1 countdown.
2. All Binaries use 151-071, 2N1305 germanium PNP transistors.
3. The diodes are 152-075 germanium diodes.
4. The Reset Pulse input through Pin 2 is clamped by D76 (Master Gate Card) at 125v.
   a. This 125v supplies the cross coupled divider (R67, R76 in the 4 Binary).
   b. The Reset Pulse is a 108v positive going pulse about 35 μsec wide.
5. The transistor bases set at about 30v when cut off and at 19.7v* when conducting.
6. The Reset Pulse pulls up on the base of the left hand transistor cutting it off.
   a. Through multi action, the right hand transistor turns on.
   b. Since all Binaries are reset simultaneously, the reset action overrides any carry-out that might trigger the next Binary.
   c. The Reset Pulse leaves all Binaries in their 0 state.
7. The collectors swing from about 3.5v cut off to 20v conducting.
   a. The cross coupling divider and .3 ma through the steering diode sets the collector level at cut off.
   b. The transistors saturate when ON, setting the collector level at 20v.

* Assuming 20v decoupled is 20v.

8. The ON steering diode has about .3 ma static current.
9. The OFF steering diode is back biased by about 16v.
10. The trigger pulse, differentiated in C62, passes through the ON diode, through the cross-coupling capacitor (C66 or C76 in the 4 Binary) to lift the base of the conducting transistor, flipping the multi.
11. The SET pulse is taken from Q65 collector (the 0 output of the Binary).
    a. The pulse is fed back through C84 and D58 to the 2' Binary.
12. R58, R59 equivalent sets D58 anode at 13.6v.
    a. When conducting, Q55 base sets at 19.7v.
    b. D58 therefore is reverse biased by 6v.
13. When the 4 Binary flips to its 1 state (leaving its 0 state), the 0 output (Q65 collector) raises 17v.
    a. The positive step coupled through C58 forward biases D58.
    b. The pulse lifts Q55 base cutting it off and flipping the multi (2' Binary).
14. When the sixth trigger arrives, the binary count becomes 0, 0, 0, 1*.
15. Feedback from 4 Binary switches 2' Binary to its 1 state.
    a. Since the 2' Binary will have left its 0 state, it will have a carry-out from its 0 output.
    b. This carry-out might be expected to feed back to the 2 Binary, switching it to its 1 state.
    c. This feedback does not occur, however.

* See Binary States Chart, Page 10-8.

d. As the 2' Binary switched to its 0 state (transient condition at the arrival of the sixth pulse), a 17v negative step occurred at the 2' Binary's 0 output.

e. An 8v charge (approximately) is placed on the coupling cap (same circuit configuration as C58, D58).

f. The coupling diode is back-biased by about 16v.

g. When (through feedback action from the 4 Binary) the 2' Binary switches to its 1 state, the carry-out from its 0 output cannot overcome the back bias on the coupling diode.

(1) The T.C. for the charge on the coupling cap is 6 μsec.

h. The Set feedback pulse does not reach the 2 Binary -- it remains in its 0 state.

16. Carry-out to the RESOLUTION switch is taken from Q75 collector through the Output EF, Q83.

a. The output is a 17v positive going step at pin 4 (3v to 20v).

XI. ÷1, 2, 5 CARD (SCALER)

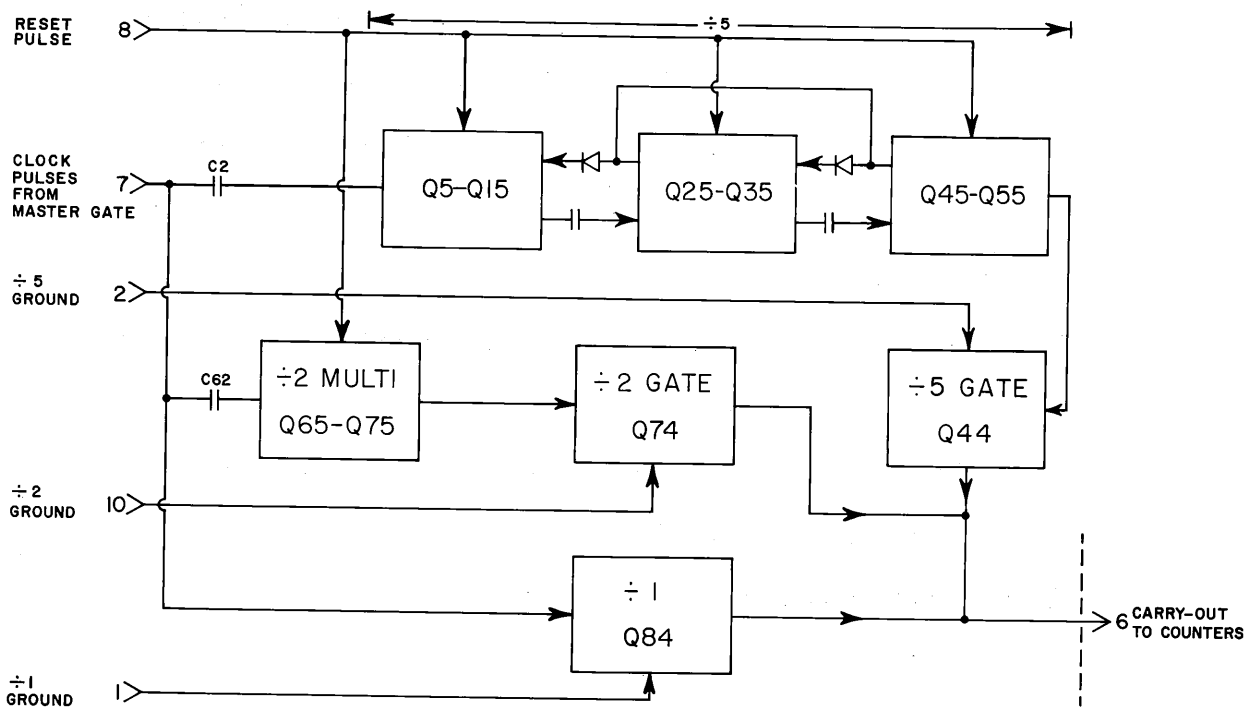
A. The ÷1, 2, 5 circuits divide the number of Clock Pulses received from the Master Gate before they are applied to the Counters.

1. The "Divide-By" circuits provide a method by which the 6R1A counters can compute the actual value of a measurement when a VOLTS/CM control or TIME/CM control position is changed.
2. The ÷1, 2, 5 circuits are used when voltage measurements are being made.
3. The ÷1, 2, 5 circuits are used when making time measurements with a Sampling system.
4. Time Measurements with a real time plug-in do not require the use of the ÷2 and ÷5 circuits.

B. Circuits that comprise the ÷1, 2, 5 card:

1. ÷1 Gate, Q84.
2. ÷2 Multi; Q65, Q75.
3. ÷2 Gate, Q74.
4. ÷5 Multi's; Q5, Q15, Q25, Q35, Q45, Q55.
5. ÷5 Gate, Q44.
6. All transistors on the card are 151-054 germanium PNP, 2N2957 transistors.
7. All diodes are 152-075 germanium diodes.

C. Block Diagram



TYPE 6RIA ÷1,2,5 CARD
BLOCK DIAGRAM

B-6RIA-0082
6-25-'64 jg

D. Inputs

1. A 108v reset pulse (from 125v to 233v) at pin 8 from the Master Gate.

   a. The pulse occurs at the start of the Print Command count condition.

   b. It resets all the binary circuits to zero.

2. 20v Gated Clock pulses from the Master Gate (negative going, 20v to 0v).

   a. The pulses appear during the Print Command Count State.

b. They are turned on by the Start Multi* and turned off by the Stop Multi*.

c. The Clock pulses are fed to the inputs of the three Divide-By circuits.

3. A ground at pin 10 turns on the ÷2 Gate.

4. A ground at pin 1 turns on the ÷1 Gate.

5. A ground at pin 2 turns on the ÷5 Gate.

E. Outputs

1. The only output is the Gated clock pulse train to the Counters.

a. The output pulses may be divided by one, two, or five depending on which of the output Gates is grounded.

b. This is a positive clock train, 0v to 20v.

F. Block Logic

1. Gated Clock Pulses from the Master Gate are fed, via pin 7, to the inputs of all three Divide-By circuits.

a. The clock pulses are inverted in the ÷1 circuit.

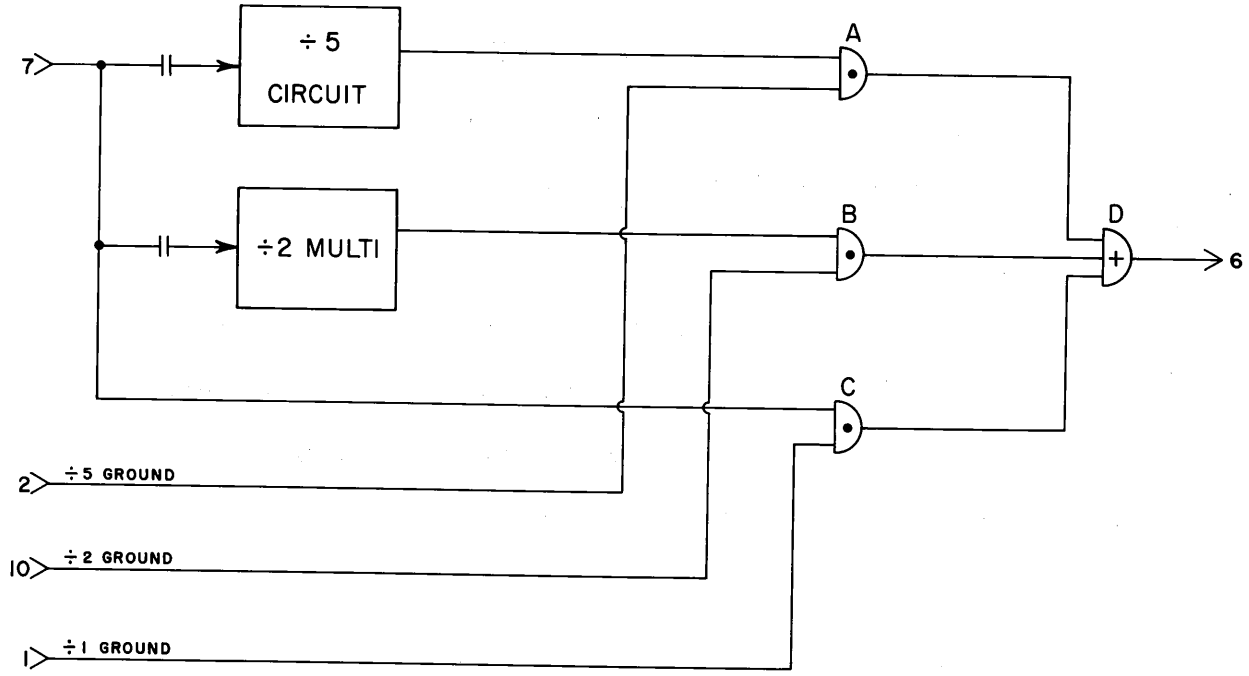
b. The clock pulses pass through a 2:1 count-down in the ÷2 circuit.

c. The ÷5 circuit is a 5:1 count-down.

2. Although the count-down (or divide) operation occurs simultaneously in both the ÷2 and ÷5 circuits, logic gates determine which of the three outputs will appear at pin 6.

* See Master Gate Card.

3. When clock pulses are present (at the inputs to Gates A, B, or C) AND a ground is present, an output is present.



TYPE 6RIA ÷1,2,5 CARD
OUTPUT GATE LOGIC BLOCK

B-6RIA-0083
8-17-'64 dl

4. Whenever an output is present at the output of the Gate A, Gate B, OR Gate C, Gate D has an output.

G. System Logic

1. Although the vertical sensitivity as it is applied to the Memories* is 1v/cm, any number of different voltages may be present at the plug-in input selected by the MV/DIV switch.
2. Similarly, the TIME/DIV switch changes the value of time per CRT graticule division.
3. Information from these switches control the operation of the Divide-By circuits.
   a. The information from the switches is in the form of a ground placed on a Divide-By gate.
   b. The ground opens the gate allowing clock pulses to pass.
   c. Since the MV/DIV switch or the TIME/DIV switch selects only one ground at a time, only one Divide-By circuit can have an output at a time.
4. Two operations are required to provide a correct readout in each MV/DIV or TIME/DIV switch position.
   a. A Divide-By output is selected.
   b. A decimal on the Nixie readout is selected.
5. If either switch (MV/DIV for amplitude measurements or TIME/DIV for time measurements) is in the .1, 1, 10, or 100 positions, the ÷1 output is selected.
   a. Pin 1 is grounded.
   b. The clock pulses are inverted in the ÷1 Gate, but not divided.
   c. The appropriate decimal is selected by the switches.

* See Memories Card.

6. If either switch is in the .5, 5, or 50 positions, the ÷2 output is selected (pin 10 grounded) and a decimal is selected.

   a. The clock pulses are divided by two.

   b. The effect is almost the same as multiplying the switch position reading by 5.

7. If either switch is in the .2, 2, 20 or 200 position, the ÷5 output is selected (pin 2 grounded) and a decimal is selected.

   a. The clock pulses are divided by five.

8. Summarizing, consider three examples:

   a. First Example:

      TIME/DIV switch set at 10 nsec/div, the DOTS/DIV at 100 and a 1 cm wide pulse displayed on the screen.

      (1) To measure the pulse width, the Master Gate would open for 1 cm.

      (2) 100 clock pulses would pass (100 DOTS/DIV).

      (3) Pin 1 would be grounded.

      (4) The Divide-By circuits would <u>not</u> divide the clock pulses.

      (5) The decimal would be arranged to show a reading of 010.0 nsec.

b. Second Example:

TIME/DIV control set at 5 nsec/div, the DOTS/DIV at 100, and the pulse covering 2 cm (or divisions) of the graticule.

(1) The Master Gate would be open 2 cm.

(2) 200 clock pulses would pass.

(3) Pin 10 would be grounded.

(4) Only half of the clock pulses would pass (÷2 output).

(5) The counter would count the 100 pulses.

(6) The decimal would be placed to read 010.0 nsec -- the correct pulse duration.

c. Third Example:

TIME/DIV control set at 2 nsec/div, DOTS/DIV at 100 and the 10 nsec pulse covering 5 cm of display.

(1) The Master Gate would open for 5 cm.

(2) 500 clock pulses would pass.

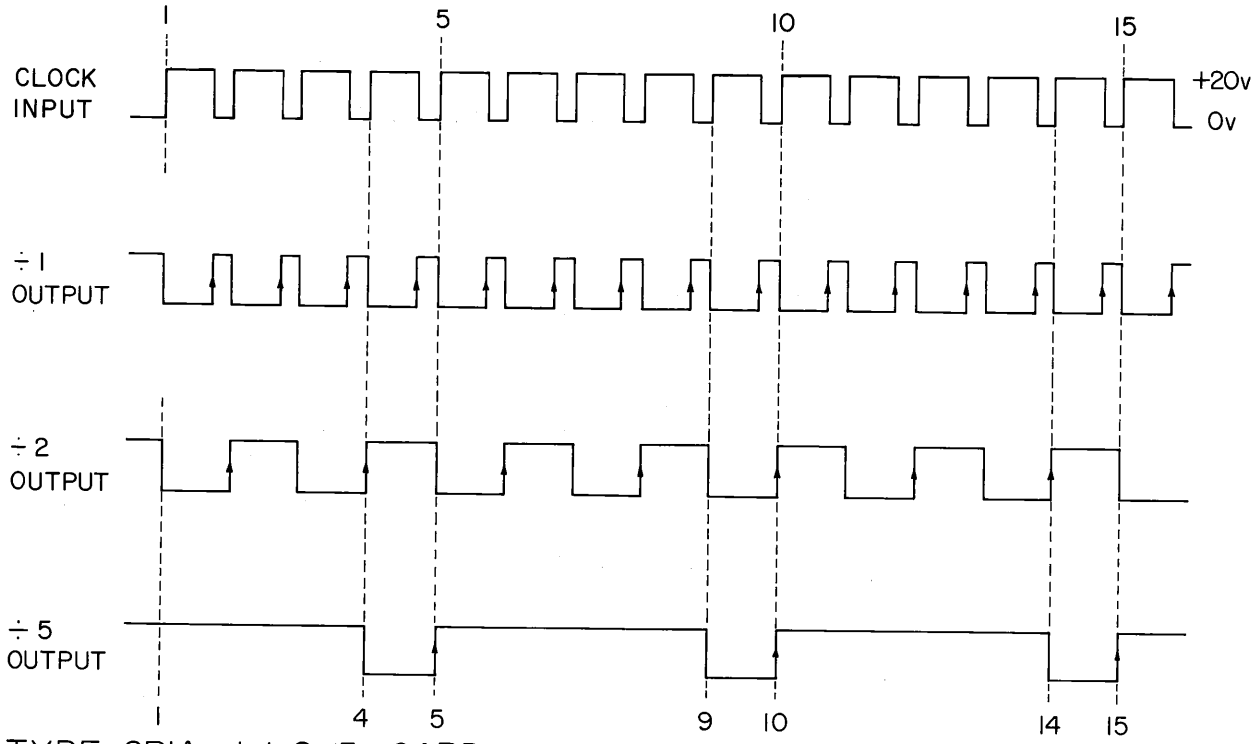
(3) Pin 2 would be grounded by the TIME/DIV switch.

(4) The ÷5 circuit would provide an output of 100 pulses (1/5 of the clock pulses).

(5) The counters would count the 100 pulses.

(6) The decimal would be placed to register a proper count of 010.0 nsec.

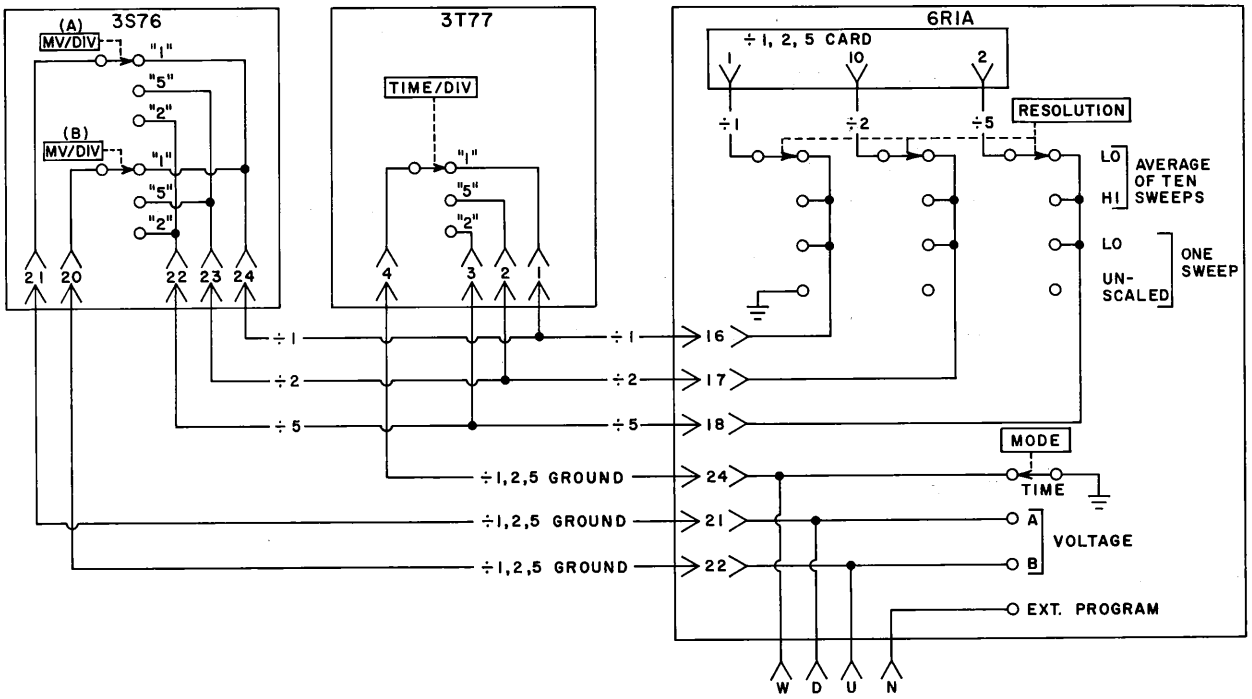
9. The illustration (below) indicates counting relationships, not waveforms.



TYPE 6RIA ÷1,2,5 CARD
INPUTS AND OUTPUTS OF 1,2,5 CARD

B-6RIA-0084
7-1-64 jg

H. Ground Selection (Sampling Plug-Ins)



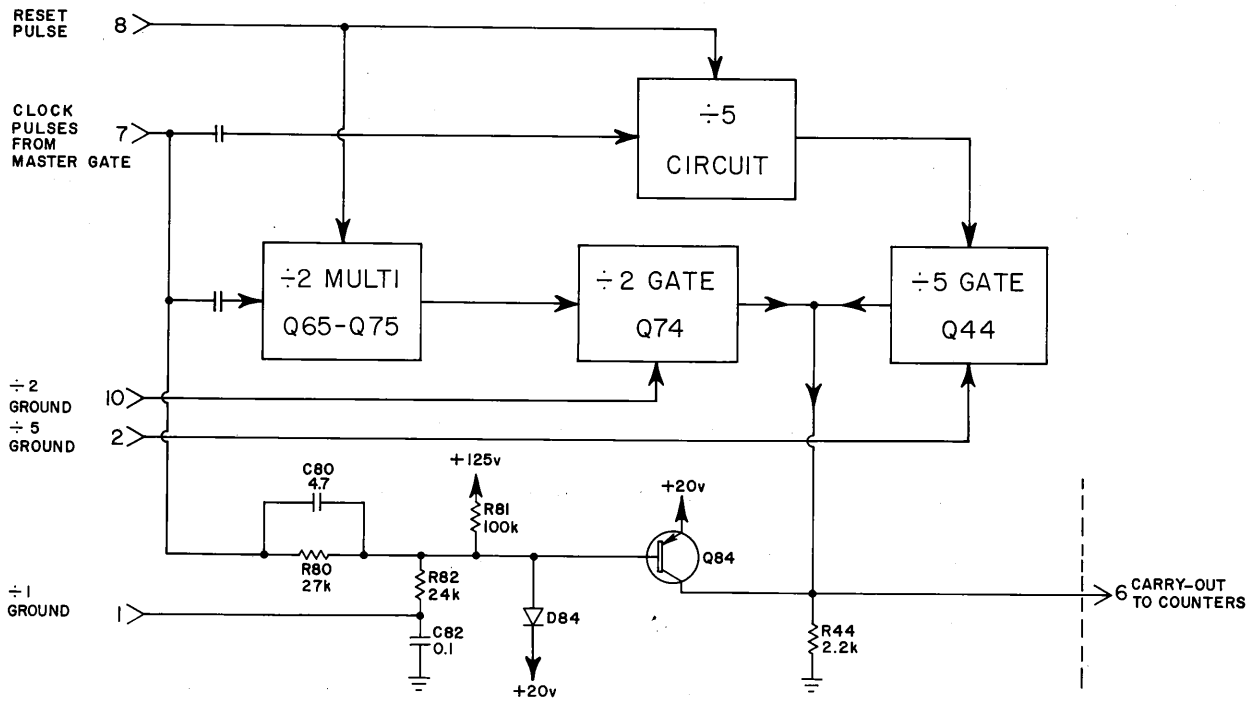
TYPE 6RIA ÷1,2,5 CARD
GROUNDING CIRCUITS

B-6RIA-0085
8-11-'64 dl

1. Ground selection is made utilizing the RESOLUTION switch and the MODE switch on the 6R1A front panel, the TIME/DIV switch in the 3T77, and the two MV/DIV switches in the 3S76.
2. The ground originates with the MODE switch.
3. If TIME is selected, the TIME/DIV switch selects and carries the ground by one of three cables to the RESOLUTION switch.

4. If either of the MV/DIV switches is selected, one of the same three cables is selected for grounding.
5. The selections are ÷1 ground for the "1" position, ÷2 ground for the "5" position, and ÷5 ground for the "2" position.
6. Whichever cable is selected carries the ground to the RESOLUTION switch.
   a. In all but the UNSCALED position, the ground is carried to the ÷1, 2, 5 Card.
   b. In the UNSCALED position, the selected ground is opened and pin 1 (÷1 gnd) is grounded.

I. ÷1 Gate, Q84



TYPE 6RIA ÷1,2,5 CARD
÷1 GATE

B-6RIA-0086
6-29-'64 jg

1. The ÷1 Gate can be considered an AND Gate and an inverting amplifier.
2. The circuit has an input of clock pulses (on pin 7) when gated on by the Master Gate*.
3. The circuit has an output when pin 1 is grounded.
   a. Pin 1 is grounded when, for time measurements, the TIME/DIV switch is in the .1, 1, or 10 position, or for voltage measurements, a MV/DIV switch is in the .1, 1, 10, or 100 position.
4. When pin 1 is not grounded, Q84 is cut off.
   a. 1 ma through D84, R81 holds Q84 base at 20.3v**.
   b. Arrival of a clock pulse robs the diode of .75 ma but does not disconnect the diode.
5. When pin 1 is grounded, Q84 base is released to be driven by the clock pulses.

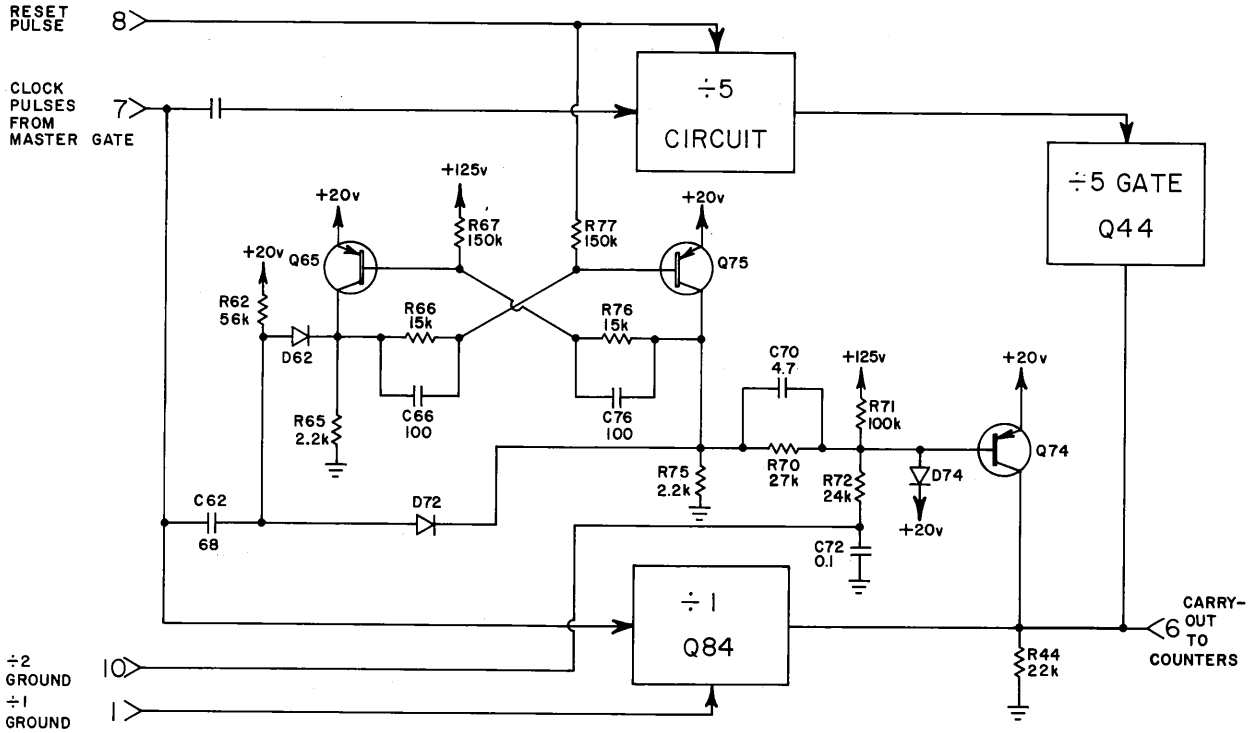
* See Master Gate Card.

** All voltages that are referenced to the 20v supply will measure about 1v low as 20v decoupled is actually 19v.

6. Prior to arrival of the clock pulse train, Q84 is conducting.
   a. Pin 7 is at ground.
   b. The divider composed of R81 to 125v and R82 and R80 in parallel to ground forms an equivalent 11k to 12.7v.
   c. This provides a .12 ma base current drive.
   d. Q84 saturates.
   e. The base-emitter junction limits the negative swing to 19.7v.
   f. Q84 collector sets at 20v.
7. The arrival of the clock pulse train at pin 7 lifts Q84 base to cut off.
   a. D84 limits the base rise to 20.3v.
   b. The divider R80, R81, R82 becomes an equivalent 11k to 22.4v.
   c. The collector drops to ground.
   d. Pin 7 rises to 20v.
8. The first clock pulse turns on Q84.
   a. The collector pulls up to 20v forming the output clock pulse.
   b. The leading edge of this and each successive positive going clock pulse actuates the counters.
9. C82 bypasses any noise that might be present on the interconnecting cable through pin 1.
10. C80 is a speed-up cap used to preserve the clock pulse risetime and falltime.

J. ÷2 Multi and ÷2 Gate; Q65, Q75, Q74

1. The ÷2 Multi is a binary multivibrator that provides a 2:1 countdown for clock pulses.



TYPE 6RIA ÷1,2,5 CARD
÷2 MULTI AND GATE

B-6RIA-0087
6-30-64 jg

2. R77 in the multi cross-coupling network returns to 125v through pin 8 to the Master Gate.

3. At the start of count period, a reset pulse is applied to the base of Q75 through R77, turning off D75 and turning on Q65.

a. The reset pulse is a 108v pulse (starting at 125v) at pin 8.

b. This resets the Multi and sets the correct logicl level for the binary.

c. The Multi output (Q75 collector) is LOW.

d. The reset pulse resets the Multi only if necessary -- the last divide-by action of the previous clock pulse train may have left the Multi in the "1" (reset) position.

4. DC levels* after the Multi is reset (Q75 off, Q65 on):

a. Q75 base, 21v.

b. Q75 collector, 4v.

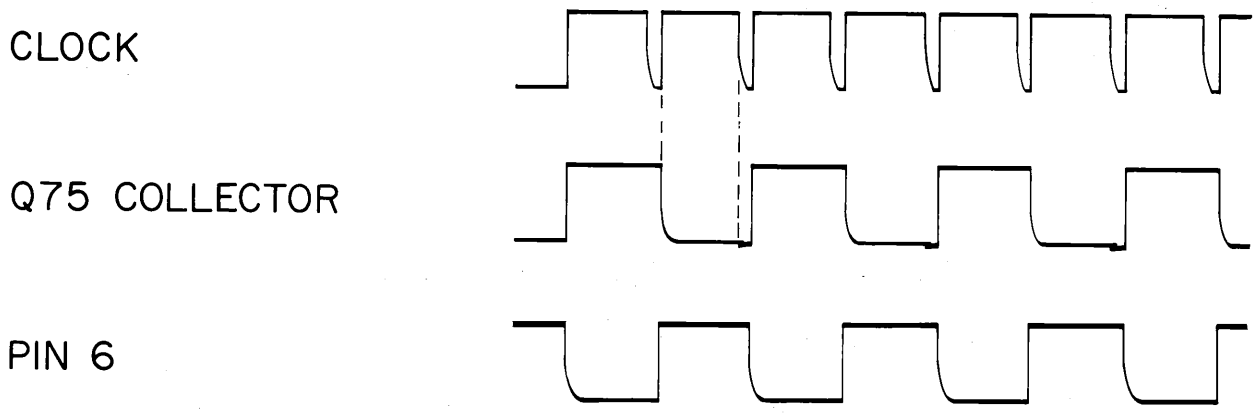
c. Q65 base, 18.7v.

d. Q65 collector, 19v.

5. D62 and D72 are steering diodes that direct clock pulses to the correct multi base to provide the required 2:1 countdown.

6. When the Multi is reset, D62 is reverse biased by about 15v.

a. D72 is conducting with about .3 ma flowing through R62.



TYPE 6RIA ÷1,2,5 CARD
÷2 MULTI WAVEFORM

B-6RIA-0088
8-25-'64 jg

* These are measured voltages when 20v decoupled measured 19v.

7. Shortly after the Multi is reset, the Gated clock pulse train arrives at pin 7.
   a. Prior to the start of the clock pulse train, pin 7 is at 0v.
   b. The clock pulses are negative going 20v pulses riding at a 20v logic level.
   c. The start of the train is a 20 positive going step, coincident with the trailing edge of a clock pulse in the Master Gate.
   d. The pulses to be divided in the ÷2 Multi start with the change in logic level from 0 to 20v, and continue to switch with each subsequent clock pulse trailing edge.
   e. A negative step has no effect on the ÷2 Multi.
8. The first positive step flips the Multi (Q65 off, Q75 on).
   a. The step is differentiated in C62.
   b. The pulse pulls current through D72 and C76 to rob current from Q65 base.
   c. Q65 base rises cutting off the transistor and through multi action turns on Q75.
9. Q75 collector (the Multi output) rises to 19v.
   a. This pulse results in a count in the counter circuits.
10. When the trailing edge of the next clock pulse arrives, the Multi flips again.
   a. The pulse passes through D62 to lift Q75 to cut off.
11. Q75 collector drops to 4v.
12. The Multi has completed one cycle (one positive output step) for each two input pulses.

13. The ÷2 Clock Gate (Q74) operates in the same manner as the ÷1 Clock Gate.

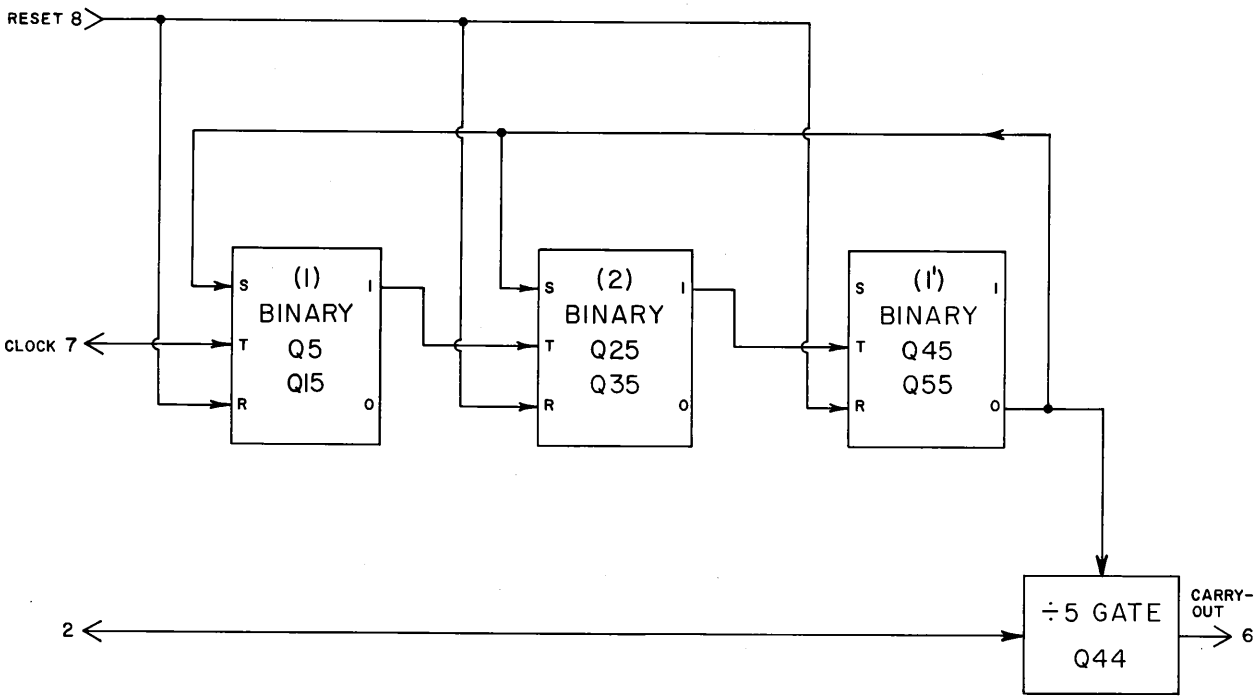
    a. Whenever pin 10 is grounded, the gate passes the ÷2 clock pulses.

    b. The positive going edge of the output pulse actuates the counters.

    c. This step is coincident with the trailing edge of every other input clock pulse.

K. ÷ 5 Binary Circuit and ÷5 Gate

1. The ÷5 circuit consists of a three stage binary counter that provides a 5:1 countdown.



TYPE 6RIA ÷1,2,5 CARD
÷5 BINARY BLOCK DIAGRAM

B-6RIA-0089
8-19-'64 dl

a. Normally a three-stage binary produces an output pulse for each eight input pulses.

b. The ÷5 circuit has a feedback from the third binary to the first and second to produce an output pulse for each 5 input pulses.

2. Binary logic symbols* entitle the binary blocks as "1" Binary, "2" Binary, and "1'" Binary.

3. Each binary has three possible inputs and two outputs.

   a. Inputs include trigger, set and reset.

   b. Outputs are 1 and 0.

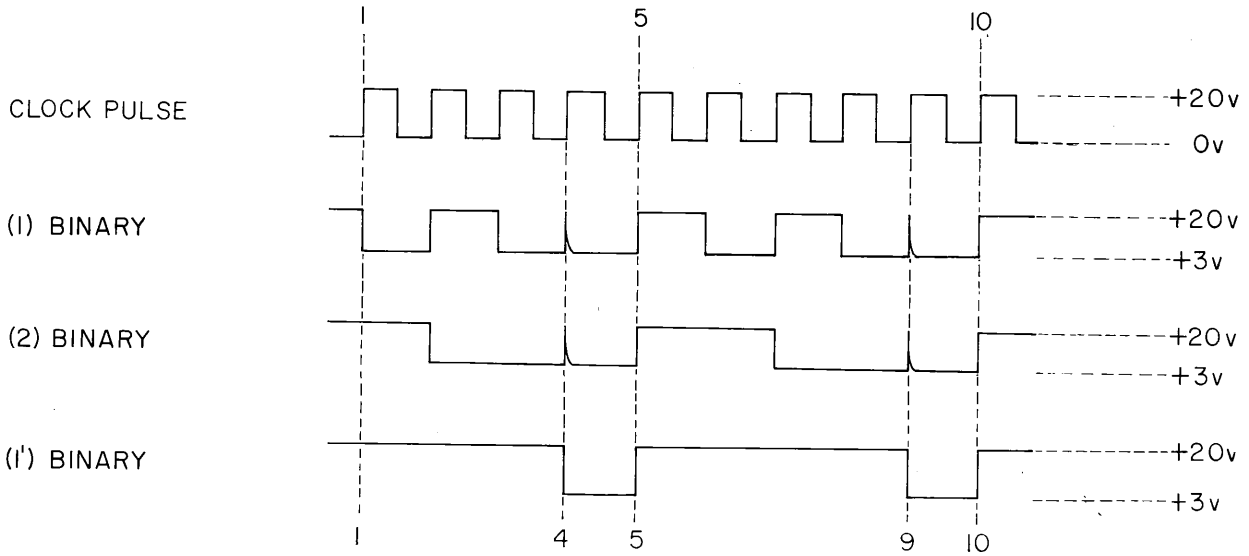
   c. A reset input pulse switches the binary to its 0 state.

   d. A set input pulse switches the binary to its 1 state.

   e. A trigger input pulse will result in the next successive output.

      (1) If in the 0 state, a trigger will switch the binary to its 1 state.

      (2) If in the 1 state, a trigger will switch it to the 0 state.



TYPE 6R1A ÷1,2,5 CARD
÷5 BINARY RELATIONSHIPS

B-6R1A-0090
7-1-64 jg

* The Language and Symbology of Digital Computor Systems, RCA.

4. At the start of Print Command count condition, a reset pulse arrives at pin 8.

   a. The reset pulse resets all binaries to their 0 state.

   b. The binaries may or may not require resetting.

5. The arrival of a clock pulse (trigger) on pin 7 switches the 1 Binary to its 1 state.

   a. The binary has a carry out only when it leaves a state, therefore, it has no carry-out from its 1 state at this time.

PULSE NUMBER	BINARY SET		
	1 (1)	2 (2)	3 (1')
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
	1	1	1
5	0	0	0

6. The Binary State as a result of the first clock pulse:

   1 Binary, 1

   2 Binary, 0

   1' Binary, 0

7. The second clock pulse switches 1 Binary to its 0 state.

   a. The 1 Binary now has a carry-out.

8. The carry-out switches the 2 Binary to its 1 state.

9. Binary states as a result of the second clock pulse:

   1 Binary, 0

   2 Binary, 1

   1' Binary, 0

10. The third clock pulse switches the 1 Binary to its 1 state.

    a. There is no carry-out to the 2 Binary.

11. Binary state as a result of the third clock pulse:

    1 Binary, 1

    2 Binary, 1

    1' Binary, 0

12. The fourth clock pulse switches the 1 Binary to its 0 state.

    a. The carry-out to the 2 Binary switches it to its 0 state.

    b. As the 2 Binary switches to its 0 state (leaving its 1 state), it has a carry-out to the 1' Binary.

    c. As the 1' Binary switches to its 1 state (leaving its 0 state) it has a carry-out from its 0 output.

    d. The carry-out from the 1' Binary feeds back to the 1 and 2 Binaries switching them to their 1 state.

13. The binary state as a result of the fourth clock and the feedback action:

    1 Binary, 1

    2 Binary, 1

    1' Binary, 1

14. The fourth clock pulse, therefore, results in a transistional state that is immediately switched by the feedback to the state shown in step 13.

15. In this state, the 1' Binary has a carry-out, but since it is inverted in the ÷5 Gate, will not result in a count.

16. The fifth clock pulse switches the 1 Binary to its 0 state.

    a. The carry-out (leaving its 1 state) switches the 2 Binary to its 0 state.

    b. The 2 Binary carry-out switches the 1' to its 0 state.

    c. The 0 state carry-out is inverted in the ÷5 Gate to form the output pulse that is counted.

17. Binary State as a result of the fifth clock pulse:

    1 Binary, 0

    2 Binary, 0

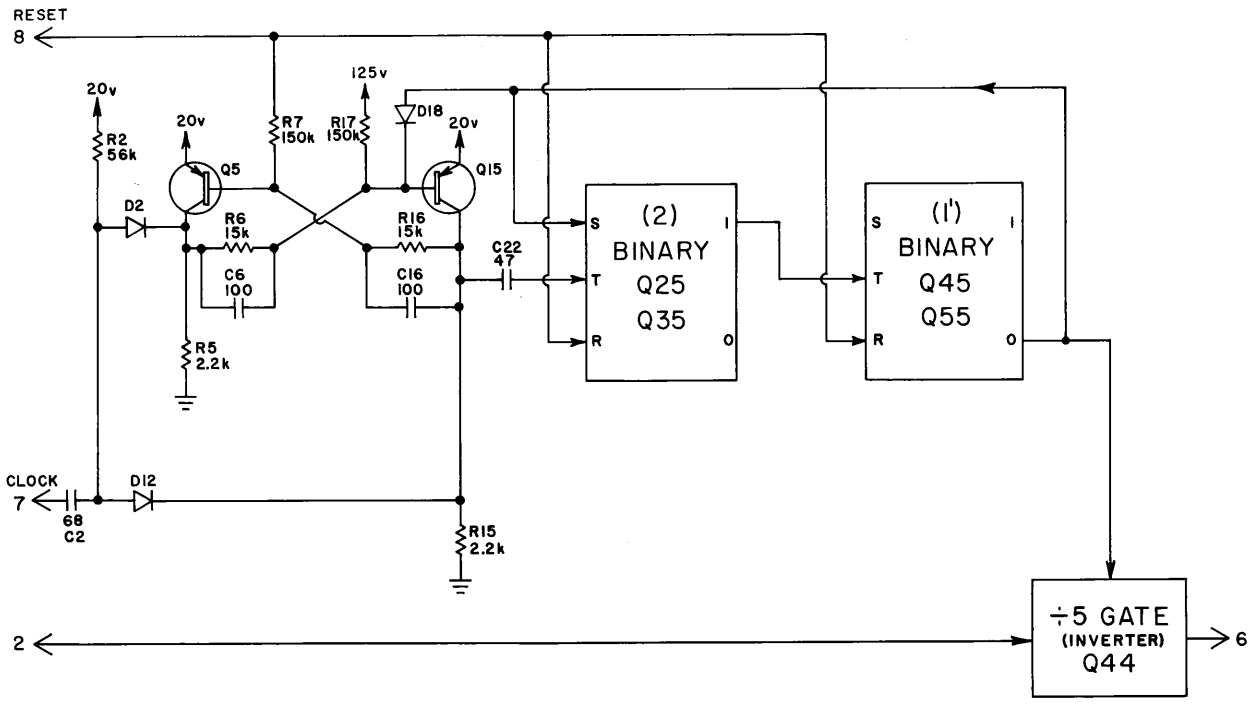
    1' Binary, 0

18. The ÷5 circuit is now reset and ready to accept another sequence of five clock pulses.

19. The 1 Binary, like the 2 and 1' Binaries, is reset and triggered in the same manner as the ÷2 Binary.

20. The Set pulse, which is fed back from the 1' Binary, when the fourth clock pulse arrives (see step 12), is a positive going 10v pulse.

a. Q15 is conducting (Binary 0 state) with its base at 18.7v.



TYPE 6RIA ÷1, 2, 5 CARD
÷5 CIRCUIT, (1) BINARY

B-6RIA-0092
8-20-'64 dl

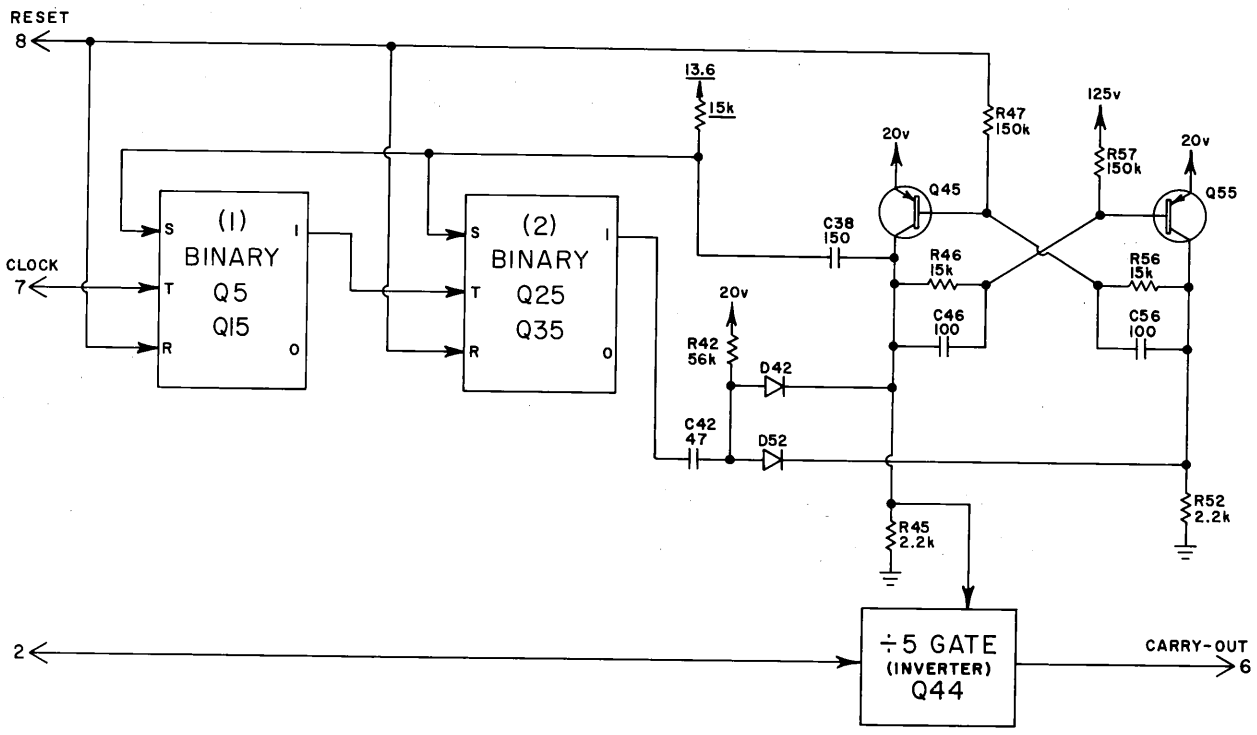
b. The pulse is fed through D18 to Q15 base (Set input to the binary block).

c. The pulse cuts off Q15 switching the Multi to its Binary 1 state.

21. The carry-out pulse, in order to flip the 2 Binary Multi, must be positive going.

    a. Q15, therefore, must cut off (switch from its 1 state) to produce the required carry-out.

22. The 1' Binary has its output taken from Q45 collector, the left hand transistor in the Multi (0 Binary output).



TYPE 6RIA ÷1,2,5 CARD
÷5 CIRCUIT, (1') BINARY

B-6RIA-0093
8-21-'64 dl

    a. The output is fed to the ÷5 Gate and fed back as the Set pulse to the 1 and 1' Binaries.

b. The Set pulse is a positive going step that is differentiated in C38 to a 10v pulse.

23. The ÷5 Gate operates in the same manner as the ÷1 and ÷2 Gates.

a. When pin 2 is grounded, the ÷5 pulses can pass.

b. The ÷5 pulse is actually a rectangular waveform.

c. The ÷5 pulse (a positive going step) is coincident with the trailing edge of the fifth clock pulse.

(1) A negative step coincident with the trailing edge of the fourth clock pulse precedes the ÷5 pulse.

XII. COUNTER CARDS

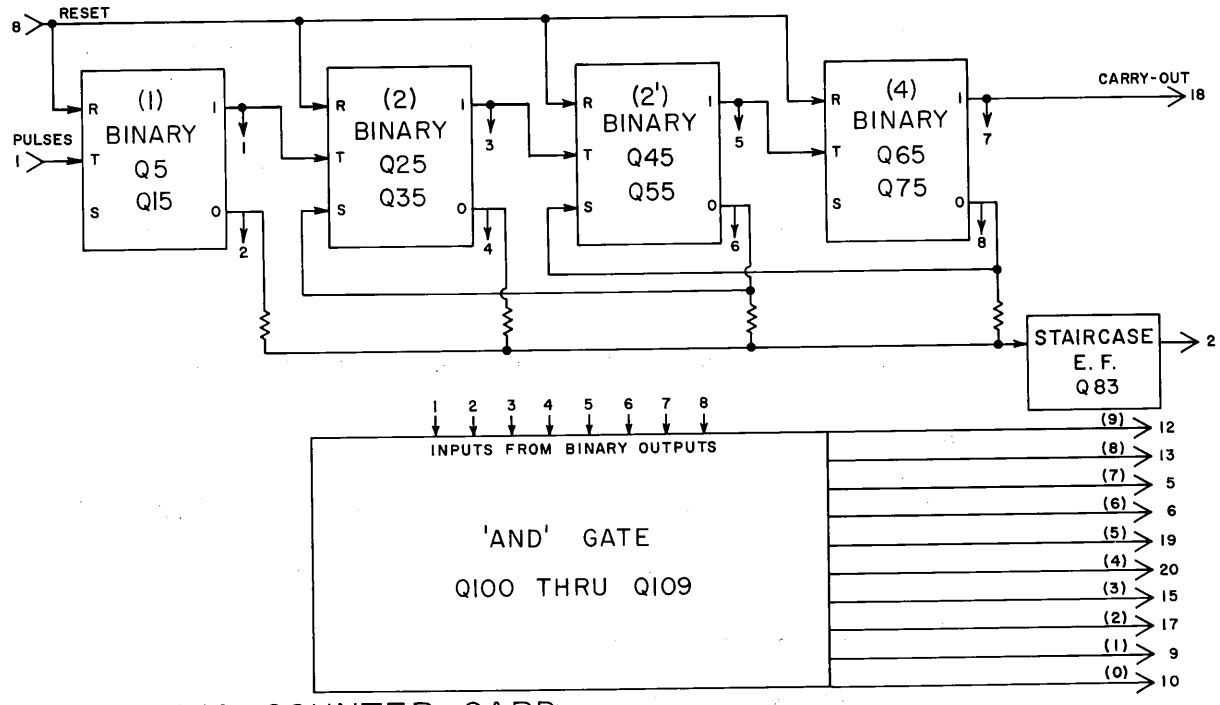
A. Four identical and interchangeable counter cards are used in the 6R1A.

1. Each counter card can count one decade.
2. Called Decade Counters, the cards may be identified as the Units, Tens, Hundreds, and Thousands counter cards.
3. Connected in series, the first card in the series (Units) counts to 10, the second (Tens) to 100, the third (Hundreds) to 1,000, and the fourth (Thousands) to 9,999.
4. The ten counter outputs from each card supply the Nixies.

B. Circuits that comprise the counter card:

1. Four binary sets, Q5, Q15, Q25, Q35, Q45, Q55, Q65, Q75.
2. Ten nixie driver transistors, Q100 through Q109.
3. Staircase Emitter Follower, Q83.
4. Transistors used in the Binaries are 151-054 germanium PNP transistors selected from 2N2957 for BV_{CBO} and BV_{CEO}.
5. The driver transistors are 151-096 2N1893 silicon NPN transistors.
6. The Staircase EF is a 153-520 germanium PNP transistor selected from 2N404.
7. All diodes are 152-075 germanium diodes.

C. Block Diagram



TYPE 6RIA COUNTER CARD
BLOCK DIAGRAM

B-6RIA-0099
9-9-'64 dl

D. Inputs

1. A 108v reset pulse (from 125v to 233v) at pin 8 from the Master Gate.

   a. The pulse occurs at the start of Print Command count condition.

   b. It resets all binary circuits to zero.

2. Input from the previous counter at pin 1.

   a. The Units counter receives gated clock pulses from the Master Gate via the ÷1, 2, 5 card.

      (1) These are 20v positive going pulses when the ÷1 circuit is selected*.

      (2) When the ÷2 or ÷5 output is selected*, the input at pin 1 is a 20v rectangular waveform; the positive step is used.

   b. The Tens, Hundreds, and Thousands cards receive the carry-out from the previous counter.

      (1) These are 17v rectangular waveforms; the positive step is used.

E. Outputs

1. Carry-out to the next counter at pin 18.

   a. A 17v (3v to 20v) rectangular waveform to the next counter, except the Thousands counter which has no carry-out.

2. The Staircase out at pin 2 to the Upper and Lower Limit NO-GO cards.

   a. The Staircase has 9 steps of 1.7v/step starting at 3.85v and ending at 19.15v.

3. Ten nixie-driver outputs are provided.

   a. The ten outputs from each counter connect to their respective nixies -- the Tens counter connects to the tens nixie, etc.

* See ÷1, 2, 5 card.

b. When an output is at ground (pulled down by a conducting driver transistor, the nixie will glow with the corresponding number -- if the 4 output is at ground; for example, the nixie will show the digit 4.

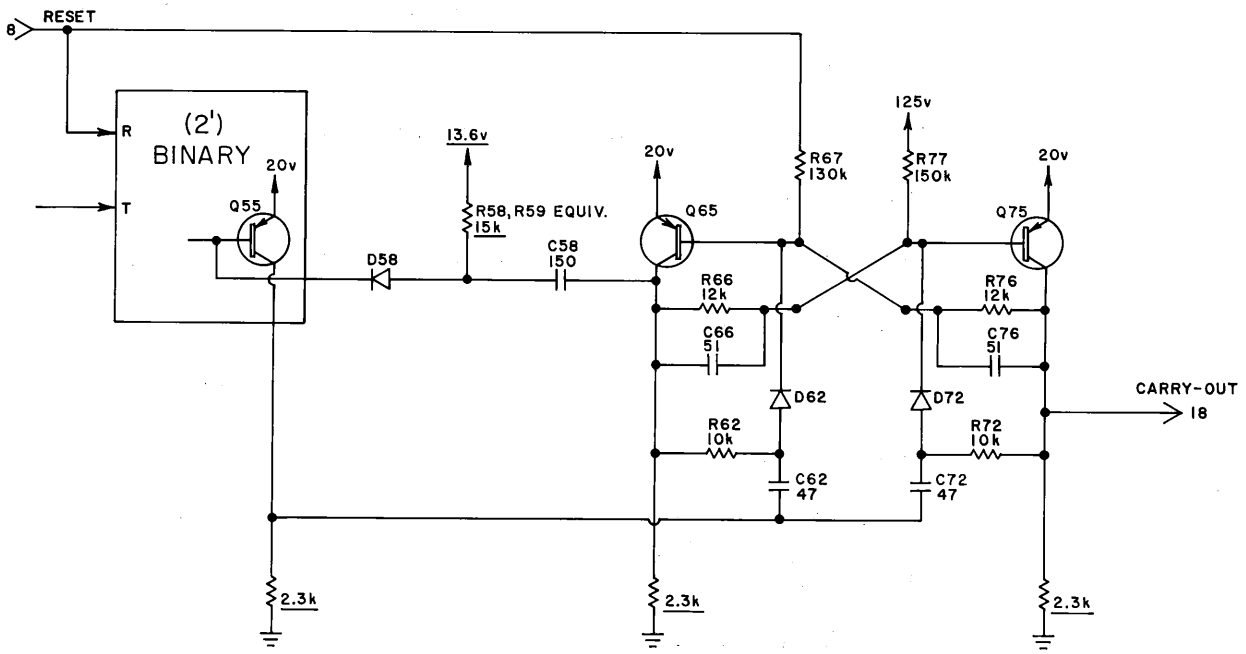
F. Block Logic

1. At the start of the Print Command count condition, a Reset Pulse resets all binaries on all counter cards to zero.
   a. The 0 outputs at pin 10 are at ground, lighting the zero digit on the four count nixies.
   b. The staircase out at pin 2 is at 3.85v on all counter cards.
2. The first clock pulse (through pin 1) flips the 1 Binary, which turns off the 0 driver and turns on the 1 driver.
   a. The 1 output at pin 9 is pulled down to ground, lighting the units nixies to 1.
   b. The staircase output voltage increases 1.7v to 5.55v.
3. Each successive clock pulse increases the count by 1*.
   a. As the count proceeds, the units nixie lights momentarily with each count.
   b. The staircase output voltage increases 1.7v with each count.
4. With the tenth clock pulse, the Binary count becomes zero.
   a. The zero output at pin 10 grounds, lighting the units nixie to zero.
   b. The staircase out voltage resets to 3.85v.
   c. A carry-out occurs at pin 18.

* See ÷10 card for Binary Logic description.

5. The carry-out is fed to the Tens counter card.
   a. The Tens card counts 1.
   b. The Tens staircase steps one step.
   c. The Tens card 1 output at pin 9 grounds, lighting the Tens nixie to 1.
6. For every ten clock pulses fed to the Units card, one pulse is fed to the Tens counter.
7. When the Tens counter has counted to 10 it has a carry-out to the Hundreds counter.
8. The output from the Hundreds counter in turn is fed to the Thousands counter.
9. The counters continue to count each clock pulse as long as gated clock pulses arrive from the Master Gate.
   a. The nixies record each count.
10. At the end of Print Command count condition, clock pulses stop arriving.
11. The nixie display, representing the total count of the gated clock pulses, are retained for the duration of the Display Period of the Print Command.

G. The Binaries (4 Binary illustrated; Q65, Q75)



TYPE 6RIA COUNTER CARD
"4" BINARY

B-6RIA-0100
9-9-'64 dl

1. The Binaries are transistorized Eccles-Jordon multivibrators.
   a. They are base triggered through steering diodes to provide each binary with its 2:1 countdown.
   b. Base triggering allows the use of smaller cross-coupling caps which in turn provides faster binary switching.

2. The Reset Pulse input through pin 8 is clamped by D75 (Master Gate Card) at 125v.
   a. The 125v provides base return for the left hand transistor in the binary.
3. The Reset Pulse (at the beginning of Print Command count condition) pulls up on Q65 base (and the base of the left hand transistor in each binary) flipping the multi to its 0 state.
   a. The Reset Pulse is a 105v pulse about 35 μsec wide.
   b. Only about 8% of the pulse reaches the base.
      (1) The start of the reset pulse charges the cross coupling cap in about .6 μsec.
      (2) The 35 μsec pulse, then, has sufficient energy to lift the base to cut off.
   c. The relatively low value of R67 (130k) provides a divider (R67, R76) that sets Q65 bias close enought to cut off so the Reset pulse will have positive control.
   d. The Reset pulse must be capable of overriding the action of a trigger.
      (1) If a binary is in its 1 state when reset, it will have a carry-out to the next binary.
      (2) The Preset must override this trigger.
4. The multi base set at 19.7v* when conducting.
   a. When cut off, Q65 base raises to 27v and Q75 base to 26v.
   b. The Reset pulse lifts Q65 base to 29v for the pulse duration.

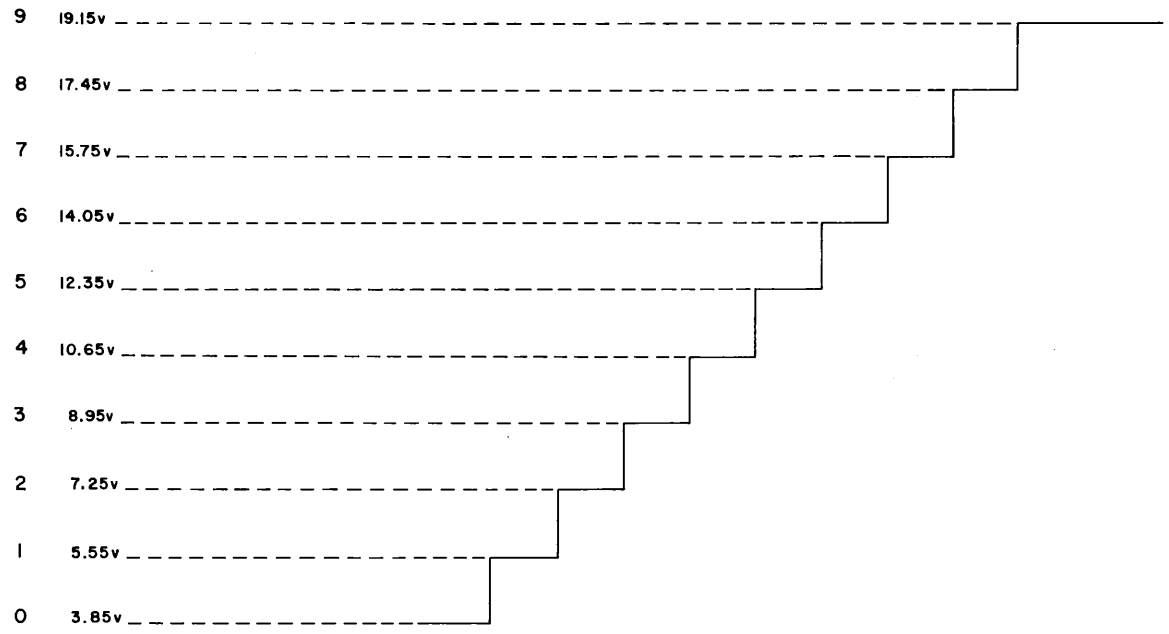
* Assuming 20v decoupled is at 20v.

5. The collectors swing from about 3v cut-off to about 20v conducting.
6. The OFF sterring diode is back biased 23v.
7. The ON steering diode is in parallel with the base-collector junction of the saturated transistor.
   a. Static current through the diode is a few μamps.
8. The trigger pulse is differentiated in a trigger coupling capacitor (C62 or C72 in the 4 Binary).
   a. TC is 47 μsec.
9. The Set pulse* is taken from Q65 collector (the 0 output of the Binary).
   a. The pulse is fed back through C58 and D58 to the 2' Binary.
10. R58, R59 equivalent sets D58 anode at 13.6v.
   a. When conducting, D58 base sets at 19.7v.
   b. D58 is reverse biased by 6v.
11. Carry-out from Q65 collector is a 17v step which is differentiated in D58.
   a. The pulse forward biases D58.
   b. As the pulse lifts Q55 base to cut-off, the 2' Binary switches*.
12. Carry-out from both 0 and 1 outputs from the Binaries is fed to the nixie drivers.
   a. Carry-out from the 0 outputs from the four Binaries drives the Staircase EF.
   b. Carry-out from the 1 output of the 4 Binary feeds the input to the next counter card.

* See ÷10 Card, page 10-14 for details of feedback action.

H. Staircase Emitter Follower, Q83

1. The Staircase Generator supplies a voltage staircase to the Upper and Lower NO-GO circuits.
   a. The staircase has 9 steps of 1.7v per step.
   b. It starts at 3.85v* with the count of zero, and ends at 19.15v* with the count of 9.
   c. The waveform resets to 3.85v* again at the count of 10 (zero) and at the start of the Print Command count condition.
2. The staircase can be considered a running total of the count from the Binaries.
   a. Each voltage step represents a count.



TYPE 6RIA COUNTER CARD
STAIRCASE

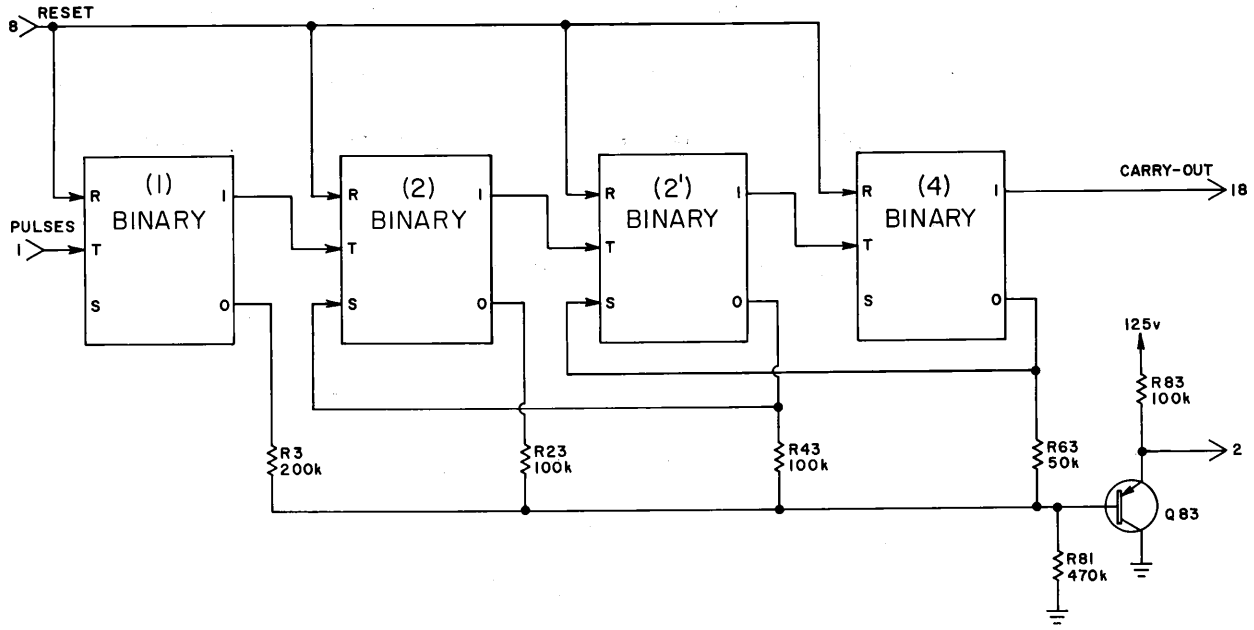
B-6RIA-0103
9-15-'64 dl

* All staircase voltages are ideal voltages. In practice, they may vary with resistor values.

3. The voltage count is generated by the 0 outputs from the Binaries.

   a. A binary has a carry-out from its 0 output when the Binary leaves its 0 state.

   b. The 0 output, therefore, is at 20v when the Binary is in its 1 state.



TYPE 6RIA COUNTER CARD
STAIRCASE E. F.

B-6RIA-0101
9-10-'64 dl

4. Voltage dividers, composed of R81 and combinations of R3, R23, R43 and R63 form the voltage count.

   a. For the 0 count, all 0 outputs are at a theoretical 3.55v.

      (1) Q83 base-emitter junction voltage riases this level to 3.85v.

b. The 1 count has binary number 1000.

(1) 1 Binary's 0 output is at 20v.

(2) A divider formed of R81 to ground, R23 and R43 to 3.55v, and R3 to 20v sets Q83 base at 5.25v.

(3) Q83 base emitter junction raises the Staircase output at pin 2 to 5.55v.

PULSE NUMBER	BINARY SET			
	1 (1)	2 (2)	3 (2')	4 (4)
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
	0	1	1	0
5	1	1	1	0
6	0	0	0	1
	0	0	1	1
7	1	0	1	1
8	0	1	1	1
9	1	1	1	1
10 (0)	0	0	0	0

c. The 2 count has binary number 0100.

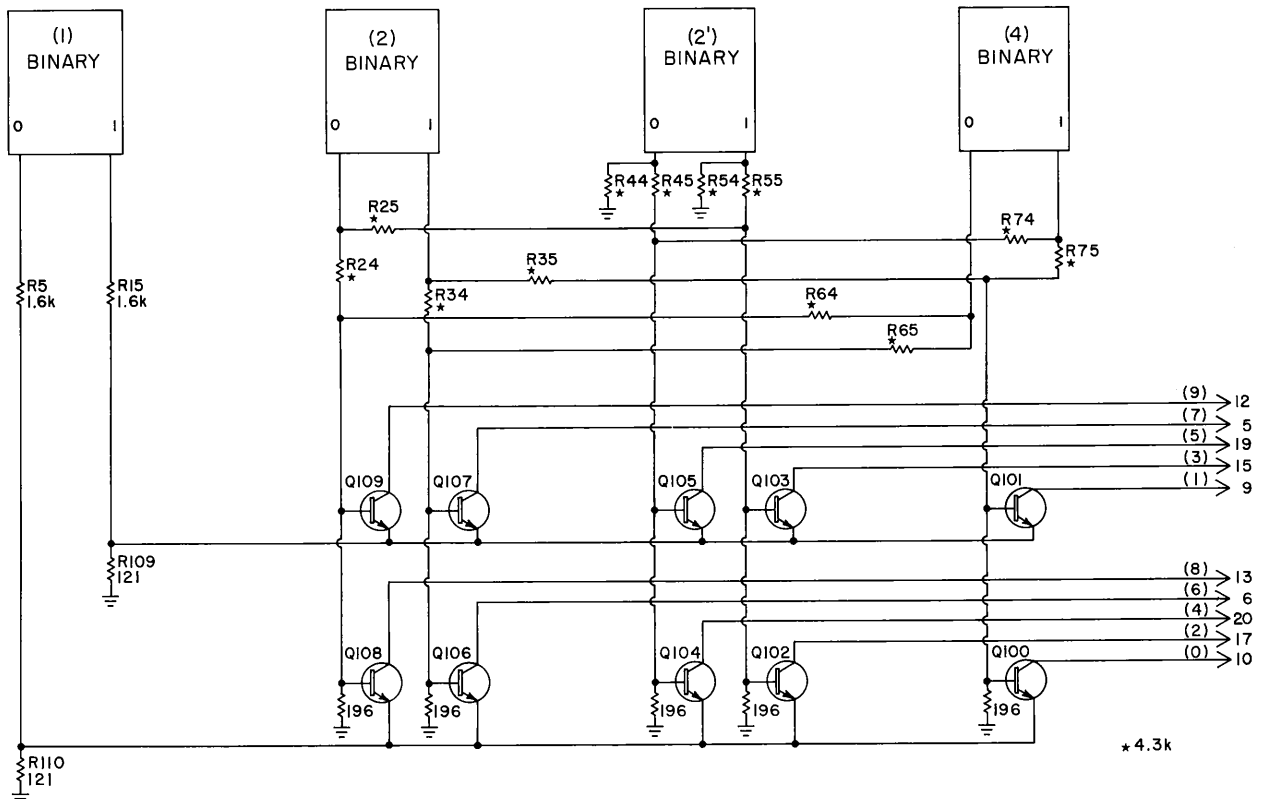
(1) 2 Binary's 0 output is at 20v with the other binaries 0 outputs at 3.55v.

(2) The divider composed of R23 to 20v, R81 to ground, and R3, R43, and R63 to 3.55v, plus Q83 base emitter junction potentials provide the required 7.25v at pin 2.

d. Subsequent binary counts result in divider ratios that provide the voltage count steps of the staircase.

I. Nixie Drivers, Q100 through Q109

1. A driver transistor is provided for each nixie cathode (0 through 9).



TYPE 6RIA COUNTER CARD
NIXIE DRIVER

B-6RIA-0102
9-14-'64 dl

a. The transistor collector is connected to the nixie cathode (6R1A main frame).

b. When the transistor saturates and its collector drops to near ground, the nixie current return is completed and the nixie glows with the number corresponding to its grounded cathode.

2. The outputs from the four binaries are connected to the nixie drivers in such a way that only one output at a time will be grounded.

a. In order for a driver output to be at ground, the emitter must be LOW (.5v) and the base HIGH (1.2v).

3. The 1 output from the 1 Binary is connected to the emitters of all the "odd" nixie drivers (Q101, Q103, Q105, Q107, Q109) corresponding to the odd nixie numbers.

a. Note (the Binary States Chart on page 12-11) that the 1 Binary is in its 1 state during an odd count.

b. A binary's 1 output is LOW during its 1 state.

c. During odd counts, therefore, the emitters of all odd driver transistors are LOW.

(1) The transistors are "enabled".

(2) If the base is HIGH, the transistor will saturate.

4. The emitters of all even driver transistors (Q100, Q102, Q104, Q106, Q108) corresponding to the even nixie numbers is tied to the 0 output of the 1 Binary.

a. Since the 0 Binary output is HIGH during its 1 state, the even driver transistors cannot conduct.

5. The even counts reverse the condition enabling the even driver transistors and biasing the odd transistors so they cannot conduct.

6. The base of each driver transistor is connected through a 4.3k resistor to two binary outputs.

   a. The 0 and 1 drivers are tied to the 1 outputs of the 2 and 4 Binaries.

   b. All other driver transistors have their bases tied to one 0 Binary output and one 1 Binary output.

   c. Note that the base on one odd and one even transistor is connected in parallel.

   d. Only one transistor can conduct at a time, however, since an odd and an even transistor cannot conduct simultaneously.

7. In order for the transistor to conduct, both base connections (Binary outputs) must be HIGH (and the emitter LOW).

   a. With one Binary output HIGH (about 20v) and one output LOW (3.55v), 4.4 ma flows through the 196Ω base return resistor.

      (1) This places the base at .86v.

      (2) With the emitter LOW (enabled position at .5v), the transistor conducts but not enough to pull its collector to ground.

      (3) The nixie number does not light.

   b. With both inputs HIGH, 8.8 ma flows to the Binaries.

      (1) 8.8 ma through the 196Ω resistor would pull the base up to 1.72v.

(2) The transistor saturates using part of the current, and limiting the base rise to 1.2v.

c. With the transistor saturated, the collector drops to near ground, lighting the nixie to the corresponding number.

8. The chart (below) shows the Binary output levels for each count.

BINARY SET								
	1 (1)		2 (2)		3 (2')		4 (4)	
COUNT	OUTPUT 0	OUTPUT 1	OUTPUT 0	OUTPUT 1	OUTPUT 0	OUTPUT 1	OUTPUT 0	OUTPUT 1
0	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH
1	HIGH	LOW	LOW	HIGH	LOW	HIGH	LOW	HIGH
2	LOW	HIGH	HIGH	LOW	LOW	HIGH	LOW	HIGH
3	HIGH	LOW	HIGH	LOW	LOW	HIGH	LOW	HIGH
4	LOW	HIGH	HIGH	LOW	HIGH	LOW	LOW	HIGH
5	HIGH	LOW	HIGH	LOW	HIGH	LOW	LOW	HIGH
6	LOW	HIGH	LOW	HIGH	HIGH	LOW	HIGH	LOW
7	HIGH	LOW	LOW	HIGH	HIGH	LOW	HIGH	LOW
8	LOW	HIGH	HIGH	LOW	HIGH	LOW	HIGH	LOW
9	HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW

TYPE 6RIA COUNTER CARD
BINARY OUTPUT

B-6RIA-0104
9-16-'64 dl

a. Number seven, for example, has a Binary count of 1011 (see Binary States Chart, page 12-11).

b. As seven is an odd number, 1 Binary is in its 1 state.

(1) The 1 Binary output is LOW enabling the odd transistors (including Q107, the No. 7 nixie driver).

(2) The 0 Binary output is HIGH, assuring cut-off of all even nixie driver transistors.

c. Q107 base is connected to 2 Binary's 1 output and to the 4 Binary's 0 output.

(1) 2 Binary is in its 0 state.

(2) Its 1 output is HIGH.

(3) 4 Binary is in its 1 state.

(4) Its 0 output is HIGH.

d. With its emitter LOW and both base inputs HIGH, Q107 will saturate, lighting No. 7 in the nixie.

e. Investigation will show that all other nixie drivers will be either cut off or conducting slightly.

f. Only Q107 will be saturated.

9. The nixie driver that is saturated at the end of Print Command count condition will remain saturated (retaining the readout on the nixie) until a reset pulse, at the start of count condition resets the counters to zero.

a. Zero count will bring Q100 into saturation and light the nixie to 0.

H. Readout Tubes

1. Five readout tubes (nixies) are used in the 6R1A.

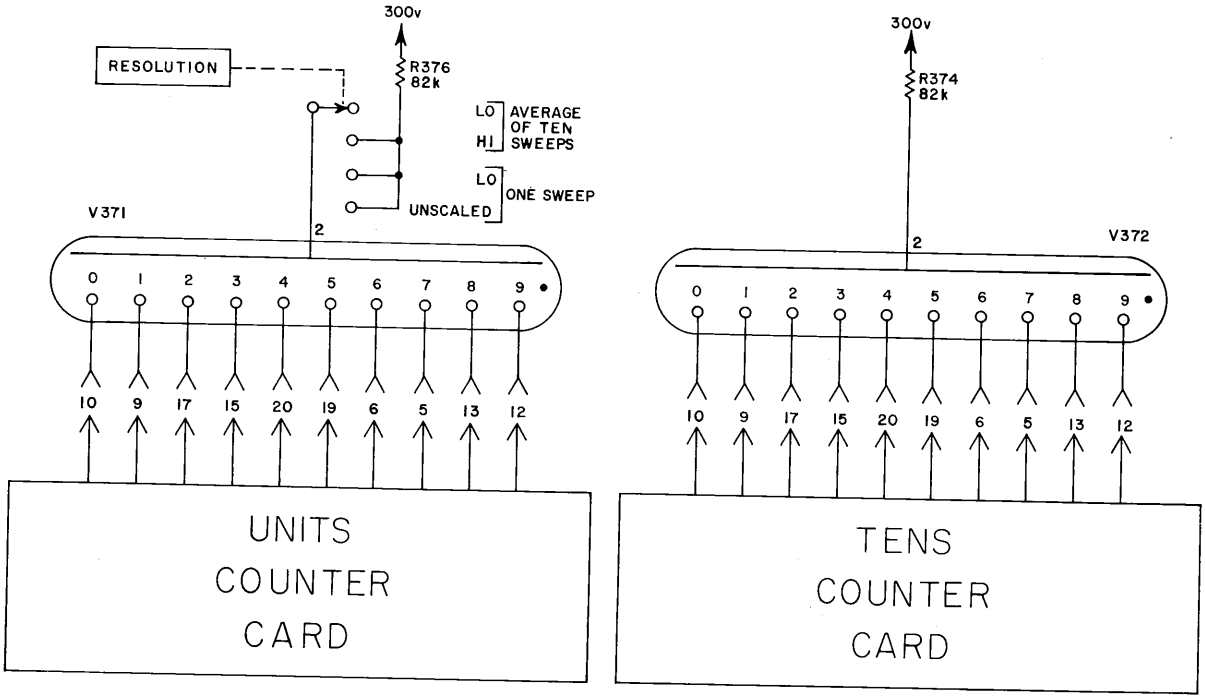
   a. V371, V372, V373 and V374 are 154-327 digit indicator tubes, Burroughs B5094.

   b. V370 is a 154-326 symbol indicator tube, Burroughs B5092.

      (1) The tube displays M, N and μ on the left of the display and V, S and A on the right.

   c. The tubes are glow discharge tubes that ignite at about 170v and operate at about 135v.

2. The four digit nixies connect to the four counter cards.



TYPE 6RIA
READOUT NIXIES

B—6RIA—0121
9—23—'64 jg

a. The nixie anodes are tied through 82k resistors to 300v.

b. The cathodes are tied to the collectors of the nixie driver transistors in the counter cards.

c. When a driver transistor is ON, the collector drops, pulling its nixie cathode to near ground.

d. Since one driver transistor on each counter card will be conducting at all times, providing a ground return, the nixie will ignite at the time of instrument turn-on, and remain on as long as the instrument is on.

(1) An exception is the Units nixie.

(2) When the RESOLUTION switch is in the AVERAGE OF TEN SWEEPS, LO position, the Units nixie is turned off.

(3) A section of the RESOLUTION switch opens the anode supply.

(4) This reduces, by one, the number of significant figures in a fractional readout.

e. The nixies each draw about 2 ma providing a bright glow (specs call for .6 ma to 1.5 ma).

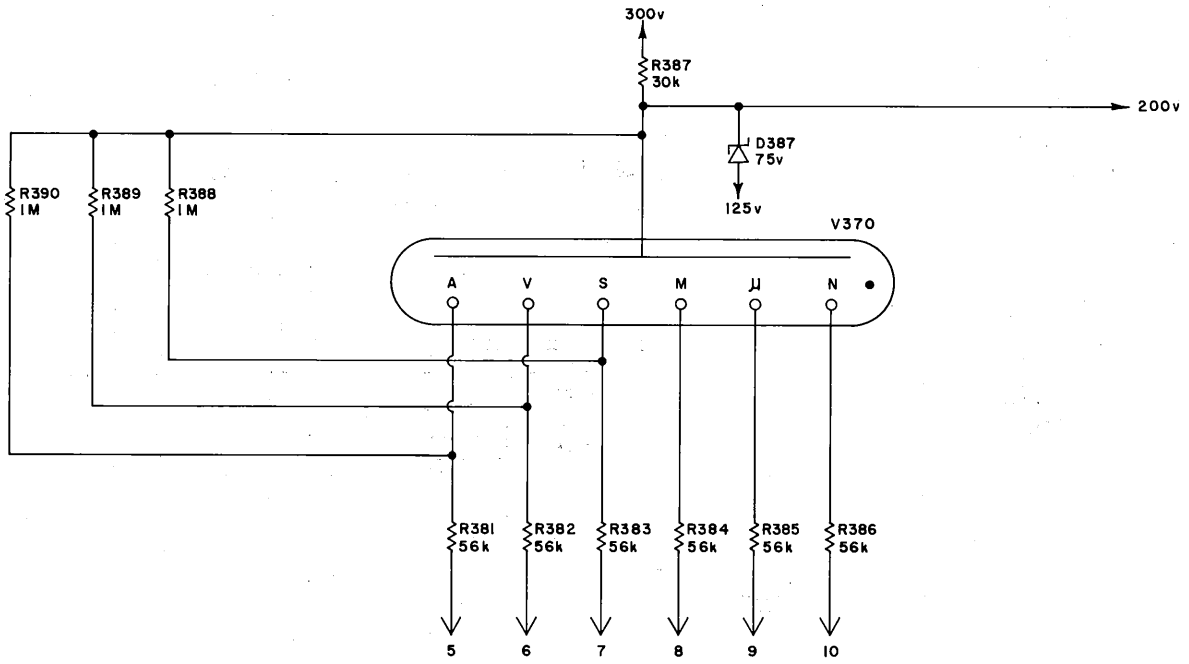
f. After the initial turn-on, the anodes set at about 135v.

3. The Units of Measure nixie anode connects to 300v through 30k.

a. A 75v zener (D387), referenced to 125v) sets the anode at 200v.

b. The cathodes are grounded through 56k resistors, the RESOLUTION switch and various Time switches in the Horizontal Plug-In and Volts/cm switches in the Vertical Plug-In.

(1) A cathode ground causes the cathode to glow.



TYPE 6R1A
UNITS OF MEASURE NIXIE

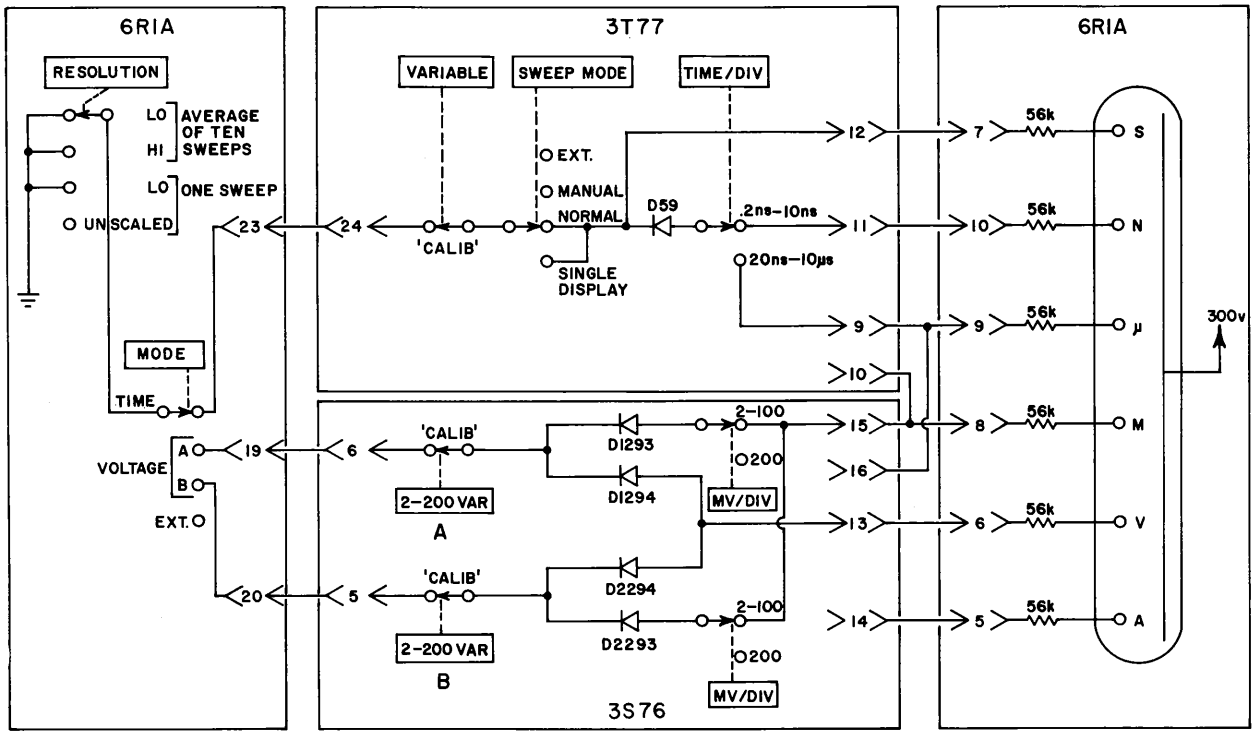
B-6R1A-0124
10-1-'64 dl

c. The tube provides for two simultaneous displays -- μs, mv, etc. (V appears alone in the 200 position of the MV/DIV switch and S appears alone with the 3B2).

(1) A is not used in the 6R1A.

d. 1 meg resistors, R388, R389, supply leakage current for diodes in the plug-ins and 262.

4. Units of Measure Ground Paths



TYPE 6RIA
GROUND PATH UNITS OF MEASURE NIXIE

B—6RIA-0122
9-25-64 jg (A)

a. The RESOLUTION switch provides the ground for all the nixie cathodes.

(1) Grounds are present in both the HIGH and LOW sections of the AVERAGE OF TEN SWEEPS positions and in the LOW portion of the ONE SWEEP position.

(2) In the UNSCALED, ONE SWEEP position, the ground is open, turning off the Units of Measure Nixie.

b. The MODE switch selects the ground path to the TIME symbols (S, N, μ) and to the VOLTS symbols (m V).

(1) The MODE switch also selects the channel in the Vertical plug-in that controls the VOLTS symbols.

c. In the Time Base plug-in, the TIME symbol ground passes through the VARIABLE TIME/DIV detent switch.

(1) The ground is present only in the CALIB position.

d. The ground passes through the SWEEP MODE switch (3T77) in the NORMAL and SINGLE DISPLAY positions only -- open in the EXT and MANUAL positions.

e. After passing through the SWEEP MODE switch, the ground connects to the S cathode.

f. Passing through D59 (3T77), the ground for the N and μ cathodes is selected by the TIME/DIV switch (3T77).

(1) The .2 μs - 10 μs positions ground the N cathode

(2) The 20 μs - 10 μsec positions ground the μ cathode.

(3) D59 prevents the S cathode from being grounded if, in some future Vertical plug-in, the μ cathode is grounded in the Vertical as well as the Sweep plug-in.

g. When the MODE switch (6R1A) is in the VOLTS position, either Channel A or Channel B in the Vertical plug-in is selected to carry the VOLTS symbol grounds.

h. The ground passes through the 2 - 200 VAR detent (3S76).

(1) The ground is connected in the CALIB detent position only.

i. A ground at the 2 - 200 VAR control will ground the V cathode through Dp294 or D2294.

j. The MV/DIV switch (3S76) selects a ground for the M cathode.

(1) The M cathode is grounded in the 2 - 100 ranges.

(2) The M cathode does not ground in the 200 range -- only the V lights in this position.

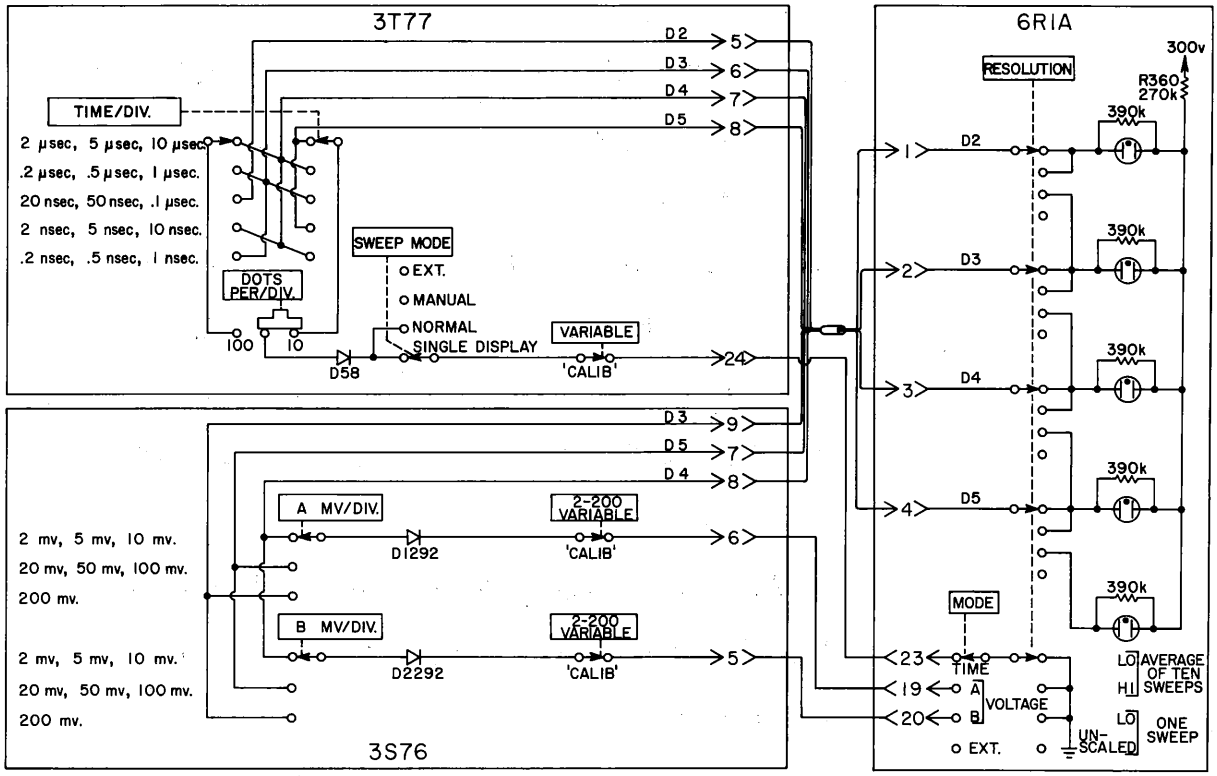
k. The diodes prevent a ground in one vertical channel from grounding the M cathode.

l. Decimal Point Neons

1. Five decimal point neons are used in the 6R1A readout.

2. The neons are all tied to 300v through 270k.

3. A ground on the other anode of each neon will cause it to glow.



TYPE 6R1A
GROUND PATH DECIMAL-POINT NEONS

B-6R1A-0123
10-1-'64 ms

4. Ground paths for the decimal neons include the RESOLUTION switch in the 6R1A, Time switches in the Sweep plug-in and MV/CM switches in the Vertical plug-in.

   a. Two switches, the RESOLUTION switch and the DOTS PER DIV switch (3T77) will shift a decimal point one place after it has been selected.

(1) The AVERAGE OF TEN SWEEPS position of the RESOLUTION switch will shift the decimal point one position to the left.

(2) The 100 DOTS PER DIV position of the DOTS PER DIV switch will also move the decimal one place to the left.

b. The ground originates with the RESOLUTION switch.

(1) Ground is connected in all but the UNSCALED position.

(2) The UNSCALED position turns off all decimal point neons.

c. The MODE switch (6R1A) selects the Time Base plug-in, or Channel A or Channel B of the Vertical plug-in to select the proper decimal.

(1) The TIME position selects the Time Base plug-in.

(2) A, VOLTS select Channel A of the Vertical plug-in.

(3) B, VOLTS select Channel B of the Vertical plug-in.

d. In TIME position of the MODE switch, the ground passes the detent switch of the VARIABLE TIME/DIV control.

(1) The ground path is provided only in the CALIB position.

e. The SWEEP MODE switch (3T77) passes the ground in the NORMAL and SINGLE DISPLAY positions only.

f. The DOTS PER DIV switch selects one of two wafers on the TIME/DIV switch.

(1) The 100 DOTS PER DIV position of the switch provides ten times as many clock pulses for a given measurement as the 10 DOTS PER DIV position.

(2) The decimal is moved one place to the left in the 100 DOTS PER DIV position.

(3) The 2 μsec, 5 μsec and 10 μsec/DIV positions of the TIME/DIV switch, for example, selects the No. 4 decimal in the 100 DOTS position and the No. 5 decimal in the 10 DOTS position -- AVERAGE OF TEN SWEEPS will shift to the No. 3 decimal.

g. The A, VOLTS position of the MODE switch (6R1A) selects Channel A of the Vertical plug-in.

(1) The ground passes through the detent (CALIB) position of the 2 - 200 VARIABLE control.

h. The MV/DIV switch selects one of three decimal points.

(1) 2 mv to 10 mv selects the No. 4 decimal.

(2) 20 mv to 100 mv selects the No. 5 decimal.

(3) 200 mv/DIV selects the No. 3 decimal.

i. Once a decimal point has been selected, the RESOLUTION switch makes a final selection.

(1) If the No. 3 decimal has been selected, for example, the RESOLUTION switch in the AVERAGE OF TEN SWEEPS position will change the selection to No. 2 decimal.

XIII. ANALOG DISPLAY CARD

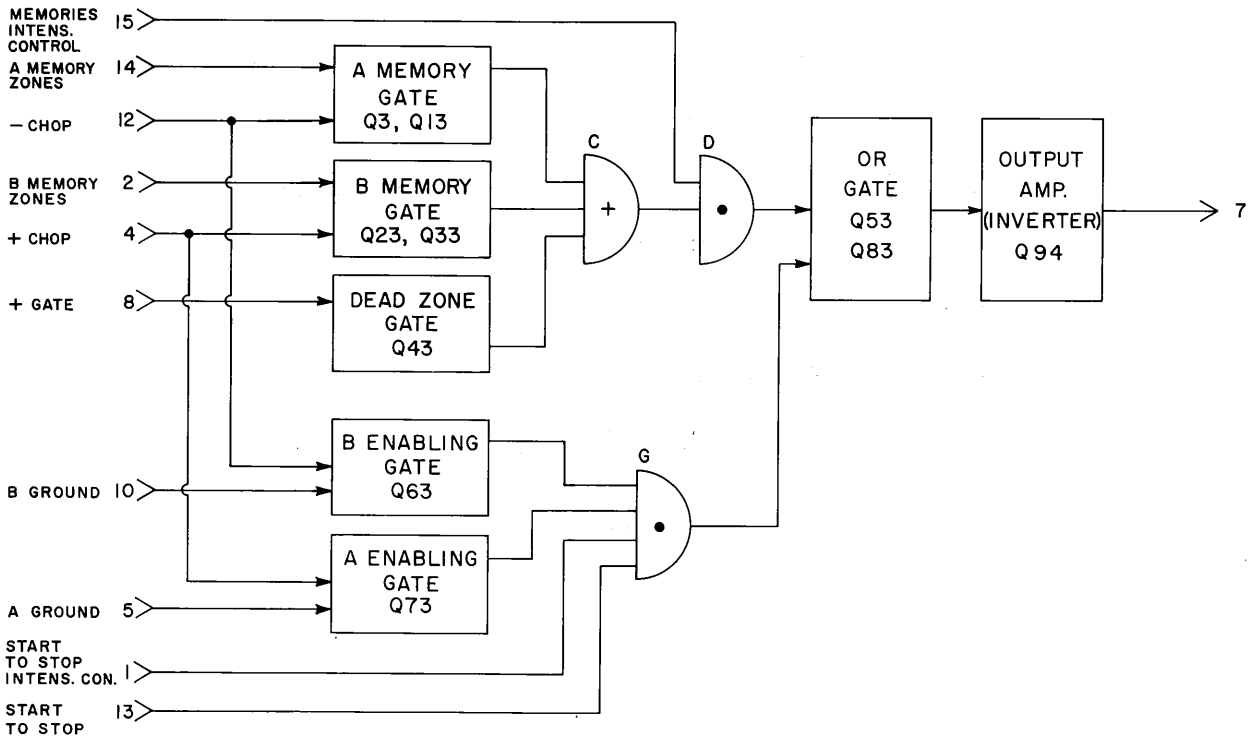
A. The Analog Display circuits intensify the CRT display during the Dead Zone, the 0% Zone, the 100% Zone and the area between the START and STOP period in time measurements.

1. The trace is intensified by increasing the CRT grid potential.
2. During dual trace operation, intensification is added to the appropriate trace on the display.

B. Circuits that comprise the Analog Display Circuits:

1. Channel A Memory Gate; Q3, Q13.
2. Channel B Memory Gate; Q23, Q33.
3. Dead Zone Gate, Q43.
4. Channel B Start-to-Stop Enabling Gate, Q63.
5. Channel A Start-to-Stop Enabling Gate, Q73.
6. OR Gate; Q53, Q83.
7. Output Amp (Inverter), Q94.

C. Block Diagram



D. Inputs

1. A Memory Zones on pin 14.
   a. Negative going composite 0% and 100% Zone pulses.
   b. From 20v to 0v.
   c. From Channel A Memory Card.
   d. The signal is present whenever Channel A of the vertical plug-in is functioning, even though Channel A is not displayed.
   e. The pulse is time variable by adjustment of the A 0% and 100% Zone controls.
2. B Memory Zones on pin 2.
   a. Same as Channel A Memory Zones except from Channel B Memory Card.
3. + Gate on pin 8.
   a. From the 0% Zone Card.
   b. An 18v positive going gate (0v to 18v).
   c. The Gate is delayed* about 5% of sweep time (about 5 mm of graticule space) from the Sweep Gate.
   d. The Gate provides CRT intensification (called the Dead Zone) for the first 5% of the sweep.
4. Start to Stop pulse on pin 13.
   a. From the Master Gate.
   b. An 18v (from 18v to 0v) negative going pulse.

* See 0% Zone Card.

c. It starts (negative step) when the Start Multi (Master Gate Card) flips and stops (positive step) when the Stop Multi switches.

5. Plus and Minus Chop.

a. The CHOP waveforms (40v peak-to-peak) are taken from the dual-trace switching multi in the vertical plug-in.

(1) The waveform is used to Gate on CRT intensification on the appropriate trace during dual trace operation.

b. The push-pull CHOP waveform is developed in the 0% Card.

c. The Chopping rate is equal to the sampling rate of the dual trace plug-in.

d. + Chop enters on pin 4 as a 20v square wave (0v to 20v).

e. - Chop appears on pin 12 as a 20v square wave.

f. + Chop is at 20v when Channel A is being displayed.

6. CRT INTENSIFICATION controls.

a. Pin 14 is tied to +20 by the Memory Zones portion of the CRT INTENSIFICATION switches (in the OFF position) to inhibit Memory Zones intensification.

(1) In the ON position, the connection to 20v is broken.

b. Pin 1 is tied to 20v by the START-TO-STOP portion of the CRT INTENSIFICATION switches to inhibit Start-to-Stop intensification.

7. Channel A and B Grounds.

a. Pin 10 is grounded by a section of the TIMING START switch or TIMING STOP switch in the Channel B positions.

(1) The Ground overrides the - Chop and allows Start-to-Stop intensification during the time B Trace is displayed.

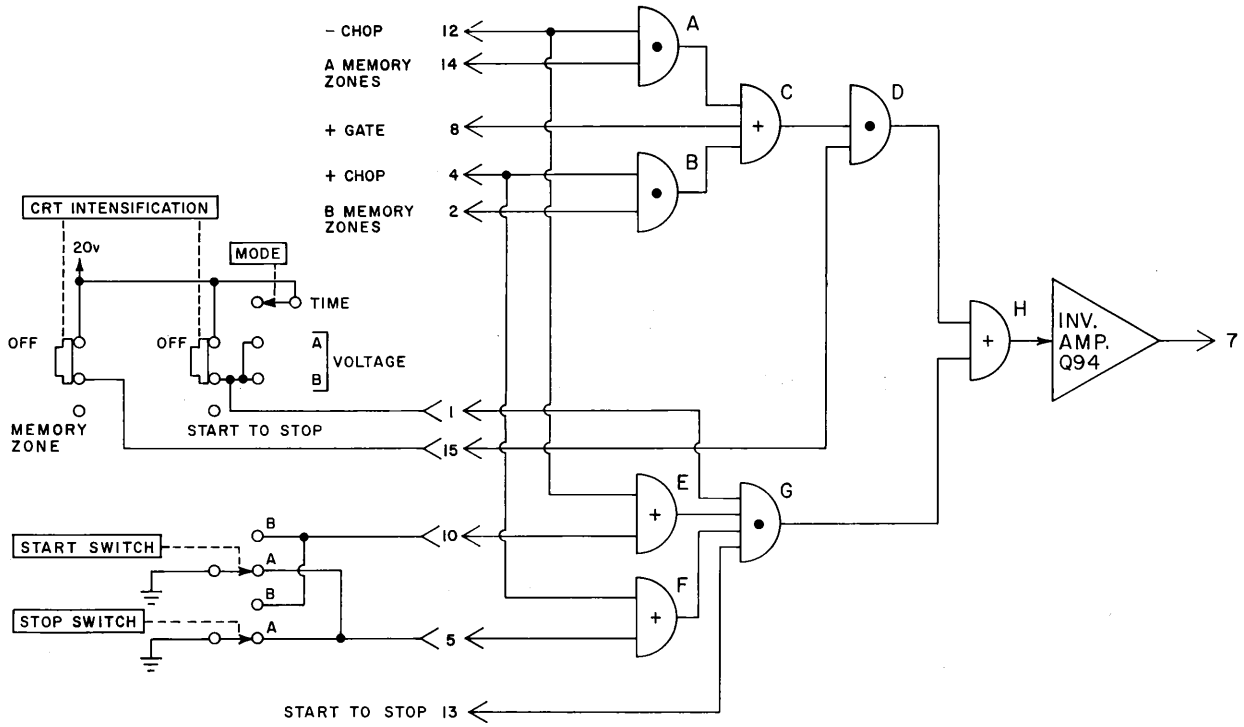
b. Pin 5 is grounded by a section of the TIMING STOP or TIMING START switch in the Channel A positions.

(1) With pin 5 grounded, Start-to-Stop intensification may appear on A Trace.

E. Outputs

1. The only output is the Analog Display waveform at pin 7.
2. The waveform is composed of positive going pulses (from 0v to 20v) representing each intensified zone.
3. The waveform is fed the Type 567 CRT grid, superimposed on the unblanking signal.

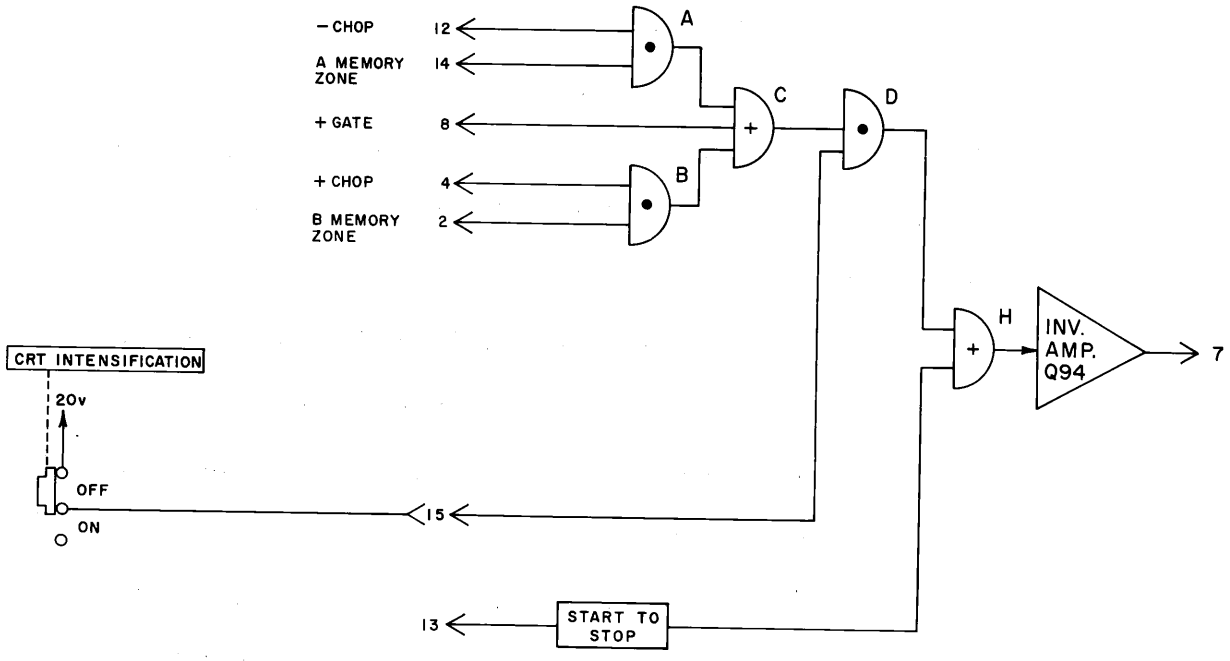
G. System Logic



TYPE 6RIA ANALOG DISPLAY CARD
LOGIC DIAGRAM

B-6RIA-0114
9-23-'64 dl

1. Logic functions of the Analog Display Card can be illustrated using four AND Gates and four OR Gates.
2. LOW level logic is used throughout the card.
   a. A LOW level indicates the presence of a signal.
   b. A HIGH level (20v) is the absence of a signal.
3. OR Gate H is a summing circuit that combines analog information from the Memory Zones (including the Dead Zone) and Start-to-Stop intensification voltage.
   a. When either (or both) input is LOW, the output is LOW.
4. The Memory Zones circuit consists of three AND Gates and one OR Gate.



TYPE 6RIA ANALOG DISPLAY CARD
MEMORY ZONE LOGIC

B-6RIA-0115
9-23-'64 dl

a. The Memories Zone circuits provide a method of displaying Memory Zone and Dead Zone intensification on the proper trace of a dual-trace display.

b. 0% and 100% Zones are generated (0% Card and Memories Card) for both Channel A and Channel B displays.

c. The zones are independently time variable (front panel controls) and independently width variable (screwdriver adjust on 0% and Memories Cards).

d. The Dead Zone is generated by the + Delayed Gate and is not variable.

(1) The Dead Zone appears on both traces of a Dual Trace display so need not be identified with one trace.

e. A switch is provided which turns off all Memory Zone and Dead Zone intensification.

5. AND Gate A receives the negative going composite 0% and 100% zones and the - Chop waveforms (when the Vertical Plug-In is in Dual Trace operation).

a. When the Chop waveform is LOW, AND the Memory Zone voltage is LOW, Gate A has an output (LOW).

b. The Chop waveform originates in the dual-trace switching multi in the Vertical Plug-In.

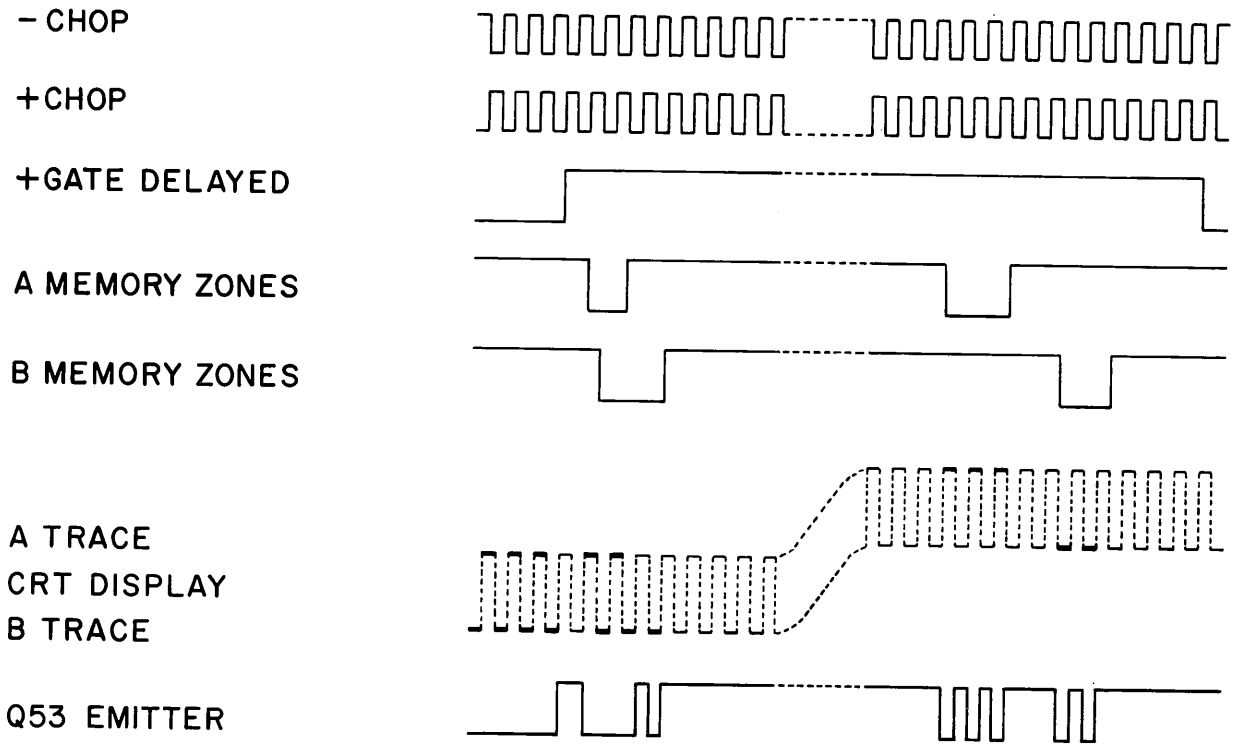
(1) The Multi switches with each sample of the sampling system; one dot appearing on Channel A and the next on Channel B.

c. The negative excursion of the - Chop waveform (LOW logic level) appears as the A trace is being sampled.

d. AND Gate A, therefore, passes A Memory Zone analog information only while the dots forming the A traces are being displayed.

(1) When the Vertical Plug-In Dual Trace switch is in A only, pin 12 goes to ground.

(2) In this case, A Memory Zone information is gated on with no interruption.



TYPE 6RIA ANALOG DISPLAY CARD
MEMORY ZONES WAVEFORMS

B-6RIA-0116
9-29-64 dl Ⓐ

6. AND Gate B receives composite 0% and 100% Memory Zone pulses from the B Memories Card, and the + Chop waveform.
   a. When the + Chop waveform is LOW, AND the B Memory Zone pulses are present (LOW), Gate B has an output (LOW).
   b. The negative excursion of the + Chop waveform occurs when Channel B is being sampled.
   c. During dual trace operation, AND Gate B passes Memory Zone information only when the dots that comprise the B trace are present.
      (1) When the Dual Trace switch is in B only position, pin 4 is at ground.
      (2) B Memory information will pass AND Gate B uninterrupted.
7. OR Gate C has inputs from AND Gate A, AND Gate B and from pin 8.
   a. The input from pin 8 is the Delayed Plus Gate from the 0% Card.
      (1) The Gate waveform is LOW until about 5% of the sweep is passed.
      (2) This period is called the Dead Zone.
      (3) The Dead Zone intensified portion of the trace is an indication that valid measurements cannot be taken from this portion of the trace.

b. If the input from AND Gate A, OR the input from AND Gate B, OR the + Gate is LOW, then OR Gate C output is LOW.

c. The output from Gate C, therefore, can be either the A Memories Zones, B Memories Zones, or the Dead Zone; OR any combination.

(1) The + Gate connects directly to Gate C input and is always present at the output of the OR Gate.

8. AND Gate D receives the output from Gate C and a connection from the Memory Zones portion of the CRT INTENSIFICATION switch.

a. The switch could be called an inhibiting control.

(1) In the OFF position, it ties pin 15 to +20v.

(2) This places the input at a HIGH logic level.

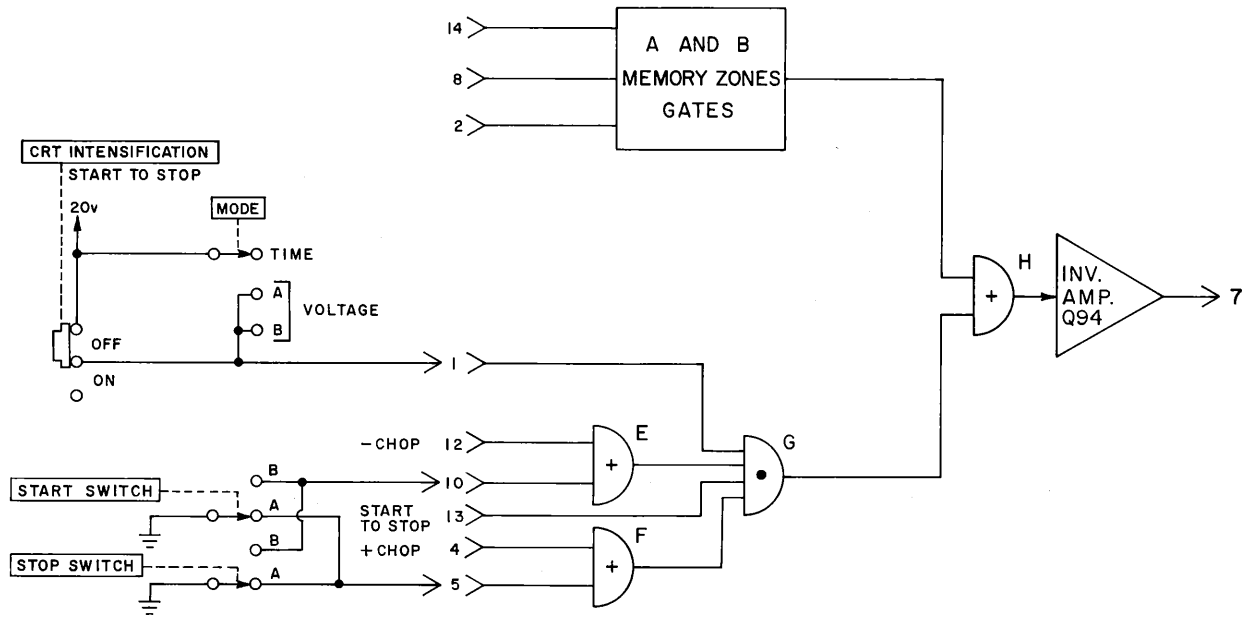
(3) The ON position opens the switch allowing pin 15 to drop to -12v (LOW logic level).

b. If the input from pin 15 is LOW (switch in ON position), AND the input from Gate C is LOW, the AND Gate D has an output (LOW).

c. The output from Gate D, therefore, is the same as the output from Gate C (composite A Memory 0% and 100% Zones, B Memory 0% and 100% Zones, and/or Dead Zone pulses).

9. The Memory Zones information mixes, in OR Gate H, with the output from the Start-to-Stop Gates, and is fed to the Output Inverter Amplifier.

10. The Start-to-Stop intensification circuits consist of two OR Gates (E and F) and an AND Gate (Gate G).



TYPE 6RIA ANALOG DISPLAY CARD
START TO STOP LOGIC

B-6RIA-0117
9-24-'64 dl

a. Provisions are made to intensify the Start-to-Stop Zone on both traces of a dual-trace display or to intensify either trace.

11. OR Gate E has two inputs, - Chop and a connection to a possible ground through the TIMING START or TIMING STOP switch and pin 10.

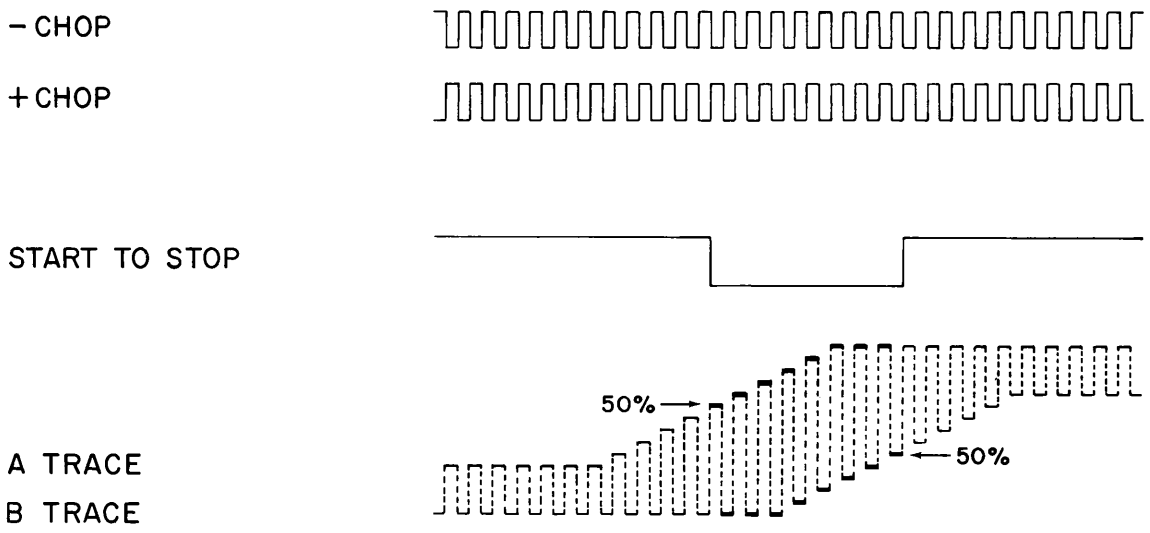
a. If the - Chop waveform is at 0v (LOW logic level) OR pin 10 is at ground (LOW logic level), Gate E has an output (LOW).

b. Pin 10 is at ground when either the TIMING START switch or the TIMING STOP switch is in the B position.

12. OR Gate F receives + Chop and a possible ground through the TIMING STOP or TIMING STOP switch and pin 5.

a. If the + Chop waveform is LOW OR pin 5 is at ground, Gate F has an output (LOW).

b. Pin 5 is at ground when either the TIMING START switch or the TIMING STOP switch is in its A position.



TYPE 6RIA ANALOG DISPLAY CARD
START TO STOP WAVEFORMS

B-6RIA-0118
9-29-'64 dl

13. AND Gate G has four inputs.

    a. The output from OR Gate E.

    b. The output from OR Gate F.

    c. Start-to-Stop pulses from the Master Gate through pin 13.

    d. An inhibiting voltage (+20v) from the Start-to-Stop section of the CRT INTENSIFICATION switch through pin 1.

        (1) The inhibiting voltage is present when the Start-to-Stop switch is OFF.

        (2) The MODE switch also provides the 20v inhibiting voltage when in the VOLTAGE positions.

14. If <u>all four</u> inputs to the AND gate are LOW, the gate has an output (LOW).

15. If the grounds to both pins 5 and 10 were open (a hypothetical condition not possible in the 6R1A), Gates E and F would have an output alternately.

    a. + Chop is LOW when - Chop is HIGH, etc.

    b. One gate would always be HIGH.

    c. Since Gates E and F feed into AND Gate G, the AND gate would never have an output.

        (1) <u>All</u> inputs must be LOW for the AND Gate to have an output.

16. If pin 10 is at ground, for example, Gate E has an output (at ground, overriding the - Chop).

    a. With pin 10 grounded and pin 5 not grounded, + Chop would provide Gate F with an output 50% of the time.

b. When + Chop is LOW, Gate F output is LOW.

c. Since + Chop is LOW at the time B Channel is displayed, the Start-to-Stop intensification will appear on B trace.

17. When the vertical plug-in Dual-Trace switch is in A only position, the Chop waveform is not present on either pins 4 or 12.

a. Pin 4 sets at 20v.

b. Pin 12 sets at ground.

c. With pin 4 at 20v, Gate F will not have an output unless pin 5 is at ground.

(1) A START or STOP switch position A will ground pin 5, however, allowing the Start-to-Stop pulse to intensify A trace.

18. If (with Dual Trace operation) pins 5 and 10 are both grounded* (START switch on A and the STOP switch on B, for example), Gates E and F will have their outputs at ground (overriding the Chop waveforms).

a. If there is no inhibiting voltage on pin 1, the Start-to-Stop intensification will appear on both traces.

b. Summarizing this condition, Gate G has the following inputs:

(1) Pin 1 at LOW logic level.

(2) Gate E output at LOW logic level.

(3) Gate F output at LOW logicl level.

(4) When the Start-to-Stop pulse arrives, pin 13 drops to the LOW logic level for the pulse duration.

(5) Gate G has an output for the Start-to-Stop pulse duration.

* Pins 5 and 10 are grounded also when either TIMING switch is in the MANUAL position.

19. OR Gate H mixes the outputs, if any, from the Memories Gates and the Start-to-Stop Gates to provide the composite intensification voltage.

20. The Output Inverter Amplifier provides proper polarity for grid drive to the CRT.

H. Memories Gates; Q3, Q13, Q23, Q33, Q43

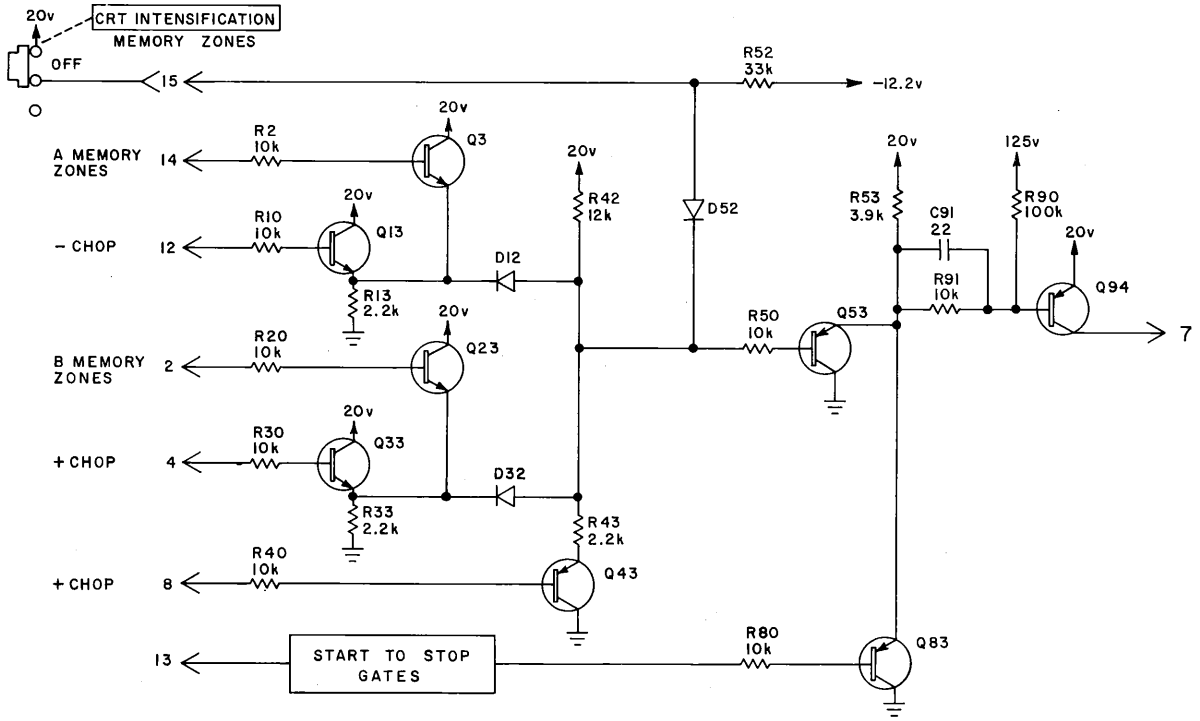
1. The Memories Gates use five transistors and three diodes.

   a. Q3, Q13, Q23 and Q33 are 151-069, 2N1304 germanium NPN transistors.

   b. Q43 is a 151-071, 2N1305 germanium PNP transistor.

   c. D12 and D32 are 152-075 germanium diodes.

   d. D52 is a 152-025, 1N634 germanium diode.



TYPE 6RIA ANALOG DISPLAY CARD
MEMORIES AND DEAD ZONE GATES

B-6RIA-0119
9-25-'64 dl

2. Q3 and Q13 make up AND Gate A.

   a. Prior to sweep, pin 14 is at 20v.

   b. Q3 is saturated with the emitter at 20v.

      (1) R2 limits base current to 2 ma.

   c. If the Vertical Plug-In is set for Dual Trace operation, pin 12 will swing between 0v and 20v.

      (1) When at 20v, Q13 saturates, holding its emitter at 20v.

      (2) When pin 12 drops to 0v, Q13 cuts off as conducting Q3 holds Q13 emitter at 20v.

   d. Q3 emitter (A Gate output) is at 20v (HIGH logic level).

   e. When a 0% or 100% zone pulse from A Memory arrives, pin 14 drops to ground.

      (1) Q3 cuts off.

      (2) If pin 12 (- Chop waveform) is at 20v, conducting Q13 will hold its emitter at 20v.

      (3) Q13 emitter is at 20v -- no output.

      (4) When the Chop waveform drops Q13 base to 0v, Q13 cuts off.

   f. Q3 and Q13 emitters are now considered to have an output.

      (1) The emitters <u>may</u> be held up by conducting D12, but since Q3 and Q13 are not conducting, the Gate has an output.

g. Since - Chop is at ground while A trace is being displayed, the - Chop will pass A Memory zones pulses during the time A trace is being displayed.

h. If the Dual-Trace switch is in A only position, pin 12 will be at ground, allowing A Memory Zones to pass.

i. If the Dual-Trace switch is in B position, pin 12 will be at 20v.

(1) Q13 will conduct.

(2) The Gate cannot have an output.

(3) A Memory Zones cannot pass.

3. Q23 and Q33 constitute AND Gate B.

a. Operation is the same as AND Gate A.

b. When pin 2 is LOW (B Memory Zones present) AND pin 4 is LOW (+ Chop at 0v while B trace is displayed), the gate has an output.

4. OR Gate C is composed of D12, D32 and Q43.

a. If Gate A is LOW (Q3 and Q13 cut off), OR if Gate B is LOW (Q23 and Q33 cut off), OR if pin 8 is LOW, the gate will have an output.

b. Note that with Q43 conducting and all other transistors cut off, three similar current paths are formed from D42 to ground.

(1) Through D12 and R13 to ground.

(2) Through D32 and R33 to ground.

(3) Through R43 and Q43 to ground.

c. If any one of these conducting paths is present, the bottom of R42 (the Gate output) will pull down far enough to saturate Q94, the Output Amp Transistor, and provide an output.

(1) One path to ground drops the Gate output to 3.1v.

(2) Two paths to ground drop the Gate output to 1.7v.

(3) All three inputs at ground drop the Gate output to 1.15v.

d. Prior to sweep, the + Gate at pin 8 is at 0v.

(1) Q43 is conducting.

(2) The emitter is down to about ground.

(3) This consitutes an output (the Dead Zone).

e. When the + Gate arrives (about 5 mm of trace after the start of sweep), pin 8 raises to 18v.

(1) Q43 collector rises to 18v.

f. When the output of Gate A or Gate B drops to its LOW state, OR Gate C will have an output.

5. AND Gate D is composed of D52 and its equivalent input resistance (R43 and/or R33, and/or R13).

a. If D52 cathode is DOWN, AND pin 15 is DOWN, the gate has an output.

b. Pin 15 ties through the Memory Zones section of the CRT INTENSIFICATION switch to +20v.

c. When the switch is OFF, pin 15 ties to 20v.

(1) The 20v provides an inhibiting voltage.

(2) D52 conducts, pulling up on its cathode and Q53 base.

(3) The Gate has no output.

d. When the switch is ON, the circuit is open.

(1) D52 cuts off as its anode drops to -12v, pulled down by R52 to -12.2v.

e. If the bottom of R42 is LOW, AND Gate D has an output (LOW).

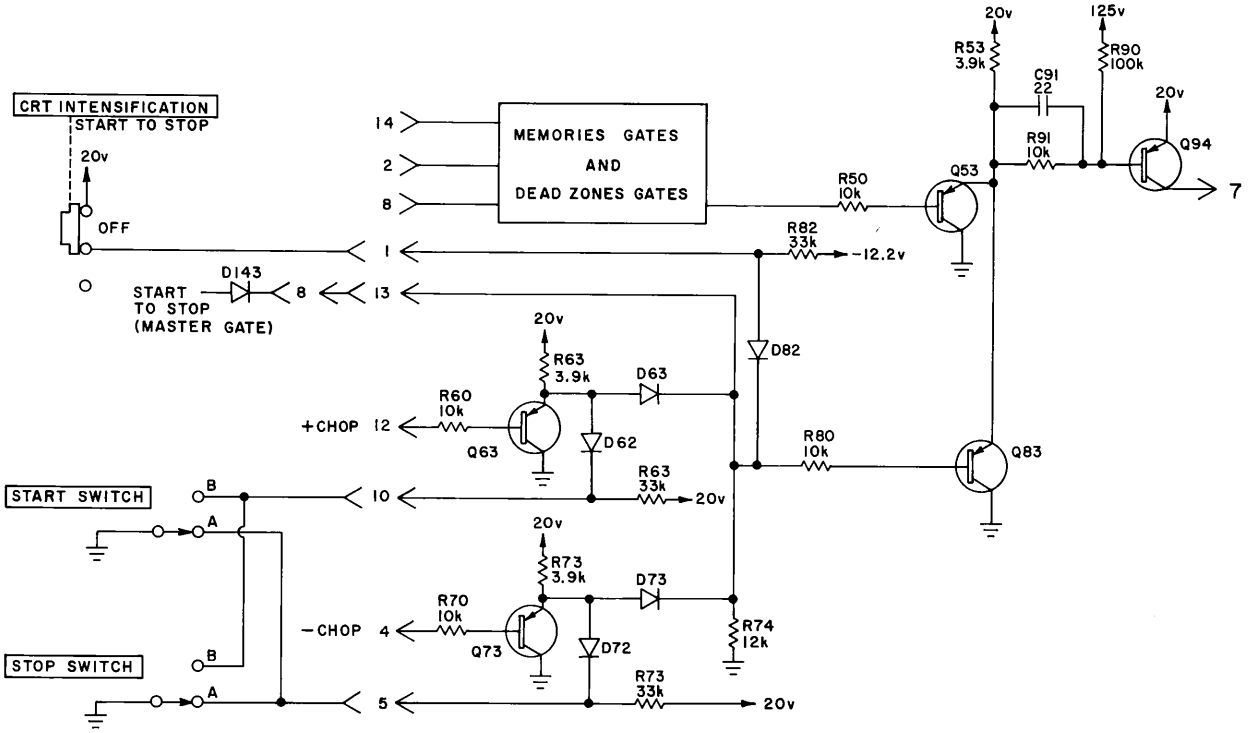
I. Start-to-Stop Gates; Q63, Q73

1. The circuit uses two transistors and five diodes.

a. Q63 and Q73 are 151-071, 2N1305 germanium PNP transistors.

b. D62, D63, D72 and D73 are 152-075 germanium diodes.

c. D82 is a 152-025, 1N634 germanium diode.



2. Q63 and D62 make up OR Gate E.

   a. If pin 10 is at ground OR if pin 12 is at ground, the gate has an output (is at ground).

   b. Pin 10 ties to ground through a section of the TIMING START or TIMING STOP switches -- they are connected in parallel.

      (1) When one or both of the switches is in one of the B positions, pin 10 is at ground.

      (2) D62 conducts, pulling its anode to ground.

      (3) This constitutes an output.

      (4) If both TIMING switches are in an A position, pin 10 raises to 20v -- pulled up through R63.

      (5) The Gate has no output.

   c. Pin 12 has the - Chop waveform when the Vertical Plug-In is operating Dual-Trace.

      (1) When the - Chop is in its LOW level (0v), Q63 saturates, and its emitter drops to ground.

      (2) This constitutes an output.

      (3) When the - Chop waveform is in its HIGH level (+20v), Q63 cuts off and its emitter rises to 20v.

   d. Note that when pin 10 is at ground, D62 pulls down to ground, overriding any action of the - Chop waveform -- even though Q63 cuts off its emitter is held down by D62.

e. In summary, when pin 10 is at ground, OR Gate E has an output.

(1) When pin 10 is at 20v, the Gate has an output only when - Chop is at its LOW level.

3. Q73 and D72 make up OR Gate F.

a. Operation is essentially the same as OR Gate E.

b. A ground at pin 5 (A position of the TIMING START or TIMING STOP switch) will pull D72 into conduction overriding the action of the + Chop waveform.

c. If pin 5 is not at ground, however, the gate will have an output when the + Chop waveform is at its LOW level.

4. AND Gate G is composed of D82, D63, D73 and D143 (located on the Master Gate Card).

a. The four inputs to the Gate:

(1) The output from Gate E -- Q63 emitter and D52 anode must be LOW.

(2) The output from Gate F -- Q73 emitter and D72 anode must be LOW.

(3) The Start-to-Stop pulse from the Master Gate through pin 13 -- the pulse must be present (LOW logic level).

(4) The 20v inhibiting voltage through the START-TO-STOP section of the CRT INTENSIFICATION switch -- the switch must be open (ON).

b. The AND Gate output is the junction of the four diodes.

c. When an input is at ground, the associated diode is cut off.

(1) If any one of the diodes is pulled up to 20v, the output will be HIGH.

(2) The gate has no output.

(3) If all four diodes are cut off, the Gate output is LOW.

d. When the Gate output is at ground, the AND Gate has an output.

J. OR Gate H and the Inverter Amplifier; Q53, Q83, Q93.

1. Q53 and Q83 make up OR Gate H and Q94 is the Output Inverter Amplifier.

a. The transistors are 151-071, 2N1305 germanium PNP transistors.

2. Inputs to the OR Gate:

a. The output from the Memories Gates.

b. The output from the Start-to-Stop Gates.

3. If either transistor (Q53, Q83) is conducting enough to pull their common emitters below 10v, Q94 will saturate.

a. A divider composed of R90, R91 sets Q94 base at 19.7v when Q53, Q83 emitters are at 10v.

b. Since any combination of intensification signals will drop the emitter below 3.4v, saturation of Q94 is assured.

c. Q94 collector pulls up to about 20v.

d. The 20 volts will intensify the CRT display.

4. When both Q53 and Q83 are cut off, current through R53, R91 and R90 pulls Q94 base up to 33v.
   a. Q94 is cut off.
   b. The collector drops to ground.
5. Since logic levels throughout the card are adequate to switch Q94 from cut off to saturation, the output (pin 7) is a clean waveform.

XIV. UPPER AND LOWER LIMIT NO-GO CARDS

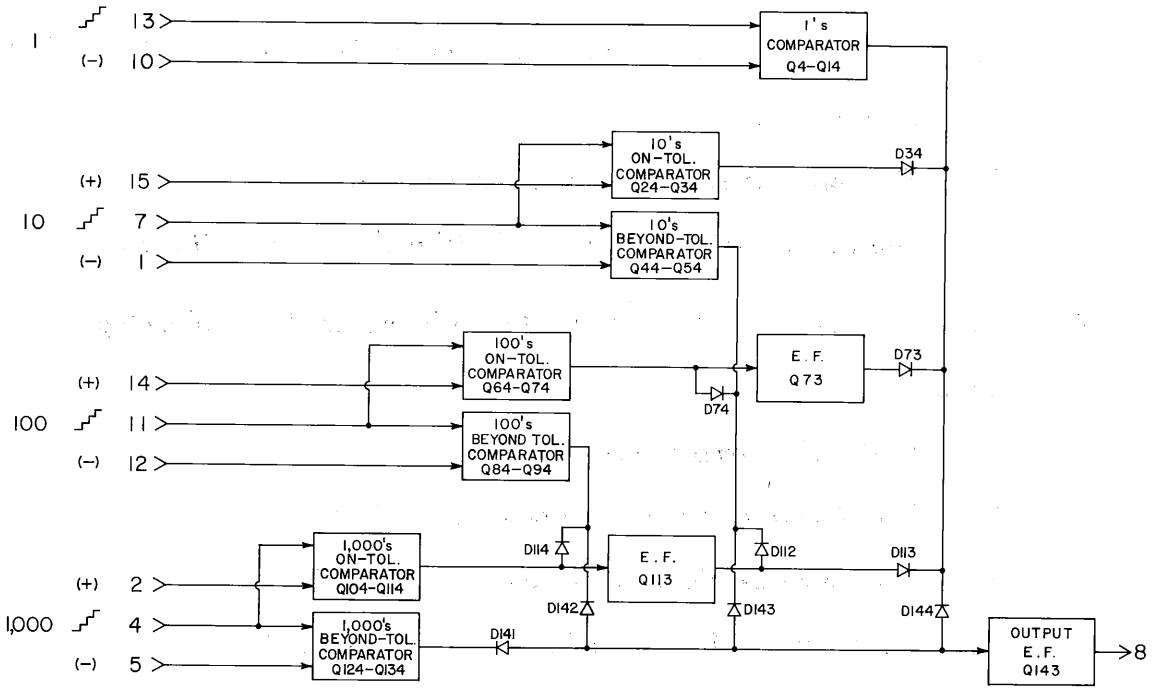
A. The Upper and Lower Limit No-Go circuits compare the count stored in the counters with limits set by the Upper and Lower Limit switches and determine which of the three GO-NO-GO lights will turn on.

1. One Upper Limit NO-GO Card and one Lower Limit NO-GO Card is provided.
2. The cards differ only in their input connections.
3. The Lower Limit NO-GO Card will be used in this discussion.

B. The Upper and Lower Limit NO-GO Cards consist of the following circuits.

1. Units (1's) Comparator; Q4, Q14.
2. Tens On-Tolerance Comparator; Q24, Q34.
3. Tens Beyond-Tolerance Comparator; Q44, Q54.
4. Hundreds On-Tolerance Comparator; Q64, Q74.
5. Hundreds Beyond-Tolerance Comparator; Q84, Q94.
6. Hundreds EF, Q73.
7. Thousands On-Tolerance Comparator; Q104, Q114.
8. Thousands Beyond-Tolerance Comparator; Q124, Q134.
9. Thousands EF, Q113.
10. Output EF, Q143.

C. Block Diagram



TYPE 6RIA NO-GO CARDS
LOWER LIMIT NO-GO BLOCK DIAGRAM

B-6RIA-0105
9-17-'64 jg

D. Inputs

1. Inputs to the Ones Comparator.

   a. Units Staircase* from the Units Counter Card.

      (1) The staircase has 9 steps, 1.7v each step; one step for each units count.

      (2) The waveform starts at 3.85v from zero count and steps up to 19.15v for the count of 9.

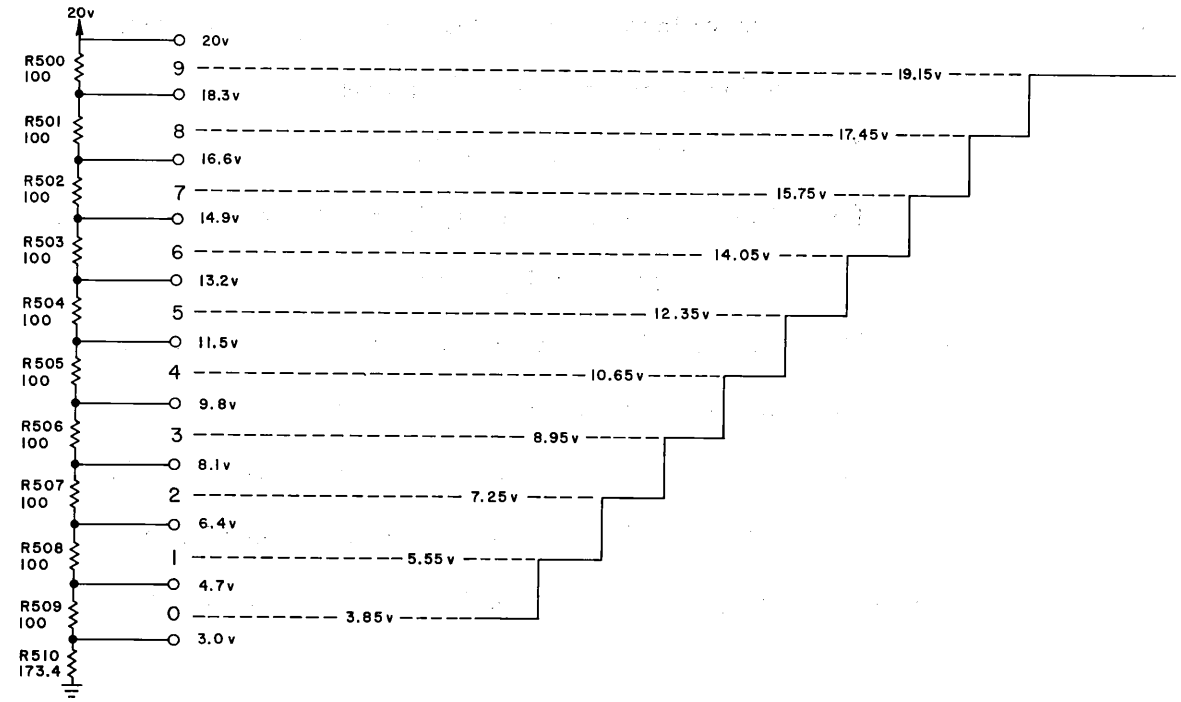
      (3) On the Upper Limit Card the staircase comes in on pin 10 and on the Lower Limit Card on pin 13.

* See Counter Cards.

b. A voltage selected by the units section of the Limits Switch.

(1) On the Lower Limit NO-GO Card this voltage will be a half step (one-half 1.7v or .85v) below the staircase voltage for the corresponding number.

(2) For the Upper Limit Card the voltage will be a half step higher than the corresponding stairstep voltage for the corresponding number.



TYPE 6RIA NO-GO CARDS
COMPARISON VOLTAGE

B-6RIA-0106
9-17-'64 dl

(3) The units voltage comes in on pin 13 on the Upper Limit Card and on pin 10 on the Lower Limit Card.

2. Inputs to the Tens Comparator.

   a. The Tens Staircase from Tens Counter Card.

      (1) The same voltage levels as the Units Staircase.

      (2) The staircase steps with each count of 10.

      (3) It enters both the Upper and Lower Limit NO-GO Cards on pin 7.

   b. Tens digit (+): A voltage selected by the Tens section of the Limit switch.

      (1) The voltage is a half step (.85v) above the staircase value for the corresponding number.

   c. The Tens digit (-) selected by the Limit switch.

      (1) The voltage is a half step below the staircase voltage for the corresponding number.

   d. The Tens digit (+) enters on pin 15 and the Tens digit (-) enters on pin 1 of the Lower Limit Card.

      (1) The inputs are reversed on the Upper Limit Card.

3. Inputs to the Hundreds Comparator and the Thousands Comparator follow the same pattern as the inputs to the Tens Comparator.

E. Outputs

1. The only output is through pin 8 to the Limit Light Driver.

   a. The Upper and Lower Limit NO-GO Cards are considered to have an output when the voltage on pin 8 is at -12v.

F. System Logic

1. The Upper and Lower Limit switches may be set to bracket the expected nixie readout.

a. A separate switch setting is required for each decade (units, tens, hundreds and thousands).

b. The Upper Limit switch will be set to a reading above the expected measurement.

c. The Lower Limit switch will be set to a reading below the readout.

d. The Limit setting must be changed when the RESOLUTION switch is changed from ONE SWEEP position to AVERAGE OF TEN SWEEPS*.

(1) The RESOLUTION switch varies the decimal on the readout.

2. If the measurement falls between the two Limit Switch settings, the MID-ZONE light will light.

3. If the measurement drops below the Lower Limit setting, the LOWER LIMIT light will light.

4. If the measurement is above the Upper Limit, the UPPER LIMIT light will glow.

5. A LOW (-12v) output is required to light a limit light.

6. Both a lower limit and an upper limit comparison must be made for each decade.

a. The thousand count must be compared with the upper and lower thousands limit set by the Limit Switches.

b. The hundreds count is compared with the upper and lower hundreds limits.

c. The tens count is compared with the upper and lower tens limits.

d. The units count is compared with the upper and lower units limits.

* See ÷10 Card.

7. A priority is given in descending order of magnitude.
   a. A BEYOND TOLERANCE count in the thousands, for example, will override the count in the hundreds, tens or units.
   b. Consider a Lower Limit setting of 7777, for example.
   c. If the count is exactly 7777, the Lower Limit light will not light.
   d. If the count is 7776, comparison will be made in the units column that will light the Lower Limit light.
   e. If the count is 7769, a comparison in the units decade will indicate ON TOLERANCE (or above tolerance).
      (1) A comparison in the tens decade, however, will show BELOW TOLERANCE, overriding the units comparison to light the Lower Limit light.
      (2) A lower reading in the hundreds decade, in turn, would take priority over a higher count in the tens decade.
   f. A count of 7876, on the other hand, would not light the Lower Limit light.
      (1) The hundreds digit would override the low count in the units digit to prevent the units comparison from lighting the Lower Limit light.
8. Comparison is made in each decade with two comparators (the units decade has only one).
   a. The comparators are termed the ON-TOLERANCE Comparators and the BEYOND-TOLERANCE Comparators.
   b. The units decade has a BEYOND-TOLERANCE Comparator only.

9. Each comparator has two inputs, the Staircase and a Digit input.

10. The Staircase is the Staircase developed in the Counter Cards.

    a. One staircase for each decade is fed to both the Upper and Lower Limit NO-GO Cards.

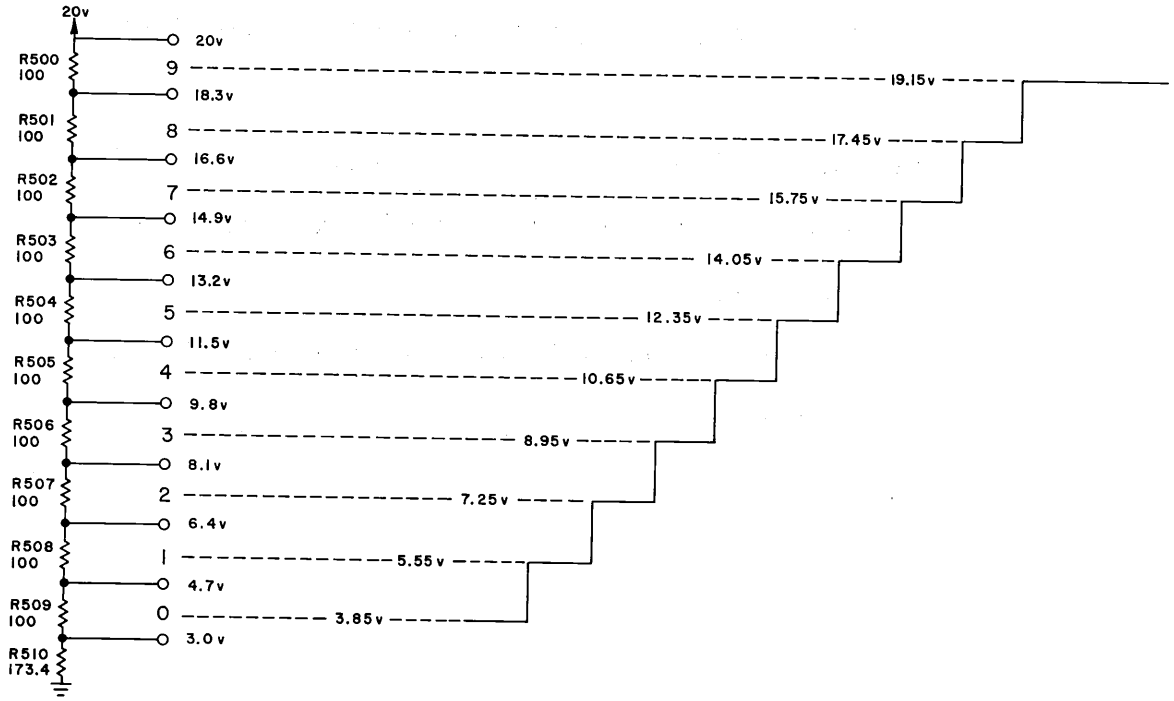
    b. The Staircase has 9 steps (one for each count) of 1.7v per step.

    c. The Staircase starts at 3.85v for the count of zero and ends at 19.15v at 9 count.

11. The Digits Inputs are selected by the Limit Switches.

    a. A separate switch is supplied for each decade for both the Upper and Lower Limits.

    b. The Limit switch selects a voltage from a divider, located in the 6R1A main frame.



TYPE 6RIA NO-GO CARDS
COMPARISON VOLTAGE

B-6RIA-0106
9-17-'64 dl

c. One divider is provided for the four decades of both Upper and Lower Limit Switches.

d. A (+) Digit input will select a voltage from the divider that is one-half step (one-half 1.7v or .85v) above the staircase value for the corresponding number.

(1) The staircase value for 5, for example, is 12.35v.

(2) The (+) Digit voltage (from the divider) is 13.2v (12.35v plus .85v).

e. A (-) Digit input will select a voltage one-half step below the staircase voltage for the corresponding number.

(1) The (-) Digit voltage for 5 is 11.5v (12.35 minus) .85v.

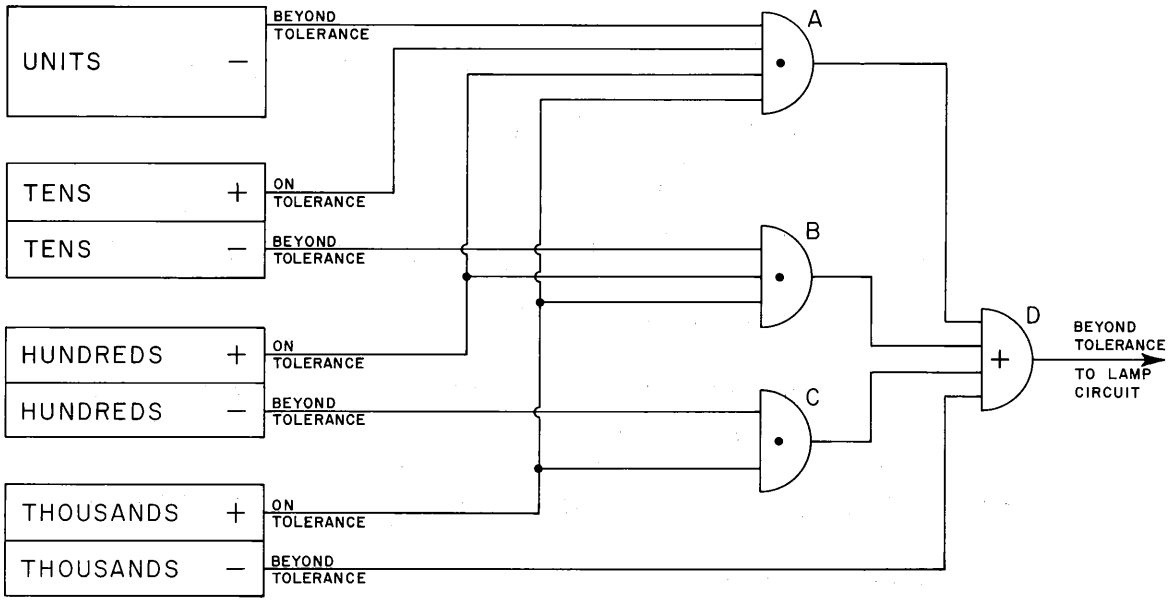
12. Each comparator has as its output two possible logic levels, HIGH and LOW.

a. The LOW logic level (-12v) ultimately lights the Limit light.

13. Referring to the block diagram; if, for comparison, the "top" input to a comparator is higher than the "bottom" input, the comparator output is HIGH.

a. If the bottom input is higher than the top input, the output is LOW.

14. The Comparator outputs pass through a series of AND and OR Gates to establish the priority or override logic.



TYPE 6RIA NO-GO LOGIC
LOWER LIMIT NO-GO LOGIC

B-6RIA-0107
9-15-'64 ms

a. AND Gate A is composed of Q14, D34, D73, D113.

(1) If all four inputs to AND Gate A are LOW, the Gate output is LOW.

b. AND Gate B is composed of Q54, D74 and D112.

(1) When all inputs are LOW, the gate output is LOW.

c. AND Gate C is composed of Q94 and D114.

(1) When both inputs are LOW, the gate output is LOW.

d. OR GATE D is composed of diodes D144, D141, D142 and D143.

(1) If any of the four inputs is LOW, the output will be LOW.

15. Consider a Lower Limit setting of 7777.

a. Since all decades are set to 7, all (+) Digit inputs would be at 16.6v and all (-) Digit inputs at 14.9v.

16. Assume a count of 7777.

a. At the end of the Print Command count condition, all staircase voltages would "freeze" at 15.75v.

b. Note that step 7 of the staircase is halfway between the (+) Digit and the (-) Digit setting for 7.

17. The Units Comparator on the Lower Limit NO-GO Card has the following conditions:

a. Top input (Units staircase on pin 13) at 15.75v.

b. The bottom input (Units (-) Digit input on pin 10) at 14.9v.

c. The top input has a higher potential than the bottom input -- the comparator output is HIGH.

(1) The HIGH output would indicate no output unless there is an override (priority) from a higher magnitude comparator.

18. The Tens On-Tolerance Comparator has these conditions:

a. The top input (Tens staircase on pin 7) at 15.75v.

b. The bottom input (Tens (+) Digit on pin 15) at 16.6v.

c. The bottom input has a higher potential than the top input -- the comparator output is LOW.

d. D34 disconnects and does not effect the system output.

19. The Tens Beyond-Tolerance Comparator has these conditions:

a. The top input (Tens staircase on pin 7) at 15.75v.

b. The bottom input (Tens (-) Digit on pin 1) at 14.9v.

c. The top input has a higher potential than the bottom input -- the comparator output is HIGH.

d. D74, D112 and D143 disconnect with no effect on system output.

20. The Hundreds Comparators have the same input potentials as the Tens Comparators.

a. The Hundreds On-Tolerance Comparator output is LOW, disconnecting D73 and D74.

b. The Hundreds Beyond-Tolerance Comparator has a HIGH output disconnecting D114 and D142.

c. The Hundreds Comparators have no effect on the output.

21. The Thousands Comparators have the same inputs as the Tens and Hundreds Comparators.

a. The On-Tolerance Comparator has a LOW output disconnecting D113.

b. The Beyond-Tolerance Comparator has a HIGH output disconnecting D141.

c. Like the Tens and Hundreds outputs, the Thousands Comparators have no effect on the system output with these inputs.

22. Summarizing, only the Units Comparator has control.

    a. The output is HIGH; the Lower Limit light does not light.

    b. As long as the Tens, Hundreds and Thousands counts are ON TOLERANCE, the Units Comparator retains control.

23. If the count had been 7776, the Units Comparator would have had a LOW output, lighting the Lower Limit light.

    a. The upper input is at 14.05v.

    b. The lower input is at 14.9v.

    c. The lower output has the higher potential, indicating a LOW output.

24. Analyzing the forgoing condition shows that in the Lower Limit NO-GO Card, the On-Tolerance Comparators can effect the system output with a HIGH output only.

    a. The Beyond-Tolerance Comparators can influence the system output only when its outputs are LOW.

    b. This constitutes the priority or override logic.

    c. A HIGH output at the Tens On-Tolerance Comparator (a result of the Tens count being higher thant the Tens Limit Switching setting) would override a LOW output from the Units Comparator.

    d. Similarily, each higher magnitude circuit can override the lower magnitude circuits.

    e. The On-Tolerance Comparators function when a count is higher than the Limit Switch setting, overriding the lower magnitude outputs.

f. The Beyond Tolerance Comparators function when a count is lower than the Limit Switch setting, taking priority over the lower magnitude outputs.

(1) D144 disconnects in this case allowing the lower magnitude outputs to have a HIGH output while the higher magnitude output controls the system output.

25. When the count is below the Lower Limit Switch setting, the output of the Lower Limit NO-GO Card at pin 8 remains at -12v throughout the complete count.

a. If the count is at or above the Lower Limit Switch setting, the output will remain at -12v until the count reaches the Limit Switch setting, then raises to ground.

b. In this case the output returns to -12v when the Counters are reset at the start of Print Command count condition.

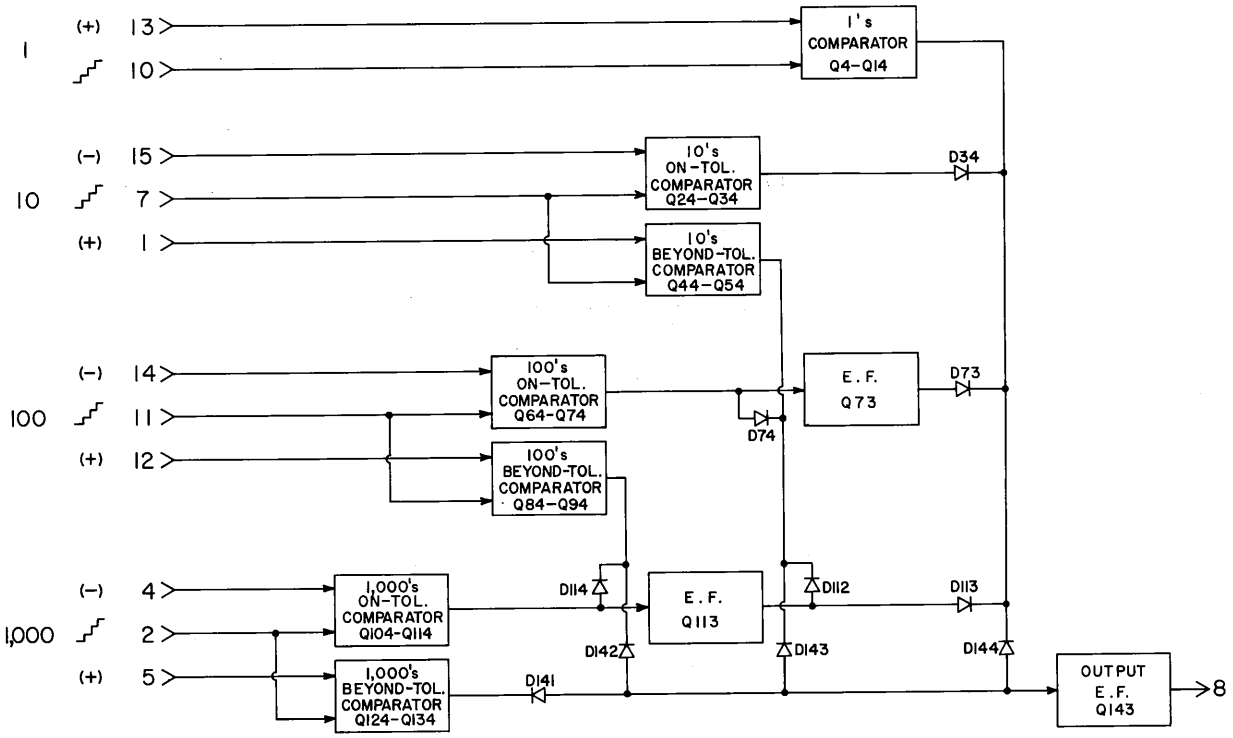
26. The Upper Limit NO-GO Card has the inputs to all comparators reversed from those found in the Lower Limit Card.

a. The (-) Digit is fed to the On-Tolerance Comparators and the (+) Digit is fed to the Beyond-Tolerance Comparators.

b. The Staircase voltages are connected to bottom input to each Comparator.

27. System Logic is the same as the Lower Limit NO-GO Card.

    a. A LOW output (-12v) constitutes an output, lighting the Upper Limit light.



TYPE 6RIA NO-GO CARDS
UPPER LIMIT NO-GO BLOCK DIAGRAM

B-6RIA-0108
9-18-'64 dl

28. When the Upper Limit switches are set to read lower than the count, the output (pin 8) will set at ground until the count equals, then exceeds the Limit Switch setting.

    a. The output then drops to -12v lighting the Upper Limit Light.

b. If, for example, only the Units decade exceeds the Limit Switch setting, the output will remain at ground as the count runs up.

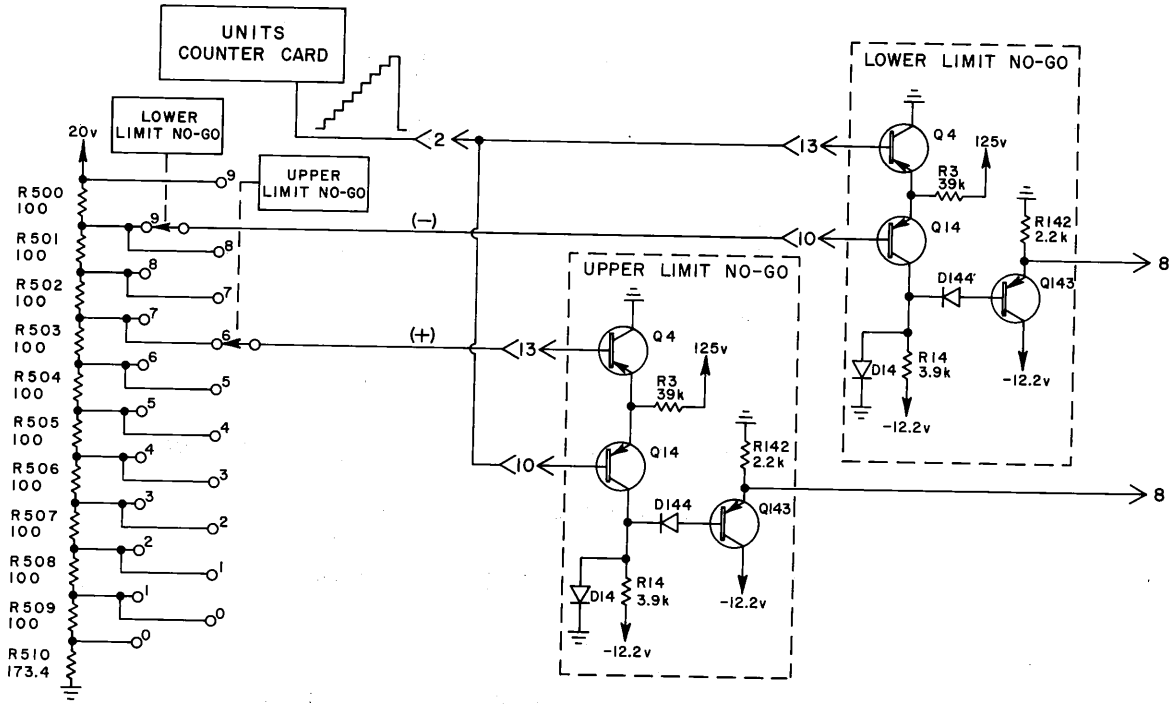
c. As the Tens decade reaches its count, the override circuits will release their control to the Units Comparator.

d. When the Units count reaches its limit, the Units Comparator output drops to its LOW state, providing the system with its LOW output and lighting the Upper Limit light.

e. The output remains LOW as the count remains frozen through the Print Command Display condition.

f. The output (pin 8) returns to ground as the counters are reset at the start of Print Command count state.

G. The Comparators (Units Comparator Illustrated; Q4, Q14)



TYPE 6RIA NO-GO CARDS
UNITS COMPARATOR SWITCH CONNECTIONS

B-6RIA-0109
9-16-'64ms

1. The Comparators are long-tailed emitter coupled amplifiers, with both bases driven.
2. Each Comparator uses on 2N1305 and one 2N1377 transistor.
   a. They are 151-071 and 151-070 respectively.
   b. Both are PNP germanium transistors.
3. All diodes are 152-075 germainum diodes.
4. Inputs to the Comparators are the staircase waveform and the "Digits" voltage taken from a voltage divider.
   a. The Units staircase voltage is fed to pin 13 on the Lower Limit NO-GO Card and pin 10 on the Upper Limit NO-GO Card.
   b. Similarly, the Tens, Hundreds, and Thousands staircase voltages are fed to both the Upper and Lower Limit NO-GO Cards.
   c. Note that the staircase is the top input to the Lower Limit Units Comparator and the bottom input to the Upper Limit Units Comparators.
   d. The Digits input to the Lower Limit Units Comparator (pin 10) is identified as a (-) Digits voltage.
      (1) The (-) refers to the selection of a voltage from the divider a half step (.85v) below the staircase voltage for the corresponding number.
   e. The Digits input to the Upper Limit Units Comparator (pin 13) is a (+) Digits voltage.
      (1) This voltage selection (by the Upper Limit NO-GO switch, Units section) is a half step above the staircase value for the corresponding number.

f. Note that the Lower Limit switch selection for the digit 8, for example, is taken from the bottom of R501 while the Upper Limit switch connects to the top of R401 when 8 is dialed.

5. The .85v difference between a staircase voltage (for a certain number) and the Digit voltage selection, is enough to switch the Comparator output in and out of conduction.

a. If the top input (Q4 base) is higher than the bottom input (Q14 base), Q4 will cut off and Q14 will conduct.

b. When cut off the collector drops to -12.2v.

c. When conducting the collector pulls up to -.3v where it is clamped by D14.

(1) Although the base can swing from 3v to 18.3v (Lower Limit Card) current is held fairly constant by the 39k long tail emitter return to 125v.

H. Emitter Followers; Q73, Q113, Q143

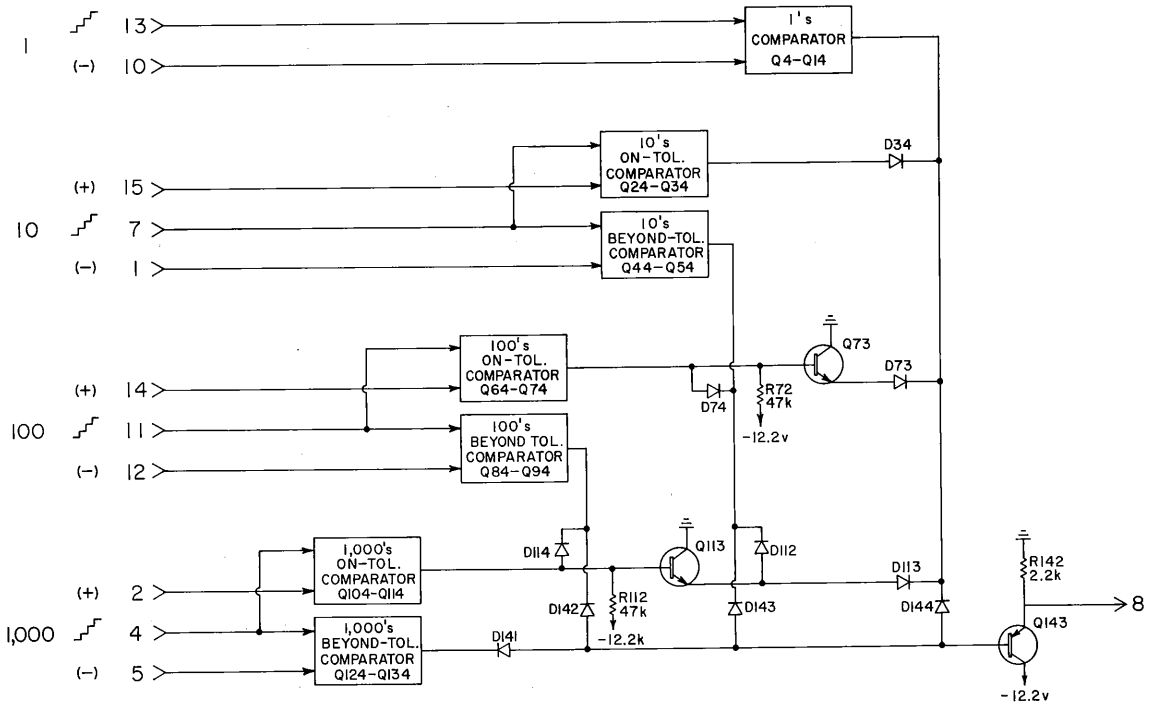
1. The Output Emitter Follwer, Q143 provides a low impedance drive to the Limit Light Driver Card.

a. Q143 is a 151-071; a 2N1305 germanium PNP transistor.

2. The Hundreds EF, Q73, supplies current to turn on D73.

a. When Q74 (Hundreds On-Tolerance Comparator output) conducts, it turns on D73 and D74.

b. Q74 cannot supply enough current to keep both diodes conducting heavily.



TYPE 6RIA NO-GO CARDS
LOWER LIMIT NO-GO EMITTER FOLLOWERS

B-6RIA-0110
9-21-'64 dl

c. Q34, in a similar configuration, has only 1 diode (D34) to pull into conduction so an EF is not required.

d. Q73 is a 151-059; a Rheems RT5830 silicon NPN transistor.

3. The Thousands EF, Q113, supplies current to turn on D113 when Q114 conducts.

a. Q113 is a 151-059, like Q73.

XV. LIMIT LIGHT DRIVER CARD

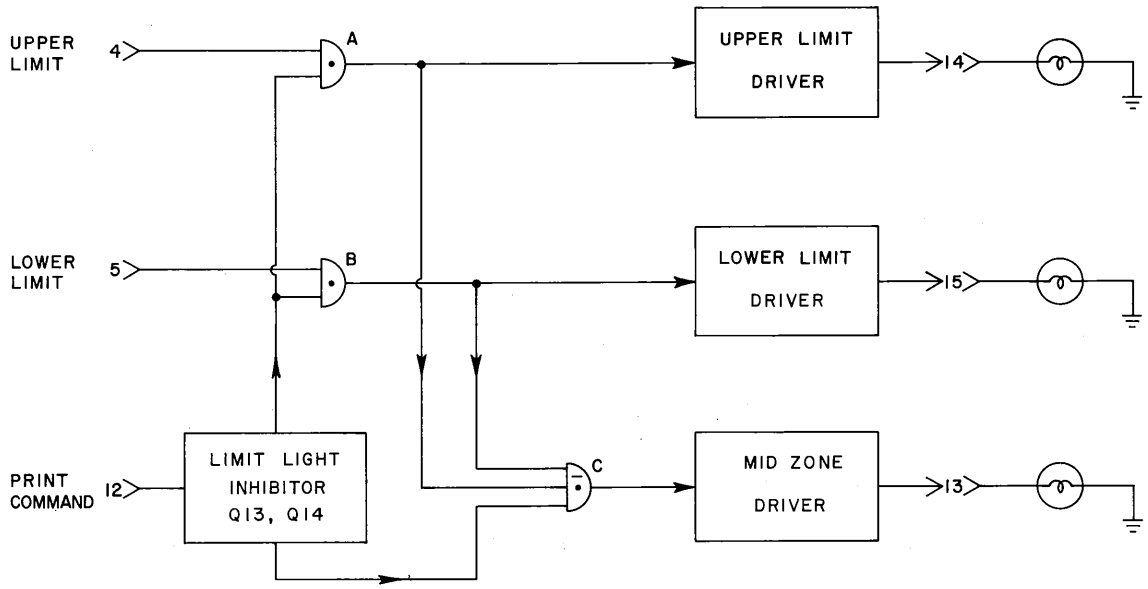
A. The Limit Light Driver turns on the Lower Limit and Upper Limit NO-GO lights and the Mid-Zone light on command from the Upper and Lower Limit NO-GO Cards.

1. One Limit Light Driver Card is used in the 6R1A.

B. Circuits that comprise the Limit Light Driver Card:

1. Limit Light Inhibitor; Q13, Q14.
2. Upper Limit AND Gate, Q23.
3. Lower Limit AND Gate, Q43.
4. Mid Zone NAND Gate, Q64.
5. Upper Limit Light Driver, Q33.
6. Lower Limit Light Driver, Q53.
7. Mid Zone Light Driver, Q63.

c. Block Diagram



TYPE 6RIA LIMIT LIGHT DRIVER BLOCK DIAGRAM

B-6RIA-0111
9-14-'64ms

D. Inputs

1. The Upper Limit NO-GO signal at pin 4.
   a. A 12v negative going signal from the Upper Limit NO-GO Card.
   b. The input sets at ground except when it drops to -12v to indicate a BEYOND TOLERANCE reading.
   c. The -12v, therefore, constitutes an input.
2. The Lower Limit NO-GO signal at pin 5.
   a. Like the Upper Limit Signal, -12v indicates a BEYOND TOLERANCE reading.
3. Print Command from the Master Gate.
   a. The signal is at 2v for Count Condition and 20v for Display State.

E. Outputs

1. The output at pins 13, 14 and 15 drop to about -4v to light the Limit Lights.
   a. The Limit Lights are No. 47, 6.3v, 150 ma pilot lights.

F. Block Logic

1. Two AND Gates and a NAND Gate pass the Limit Light signals on to the Limit Light Drivers.
2. Both AND Gates and the NAND may be inhibited by the Limit Light Inhibitor circuit.
   a. The Inhibitor is a current source for the three Gates.
   b. The Inhibitor is considered ON when it inhibits the operation of the gates by cutting off their current.

c. When Print Command is in its Count Condition, current is cut off from the Gates, resulting in no output from the Limit Light Driver Card.

d. A Limit Light, therefore, cannot light during the Count Condition.

3. If the Upper Limit NO-GO input (pin 4) is LOW (-12v) AND the Limit Light Inhibitor is off, AND Gate A has an output.

4. If the Lower Limit NO-GO input (pin 5) is LOW, AND the Inhibitor is off, AND Gate B has an output.

5. An output is present when the AND Gate output drops to -12v (from ground).

6. When AND Gate A or B has an output (indicating a BEYOND TOLERANCE reading on the Nixies) and the Print Command is in its Display Condition, the associated Limit Light lights.

7. NAND Gate C has inputs from AND Gate A, AND Gate B, and an input from the Limit Light Inhibitor.

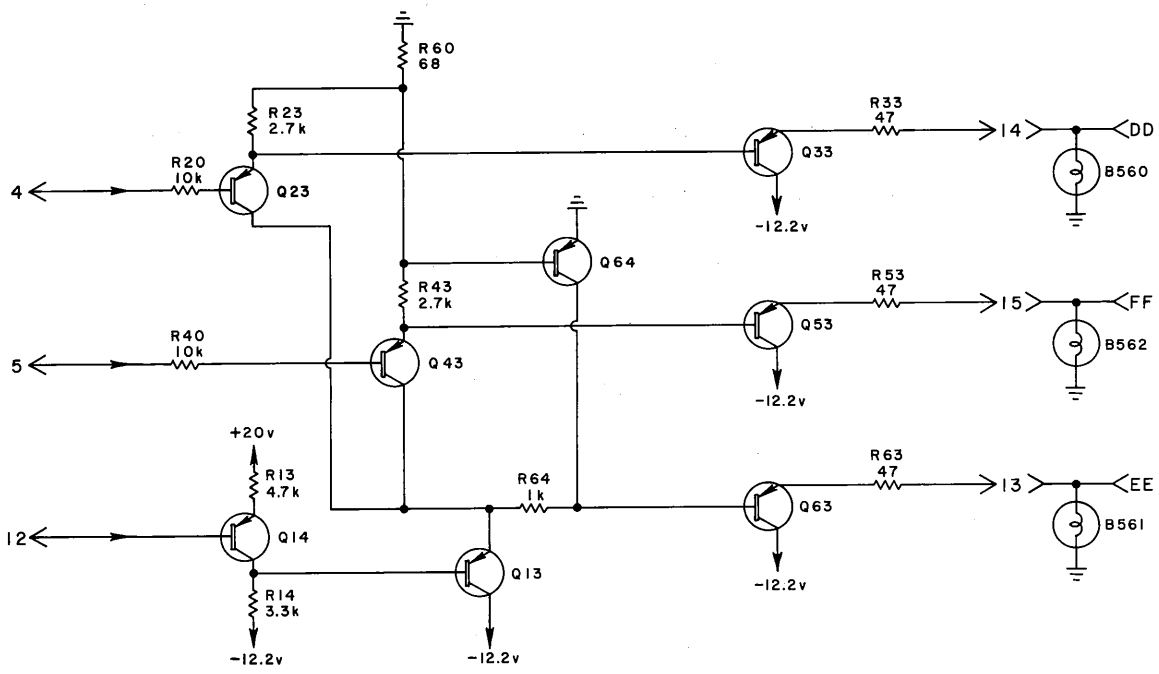
a. When there is <u>no</u> input from AND Gate A, and <u>no</u> input from AND Gate B, and the Inhibitor is not on, NOR Gate has an output.

b. An output from the NOR Gate causes the Mid Zone light to light.

c. The Mid Zone lights, then, when neither the Upper Limit NO-GO light or the Lower Limit NO-GO light is on.

G. Limit Light Inhibitor; Q13, Q14

1. The Limit Light Inhibitor is a current source for the three Gates.



TYPE 6RIA
LIMIT LIGHT DRIVER CARD

B-6RIA-0112
9-14-'64ms

2. The circuit uses two 151-070, 2N1377 germanium, PNP transistors.

3. Q14 is the Inhibitor and Q13 is a switch that opens, removing the current supply from the Gates.

4. The 18v (2v to 20v) Print Command waveform is inverted in Q14 to control current through Q13.
5. Inhibiting takes place during the Print Command count state -- while the nixies are accumulating their count.
   a. Q14 base drops to 2v (from 20v).
   b. The collector pulls up to 2v as the transistor saturates.
   c. Q13 is cut off, removing the current source for Q23, Q43, and Q64.
6. At the end of the Count Condition (the Nixies display their count) the Inhibitor turns on Q13, returning Q23, Q43, Q64 current supply.
   a. Q14 base pulls up to 20v cutting off the transistor.
   b. The collector drops to -12.2v*.
   c. Q13 emitter drops to -12v as the transistor saturates.
   d. Q13 emitter current is the collector supply for Q23, Q43, and Q64.

H. The AND and NOR Gates; Q23, Q43, Q64.

1. The transistors that constitute the Gates are 151-071, 2N1305 germanium PNP transistors.
2. Quiescently Q23, the Upper Limit NO-GO AND Gate (Gate A) is cut off.
   a. The input at pin 4 is at ground.
   b. The emitter returns to ground.
3. Q23 output (the emitter) is at ground.

* Assuming the -12.2v decoupled is actually -12.2v -- it usually sets at -11v.

4. When the Lower Limit NO-GO Signal drops Q23 base to -12v (indicating a Beyond Tolerance nixie reading), the transistor saturates.

   a. The Inhibitor must be off, however, or collector current will not be available.

5. As Q23 conducts, its emitter pulls down to -12v.

   a. The -12v constitutes an output, lighting the Upper Limit NO-GO light.

6. Q43, the Lower Limit NO-GO AND Gate (Gate B) operates in the same manner as Q23 when supplied with a signal from the Lower Limit NO-GO Card.

7. Q64, the NAND Gate (Gate C) has two operating conditions.

   a. During Print Command Count state, the current source is removed from the three gates.

      (1) Q64 base raises to ground, cutting off the transistor.

      (2) Q64 collector drops to about -1v as Q23 and Q43 I_{CBO} draws about 150 μa base current through Q63.

      (3) Whether count is in the Mid-Zone or not, the collector remains at -1v during the count condition.

   b. During Print Command Display Condition, Q64 responds to the output from Q23 and Q43 (the two AND Gates).

      (1) If either AND Gate output is LOW (-12v), Q64 will conduct.

      (2) Q64 base will set at -.3v limited by Q64 base-emitter junction.

(3) The collector will be at ground -- Gate C output is HIGH.

(4) If neither AND Gate output is LOW, Q64 base will pull up to ground.

(5) The transistor will cut off.

(6) Q13 emitter current will pull Q64 collector to -12v (LOW logic level).

(7) The MID-ZONE light will light.

I. Limit Light Drivers

1. The driver transistors supply current to the Limit Lights.

2. Q33, Q53 and Q63 are 151-001, 2N301 PNP germanium power transistors.

3. The Limit Lights are No. 47 6.3v, 150 ma lights.

4. When a Beyond-Tolerance signal is received, dropping Q33 or Q53 base to -11v*, the transistors conduct.

   a. The emitters pull down to about -10v.

   b. The 47Ω resistors (R33, R53) drop the Limit light voltage to about 4v.

      (1) 4v on a 6.3v pilot light lengthens the life of the bulb.

      (2) The 47Ω resistors protect the transistors from damage from a possible external load.

* -12v decoupled usually sets at about -11v.

5. When the nixie reading is on tolerance, Q63 base drops to -11v, lighting the MID-ZONE light.
6. The bulbs must be removed before an external programming load can be placed on the Limit Light outputs.

SECTION 16

EXTERNAL PROGRAMMING FOR THE 6R1A

INTRODUCTION:

The 6R1A can be programmed externally, as well as by operating its front panel controls. External programming is useful when a series of measurements is to be repeated. The circuits of the 6R1A can be controlled by externally connecting circuit blocks to duplicate the operations performed by the front panel controls. These connections may be made by automatic or semiautomatic external devices. Tektronix manufactures the Type 262 as a general-purpose external programming device. The 262 simplifies the actual connections necessary for each program that is desired, and provides circuits to switch through a sequence of programs automatically. It also provides external go-no go checking. While other devices may be used to externally program the 6R1A, the same functions must be provided as are provided by the 262. The programmer is a passive device; that is, it only operates switch connections or inserts resistance in the circuit. Therefore, there is no need for stable power supplies. However, no power is provided by the 6R1A for operating the programmer.

In the basic 567-6R1A system, only the 6R1A is externally programmable. The vertical and horizontal plug-ins must be manually set. The vertical units are provided with two channels, and output from either channel may be selected for measurement by the 6R1A programmer. The horizontal display (time base) is fixed in one setting, and it is convenient to lay out the testing program to allow all tests to be made with one sweep time/cm with a fixed delay in relation to the trigger signal.

Before studying the programming of the 6R1A, a thorough knowledge of how the 6R1A operates, as a system is advisable. This knowledge will aid in selecting the best programming technique.

PROGRAM CONNECTIONS

Connector J34, at the back of the 6R1A plug-in, has all the connections used to control the operation of the 6R1A externally. The following functions are provided for:

OPERATION	METHOD OF PROGRAMMING
1. Selection of voltage or time clock.	Return required terminat to ground.
2. Selection from one of the following as DC level to be fed to the start comparator.	
a. 0 or 100 percent memory. (Voltage measurement)	a. Connect memory output to comparator input.
b. Voltage level offset from 0% or 100% zone. (Time measurement)	b. Requires fixed voltage floating above or below zone voltage selected.
c. Percent division of voltage between 0% and 100% memories. (Time measurement)	c. Connection of voltage from resistive divider between 0% and 100% zones.
d. Voltage level from start of sweep. (Time measurement)	d. Connection of DC level corresponding to sweep voltage at desired point.
3. Selection for stop comparator DC level, from the above list. DC level does not need to be selected from same source for both comparators. Note that there are two inputs (+ and -) to each comparator. The moving level must be connected to the input with the same sign as the direction in which the signal is moving. The DC level is connected to the remaining terminal.	
4. Moving signal selection for comparators, from one of the following:	
a. Vertical signal from either A or B. (Time measurements)	a. Connection between correct signal comparator input and desired channel signal.
b. Horizontal signal (used with fixed signal d., above). (Time measurements)	b. Connection from sweep input to + input of comparator.

c. Voltmeter ramp. (Voltage measurements).	c. Connect voltmeter ramp to + inputs of comparators.
5. Selection of first or second crossing to operate start comparator.	Ground required terminal.
6. First or second crossing selection for stop comparator.	Ground required terminal.
7. Selection of divide-by scaling from input channel used for measurement.	Ground correct terminal.
8. Selection of decimal from channel used for measurement.	Ground correct terminal.
9. Display Hold: Holds in display mode and allows print command to reset.	Ground to hold display connect to +20 from 6R1A to allow display reset.
10. Zone positioning.	Connection of desired resistance across zone override terminals.

NOTE: The 262 program cards are not provided with override connections. Zone override must be selected on separate external program cards. The other functions mentioned here are provided for in the 262.

SIGNAL OUTPUTS FROM 6R1A

In addition to the connections provided for controlling the 6R1A, listed in table 1, there are outputs from the counters and other circuits that may be used for operating go-no-go detection circuits, and may be used to print out or be stored in a memory. The Type 262 has no built-up circuitry for use of the signal readout except for a go-no-go circuit. Outputs are connected to J33. The use of these outputs is dependent on the system design. These are the outputs provided:

1. Counter outputs: Each digit on each of the four counters is provided with an external connection on J33. The digits being displayed ground the connection, while the other digits are open circuit (collector circuits of back-biased transistors).
2. Decimal: An output is provided for each decimal. The decimal selected is grounded at its output; the other open.
3. Units: Outputs are provided for both the units and the multipliers. The units being measured are grounded; the others open.
4. Zones: Outputs are provided for the below, mid-zone, and above outputs, referring to the setting of the front panel switches on the 6R1A. This display is not controlled by external programming. The lamp displaying provides -12.2 volts at the connector. The other lamp outputs are grounded.
5. Print Command: Gate signal is at ground when system is measuring, rises to +20 when system is holding count for display. Alternate connection gives +20 when system is measuring; ground when displaying. Connection must be made on master gate card.

Also, provided are staircase voltages at J34. Each decade counter has a staircase output that rises 1.67 volts per step from zero, at ground potential. These outputs may be used as an analog readout of the counter load.

6R1A SLIDE LIST

0% Zone Card

B-6R1A- 0001
0002
0003
0019
0004
0017
0018
0005

0% and 100% Memories Card

B-6R1A- 0006
0007
0008.1
0008
0009
0010
0011
0013*
0012
0013
0014
0015
0016

Comparator Card

B-6R1A- 0036
0037
0043
0044
0045
0038
0039
0046
0040
0047
0041
0048
0049
0050
0051
0042
0052
0053
0054

Voltmeter Card

B-6R1A- 0020
0021
0022
0030
0023
0031
0029
0024
0025
0032
0033
0027
0034
0026
0035
0028

Master Gate

B-6R1A- 0055
0056
0057
0058
0059
0060
0061
0062*
0063
0064
0065
0066
0067
0068
0069
0062
0070
0071
0072
0073
0125
0075
0076
0077
0078
0079*
0080
0079
0081

6R1A Slide List

÷10 Card

B-6R1A- 0073
0094
0095
0098
0097
0096

÷1, 2, 5 Card

B-6R1A- 0082
0083
0084
0085
0086
0087
0088
0089
0090
0091
0092
0093

Counter Cards

B-6R1A- 0099
0100
0103
0101
0097
0102
0104
0121
0124
0122
0123

Analog Display Card

B-6R1A- 0113
0114
0115
0116
0117
0118
0119
0120

Upper and Lower Limit No-Go Cards

B-6R1A- 0105
0106
0107
0108
0109
0110

Limit Light Driver Card

B-6R1A- 0111
0112

Manual Schematic Slides

C-6R1A- 0005
0010
0015
0020
0025
0030
0035
0040
0045
0050
0055
0060
0065
0070
0075
0080
0085
0090
0095
0100
0105
0110

6R1A RECOMMENDED HANDOUTS

0% Card

B-6R1A- 0001	Block Diagram
0017	Waveforms
0018	Waveforms
0019	Waveforms

Memories Card

B-6R1A- 0006	Block Diagram

Voltmeter Card

B-6R1A- 0020	Block Diagram
0030	Waveforms
0031	Waveforms
0032	Waveforms
0033	Waveforms

Signal Comparator Card

B-6R1A- 0036	Block Diagram
0037	Signal Source, Time
0038	Signal Source, Volts
0047	Waveforms
0050	Waveforms
0052	Waveforms

Master Gate

B-6R1A- 0056	Block Diagram
0058	Waveforms
0059	AND Circuit
0060	Waveforms
0063	Waveforms
0065	Waveforms
0067	Waveforms
0068	Waveforms
0069	Waveforms
0071	Waveforms
0072	Waveforms
0073	Waveforms
0125	Waveforms
0076	Waveforms
0076	Waveforms
0078	Waveforms
0080	Waveforms
0081	Waveforms

÷ 1, 2, 5 Card

B-6R1A- 0082	Block Diagram
0084	Waveforms
0085	Grounding Circuits
0088	Waveforms
0089	Binary Block
0090	Binary Relationships
0091	Binary States
0098	Binary Relationships

÷ 10 Card

B-6R1A- 0094	Binary Block
0097.1	Binary States Work Sheet

Counter Card

B-6R1A- 0099	Block Diagram
0103	Staircase
0104	Binary Output
0123	Ground Path Decima Point Nixies
0122	Ground Path Units o Measure Nixies

Limit Light Driver

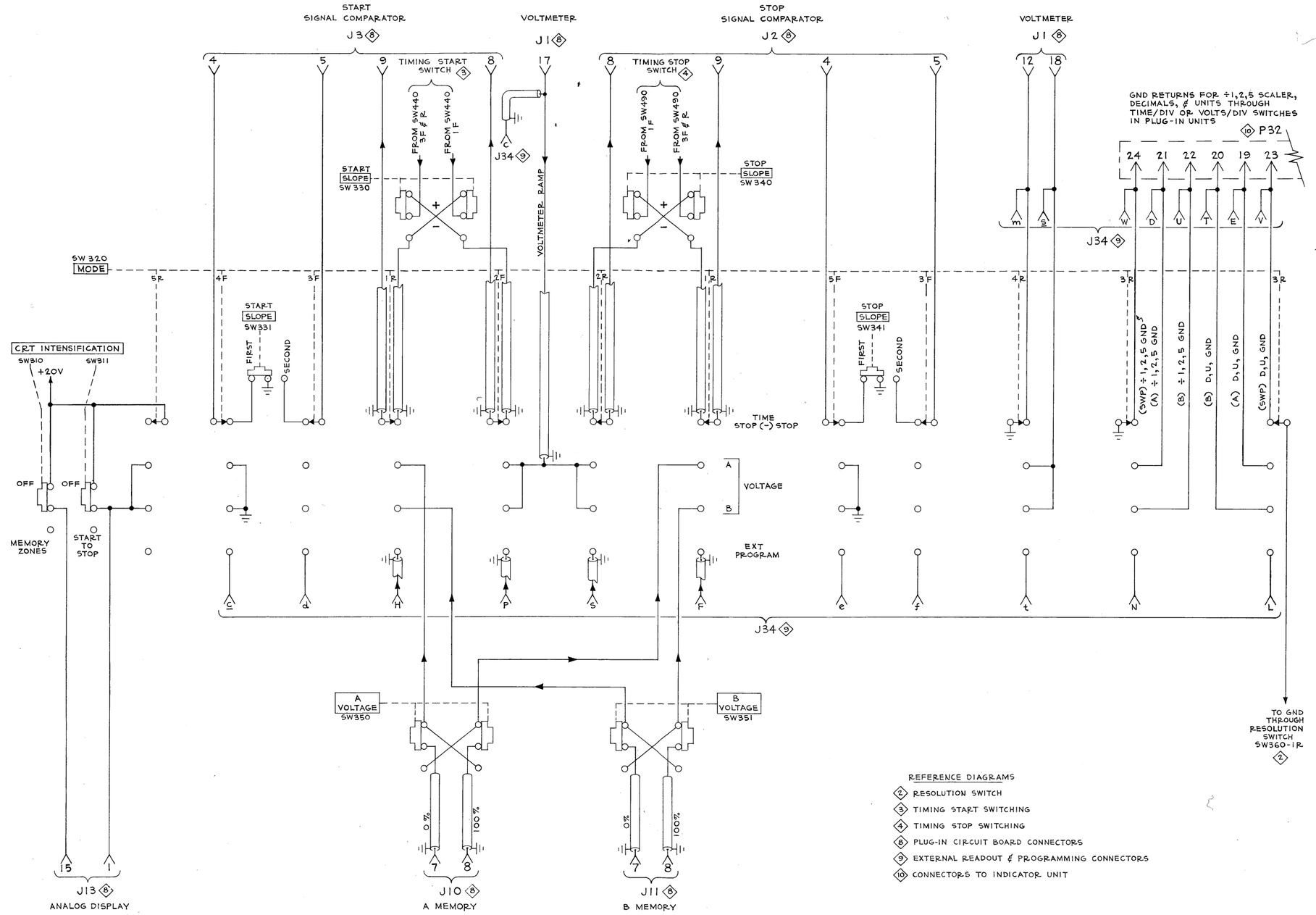
B-6R1A- 0111	Block Diagram

Upper and Lower Limit No-Go Cards

B-6R1A- 0105	Lower Limit Block
0106	Comparison Voltage
0109	Units Comparator Switch Connectors
0107	Lower Limit No-Go Logic
0108	Upper Limit Block

Analog Display

B-6R1A- 0113	Block Diagram
0114	Logic Diagram
0116	Waveforms
0118	Waveforms



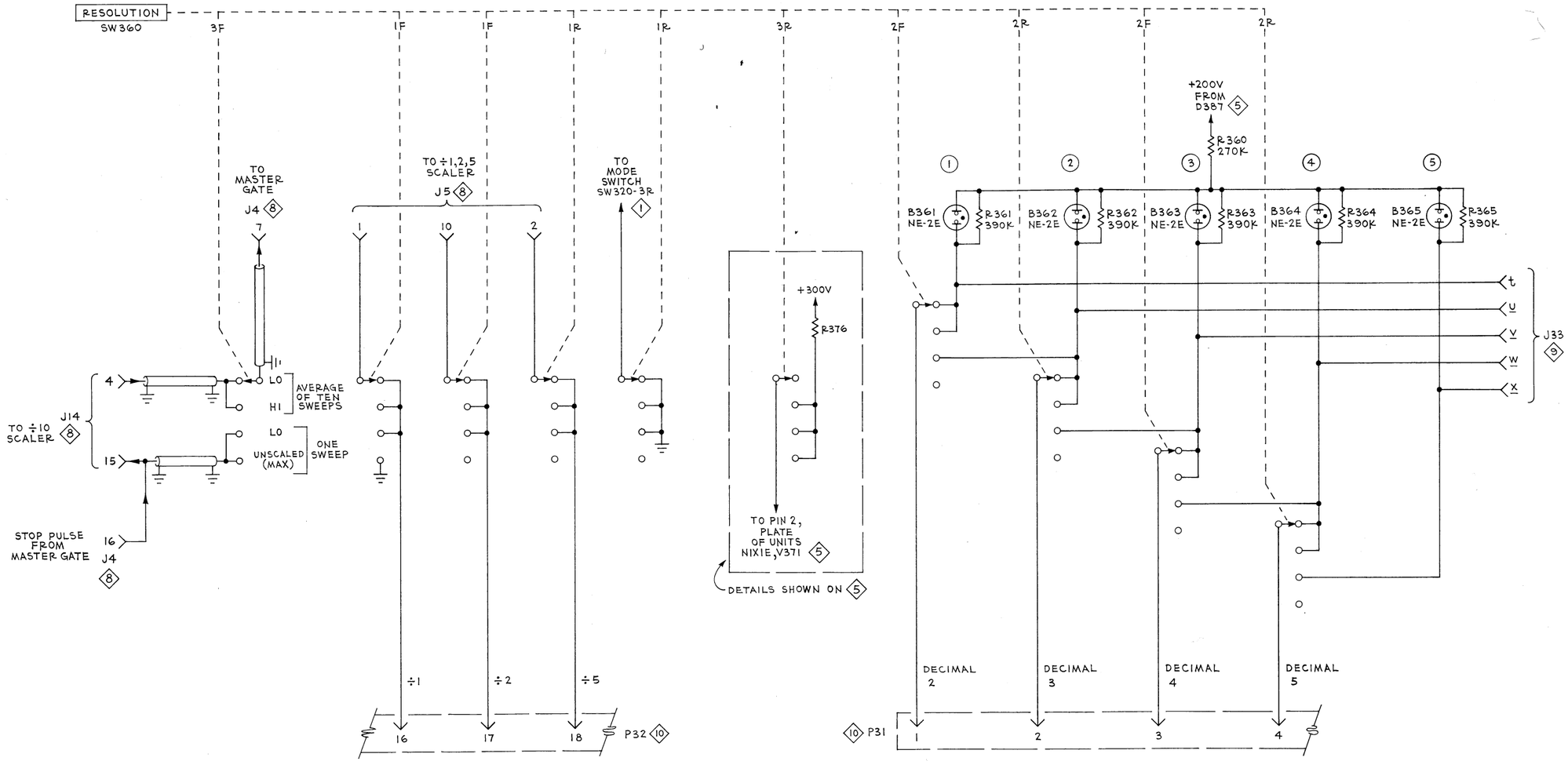
REFERENCE DIAGRAMS

- 2 RESOLUTION SWITCH
- 3 TIMING START SWITCHING
- 4 TIMING STOP SWITCHING
- 8 PLUG-IN CIRCUIT BOARD CONNECTORS
- 9 EXTERNAL READOUT & PROGRAMMING CONNECTORS
- 10 CONNECTORS TO INDICATOR UNIT

TYPE 6R1A

MODE SWITCH 1

364



REFERENCE DIAGRAMS

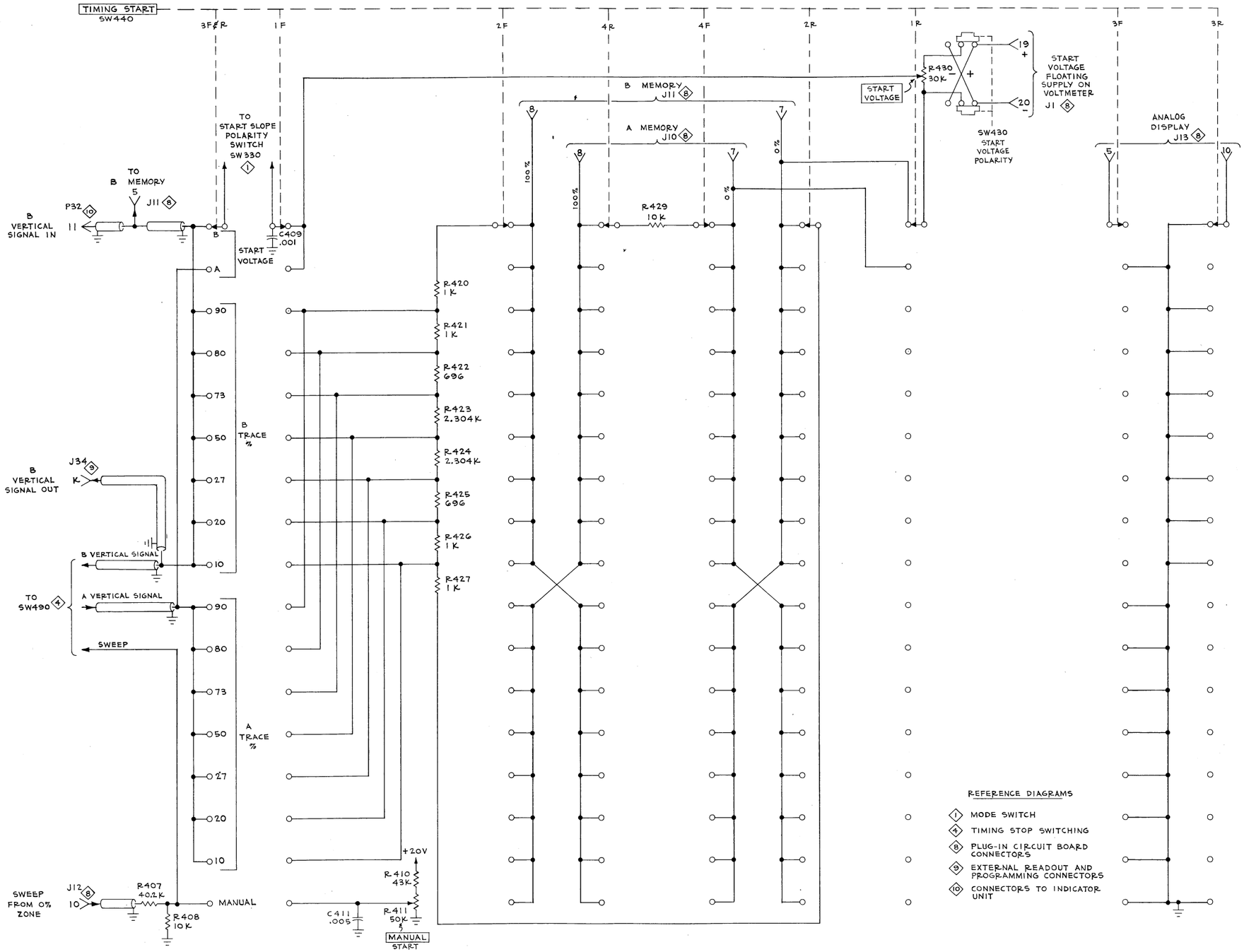
- 1 MODE SWITCH
- 5 READOUT TUBES
- 8 PLUG-IN CIRCUIT BOARD CONNECTORS
- 9 EXTERNAL READOUT & PROGRAMMING CONNECTORS
- 10 CONNECTORS TO INDICATOR UNIT

TYPE 6R1A

A

RESOLUTION SWITCH 2

GAB 364

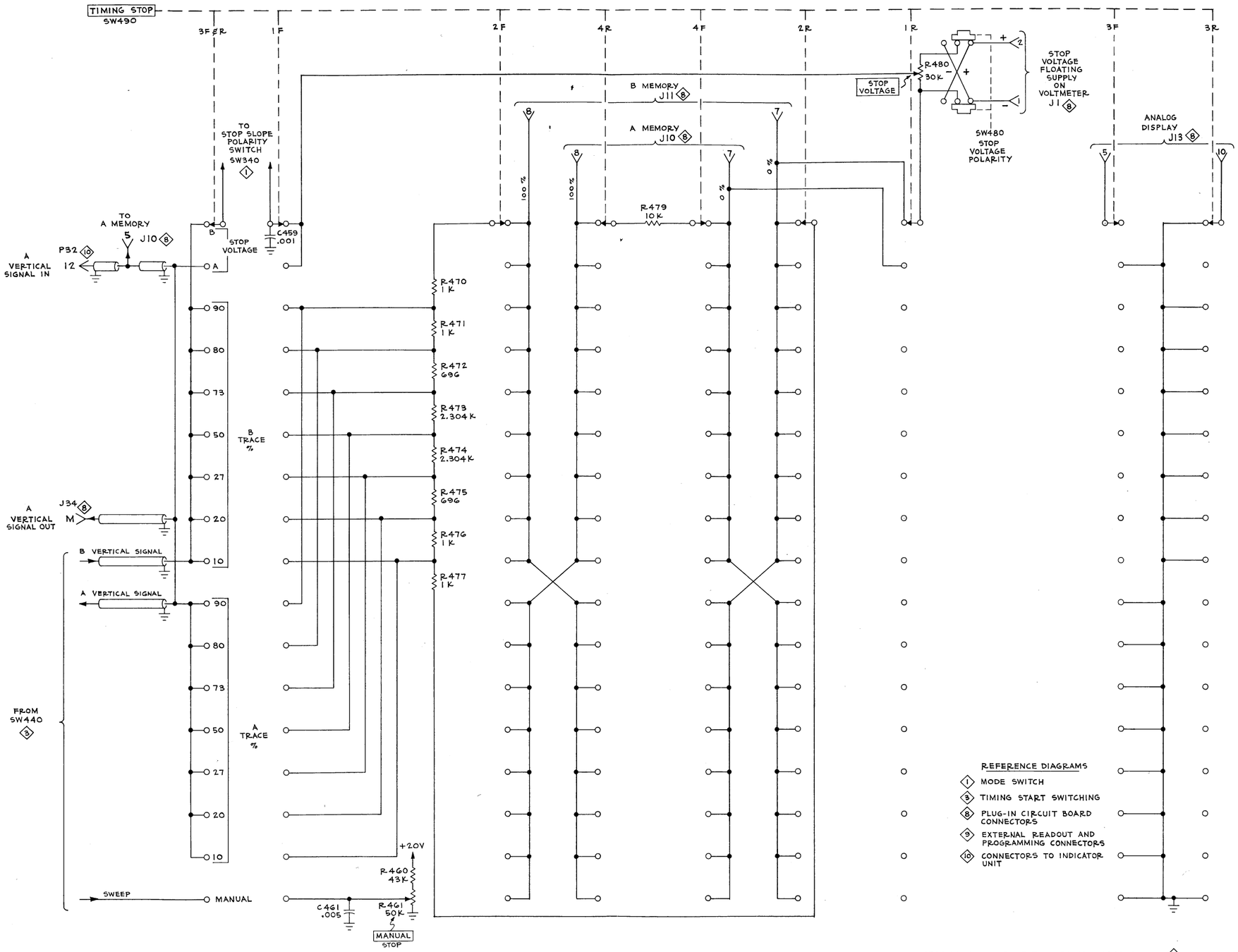


TYPE GR1A

A

TIMING START SWITCHING 3

3G4



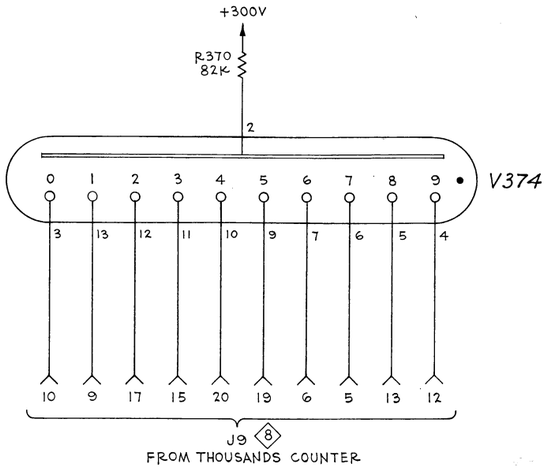
TYPE 6R1A

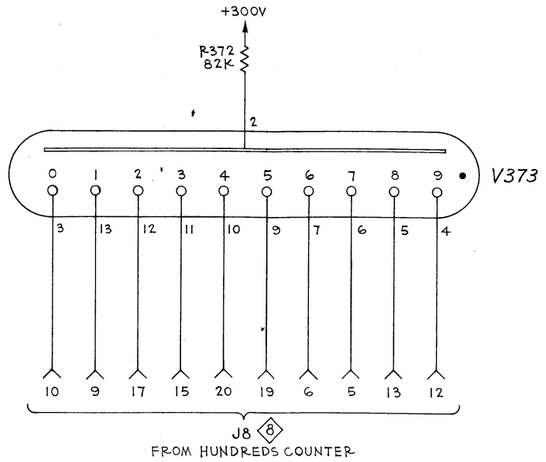
REFERENCE DIAGRAMS

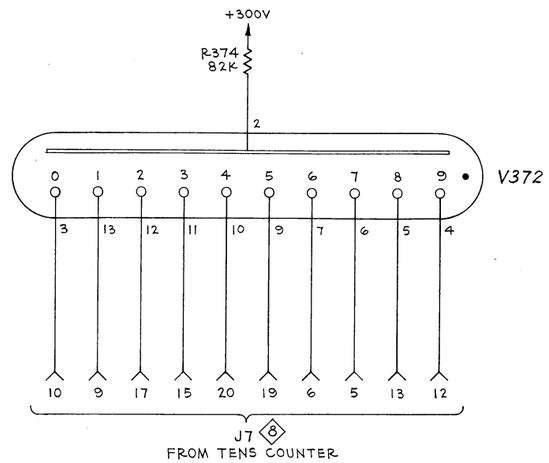
- 1 MODE SWITCH
- 3 TIMING START SWITCHING
- 8 PLUG-IN CIRCUIT BOARD CONNECTORS
- 9 EXTERNAL READOUT AND PROGRAMMING CONNECTORS
- 10 CONNECTORS TO INDICATOR UNIT

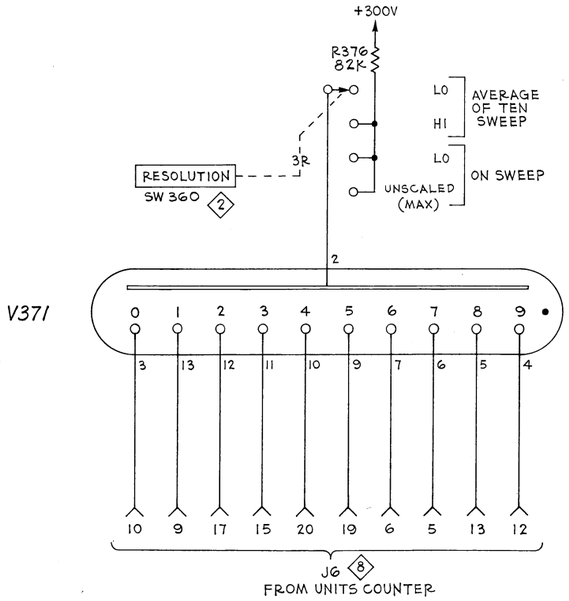
TIMING STOP SWITCHING 4

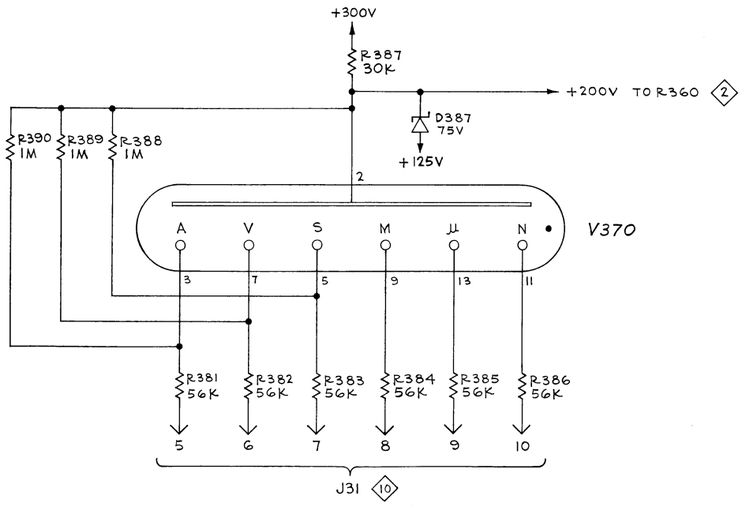
3G4





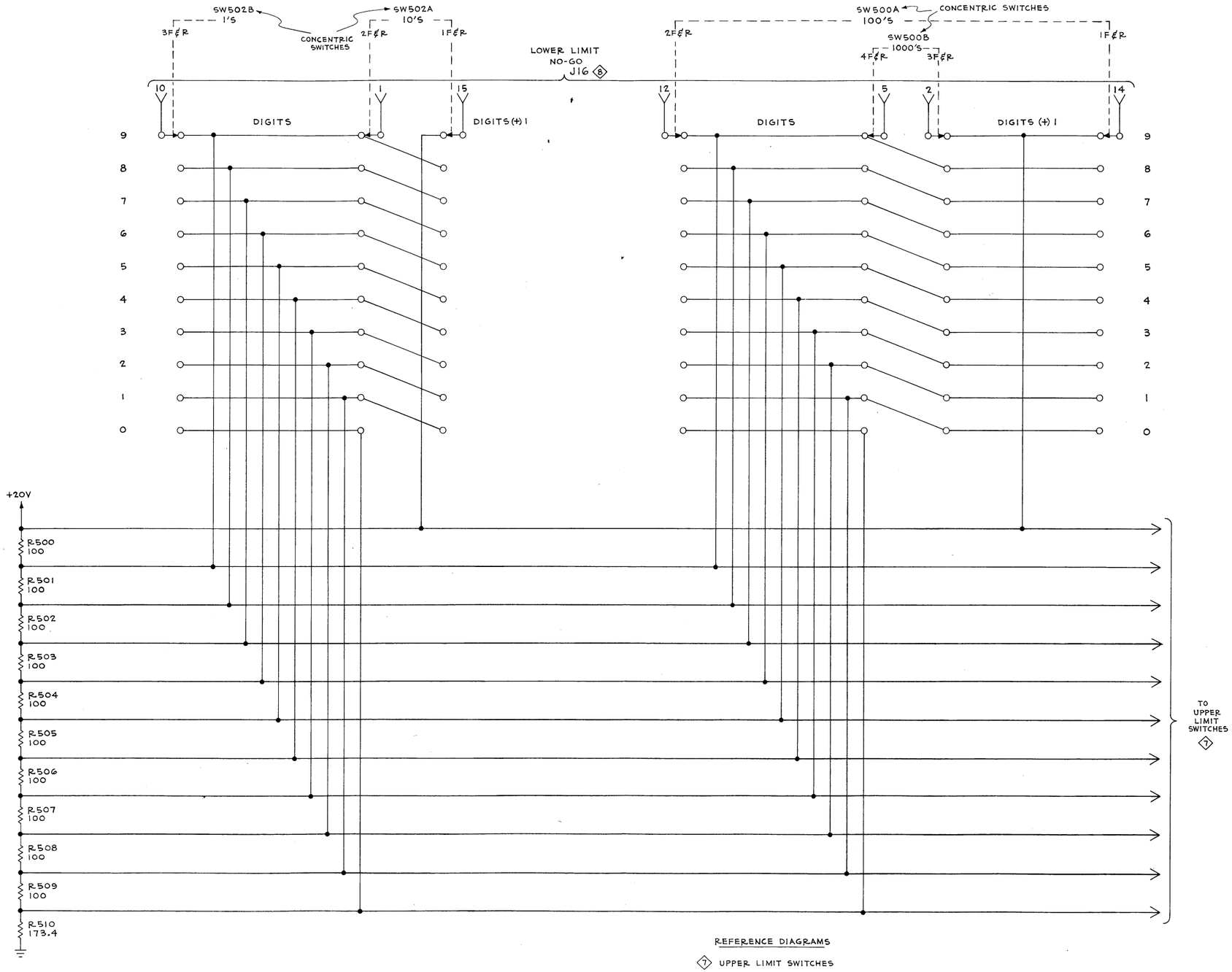






REFERENCE DIAGRAMS

2 RESOLUTION SWITCH
8 PLUG-IN CIRCUIT BOARD CONNECTORS
10 CONNECTORS TO INDICATOR UNIT



REFERENCE DIAGRAMS

7 UPPER LIMIT SWITCHES

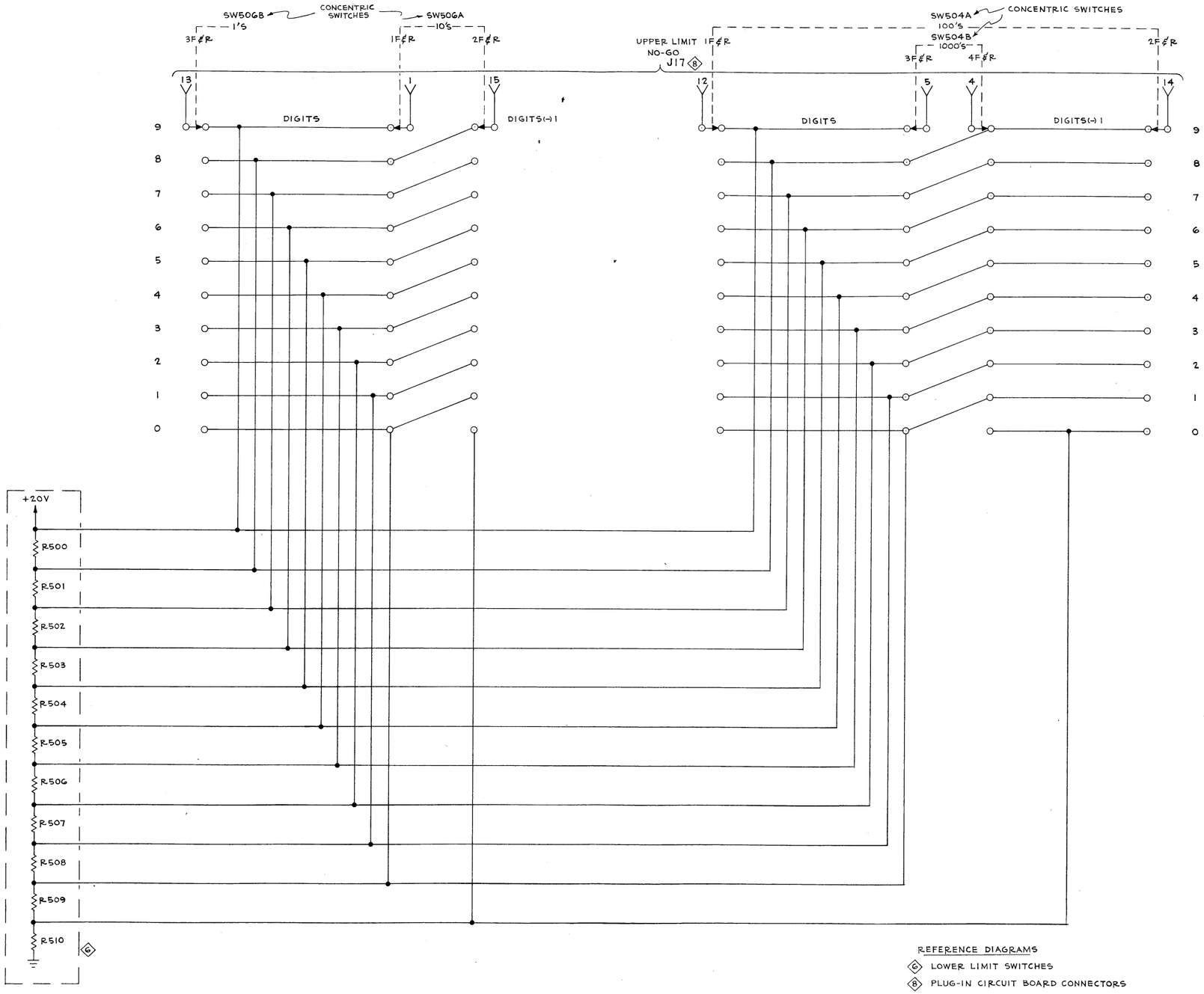
8 PLUG-IN CIRCUIT BOARD CONNECTORS

TYPE 6R1A

A

LOWER LIMIT SWITCHES 6

364



REFERENCE DIAGRAMS

6 LOWER LIMIT SWITCHES

8 PLUG-IN CIRCUIT BOARD CONNECTORS

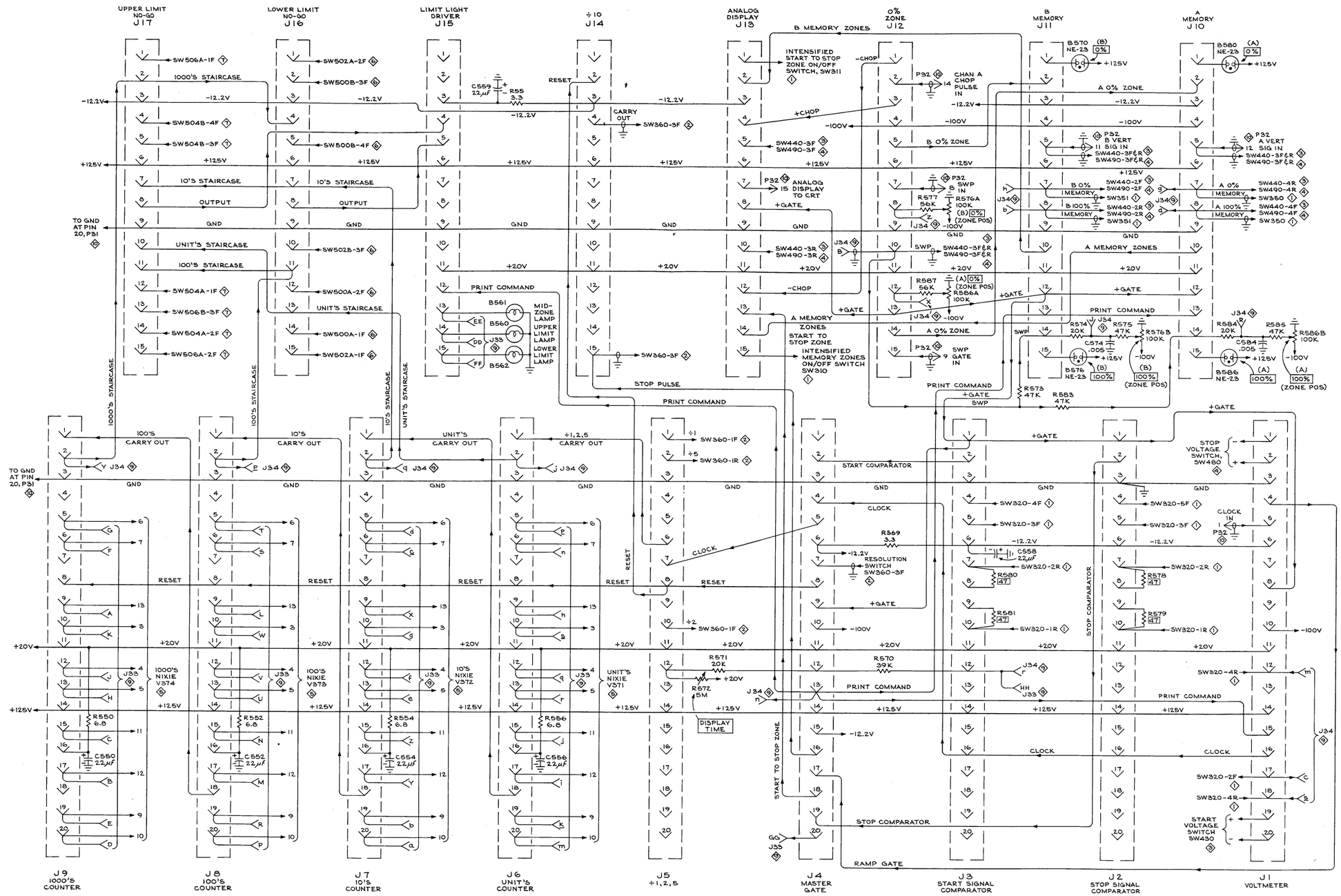
TYPE GRIA

A

UPPER LIMIT SWITCHES 7

3G4

UPPER LIMIT SWITCHES



REFERENCE DRAWINGS

1. MODE SWITCH
2. RESOLUTION SWITCH
3. TIMING START SWITCHING
4. TIMING STOP SWITCHING
5. READOUT TUBES
6. LOWER LIMIT SWITCHES
7. UPPER LIMIT SWITCHES
9. EXTERNAL READOUT & PROGRAMMING CONNECTORS
10. CONNECTORS TO INDICATOR UNIT

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.

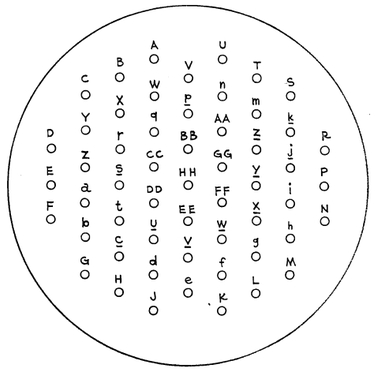
TYPE 6RIA

B1

PLUG-IN CIRCUIT CARD CONNECTORS 8 DON 964

PLUG IN CIRCUIT CARD CONNECTORS

EXTERNAL READOUT J33

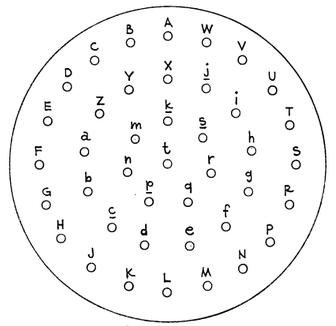


A	1000S'-1	J9-9 ◇8	f	10S'-9	J7-12 ◇8
B	1000S'-2	J9-17 ◇8	g	10S'-0	J7-10 ◇8
C	1000S'-3	J9-15 ◇8	h	1S'-1	J6-9 ◇8
D	1000S'-4	J9-20 ◇8	i	1S'-2	J6-17 ◇8
E	1000S'-5	J9-19 ◇8	j	1S'-3	J6-15 ◇8
F	1000S'-6	J9-6 ◇8	k	1S'-4	J6-20 ◇8
G	1000S'-7	J9-5 ◇8	m	1S'-5	J6-19 ◇8
H	1000S'-8	J9-13 ◇8	n	1S'-6	J6-6 ◇8
J	1000S'-9	J9-12 ◇8	p	1S'-7	J6-5 ◇8
K	1000S'-0	J9-10 ◇8	q	1S'-8	J6-13 ◇8
L	100S'-1	J8-9 ◇8	r	1S'-9	J6-12 ◇8
M	100S'-2	J8-17 ◇8	s	1S'-0	J6-10 ◇8
N	100S'-3	J8-15 ◇8	t	DECIMAL 1 FROM SW360-2F	◇2
P	100S'-4	J8-20 ◇8	u	DECIMAL 2 FROM SW360-2F&R	◇2
R	100S'-5	J8-19 ◇8	v	DECIMAL 3 FROM SW360-2F&R	◇2
S	100S'-6	J8-6 ◇8	w	DECIMAL 4 FROM SW360-2F&R	◇2
T	100S'-7	J8-5 ◇8	x	DECIMAL 5 FROM SW360-2R	◇2
U	100S'-8	J8-13 ◇8	y	m FROM P31-8	◇10
V	100S'-9	J8-12 ◇8	z	n FROM P31-10	◇10
W	100S'-0	J8-10 ◇8	AA	μ FROM P31-9	◇10
X	10S'-1	J7-9 ◇8	BB	V FROM P31-6	◇10
Y	10S'-2	J7-17 ◇8	CC	S FROM P31-7	◇10
Z	10S'-3	J7-15 ◇8	DD	NO-GO UPPER LIMIT FROM J17-14	◇8
a	10S'-4	J7-20 ◇8	EE	NO-GO MID-ZONE FROM J17-13	◇8
b	10S'-5	J7-19 ◇8	FF	NO-GO LOWER LIMIT FROM J17-15	◇8
c	10S'-6	J7-6 ◇8	GG	PRINT COMMAND FROM J4-20	◇8
d	10S'-7	J7-5 ◇8	HH	DISPLAY HOLD FROM J3-12	◇8
e	10S'-8	J7-13 ◇8			

TYPE 6RIA

A

EXTERNAL PROGRAMMING J34



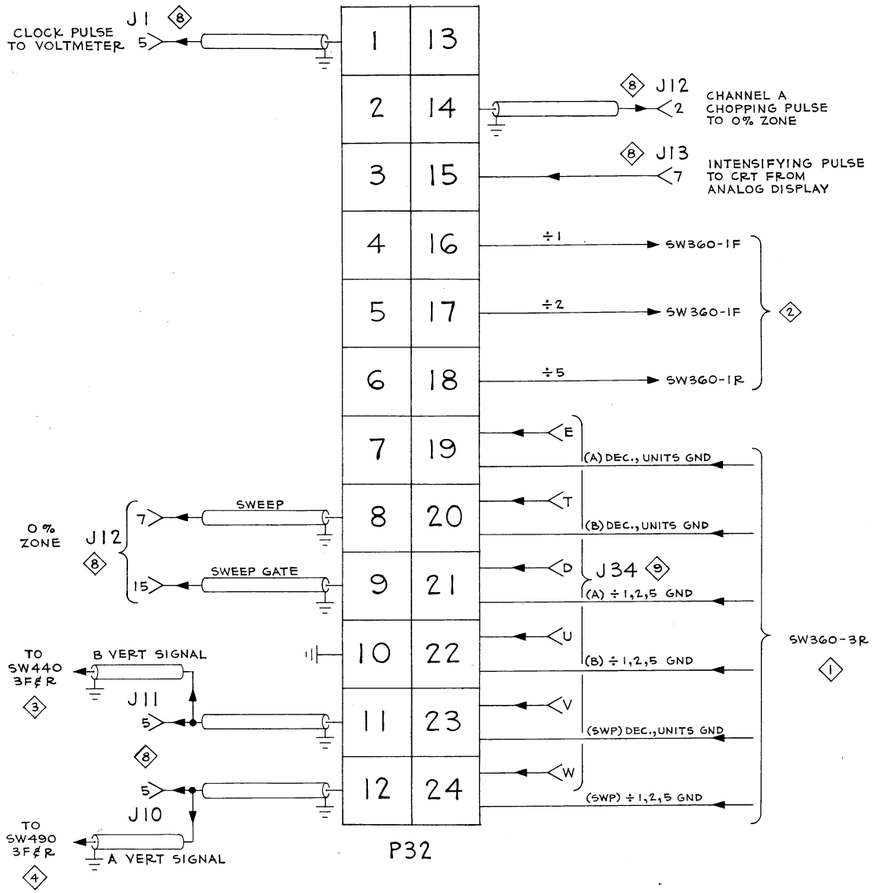
A	GROUND		a	100% A MEMORY FROM J10-8	◇8
B	SWEEP OUT FROM J12-10	◇8	b	100% B MEMORY FROM J11-8	◇8
C	VOLTMETER RAMP FROM J1-17	◇8	c	1ST START SLOPE TO SW320-4F	◇1
D	A VERT ÷1,2,5 GND TO P32-21	◇10	d	2ND START SLOPE TO SW320-3F	◇1
E	A VERT DEC, UNITS GND TO P32-19	◇10	e	1ST STOP SLOPE TO SW320-5F	◇1
F	-STOP COMPARATOR TO SW320-1R	◇1	f	2ND STOP SLOPE TO SW320-3F	◇1
G	+20V		g	0% A MEMORY FROM J10-7	◇8
H	-START COMPARATOR TO SW320-1R	◇1	h	0% B MEMORY FROM J11-7	◇8
J	B 100% OVERRIDE TO J11-14 THRU R574	◇8	i	SPARE	
K	B SIGNAL FROM START, SW440-3F&R	◇3	j	1S' STAIRCASE FROM J6-2	◇8
L	DEC, UNITS RETURN FROM SW320-3R	◇1	k	-12.2V	
M	A SIGNAL FROM STOP, SW490-3F&R	◇4	m	TIME CLOCK TO J1-12	◇8
N	÷1,2,5 RETURN FROM SW320-3R	◇1	n	PRINT COMMAND, FROM J4-13	◇8
P	+START COMPARATOR TO SW320-2F	◇1	p	100S' STAIRCASE FROM J8-2	◇8
R	A 100% OVERRIDE TO J10-14 THRU R584	◇8	q	10S' STAIRCASE FROM J7-2	◇8
S	+STOP COMPARATOR TO SW320-2R	◇1	r	DISPLAY HOLD TO J3-12	◇8
T	B VERT DEC, UNITS GND TO P32-20	◇10	s	VOLTMETER OSC TO J1-18	◇8
U	B VERT ÷1,2,5 GND TO P32-22	◇10	t	VOLTMETER OSC, TIME CLOCK RETURN FROM SW320-4R	◇1
V	HORIZ DEC, UNITS GND TO P32-23	◇10			
W	HORIZ ÷1,2,5 GND TO P32-24	◇10			
X	A 0% OVERRIDE FROM J12-12	◇8			
Y	1000S' STAIRCASE FROM J9-2	◇8			
Z	B 0% OVERRIDE FROM J12-8	◇8			

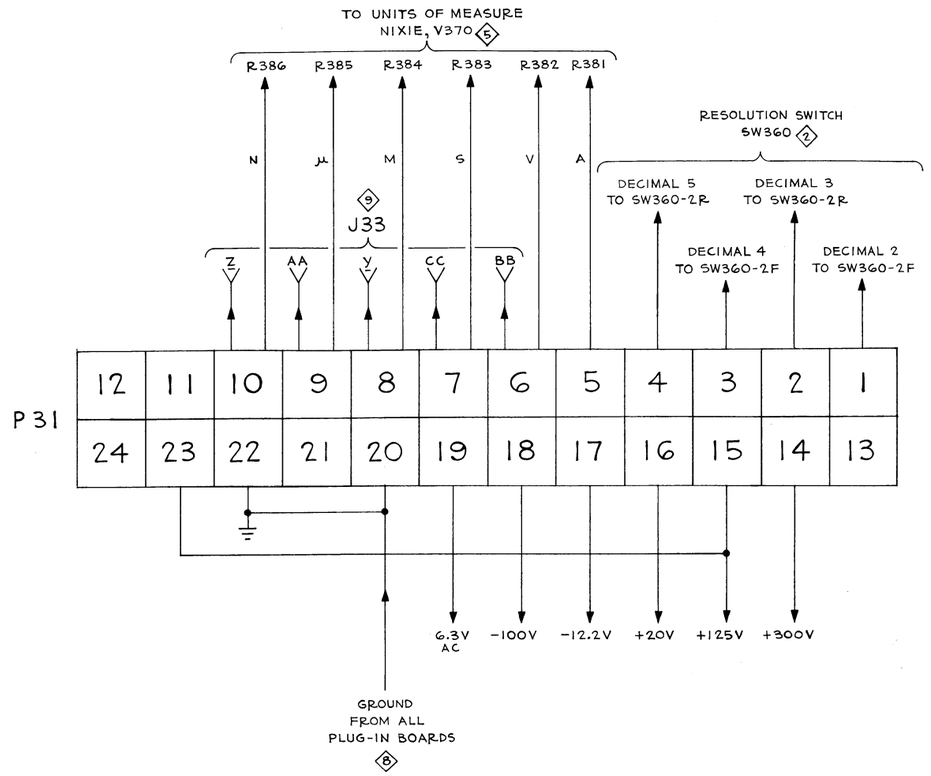
REFERENCE DIAGRAMS

- ◇1 MODE SWITCH
- ◇2 RESOLUTION SWITCH
- ◇3 TIMING START SWITCHING
- ◇4 TIMING STOP SWITCHING
- ◇8 PLUG-IN CIRCUIT BOARD CONNECTORS
- ◇10 CONNECTOR TO INDICATOR UNIT

GAB 364

EXTERNAL READOUT & PROGRAMMING CONNECTORS ◇9





REFERENCE DIAGRAMS

- ① MODE SWITCH
- ② RESOLUTION SWITCH
- ③ TIMING START SWITCHING
- ④ TIMING STOP SWITCHING
- ⑤ READOUT TUBES
- ⑧ PLUG-IN CIRCUIT BOARD CONNECTORS
- ⑨ EXTERNAL READOUT & PROGRAMMING CONNECTORS

TYPE 6R1A

CONNECTORS TO INDICATOR UNIT ⑩

364

A

IMPORTANT

The waveform photographs shown on certain of the 6R1A schematics were taken from the crt face of a Tektronix Type 545A/CA oscilloscope system. The equipment was initially set up as listed below. After the initial setup was made, the controls were changed as necessary to obtain the individual photographs.

545A

TIME/CM	2 mSEC/CM
MAGNIFIER	OFF
Triggering controls	To obtain stable display

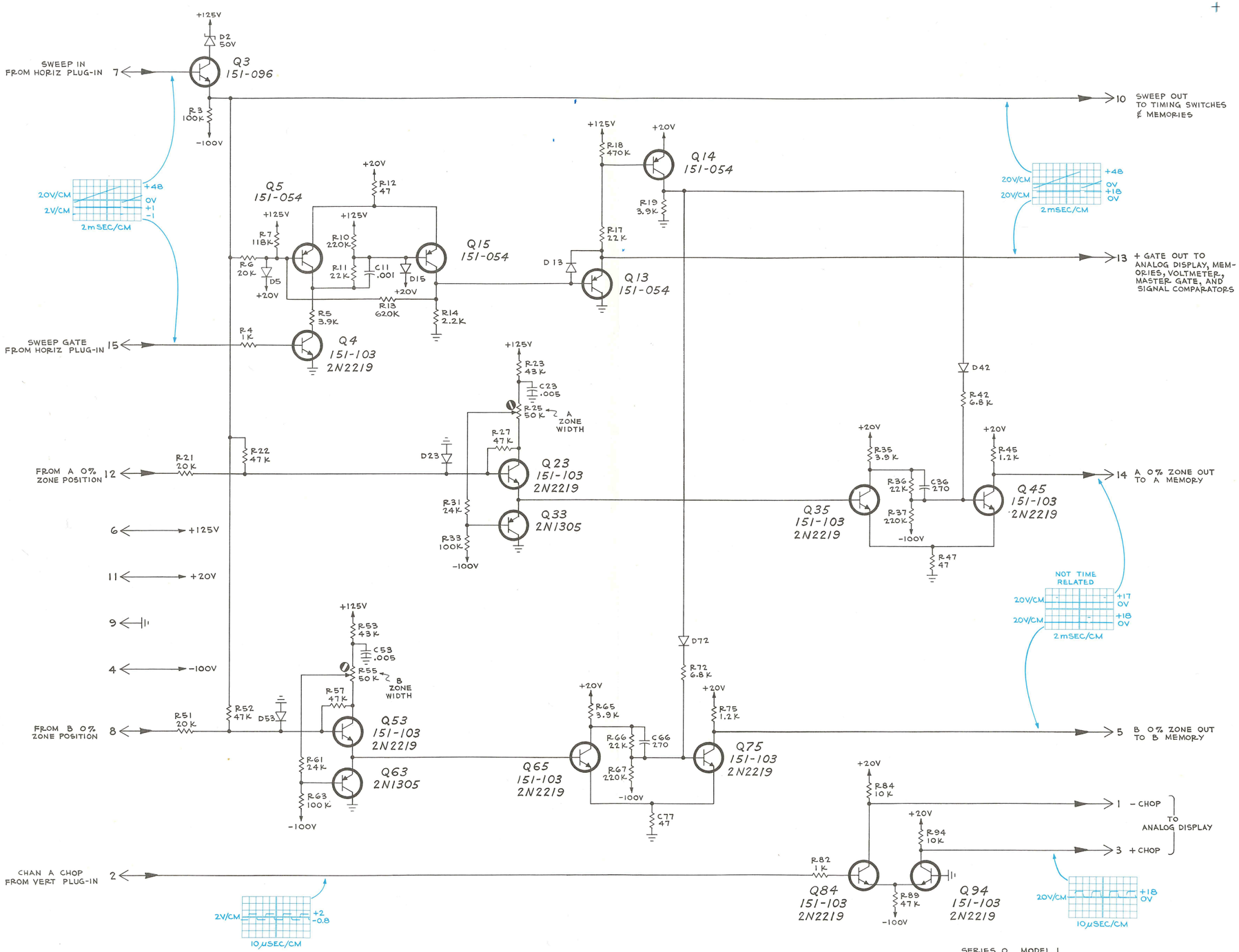
CA Unit

VOLTS/CM	1
Probe	10X
POLARITY	NORMAL
Coupling	DC

CHOPPED mode was used when photographing two time related signals.

3S76

MV/DIV	100
Mode	A ONLY
Polarity	NORM.
INTERNAL TRIGGER	A
Signal input	2 cm of 1 mc squarewave



TYPE GR1A

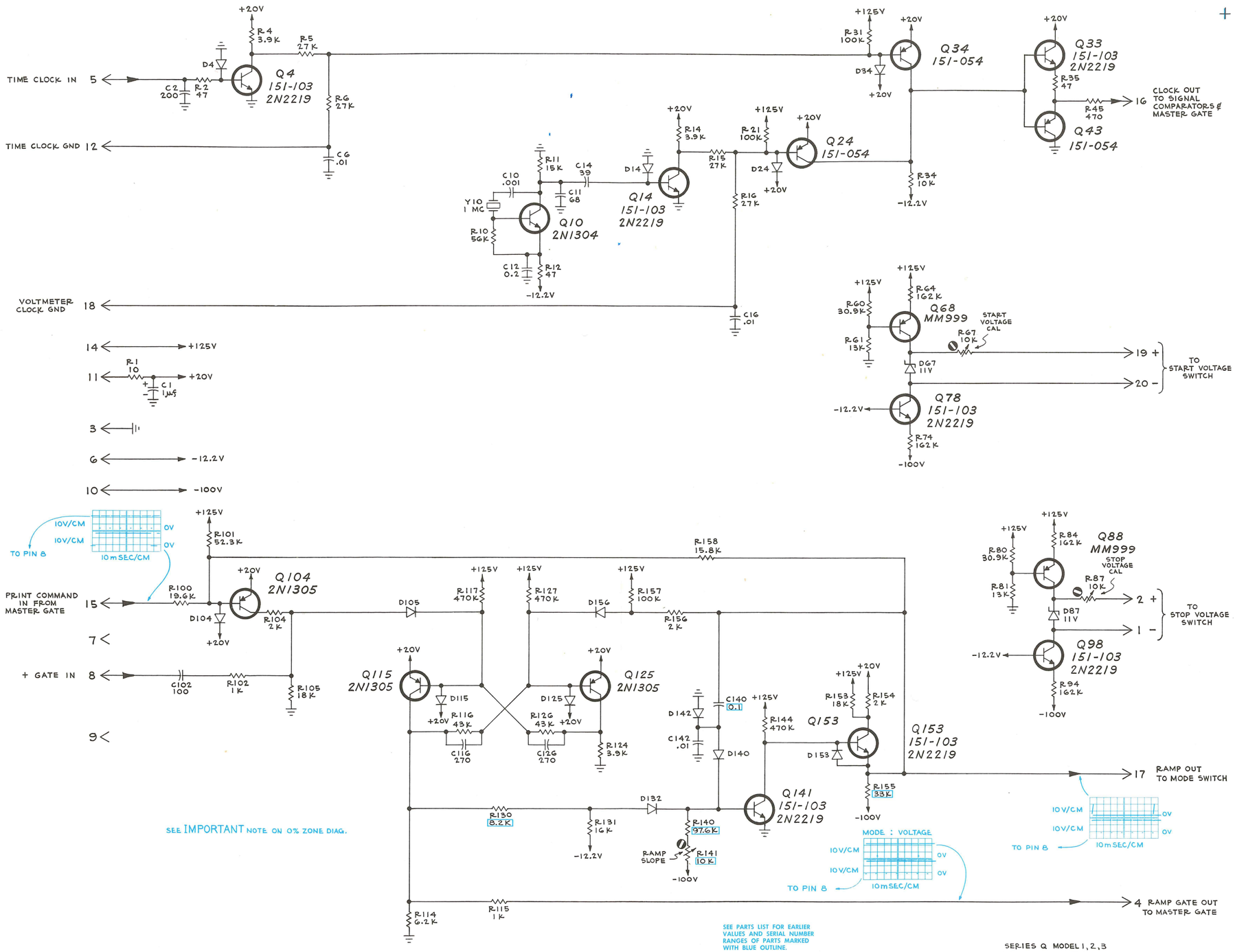
A1

SERIES O MODEL 1

0% ZONE

364

0% ZONE

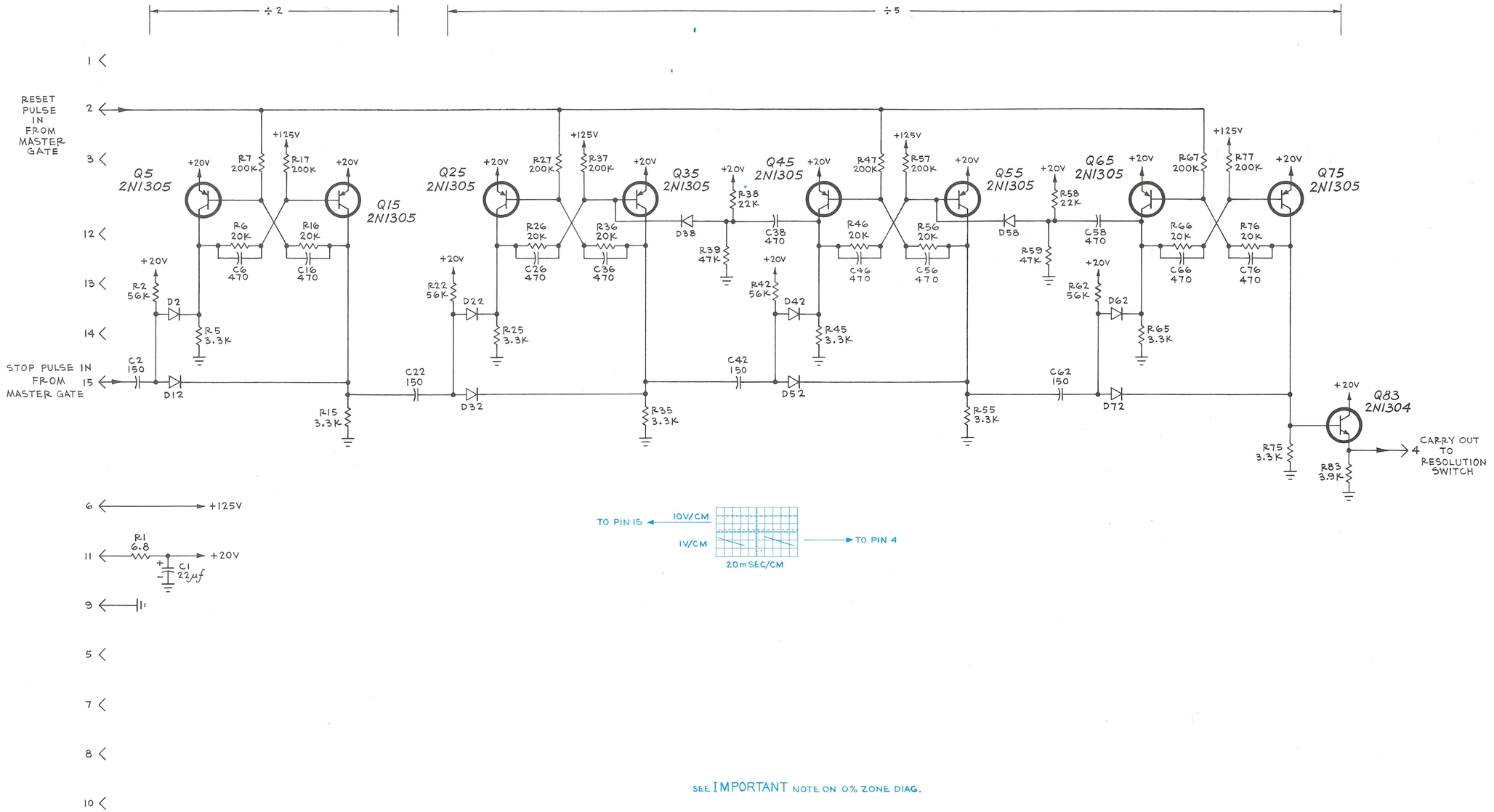


TYPE GR1A

C1

SERIES Q MODEL 1,2,3
VOLTMETER
9G4

VOLTMETER



SEE IMPORTANT NOTE ON 0% ZONE DIAG.

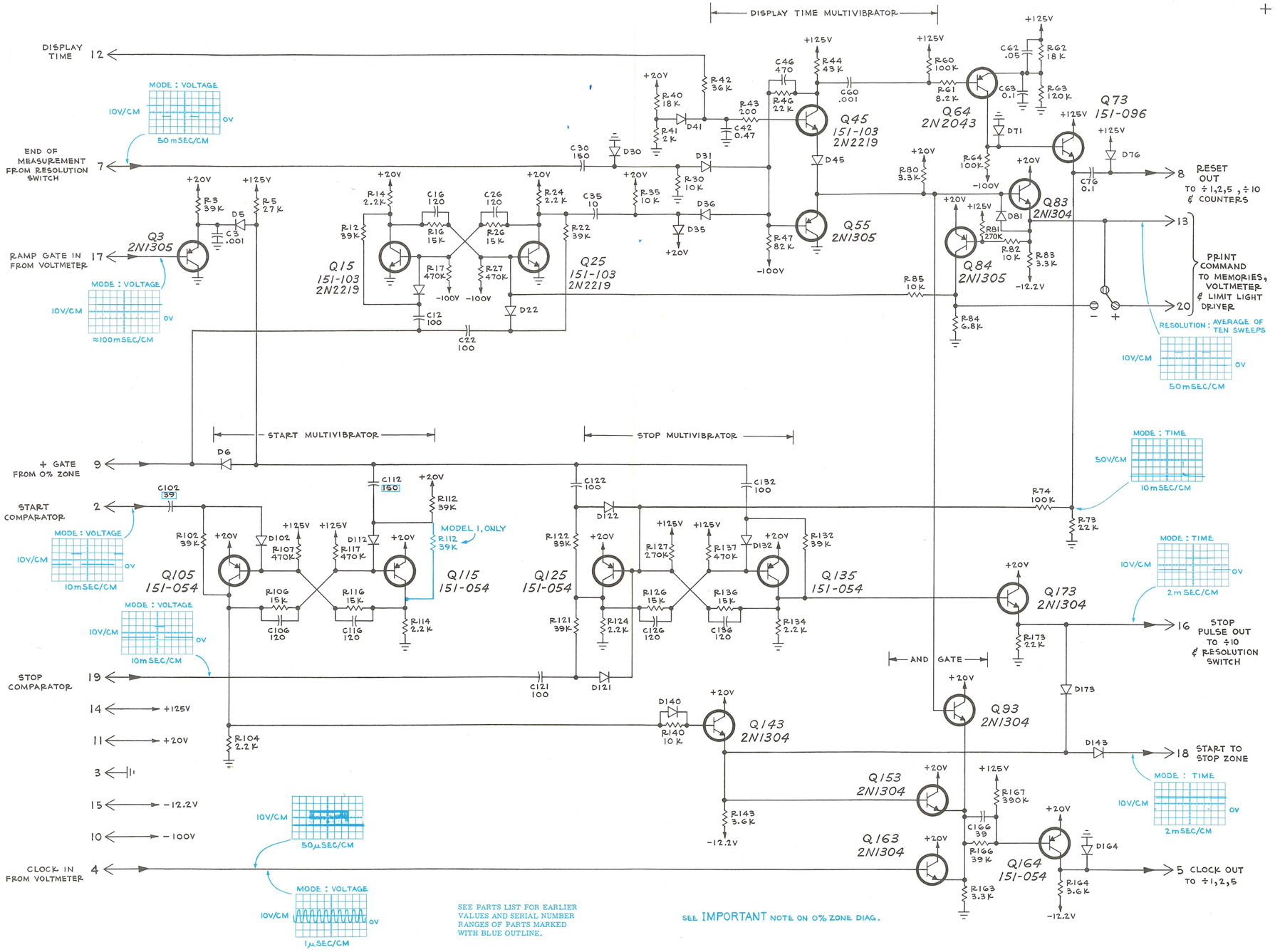
TYPE GR1A

A

SERIES I MODEL 3

÷ 10

GAB 3-9-1

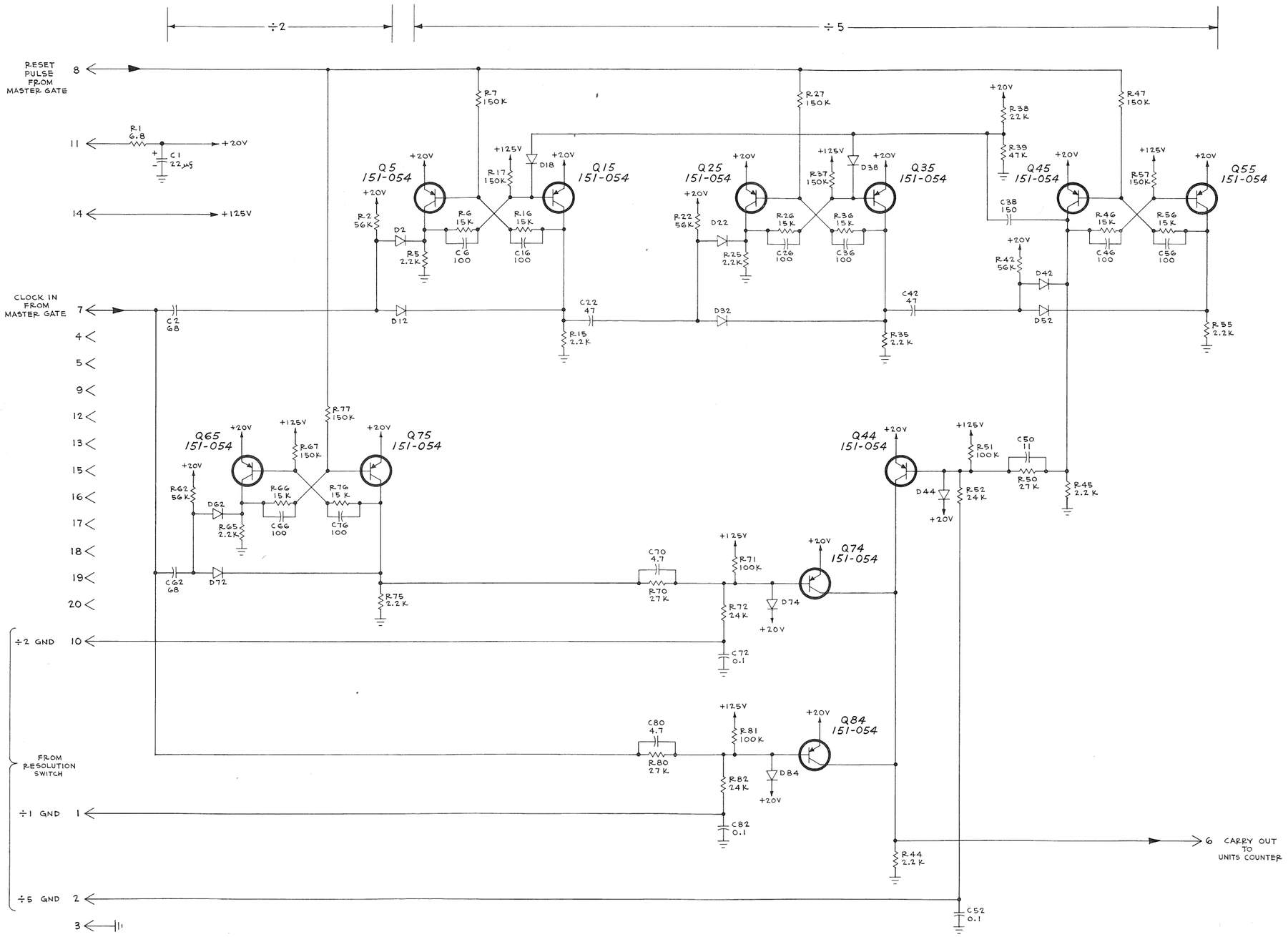


TYPE 6R1A

SERIES M MODEL 1,2,3

MASTER GATE

9G4



TYPE 6R1A

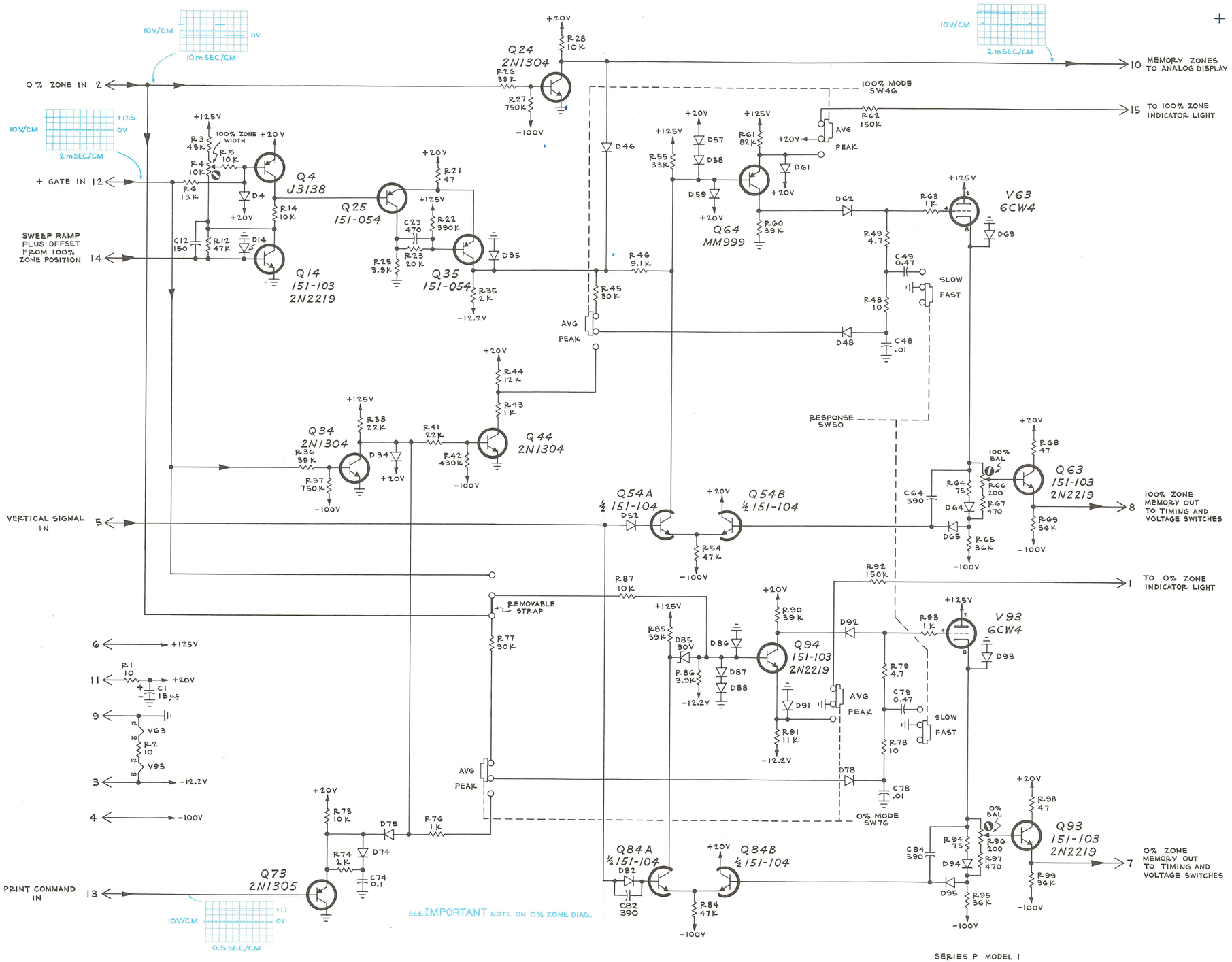
A

SERIES B-MODEL

÷ 1, 2, 5

364

÷ 1, 2, 5



TYPE GRIA

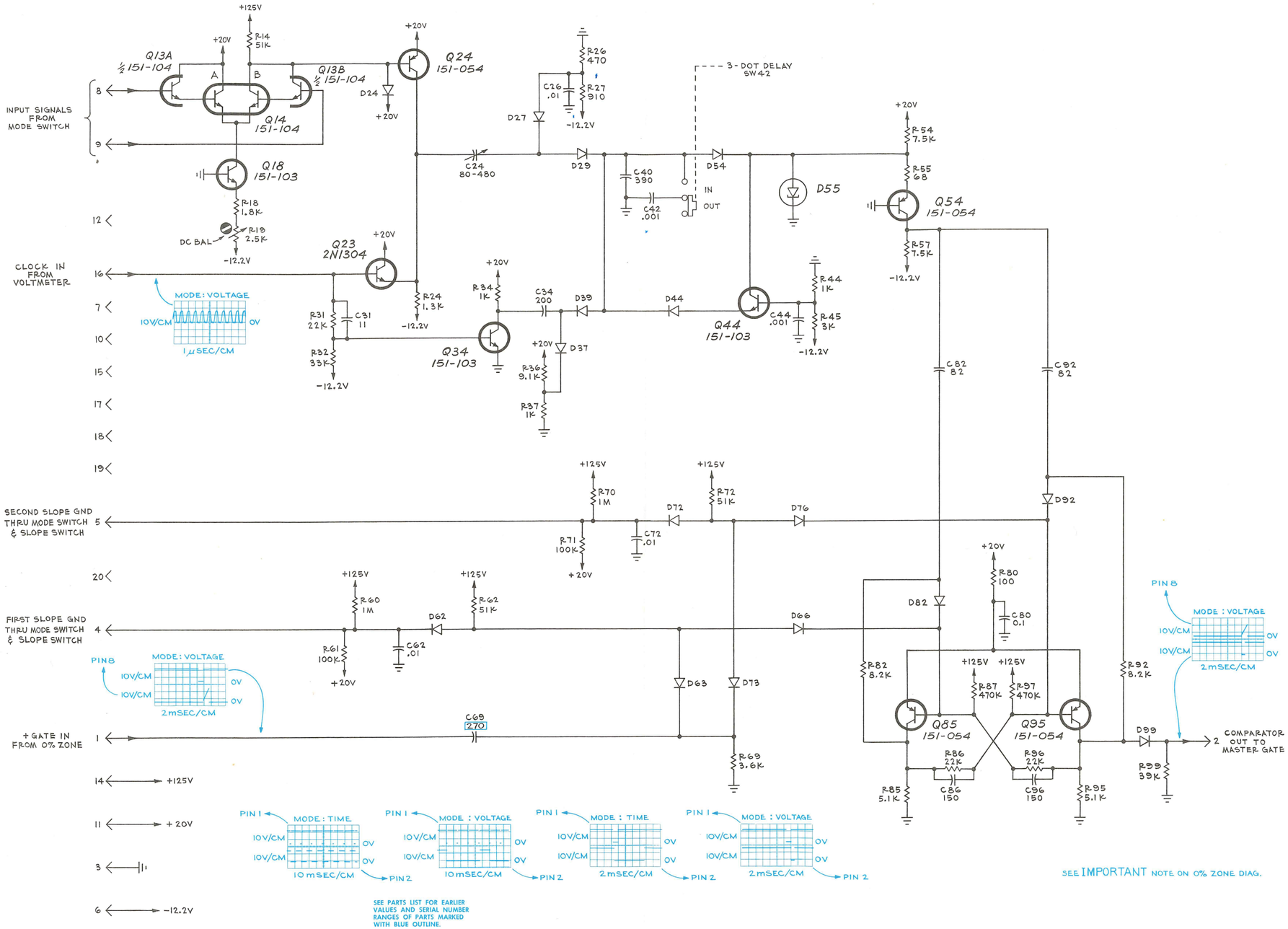
A1

SERIES P MODEL I

0% & 100% MEMORIES

9G4 4F

MEMORY



SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.

SEE IMPORTANT NOTE ON 0% ZONE DIAG.

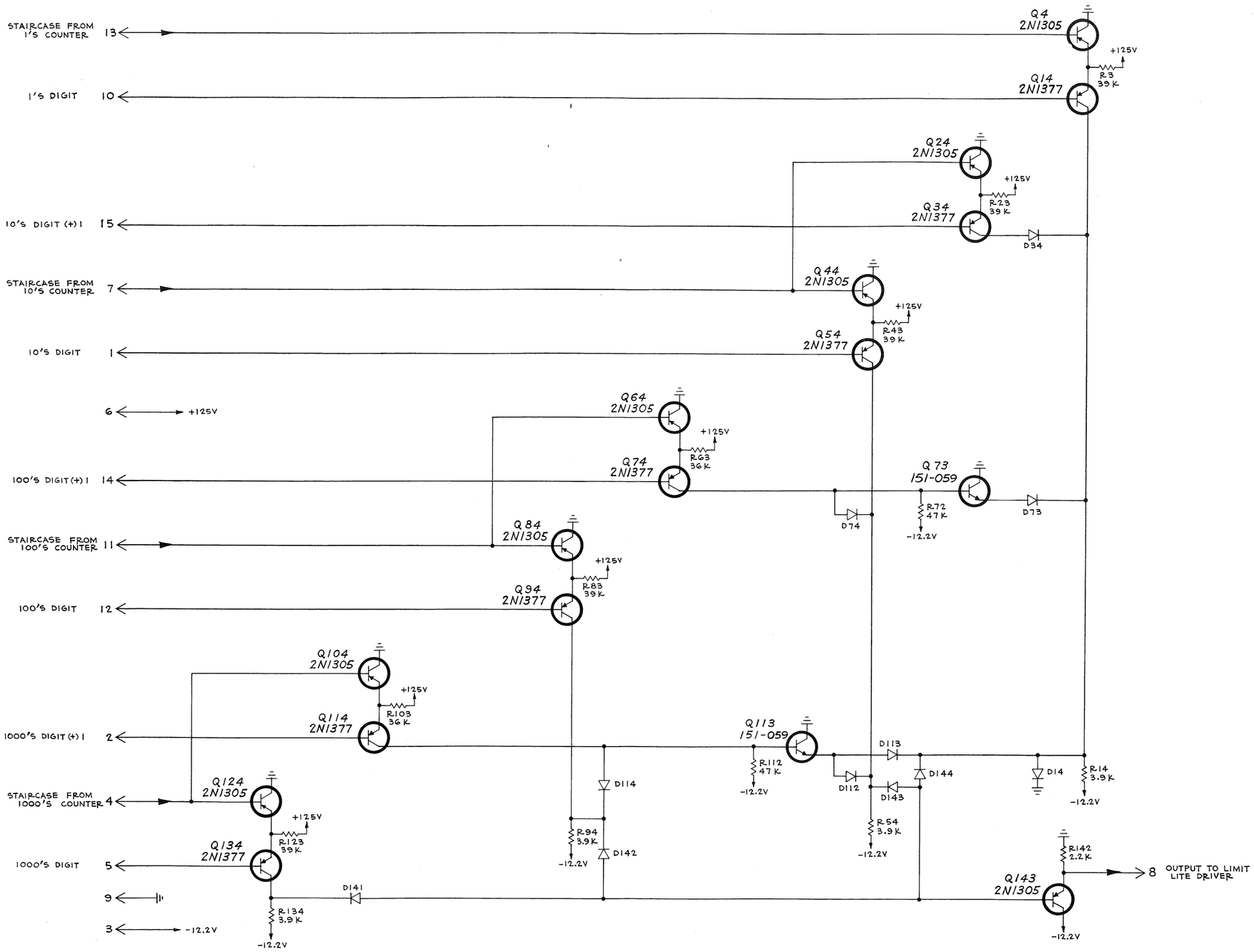
TYPE 6R1A

B1

SERIES N MODEL 1,2

SIGNAL COMPARATOR

GAB 964



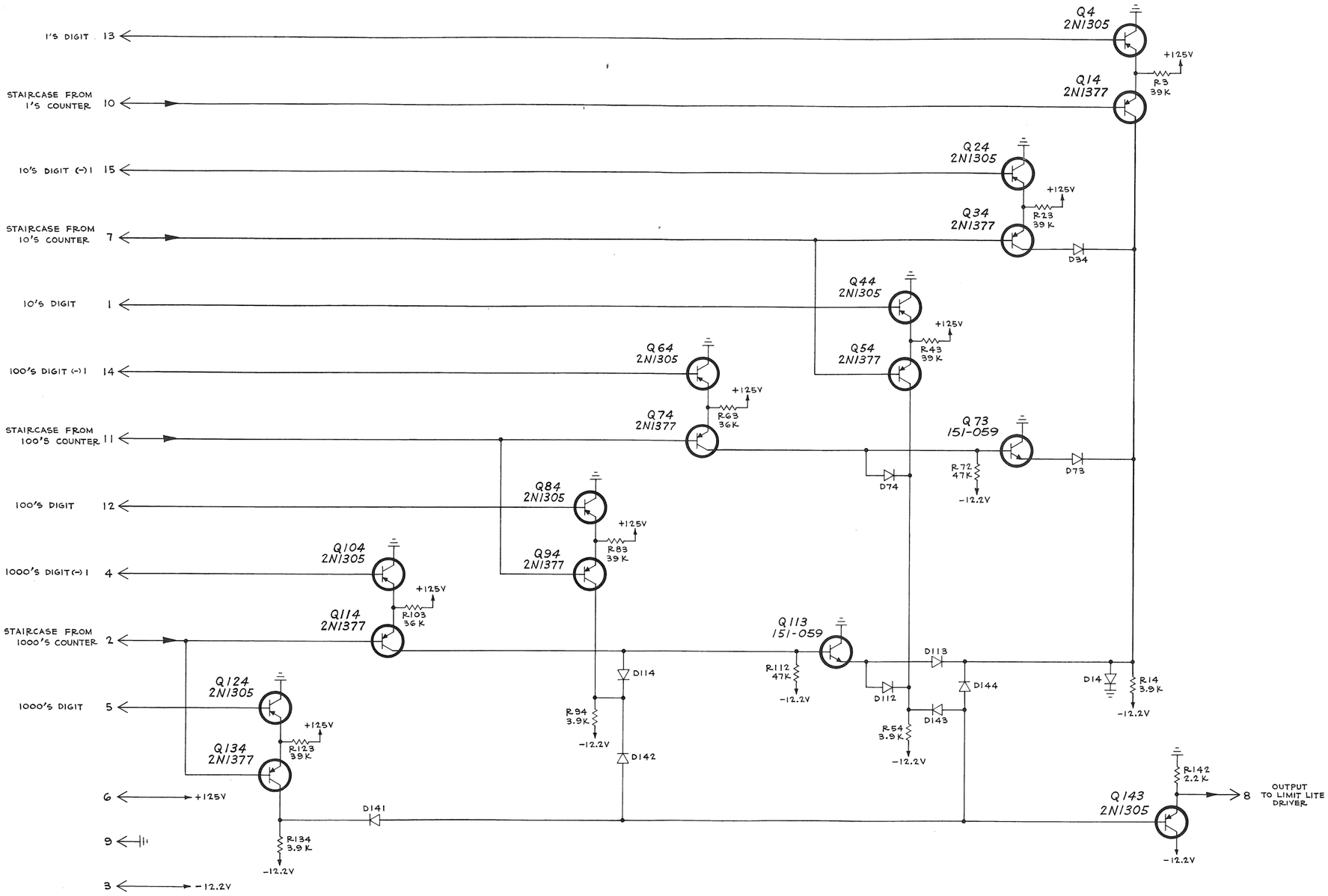
TYPE GR1A

SERIES G MODEL 1A

LOWER LIMIT NO-GO

964

A1



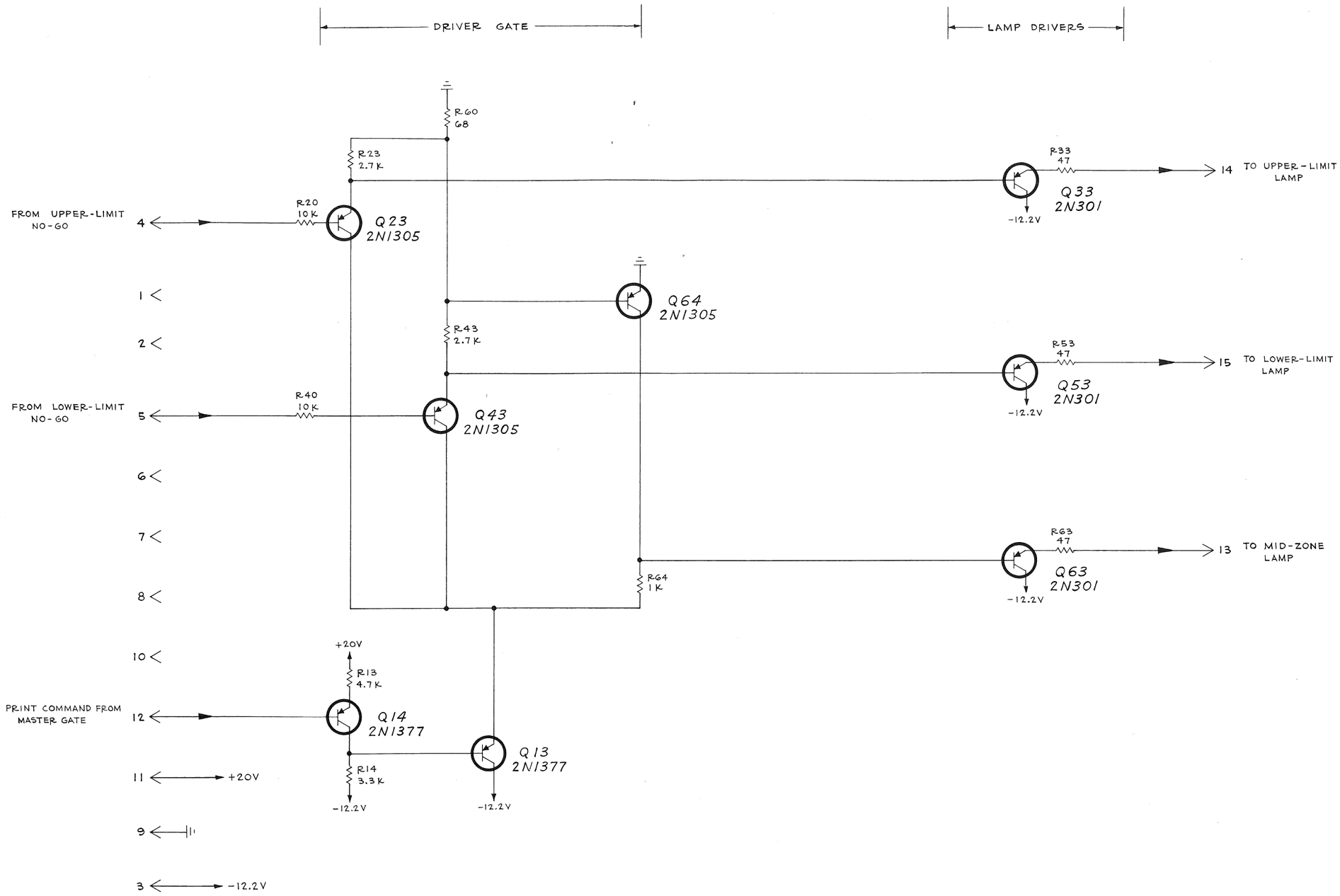
TYPE GR1A

SERIES F MODEL 1A

UPPER LIMIT NO-GO

964

A1



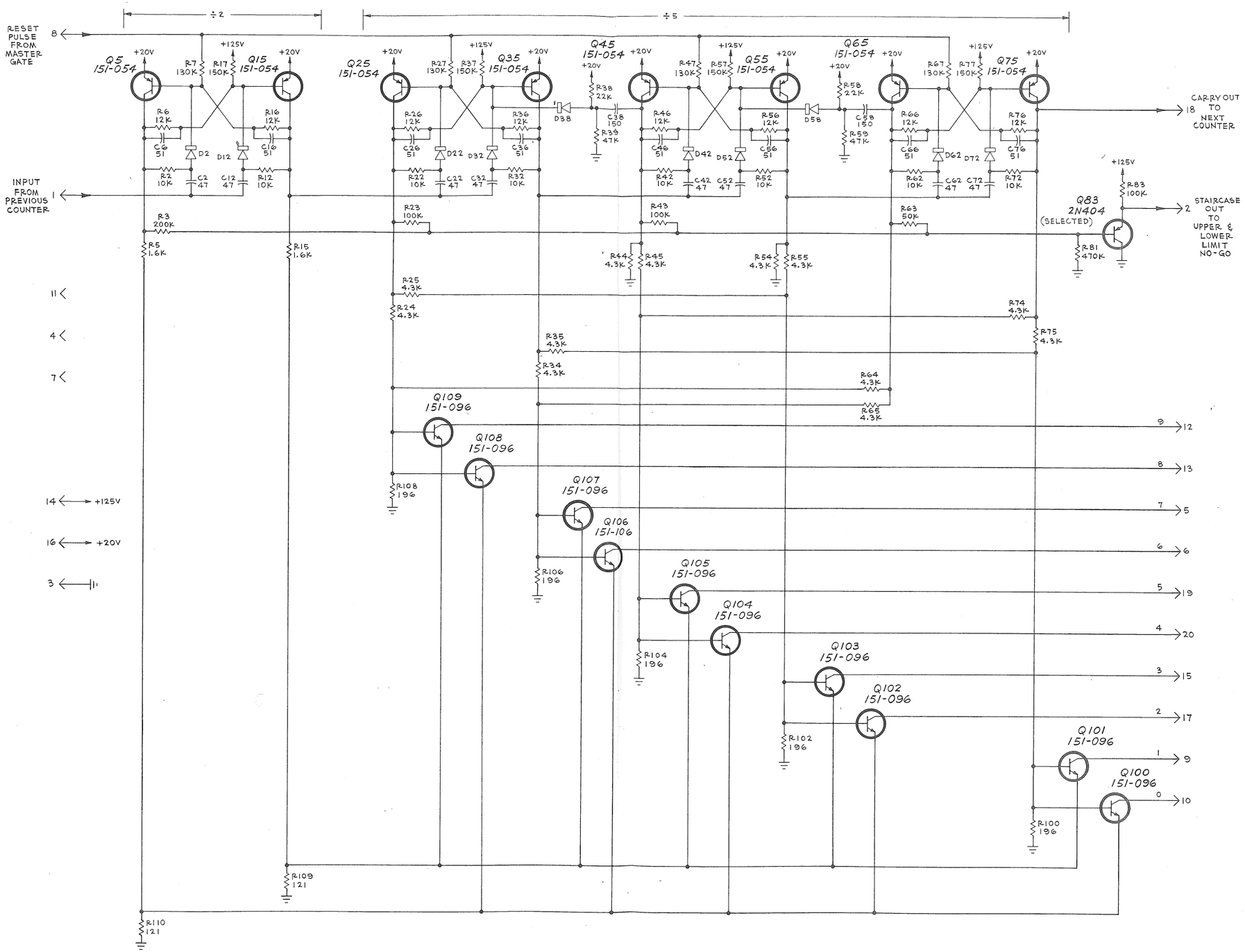
TYPE GR1A

A

SERIES H MODEL 1

LIMIT LIGHT DRIVER

364



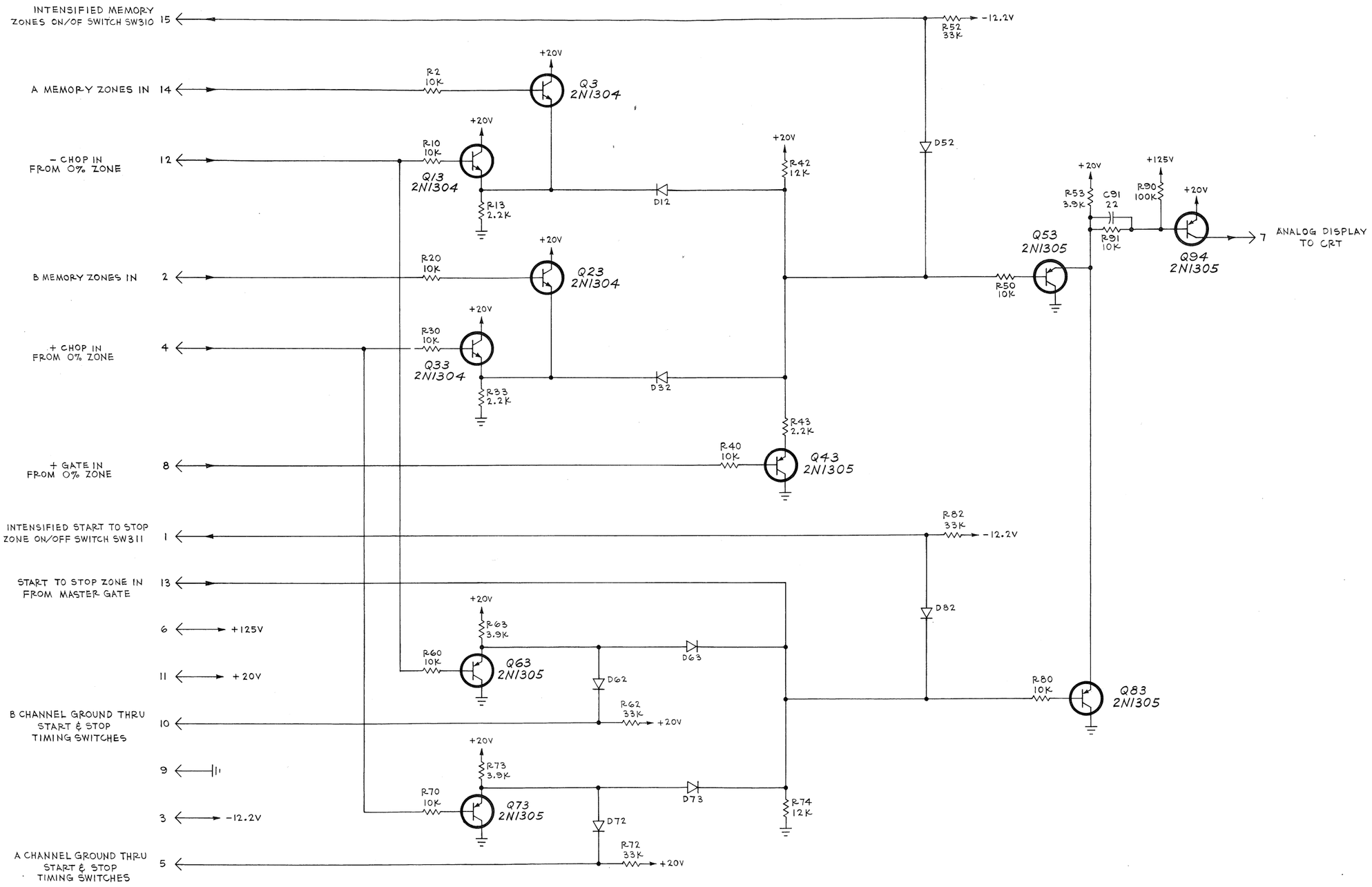
TYPE GRIA

A

SERIES A MODEL 3

COUNTER

GAB 324



SERIES J MODEL 1

ANALOG DISPLAY GAB 364