component news

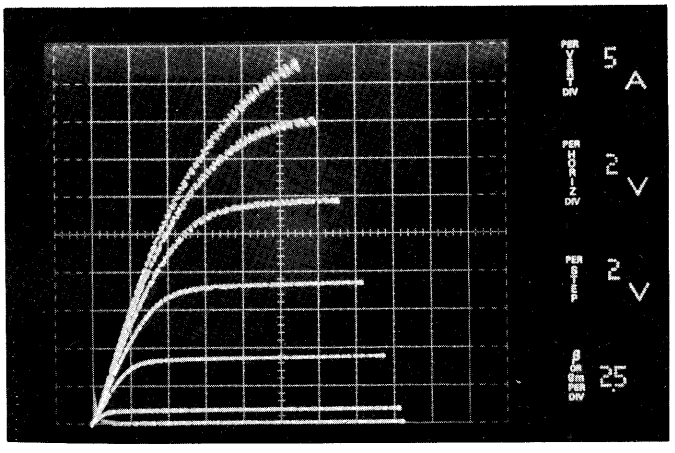
Jan. 22, 1979 COMPANY CONFIDENTIAL Issue 267

FET technology update

More power; higher voltage, current and frequency; and performance beyond theoretical limits can be reported as field effect transistor (FET) technology continues to advance.

As in the recent past, MOS types are leading the way. Almost all are short channel devices (DMOS, VMOS) or an improvement in standard processes to obtain similar results.

Ironically, one of the latest structures to emerge, a power FET with very impressive performance, brings development to a completed circle; it is, in fact, a replica of the very first double-diffused MOSFET.



FETs put out! This VMOS is rated at 16 amps, yet we see it delivering an astonishing 48 amps — the limit of the test equipment (Tek 176). Note super linear g_m of 5 mhos.

Small signal JFETs and MOSFETs are making progress, too. A series of high performance JFETs, not covered in detail in this article, have been introduced by Toshiba, NEC, Hitachi, Mitsubishi and Matsushita. All feature g_m's that are three to four times that of conventional designs (as high as 110 mmhos) and all produce very little noise (0.4 $nV/\sqrt{Hz}$ for Mitsubishi).

In the past two years a lot of "cross-pollenization" has taken place between FET producers, so that it's no longer possible to relate a single supplier to a single process or component type. The following sections are an attempt to unravel any confusion by recapping, by process, the most recent activity showing who's doing what.

DMOS

The familiar form of DMOS (shown on page 5) pioneered by Signetics is now a production process at Solitron and TI as well. Devices have been designed independently by these sources producing an interesting variety of new parts.

In 1978, DMOS finally lived up to its promise of superior high frequency response along with high voltage. A breakthrough at Signetics produced parts that had voltage-speed products greater than the theoretical limit of silicon (200V/GHz predicted by E. O. Johnson of RCA). The 500 mA transistors had f_t's of 1.5 GHz. f_t measurements were made over a range of 10 to 70 volts (the limit of the bias supply) in 10-volt increments. The f_t remained constant, indicating no voltage-frequency effect. This data was forwarded to Johnson himself for verification. Johnson, who is now with RCA's Research Labs in Tokyo, agreed that DMOS

continued on page 2

Also in this issue

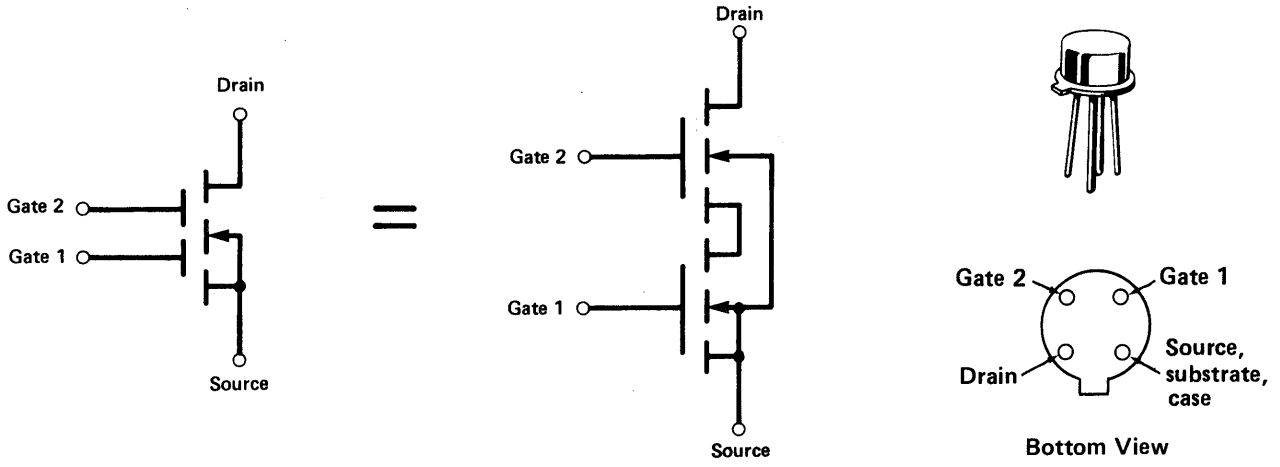


Figure 1 –

Texas Instruments' dual-gate. A dual-gate FET is actually two devices in a cascode configuration (left). As in all cascodes, the feedback from drain to the control gate (gate 1) is very small (0.01 pF in the small part, 0.1 pF in the 500 mA part). The four leaded TO-39 case (right) has its pin arranged for optimum layout. Because the source and gate 2 are at an AC ground, there is a shielding between input (gate 1) and output (drain).

legitimately avoids his limit. Signetics has also introduced a three-times-enlarged version of the part (1.5 amp) with the same outstanding performance. Although breakdown voltages frequently measure 150 and more, Signetics is specifying it at 100V to allow a guardband and some room for process variations. A selected spec of 125V could probably be negotiated.

TI has developed a series of DMOS parts using a process similar to Signetics'. Their line features both single- and dual-gate types also rated at 500 mA (see Figure 1). All have f_t's around 1 GHz with breakdowns as high as 170 volts with the promise of 250 volts in the future.

A small signal version of the dual-gate has been sampled both in singles and matched, monolithic pairs (their DMOS process is self-isolating, so multiple devices are possible on one chip). TI comments that their yields to tight matching specs are excellent and that the price will be competitive with JFET duals (under $2 in quantity).

The matched pair (Figure 2) has potential applications as differential input amplifiers and balanced mixers. Its super high common mode range, f_t and output resistance put it in a class by itself.

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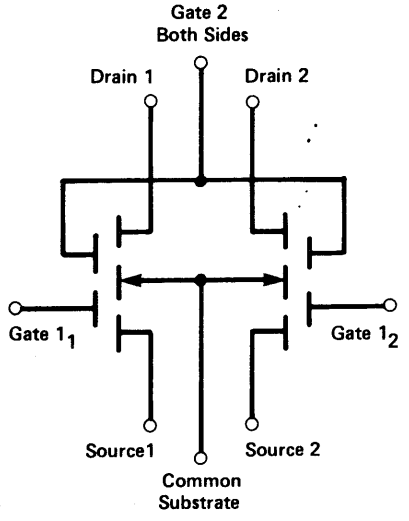
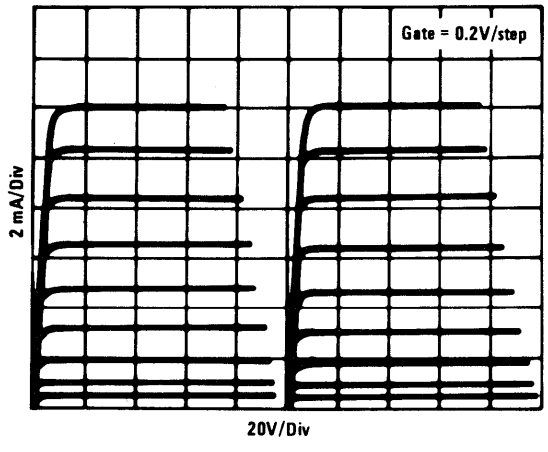


Figure 2 – Texas Instruments' dual dual-gate.

TI's DMOS process yields very well matched duals. Note that high output resistance matches well over large voltage range. Breakdown of this part was 170V.



Solitron is also supplying us with a matched dual (single-gate) DMOS FET — the 151-1117-00 (Figure 3). Although rated at a lower 25 volts breakdown, the single-gate (triode) offers simpler biasing and is adequate for many circuits.

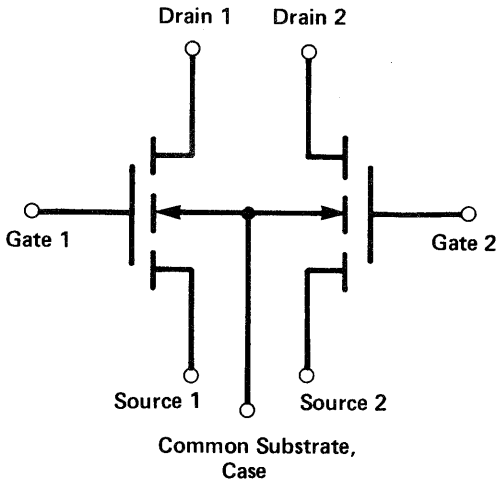


Figure 3 — Solitron dual single-gate

VMOS

Vertical, or V-Groove MOSFETs (Figure 4) are becoming more plentiful as more types are introduced by more manufacturers. Several significant milestones of performance have been reached:

- N and P complementary parts (Supertex)
- 400 volt, medium current switchers (Siliconix, IR)
- 100V, 12-16 Amp N-channel (Siliconix, IR, Intersil)
- Cheap plastic packaging (Siliconix, Supertex)

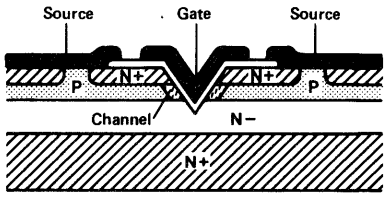


Figure 4 — VMOS FET

Other companies intending to introduce VMOS products are TI, Motorola and probably GE.

Of the field, only Supertex and Hitachi have complementary parts. (The Hitachi FETs are not VFETs. More later.) We have just recently part-numbered a pair of Supertex TO-92 plastic 1 Amp, 60V devices (P/Ns 151-1120-00[P] and 151-1121-00[N]). Expected from them by midsummer is an N and P pair of 15 amp parts. Two voltage ranges are planned — 100 and 200 volts. Supertex also intends to have a line of 400V parts sometime later this year.

A few months ago, in a surprise move, Supertex revealed a *new* vertical FET structure which they believe will make V-groove FETs obsolete. They call it "Vertical DMOS," and have just finished converting their whole product line over from VMOS to the new process. A little later in this article Vertical DMOS will be described and compared to VMOS.

Hitachi/NEC Power MOS

The Hitachi approach to power FETs is just a very large conventional MOSFET. Their original design (see Figure 5) was unique in that the drain was connected to the back of the chip by a deep diffusion. The drain was disconnected from the channel by a lightly doped region (they call it an "extended drain") that functions as a drift region. However, the channel and gate are similar to standard silicon gate devices and are quite long (8μM).

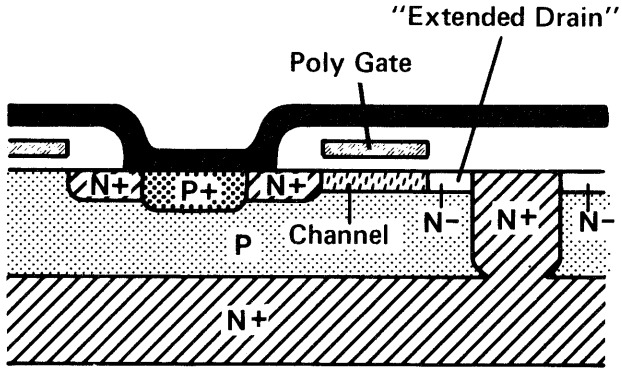


Figure 5 — Hitachi FET (old structure)

Later, the drain connection was moved from the back of the chip to the top (Figure 6) to improve breakdown voltage which had been limited to 100 volts or so but now frequently yields as high as 300 volts. But the new design results in a non-standard TO-3 pin configuration — the case is the source.

continued on page 4

Their long channels limit the transconductance to about 1 mho, considerably less than that of a VMOS of the same size. Also, the polysilicon gate contributes a large series resistance in the gate circuit that causes a high frequency roll-off to a value much below its intrinsic f_t (30 MHz vs. 265 MHz).

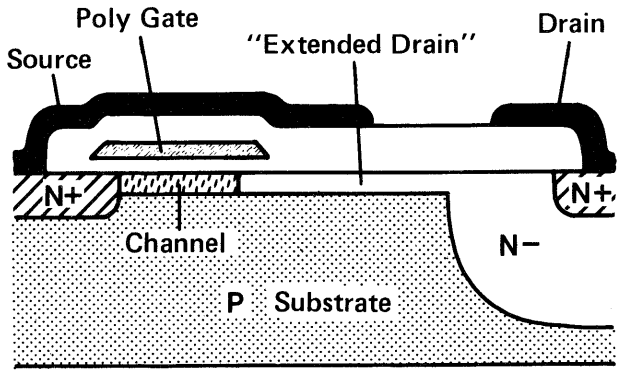


Figure 6 — Hitachi FET (new structure)

While not the pinnacle of performance, Hitachi's FETs are readily available at competitive prices compared to similarly rated bipolars — under $5 — and offer P and N complements.

The parasitic gate resistance can be largely eliminated by using a metal gate. NEC has taken this route in parts similar to Hitachi's.

But, there's still hope for the less expensive polysilicon gate because of work done by researchers at Stanford University [1]. By annealing the polysilicon with a laser, its resistance can be reduced significantly.

Vertical DMOS

DMOS has had the disadvantage of having all three electrodes on top of the chip, making high density interdigitation impossible. As a result, for a given current rating, DMOS was about four times larger than a bipolar or VMOS transistor. Therefore, lateral DMOS is limited to five amps or less in a practical device.

Hitachi, faced with the same problem, solved it by burying the gate under the source metal (see Figure 6). In DMOS, this can't be done without sacrificing its excellent high frequency performance by adding parasitic capacitance and resistance. While such a part would still have high g_m via its short channel, the extra processing complexities would offset even this benefit.

On the other hand, DMOS is superior to VMOS in two ways:

1. it's planar (flat); its surface not "violated" by V-groove etching;

2. and it inherently has more g_m. This is due to the fact that current is conducted horizontally through a channel occurring on the <100> plane of the silicon crystal as opposed to VMOS which operates down the <111> plane. Carrier mobility in a <100> channel is about 35% better than in <111>. Consequently, g_m and f_t, which are directly related to mobility, are about 35% better in DMOS (see Figure 7).

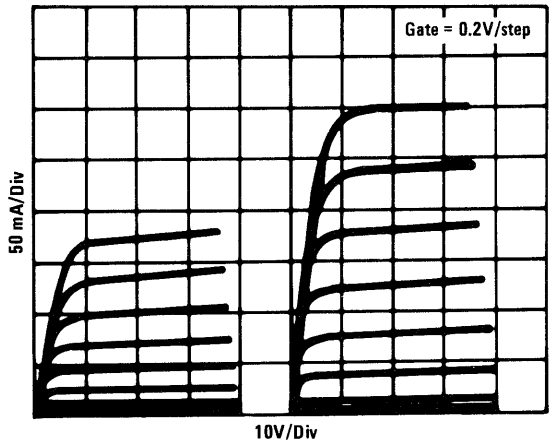


Figure 7 — These two Supertex parts are identical in size and geometry. VMOS (left) has lower g_m than vertical DMOS (right). A difference in carrier mobility is why (see text).

Vertical DMOS is a simple modification to the lateral structure. It can be viewed as a DMOS with the drain diffusion eliminated — being replaced by a drain layer on the bottom (the substrate) or, as a VMOS that has been pulled apart sideways to straighten it out (see Figure 8).

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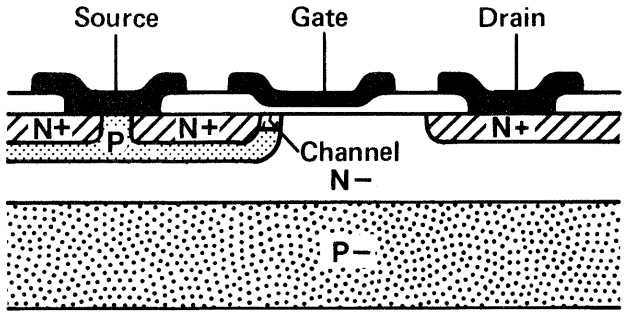
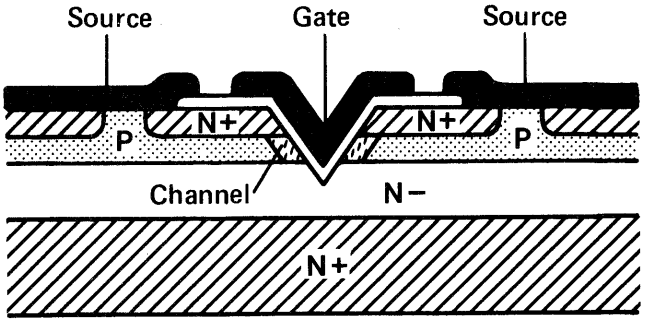
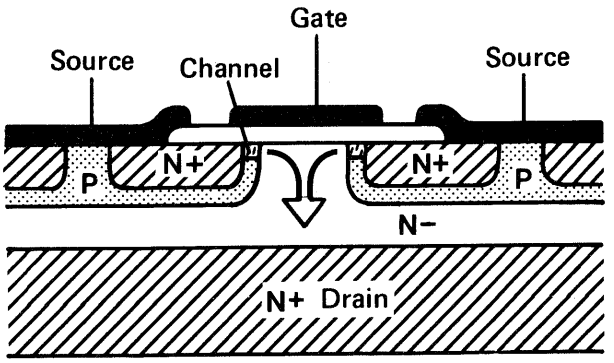


DMOS



VMOS



Vertical DMOS

Figure 8 — DMOS, VMOS, Vertical DMOS

Vertical DMOS certainly is new as far as being a commercial product. But, a little research will reveal that it's not exactly a new invention. Figure 9 is an excerpt from a paper published ten years ago.

Signetics attempted to build a vertical DMOS in 1975 but their results were not too good, so they shelved it and concentrated on lateral DMOS where they have had good success.

Supertex, as mentioned earlier, has made Vertical DMOS their production process. IR also uses it to build their 400 Volt IRF 300, but they use regular VMOS in their 100 Volt, 16 amp IRF 100. They will very likely switch to Vertical DMOS for it, too, in the near future.

Which is better:

VMOS or Vertical DMOS?

Well, it's a little early to tell. The question will probably be settled with the answer to another question: which has the lowest ON-resistance? (See inset, page 7).

While Vertical DMOS has higher g_m, it also has a slightly lengthened path from channel to drain that might contribute to a larger ON-resistance. VMOS proponents claim [3] that by having its gate extend down into the drain (Figure 8) an enhancement of that region occurs when a gate voltage is applied which reduces its resistance. In the near future we should have enough parts from both processes to make a fair comparison.

for more information

In another article to follow soon, several of the more important FET products available will be covered in greater detail, including modeling information and application suggestions. By then some of the bigger and better parts will have arrived.

If you have any questions or comments, please contact me on ext. 7461, or stop by 58-299.

Jerry Willard
Analog Component Engineering

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References:

[1] Semiconductor International, November-December, 1978, pp. 14 and 34.
(Note: In a private discussion with a Stanford research associate, he said the actual improvement was far less than the amount shown on page 34.)

[2] "Optimization of Nonplanar Power MOS Transistors," IEEE Transactions on Electron Devices, Vol. ED-25, No. 10, Oct. 1978, pp. 1229-1234.

[3] "A 600 Volt MOSFET with Near Ideal ON-Resistance," presented at 1978 IEDM, Washington, DC.

History repeats itself!

PROCEEDINGS OF THE 1ST CONFERENCE ON SOLID STATE DEVICES, TOKYO, 1969
SUPPLEMENT TO THE JOURNAL OF THE JAPAN SOCIETY OF APPLIED PHYSICS VOL. 39, 1970

4-1 *Diffusion Self-aligned MOST: A New Approch for High Speed Device*

Y. TARUI, Y. HAYASHI and T. SEKIGAWA
Electrotechnical Laboratory,
Tanashi, Tokyo

A new method of realizing the field effect transistor with a sub-μ channel width is described. The sub-μ channel width is made possible by etching grooves into $n^+pn\ n^+$ structure and using p region at the wall for the channel region of the Metal-Oxide Semiconductor transistor (MOST), or by diffusing two different types of impur[illegible] with the same diffusion mask and using p region at the surface for th[illegible]

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ows a schematical cross-section
.ucture. The gate electrode overlaps

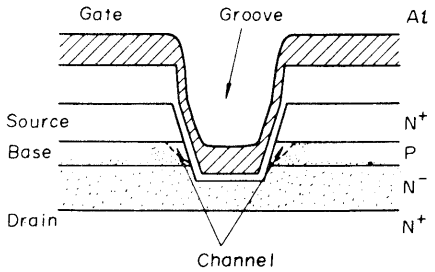
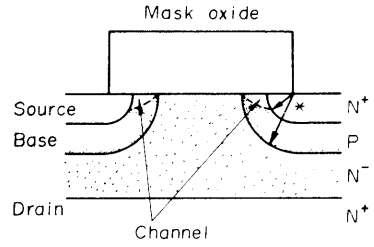


Fig. 2 Cross-section of the diffusion self-aligned MOST (DSAMOST) non-planar type .

the source region through the thin g[illegible]
by sub-μ distance, and the
gate electrode is l[illegible]

Diffusion Self-alignea .



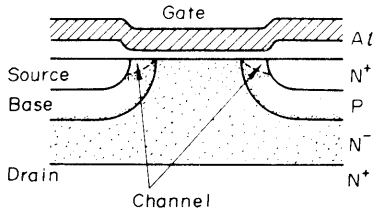


Fig. 3 Cross-section of DSA-MOST —planar type—.
(top) with the diffusion mask, (bottom) with the gate electrode.

iffusion as shown Fig. 3. T[illegible]

Figure 9 — These excerpts are from the original paper describing DMOS, or Diffusion Self-Aligned MOS as the Japanese call it. Not only was the original DMOS vertical, but the other version of it shown here is apparently the first VMOS as well. (The V-groove shown was not etched to the bottom, which is a technique now used by GE and others to improve breakdown voltage.)

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ON-resistance: How low will it get?

A bipolar transistor exhibits a very low saturation resistance because, in saturation, the collector-base junction is forward biased. Injected minority carriers increase the conductivity of the silicon many times over that of its nominal value, which is determined by the doping concentration. However, the injected minority carriers must be removed to stop conduction and the time required to do so (storage time) interferes with the operation of many circuits.

FETs do not have storage time precisely because they do not have forward biased junctions. Rather, their resistance is now that of the doped silicon itself. Some circuits can tolerate the extra saturation resistance, some can't.

Where ON-resistance must be minimized, such as in inverter-converters, the FET must be carefully designed to compete with a similarly rated bipolar. Even then, it will usually have more resistance.

Three factors contribute to a FET's ON-resistance:

1. The resistance and thickness of the silicon material
2. The size (area) of the chip
3. The amount of channel area packed into a given chip area (packing density).

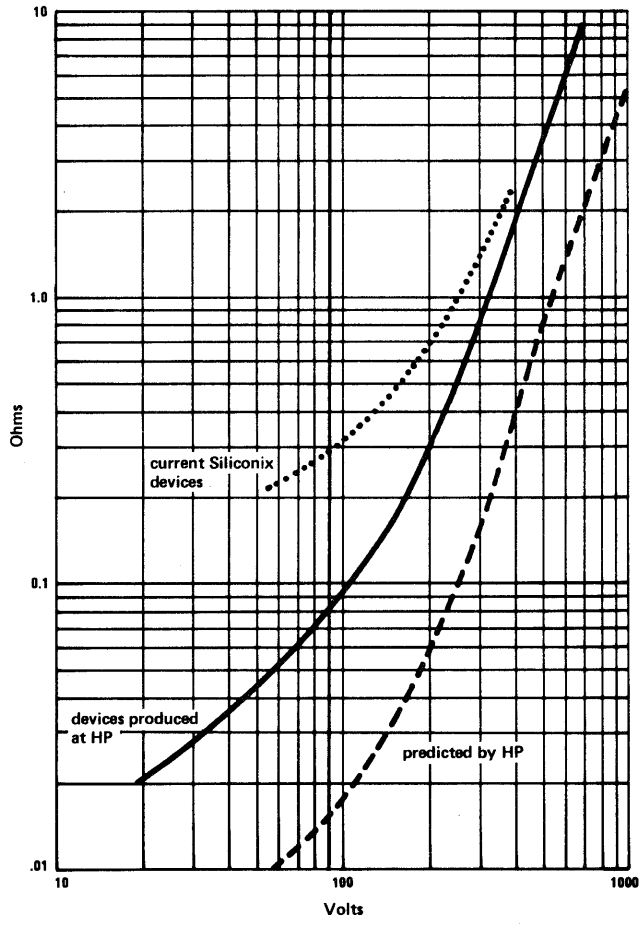
Factor 1 is most significant. It correctly implies that ON-resistance is directly related to breakdown voltage because thick, high resistance drain structures are needed in high voltage parts.

Doubling a FET's channel width is the same as paralleling two discrete parts — the resistance is halved. In the same way, more channel width results in lower ON-resistance whether accomplished through a larger die or packing more channel into the same size die.

There are practical limits to how large a die can get and how much channel can be crowded onto it. Therefore, the question becomes — how low can the resistance be in a device of a practical size and a given voltage rating? Good question. A lot of people are asking it.

Recent reports from Hewlett-Packard and GE [2], [3], go a long way toward answering the question. A very useful graph is given by H.P. that correlates the three factors mentioned above. Their data was measured on a device 2x2 mm (80x80 mils) in size. The accompanying figure shows the same data extrapolated to a die size of 180x180 mils (a size common in power transistors).

When polled, some manufacturers expressed the opinion that H.P.'s low values were unrealistically low. Others, however, agree that they can be attained but perhaps not in a mass produced part.



Commercially available FETs have a way to go in reducing ON-resistance, according to HP's findings. However, developments are definitely heading in that direction. The lowest values shown will probably remain theoretical for some time.

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FET Product Roundup

DMOS (all are N-channel)

Vendor	Product	Comments
TI	Small signal dual-gate, 150V, 1 GHz Monolithic matched pair of above 500 mA single-gate, 150V, TO-39 500 mA dual-gate, 150V, TO-39	Available, no Tek P/N Available, no Tek P/N Available, Tek Search Spec Available, Tek Search Spec
Signetics	Extensive line of small signal 25V parts 500 mA single-gate, 100V, 1.5 GHz 1.5 amp single-gate, 100V, 1.5 GHz	151-1103-00, 156-1303-00 (Quad.) 151-1104-00 Available soon in TO-220
Solitron	Small signal single-gate monolithic matched pair	151-1117-00

VMOS (all are N-channel)

Siliconix	Extensive line of 1.5 amp parts 12.5 A, 80V, TO-3 (VN84G) 4 A, 200V, TO-3 2.5 A, 400V, TO-3	151-1108-00 Available, no Tek P/N Available, no Tek P/N Available, no Tek P/N
IR	16 amp, 80V, TO-3 (IRF 100)	Available, no Tek P/N
Intersil	5 amp, 65V, TO-39 (0.4Ω R_{ON}) 15 amp, 100V, TO-3	151-1119-00 Available mid-'79

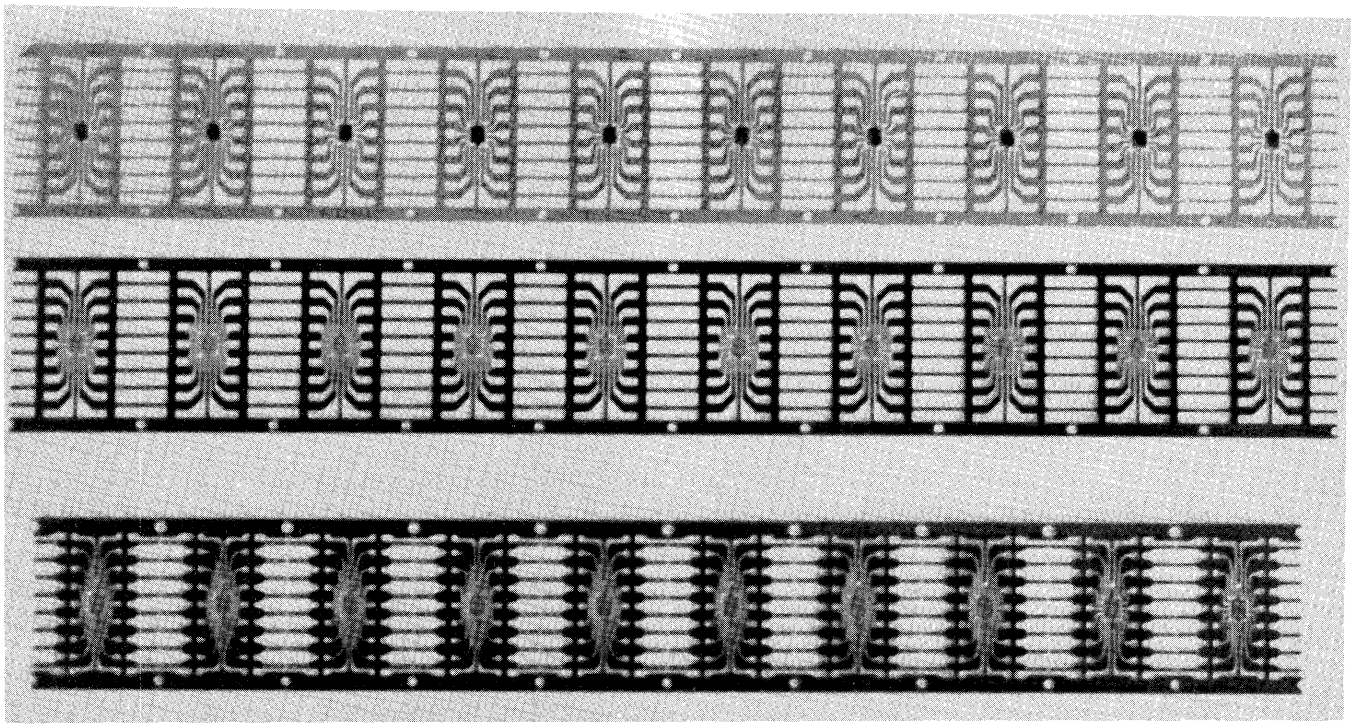
Vertical DMOS

Supertex*	1 amp, 60V, TO-92 P-channel 1 amp, 60V, TO-92 N-channel 15 amp, 100V, TO-3 P-channel 15 amp, 100V, TO-3 N-channel 15 amp, 200V, TO-3 P-channel 15 amp, 200V, TO-3 N-channel 3 amp, 400V, TO-3 N-channel	VP3 151-1120-00 VN3 151-1121-00 Available later in '79. Also in TO-220. " " "
IR	3 amp, 400V, TO-3	Available, no Tek P/N

Power MOS

Hitachi	7 amp, 140V, TO-3 N-channel 7 amp, 140V, TO-3 P-channel	Available, no Tek P/N Available, no Tek P/N
NEC	7 amp, 140V, TO-3 N-channel 7 amp, 140V, TO-3 P-channel	Samples not yet received Samples not yet received

*Supertex is the supplier for a line of similar parts sold by Fairchild and ITT.



Top: Old style lead frame with overall gold plating, 0.756-inch pitches and flat lead tips.
Center: Interim-use lead frame, same dimensions as above except with spot gold and solder coat.
Bottom: New style lead frame with spot gold plating, 0.720-inch pitches and pointed lead tips.

LEAD FRAMES NOW SPOT-GOLD PLATED

Lead frames are die-cut strips of "units," usually ten to a strip, that are the connectors in dual in-line packages (DIPs). When cut apart from each other these units are the leads to which integrated circuits, microprocessors and microcomputers are mounted and externally wired.

For about ten years the industry has standardized on lead frames made of Kovar with 80 to 100 microinches of spot gold plating on the mounts and out-leads, a 0.720-inch pitch (centerline unit-to-unit), and pointed lead tips for ease in insertion in a circuit board. (Kovar is a 29% nickel, 17% cobalt, 54% iron alloy.)

Tek, on the other hand, has continued to specify that its lead frames have overall gold plating of about 100 microinches with 0.756-inch pitches and flat lead tips. This has put us out of synch with the industry, and has resulted in expensive custom ordering from our vendors. Also, Tek-made DIPs have traditionally experienced insertability problems due to their flat lead tips.

All of this is going to change, however. Effective immediately, all 16-lead frames used by Tek (except, for the time being, copper-clad frames) will conform to the above-mentioned industry standards. Sixteen-lead frames amount to 80% of our total usage, which is expected to reach 1.6 million frames in 1979.

The change will save over $400,000 each year in gold plating along!

To accommodate the new design and dimensions, IC Manufacturing is spending $91,000 for new molds, mold press and die cutter — a small amount when contrasted with the savings in raw materials alone.

Plans to expand this standard to include the remaining 20% of usage (the 20-lead and mini-pak types) will be based on performance and experience with the 16-lead frames.

During the interim, ICM will use lead frames with present (0.756-inch) dimensions, but will change to spot gold and solder coating in place of overall gold plating. These frames will be available by period 909. Mods have been written and accepted on P/Ns 155-0022-00 through 156-0027-00. The remaining 26 P/Ns will follow.

For more information please contact **Sudi Kulkarni, Senior Process Engineer, IC Manufacturing (ext. 7074).**

Wire Prep part-numbers wires

Wire Prep currently constructs about 24,000 different configurations of wires for Tektronix instruments. After these wires are constructed they are assembled into kits and distributed to the various instrument lines. However, due to the large number of configurations, it has become impossible to plan and control this manufacturing area by manual methods.

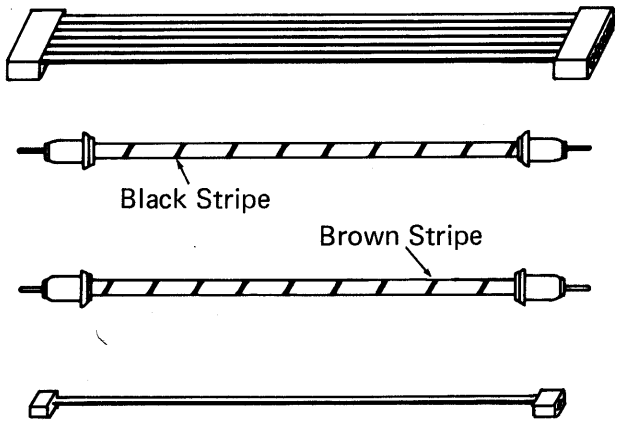
As a result, an effort is underway to put a Tek part number on each one of the configurations in Wire Prep so that the processes can be managed by computer-assisted methods.

As part of the project, it will be necessary to set up all new kits in the following manner:

- Each striped wire configuration will have a Tek part number. Most of these are currently set up.
- All new wire configurations will be assigned a part number, depending upon the material from which they are made.
- Anything that is "Wire, Electrical" will have a 195- 196- or 197- prefix part number and will be renamed "Lead, Electrical."
- All cable configurations made from "Cable, Special Purpose Electrical" or "Cable, RF" will have a 175- or 178- prefix, and will be renamed "Cable Assembly, RF" or "Cable Assembly, Special Purpose Electrical."

Whenever possible, wire kits will not be set up and wire or cable assemblies will be shipped directly to the instrument lines as an end item.

For example, if an instrument requires four wires to connect the vertical amplifier to the rest of the instrument, the Bill of Materials would be set up in the following manner: One wire is actually a six-conductor, flat cable. Two others are peltola cables (one has a black stripe and the other a brown stripe). The last wire is a single connector wire. They would be constructed as follows:



The Bill of Materials should be structured this way:

7603 (INSTRUMENT)
670-1442-00 (VERTICAL AMPLIFIER KIT)
198-3154-00 (WIRE KIT)
175-0108-00 1 ea. (PELTOLA CABLE)
177-1120-00 1 ft.
210-0774-00 2 ea.
210-0775-00 2 ea.

175-0109-00 1 ea. (PELTOLA CABLE)
177-1120-00 1 ft.
210-0774-00 2 ea.
210-0775-00 2 ea.

178-1900-00 1 ea. (RIBBON CABLE)
131-0707-00 12 ea.
352-xxxx-00 2 ea.
175-xxxx-00 1 ft.

195-9000-00 1 ea.
(SINGLE CONDUCTOR WIRE)
177-1200-00 1 ft.
131-0707-00 2 ea.
352-xxxx-00 2 ea.

We expect to begin this process some time in March, and all new kits set up after that time must be structured in this fashion. If you have any questions, please contact **Mike Waggoner, Project Mgr., ext. 5796; Dick O'Brien, Scheduling Mgr., ext. 7345 (Vancouver); or Bud Siegle, Wire Prep Pilot, ext. 7364 (Vancouver).**

Mike Waggoner

Environmental stress degrades LCDs

We've received numerous inquiries lately about liquid crystal displays (LCDs). This is understandable because they are low power devices that are visually appealing to many people. LCDs are also easy to customize – you pick a standard glass size and the manufacturer merely puts on the electrodes to display whatever message you want.

There is one big problem associated with LCDs, though; they won't pass the standard ten-day humidity test we perform on components. The trouble lies not in the display itself, but rather in the external polarizers which can't take the combination of high temperature and high humidity.

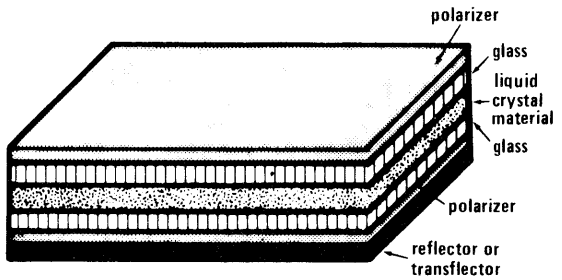


Figure 1 – Construction of LCD

An LCD consists of liquid crystal material sandwiched between two layers of glass (see Figure 1). On the outside, a polarizer is glued to the top of the display. Then another polarizer, plus reflector, is glued to the bottom.

The polarizers are made by taking polyvinyl alcohol (PVA), which is a thin plastic film, and stretching it. This stretching action lines up the molecules, and then the sheet is dyed with iodine. It is then laminated to a thicker piece of plastic for rigidity.

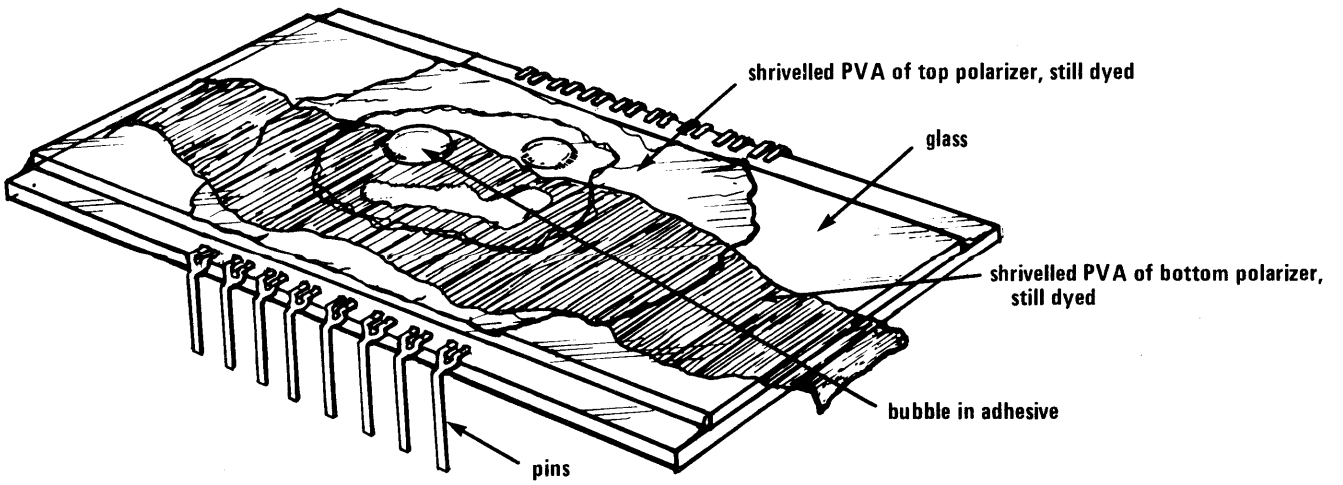
In the humidity test, a ten-day test that temperature cycles the parts from 25°C to 65°C at 95% relative humidity, the polarizers bleach out. The iodine sublimes out, leaving clear plastic with no polarizing properties. In more extreme cases, the PVA tends to shrivel up as well (see Figure 2). The crystal itself is still good, and the display still works if you replace the polarizers.

Because the LCDs won't pass the ten-day humidity test (the mere mention of this test makes LCD manufacturers shudder in horror), we have tried testing them to the humidity requirements of Class 3 instruments per MIL T 28800B. This test's most severe conditions are 95% RH at 55°C. Polaroid's standard polarizer fades somewhat in this test, but the display is still legible. Displays put through the Class 5 test (worst case – 95% RH at 25°C) don't fade at all.

Polaroid does make a "K-polarizer" which is a high stability-type material. This is made the same way as the standard polarizers, except that

continued on page 12

Figure 2 – Display with K-polarizer after 10-day test



the iodine molecules are chemically bonded to the PVA molecules, to keep the polarizer from bleaching out. This polarizer is specified to withstand 120 hours of 95% RH at 49°C. It still shrivels up in the ten-day test, but survives the Class 3 test well. Manufacturers generally have this polarizer available as an option, at roughly 10 to 20 cents more per display.

Beckman buys its polarizers from Sanritsu, a Japanese company. They have a "premium" polarizer also, but it bleaches out in the ten-day test. However the polarized reflector only bleaches out around the edges. Beckman displays do well in the Class 3 test.

In addition to the problems with polarizers, there are problems with some of the reflectors. Crystaloid uses several types of reflectors. Their "diffused reflective" backing has a grainy appearance and blisters during testing (see Figure 3). Instead of this backing, Crystaloid recommends using the "brushed aluminum" reflector, which has a flat appearance. It doesn't blister as badly in the ten-day test, and doesn't blister at all in the Class 3 test.

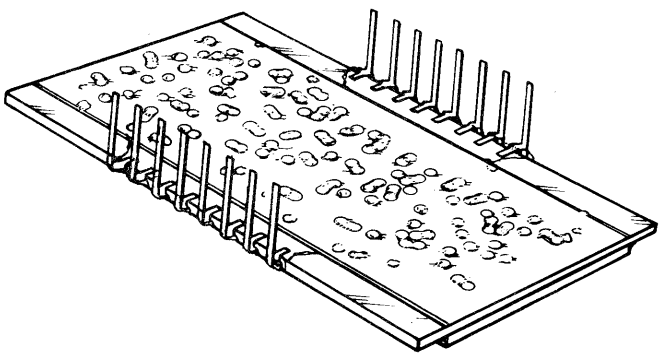


Figure 3 — Display after test; reflector on bottom blistered

The final problem is the adhesives. In many cases the reflectors and polarizers loosened from the glass or fell off during testing. In cases where the polarizers loosened, they usually resealed after being removed from the humidity chamber, but bubbles often got trapped underneath (see Figure 4). Motorola plans to start clamping the polarizers on mechanically sometime in the future.

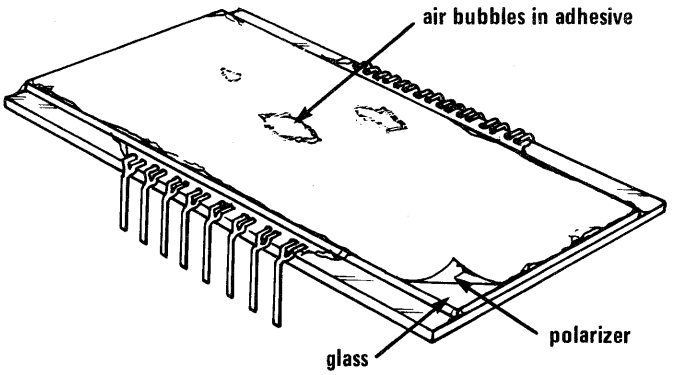


Figure 4 — Display after test showing bubbles in adhesive after polarizer "resealed"

The moral of the story is: if you're considering using LCDs, give some thought to your environmental requirements. Are the displays good enough for your application?

If you're interested in looking at some displays that have come out of various tests, contact **Betty Lise Anderson (ext. 6389), or stop by 58-299.**

Missing μC board

Would whoever borrowed the TM990/100M microcomputer board from the Component Engineering area (58-299) please return it immediately!

The 64K RAM race is on!

Designs for the 64K dynamic RAM are starting to be released, and we in CE are starting to get a picture of what is coming. The picture is by no means clear at this time, but some things are becoming apparent.

Fujitsu

The first semiconductor manufacturer to announce the 64K RAM was Fujitsu. The part uses +7V and –2V power supplies. Because of the power supply requirements and some other features of the part, this device has not been taken very seriously by either semiconductor or equipment manufacturers in the U.S.

IBM

The IBM part appears to have been designed for the "world of IBM." It does not offer any major technology advances that the semiconductor houses are anxious to adopt. The IBM part does appear to be the first 64K RAM in large production, but the market for the part is unique. Outside of the fact that IBM has a 64K RAM reducing their memory cost, which in itself gets the attention of the electronics world, the part does not appear to have had much influence on the rest of the semiconductor industry.

"5V-only" bandwagon

The U. S. manufacturers definitely appear to be lined up behind a 5V-only part. TI was the first to announce such a part. Being first is not always best in this business, and TI may also find this to be the case. The TI part uses 256 refresh cycles (supposedly every 4 mS) and no substrate bias (substrate = GND). There is reason to believe that the part was actually designed for +8V and –3V power supplies and is now being adapted to +5V only. Although Tek has yet to receive samples, the readings obtained from the industry are not particularly favorable. The lack of adequate substrate bias and the 256-cycle, 4 mS refresh time presently appear to be questionable designs. However, TI has assured us that their design is fine.

National Semiconductor also appears to have taken the 256-cycle, 4 mS refresh approach. Their cell and sense amp designs are different from TI's, and it is still too early to comment on the design. More details of the part are to be released at the ISSCC in February.

The other U. S. manufacturer to announce a 5V-only part is Motorola. Presently, the Motorola design appears to be superior to TI's (without actually testing the chips). We expect samples from both TI and Motorola in the first quarter of 1979. Motorola uses a substrate bias generator and 128 refreshes every 2 mS. The operation of this part sounds very similar to what Intel and Mostek have indicated for their 64K RAMs. Mostek and Intel have yet to release what function will be on Pin 1. Motorola uses Pin 1 for on-chip refresh. If Motorola, Mostek and Intel agree on the specification of the 64K RAM and are able to build it, the momentum to make this the standard 64K RAM would be enormous.

NEC

NEC is presently recommending a +7V and – 5V power supply part. The reasons relate to their more conservative design philosophy. They do not presently believe that they can build a 5V-only part in large volume with the yields and reliability they expect. There is no doubt, however, that designs for a 5V-only part are being pursued by NEC in case they are needed.

VMOS

As for the VMOS designs at AMI and Siemens, they do not appear to be shaking up the rest of the world. The additional complexity of the VMOS technology in memory chips does not appear to be offset with the superior performance needed to compete in this market. With the advances that Intel in static RAMs (~400 pS gate delays) and Mostek in 64K ROMs have made using HMOS-type technology, it is presently questionable whether VMOS has much of a future in memory chips.

conclusion

Thus, the 64K RAM race is now on, and it should be an exciting race. For the moment it appears that Motorola, Mostek and Intel are the ones to watch; however, the race is yet to be won. Within the next six months, the picture should become much more clear.

Ron Burghard and Eric Peterson

GPIA chip progress report

Motorola XC68488

Several samples of the XC68488-HH mask have recently been evaluated. This mask will not be put into production, but represents the next-to-last design stage for the device. The last stage of the design will be the "M2H" mask, which we expect to be complete in January.

The primary and secondary address recognition has been completely redesigned relative to the 'GG' mask part. It appears that the design is now in compliance with IEEE-488 (see **Component News 253,** pages 2-3). The device will hold in Accept Data State (ACDS) for secondary address recognition only when the last primary address on the bus was My Listen Address (MLA) or My Talk Address (MTA).

Other changes are as follows:

1. Setting 'My Secondary Address' (msa) bit false has no ill effect. In the 'GG' parts, this action caused the part to become hung, unable to respond to the Unlisten command or to Interface Clear.

2. The address status bits 'LPAS' (Listen Primary Address State) and 'TPAS' (Talk P.A.S.) are only functional when extended addressing is enabled. Previously, these two bits would always indicate that MLA or MTA had at some time been received.

3. In the Talk-Extended (TE) function implementation, if a secondary address had previously been accepted by setting 'msa' true, any new secondary address placed on the bus automatically clears the 'msa' bit, thus providing the exit from Talk Addressed State (TADS) on receipt of an Other Secondary Address (OSA). This exit transition had not previously been implemented.

The XC68488-HH still has the problem of undetected data loss following serial poll (see **Component News 262,** page 20). This problem will be designed out of the 'M2H' mask part, but the 'M2H' device will still have one undesirable defect because there will be no facility for clearing the data-out register or for clearing the END message. This means that instruments implemented with the 68488 must have their output buffers flushed by the GPIB controller following an abort condition such as Device Clear.

In addition, the SPAS bit will still be capable of disappearing after having caused an interrupt, and the SRQ pin must be externally pulled up through 10K to +5V.

Because of these problems and because there are alternative choices available at competitive prices, with relatively fewer problems, the 68488 is not recommended for new designs.

Intel 8291

Problems with this device have been noted before (see **Component News 263,** pages 7-10; and **265,** page 14). Several points in these articles need to be corrected and expanded on.

In the earlier article, the description of data input is in error. The Acceptor Handshake (AH) function will hold in Acceptor Not Ready State (ANRS) until the data-in register is read, rather than proceeding one full cycle as stated.

To expand on the problem noted in the later article, we have found that three of the state change interrupt bits actually *invert*, rather than *set*, on state change. Those bits are SPASC, REMC and LLOC. These bits invert regardless of the state of other interrupt status bits. On the other hand, the ADSC bit will not back up in the master register when ADSC is enabled to cause interrupts. Thus, multiple Addressed State Changes will be read out of the device as *one* interrupt, rather than as *two.* It appears that all four of these bits are functioning improperly.

A clarification of the function of Interrupt Register 2 is also necessary. The three status bits read in Register 2, (SPAS, REM and LLO), represent the past state of the device, sampled at the time of Interrupt Request, rather than the state of the device at the time of read. These bits are "frozen" along with the interrupt bits.

If you have any questions regarding these GPIA chips, please contact me at 58-125, ext. 6303.

Jim Howe

Input wanted for reliability survey

Component Test Engineering (CTE) is a relatively new department in Manufacturing Engineering. CTE is chartered to provide long-range capability for testing and preconditioning purchased components. We work closely with Incoming Inspection, Component Preconditioning & Test, Component Reliability Engineering and Component Evaluation Engineering. We also work with the managers and engineers in the various product lines.

CTE tries to foresee the need for capital equipment, such as component test and burn-in systems used in Incoming Inspection and Component Preconditioning & Test. After a need has been determined and evaluated, we provide input on budgeting requirements and assist with the required justifications and CCAs.

reliability survey underway

Ron Schwartz, Component Reliability Engineering manager, and personnel from CTE have been informing the product lines as to the degree of testing and burn-in their components will require to meet product goals. Goals such as reliability, quality and availability of components are discussed. Recently, particular attention has been paid to digital ICs.

The decision concerning the degree and type of testing required must be made **now** to allow CTE time to justify equipment for FY000 budgets. Feedback is needed immediately to provide proper equipment to meet your needs.

To this end, CTE has sent out a "Usage Survey" to the product lines asking for specific information. It is essential that we receive answers well before the FY000 budget cycle begins. If you have questions regarding the level of reliability, availability or cost of ICs, call Ron Schwartz (ext. 6511), and/or reference **Component News 261,** pages 9-12. If you have suggestions relating to the future of Incoming Inspection and Component Preconditioning & Test, call me on ext. 5186.

Your product line should have already received its questionnaire. If not, call Ron or me.

Paul Wohlfarth, manager
Component Test Engineering

NPI Project Manager role defined

In June of 1978, a communications concept was introduced to help increase the effectiveness of new product program development between the business units and Central Manufacturing.

The concept involves placing a person from Central Manufacturing into each of the major business units with accountability for enhancing communications between these groups on new product development programs. This person, called an NPI Project Manager, works with the business unit's development teams to help assure that questions on part buildability, process capabilities, component testing, cost analysis, etc., get communicated to the correct people in Central Manufacturing.

The Project Manager is an NPI resource whose efforts will help provide a smoother transition from product concept to customer availability.

Presently there are three NPI Project Managers assigned to business units. They are: Kathy Rudyk, Communications Division; Jerry Sherrill, Measurement Systems Division; and Tom Schaper, Logic Development Products.

How is the concept working? According to Dale Vanderzanden, manager of Manufacturing Engineering NPI, it's still too early for an in-depth appraisal, but the overall concept as well as the NPI Project Managers have been well accepted by the business units. We are now getting a much better understanding of mutual concerns and problems that affect a product's development program, and are working toward easier solutions to problems in the NPI process.

If you have further questions about the NPI Project Manager concept, please call Dale at ext. 5644.

Tom Schaper
Manufacturing Engineering NPI

ComponentNewsNewComponents

This column is designed to provide timely information regarding new components, vendors, availability and price. "New Components" can also be used as an informal update to the Common Design Parts Catalogs. Samples may or may not be available in Engineering Stock.

Vendor	No.	Description	When available	Tek P/N	Approx. cost	Engineer to contact
		analog devices				
Fujitsu	2SC2527	Transistor, NPN 120V, 10A, RET, TO-220 pkg., 80 MHz	2nd Qtr.	in process	$ 1.35	Jim Williamson, 5345
Fujitsu	2SA1077	Transistor, PNP 120V, 10A, RET, TO-220 pkg., 60 MHz	2nd Qtr.	no P/N	1.50	Jim Williamson, 5345
Motorola	MJE350	Transistor, PNP, 0.5A, 300V, TO-126, complement to 151-0311-01	1st Qtr.	151-0698-00	0.98	Jim Williamson, 5345
NEC	2SA1006B	Transistor, PNP, 1.5A, 250V, TO-220, 25W, 80 MHz, emitter ballasted	1st Qtr.	151-0696-00	1.15	Jim Williamson, 5345
NEC	2SC2336B	Transistor, NPN, 1.5A, 250V, TO-220, 25W, 95 MHz, emitter ballasted	1st Qtr.	151-0697-00	1.05	Jim Williamson, 5345
TRW	ZN6587	Transistor, Power, NPN, 120A, 450V, switching, TO-61 isolated case	1st Qtr.	in process	12.00	Jim Williamson, 5345
Motorola	MMBT3906	Transistor, 2N3906, SOT-23 type	——	no P/N	0.23	Matt Porter, 7461
Motorola	MPSH10	Transistor, complement to 151-0438-00, MPSH81	now	no P/N	0.70	Matt Porter, 7461
		digital devices				
National	27014	IC, Asynchronous Communications element, INS8250	now	no P/N	5.00	Bill Pfeifer, 6303
National	MM74C374	IC, CMOS 8-bit latch	now	no P/N	1.75	Wilton Hart, 7607
		electromechanical devices				
AMP	67887-1	Connector, plug, elect., ckt. bd., 72 contacts	——	131-1147-01	——	Peter Butler, 5417
		optoelectronic and passive devices				
H-P	5082-4955	LED, green, 3 mcd	now	150-1071-00	0.75	Betty Anderson, 6389
Allen Bradley	CC3.244FZ	Resistor, fixed, film: 3.24 MΩ, 1-B, 0.125W, TC=TO	Feb. 1	321-1720-00	——	Ray Powell, 6520
Dale	MFF1226G69-R80F	Resistor, 69.8 Ω, ½W, 1-B	Feb. 1	323-0082-00	——	Ray Powell, 6520

TECHNICAL STANDARDS

The function of Technical Standards is to identify, describe, and document standard processes, procedures, and practices within the Tektronix complex, and to insure these standards are consistent with established national and international standards. Technical Standards also provides a central repository for standards and specifications required at Tektronix. *Chuck Sullivan, manager (58-187)*

new publications

Vaughn Weidel, Product Safety, has created an omnibus of standards material in the form of a research paper for a class at Portland State University. Subject matter includes information on standards activity in the United States, such as ANSI and UL, the Consumer Product Safety Commission, and proposed Federal controls of the Voluntary Standards associations. The paper may be reviewed at 58-123. Vaughn's phone is ext. 7357.

Product Safety and Loss Prevention, a booklet published by the National Safety Council, contains: Common Sources of Product Liability, Product Safety and Product Loss Prevention Program, Key Elements of the Consumer Product Safety Act, Identification Data Required by CPSC.

new NEMA publications

ICS1-1978 General Standards for Industrial Controls and Systems.
ICS2-1978 Standards from Industrial Control Devices, Controllers and Assemblies.
ICS3-1978 Industrial Systems.
ICS4-1977 Terminal Blocks for Industrial Control Equipment and Systems, includes Revision 1.
ICS5-1978 Resistance Welding Control.
ICS6-1978 Enclosures for Industrial Controls and Systems.

available from reprographics

Drafting Standard 062-2476-00, Symbols and Practices for Schematic Diagram Drafting, is available from Reprographics, ext. 5577. This standard identifies reference designations and graphic symbols to be used in documentation of electrical and electronic parts and equipment. The standard is based on the work of the Ad Hoc committee consisting of a representative from each manuals group within Test and Measurement. It includes the most frequently used symbols from ANSI (American National Standards Institute) Y32.2-1975, plus symbols devised for use by Tektronix that are not included in the ANSI standard.

Carol Jones, ext. 6224
Technical Standards

NOTICE: Technical Standards procures many external standards for Tek people, but we cannot maintain lists of users. Therefore, if you are using a document over five years old, or have a critical application, call us to see if the document is the latest issue.

Catalog of the National Bureau of Standards Publications covers a wide range of subjects and a short summary of the contents of each. Also has an alphabetical index of authors and subject matter. This catalog is much more than a list of names; it has high value as a source of information for every Tektronix function.

NOTICE: The August 1978 issue of the Common Design Parts Catalog, Vol. 3, Materials, lists new ASTM alloy numbers for Copper, Brass, Copper Beryllium, Phosphor Bronze and Stainless Steel. In order to properly identify these alloys on drawings it will be necessary to use the new alloy numbers.

For example, PN251-0342-00, Brass Sheet, previously identified as Alloy 260, is now Alloy C26000.

Other possible changes in material designations by ASTM will be announced when/as they occur.

for information on the above publications, please call Carol Whitmore, Technical Standards, ext. 7976.

Tek instrument availability

For many applications, the need for vendor-supplied instruments can be satisfied by utilizing Tek-made products. Before requisitioning any 3½-digit DMM, compare your requirements with the specs and features of our DM501s and DM502s.

If you still have concerns about your "special application," contact the Calibration/ Certification Lab manager, Gene Brox (ext. 5397). Gene can assist you on measurement techniques and instrument applications.

Occasionally non-saleable units are available under modified acquisition policy. Contact Joe Rowland (ext. 7141) for transfer details.

Ray Barrett, manager
Instrument Control

Return lost notebook

Someone borrowed a black loose-leaf notebook on aluminum electrolytic capacitors from Component Engineering. It is very important to our work, so please return it as soon as possible.

Splicing tape no longer available

I have been informed by Purchasing that splicing tape (Tek P/N 006-1856-00) is no longer available. Anyone having a need for this tape should contact me by *February 28, 1979.*

Jakee Ius, ext. 5937
Central Mods

COMPONENT

RICHARD DUNIPACE

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