TDC1007

Monolithic Video A/D Converter
8-bit, 20MSPS

The TDC1007 is an 8-bit fully parallel (flash) analog-to-digital converter, capable of digitizing an input signal at rates up to 20MSPS (megasamples per second). It will operate accurately without the use of an external sample-and-hold amplifier, with analog input signals having frequency components up to 7MHz.

A single CONVert (CONV) signal controls the conversion operation of the device which consists of 255 sampling comparators, encoding logic, and a latched output buffer register. The device will recover from a full-scale input step in 20ns. Control inputs are provided to format the output in binary, two's complement, or inverse data coding formats.

The TDC1007 is patented under U.S. Patent No. 3283170 with other patents pending.

Features

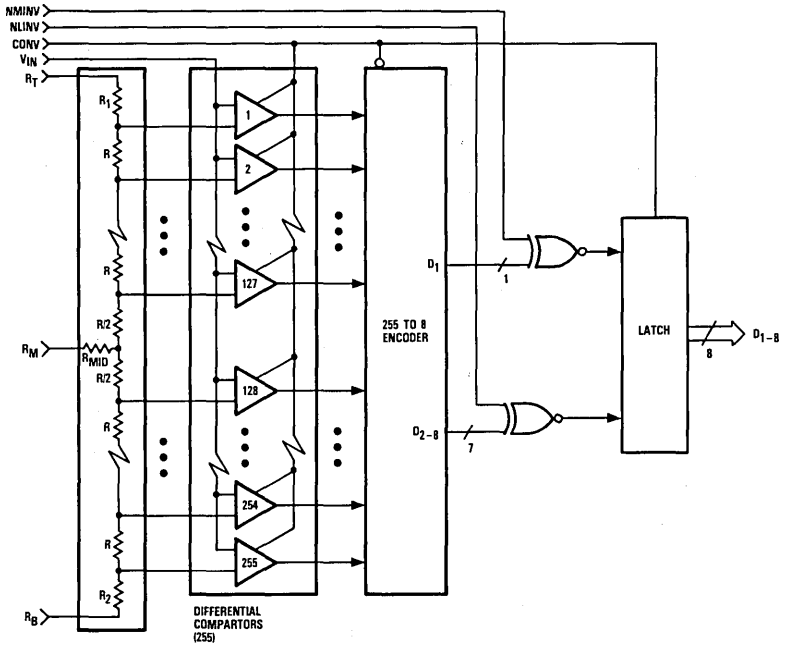
- 8-Bit Resolution
- Conversion Rates Up to 20MSPS
- Sample-And-Hold Amplifier Not Required
- Bipolar Monolithic Construction
- TTL Compatible Inputs and Outputs
- Binary or Two's Complement Mode
- Differential Phase = 1.0 Degrees
- Differential Gain = 1.7%
- Evaluation Boards Available: TDC1007E1C or TDC1007P1C

Applications

- Video Systems 3x or 4x Subcarrier, NTSC or PAL
- Radar Systems
- High-Speed Multiplexed Data Acquisition
- Digital Signal Processing

D

Functional Block Diagram



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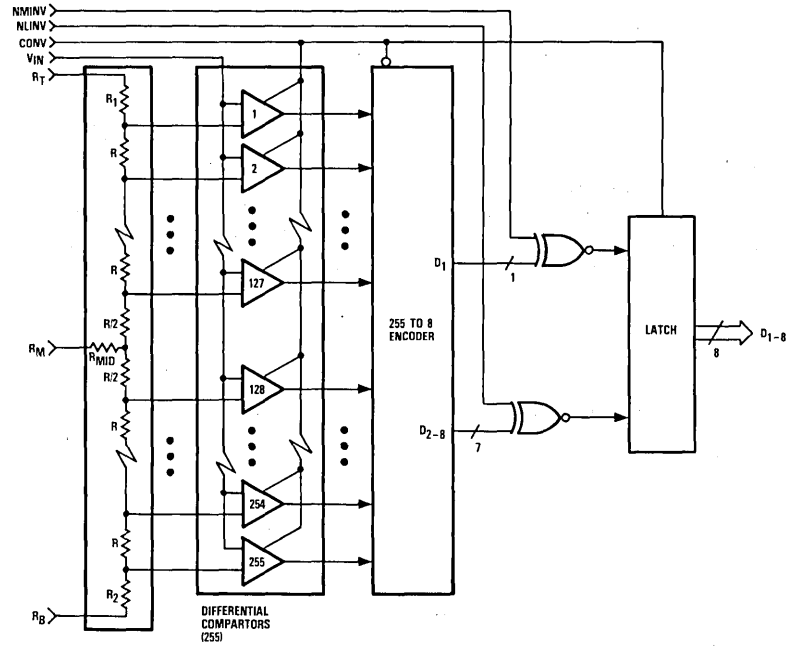
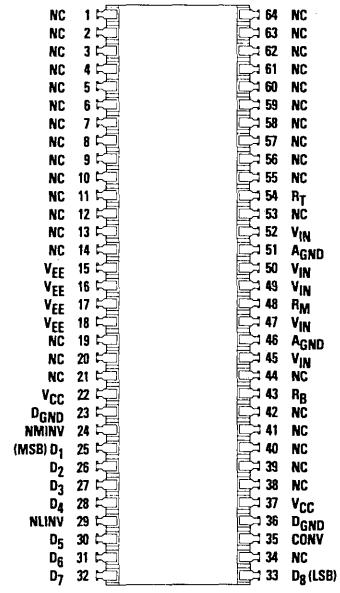
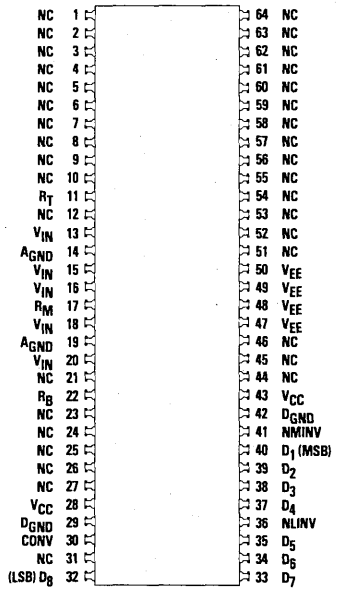
Functional Block Diagram



Pin Assignments

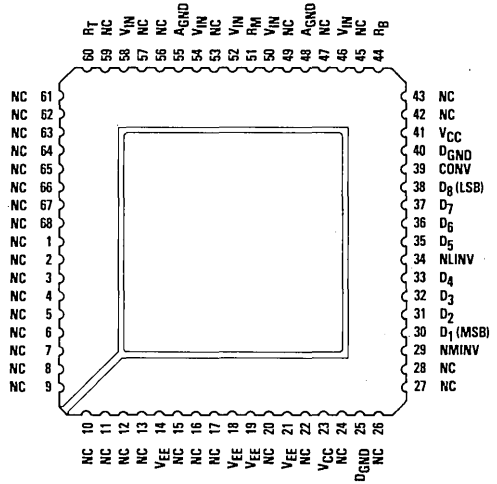


64 Lead DIP – J0 Package



64 Lead DIP – J1 Package

Pin Assignments



68 Contact Or Leaded Chip Carrier – C1, L1 Package

Functional Description

General Information

The TDC1007 has three major functional sections: a comparator array, encoding logic, and output data latches. The input voltage is compared with 255 separate reference voltage points tapped from the reference resistor chain. The 255 comparator outputs form a code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The "thermometer" code from the comparator array is encoded into an eight-bit binary word by the encoding logic section. Each of these eight results is sent through an exclusive-OR gate where they are inverted by use of the NMINV or NLINV inputs. This allows operation in binary, two's complement, or inverted data formats.

Power

The TDC1007 operates from two supply voltages, +5.0V and -6.0V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return path for I_{EE}, the current drawn from the -6.0V supply, is A_{GND}. All power and ground pins must be connected.

Name	Function	Value	C1, L1 Package	J1 Package	J0 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 23, 41	Pins 28, 43	Pins 22, 37
V_{EE}	Negative Supply Voltage	-6.0V	Pins 14, 18, 19, 21	Pins 47, 48, 49, 50	Pins 15, 16, 17, 18
D_{GND}	Digital Ground	0.0V	Pins 25, 40	Pins 29, 42	Pins 23, 36
A_{GND}	Analog Ground	0.0V	Pins 48, 55	Pins 14, 19	Pins 46, 51

Reference

The TDC1007 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RT} (the voltage applied to the pin at the top of the reference resistor chain), and V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) should be between +0.1V and −2.1V, with the difference between them less than 2.1V. V_{RT} should be more positive than V_{RB} within that range. In order to insure optimum operation of the TDC1007, these points should be driven by low-impedance sources capable of providing the necessary reference resistor chain current. The voltages on R_T and R_B may be varied dynamically up to 7MHz. Due to variations in reference current with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are varied dynamically (as in an AGC application) a low-impedance reference source is required.

Name	Function	Value	C1, L1 Package	J1 Package	J0 Package
R_T	Reference Resistor (Top)	0.0V	Pin 60	Pin 11	Pin 54
R_M	Reference Resistor (Middle)	−1.0V	Pin 51	Pin 17	Pin 48
R_B	Reference Resistor (Bottom)	−2.0V	Pin 44	Pin 22	Pin 43

Control

Two control inputs are provided on the TDC1007 for changing the format of the output data. When NMINV is tied to a logic "0", the most significant bit of the output data is inverted; when NLINV is tied to a logic "0", the seven least significant bits of the output are inverted. By using these controls, the output data format can be binary, inverted binary, two's complement, or inverted two's complement. Output data versus input voltage and control input state is illustrated in the Output Coding table on page 40.

Name	Function	Value	C1, L1 Package	J1 Package	J0 Package
NMINV	Not Most Significant Bit INVert	TTL	Pin 29	Pin 41	Pin 24
NLINV	Not Least Significant Bit INVert	TTL	Pin 34	Pin 36	Pin 29

Convert

The analog input to the TDC1007 is sampled (comparators are latched) approximately 10ns after the rising edge of the CONV Signal. This time delay is the sampling time offset (t_{STO}) and varies only by a few nanoseconds from device to device and as a function of temperature. The short-term uncertainty (jitter) in sampling time offset is approximately 30 picoseconds. The output data is encoded from the 255 comparators on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge of the CONV signal. Note that there are minimum pulse width (t_{PWH}, t_{PWL}) requirements on the waveshape of the CONV signal.

Name	Function	Value	C1, L1 Package	J1 Package	J0 Package
CONV	Convert	TTL	Pin 39	Pin 30	Pin 35

Analog Input

The input impedance of the TDC1007 varies with input signal level. As the signal varies, the comparator input transistors change from active to cut-off, causing the net input resistance and capacitance to change. To prevent this action from degrading the integrity or accuracy of the output data, it is desirable to drive the TDC1007 inputs from a low-impedance source (less than 25 Ohms). The input signal level should remain within the range of V_{EE} to +0.5V in order to prevent damage to the device. When the input is at a level between V_{RT} and V_{RB} reference voltages, the output data value will be directly proportional to the amplitude of the analog input signal. When the analog input is beyond the range of the reference voltage, the output data will be the appropriate full-scale value. Note that there are two components to the input bias current flowing into the V_{IN} pins. One component is constant for constant input voltage and is the sum of the bias currents of the subset of comparators that are active (I_{CB}). The other component is related to the action of the CONV signal on the comparator chain (I_{SB}). All analog input pins of the TDC1007 must be used in order to insure operation over the full input range.

Name	Function	Value	C1, L1 Package	J1 Package	J0 Package
V_{IN}	Analog Input Signal	0V to -2V	Pins 46, 50, 52, 54, 58	Pins 13, 15, 16, 18, 20	Pins 45, 47, 49, 50, 52

Outputs

The outputs of the TDC1007 are TTL compatible and capable of driving four low-power Schottky unit loads (54/74 LS). The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal, and the new data becomes valid after a maximum time of t_D.

Name	Function	Value	C1, L1 Package	J1 Package	J0 Package
D_1	MSB Output	TTL	Pin 30	Pin 40	Pin 25
D_2		TTL	Pin 31	Pin 39	Pin 26
D_3		TTL	Pin 32	Pin 38	Pin 27
D_4		TTL	Pin 33	Pin 37	Pin 28
D_5		TTL	Pin 35	Pin 35	Pin 30
D_6		TTL	Pin 36	Pin 34	Pin 31
D_7		TTL	Pin 37	Pin 33	Pin 32
D_8	LSB Output	TTL	Pin 38	Pin 32	Pin 33

No Connects

There are several pins labeled No Connect (NC), which have no connections to the chip. These pins may be left open.

Name	Function	Value	C1, L1 Package	J1 Package	J0 Package
NC	No Connect	Open	Pins 1-13, 15-17, 20, 22, 24, 26-28, 42, 43, 45, 47, 49, 53, 56, 57, 59, 61, 62-68	Pins 1-10, 12, 24-27, 31, 44-46, 51-64	Pins 1-14, 19-21, 34, 38-41, 53, 55-64

Figure 1. Timing Diagram

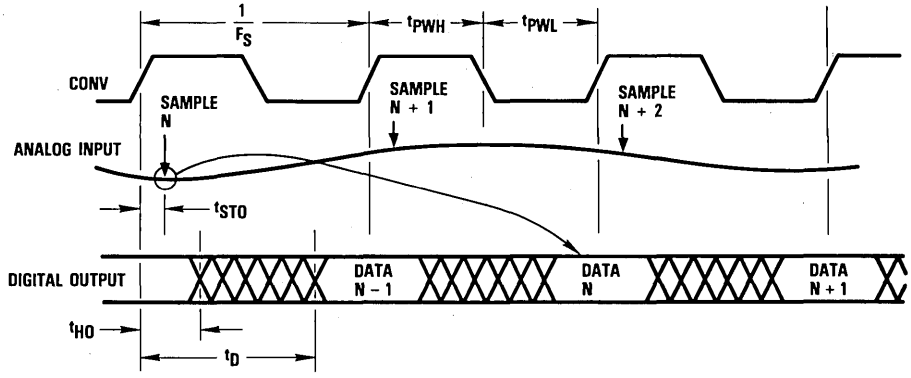
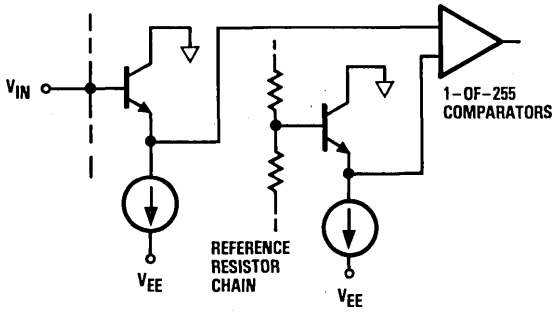
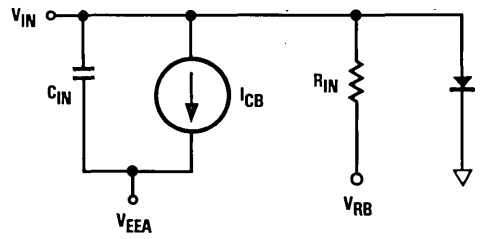


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Digital Input Equivalent Circuit

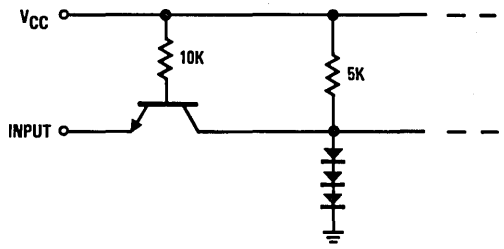
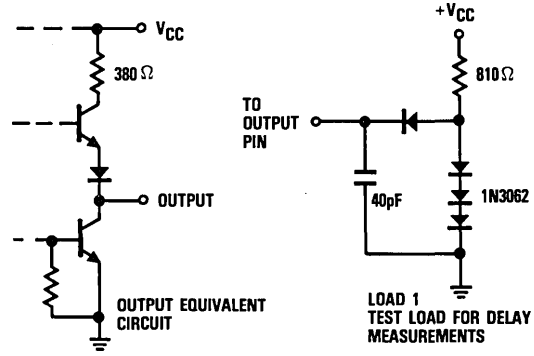


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−1.0 to +1.0V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}V
V_{RT} (measured to V_{RB})	+2.2 to −2.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to +5.5V [2]
Applied current, externally forced	−1.0 to +6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, ambient	−60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. *Current is specified as positive when flowing into the device.*

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (Measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (Measured to A_{GND})	−5.75	−6.0	−6.25	−5.75	−6.0	−6.25	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, Low	25			25			ns
t_{PWH}	CONV Pulse Width, High	15			15			ns
V_{IL}	Input Voltage, Logic Low			0.8			0.8	V
V_{IH}	Input Voltage, Logic High	2.0			2.0			V
I_{OL}	Output Current, Logic Low			4.0			4.0	mA
I_{OH}	Output Current, Logic High			−400			−400	μA
V_{RT}	Most Positive Reference Input [1]	−1.1	0.0	0.1	−1.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input [1]	−0.9	−2.0	−2.1	−0.9	−2.0	−2.1	V
V_{RT}−V_{RB}	Voltage Reference Differential	1.0	2.0	2.2	1.0	2.0	2.2	V
V_{IN}	Input Voltage	V_{RT}		V_{RB}	V_{RT}		V_{RB}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note:

1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = MAX, Static[1]		30		35	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, Static[1]					
		T_A = 0°C to 70°C		-400			mA
		T_A = 70°C		-350			mA
		T_C = -55°C to 125°C				-470	mA
		T_C = 125°C				-320	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM		35		40	mA
R_{REF}	Total Reference Resistance		57		50		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	5		5		kOhms
C_{IN}	Input Capacitance			250		250	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		400		500	μA
I_{SB}	Input Clock Synchronous Bias			200		200	μA
I_{IL}	Input Current, Logic Low	V_{CC} = MAX, V_I = 0.5V		-2.0		-2.0	mA
I_{IH}	Input Current, Logic High	V_{CC} = MAX, V_I = 2.4V		75		75	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic Low	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic High		2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, Output High, one pin to ground, one second duration.		-25		-25	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	20		20		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN	0	10	0	10	ns
t_D	Output Delay Time	V_{CC} = MIN, V_{EE} = MIN, Load 1	15	40	15	45	ns
t_{HO}	Output Hold Time	V_{CC} = MAX, V_{EE} = MAX, Load 1	10		10		ns

System performance characteristics within specified operating conditions

Parameter			Test Conditions	Temperature Range				Units
				Standard		Extended		
				Min	Max	Min	Max	
E_{LI}	Linearity Error	Integral, Independent	V_{RT}, V_{RB} - NOM		±0.3		±0.3	%
E_{LD}	Linearity Error	Differential	V_{RT}, V_{RB}		0.3		0.3	%
Q	Code Size		V_{RT}, V_{RB} - NOM	15	185	15	185	% Nominal
E_{OT}	Offset Error	Top	V_{IN} - V_{RT}		35		45	mV
E_{OB}	Offset Error	Bottom	V_{IN} - V_{RB}		-22		-24	mV
T_{CO}	Offset Error	Temperature Coefficient			±50		±50	µV/°C
BW	Bandwidth, Full Power Input			7		5		MHz
t_{TR}	Transient Response, Full Scale				20		20	ns
SNR	Signal-to-Noise Ratio		10MHz Bandwidth 20MSPS Conversion Rate					
		Peak Signal/RMS Noise	1.248MHz Input	53		52		dB
			2.438MHz Input	50		49		dB
		RMS Signal/RMS Noise	1.248MHz Input	44		43		dB
			2.438MHz Input	41		40		dB
NPR	Noise Power Ratio		DC to 8MHz White Noise Bandwidth 4 Sigma Loading 1.248MHz Slot 20MSPS Conversion Rate	36.5		36.5		dB
E_{AP}	Aperture Error				60		60	ps
DP	Differential Phase		NTSC @ 4x Color Subcarrier		1.0		1.0	Degree
DG	Differential Gain		NTSC @ 4x Color Subcarrier		1.7		1.7	%

Output Coding (Input range from 0.000 to −2.000V)

Input Voltage (−7.84 mV/Step)	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
	NMINV = 1 NLINV = 1	0 0	0 1	1 0
0.000	00000000	11111111	10000000	01111111
•	•	•	•	•
•	•	•	•	•
−0.0078	00000001	11111110	10000001	01111110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.9960	01111111	10000000	11111111	00000000
−1.0039	10000000	01111111	00000000	11111111
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−1.9921	11111110	00000001	01111110	10000001
•	•	•	•	•
•	•	•	•	•
−2.000	11111111	00000000	01111111	10000000

Calibration

To calibrate the TDC1007, the top of the reference resistor chain, R_T, is connected to analog ground. The reference voltage is then set up by adjusting the bottom of the resistor chain to −2.0V. When this technique is used, offset errors are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the A/D. These parasitic resistors are shown as R_1 and R_2 in the Functional Block Diagram. The offset voltage error is the result of the resistor chain current flowing through the parasitic resistance. These errors can be compensated for by applying an equal offset to the analog input signal or by adjusting the voltages on R_T and R_B.

The effect of the offset error at the bottom of the resistor chain manifests itself in the form of a slight gain error which can be compensated for by varying the voltage applied to R_B. This voltage will necessarily be more negative than the desired reference level of −2.0V. The actual operating range of the A/D converter will be:

$$(V_{AGND} - (I_{REF} \times R1)) \text{ to } (V_{RB} + (I_{REF} \times R2)).$$

However, if both ends of the resistor chain are driven by transistor-buffered operational amplifiers, the voltages on R_T and R_B could then be adjusted to remove the effect of the parasitic resistances and therefore eliminate the need to apply a compensating offset voltage to the analog input signal. Here the operating range of the A/D will be:

$$(V_{RT} - (I_{REF} \times R1)) \text{ to } (V_{RB} + (I_{REF} \times R2)).$$

Since both V_{RT} and V_{RB} are adjustable, the offset voltage error effect can be cancelled and the A/D operated with gain and offset errors removed.

The TDC1007 provides access to the mid-point of the reference resistor chain, R_M. This point can be sensed by external circuitry for temperature compensation or gain tracking functions in the system. It can also be driven in the manner shown in Figure 6 for fine linearity correction.

Typical Application

Figure 5 shows a typical interface circuit for a TDC1007, an input buffer amplifier, and the reference voltage source. The reference voltage is supplied by an inverting amplifier that has been buffered with a PNP transistor. The transistor sinks the current flowing through the reference resistor chain and keeps the driving impedance at the bottom end of the resistor chain low. The gain of the overall circuit is adjusted by varying the input voltage to the operational amplifier.

The input amplifier is a bipolar wideband operational amplifier followed by an NPN transistor buffer. The transistor drives the input capacitance of the A/D converter and keeps the overall circuit frequency stable. The offset error is compensated by varying the current into the summing junction of the op-amp. Note that all five V_{IN} points are connected together and the buffer amplifier feedback loop is closed at that point. The buffer amplifier has a gain of two, raising the 1V p-p video input signal to 2V p-p at the input to the A/D converter. The A/D converter operates with a 2V full-scale.

Figure 5. Typical Interface Circuit

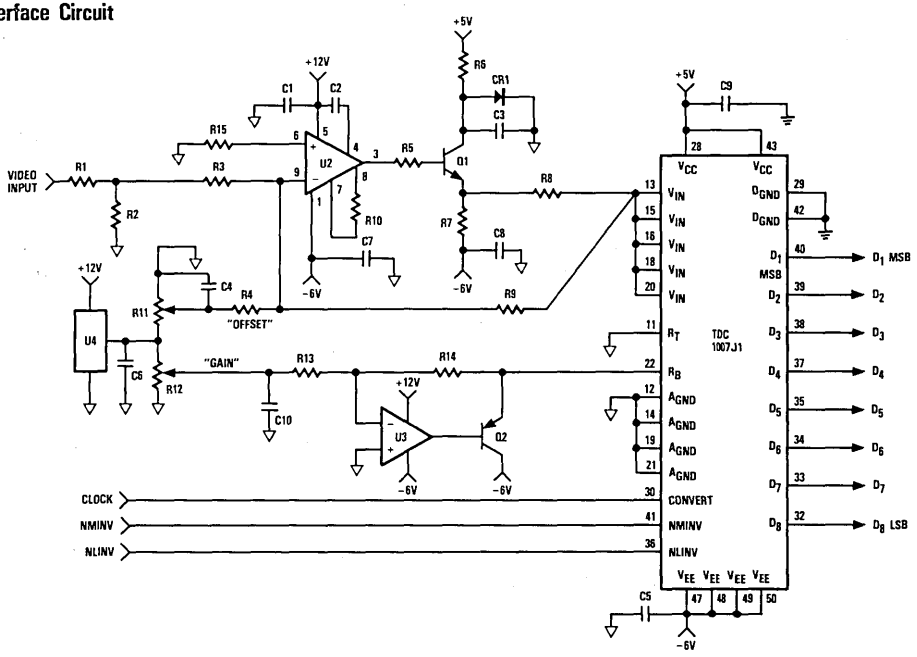
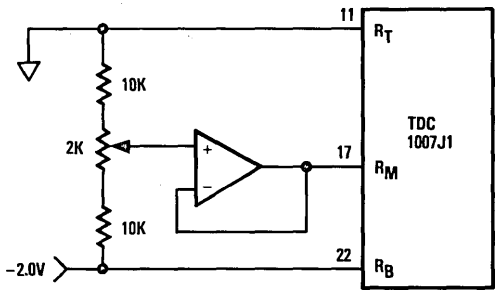


Figure 6. Method For Driving Mid-Point Of Resistor Chain



Parts List

Resistors

R1	†	1/4W	
R2	†	1/4W	
R3	1K	1/4W	5%
R4	4.3K	1/4W	5%
R5	10	1/4W	5%
R6	56	1/2W	5%
R7	240	2W	5%
R8	6.8	1/2W	5%
R9	2K	1/2W	5%
R10	*	1/4W	5%
R11	2K	1/4W	10-turn
R12	2K	1/4W	10-turn
R13	1.3K	1/4W	5%
R14	2.2K	1/4W	5%
R15	680	1/4W	5%

Capacitors

C1	0.1	50V
C2	*	50V
C3	0.1	50V
C4	0.1	50V
C5	0.1	50V
C6	1.0	15V
C7	0.1	50V
C8	0.1	50V
C9	0.1	50V
C10	0.1	50V

Integrated Circuits

U1	TDC1007J1
U2	Plessey SL541C
U3	μA741
U4	MC14030

Diodes

CR1	1N4001

Transistors

Q1	2N5836
Q2	2N2907

† Indicates input terminator/divider

* Indicates amplifier compensation

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1007C1F	EXT-T_C = -55°C to 125°C	Commercial	68 Contact Chip Carrier	1007C1F
TDC1007C1A	EXT-T_C = -55°C to 125°C	MIL-STD-883	68 Contact Chip Carrier	1007C1A
TDC1007C1N	EXT-T_C = -55°C to 125°C	Commercial With Burn-In	68 Contact Chip Carrier	1007C1N
TDC1007J1C	STD-T_A = 0°C to 70°C	Commercial	64 Lead DIP	1007J1C
TDC1007J1G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	1007J1G
TDC1007J1F	EXT-T_C = -55°C to 125°C	Commercial	64 Lead DIP	1007J1F
TDC1007J1A	EXT-T_C = -55°C to 125°C	MIL-STD-883	64 Lead DIP	1007J1A
TDC1007J1N	EXT-T_C = -55°C to 125°C	Commercial With Burn-In	64 Lead DIP	1007J1N
TDC1007J0C	STD-T_A = 0°C to 70°C	Commercial	64 Lead DIP	1007J0C
TDC1007J0G	STD-T_A = 0°C to 70°C	Commercial With Burn-In	64 Lead DIP	1007J0G
TDC1007J0F	EXT-T_C = -55°C to 125°C	Commercial	64 Lead DIP	1007J0F
TDC1007J0A	EXT-T_C = -55°C to 125°C	MIL-STD-883	64 Lead DIP	1007J0A
TDC1007J0N	EXT-T_C = -55°C to 125°C	Commercial With Burn-In	64 Lead DIP	1007J0N
TDC1007L1F	EXT-T_C = -55°C to 125°C	Commercial	68 Leaded Chip Carrier	1007L1F
TDC1007L1A	EXT-T_C = -55°C to 125°C	MIL-STD-883	68 Leaded Chip Carrier	1007L1A
TDC1007L1N	EXT-T_C = -55°C to 125°C	Commercial With Burn-In	68 Leaded Chip Carrier	1007L1N