TEK INSTRUCTION MANUAL

PART NO. 070-3434-00
PRODUCT GROUP 26

# 7L14 SPECTRUM ANALYZER

## OPTIONS INCLUDED

*Please Check for CHANGE INFORMATION at the Rear of This Manual*

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Tektronix®
COMMITTED TO EXCELLENCE

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**WARNING**

*THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.*

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# OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

### Terms In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

### Terms As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

### Symbols In This Manual

This symbol indicates where applicable cautionary or other information is to be found.

### Symbols As Marked on Equipment

DANGER — High voltage.

Protective ground (earth) terminal.

ATTENTION — refer to manual.

### Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

### Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

### Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

### Do Not Remove Covers or Panels

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

# SERVICE SAFETY SUMMARY

## *FOR QUALIFIED SERVICE PERSONNEL ONLY*

*Refer also to the preceding Operators Safety Summary.*

### Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

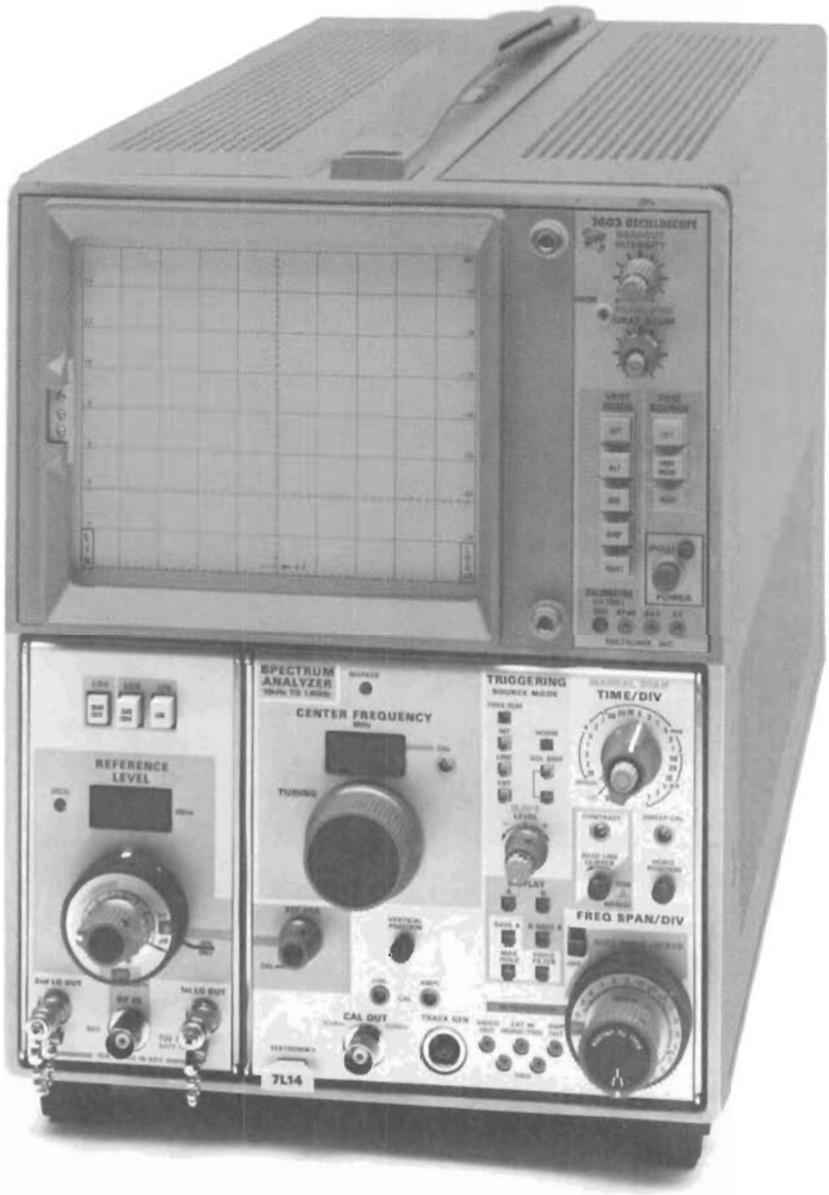
### Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

### Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.




3434-1

7L14 Spectrum Analyzer

# GENERAL INFORMATION AND SPECIFICATION

## GENERAL INFORMATION

### Product Description

The 7L14 Spectrum Analyzer displays information of signals within the frequency span of 10 kHz to 1.8 GHz. It contains horizontal sweep and timing circuits for frequency and time domain displays, and provides means for using an external sweep source to slave the 7L14 to some external device, such as a recorder.

The 7L14's digital storage capability permits flicker-free displays at slow sweep speeds. In the storage mode, the vertical display can be divided with a positionable threshold level: above this level video peaks are detected, below it video peaks are averaged. This threshold level is indicated by a horizontal cursor on the display.

The 7L14 requires three plug-in widths in any of the TEKTRONIX 7000 series mainframe oscilloscopes.

### Standards, Documents, and References Used

Terminology used in the manual is in accordance with industry practice. Abbreviations are in accordance with ANSI Y1.1-1972, with exceptions and additions explained in parentheses after the abbreviation. Graphic symbology is based on ANSI Y32.2-1975. Logic symbology is based on ANSI Y32.14-1973 and the manufacturer's data books or sheets. A copy of ANSI standards may be obtained from the Institute of Electrical and Electronic Engineers, 345 47th Street, New York, NY 10017.

### Change and History Information

Change information that involves manual corrections and/or additional data is located at the back of the manual in the CHANGE INFORMATION section. History information with the updated data is integrated into the text or diagrams when a page or diagram is updated.

### Accessories

For a complete listing of the Standard and Recommended Accessories for the 7L14, refer to the Mechanical Parts List in the back of this manual.

## SPECIFICATION

The following list of instrument characteristics and features apply to the 7L14 Spectrum Analyzer after a 20 minute warmup, except as noted.

The Performance Requirement column describes the limits of the characteristic, and the Supplemental column describes features and typical values or information that may be useful to the user. Procedures to verify performance requirements are provided in the Calibration section of the Service Instructions. The Performance Check procedures require sophisticated equipment as well as technical expertise to perform.

The Operator's Section contains a procedure that checks all functions of the 7L14. This check is recommended for incoming inspections to verify that the instrument is performing properly.

**Table 1-1**

**ELECTRICAL CHARACTERISTICS**

| Characteristic | Performance Requirement | Supplemental Information |
|---|---|---|
| **Frequency Related** | | |
| Center Frequency | | |
| Range | 10 kHz to 1.8 GHZ | |
| Readout Resolution | Within 1 MHz | |
| Readout Accuracy | ±(5 MHz +20% of Frequency Span/Div) | |
| Frequency Span | 200 Hz/Div to 100 MHz/Div | In calibrated steps in a 1-2-5 sequence |
| Accuracy | Within 5% of the span selected | |
| Linearity | Within 5% of the span selected | |
| Max Span | | Provides 1.8 GHz of span |
| 0 Span | | Provides fixed frequency operation for time domain display |
| Resolution Bandwidth Range | | 30 Hz to 3 MHz, in decade steps |
| Accuracy (6 dB down) | Within ±20% of the resolution selected | |
| Shape Factor (60/6 dB) | 4:1 or less for 3 MHz to 0.3 kHz; 12:1 or less for 30 Hz resolution | |
| Signal level change between any two bandwidths | ±0.5 dB at room temperature[a]<br>±2.0 dB max over temperature | |
| Incidental Fm'ing | ≤13 Hz (P-P) when phaselocked<br>≤10 kHz (P-P) for 20 ms when not phaselocked | |
| Stability, at a fixed frequency and temperature after a two hour warmup and stable ambient temperature. | Within 2 kHz/Hr phaselocked<br>Within 75 kHz/Hr not phaselocked | A restabilization time of 10 minutes per GHz of 1st LO frequency change must be allowed if the center frequency is retuned. |

[a] **0 RF attenuation, −30 dBm reference level**

Table 1-1 (cont.)

| Characteristic | Performance Requirement | Supplemental Information |
|---|---|---|
| **Amplitude Related** | | |
| Display Modes<br>LOG 10 dB/Div | | Provides 70 dB dynamic range |
| Accuracy | Within 0.15 dB/dB to 2 dB max over 70 dB dynamic range | |
| LOG 2 dB/Div | | Provides 14 dB dynamic range |
| Accuracy | Within ±0.4 dB/2 dB to 1.0 dB max over 14 dB dynamic range | |
| LIN | Within 10% over 8 divisions | |
| Deviation Between Display Modes[b] | ≤2 dB from 2 dB/Div to 10 dB/Div<br>≤0.5 Divisions from 2 dB/Div to LIN | |
| Reference Level<br>Below 100 KHz | | +30 dBm to −50 dBm, as the center frequency approaches 10 KHz |
| Above 100 KHz | | +30 dBm to −100 dBm in 10 dB calibrated steps |
| Display Flatness | ±1.5 dB, with respect to 50 MHz, over any selected frequency span. | |
| Sensitivity<br>At 50 MHz Resolution Bandwidth | Equivalent (average) Input Noise Level (worst case) | Applicable from 100 KHz to 1.8 GHz |
| 30 Hz<br>300 Hz<br>3 kHz<br>30 kHz<br>0.3 MHz<br>3 MHz | −130 dBm<br>−120 dBm<br>−110 dBm<br>−100 dBm<br>− 90 dBm<br>− 80 dBm | |
| Spurious Responses<br>Residual | ≤−100 dBm (referenced to the 1st mixer input) | |
| Second order inter-modulation products | 100 kHz −1.8 GHz: down 70 dB or more from two −40 dBm signals, within any frequency span | |
| Third order inter-modulation products | 100 kHz −1.8 GHz: down 70 dB or more from two −30 dBm signals, within any frequency span | |
| RF Attenuator | | Calibrated in 10 dB steps |
| Accuracy | ±0.25 dB or 1.2% of dB reading; whichever is greater | |

[b]For full screen signal.

Table 1-1 (cont.)

| Characteristic | Performance Requirement | Supplemental Information |
|---|---|---|
| **Amplitude Related** | | |
| IF Gain | | |
| Range | | 70 dB (80 dB when operating in 30 Hz resolution bandwidth) |
| Step Accuracy | ±1 dB per 10 dB step to ±2 dB max over entire range[c] | |
| **General Characteristics** | | |
| Noise Sidebands | 70 dB down; 25X resolution bandwidth | See Fig. 1-1 |
| Sweep | | Triggered, manual, external |
| Sweep Time | | 10 s/Div to 1 μs/Div in a 1-2-5 sequence |
| Accuracy | ±6% of selected Time/Div | |
| Triggering Modes | | INTERNAL, EXTERNAL, EXT in HORIZ/TRIG and LINE |
| Sensitivity | ≤0.5 division of internal signal (P-P) and/or ≤0.5 volt (P-P) of external signal | |
| Power requirements from the mainframe | | |
| To +50 V | | Approx 35 mA |
| −50 V | | Approx 65 mA |
| +15 V | | Approx 875 mA |
| −15 V | | Approx 900 mA |
| +5 V | | Approx 1080 mA |
| +5 V Lights | | Approx 130 mA |
| Total Lights | | 38 Watts typical |
| **Input Signal Characteristics** | | |
| RF Input | | |
| Maximum input power level | | +30 dBm |
| Maximum input power level to the RF attenuator ≥10 dB | | 1 watt average (including DC), 100 watts peak simultaneously |
| Input Impedance | | 50 ohm; vswr 1.35 max with 10 db of RF attenuation |

[c]Gain and attenuator not off-setting each other.

Table 1-1 (cont.)

| Characteristic | Performance Requirement | Supplemental Information |
|---|---|---|
| **Input Signal Characteristics (cont)** | | |
| External Horizontal/Trigger Input Connector | | |
| Input Voltage Range | | Typically 0 V to 10 V for 10 division sweep<br>Typically 0.5 V (P-P) to trigger the sweep circuits. 40 V peak max |
| **Output Signal Characteristics** | | |
| CAL OUT | −30 dBm, ±0.3 dB at 50 MHz, ±0.01% | 50 MHz comb markers are provided for frequency and span calibration |
| 1st LO OUT and 2nd LO OUT | | Provide access to the output of the respective local oscillators (1st LO +5 dBm min., 2nd LO −10 dBm min. +10 dBm max. These ports must be terminated in 50 ohms. |
| SWP OUT | | 0 to −5 V |
| Video Output | | Typically 0.5 V of video signal per display division. Output impedance approx. 10 K ohm. Markers can be inserted upon the stored or non-stored trace by providing the VIDEO OUT port with a negative-going signal. Max. input level −10 V peak. |

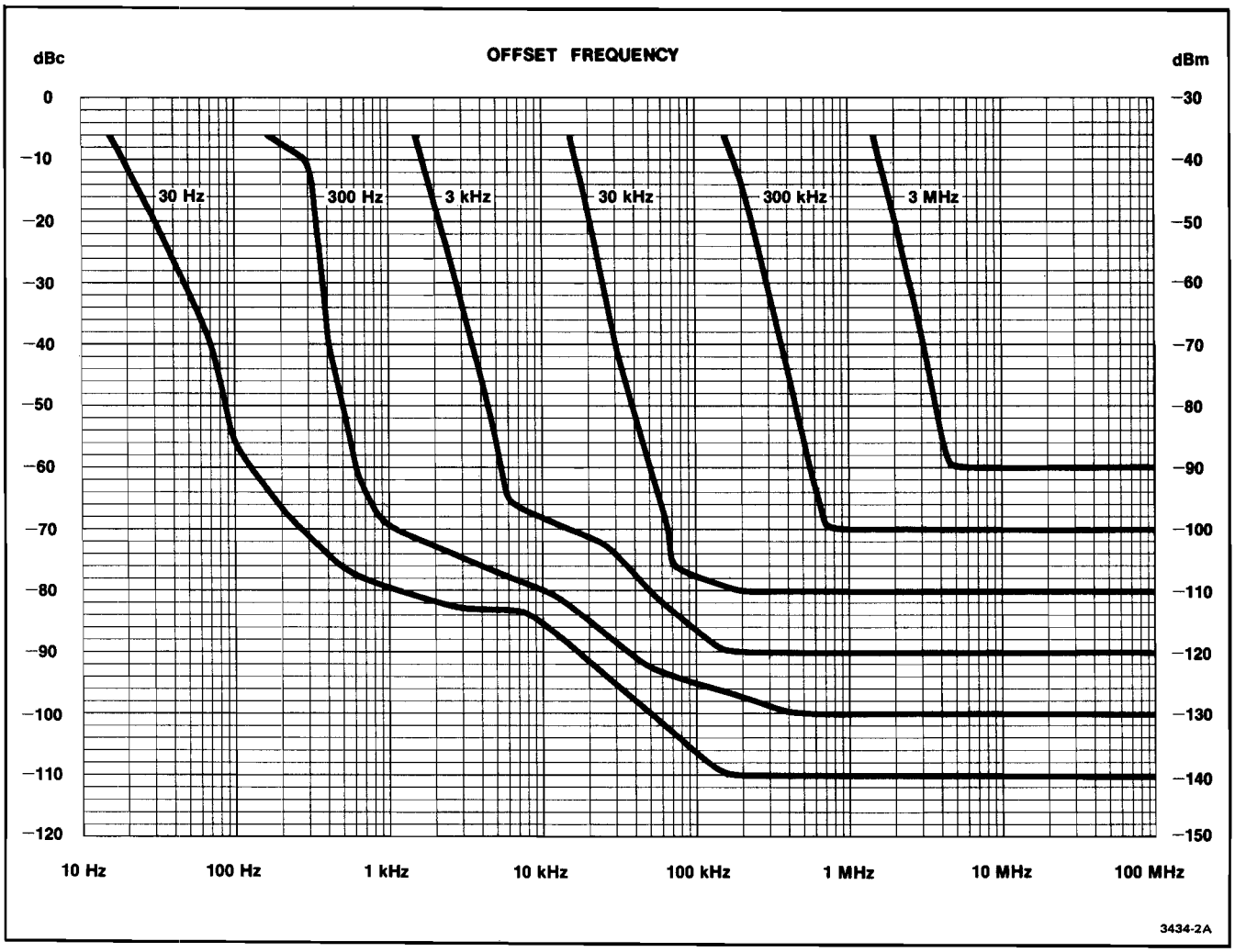



Fig. 1-1. Typical filter shape, phase noise sidebands and sensitivity for the 7L14.

**Table 1-2**

**ENVIRONMENTAL CHARACTERISTICS**

| Characteristic | Description | |
|---|---|---|
| Temperature and Relative Humidity | | |
| Operating | +10°C to +40°C (75% humidity) | |
| Non-operating | −55°C to +75°C (75% humidity) | |
| Vibration | | |
| Operating | Resonant searches along all three axes at 0.015 inch, frequency varied from 10-55 Hz, 15 minutes. All major resonances must be minimum per axis plus dwell at resonant frequency or 55 Hz for 10 minutes minimum per axis. Instrument secured to vibration platform during test. Total vibration time about 75 minutes. | |
| Shock | | |
| Operating | Three shocks of 30g, one-half sine, 11 ms duration, each direction along each major axis. Guillotine-type shocks. Total of 18 shocks. | |
| Electromagnetic Interference (EMI) | **Test Method** | **Remarks** |
| Conducted Emissions | CE01 | 60 Hz to 20 KHz |
| | CE03<br>20 KHz to 50 MHz power leads | Full limits |
| Conducted Susceptibility | CS01<br>30 Hz to 50 KHz power leads | Full limits |
| | CS02<br>50 KHz to 400 KHz power leads | Full limits |
| | CS06 spike power leads | Full limits |
| Radiated Emissions | RE01<br>30 Hz to 30 KHz magnetic field | Full limit |
| | RE02<br>14 ± 3 KHz to 1 GHz | Full limits |
| Radiated Susceptibility | RS01<br>30 Hz to 30 KHz magnetic field | Full limit |
| | RS03 up to 1 GHz | Except 100 to 110 MHz |

**Table 1-3**

**PHYSICAL CHARACTERISTICS**

| Characteristic | Performance Requirement | Supplemental Information |
|---|---|---|
| Weight | | 16 lbs. (7.2 kg) |
| Length | | 14.75 inches (375 mm) |
| Height | | 5.00 inches (120 mm) |
| Width | | 8.15 inches (200.5 mm) |

# OPERATING INSTRUCTIONS

## Unpacking and Initial Inspection

Before unpacking the 7L14 from its shipping container or carton, inspect for signs of external damage. If the carton is damaged, notify the carrier, as well as TEKTRONIX, Inc. The shipping carton contains the basic instrument and its standard accessories. Optional accessories are shipped in separate containers. Refer to the Accessories listing in the Mechanical Parts List for a complete listing.

If the contents of the shipping container are incomplete, if there is mechanical damage or defect, or if the instrument does not meet operational check requirements, contact your local Tektronix Field Office or representative.

The instrument has been inspected both mechanically and electrically before shipment. It should be free of mechanical damage and meet or exceed all electrical specifications. Procedures to check functional or operational performance are in the Operational Check Procedures. This check should satisfy the requirements for most receiving or incoming inspections. The electrical performance check procedure is part of the Service Instructions.

## Installation

Installation of the 7L14 into the 7000 series mainframe consists of sliding the unit into the mainframe compartment.

**CAUTION**

*Power to the mainframe should be OFF when installing the 7L14.*

Ensure that the 7L14 is securely latched into place.

*NOTE*

*A safety latch is used to reduce the possibility of the instrument slipping out of the mainframe.*

For information on power source and power requirements, and environmental considerations, refer to the manual supplied with the 7000 series mainframe oscilloscope.

## Repackaging for Shipment

When the 7L14 is to be shipped to a Tektronix Service Center for service or repair, attach a tag showing: owner and address, name of individual at your firm that can be contacted, complete serial number, and a description of the service required. If the original packaging is unfit for use or not available, repackage the equipment as follows:

1. Obtain a carton of corrugated cardboard having inside dimensions that are at least six inches more than the equipment dimensions, to allow for cushioning. Carton test strength should be 275 lbs (102.5 kg).

2. Surround the 7L14 with polyethylene sheeting to protect the finish.

3. Cushion the equipment on all sides with packing material or urethane foam between the carton and the sides of the equipment.

4. Seal with shipping tape or industrial stapler.

**CAUTION**

*A safety latch must be released before the 7L14 can be pulled from the oscilloscope compartment. The unit will pull out part way when the front panel release (see Fig. 2-1) is pulled, then the spring safety latch must be pushed up to free the unit completely. This safety latch is located underneath the right rail, near the front corner.*

**CAUTION**

*Do not ship the 7L14 when it is installed in the mainframe, unless it is bolted into the mainframe. A spectrum analyzer securing kit is available from Tektronix, Inc. for the following instruments: 7313/R, 7603/R, 7613/R, 7623/R, 7623A/R, and 7633/R. Order by Tektronix part number 016-0637-00.*

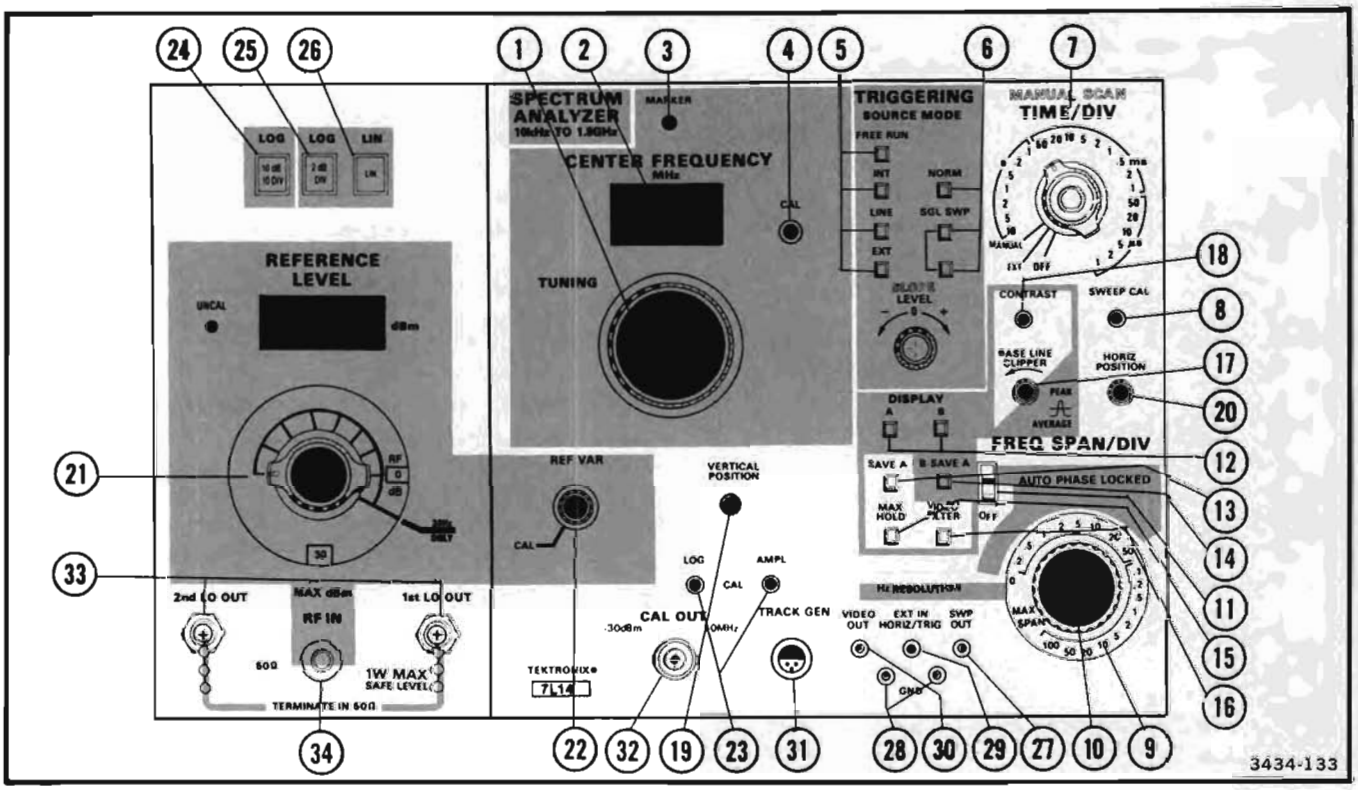



**Fig. 2-1. Front-panel controls.**

# CONTROLS, INDICATORS, AND CONNECTORS

The following describes the function of the controls, indicators, and connectors on the front panel of the 7L14. Figure 2-1 illustrates their location.

(1) **TUNING.** The center frequency is tuned with this one-speed control. The tuning range is decreased to +50 kHz when the FREQ SPAN/DIV is 50 kHz or less and the AUTO PHASE LOCKED switch is on.

(2) **CENTER FREQUENCY.** The center frequency or marker frequency is indicated by the LED readout.

(3) **MARKER.** This indicator lights when the FREQ SPAN/DIV is at the MAX SPAN position. A notch on the baseline of the display indicates the center portion of the span that will be displayed when the FREQ SPAN/DIV is reduced.

(4) **CAL.** The frequency readout can be calibrated to center frequency by adjusting the TUNING control for the correct reading.

(5) **TRIGGERING SOURCE.** One of four triggering sources can be selected.

**FREE RUN.** The sweep is free running without regard to trigger signals.

**INT.** Uses the displayed signal as a trigger source. The signal is ac coupled with an approximate frequency range from 15 Hz to 1 MHz.

**LINE.** The trigger signal source is a sample of the ac power line. Line signals are dc coupled to the triggering circuits.

**EXT.** Selects the signal that is applied to the EXT IN/HORIZ TRIG connector. External signals are dc coupled to the triggering circuits. Maximum signal input to the external input connector should not exceed 40 V (dc + ac peak) for triggering. Input impedance for the external input is about 30 k ohm.

(6) **TRIGGERING MODE.** One of two triggering modes can be selected.

**NORM.** The sweep will automatically recur at the end of holdoff time, if a trigger signal is absent. This feature provides a baseline on the display. In this mode triggering occurs at the slope and level selected by the SLOPE/LEVEL controls unless the triggering signal is below the required amplitude, or beyond the frequency limits of the circuit. Minimum signal amplitude for internal triggering is 0.5 division of signal for external triggering.

In the **SGL SWP** mode, the sweep is triggered by pushing the adjoining button. This button lights during sweep time and serves as an indicator to determine camera shutter time when photographing slow-scan time displays. Minimum signal amplitude for triggering is 0.5 division of signal and 0.5 V of external signal.

(7) **TIME/DIV and MANUAL SCAN.** Three sweep modes and an OFF state are provided.

TIME/DIV is calibrated in a 1, 2, 5 sequence from 10 S/Div to 1 μs/Div. This control selects the sweep rates and the MANUAL, EXT and OFF modes.

In the OFF position, the crt beam is horizontally centered and the analyzer becomes a tuned receiver to the frequency indicated by the readout.

The EXT position connects any signal applied to the EXT IN/HORIZ TRIG connector to the horizontal deflection circuits of the 7L14. External sweep voltage (0 V to 10 V) signal can be used to slave the 7L14 to an external device, such as a recorder.

The MANUAL position connects the sweep circuits of the 7L14 to the MANUAL SCAN control, so the crt beam deflection can be manually controlled.

(8) **SWEEP CAL.** This adjustment compensates for differences in deflection sensitivities between oscilloscopes.

(9) **FREQ SPAN/DIV.** This control sets the horizontal frequency calibration on the crt. The calibrated range of the selector is 100 MHz/Div to 200 Hz/Div in a 1, 2, 5 sequence. A MAX span position provides approximately 1.8 GHz of spectrum and a 0 Hz position converts the analyzer to a fixed tuned receiver for time-domain displays. Time analysis of the signal characteristics, within the bandwidth capabilities selected with the RESOLUTION control, can then be performed. In this case, Time/Div is read out on the crt instead of Span/Div.

(10) **RESOLUTION.** This control allows the operator to analyze discrete frequency components within a frequency span. The calibrated range (within 20%) is 30 Hz to 3 MHz in decade steps. The RESOLUTION control can be coupled to the FREQ SPAN/DIV control when the knobs align with indicating marks. A concentric sleeve labeled PULL TO UNLOCK will uncouple the two selectors when it is pulled out and allow independent settings of each control.

(11) **AUTO PHASE LOCKED.** This switch is used to disable the phase lock for some applications, such as tuning the analyzer more than 1 MHz when the instrument is used as a tuned receiver (0 span).

(12) **DISPLAY A, DISPLAY B.** Without either of the pushbuttons activated, the 7L14 display is stored, but not displayed. When either or both these pushbuttons are selected, the contents of memory A and/or memory B are displayed. With SAVE A memory off, all memory locations are displayed and updated continuously. Data in A memory is interlaced with data from B memory.

(13) **SAVE A.** When activated, this mode holds data in A memory and inhibits further updating. With SAVE A and VIEW A active, data in A memory is displayed but not updated, serving as a reference to compare contents of B memory.

(14) **B-SAVE A.** When this button is activated, the contents of memory B minus the contents saved in memory A are displayed. This permits a comparison between two displays. The SAVE A function is also in effect.

(15) **MAX HOLD.** When activated, the digital storage memory retains the maximum signal amplitude at each memory location. This permits visual monitoring of signal frequency and amplitude at each memory location over an indefinite period of time. This feature is used to measure drift, stability, and record peak amplitudes.

(16) **VIDEO FILTER.** When the VIDEO FILTER button is pushed, one of three filters (10 Hz, 300 Hz or 30 kHz) is selected depending on the Resolution Bandwidth setting. The bandwidth of the filter selected is displayed on the crt. Video filters restrict the video bandwidth and reduce high frequency components for display noise averaging.

(17) **BASELINE CLIPPER-PEAK AVERAGE.** When the digital storage is off, this control operates as a baseline clipper (i.e. as the control is rotated counterclockwise, more of the vertical display is progressively

clipped, or blanked). When the digital storage is on, the control sets the level at which the vertical display is either peak detected or averaged. Video signals above the level set by the control (shown by the horizontal cursor) are peak-detected and stored; video signals below the cursor are averaged and stored.

(18) **CONTRAST.** When the digital storage is off, this control adjusts the brightness ratio between the blanked and unblanked portion of the display. Overall display intensity is set by the oscilloscope Intensity control. When digital storage is on, this control adjusts the intensity of the cursor. This feature is especially helpful for use with a digital processing oscilloscope or a 7854 oscilloscope.

(19) **VERTICAL POSITION.** This control positions the display vertically.

(20) **HORIZONTAL POSITION.** This control positions the display horizontally.

(21) **REFERENCE LEVEL.** (Reference and IF Gain). These concentric controls select input attenuation to the input mixer, and the IF gain. The readout windows indicate REFERENCE LEVEL in dBm, of the full scale display, MAXimum signal input level (in dBm) for linear operation, and the input RF attenuation (from 0 to 60 dB).

The RF attenuation is in series with the input signal path to the input mixer, therefore its settings affect the maximum input signal level to the 7L14. With 0 dB attenuation, maximum input signal level for linear operation is −30 dBm. Changing the RF Attenuator to 60 dB increases the maximum input signal level to +30 dBm.

The IF gain selector has a range of 80 dB in 10 dB steps. The combination of RF attenuator settings and IF gain settings establishes the REFERENCE LEVEL; therefore, both controls function as REFERENCE LEVEL selectors. The maximum sensitivity of the display will not exceed −130 dBm. Since the dynamic window is 70 dB in the 10 dB/Div display mode, the REFERENCE LEVEL readout is valid to −60 dBm. With the RF attenuator at 0 dB and the IF gain fully ccw, the REFERENCE LEVEL is −30 dBm. Increasing the IF gain 30 dB changes the REFERENCE LEVEL to −60 dBm, which is the limit for a calibrated reference level in the 10 dB/Div mode. The blue tint that borders the 10 dB/Div switch and four positions of the gain selector correlates REFERENCE LEVEL readout to the gain settings applicable in the 10 dB/Div mode.

When the gain selector is rotated beyond the blue tint sector, REFERENCE LEVEL readings do not change because the gain is electrically locked out. In the 2 dB/Div mode, the full 80 dB range of the gain selector is usable. Seventy dB of the range is available only when the RESOLUTION is set at 30 Hz. With the RF attenuator at 0 dB, switching the gain produced up to an accurate −100 dBm reference level. When the RESOLUTION is 30 Hz, the fully cw gain position permits a −100 dBm reference level for a calibrated −124 dBm.

(22) **REF VAR.** This control is a reference vernier provided with a 10 dB control range. The display amplitude is uncalibrated when this control is out of detent.

(23) **LOG AND AMPL CAL.** These adjustments calibrate the dynamic range of the display. LOG calibrates the logarithmic gain in db/div, AMPL calibrates the reference level of the top graticule line at the top of the screen.

(24) **LOG 10 dB/DIV.** Selecting this pushbutton gives a calibrated display with a dynamic range of 70 dB (to the 7th graticule line from the reference) at 10 dB/Div. The bottom graticule division is not calibrated.

(25) **LOG 2 dB/DIV.** When this pushbutton is pressed, the dynamic range of the display is a calibrated 14 dB at 2 dB/div.

(26) **LIN.** This selects a linear display. The LIN graticule calibration permits relative signal level measurements as follows: adjust the level of one signal to the 1.0 line (when used with a spectrum analyzer graticule) with the gain or RF attenuation. Read the level of the other signals as a percentage of this reference.

(27) **SWP OUT.** This connector supplies a negative-going ramp of about 0 V to −5 V and a source impedance of about 1 k ohm.

(28) **GND.** These two pin connectors are connected to signal ground in the instrument. DO NOT use these pins for safety earth connections.

(29) **EXT IN HORIZ/TRIG.** The function of the dual-purpose input depends on the settings of the TIME/DIV control. When the TIME/DIV control is set to any sweep position (or AUTO), a positive applied signal will initiate the sweep. When the TIME/DIV control is set to EXT IN, an applied voltage will position the beam horizontally. To sweep the full span, a voltage of 0 V to +10 V, ±1 V is required (sensitivity is about 1 V/div). Zero volts corresponds to the right edge.

(30) **VIDEO OUT.** This connector provides a buffered video output to drive an external device such as a chart recorder. Output level is about 500 mV per displayed division. The source impedance is about 10 k ohm.

(31) **TRACK GEN.** A source of control signals for a tracking generator. Pin 5 of the connector is the source of a +10 V to −10 V sweep ramp, with +10 V representing the left edge of the display and −10 V the right edge of the display.

(32) **CAL OUT.** Provides an accurate −30 dBm, 50 MHz signal source. This signal provides an absolute reference on the display to calibrate the REFERENCE LEVEL and check dBm readings. Harmonics of the 50 MHz fundamental provide a comb of markers across the frequency span for accurate frequency and span measurements.

(33) **1ST and 2ND LO OUT.** These connectors provide access to the output of the respective local oscillators. They must be terminated into 50 ohm. Keep the termination plugs on the output jacks unless these ports are connected to an external device such as a tracking generator.

(34) **RF IN.** A 50 ohm input connector for applying the input signal to the 7L14. REFERENCE LEVEL readout refers to the signal level at this connector. Any signals riding on some dc potential must be applied through a dc block. Refer to the *General Operating Information* with regard to signal applications.

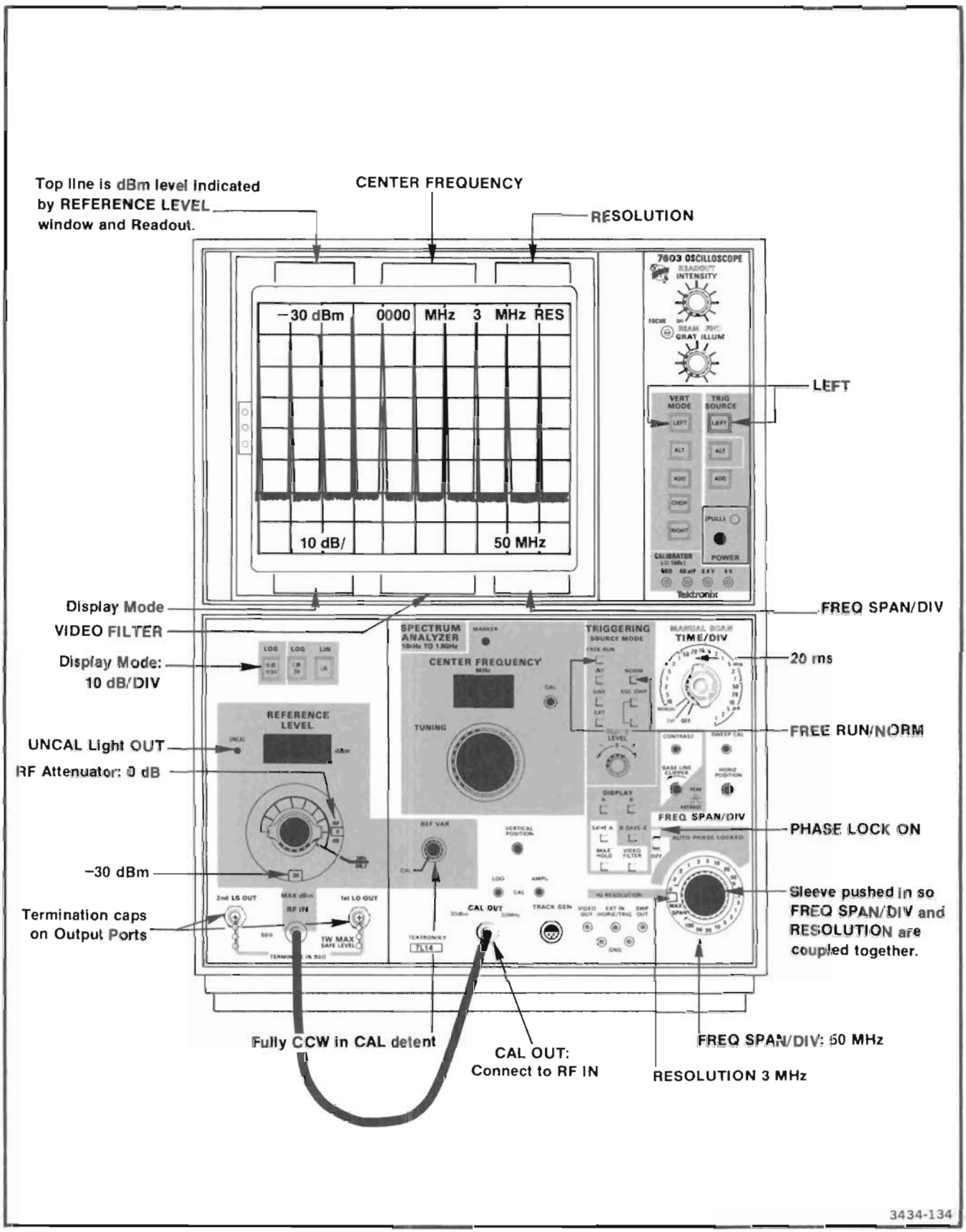



Fig. 2-2. Front-panel selector positions for front-panel calibration.

# FRONT-PANEL CALIBRATION

## 1. Preliminary Operational Procedure that Calibrates the 7L14 to the Oscilloscope Mainframe

When the 7L14 plug-in unit is installed in a 7000-Series mainframe, the spectrum analyzer should be calibrated to ensure correlation between plug-in and and mainframe deflection sensitivities. We recommend that the front-panel calibration procedure be performed anytime the instrument is turned on, and before making critical measurements, to ensure optimum accuracy.

a. Plug the 7L14 Spectrum Analyzer into the 7000-Series mainframe. Ensure that the 7L14 is securely latched in the compartment.

*NOTE*

*A safety latch is used to reduce the possibility of the instrument slipping out of the mainframe.*

b. Connect the oscilloscope mainframe to a suitable power source and switch the power on. Allow about 30 minutes for instrument stabilization.

c. Set the front-panel controls as illustrated in Fig. 2-2 and connect the CAL OUT signal through a short coaxial cable to the RF INput.

d. Adjust the oscilloscope Intensity and Focus controls for optimum display.

e. Depress the 2 dB/DIV display mode button. Position the baseline of the display to the bottom graticule line with the VERTICAL POSITION control and line up the first marker with the first vertical graticule line, using the HORIZ POSITION control.

f. Depress the 10 dB/DIV display button. The display should now resemble that shown in Fig. 2-2.

## 2. Calibrate the Frequency Readout

Due to hysteresis in the tuning system, the calibration and accuracy of the readout must be performed and checked from the same direction (low to high).

a. Without applying the calibrator signal to the RF INput, decrease the FREQUENCY SPAN/DIV setting to 10 MHz, and increase the CENTER FREQUENCY readout to 50 MHz.

b. Apply the CAL OUT signal to the RF INput. Center the 50 MHz calibrator signal over the center graticule line.

c. Adjust the frequency CAL for a CENTER FREQUENCY readout of 50 MHz.

*NOTE*

*It is important to tune the signal from low to high. If the tuning direction is reversed, repeat the procedure by returning the FREQ SPAN/DIV to MAX and the CENTER FREQUENCY to 000 to establish the same reference point on the hysteresis loop.*

## 3. Calibrate the Sweep Span

a. With the CAL OUT signal applied to the RF INput, increase the FREQ SPAN/DIV to 50 MHz and tune the 250 MHz marker to the center graticule line (see Fig. 2-3).

b. Calibrate the frequency span to 50 MHz/div by adjusting the SWP CAL for 1 marker per division. It may be necessary to keep the 250 MHz marker centered with the frequency TUNING control as the sweep is calibrated. Final display should resemble that in Fig. 2-3.

## 4. Check and Adjust LOG-AMPL Calibration

The LOG CAL adjustment calibrates the gain of the analyzer vertical output so the 2 dB/DIV and 10 dB/DIV modes may be accurately set. The AMPL CAL adjustment sets the reference level to the top graticule line.

a. Set the 7L14 selectors and controls as directed in step 2 and tune the fundamental 50 MHz calibrator signal to the center of the graticule.

b. Alternately switch Vertical Display from 10 dB/DIV to 2 dB/DIV and adjust AMPL CAL so the peak amplitude of the signal is the same for each logarithmic display mode. Adjustments should be made in 2 dB/DIV mode.

c. With the Vertical Display mode at 10 dB/DIV, set the top of the calibrator signal to the top graticule line with the LOG CAL adjustment so the signal level indicates −30 dBm.

d. Check the display log scale by switching the REFERENCE LEVEL in 10 dB steps from −30 dBm to +30 dBm and note that the display amplitude decreases 10 dB, or one division, per step.

e. Switch the display modes from 2 dB/DIV to LIN. Signal amplitude reference level should not change more than 2 dB for 2 dB/DIV to 10 dB/DIV, or 0.5 division from 2 dB/DIV to LIN mode.

## 5. Adjust Contrast and Check Baseline Clipper Operation

*NOTE*

*The contrast ratio between the clipped portion of the display baseline and the rest of the display is affected by the sweep rate, frequency span, resolution, and ambient light.*

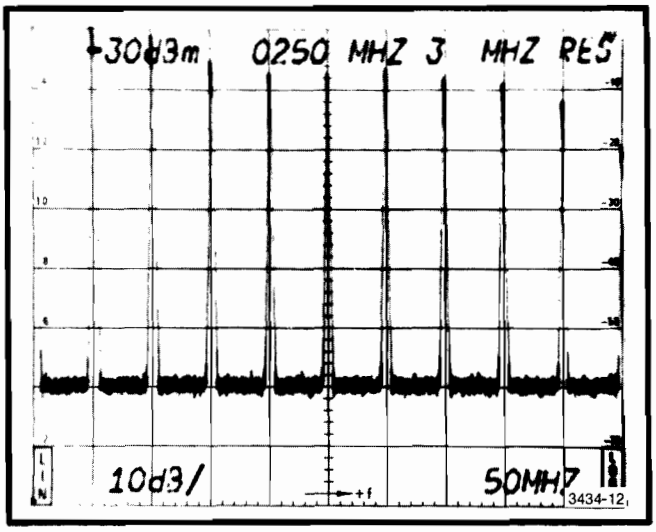



**Fig. 2-3. Calibrating the sweep span.**

a. With the BASELINE CLIPPER control set midrange, adjust the CONTRAST control for the desired ratio between the clipped or subdued portion and the rest of the display. Usually the contrast is adjusted so the clipped baseline portion is just visible.

*NOTE*

*When the 7L14 is in digital storage mode and a Digital Processing Oscilloscope is used, the CONTRAST control should be turned clockwise so the baseline clipper is not visible on the display.*

b. Adjust the BASELINE CLIPPER control so the baseline is subdued. If there is excessive noise, it may be desirable to clip noise level as well.

# FUNCTIONAL OR OPERATIONAL CHECK

This procedure uses minimum test equipment to check instrument operating modes, functions, and basic performance. The procedure serves to check for instrument malfunctions and should satisfy most incoming inspection or pre-operational check-out requirements. A detailed Performance Check, which requires extensive test equipment, is part of the Calibration Procedure in tthe Service Instructions. This operational check also familiarizes the user with instrument operation.

## Equipment Required

The internal calibrator, and the internal attenuator are used as the reference source for the checks in this procedure. Also required are:

50 Ω coaxial cable: 18 inch, BNC to BNC connectors (part of the Standard Accessories).
20 dB of attenuation.

## Preparation

Set and calibrate the front-panel controls as described in the previous procedure.

## 1. Check Operation of Front-Panel Pushbuttons and Controls

**VERTICAL DISPLAY.** Display modes are activated by three pushbuttons. Pressing any of these buttons cancels the other mode.

— **10 dB/DIV.** Active, display is a calibrated 10 dB/division, 80 dB dynamic range. Calibration is checked later in this procedure.

— **2 dB/DIV.** Active, display is calibrated 2 dB/division, 16 dB dynamic range. Calibration is checked later in this procedure.

— **LIN.** Active, display is linear between the reference level (top of graticule) and zero volt (bottom of graticule).

**REFERENCE LEVEL.** (Reference level and IF Gain). Continuous controls that change the reference level 10 dB for each detent. Reference level goes from −30 dBm to +30 dBM in all display modes, without the gain control. With the gain control, and the Vertical Display in 10 dB/Div, the range is from −60 dBm to +30 dBm. In 2 dB/DIV and LIN Display Modes, the range is −100 dBm to +30 dBm.

**REF VAR** is a reference level vernier with a 10 dB control range.

**TRIGGERING.** Triggering source is activated by pressing one of four pushbuttons. Pressing any one of the buttons cancels or deactivates the other mode.

— FREE RUN Active, the trace free runs.

— INT Active, the displayed signal is used as a trigger source.

— LINE Active, the trace is triggered at power line frequency.

— EXT Active, trace runs only when an external signal is applied to the EXT IN HORIZ/TRIG connector.

**SGL SWP.** Pressing this button aborts the current sweep. Pressing the adjoining button arms the sweep generator; the button lights and remains lighted until the sweep completes. The analyzer makes a single sweep of the selected spectrum.

**TIME/DIV.** Selects sweep rate and manual scan operation. In MNL position, MANUAL SCAN control should vary the crt beam across the full horizontal axis of the crt graticule.

**BASELINE CLIPPER.** When digital storage is off, this control subdues the display intensity at the baseline. When digital storage is on, this control positions a horizontal line, or cursor, on the display. Signals above the cursor are peak detected; signals below the cursor are averaged. The cursor should position anywhere within the graticule window.

**DISPLAY A.** Active, half of digital storage memory is displayed. Signal amplitude should remain constant. Vary the BASELINE CLIPPER control and note that the noise level below the cursor is averaged.

**DISPLAY B.** Active, the other half of memory is displayed. Signal amplitude should remain constant. Vary the BASELINE CLIPPER control and note that the noise level below the cursor is averaged.

When both DISPLAY A and DISPLAY B are active, contents of A and B memory are interlaced and displayed.

Both sections are updated each sweep. Update of A memory depends on the state of SAVE A.

**SAVE A.** Active, contents in A memory are saved and not updated. Verify operation by changing REFERENCE LEVEL and observe that the DISPLAY A display does not change when DISPLAY B is inactive.

**MAX HOLD.** Active, stores maximum signal amplitude at each memory location. Verify operation by changing CENTER FREQUENCY or REFERENCE LEVEL and note that the maximum level at each location is retained.

**B—SAVE A.** Active, the difference between updated data in B section of memory and that saved in A is displayed. Verify by saving data in A, then changing the reference level and pressing B—SAVE A; only the difference can be observed by canceling DISPLAY A and DISPLAY B. The reference (zero difference) level is normally set at graticule center, but can be internally adjusted by service personnel.

**VIDEO FILTER.** Active, one of three filters is selected depending on the resolution bandwidth setting, for display noise averaging.

**FREQUENCY SPAN/DIV.** As this control is rotated clockwise or counterclockwise, frequency span/div should change from 0 to MAX in 5-2-1 sequence. Display should indicate this change.

**RESOLUTION.** As this control is rotated, resolution bandwidth should range from 30 Hz to 3 MHz in decade steps. The RESOLUTION control can be coupled to the FREQ SPAN/DIV control when the knobs align with indicing marks.

**CAUTION**

*The 1st and 2nd LO OUT ports must be terminated into 50 Ω at all times. For optimum performance, keep the termination caps in place when these ports are not used.*

**2. Check the 10 dB/DIV** (within 0.15 dB/dB to 2 dB max. over 70 dB dynamic range) **and LIN Mode** (within 10% over 8 divisions) **Calibration**

a. Set the FREQ SPAN/DIV to 10 MHz and the RESOLUTION bandwidth to 300 kHz. Turn the BASELINE CLIPPER control fully clockwise.

b. Apply the Calibrator signal to the RF INput and tune the fundamental 50 MHz signal to center screen.

c. Reduce the FREQ SPAN/DIV setting to 5 kHz and the RESOLUTION bandwidth to 3 kHz, keeping the signal centered on screen with the TUNING control. Activate AUTO PHASELOCKED.

d. Switch in VIDEO FILTER, and increase the TIME/DIV setting to 50 ms.

e. Position the top of the signal to the top graticule line with the VERTICAL POSITION control to establish a reference.

f. Increase the RF Attenuator settings in 10 dB increments, noting that the signal amplitude decreases 1, ±0.1 division between steps.

*NOTE*

*It may be easier to observe the change if the video filter is switched in. If used, decrease the sweep speed until the UNCAL indicator light goes out.*

g. Since the RF Attenuator range is 60 dB, the last 10 dB step of the 70 dB dynamic range may be checked as follows:

(1) Return the RF Attenuator to 30 dB and add a 20 dB attenuator between the RF INput and CAL OUT signal. Adjust the signal amplitude to some reference line on the graticule with the REF VARiable control.

(2) Increase the RF Attenuator setting 20 dB and note that the signal is still visible above the noise level.

The total deviation over the 70 dB dynamic range of the display must not exceed 1.5 dB or 0.75 minor divisions.

h. Remove the 20 dB attenuator and again apply the CAL OUT signal directly to the RF INput. Switch off the VIDEO FILTER and set the RF Attenuator to 10 dB. Set the FREQ SPAN/DIV to 1 MHz and the RESOLUTION to .3 MHz.

i. Change the display mode to LIN. Position the baseline of the display on the bottom graticule line then adjust the 50 MHz amplitude with the REF VARiable control so it is 6.3 divisions.

j. Increase the RF Attenuation 10 dB by switching to 20 dB, and note that the signal amplitude decreases to 2.0, ±0.6 division for an amplitude change ratio of 3:16:1, ±10%.

k. Return the REF VARiable control in its CAL detent and the RF Attenuator to 0 dB.

**3. Check the Frequency Readout Accuracy** [± (5 MHz +20% of Frequency Span/Div)]

*NOTE*

*Due to hysteresis in the tuning system (1st LO), the accuracy of the frequency readout should be checked by approaching each check point from the same direction (low to high). The FREQ SPAN/DIV is first switched to MAX SPAN and the center frequency tuned to 0000 before tuning to the desired check point. If for any reason the direction of tuning is reversed, this procedure must be repeated to establish the same point of reference on the hysteresis loop.*

a. Switch the display mode to 10 dB/DIV, RESOLUTION bandwidth to 300 kHz, FREQ SPAN/DIV to MAX and tune the CENTER FREQUENCY to 0000. With the Calibrator signal applied to the RF INput, decrease the FREQ SPAN/DIV to 1 MHz and increase the CENTER FREQUENCY readout towards 50 MHz until the 50 MHz signal is centered on screen. (The signals will move from right to left as the frequency is increased.)

b. Adjust the front-panel CAL for a CENTER FREQUENCY readout of 50 MHz.

c. Tune the CENTER FREQUENCY from low to high, checking the accuracy of the readout in 50 MHz increments. Readout accuracy, when the signal is centered on the screen, should be within ±(5 MHz + 20% of the FREQ SPAN/DIV) or within ±5 MHz with a frequency span of 1 MHz/DIV.

**4. Check the Range of the REF VAR Control**

a. Switch the display mode to 10 dB/DIV, FREQ SPAN/DIV to 500 kHz and the RESOLUTION bandwidth to 30 kHz. Apply the CAL OUT signal to the RF INput and tune the 50 MHz signal to the center of the screen. Decrease the FREQ SPAN/DIV to 50 kHz keeping the signal centered with the TUNING control.

b. Switch VIDEO FILTER in, turn the Gain selector ccw and switch the RF Attenuator to 50 dB to establish +20 dBm REFERENCE LEVEL. Set the TIME/DIV selector to 50 ms.

c. Position the top of the signal at the 4th graticule line (center screen) with the VERTICAL POSITION control.

d. Check the REF VAR control range by turning it fully cw from its CAL detent. Gain increase should equal approximately 10 dB or the signal amplitude should increase 1 division. Return the REF VAR control to its CAL detent.

**5. Check the Operation of the VIDEO FILTERS**

The VIDEO FILTER reduces or averages the noise level on the display. See Fig. 2-4. Tune to one of the Calibrator signals and check the operation of the filters with RESOLUTION settings of 3 MHz, 30 kHz, and 300 Hz.

**6. Check Sensitivity** <−130 dBm to −80 dBm, depending on Resolution Bandwidth.

*NOTE*

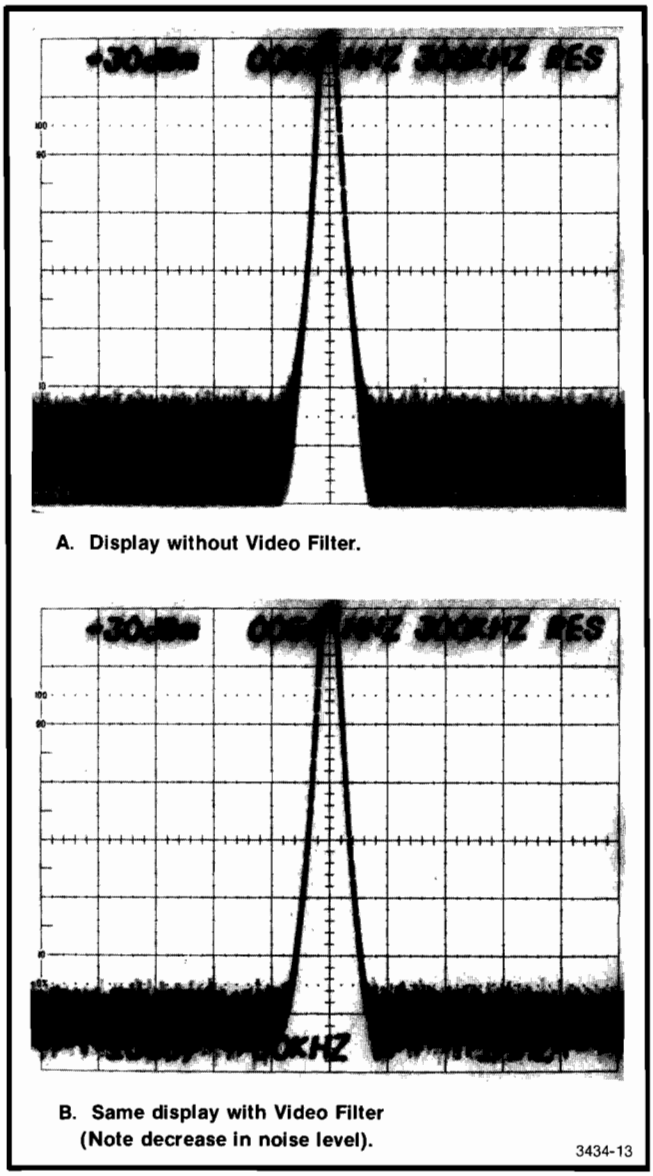
*Sensitivity is specified according to the input or average noise level. The 7L14 calibrator is the reference used to calibrate the display.*

a. Set the 7L14 front-panel controls as follows:

| | |
|---|---|
| REFERENCE LEVEL | −80 dBm |
| Display Mode | 2 dB/Div |
| TIME/DIV | 50 ms |
| FREQ SPAN/DIV | 0 |
| RESOLUTION | 3 MHz |
| DISPLAY A | on |
| VIDEO FILTER | on |
| TRIGGERING SOURCE | FREE RUN |
| TRIGGERING MODE | NORM |

b. Terminate the RF INput into 50 Ω. Note that the displayed noise level is below the top of the screen (−80 dBm).

c. Decrease the resolution to 300 kHz and the reference level to −90 dBm. Note that the displayed noise level is below the top of the screen (−90 dBm).



A. Display without Video Filter.

B. Same display with Video Filter (Note decrease in noise level).

3434-13

Fig. 2-4. Video Filter Operation.

d. Decrease the resolution to 30 kHz and the reference level to −100 dBm. Decrease the TIME/DIV to .5 seconds. Note that the displayed noise level is below the top of the screen (−100 dBm).

e. Decrease the resolution to 3 kHz and switch the display mode to 10 dB/DIV. Decrease the TIME/DIV to 1 second/div. Note that the displayed noise level is below the 5th graticule line from the top (−110 dBm).

f. Decrease the resolution to 300 Hz. Decrease the TIME/DIV to 2 seconds/div. Note that the displayed noise level is below the 6th graticule line from the top (−120 dBm).

g. Decrease the resolution to 30 Hz. Decrease the TIME/DIV to 5 seconds/div. Note that the displayed noise level is below the 7th graticule line from the top (−130 dBm).

**7. Check for Spurious Signals from Internal Sources (Residual Responses)** (≤ −100 dBm, referenced to the RF INput)

a. Remove any signal connected to the RF INput so it is free of signals from any external source. Switch the RF Attenuator to 30 dB to further isolate the 1st mixer from the input.

b. Switch out the VIDEO FILTER, turn the Gain selector fully ccw and ensure that the REF VARiable control is in its CAL detent. The REFERENCE LEVEL will now read 0 dBm. The signal level at the 1st mixer however represents −30 dBm, because the RF Attenuator subtracts an additional 30 dB.

c. Set the FREQ SPAN/DIV to 1 MHz and the RESOLUTION bandwidth to 30 kHz. Switch the TIME/DIV to 50 ms or less so the UNCAL indicator is not lighted.

d. Switch to the 2 dB/DIV display mode, verify that the trace is on the bottom graticule line, then switch the display mode to 10 dB/DIV. The dynamic range of the graticule is now a calibrated 10 dB/DIV, with the top line representing −30 dBm into the 1st mixer as described in step b.

e. Tune slowly across the frequency band (10 kHz to 1.8 GHz) checking for spurious signals. The amplitude of any spurious signal must not exceed −100 dBm (signals above the 7th graticule line from the top). NOTE: Subtract 2 dB for noise which will be riding on top of the signal. If the spur is marginal (within a 3 dB of specifications) and you desire to check its amplitude more accurately, proceed as follows:

(1) Decrease the FREQ SPAN/DIV to 50 kHz or less and the RESOLUTION bandwidth to 3 kHz. (This will decrease the noise with respect to the signal amplitude.) Keep the signal centered on screen with the TUNING control as the FREQ SPAN is decreased.

(2) Decrease the sweep speed if the UNCAL indicator lights. Note the spurious response amplitude and verify that it does not exceed specifications.

f. Return the FREQ SPAN/DIV and RESOLUTION selectors to their original settings (step c).

**8. Check Resolution Bandwidths and Shape Factor** (Bandwidth 3 MHz to 30 Hz within 20% in decade steps; shape factor 4:1 to 300 Hz except 3 MHz resolution. Maximum bandwidth 60 dB down, with 3 MHz resolution is 13 MHz. Shape factor for 30 Hz is 12:1)

a. Apply the Calibrator signal to the RF INput and set the RF Attenuator to 0 dB. Turn the Gain selector fully ccw for a REFERENCE LEVEL of −30 dBm.

b. Tune the 50 MHz marker to the center of the screen, set the FREQ SPAN/DIV to 1 MHz, and the RESOLUTION bandwidth to 3 MHz.

c. Switch the display mode to 2 dB/DIV and adjust the REF VARiable control if necessary, for a full screen display.

*NOTE*

*Ensure that the sweep rate is set so the UNCAL light is out and the baseline of the display is on the bottom graticule line.*

d. Check the bandwidth of the signal at the 6 dB down level (see Fig. 2-5A). Bandwidth must equal 3 MHz ±600 kHz.

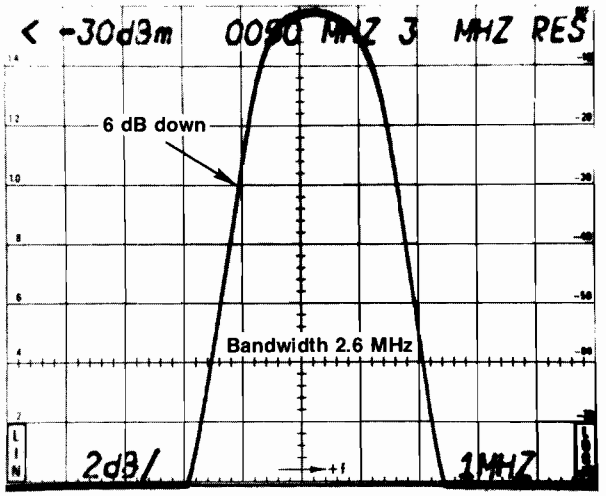
e. Switch the display mode to 10 dB/DIV and the VIDEO FILTER in. Switch the FREQ SPAN/DIV to 2 MHz and check the shaper factor (see Fig. 2-5B).

f. Return the display mode to 2 dB/DIV, decrease the FREQ SPAN/DIV to 100 kHz and the RESOLUTION bandwidth to 300 kHz. Keep the signal centered on screen with the TUNING control as the FREQ SPAN is decreased.

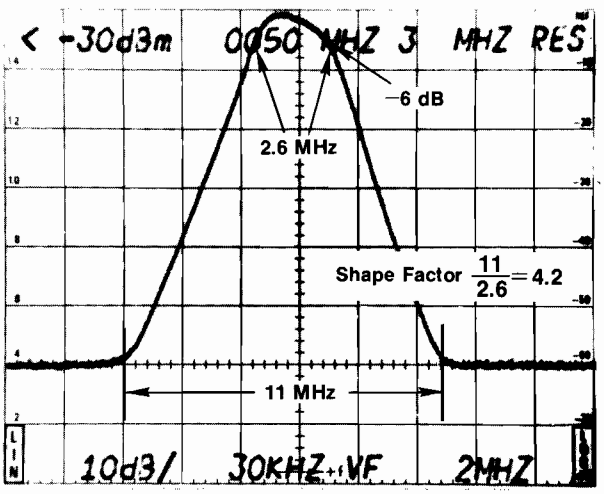
g. Check the bandwidth at the 6 dB down level. Bandwidth must equal 300 kHz ±60 kHz.

h. Switch the FREQ SPAN/DIV to 200 kHz, display mode to 10 dB/DIV, and check the shape factor as described in step e.

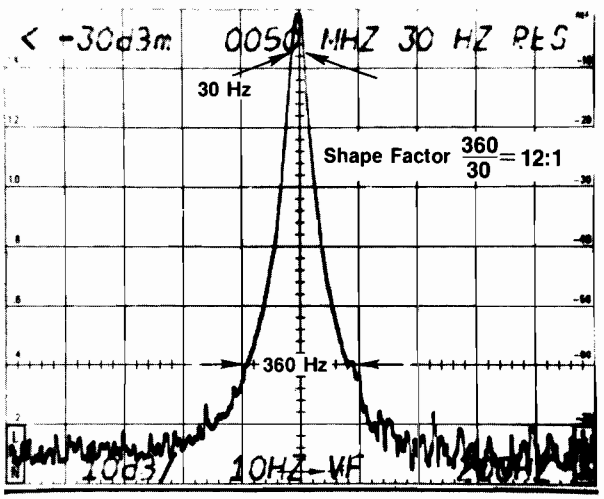
i. Reduce the FREQ SPAN/DIV to 10 kHz, the RESOLUTION bandwidth to 30 kHz, and the display mode to 2 dB/DIV. Center the display with the TUNING control if necessary.




A. Measure bandwidth at the 6 dB down level.




B. Shape factor is ratio of bandwidth at −60 dB to −6 dB levels.




C. Shape factor of 12:1 with 30 Hz resolution.

3434-14A

Fig. 2-5. Measuring bandwidth and shape factor.

j. Check the bandwidth. Bandwidth must equal 30 kHz ±6 kHz.

k. Reduce the FREQ SPAN/DIV to 200 Hz and the RESOLUTION bandwidth to 300 Hz. Center the display with the TUNING control if necessary. Adjust the REF VARiable control for a full screen display.

l. Check the bandwidth of the response at the −6 dB level. Bandwidth must equal 300 Hz ±60 Hz.

m. Switch the display mode to 10 dB/DIV, reduce the sweep speed to 2 s/Div to maintain a calibrated display. Measure the response shape factor.

n. Reduce the RESOLUTION to 30 Hz and change the display mode to 2 dB/DIV. Check the bandwidth at the −6 dB (half screen) level. Bandwidth must equal 30 Hz ±6 Hz.

o. Switch the display mode to 10 dB/DIV and measure the shape factor. Shape factor for 30 Hz resolution must equal 12:1 or better (see Fig. 2-5C).

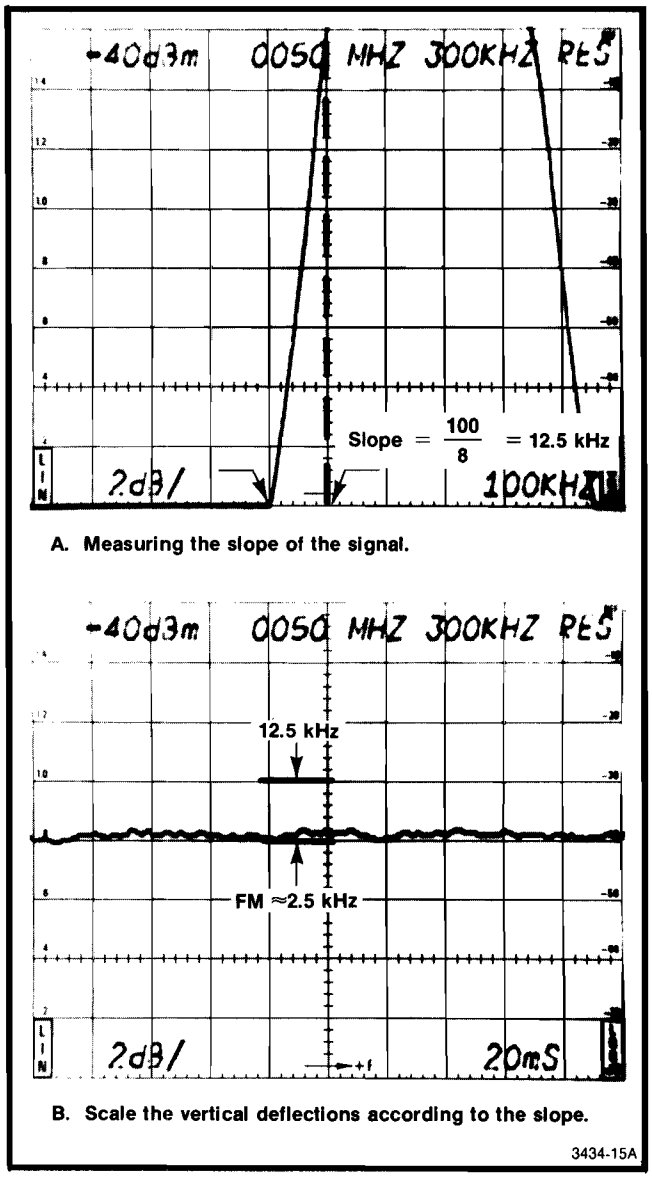
**9. Check Residual (Incidental) FM** (10 kHz (p-p) for 20 ms when not phaselocked )

a. Set the 7L14 front-panel controls as follows:

| | |
|---|---|
| Display Mode | 2 dB/Div |
| REFERENCE LEVEL | −40 dBm (0 RF Attenuation, 10 dB gain) |
| TIME/DIV | 20 ms |
| TRIGGERING SOURCE | FREE RUN |
| TRIGGERING MODE | NORM |
| DISPLAY A | on |
| RESOLUTION | 300 kHz |
| FREQ SPAN/DIV | 100 kHz |
| AUTO PHASELOCKED | OFF |

b. Apply the CAL OUT signal to the RF INput. Tune the center frequency to 50 MHz. Center the signal on screen.

c. Position the marker signal with the CENTER FREQUENCY control so the slope (horizontal versus vertical excursion) of the response can be measured as illustrated in Fig. 2-6A. It may be advantageous to SAVE A to freeze the display. The slope must be calculated on the linear portion of the waveform.




A. Measuring the slope of the signal.

B. Scale the vertical deflections according to the slope.

3434-15A

**Fig. 2-6. Measuring residual FM.**

d. Switch FREQ SPAN/DIV to 0 (time domain) and adjust CENTER FREQUENCY to position the display near center screen as shown in Fig. 2-6B. Note the peak-to-peak amplitude of the display within any horizontal division scaling the vertical deflections according to the slope estimated in step c. Residual FM must not exceed 1 kHz for 20 ms, measured within the linear portion determined in step c.

**10. Check Residual (Incidental) FM** (≤13 Hz (p-p) for 20 ms when phaselocked)

a. Set the 7L14 front-panel controls as follows:

| | |
|---|---|
| Display Mode | 2 dB/DIV |
| REFERENCE LEVEL | −40 dBm (0 RF Attenuation) |
| TIME/DIV | 20 ms |
| TRIGGERING SOURCE | FREE RUN |
| TRIGGERING MODE | NORM |
| DISPLAY A | on |
| RESOLUTION | 300 Hz |
| FREQ SPAN/DIV | 200 Hz |
| AUTO PHASELOCKED | on |

b. Apply the CAL OUT signal to the RF INput. Tune the center frequency to 50 MHz. Center the signal on screen.

c. Calculate the slope as described in procedure 9, step c.

d. Switch FREQ SPAN/DIV to 0 (time domain). Measure residual FM using the same technique as described in procedure 9, step d. Residual FM must not exceed 13 Hz for a 20 ms period.

**11. Check Sweep Circuit Operation with the TIME/DIV Selector in the MANUAL and OFF Positions**

a. Switch the TIME/DIV selector to the MANUAL position and rotate the MANUAL SCAN control through its range. Note that the crt beam scans the full 10 division graticule width.

b. With DISPLAY A off, switch the selector to the OFF position. Note that the crt beam is now vertically centered on the screen.

c. Return the TIME/DIV selector to 50 ms position for normal operation.

**12. Check Digital Storage**

a. Set the 7L14 front-panel controls as follows:

| | |
|---|---|
| REFERENCE LEVEL | −30 dBm |
| Display Mode | 10 dB/Div |
| RESOLUTION | 300 kHz |
| FREQ SPAN/DIV | 200 kHz |
| TIME/DIV | 50 ms |
| DISPLAY A | on |
| VIDEO FILTER | on |

b. With the calibrator signal applied to the RF INput, tune the signal to center screen, then activate SAVE A.

c. Change the REFERENCE LEVEL to −10 dBm and activate DISPLAY B. The display of the calibrator signal should be 2 divisions lower (20 dB less) than DISPLAY A.

d. Activate B-SAVE A and check display. It should show the difference between DISPLAY B and DISPLAY A (see Fig. 2-7).

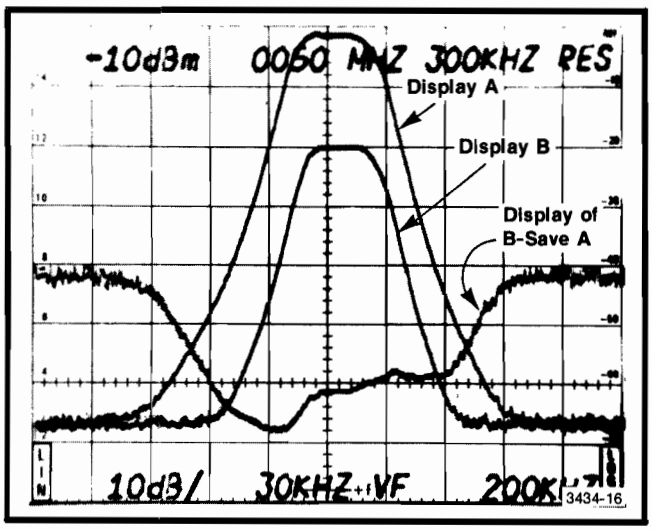



**Fig. 2-7. Using digital storage to measure the difference between two displays.**

e. Deactivate SAVE A, B-SAVE A, and VIDEO FILTER. Activate MAX HOLD.

f. Change both CENTER FREQUENCY and REFERENCE LEVEL and note that MAX HOLD function retains and holds the maximum signal amplitude and frequency excursion.

g. Deactivate MAX HOLD and select DISPLAY A.

h. Vary the PEAK/AVERAGE control to shift the cursor over the screen height and note that signal and noise are averaged below the cursor.

This completes the operational check of the 7L14.

# GENERAL OPERATING INFORMATION

## 1. Signal Application

The RF INput impedance to the 7L14 is 50 Ω. At high frequencies, impedance mismatches between the RF INput and the signal source can cause reflections in the transmission line and degrade instrument performance. Flatness, sensitivity, spurious response, etc., are all affected. To reduce mismatch, use good quality 50 Ω coaxial cable to connect the signal source to the RF INput and keep the cable as short as possible. Cable losses become excessive above frequencies of 1 GHz.

Avoid applying high level signals (above −30 dBm) to the 1st mixer of the 7L14. High level signals overload the mixer and may produce spurious signals. A conversion chart shown in Fig. 2-8 will aid in determing input signal level, in dBm, μV, and μW, from a voltage or power source.

**CAUTION**

*The maximum input power level to the RF attenuator is 1 W average and 100 W peak. When the RF input signals are riding on a dc potential, use a dc block to prevent the dc from reaching the 1st mixer. When the signal source is 75 Ω and you are using the 75 to 50 Ω minimum loss attenuator, a dc block is not required (one is incorporated in the attenuator.) Line stabilization networks, used for conducting EM/RFI measurements, will often have several volts of 60 Hz signal at the output. The dc block will protect the input mixer and prevent its destruction.*

Spurious response, caused by signal overload into the 1st mixer, can be minimized if the signal amplitude is kept within the graticule limits. A recommended procedure is to adjust the Gain selector for some baseline noise on the display, then increase the RF Attenuator setting until the strongest signals are within the graticule limits. If this does not bring these signals within limits, add external attenuators.

The 7L14 can be used with a 75 Ω signal source by using a 75 Ω to 50 Ω minimum loss attenuator. This attenuator is available as an optional accessory (refer to the Accessory page for ordering information). Sensitivity and power levels are often rated in dBm (dB with reference to 1 mW regardless of impedance). Sensitivity and power levels for 75 Ω systems are usually rated in dBmV (dB with reference to 1 mV across 75 Ω). Figure 2-9 is a circuit diagram of a suitable matching pad for this purpose. Figure 2-10 shows the relationship between 50 Ω and 75 Ω units, with matching attenuators included; the conversion is described as follows:

(1) dBmV (75 Ω) = dBm (50 Ω) + 54.47 dB. For example, −60 dBm (50 Ω) + 54.47 dB = −5.5 dBmV (75 Ω).

(2) dBm (75 Ω) = dBm (50 Ω) +5.72 dB. For example, −60 dBm (50 Ω) +5.72 dB = −54.3 dBm (75 Ω).

(3) For some applications you may wish to know the relationship between dBm and dBμV. For 50 Ω systems dBμV = (dBm) + 107 dB.

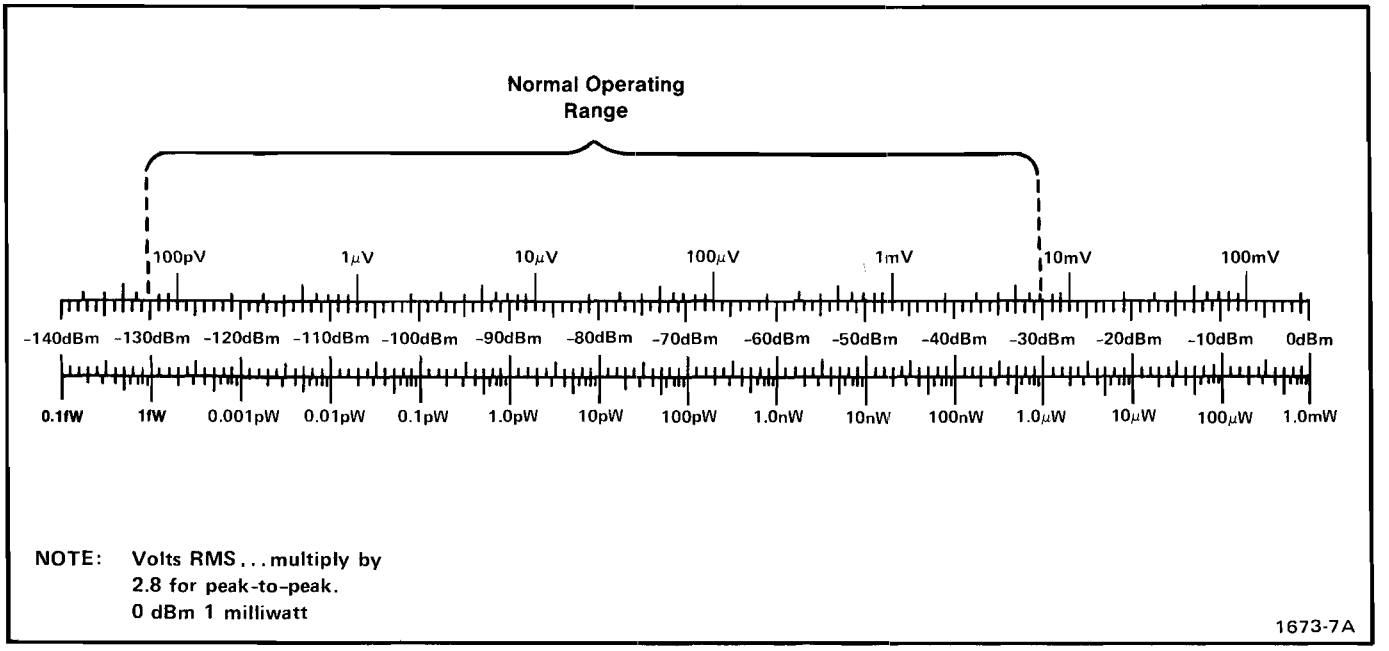



**Fig. 2-8. Volts-dBm-Watts conversion chart for 50 Ω impedance.**

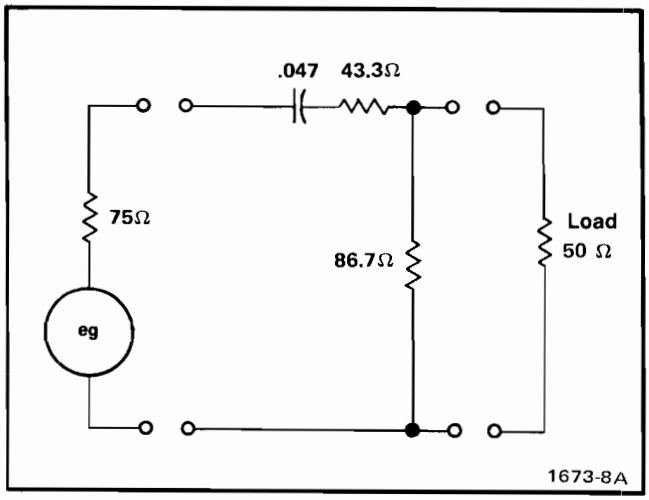



**Fig. 2-9. Circuit of a 75 Ω-to-50 Ω matching pad (ac coupled).**

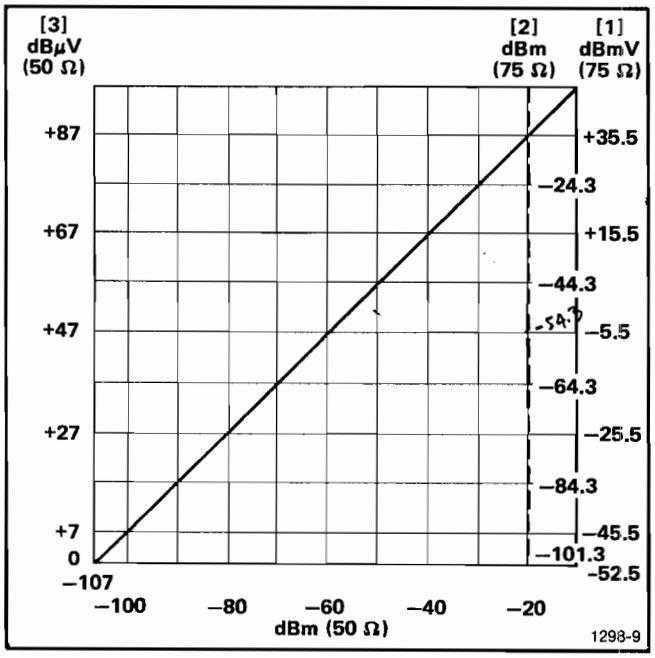



**Fig. 2-10. Graph to illustrate the relationship between dBm, dBmV and dBμV (matching attenuator included where necessary).**

## 2. Resolution, Sensitivity, and Frequency Span

Resolution is the ability of a spectrum analyzer to discretely display adjacent signals within a frequency span. This resolution ability is a function of analyzer bandwidth, sweep speed, frequency span, and incidental FM. The frequency span and sweep time are adjusted for minimum bandwidth to a cw signal. Theoretically, resolution and resolution bandwidth become synonymous at very long sweep times.

Resolution bandwidth is measured and specified for the 7L14 as the bandwidth (separation) at the 6 dB down point on the signal.

As the analyzer sweep rate is increased, the signal amplitude will decrease and bandwidth will increase, signifying that both sensitivity and resolution have been degraded.

The best resolution with no video filter, for a given frequency span and sweep time is expressed as:

$$R_0 = \sqrt{\frac{\text{Frequency Span (in kHz)}}{\text{Sweep Time (in ms)}}}$$

Bandwidth determines both noise level and the resolution capability of the analyzer. As the bandwidth decreases, the signal-to-noise level and, therefore, sensitivity increases. Maximum sensitivy is obtained at the higher resolution settings.

The frequency span is symmetrical about the center frequency. The frequency span to be used depends on the application. Wide frequency spans are used to monitor a frequency spectrum for spurious signals, check harmonic distortion, etc. Narrow frequency spans are used to identify a particular signal and check its characteristics such as modulation, bandwidth, etc.

When wide frequency spans are displayed, sweep rate is usually increased to eliminate flicker; this requires the use of wide resolution bandwidths. When narrow frequency spans are used, high resolution capability is usually desired and slow sweep speeds are required.

The FREQ SPAN/DIV and RESOLUTION selectors for the 7L14 are normally coupled together to optimize resolution for the frequency span selected; however, either can be independently set by pulling out the "PULL TO UNLOCK" sleeve around the FREQ SPAN/DIV selector.

An UNCAL indicator will light when the sweep time is too fast for an amplitude calibrated display. Sweep speed should be reduced to maintain a calibrated reference level if the UNCAL indicator lights.

For pulsed applications, the resolution bandwidth of the analyzer should be on the order of 1/10 the side lobe frequency width, or the reciprocal of the pulse width, in order to ensure adequate resolution. The RESOLUTION selector is usually set for optimum main lobe detail after the sweep rate has been adjusted.

### 3. Gain Desensitization Near 0 Hz

If the Gain selector is set for a REFERENCE LEVEL that is −50 dBm or more (e.g. −60 dBm) with the RF Attenuator at 0 dB, a decrease in sensitivity will be noticed below 1 MHz. This effect is caused by the 0 Hz response overdriving the 1st IF amplifier. If you are operating between 0 Hz and 2 MHz, do not set the Gain selector in this region.

### 4. Using the Video Filter

The video filter is used for effective averaging of distributed signals, such as noise, and high frequency components on the display. When signals are closely spaced, the filter may be useful in reducing modulation between the two signals so they can be more easily analyzed. The filters can also be used to average the envelope of pulsed RF spectra that has a relatively high PRF (pulse repetition frequency); however, because the filter is basically an integrating circuit, low PRF signals produce poor results.

The use of the video filter may require a reduction in sweep speed in order to maintain a calibrated display. Again, the UNCAL indicator will light if the sweep speed is too fast for the video filtering, RESOLUTION and FREQ SPAN/DIV selected.

### 5. Selecting Sweep Rate

Because the FREQ SPAN changes the resolution and sensitivity, the sweep rate must be decreased as the frequency span and resolution bandwidth are decreased, or when the UNCAL indicator lights. When the FREQ SPAN is reduced to 0, the analyzer functions as a fixed tuned receiver. The analyzer now displays time domain characteristics of the signal, within the bandwidth capabilities of the analyzer. Sweep Time/Div can now be used to examine or analyze such characteristics as modulation pattern, pulsed repetition rates, etc.

*NOTE*

*The RESOLUTION bandwidth should be maximum for time domain analysis.*

### 6. Triggering the Display

The sweep trigger source is usually switched to the FREE RUN mode for normal spectrum displays; however, it may be desirable or necessary to trigger the display when the event is time related to some source, or when the frequency span has been reduced to zero and a time domain analysis is performed.

The sweep can be triggered from the vertical or video signal from either vertical plug-in compartment, from the power line voltage, or from an external source. Trigger slope for any mode can be + or −; the triggering level is adjustable over the full range of a displayed signal when using INTernal trigger source, over a 10 V range of an external signal when using EXTernal source, and over the peak-to-peak range of the line signal when using LINE.

In the NORM triggering mode, the display is triggered when the triggering signal source is within specifications. If the triggering signal is absent or outside of specifications, the sweep recurs automatically to provide a display baseline.

The amplitude of triggering signal that is required to trigger the sweep depends on the sweep mode selected. The internal signal is ac coupled; the line and external signals are dc coupled. Trigger sensitivities are: 1) ≤0.5 division of signal (peak-to-peak) and ≤0.5 volt (peak-to-peak) of external signal for NORM mode. 2) ≤0.5 division of signal (peak-to-peak) and ≤0.5 volt (peak-to-peak) of external signal for SGL SWP mode.

Maximum safe trigger input signal level to the EXT INputs is 50 volts (dc + peak ac).

In the FREE RUN state, the sweep will not synchronize with any input trigger signal.

When the SGL SWP button is depressed, the sweep will run after the adjoining button is depressed. During the sweep cycle, the activating button lights to indicate that the sweep is running. This feature is useful when photographing displays at slow sweep rates. The activating button does not arm the trigger circuit like some time base units.

When triggering on pulsed spectra, it may be necessary to fine tune the sweep start away from a null point to trigger the display.

### 7. Manual Scan of the Spectrum

This position is used to examine a particular point or portion of the display, such as one of the null points of a frequency modulation spectrum.

a. Calibrate the sweep span with the TIME/DIV selector in one of the scan positions as previously described, then switch to the MANUAL position.

b. Use the MANUAL SCAN control to scan the selected frequency spectrum.

## 8. Using an External Sweep Source

A signal source is required to sweep the analyzer externally. A voltage ramp from 0 V to 10 V ±1 V will sweep the analyzer through its full span. 0 V corresponds to 0 Hz and 10 V to the high frequency end of the selected span. Input impedance is approximately 12 kΩ for an external sweep signal.

Before switching to external operation, calibrate the sweep span using the internal sweep and the 50 MHz calibrator signal as described under Operational Check. Switch the TIME/DIV selector to its EXT position and apply the external voltage to the EXT IN HORIZ/TRIG jack. Adjust the upper end of the voltage (10 V) until the analyzer sweep span is calibrated.

*NOTE*

*The frequency deviation across the selected span is a linear function (within 20%) of the input voltage, so +5 V dc should tune the analyzer to the center of the selected frequency span.*

## 9. External Trigger Operation

This procedure is applicable when an external trigger source, such as a pulse generator or modulator, is used to trigger the display so it can be synchronized to an event (e.g., measuring PRF of a radar signal).

a. Apply the trigger signal (≥0.5 V peak) to the EXT IN HORIZ/TRIG jack of the 7L14. Switch the TRIGGERING SOURCE to EXT and the TIME/DIV selector to the desired sweep rate.

b. Adjust the triggering SLOPE and LEVEL for the desired triggering point.

c. If time domain information is desired, reduce the FREQ SPAN/DIV to 0 and set the RESOLUTION to 3 MHz.

The analyzer is now triggered by the external source so the display sweep rate can be controlled externally.

## 10. Digital Storage

Digital storage provides a smooth (flicker free) display. Two complete events can be stored. One of these can be saved and then compared to subsequent updated information. A MAX HOLD feature updates the stored data in memory when the new input is of higher amplitude, thus allowing monitoring and graphic plotting of display changes with time. Vertical information can be divided by a cursor, or horizontal line, that is positioned with the PEAK/AVERAGE control. Above the cursor, video information is peak detected and displayed; below the cursor, signal averaging occurs. The average (number of samples) is a function of sweep speed. The slower the sweep, the greater the number of samples averaged. This feature suppresses noise in that portion below the cursor and allows full peak detection of vertical data above the cursor. An intensified spot on the cursor indicates the horizontal position at which memory is being updated.

When digital storage is used, an additional quantization error of 0.5% of full screen must be added to the amplitude performance characteristics (i.e., frequency response, sensitivity, etc.)

Digital storage memory is functionally divided into two sections—A and B. Data can be stored in A or B or in both. There are 512 horizontal locations in A and 512 horizontal locations in B. When both are displayed, the origin of B is shifted such that the A and B coordinates are interlaced to provide 1024 display increments. Data in memory is continually updated with each sweep so the display, when displaying A or B, is always current.

When SAVE A function is activated, data in A memory is held in storage and only B memory is updated. This inhibition takes place whether A is displayed or not. This mode captures an event or waveform for comparison with a subsequent event displayed by DISPLAY B mode. In this mode all of A memory is displayed, then all of B, each by a separate sweep.

When B—SAVE A is activated, the contents of data in B memory minus the contents saved in A are displayed. This provides the comparison of the two events by presenting the algebraic difference of the two displays. This convenient mode can be used to align filters or other devices when tuning for a null. The reference waveform is stored in A and the unknown in B. If the device under test is active, the B waveform may be larger than the reference which results in a shift in the zero reference line. The position of the zero reference can be selected with an 8-bit digital switch. The reference level is normally set mid-screen so positive and negative quantities can be observed. Qualified service personnel can position the reference anywhere within the graticule window.

MAX HOLD causes the digital memory to be updated only if the new input is of higher magnitude than the former (B memory only if SAVE A is active). This allows

monitoring of signals that may change with time and provides a graphic record of amplitude/frequency excursions.

Signal averaging is useful for suppressing noise. The number of samples averaged per digitized slot (increment) is a function of the spectrum analyzer sweep rate. The slower the sweep speed, the more samples averaged per resolution bandwidth. Resolution bandwidth also affects the amplitude difference between peak detected and average levels of cw signals. When the resolution bandwidth is less than 1/30th the span/division (e.g., 100 kHz or less with 5 MHz span/div) there will be significant difference between peak and average amplitude levels of cw signals. The peak value will be the true value, the average value will be in error, especially if only A or B is displayed. It is best to run digital storage with both A and B interlaced when using narrow resolution bandwidth with wide frequency spans.. To analyze signal amplitude level, set the cursor at least 1/4 division below the signal peak. To average noise, set the cursor at least 1/4 division above the noise level.

## 11. Using the CAL OUT Signal Reference for Accurate Frequency and Amplitude Measurements

The accuracy of frequency measurements may be improved by using harmonics of the crystal controlled Calibrator. The Calibrator accuracy is within 0.01%. Frequency measurements within 2 MHz are possible by using either of the two methods described below.

### Measuring the Frequency Span between a Calibrator Marker and the Signal to Obtain an Absolute Frequency Measurement

a. Tune the signal to the center graticule line, approaching this point from the low frequency side of the display. Couple the FREQ SPAN/DIV and RESOLUTION selectors together and open up the display to obtain an accurate setting, by reducing the FREQ SPAN/DIV to 5 MHz and increasing RESOLUTION to .3 MHz. Adjust SWP CAL, if necessary, to calibrate the display for 10 divisions between the 50 MHz calibration markers. (Remember to approach the center point from the low frequency side.)

b. Connect the CAL OUT signal and the signal source through a BNC "T" connector to the RF INput so both signal and markers are displayed.

c. Measure the frequency span between the signal and the nearest 50 MHz marker. (Frequency span is 5 MHz/Div.)

d. Add or subtract the frequency span to the respective marker to obtain the signal frequency. Since the maximum frequency span between the signal and marker is 25 MHz ±5%, marker accuracy is 0.01% and human observation error is approximately 1/2 a minor division or 0.5 MHz. The accuracy using this method is within 2 MHz.

### Measuring the Frequency after the Frequency Readout Correction Factor Has Been Established

a. As described for the frequency span method, tune the signal to the graticule centerline, opening the display to 5 MHz/Div to obtain an accurate setting. Tune the signal to the center from the low frequency side.

b. Note the frequency readout (e.g., 1002 MHz).

c. Apply the CAL OUT signal to the RF INput and tune the nearest 50 MHz marker to the graticule centerline.

d. Set the frequency readout, with the CAL adjustment, to read the exact frequency (e.g., 1000 MHz.).

e. Retune to the unknown signal, approaching it from the low side, and note the frequency readout.

### Measuring Absolute Signal Levels

Since the top of the graticule is a calibrated REFERENCE LEVEL and the graticule is calibrated in dB/DIV, as described in the Preliminary Front Panel Calibration procedure at the beginning of this section, it is easy to measure the absolute level of most signals.

a. Calibrate the graticule as previously described in the Operational Check procedure. Ensure that the REF VARiable (gain) control is in its CAL detent.

b. Connect the signal source to the RF INput, as described under Signal Application. Switch to the 10 dB/DIV or 2 dB/DIV display mode.

*NOTE*

*For maximum accuracy, use the same cable that was used to calibrate the REFERENCE LEVEL and use the 2 dB/DIV display mode.*

c. Select a REFERENCE LEVEL with the RF Attenuator and gain selector to bring the signal to be measured within the screen or graticule window.

*NOTE*

*If you are operating in the 10 dB/DIV mode, the gain selector should be within the blue sector.*

d. The absolute signal level equals the number of dB graticule divisions from the reference level (top of the screen) to the signal reference (usually the signal peak) plus the REFERENCE LEVEL readout in dBm. For example: A signal level 4.5 divisions below the top with a REFERENCE LEVEL readout of −60 dBm, in the 2 dB/DIV display mode, is −60 dBm + (−9 dB) or −69 dBm. This refers to the signal level at the RF INput connector. Add the insertion loss of any external attenuators and cables (if they are used) between the signal source and the RF INput.

*NOTE*

*The maximum input level to the RF INput, for linear operation, is −30 dBm with 0 dB RF attenuation; or +30 dBm with 60 dB of RF attenuation. Accurate measurement of signals above this level can only be performed if an external attenuator is used.*

**Accurate Signal Level Difference Measurements in dB**

a. Using the 2 dB/Div display mode, position the top of the lowest amplitude signal to a reference line within the graticule area with the REF VARiable or VERTICAL POSITION controls. If display noise is excessive, use the VIDEO FILTER and reduce the sweep speed to maintain signal amplitude, or decrease the RESOLUTION bandwidth.

b. Use the RF Attenuator selector to reduce the amplitude of the larger signal until it is within the graticule area, and note the increased attenuator reading.

c. Measure the signal level from the reference line established for the smaller signal (graticule is calibrated in 2 dB/DIV), then add the change in RF Attenuator reading to obtain the difference level (in dB) between the two signals.

**Measuring Relative Signal Amplitude in LIN Display Mode**

The vertical scale on the spectrum analyzer graticule is calibrated in dB for LOG display and in increments of 0.2 for the LIN display. Relative signal levels can be made by adjusting the amplitude of one signal with the gain and attenuator controls to 1.0 division, then directly reading from the graticule, the amplitude of the other signals as a percentage of this reference.

### 12. Using the Analyzer Below 100 kHz

The sensitivity of the analyzer degrades about 0.3 dB/kHz below 100 kHz; for example, the sensitivity is about −113 dBm at 50 kHz with 30 Hz resolution. Reference level operation becomes limited to −50 dBm as the center frequency approaches 1 kHz, because of the LO energy that exists in the 1st IF pass-band.

## APPLICATIONS

### 7L14 and the TEKTRONIX TR 502 Tracking Generator

The 7L14 Spectrum Analyzer, combined with the TR 502 Tracking Generator, has the characteristics of a very sensitive synchronized detector. It allows for a number of measurements such as:

— frequency measurements with counter accuracy of low level (below -100 dBm) signals.

— accurate frequency measurements of the modulation components of complex signals.

— return loss and swr measurements.

### 7L14 and the TEKTRONIX 1405 Sideband Analyzer Adapter

The 7L14 Spectrum Analyzer, in conjunction with the 1405 Sideband Analyzer Adapter, allows sideband analysis to be performed directly on the rf carriers in television appications.

Interconnections for operation with the 1405 Side-band Adapter are described below.

a. Connect the 7L14 1ST LO OUT to the 1405 LO IN.

b. Connect the 1405 Z-AXIS OUT to the oscilloscope mainframe EXT Z-AXIS IN.

c. Connect the 1405 VIDEO OUT to the video input of the tv transmitter or circuit under test.

d. Connect a sample of the output of the tv transmitter or circuit under test to the RF INput of the spectrum

analyzer, using an appropriate cable and coupler to avoid exceeding the maximum input power level of +30 dBm.

**CAUTION**

*Use care to keep the power level into the spectrum analyzer low; an off-screen signal can damage the spectrum analyzer. External attenuators should be used if the internal attenuator will not reduce the signal sufficiently.*

For these applications, as well as applications for spectrum analyzers alone, such as: measuring intermodulation products, cross modulation, radiation interference, modulation percentage, modulation index, absolute and relative signal levels, etc. contact your local Tektronix Field Office or representative.

# THEORY OF OPERATION

This section describes the functions of the major circuits in the 7L14 and their relationship in the overall operation of the instrument. The description is general and intended as an aid for the technician and operator to help service, or operate the instrument at maximum efficiency.

The section begins with a functional block diagram description, followed with more detailed analysis of the major circuits. Positive logic is used for digital circuits. The diagrams contain typical waveform and voltage data that should be helpful to understand circuit functions and aid in troubleshooting the instrument.

## BLOCK DIAGRAM

The 7L14 is a swept front-end spectrum analyzer that covers the frequency range from 10 kHz to 1.8 GHz and provides a frequency span of 1.8 GHz. A detailed block diagram in the Diagrams section, illustrates signal paths and function of the major circuits. Refer to this diagram while reading the description.

The input signal path to the 1st mixer consists of a 0 to 60 dB step attenuator, a limiter (to protect the mixer from a DC voltage), a 1.8 GHz low-pass filter, and a 3 dB isolation pad. The stop band for the filter begins at 2.095 GHz. The filter attenuates frequencies of 2.095 GHz (1st IF) and higher, that may exist between the 1st mixer and the RF INput. This reduces susceptibility to image responses, IF direct feed-through from the RF INput, and keeps the 1st LO output from reaching the RF INput connector.

The 1st mixer is a double-balanced type mixer, with its input and output isolated by a 3 dB pad and a traveling wave directional filter, respectively. The 3 dB pad reduces VSWR interaction and improves the response flatness. The traveling wave directional filter reduces intermodulation distortion and provides a termination for image responses from the 1st mixer.

The frequency of the 1st LO is swept, when the frequency span is 100 kHz/Div or more, through some portion or all of the frequency range from 2.095 GHz to 3.895 GHz. The center frequency of the oscillator can also be tuned through the selected frequency span. When the frequency span is 50 kHz/Div or less, the 1st LO frequency is fixed and the 2nd LO is swept through the selected span.

The output of the 1st mixer (1st IF) is centered at 2.095 GHz. A bandpass filter 10 MHz wide (with a center frequency of 2.095 GHz) attenuates the upper sideband, and a 2.2 GHz low-pass filter ensures the outband integrity of the bandpass filter. The 1st IF is converted to 105 MHz (2nd IF) in the 2nd mixer by mixing the 2nd LO frequency of 2.2 GHz with the 1st IF of 2.095 GHz.

The 2nd IF signal is amplified by a Pre-Resolution amplifier, then reduced in bandwidth to 3 MHz by a three-cavity helical resonator filter. The 105 MHz IF is converted down to 10 MHz in the 3rd mixer by the 3rd LO frequency of 95 MHz mixing with the 2nd IF of 105 MHz. Amplification and bandwidth of the 10 MHz 3rd IF, are controlled in the resolution and function IF amplifier stages. Amplification is controlled by switching in amplifier stages. Bandwidth is controlled, in decade steps from 3.0 MHz to 30 Hz, by switching bandpass filters into the signal path. IF gain can be selected in 10 dB steps from 0 to 70 dB. Gain stages are in the Pre-Resolution amplifier and the Function IF amplifier, with an additional 10 dB of gain in the 30 Hz filter. The additional 10 dB of gain may be added only when the resolution bandwidth is 30 Hz and the display mode is 2 dB/DIV or LIN. Variable gain between the 10 dB steps, is provided by a variable gain stage in the Post-Resolution amplifier.

The Function IF amplifier contains circuits for logarithmic, linear, and vertical deflection factor. The log displays are 2 dB/Div and 10 dB/Div. The amplifier also compensates for the gain variation when the resolution bandwidth and display modes are changed, so the reference level remains constant through all combinations of resolution and display modes.

The detected signal from the Function IF amplifier is amplified and summed with voltage levels for vertical positioning, then applied through push-pull amplifiers to the oscilloscope mainframe interface. Three auxiliary circuits can be switched into the video signal path. These circuits provide: video filtering (30 kHz, 300 Hz, and 10 Hz), digital storage (DISPLAY A, DISPLAY B, SAVE A, B-SAVE A, and MAX HOLD), and baseline suppression, peak detention, or averaging when digital storage is activated.

The sweep circuits provide the frequency base or time base for the display. In the frequency domain, the output from the sweep generator is applied through the horizontal amplifier to the mainframe interface, for the horizontal deflection, and through the frequency span attenuator to

the 1st or 2nd local oscillator, for frequency sweeping. The frequency span of the display is therefore a function of how much the 1st LO or the 2nd LO is swept.

The sweep ramp from the sweep generator is attenuated in calibrated increments by the FREQ SPAN/DIV attenuator, then applied through switch contacts to either the 1st LO (YIG) driver circuits or the voltage controlled 16-19 MHz oscillator in the 2nd LO phase lock loop.

A current ramp through the main tuning coil, sweeps the 1st LO for frequency spans from 100 MHz/Div through 5 MHz/Div, the current ramp is then applied to the FM coil of the YIG oscillator for spans of 2 MHz/Div through 0.1 MHz/Div. When the frequency span is decreased to 50 kHz/Div or less, the 1st LO may be phase locked and the sweep ramp is applied through switch contacts to a voltage controlled 16-19 MHz oscillator in the 2nd LO phase lock loop. The 2nd LO phase lock loop is a servo system which transmits changes of the 16-19 MHz oscillator frequency to the 2nd LO.

The marker (or ditch) in the signal that is displayed when the FREQ SPAN/DIV selector is in MAX position, is produced by the marker generator. The marker position is relative to the setting of the tune control: it indicates the portion of the span that will be the center of the display when the frequency span is reduced. When digital storage is on, the marker is displayed on the signal as well as on the cursor. The marker, summed with the video at the amplifier, drives the vertical output stage.

This completes the signal path flow and the function of the frequency span circuits.

## DETAILED CIRCUIT DESCRIPTION

The following is more detailed than the block diagram description and should assist in servicing and operating the instrument.

### RF or Microwave Circuits ◈2

The RF section consists of sealed microwave assemblies that contain hybrid circuits on ceramic substrates, or circuit boards mounted in a metal substrate. The cover of the assembly is then sealed with a conductive sealant. This seal should not be broken, nor repair attempted. Components in the RF microwave assemblies are identified with a circuit number when they are referred to in the calibration procedure (e.g., C15, C16, and C17 in A8). The circuitry within the block is simplified to illustrate the function of the hybrid assembly.

As previously described in the block diagram description, input signals to the unit can be attenuated in 10 dB increments up to 60 dB, by A86. A limiter protects the first mixer from signals which have more than 1 W input power, and from those containing a dc component. Signals then pass through a 1.8 GHz low-pass filter (FL2) with a stop band that begins at 2.095 GHz. Signals in the frequency band from 0 to 1.8 GHz, then pass through a 3 dB isolation pad to the 1st mixer.

The 1st mixer, a double balanced type, converts the incoming broad spectrum of signals to a 2.095 GHz IF, by mixing these incoming signal frequencies with the output of the 1st LO (A12). The 1st LO may be swept and tuned within the 2.095 GHz to 3.895 GHz band.

The output of the 1st mixer (A2) is isolated by a traveling wave directional coupler that couples the 2.095 GHz IF signal to a 2.2 GHz LP filter, 2.095 GHz band pass filter, and into the 2nd mixer in assembly A10. As previously described this isolation improves the performance of the 1st mixer and reduces spurious signals.

The 2nd mixer in assembly A10, mixes the output of the 2.2 GHz 2nd LO (in A20) to convert 2.095 GHz down to 105 MHz IF.

The bandpass and center frequency of the 2.095 GHz IF is adjusted by the capacitors C15, C16, and C17 (in A8) and the coupling of the 2nd mixer, in assembly A10. These adjustments are performed to obtain a bandpass of 10 MHz that is centered at 2.095 GHz with optimum skirt shape. The mixer is oriented in the chamber to one of two balance points to provide the best rejection of spurious products generated by the 1st LO and 2nd LO.

Band reject filters, consisting of 1/4 wavelength stubs that are separated 1/4 wavelength, are distributed along the output transmission lines of the 2nd mixer to the 105 MHz IF. These suppress 2.3 GHz and 4.6 GHz.

The active component for the 2nd LO (in A20) is transistor Q20. Its collector load is a stripline resonator. The center frequency of this oscillator and the frequency span are controlled by an error voltage from the 2nd LO frequency servo system. The oscillator output is coupled through a directional coupler to the 2nd mixer and through a low pass filter to another directional coupler which is part of the 2nd LO frequency servo system.

The phase lock loop for the 2nd LO (in A20) contains a 99.2045 MHz oscillator which is multiplied by a factor of 22. This frequency of 2.1825 GHz is then passed through a bandpass filter (A14) and mixed in A22 with the output of

the 2nd LO to produce an IF between 16 to 19 MHz. Bandpass characteristics and center frequency response of A14 are adjusted by the same procedure that is used to adjust the bandpass characteristics of assemblies A8 and A10.

The 16-19 MHz IF output from assembly A22, is also passed through a 2.3 GHz and a 4.3 GHz filter that is identical to the filter in assembly A20.

The 1st LO (in A12) is a YIG (yittrium-iron-garnet) tuned oscillator. YIG is a material that changes its resonant frequency when it is subjected to a changing magnetic field. The intensity of this field is controlled by current through the tuning coil. When the oscillator is swept, a current ramp from the YIG driver amplifier stage is applied to this tuning coil. The amplitude of this current depends on the setting of the FREQ SPAN/DIV selector. With FREQ SPAN/DIV setting of 50 kHz/Div or less, the normal state of the 1st LO is to operate in a phase locked mode at a frequency which depends on the setting of the TUNING control and some multiple of a 2.19 MHz reference oscillator.

The front panel 1st LO and 2nd LO OUT jacks (J30 and J36) provide access to the two oscillator outputs. These outputs are used by tracking generators. The two ports must be terminated at all times to prevent reflections back into the system. Termination plugs P30 and P36 provide this termination when the ports are not used.

### Phase Lock and Frequency Stabilization ◇3

Frequency stabilization is increased and incidental FM'ing reduced to 10 Hz or less, by a phase lock system that automatically locks the 1st LO at frequency spans of 50 kHz/Div or less unless the front-panel PHASE LOCK switch is in the OFF position. The 2nd LO is always phase locked by a translation phase lock system which is described below.

The 1st LO phase lock loop contains a reference oscillator, a pulse generator and sampler, a phase detector, an error amplifier, and a compensating amplifier that drives the frequency determining element of the oscillator. A narrow rectangular pulse from the sampler driver, at one-half the reference oscillator period, and the output of the 1st LO are applied to a diode detector. The detector output charges to the voltage of the pulse plus the amplitude (at the instant) of the coupled oscillator signal. The summation of these signals is proportional to the phase difference between the 1st LO and the reference oscillator. This voltage is amplified by the error amplifier and drives the compensating amplifier. The output of the compensating amplifier maintains a constant phase difference between the 1st LO and some multiple of the reference oscillator. While a phase difference may exist, there is no frequency error. When locked, the long term frequency stability of the locked oscillator is that of some multiple of the reference oscillator.

To achieve the required stability, the 2nd LO is controlled by a translation phase lock oscillator system. The phase lock loop consists of the circuitry shown in Fig. 3-1. The 2nd LO output is applied through a directional coupler to the phase lock loop mixer A22. It mixes with the 22nd multiple of a 99.2045 reference oscillator in A48A4 and generates an IF signal between 16 to 19 MHz. The 16 to 19 MHz IF signal is amplified and applied to a phase detector (A48A3) where it is compared with the signal from a 16 to 19 MHz oscillator (A48A2). The phase difference is detected, amplified by the error amplifier (A48A5), and applied as a control voltage to the 2nd LO.

When the 1st LO switches from a swept oscillator to phase locked mode, it may shift in frequency. This shift in frequency is coupled through to the VCO for the 2nd LO frequency servo system and pulls the frequency of the 2nd LO in a direction to offset the frequency shift of the 1st LO. The center frequency on the display therefore remains stable. This offset information is provided by the voltage memory circuit.

The memory looks at the offset voltage of the 1st LO before and after phase lock is set, then generates an offset voltage to apply through a summing amplifier to the 2nd LO frequency servo system.

The 16 to 19 MHz oscillator consists of an emitter coupled logic (ECL) IC with a high Q resonant circuit, that is tuned by a hyperabrupt tuning diode CR1564. The frequency of this voltage controlled oscillator (VCO) is affected by the voltage it receives from the TUNE control memory circuit, offset voltage, and, at spans 50 kHz/Div or less, the sweep voltage. The control voltages are applied to both ends of the diode. The summed combination of offset, tune control, and memory voltage is applied through pin F to one side of the tuned circuit and the sweep voltage is applied through pin G, a 30:1 divider (R1560, R1562) to the anode of CR1564.

The sweep voltage comes through the 5 volt regulator circuit board, where its amplitude is adjusted by the Swp Gain adjustment R1960. Additional filtering with C1960, C1962, is switched in at the slower sweep rates to reduce the amount of residual line-related noise that may be riding on the sweep line.

The summing amplifier for the tune control, memory and offset voltage, is U1735. The memory voltage is applied through pin AD and the tune control voltage through pin AC, to the input of the amplifier. The offset

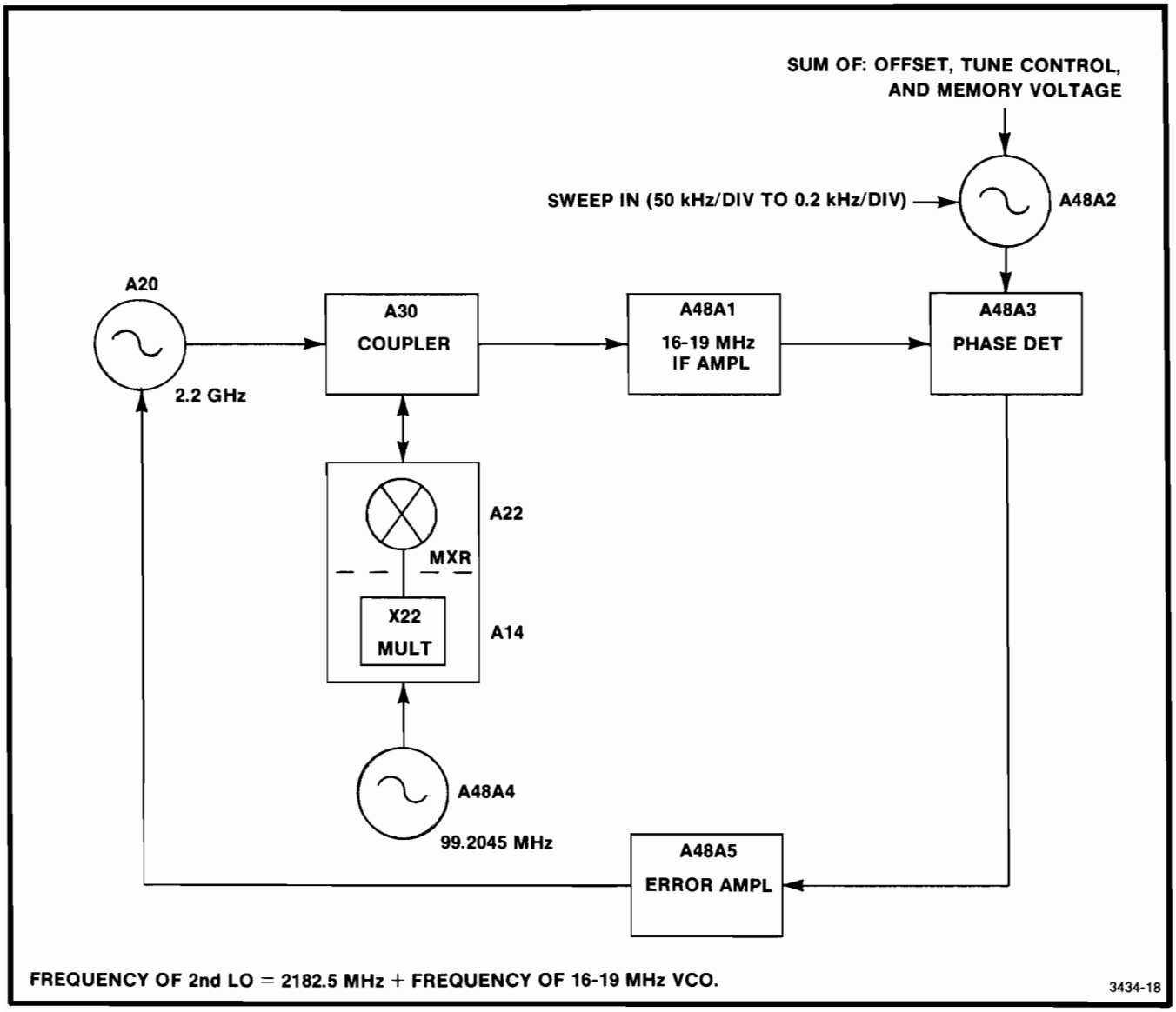



**Fig. 3-1. Functional block diagram of 2nd LO phase lock circuit or frequency servo system.**

voltage that establishes the center frequency of tuning, is supplied by VR1720 and a selectable resistor R1725. Select resistor R1735 sets the gain of U1735 and the response of the 16 to 19 MHz oscillator to the tune and memory voltage.

The output of the phase detector (A48A3) is amplified by the error amplifier U1715, Q1715, on A48A5. The amplifier output drives the collector of the 2.2 GHz oscillator to control its frequency.

The sampling generator and driver (A48A6) are part of the 1st LO phase lock loop. The output from a 2.1944 MHz crystal controlled oscillator is applied through Q1820 and Q1825 to a divide-by-two counter U1825. The 1.0972 MHz output, from the counter, triggers avalanche diode CR1832 to generate strobe pulses for the sampling gate in A24.

The error voltage from the phase detector is applied through J1900 and pin S to the input of U1755, which is the active component for a double-bounded conditionally stable search amplifier. The double bounding of this amplifier is achieved with diodes CR1748 and CR1749 (low leakage, temperature stable diodes) which limit the search amplitude; and CR1742, CR1744, CR1745, and CR1746 which limit the holding range of the loop within the stable gain response range of the phase detector.

The 5 volt regulator board contains a 5 volt regulated supply, phase lock enable relay K1955, sweep gain adjustment for the 16-19 MHz oscillator, and additional filtering for the sweep voltage line when the resolution is 30 Hz. The phase lock enable relay K1955 switches the 1st LO FM coil from the sweep voltage source to the output of compensating amplifier U1755 (in the phase lock circuit) when phase lock is set. Relay K1965 is energized when the resolution bandwidth is reduced to 30 Hz and adds additional filtering to the sweep line. Gain adjustment R1960 calibrates the 50 kHz/Div and less, frequency spans.

### YIG Driver, Voltage Memory, Phase Lock Logic, and Marker Generator ◇5

The YIG driver consists of a main coil driver and an FM coil driver. The main coil driver contains an operational amplifier U1048, and a Darlington transistor Q1041. The FM coil driver contains amplifier U2042, driving transistors Q2041 and Q2039. Operation of these drivers is described under Frequency Tuning and Readout that follows this title.

The phase lock logic circuit locks the 1st local oscillator. When phase lock mode is set, the sequence of events is as follows: The 2nd LO tune control is engaged and the 1st LO tune control is disengaged. At the same time the sampling generator for the 1st LO phase lock loop is enabled. At the end of a delay period, the phase lock enable relay is energized and the search cycle of the loop begins. At the end of another delay period, the memory is activated and it looks at the shift the 1st LO made to reach a lock point. The memory stores this data, which is later applied to the 2nd LO and summed with other controlling voltages to shift the 2nd LO frequency an equivalent amount so it compensates for the shift of the 1st LO frequency when it locked.

Pin 1 of P2053 (input to U2059E) is grounded through the FREQ SPAN/DIV selector when the frequency span is 50 kHz/Div or less. The output of a set-reset flip-flop (U2052A U2052C) is low when the PHASE LOCK switch S1015 is ON. The two high inputs at U2052B produce a low-to-enable signal out, which is inverted by U2059A and applied through pin 4 of P2034 to switch the tuning logic from the 1st LO tuning potentiometer to the 2nd LO tuning potentiometer R20. This high is also applied through U2055A, Q2068 and Q2061 to enable the sampling generator for the 1st LO phase lock loop.

The low-to-enable signal out of the NAND gate U2052B also triggers a mono-stable multivibrator, U2048. At the end of some delay period, the output of U2048 goes high. This is compared by NAND gate U2052D, to the high at the output of U2059A.

The delayed low out of U2052D is applied through buffer amplifier U2055D and energizes phase lock enable relay K1955, on the 5 V regulator board on diagram 3. The delayed low signal is also inverted by U2059B and applied through buffer amplifier U2055B as a high for the TRACK GEN connector J70, and through a second buffer, U2055C, to another delay circuit in the voltage memory.

At this time, the phase lock loop is closed and starts its search mode. Before one cycle is complete, the 1st LO should acquire lock. To provide the time necessary for the loop to lock, a second delay is inserted in the sequence path by a one shot mono-stable multivibrator U2033 and NAND gate U2032B. At the end of this delay, the output of U2032B goes high, which is inverted by U2032A and energizes L2025 to close S2025.

The closing of S2025 contacts allows the capacitor C2020 to charge to the input error voltage at pin 2 of U2034. This error voltage is indicative of the direction and amount the 1st LO traveled to reach a lock point. The contacts of S2025 open and the output of Q2021 goes to the voltage that was stored across C2020. Memory now sends this compensation voltage to the 2nd LO and the center frequency on the display remains stationary.

### Frequency Tuning Control and Readout ◇4 ◇5

Three modes of operation are used to tune the center frequency: 1) Tune control voltage is summed with the sweep voltage at the driver input for the main coil of the YIG oscillator, over frequency spans of 100 MHz/div through 5 MHz/div. 2) The sweep voltage is removed from the main coil driver and applied to the FM coil driver for frequency spans of 2 MHz/div to 0.1 MHz/div. The tune control voltage is still applied to the main coil driver. 3) The sweep and tune control voltages are removed from the YIG oscillator driver circuits and applied to the 2nd LO driver, for frequency spans of 50 kHz/div or less. The 1st LO is phase locked, providing the front-panel PHASE LOCK switch is on.

### Tune Control ◇4

The input to P2078-3 (U1068 pin 10) is high when the phase lock is set (PHASE LOCK switch S1015 on and FREQ SPAN/DIV selector 50 kHz or less). This condition energizes MP22, which engages the drive clutch to the tuning potentiometer R20 for the 2nd LO. MP20 engages when the input to P2078-3 is low, which is its state for frequency spans of .1 MHz/div (100 kHz/div) and higher. This drives the tuning potentiometer R22 for the 1st LO.

The voltage source for the tuning potentiometers is the outputs of operational amplifiers U1055B, Q2062, and U1055A, Q1048. Zener diode VR 2059 sets the non-

inverting input of U1055B at 6.3 volts, which establishes approximately +9.2 volts at the emitter of Q2062 and −9.2 volts at the emitter of Q1048.

The output of U3068 is a proportional to the position of the tuning potentiometer. This voltage is summed with the sweep voltage at the input to the search marker generator, then applied through cam 33 (100 MHz/Div or less) to the YIG driver. The center arm potential of the tuning potentiometer R20 is applied to the summing point at U1735, which drives the frequency determining circuits for the 2nd LO oscillator.

### YIG Driver ◈5

The dc level, out of the center frequency tuning potentiometer R22, is summed with the sweep voltage at the inverting input to U1048. U1048 is an operational amplifier with a Darlington transistor Q1041 as the negative supply source. Increasing the voltage input to the amplifier increases the current demand from the negative supply. This forward biases Q1041 and increases the current output so the current through the YIG main coil increases until the voltage output of R22 balances the input voltage change to U1048. As the current increases through the YIG main coil, the frequency of the oscillator increases.

When the FREQ SPAN/DIV is reduced to 2 MHz or less, the sweep voltage is removed from the input to U1048 and applied to the FM coil driver (U2042, Q2041 and Q2039). Current through the main coil is now dependent on the dc level from the tune potentiometer R22, which sets the center frequency of the YIG oscillator. K1063 is energized to shunt the main coil with a filter network consisting of R1065, C1062, C1063 and C1059.

The FM coil driver is similar to the main coil driver, with the addition of Q2041 supplying positive current to the FM coil.

R1045 adjusts an offset voltage into the summing point of U1048 so the center frequency of the YIG oscillator can be calibrated. R1044 and R1052 set the gain of the operational amplifiers so the frequency span of the YIG oscillator is calibrated for spans of 100 kHz/div and higher.

### Frequency Span ◈13 ◈5

The sweep ramp from either the sweep generator (U1170), the external sweep source, or the manual control circuit, is applied through R1254 to the inverting input of operational amplifier U1250A. This is a voltage ramp from 0 to about 9 volts, which is summed with a dc offset voltage set by R1255. The output sweep amplitude of U1250A, is set by R1250 (Swp Gain) so the ramp is a calibrated 20 V centered about 0 V. This voltage ramp drives both the search marker generator (U3015A and U3015B) and the frequency span attenuator circuit.

U1250B is the active component of an operational amplifier whose gain is a function of the input-to-feedback resistance ratio. This ratio is selected by the FREQ SPAN/DIV selector S108B. The output voltage ramp of U1250B is applied to the YIG oscillator main tuning coil driver U1048, for frequency spans of 5 MHz/Div or more, and to the FM coil for spans of 0.1 MHz/Div and 2 MHz/Div. When the FREQ SPAN/DIV is 50 kHz or less, this sweep is applied to the phase lock loop for the 2nd LO.

### Marker Generator ◈5

Switching the FREQ SPAN/DIV selector to MAX SPAN, closes cam 34 and opens cams 33 and 32. This routes the tune control dc voltage and sweep voltage output from U1250A on diagram 13 to the input of amplifier U3015A. The YIG oscillator is now swept its full frequency span and a marker is generated that is commensurate to the dc potential out of the 1st LO tune control (R22).

The output of U3015A causes diodes CR3013 and CR3012 to switch as the sweep ramp crosses through the dc level setting of the tune control circuit, developing a positive ditch or marker at the output of U3015B. This marker is applied to the vertical output circuit to provide the center frequency marker on the display.

### 105 MHz IF Amplifier, 3rd Mixer and Oscillator ◈6

Signals within the 10 MHz bandwidth of the 105 MHz IF, are amplified by Q85. The output load for Q85 is a three sectional helical resonator that is tuned so the bandwidth is reduced to 3 MHz. The 3rd mixer converts the 105 MHz IF to 10 MHz IF, by mixing 105 MHz with the output of a crystal controlled 95 MHz oscillator.

Aperature coupling is used between each section of the helical resonator. The 3rd mixer is a balanced mixer. L85, and C95 are tuned to the sum of the two input frequencies (about 200 MHz). This reflects the upper sideband back into the mixer and reduces IM signals. C87, R87, L89, and R241 provide a constant impedance-matching circuit to the input of the 10 MHz IF amplifier.

### 10 MHz IF Pre-resolution Amplifier and Resolution Filter Circuits ◈6 ◈7

Three circuit blocks comprise the resolution circuit; the 10 MHz preamplifier, five selectable resolution filters, and

a post-resolution amplifier. As the resolution bandwidth is selected, gain compensation is provided to maintain a constant signal level input to the Function IF amplifier. The Function IF amplifier is then adjusted so a constant signal reference level is maintained on the display for changes of resolution or display modes.

The signal path through the resolution preamplifier depends on the position of relay K281.This relay is energized in all positions of the Gain selector except the first two (0 dB and 10 dB). When energized, the signal path is through Q280 and Q290, which has a gain of 20 dB. Gain of the operational amplifier, containing Q250 and Q260, is increased by 10 dB when the base of Q270 is grounded through the gain selector. This occurs every odd 10 dB step of the selector.

With the gain selector fully ccw (0 dB), the 10 MHz input signal to T240 is amplified by the IF amplifier Q240 and the operational amplifier that contains Q250 and Q260. The front panel AMPL (CAL) adjustment R80, sets the gain of Q240 so a −30 dBm, 50 MHz signal, at the RF INput provides full-screen signal amplitude.

Switching the Gain selector one position cw, grounds the base of Q270, turning the transistor on, and bypasses some of the feedback current of the operational amplifier Q250. The closed loop gain of the stage is therefore increased 10 dB. Gain is accurately calibrated by the 10 dB gain adjustment R267.

Increasing the Gain selector position an additional 10 dB, opens the base of Q270 and energizes relay K281. The output of T264 is now switched through Op Amp Q280-Q290, for 20 dB of additional gain.

Increasing the Gain position to 30 dB grounds the base of Q270, increasing the gain of the preamplifier an additional 10 dB for a total gain increase through the preamplifier of 30 dB. As previously described, the relay K281 remains energized through the remaining four positions of the Gain selector.

The resolution section contains four crystal filters (for 30 Hz to 30 kHz resolution) and a 300 kHz coupled-resonator filter. The 300 kHz filter consists of six resonant sections and an amplifier. Signal path through or around the filters, is directed and controlled by relays K300, K353, K354, K355, K356, and K357. (The 30 Hz filter is located on YIG Driver, Voltage Memory and 30 Hz filter board, Diagram 5). These relays are energized as the RESOLUTION cam switch S108A is switched to positions that connect the relay armature to the −15 V power source.

Amplitude adjustments for each filter section establish a signal output level as the resolution is changed, so the signal reference level on screen remains constant through the RESOLUTION range. It is important when aligning the filters, that their center frequency is centered on the others. This is done by switching in one of the crystal filters periodically to re-establish the center of the band-pass for the 300 kHz and 3 MHz filters.

The resolution output amplifier provides approximately 15 dB of gain. The gain compensates for loss in sensitivity through the microwave circuits. The response across the 1.8 GHz span remains relatively flat (within +1 dB, −2 dB).

The 10 MHz IF signal is routed (by K357) through either a wide filter (3 MHz) or a narrow filter, for additional shaping and noise reduction. Bandpass of the narrow filter is 300 kHz. K357 is de-energized when the RESOLUTION is switched from 3 MHz to 0.3 MHz.

### 30 Hz Filter ◇5

This filter contains an amplifier, crystal filter, and a 10 dB gain boost circuit. The 10 MHz IF is routed through the filter when K354 on diagram 7 is de-energized, and K3021 is energized. Q3024 and Q3022 are emitter coupled amplifiers. Gain of the amplifier is set by adjusting the amount of feedback from the output of T3029 to the base of Q3024. This adjustment is R3038.

The additional 10 dB of gain is provided when the 30 Hz filter is in the signal path and the gain selector is advanced to its cw position. This turns on Q3032 and decreases the negative feedback for the amplifier. Gain is calibrated by adjusting R3030.

### 50 MHz Calibrator ◇8

The calibrator is a crystal controlled oscillator configured with the crystal in the feedback loop of a multivibrator. Output of the oscillator is calibrated to a −30 dBm with adjustment R956. Output impedance is 50 Ω.

### Function IF Amplifier ◇8

The Function IF consists of six cascode amplifier cells or blocks, connected in cascade. Each cell operates as a linear or logarithmic amplifier depending on the display mode selected to provide the gain characteristics required for the three display modes of 7L14. The gain of each cell is a function of the emitter resistance of the input transistor. In the Log mode, diodes in the emitter circuit of the amplifier reduce the gain at a logarithmic rate from 10 dB to 0 dB as the signal level increases.

When the operator depresses the 10 dB/DIV display button, +15 V is applied through S130A, pin 1 of P135 and pin 2 of P520 to the anodes of the log diodes; CR511-CR512, CR514-CR515, CR517-CR518, CR521-CR522, CR524-CR525, and CR531-CR532. These diodes are forward biased (with no signal input) and the amplifier cell operates at full gain. As the signal input level increases, the emitter voltage approaches the bias of the diodes to turn the diodes off. The amplifier gain therefore decreases to 0 dB.

The gain decreases to 0 dB progressively as the signal level increases, starting with Q720-Q710 and progresses toward the front end.

In the 2 dB/DIV mode, +15 V is applied to diodes CR527-CR528 and CR534-CR535 in the emitters of Q680 and Q720, and +15 V is removed from the anode of the 10 dB log diodes so they are now back biased.

CR534-CR535, in the emitter of Q720, and CR527-CR528 in the emitter of Q680, provide approximately 4 dB of log gain per amplifier cell. This provides two break points, at about 4 dB and 8 dB of the gain curve over the dynamic window. These two break points change the curve slope suffieiently to shape the curve for 2 dB/DIV. R737 and R697 set the slope of the curve after the break point.

The 10 dB and 2 dB/Div Ref Level adjustments R802 and R801, position the linear portion of the log gain curve (see Fig. 3-2) within the 8 division graticule window.

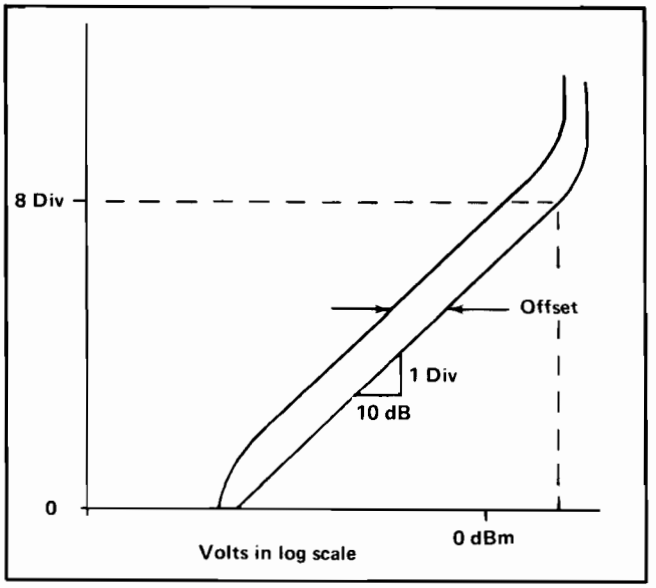



**Fig. 3-2. Log converter curve.**

The 2 dB/DIV and LIN mode displays require at least 70 dB of gain through the analyzer's IF; therefore, additional stages are switched in to increase the Function IF gain. S130A is disengaged then the 2 dB/DIV or LIN mode buttons are pressed. The base of transistors Q570 and Q600 now have a return path to ground, through U2890 in the 40 dB or 50 dB positions of the gain selector. Grounding the base of the transistors, turns them on and boosts the gain through these amplifier cells an additional 10 dB per cell. Transistors Q630 and Q660 are turned on when the gain selector is switched to the 60 or 70 dB positions.

Gain of the Function IF amplifier, in the LIN and 2 dB modes, is calibrated at the 40 dB and 60 dB steps by adjusting R603 and R663. Q730 is turned on when the LIN mode is selected and R733 (LIN Ref Lvl) sets the reference level of the display to the top line of the graticule.

The output signal of Q700 is coupled to a linear detector. The linear detector consists of Q740 driving the common emitter amplifier Q750-Q760 with feedback through C766, the detector diodes CR772-CR771, resistors R775-R776, and C776 to the input of the amplifier.

During the positive and negative excursion of the IF signal, feedback current is supplied through CR772 and CR771. This produces a circulating current through the diodes proportional to the average signal input level. The negative video output signal is developed across R772-R819 and R771. The video is then applied through a filter network to the vertical output stages.

Linear Baseline Offset adjustment R803, compensates for baseline shift when the display mode is switched from LOG to LIN.

## Video Filter, Baseline Clipper and Vertical Output ◈9

Video signals from the detector are amplified by operational amplifier U820B. Its feedback resistance, R826, is shunted by baseline-clamping diodes and fast or slow video filter circuits that are switched in by U830 and U840.

Clamping diode CR825 maintains the video baseline reference by clamping the amplifiers input signal level. CR825 clamps the input of the amplifier from shifting positive.

The three sections of U840 are connected so they operate as OR gates to connect C840 in the feedback loop for U820B. Pulling pin 2 or 3 of P830 low, or activating the

30 kHz video filter, turns one section of U840 on, to connect C840 in the feedback loop. Pin 2 of P830 is pulled low when the front-panel RESOLUTION selector is switched to the 30 kHz position. Pin 3 of P830 is pulled low when the RESOLUTION is switched to 3 kHz or 300 Hz position.

The three sections of U830 and one section of U840 are connected to operate as an AND-OR gate. When the video filter selection switch is closed, one section of U830 is turned on to connect C830 in the feedback loop. Closing both S90A and S90C (300 Hz and 30 kHz) turns two sections of U830 and one section of U840 on. This connects C830, C832, and C840 in the feedback loop. The following logic describes the three filter combinations:

30 kHz = (30 kHz RESOLUTION) OR (3 kHz to 300 Hz RESOLUTION) OR (C90C closed).

300 Hz = (S90A closed).

10 Hz = (S90A) AND (S90C closed).

The output of U820B is isolated from summing amplifier U820C by Op Amp U820D. U820C sums the video signal with the dc level set by the vertical position control plus the search marker, when present. The output of U820C drives the positive output for the oscilloscope interface, the inverting amplifier U820A (which drives the negative output to the oscilloscope interface) and the Baseline Clipper circuit.

The Baseline Clipper circuit consists of a common emitter current switch (Q887-Q890) and a logic circuit (Q895-Q898) that modulates the Z Axis switching circuit. The Z Axis switching circuit consists of a current switch (Q2320-Q2330) that is controlled by an exclusive OR gate (Q2335 and CR2336). The output of the current switch drives the Z axis common (pin B17) and the Aux Z axis (pin A17).

Q2335 with CR2336, operate as an exclusive OR, to gate the state of either interface pin B7 (channel switch) or A16 (mode info) to the base transistor Q2330. When this state is high, Q2320 is switched on and positive current through the interface pin A17 (High) reduces or clips the crt beam intensity.

The CONTRAST control sets the quiescent current through CR898 which establishes the contrast between the clipped and unclipped portions of the display.

The amount of current through Q2320 or Q2330 is a function of the Baseline Clipper logic circuit. The common emitter current switch Q887-Q890, switches transistor Q898 off when Q887 is on. Composite video from U820C will cause the circuit to switch at some level set by the BASELINE CLIPPER control R96. When Q890 switches on, Q898 is switched on increasing the current through Q2320 to decrease the crt beam intensity.

The BASELINE CLIPPER control range is about 100% of the display amplitude.

## Frequency Readout 

The frequency readout system looks at the frequency tune control voltage and outputs both a standard readout signal for the mainframe, and a LED readout for the frequency indicator on the 7L14. The system consists of a digital voltmeter, drivers for multiplexing the LED readout, and an A to D converter to drive the mainframe readout circuits. Fig. 3-3 is a basic functional block diagram.

The DVM is a precision oscillator. An integrator is ramped up and down by switching its input currents. These input currents are switched by commands from a digital counter and an analog comparator. During one transition, the count is loaded into latches. This number is then displayed during the next transition.

The integrator generates an output ramp with a timing sequence proportional to the dc level set by the tuning potentiometer for the 1st LO. The comparator generates a step signal output when the ramp signal crosses a reference voltage which triggers the multivibrator.

The counter counts towards 20,000 during the run-up time of the ramp. When the output of the comparator steps positive, it triggers the flip-flop which loads the count into the latch and also shifts its number into decoders and drivers for the LED readout. The new state of the flip-flop also switches the reference current off and the output voltage of the integrator ramps down towards 0 volts.

Referring to the schematic diagram 20, the voltage output of the amplifier U2110 is proportional to the input voltages at pins 2 and 3. The voltage at pin 3 is from the tuning potentiometer, and ranges from about −9 volt to +9 volt. An offset voltage can be summed in with this tuning voltage, for calibration, by adjustment R2135.

Reference current for the integrator U2140, is supplied by a buffered operational amplifier U2120 and Q2120. An input reference voltage of 11.7 volts to U2120 is set by Zener diode VR2115. This sets the current output of Q2120 to a value that is independent of the signal voltages. The current from this source is steered either to the input of the integrator, or to the power supply by diodes CR2130, CR2132, and CR2134.

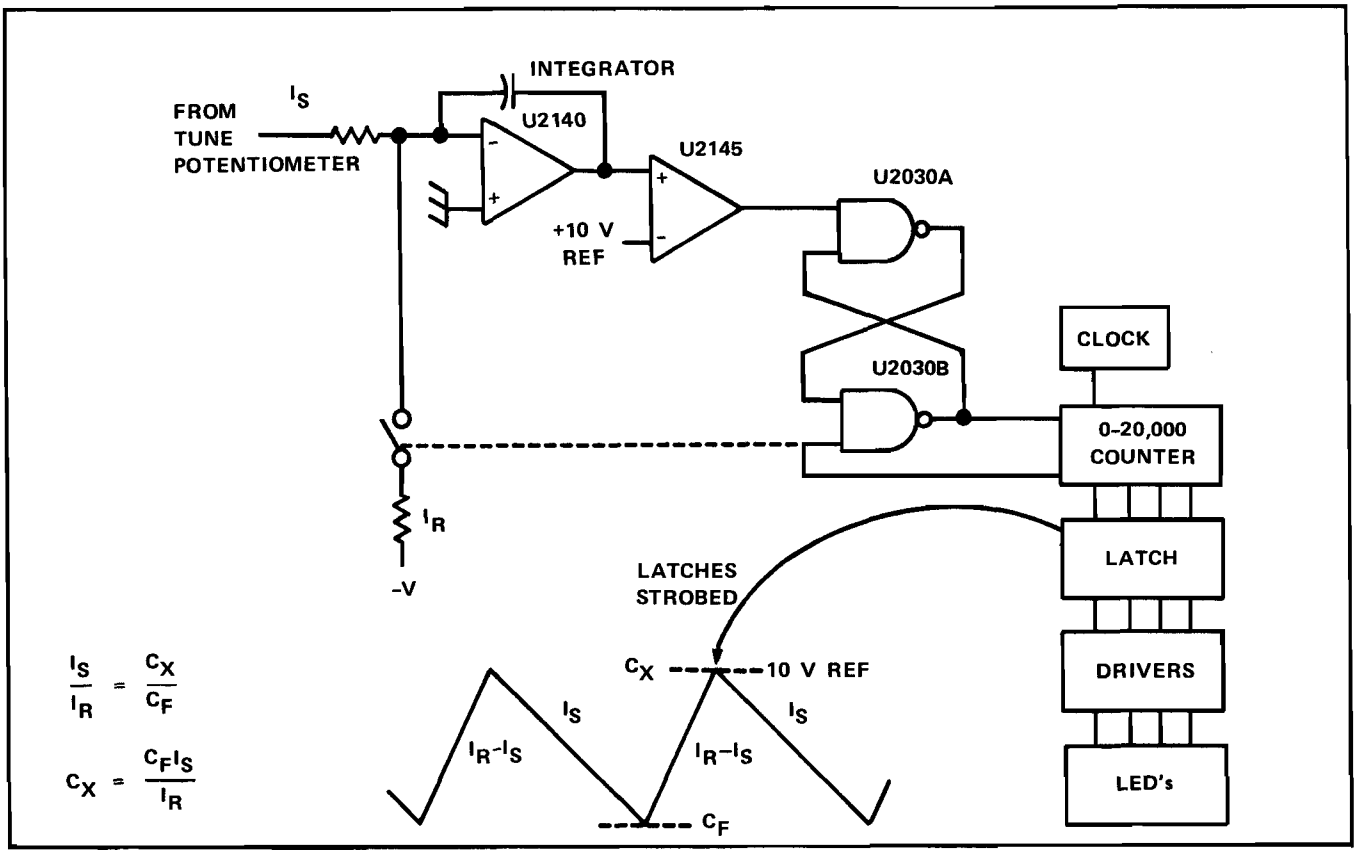



**Fig. 3-3. Functional block diagram of the frequency readout circuit.**

The voltage state of pin F is set by the multivibrator U2030A, U2030B in the digital section of the DVM. When the state is low, CR2132 and CR2134 are off and reference current is steered through CR2130 to the input of the integrator. When the state is high, the diodes are turned on to steer the reference current through R2147 to the power supply.

As indicated in Fig. 3-3, the reference current is larger than the signal current so the output of the integrator is a positive-going ramp when it is summed with the signal current. When the reference current is switched off, the output of the integrator is a negative-going ramp.

The reference voltage source for the comparator U2145, is the output of operational amplifier U2130. The 11.7 V Zener diode VR2115 sets this output at a very stable 11.7 V. This source provides the reference for the offset current through R2135 and the reference for the negative input of the comparator U2145.

As the positive-going ramp from U2110 crosses the reference voltage, the output of the comparator steps high. This triggers the multivibrator U2030A, U2030B and the voltage at pin F goes high to turn diodes CR2132 and CR2134 on. The output of the integrator swings past the reference voltage a slight amount before it starts negative. When it again crosses the reference potential, the output of the comparator switches low.

U2015, in the digital section of the DVM, is a 0 to 20,000 counter and latch. When it counts to 20,000 or 0, pin 18 goes high. This high is fed back through two inverters U20000B and U20000C to reset the flip-flop. The resultant low on pin F turns diodes CR2132 and CR2134 off. The reference current is again summed with the signal current and the cycle repeats. The slope of the positive-going ramp determines the time required for the voltage to reach the reference that determines the count of the counter.

The clock input to the counter U2015 is generated by oscillator Q2005-Q2010. The output of the oscillator is applied through emitter follower Q2015, to pin 1 of U2015. The digit output on pins 4,5,6, and 10 is in binary format. The count in the latch of U2015 is transferred, when the latch is strobed, to a BCD-to-7 segment decoder (U2020) and through inverter drivers (U2000A, U2000D, U2000E, and U2000F) to a digital-to-analog converter U2065. The converter sums the digital current input and provides column sense data (at pin 19) for the readout circuits of the mainframe.

The digits are displayed sequentially. The seven digit code for the LED's is applied from decoder U2070; however, only one digit lights at a time. The command to light each digit is sent out on pins 8, 7, 17, and 22 of U2015, to LED DS2075. The clock pulse that strobes the display command from one digit to the next is applied to pin 11 of U2015 from NAND gate U2030D. When a time slot goes low, the clock continues to strobe the counter from one digit to the next (1, 10, 100, 1000) until the corresponding digit display command is gated through AND-NOR gate U2040. At this time the clock signal through the NAND gate U2030D is blocked and the column sense signal current is sent from pin 19 of the D to A converter U2065, to the mainframe readout.

One unit of current differential exists between the LED readout and the mainframe. Resistors R2020, R2026, R2133, and R2137 are connected between the respective time slot line and the sense line to add an additional unit of current for the mainframe readout circuit.

## Uncal Circuit ◈14◈

Reference level calibration of the display depends on the combination of frequency span, resolution bandwidth sweep rate, and video filter bandwidth. It was determined from the amplitude loss factor equation

$$\propto = \left[1 + 0.195 \left(\frac{D}{tB^2}\right)^2\right]^{-1/4}$$

that the display is calibrated when the combination of the above parameters cause the equations

$$\frac{\text{Freq Span}}{0.5\ (\text{min B, V})\ (B)\ (t)}$$

to equal or exceed 1, where

min B, V = minimum bandwidth of either the resolution or video filter

B = Resolution bandwidth

t = Sweep time

The multiplication and division of quantities in this equation can be done by summing the logarithm of the various parameters. The equation becomes:

$$\log(\text{freq apan}) - \log(0.5) - \log(\text{min B,V}) - \log(t) \geq 1$$

By normalizing these parameters so each term is equal to or greater than zero, the equation becomes:

$$-\log\left(\frac{200 \times 10^6}{\text{Freq Span}}\right) + \log\left[\max\left(\frac{10^6}{B} \text{ or } \frac{10^6}{V}\right)\right] +$$

$$\log\left(\frac{10^6}{B}\right) - \log\left(\frac{t}{5 \times 10^{-3}}\right) - 1.097 \geq 0$$

The logarithmic summation of these parameters is performed by an analog circuit and compared against ground or zero. The resultant indicates if the display is uncalibrated or calibrated. Fig. 3-4 illustrates the basic uncal circuit.

## Sweep Triggering, Sweep Generator and Horizontal Amplifiers ◈11◈ ◈12◈ ◈13◈

The sweep ramp is generated by U1170 when it is gated on by a positive gate signal from U1180. U1180 can be triggered, or it will automatically recycle after an RC time interval (set at pin 12) to provide a constant baseline.

Triggering for the sweep generator circuit is supplied from one of three sources which are selected by S101. The selected trigger signal is applied to the input of an operational amplifier U1010B. The output of U1010B is summed with the dc level set by the LEVEL control R100. When the triggering signal amplitude exceeds this dc level, CR1038 is switched on to generate a positive trigger signal for the trigger input to U1180. The following occurs as each source is selected: 1) EXT connects the EXT IN HORIZ/TRIG connector to the input of operational amplifier U1010B. 2) INT selects the output of a differential amplifier U1010A, which receives its trigger signal from the mainframe interface. 3) LINE selects a sample of the line voltage from the mainframe interface and applies it to the input of U1010B. FREE RUN (a triggering mode) grounds the input of U1010B, which sets the output of U1010C to approximately 0 V and the input to pin 4 of U1180 low (approximately −0.7 V). The gate generator free runs when pin 4 is low.

The positive gate out of U1180 provides the signal for the sweep generator U1170. The negative gate is amplified and inverted by Q1230 to provide the unblanking gate for the crt. Pin 15 goes high at the end of the sweep gate and gates a holdoff pulse through U1160A, U1160B and Q1160 to the mainframe interface.

Current for the SWP indicator light DS1152, is supplied by transistor Q1150. During gate time, in the SGL SWP mode, the lamp drive from U1180 goes low. This gates a low out of U1160B to turn transistor Q1150 on. In the SGL SWP mode, pin 6 of U1180 is grounded so the gate generator will not run until it has been reset by pushing the Start button and gating a signal through the NAND gate

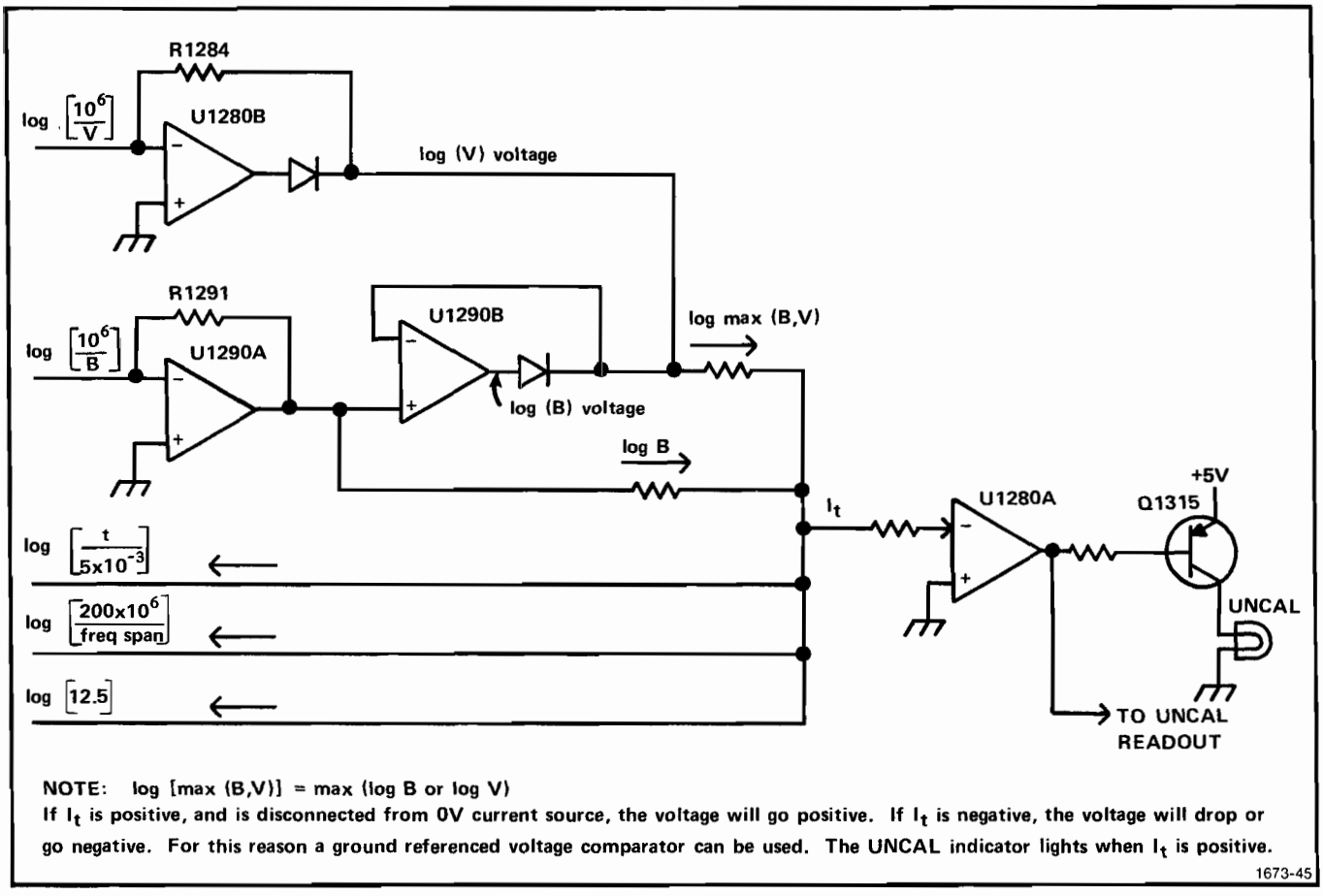



**Fig. 3-4. Basic functional block diagram of the uncal circuit.**

U1160C to trigger Q1120. This pulls pin 7 of U1180 high and resets the gate generator so it recycles.

U1170 generates a sweep ramp of 10 V, with a duration that depends on the timing current into the summing point at pin 9. The timing current for the capacitors C1173, C1174, and C1175 is supplied through timing resistors R1220, R1221, R1222, and R1224 by operational amplifier U1120A. Timing combinations are switched into the circuit by the TIME/DIV selector S104.

The dc level at the input to U1120A is adjusted by R1200 to compensate for offset of the IC U1170. The jumper across P1200 permits a step compensation when U1170 is replaced and the offset is outside the range of R1200.

Pin 6 of P1160 is an input from a tracking generator. When this input is high, Q1215 and Q1216 are turned on. Q1216 shunts the integrating current for U1170 from U1120A to ground. Q1215 sets the sweep output line to a dc level that represents center sweep. R1215 adjusts or calibrates this offset dc level of the sweep integrator in U1170 so the crt beam is centered during the input signal period from the tracking generator.

The sweep output of U1170 is connected through cam 29 of S104, to the output amplifier U1050A. U1050A drives U1040D and both amplifiers supply approximately 0.5 V of push-pull drive to the mainframe deflection circuit. Gain of U1050A is set by SWP CAL adjustment R107. U1050C provides a sweep to the mainframe for sweep logic, which provides the + Sawtooth Output at the front panel of the 7000-Series oscilloscope.

## Digital Storage ◈15◈ ◈16◈

Digital Storage provides the operator with the capability of selecting the method for displaying and processing information contained in the digital storage memories. This allows operations such as determining the highest amplitude that occurred during a selected period (MAX HOLD mode), storing a signal for later examination (SAVE A mode), subtracting one signal from another (B–SAVE A mode), and comparing signals (DISPLAY A, DISPLAY B modes). Two memories are used independently in these operations to store two complete signals that are each digitized at 512 points across the sweep. Thus, two signals may be observed simultaneously or processed in various ways.

In MAX HOLD mode, the highest amplitude at each of the 1024 points in successive sweeps is stored and displayed. In SAVE A mode, a signal is stored in one memory for later examination, and is not updated. In the B–SAVE A mode, the A signal is stored and not updated, then arithmetically subtracted from the B signal, which is stored and continually updated. In the AVERAGING mode, the display area is divided by a horizontal cursor. Above the cursor, signals are peak detected and displayed; below the cursor signals are averaged. In the DISPLAY A and DISPLAY B modes, the contents of the selected memory or memories are displayed.

Graphical presentation of mathematic functions or experimental data is common today. One class of such graphs is those that have a single Y value for each X value. An alternate presentation of the data in this graph would be a table in which the X coordinate values were simply listed along with a corresponding Y value for each X value. In further simplification, if the first X value and the spacing between X values (assuming that all spacings are equal) were known, the two column table could be reduced to a single column with the X value implied by the position of the Y value in the column. This then is the essence of digital storage: to convert a vertical analog voltage (Y coordinate value) to a binary number and insert that number in a stored table. The location of the Y value in the table is determined by converting to binary the analog sweep voltage (X coordinate value). Once the table is created by storing a set of binary numbers respresenting values across a waveform, the waveform can be recreated at any time by converting the table values (Y) and positions (X) back to analog voltages representing amplitude and sweep position.

The digital storage system used in the 7L14 uses two tables: A and B. Table B is always updated on every sweep. Table A is changed unless SAVE A mode is selected. There are 512 A values and 512 B values. The spacing between values is the same throughout both tables, but the starting point for table B is shifted slightly so that, when both tables are being read, the read-out values are interlaced.

When the signals are recreated, the operator has the option of displaying either A or B, or both A and B. If both are to be displayed, and SAVE A mode is also selected, the contents of both table A and table B are drawn, each display in its own trace. If SAVE A mode is not selected, the contents of both table A and table B are displayed on one trace, with 1024 value positions across the screen. A third trace option is also available. In the B minus A mode, the displayed values are those resulting from an arithmetic operation and are the difference between the contents of table A and table B for each X value of analog sweep voltage.

Since a signal waveform is continuous and a table has discrete X values, an algorithm is used to determine the Y value to be stored for a particular X value. This allows the operator to select one of two methods for determining Y values: peak or average. The Y analog voltage is continually sampled, with the sampling rate dependent upon sweep speed. For each X value, there are always at least two samples and there may be as many as $2^{17}$ samples. From this set of samples then, the user may select either the largest sample value (peak value) or the mean of all of the samples (average value). Selection between peak and average is controlled by the front-panel PEAK/AVERAGE control, which sets a dc level that is compared with the analog vertical input to produce the PEAK/AVERAGE logic signal. When the input signal is below the level selected by the front panel control, the signal is averaged; when the input is above that level, the peak signal is displayed. The dc level appears on the display as a positionable horizontal line. This marker line is created by switching the dc level to the analog output line during the marker cycle to produce the MARKER logic control signal.

Superimposed on the marker line is an intensified spot called the UPDATE MARKER, which indicates the X value at which new Y values are being computed for display update. The update marker is formed by comparing the analog sweep input to the display analog X output. When the two are the same value, the sweep is forced to pause, thus increasing the marker intensity at that point.

Central to the 7L14 digital storage system are two specially designed and manufactured IC's; U2045 and U2020. Vertical section IC U2045 contains the vertical acquisition and display logic, peak detection, signal averaging, Z axis blanking, and special Y-value processing circuits. Horizontal section IC U2020 contains the horizontal acquisition address counter, horizontal display counter, 10-bit RAM address multiplexer, and a programmable logic array system control matrix. The remainder of the digital storage control circuits consists of two 8-bit digital-to-analog converters, two 10-bit digital-to-analog converters, one 10-bit latch, 8k bits of random access memory, and various ancilliary circuits.

### Vertical Section ◈15

The input video signal is applied to input buffer U3084, which amplifies the video signal to the level necessary for proper operation of the digital storage. The buffered video signal is applied to sample and hold U4084, which is used as a peak detector. Whenever the input video signal exceeds the output of U4084, a sample pulse is generated for U4084 by comparator U3079B and gate U4032, thus performing a peak-detecting function. A sample pulse is also generated by the ST DIVIDE signal for U2020, which serves to reset the peak detector at the beginning of each sweep. The peak detector is disabled whenever the video signal is below the level set by the peak average/baseline clipper level.

The output of peak detector U4084 is applied to sample and hold U3092, which is controlled by flip-flop U1058A. Flip-flop U1058A generates the sample pulse, and is enabled during the clock cycle after the last sample, as indicated by the least significant bit from the successive approximation register in U2045. The sample is then applied to a summing junction, at which point the output current from the digital-to-analog converter, which is supplied from the successive approximation register, is subtracted from the sample current. The difference current is applied through comparator U2063 to pin 18 of U2045 as the UP/DOWN signal. Thus the combination of the successive approximation register, the digital-to-analog converter, and the sample and hold circuit effectively produces the binary equivalent of the input sample.

The peak average/baseline clipper from the front panel is scaled to 0-5 V by buffer U3086A. This voltage is then compared to the buffered video signal to determine the state of the peak-average line. The peak-average line is gated into peak register of U2045 by the valid data line. When the peak average input of U2045 is high, the M180 will store the peak data taken during this time. Flip-flop U3032 is used to determine when data is valid. U3032 is cleared at power-up and at the end of each sweep. It is set at the start of the sweep by the ST DIVIDE line, which originates from U2020.

The vertical analog voltage is converted to a Y binary value using an 8-bit successive approximation register. Nine clock cycles are required for each Y conversion. After the conversion has taken place, the successive approximation register produces the negative-going SYNC signal. Most functions on both the vertical and horizontal control IC's are synchronized by this signal. On the negative-going transition of SYNC, the successive approximation register is reset to 10 00 00 00 (binary) and the next conversion cycle begins. Incoming data bits are latched into the successive approximation register on the negative-going clock transition. From the register, the output data are applied to the peak and the averaging circuits.

The averaging circuit consists of three groups of circuits: those that accumulate the grand total of all of the Y values for a given X value (this total is called the numerator), those that count the number of samples that make up the numerator (this total is called the denominator), and those that subtract and shift to perform the division process.

As each new Y value is converted, it is added to the eight least significant bits of the numerator. Each carry from the most significant bit of this addition is counted by a 17-bit ripple counter. The contents of this counter and the 8-bit sum are cascaded to form a 25-bit grand total. Each time a new sample is added to the numerator, a second 17-bit ripple counter is incremented to produce the denominator.

A division cycle is initiated when the horizontal control IC U2020 detects a change in the X value. At that time, U2020 produces the ST DIV (start divide) signal. Upon receipt of this signal, and in synchronization with the SYNC signal, vertical control IC U2045 performs several functions: 1) It latches the current numerator in a 25-bit latch, and latches the denominator in a 17-bit latch. 2) It clears the numerator adder circuits. 3) It performs a 17-bit priority encode on the denominator and loads a 1 in the appropriate cell of the 25-bit shift register. 4) It loads the latched numerator and denominator serially into the divide circuit, using the contents of the 25-bit shift register as a mask. 5) It clears the denominator ripple counter to zero.

Ten clock periods are required to load the numerator and denominator into the divide circuit. The cycle starts on a SYNC pulse and the first bit of the quotient is available shortly after the first clock pulse following the next SYNC pulse. Division is performed by repeated subtract and shift operations. The quotient is arrived at serially with the most significant bit first. Only 8-bit accuracy is required, so, by using the priority encoder output as a mask, the divider circuit is loaded with the 8 most significant bits of the denominator and the 16 most significant bits of the numerator. (Ripple borrow for a 17 by 25 bit subtractor would be so long as to be impractical.)

The peak circuit consists of a peak detector and an 8-bit peak shift register. In operation, the previous peak Y value from the last set of samples is still stored in the peak shift register at the start of a conversion cycle. At that time, the peak detector, which is a serial compare circuit, is set to the state that will question whether the old or new number is larger. Each bit of the new value is then compared with the corresponding bit of the old value, most significant bit first. When one value is found to be larger, a flip-flop is set and the smaller number is gated out of the shift register. The start divide logic signal being true then forces the peak detector to select the new value and ignore the number in the shift register.

The peak/avg selector, a multiplexer, selects either the peak or average value to be routed to the memories under control of the PEAK/AVE signal. The selector output is routed through the max hold circuit, which functions in the same manner as the peak detector. When the MAX HOLD signal is high, the value that is routed to the output multiplexer is the larger of two values: the current memory value at the subject X coordinate or the previously selected peak or average value.

Timing for setting up the divide operation and cleaning the numerator, denominator, and peak circuit is controlled

by a 10-stage Johnson counter. NOR-gate taps are taken from appropriate stages to develop the necessary clear and latch timing pulses. Because the denominator is loaded into the divide circuit using a priority encoder, the most significant bit is always a 1. Space and power were saved by modifying the subtractor and not storing this 1.

All data enter and leave the memory serially. Data read from memory enter an 8-bit shift register, and timed by SYNC, are transferred to the vertical display output latch (display register on the block diagram). The same shift register is used for other purposes, so the DISPLAY ENABLE signal prevents non-display information from being transferred to the output latches. An example of data moving through this shift register is that during the B minus A display mode. The A value is first read from memory and stored in the shift register. As the B value is ready, the subtration is done serially and the answer is applied to the shift register. Since the subtraction must be performed least significant bit first, a set of exclusive-OR gates change the order of extracting B from memory. The direction of shift for the shift register is reversed also to present the most significant bit to the proper display latch. The shift register output is also applied to the output multiplexer.

In the subtraction, the operation performed by the serial calculator is not merely B minus A. The actual expression implemented if (B-A) + K, where K is a serial input external constant specified by the user. This permits zero to be placed anywhere on the screen. To avoid confusion, when (B—A) + K results in an off-screen position, the subtractor blanks the display. This is done by examining the carry bit and borrow bit when the most significant bit is calculated. If either bit is a 1, the screen is blanked.

When SAVE A mode is not selected and both A and B are being displayed, maximum resolution is obtained (1024 points across the display). If this display includes a very narrow pulse, it is possible that the top of the pulse is only as wide as a single X coordinate (2 to $2^{17}$ samples). If this maximum value were in the B table and SAVE A mode were selected and B turned off, there would be an apparent drop in amplitude. For this reason, when SAVE A mode is selected, a special set of circuits in U2045 compares all A and B values that have the same X value and stores the larger in table A. This is accomplished by first reading the B value and storing it in the display shift register. Then, as the A value is read, it is compared with the B value and the larger of the two is loaded into the display shift register. Finally, the number in the shift register is written into memory from the shift register. This operation is performed once each time that SAVE A mode is selected.

Vertical control IC U2045 also contains a 3-bit synchronous counter that identifies the specific bit of an 8-bit vertical value that is to be read from memory or written into memory. This is the only memory addressing that is performed by the vertical control IC. All other addressing is under control of the horizontal control IC (U2020).

**Maximum Hold.** As described previously, when MAX HOLD mode is selected, circuits in U2045 compare the binary equivalent of the input signal for a given X value with the information in memory for that same X value and cause the larger of the two to be stored in memory.

**Constant Circuit.** As described previously, in the B minus A operation, a constant is used. This constant is internally selectable with switch S1046. This switch, in combination with multiplexer U1028, supplies the constant to U2045. Multiplexer U1038 is in turn controlled by address bits 0, 1, and 2 to provide the proper switch signal to U2045.

**Output Circuits.** From the U2045 vertical display register, the parallel data output is applied to 8-bit digital-to-analog converter U2052. The converter output is then applied through a vector generator, consisting of an integrator (U2072 and C1086) with an associated feedback loop sample-and-hold circuit, to the output storage/cursor switch. Integrator U2072 has a time constant that provides a ramp lasting between the existing sample and the new sample (that is, between sync pulses). Sample and hold U2088 retains the last sample.

From U2088, the output current through resistor K1084 subtracts from the digital-to-analog converter output current to modify the slope of the output ramp. The output of the vector generator is then applied to switch Q3072 and Q2069 which selects between the stored data and the marker under control of the buffered PK/AVG LVL (peak/average level) control signal from U3052, and supplies the output to the horizontal circuits.

## Horizontal Section 

The horizontal analog voltage is converted to a current table value through the use of a 10-bit tracking analog-to-digital converter, which consists of a 10-bit up/down counter (U2020) and an external 10-bit digital-to-analog converter (U2012). As the sweep moves to the right, the counter increments; as the sweep retraces, the counter decrements. Each time the counter increments, a new X coordinate value is generated (the digital-to-analog converter output) and a ST DIV (start divide) signal is generated to start the storage cycle. The increment clock is the SYNC signal, the decrement clock is the basic 0.9 MHz clock divided by two. When SAVE A mode is selected, the counter skips every other binary number. Thus, only B coordinates appear as addresses.

Intelligence for the horizontal system is provided by a programmable logic array ROM state device (PLA). This PLA determines which trace is to be written on the screen, determines when to switch from read to write, generates the B-A coordination signals for vertical control IC U2045 and controls the incrementing of the 9-bit display counter.

The combination of the 10-bit up/down register, 9-bit display counter, and horizontal display multiplexer constitute the primary circuits that: 1) convert the sweep voltage to binary form to generate X values to be written into memory, or 2) read the X values from memory by counting sync cycles and causing the external logic to read stored data from memory and produce a vertical signal (Y value) for each corresponding X value. During acquisition cycles, the 10-bit up/down counter operates in a loop with the external 10-bit digital-to-analog converter to derive the equivalent (X value) of a sample section of the sweep voltage. From the counter, the 10-bit output is applied to the 10-bit up/down register. During display cycles, the 9-bit display counter counts sync pulses to derive the X value. Either the 10-bit up/down register output or the display register output is applied to the horizontal multiplexer under control of the SELECT signal from the PLA. From the multiplexer, the output is applied to the memories.

**Tracking Analog-to-Digital Converter.** As discussed previously, the 10-bit digital-to-analog converter operates as part of the loop that derives a binary equivalent of the SWP (sweep) input signal from the Sweep board. Converter U2012 accepts the output from the 10-bit up/down counter and converts that output to an analog current that is subtracted from the sweep signal, which is applied at connector pin K and through buffer U4024B. The result of this subtraction is then supplied to up comparator U4022B and down comparator U4022A to produce the UP or DOWN signal, as appropriate to control the direction of the count of the 10-bit up/down counter in U2020. The counter then counts in the appropriate direction, thereby changing the digital-to-analog converter output to reflect the proper value.

From buffer U4024B the sweep is inverted and added to the STORE HORIZ sweep (U2082). Comparator U3052A uses this to detect a zero crossing. This output triggers one-shot U3034. When the output of U3034A goes high, the the MARKER signal is also high, the 9-bit display counter in U2020 is stopped and the STORE HORIZ sweep terminates for the duration of the pulse out of U3034A. When the sweep is stopped, it generates an intensified spot on the display.

**Fast Retrace Blanking.** Between the display of the B memory contents and display of the A memory contents, a fast retrace occurs. This retrace, unlike that following the A memory display (cursor), is not required to be seen and is thus blanked. This is accomplished by blanking control one-shot U3034B which is controlled by the most significant bit of the memory address and the display enable signal during a marker cycle.

**Memories.** Integrated circuits U1010 and U1026 provide 8k bits of random access memory for storage of the 1024 data points used in the digital storage system. Addressing is controlled by horizontal control IC U2020.

## Reference Level Readout ◈19◈

The Reference Level Readout circuit receives attenuator and gain setting information. With the gain information, it sets the gain of the instrument in steps of 10. It also calculates the reference level, depicts it on LEDs on the front panel, and provides appropriate current for the crt readout.

Nine discrete gain steps (0 to 80 dB) of the IF Gain selector generate a four-bit word for multiplexer U2880, which sets the four output lines according to the state of its control lines, or a predetermined condition. The predetermined condition is when U2880 pin 6 or 3 is high, and P5 Pin 4 is high; this causes U2880 pin 1 to go low, giving a high output at pins 12 and 19 and a low output at pins 7 and 4. This condition occurs to prevent exceeding 30 dB of gain when in 10 dB/Div, which would permit invalid reference levels.

The four output lines from multiplexer U2880 control the gain and provide reference level information. Reference level ROM U2885 takes the attenuator information plus the gain information and selects the reference level. Gain control ROM U2890 takes the four gain control lines plus a fifth line with the status of the 30 Hz filter from P7-2 (line is −15 V when the filter is on) and controls the gain in the analyzer through P84 pins 1 and 5 and P83 pins 1 and 2. One of the lines is buffered by transistor Q2880. A line also goes to P7-1 to control the 110 dBm reference level step, which provides 80 dB gain (−15 V on the line tells an amplifier to add 10 dB of gain). This position is valid only when the 30 Hz filter is in, and the amplifier is at the 70 dB gain position.

The output of the reference level ROM U2885 is on lines B1 through B8, which go to the other two boards. Four of the lines (B1 through B4) control the third digit; the fourth digit is hard-wired (in U2800 and U2802) so that it is always zero. Integrated Circuits U2800, U2802, U2804, and U2808 multiplex the display; U2815B, U2815C, and U2815D form a clock oscillator. U2804 is a divide-by-four circuit whose two output lines Q1 and Q2 provide four logic states: 00, 01, 10, and 11. U2808 decodes these lines to sequentially turn on each digit. U2800 and U2802 decode the reference level lines to provide the inputs to the BCD-to-seven segment decoder/driver, U2806.

The reference level outputs of U2885 also control the crt readout by switching the appropriate currents through analog switches U2820 and U2830, via buffers Q2825 through Q2850. Q2895 and Q2896 function as a wired AND gate to turn off Q2855, and hence all current gates, when the reference level is 0 dBm. U2878 and CR2878 function as a −6 V regulated supply for Q2855.